Contents

List of Figures

List of Abbreviations

ADC	analog-to-digital converter.
ADDLL	all-digital delay-locked loop.
ASIC	application-specific integrated circuit.
CLB	configurable logic block.
CMOS	complementary metal–oxide–semiconductor.
DAC	digital-to-analog converter.
DCDL	digital-controlled delay line.
DLL	delay-locked loop.
DNL	differential nonlinearity.
DS	dual sample.
FF	flip-flop.
FLIM	fluorescence lifetime imaging microscopy.
FPC	four-phase clock.
FPGA	field programmable gate array.
INL	integral nonlinearity.
LiDAR	light detection and ranging.
LSB	least significant bit.
LUT	lookup table.
PLL	phase-locked loop.
PVT	process, voltage and temperature.
RAM	read access memory.
RBC	reflected binary code.
RMS	root mean square.
RO	ring oscillator.

TDC	time-to-digital converter.
TDL	tapped delay line.
ToF	time-of-flight.
VCDL	voltage-controlled delay line.
WU	wave-union.

Chapter 1: Introduction

This chapter provides an overview of the context, motivation, objectives, and methodology of this dissertation. It begins by discussing the applications of all-digital time-to-digital converter (TDC) and providing a brief review of the different platforms that could be used to develop such system. The motivation for the project is then presented, outlining the problem that the author seeks to address. To ensure that all of the planned results are achieved, the project objectives and methodology must be established. Finally, this chapter concludes with a description of the dissertation document structure.

1.1 Contextualization

Precise measurement of time elapsed between two event or time pulses is an essential requirement for many science and engineering applications. Time-to-digital converters are extremely high-precision stopwatches which convert time domain information into a digital representation. They represent the fundamental building blocks between the continuous time domain and the digital world.

All-digital phase-locked loops (PLLs) were the first TDC application. PLLs are feedback systems that generate signals phased locked with external input signals where a TDC serves as phase detector [1]. TDCs are used in applications where precise time interval measurements are required. They have been applied for a long time in the nuclear and particle high-energy physics field [2]. Other applications cover space sciences [3], biomedical applications, such as positron emission tomography and fluorescence lifetime imaging microscopy (FLIM) [4], and time-of-flight (ToF) measurements thus light detection and ranging (LiDAR) systems [5].

Among other applications, LiDAR imaging systems play a key role in autonomous vehicles. The Society of Automotive Engineers currently defines six levels of driving automation ranging from Level 0 (fully manual) to Level 5 (fully autonomous) [6]. These levels have been also adopted by the U.S. Department of Transportation. Although being relatively new in automotive markets, the vehicle surrounding mapping advantages offered by LiDAR, when compared to other technologies, have propelled massive innovations. LiDAR imaging systems are a novel type of sensor which enable complete three-dimensional perception of the environment, and not just the two-dimensional projection obtained from a camera. A combination of radar, video cameras, and LiDAR with deep learning procedures is the most likely solution for a vast

majority of cases [7]. Thus, LiDAR will be at the core of this revolution.

LiDAR sensors bounce pulses of light off the car's surroundings to measure distances, detect road edges, and identify lane markings [7]. This working principle is illustrated in Figure 1.1. Companies previously established in the field are being acquired by large industrial corporations, mainly from the automotive industry. This activity is due to the lack of an adequate solution in all aspects for LiDAR image systems for automotive either because performance, lack of components, industrialization, or cost issues [7].

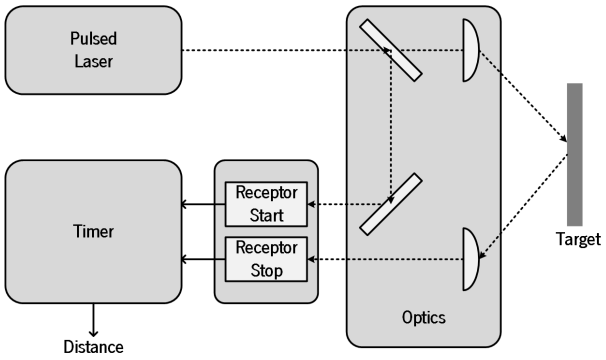

Figure 1.1: Pulsed time-of-flight measurement principle (adapted from [7]).

TDCs can be divided into two categories based on their operating principles. Analog TDCs convert a time interval into a voltage, which is then digitized by an analog-to-digital converter (ADC). These TDCs have good resolution and linearity, but they also have high-power dissipation, large size, low scalability, and high susceptibility to noise. All-digital TDCs, on the other hand, can simultaneously achieve high resolution and wide dynamic range, with small area and low power dissipation [8]. Due to these advantages, all-digital TDCs are currently the most attractive approach to most applications.

All-digital TDCs are primary implemented either using application-specific integrated circuit (ASIC) or field programmable gate array (FPGA) devices. The requirements for price, reproducibility, and suitability for mass production differ depending on the application. Over the years, the performance gap between FPGAs and ASICs has been narrowed due to the constant development of FPGA technology, including the fabrication process and development tools technology [9]. This has made FPGAs a viable option for final products, rather than just prototypes. The high performance,and lower development cost and time to market make FPGA-based systems attractive to different applications, including TDCs. As a result, FPGA-based TDCs have become increasingly popular in recent years.

1.2 Motivation

The main key performance indicators of TDCs are the measurement range, resolution and precision, nonlinearities, dead-time, power consumption and resources usage. Much research has focus on increasing resolution of TDCs; however, nonlinearities can have a direct impact on the overall system precision. Process, voltage and temperature (PVT) variations are one of the main causes of TDC nonlinearities. A high-stability power supply and temperature control equipment can be used to control voltage and temperature variations, but this increases system cost and complexity. Therefore, a special correction strategy is needed to compensate for PVT variations without affecting TDC normal operation. This dissertation aims to develop such a calibration.

1.3 Objectives

The goal of this dissertation is to develop a high-resolution TDC with 20 ps resolution and 20 ps precision that is not heavily influenced by PVT conditions. To achieve this, several objectives must be pursued:

- Review the state-of-the-art in time interval measurement systems;
- Develop a high-performance time interval measurement system;
- Develop and integrate a calibration system to compensate PVT variations;
- Evaluate the performance of the developed architecture to understand its viability in different scenarios and how should the ToF measurement systems should be characterized;
- Evaluate the proposed architecture and compare it to the existing state-of-the-art TDCs.

1.4 Methodology

To focus and guide the activities involved in the research process that would enable the attainment of the proposed objectives, several research methodologies will be adopted during this dissertation:

- **State-of-the-art of TDC:** A review of the state-of-the-art of interval measurement systems will be performed to understand the different type of architectures that are being implemented and their

typical performances. This review will focus on FGPA-based TDCs, as they are the target application for this research.

- **Study the FPGA development framework:** To develop time interval measurement systems with a resolution under the clock frequency, a deep understanding of how the development frameworks are configure is required, as well as advanced knowledge of the FPGA platform being used. A study of the Xilinx Vivado framework will be conduct to learn how to avoid automatic optimizations on parts of the design and force the framework to generate specific hardware directly mapped to the FPGA configurable blocks. This study will also explore how manual placement and routing can be used to improve the overall performance of the time interval measurement system. In addiction, a study of the available FPGA platform resources and their configuration will be performed.

- **Evaluation FPGA-based TDCs:** The main metrics that need to be consider for proper TDC evaluation will be characterized. This include determining which tests need to be performed and how to conduct them. Code density tests to evaluate TDC's mean resolution and nonlinearities, performance measurements to obtain the TDC's precision and tests to analyze the TDC's performance variation with temperature will be the main focus of the evaluation.

- **Development of FPGA-based TDC prototype:** An architecture will be developed targeting a FPGA device with the goal of achieving the highest possible resolution.

- **Development of calibration system:** A calibration system will be developed to compensate PVT variations.

- **Characterization and integration of the developed TDC:** To compare the developed TDC with the existing implementations, a set of tests will be performed to evaluate the FPGA-based TDC. The architectures will be compared using the main TDC performance metrics.

Chapter 2: State of the Art

This chapter presents a review of the state-of-the-art, of ToF measurements using FPGA-based platforms. Unlike ASIC implementations, which do not have architectural limitations are imposed, FPGA implementations are beforehand restricted by the available cells.

In the literature, there is not a consistent FPGA-based TDC architecture categorization. Some publications use the circuit topology to classify the implemented TDC, while others use the principle of operation. To address this lack of convention, Machado et al. [10] proposed a standardized taxonomy. This taxonomy categorize TDC architectures based on their characteristics and topologies. Whenever there are changes to the main architecture in a research work, subcategories were created. This taxonomy does not include gray code TDC architecture, as it was not considered relevant at the time of publication. The proposed taxonomy with addiction of gray code architecture is illustrated in figure 2.1. The coarse counters group includes all the systems that have resolutions defined by the system clock period. The phased clocks group includes architectures that use multiple clocks with phase relationships. The tapped delay line (TDL) group includes all TDC architectures that use the intrinsic propagation delay of the FPGA cells as the interpolation element. The differential group includes all TDC architectures where the resolution is given by the difference between two elements. The pulse shrinking group included architectures that use the FPGA cells' rise and fall time discrepancies to build a delay-line loop that reduces the pulse duration at each loop cycle. Finally, the gray code group includes all TDC architectures that implement a gray code sequence where there is only a single bit transition between two consecutive states.

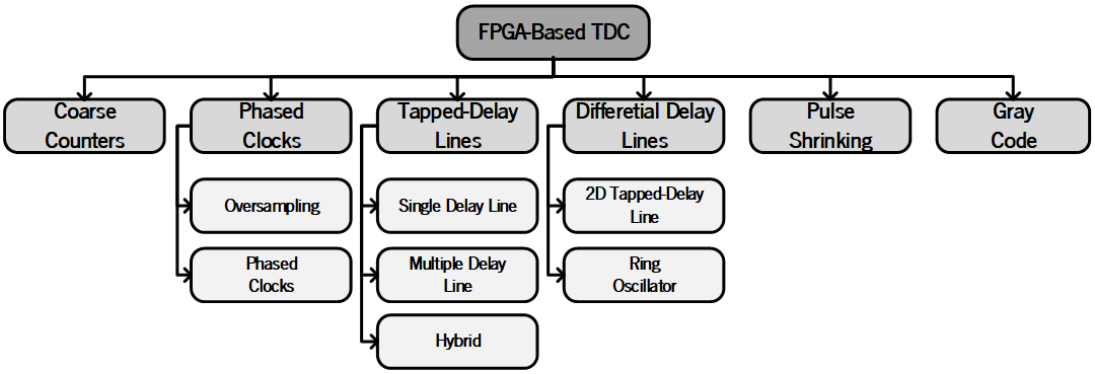

Figure 2.1: FPGA-based TDC architectures (based in [10]).

This chapter is structured as follows: in section 2.1, the main performance metrics used to evaluate TDC devices are described. In section 2.2, the most popular FPGA-based TDC designs are presented,

along with their principles of operation, advantages, and disadvantages. In section 2.3, self-calibration mechanisms that can be used to compensate for PVT variations in both FPGA and ASIC-based platforms are discussed. Finally, in section 2.4, gaps in the current state-of-the-art are identified and potential research directions are suggested.

2.1 Performance Metrics

Before analyzing and starting any discussion on the FPGA-based TDC state-of-the-art, it is crucial to identify and understand the key metrics used to characterize them, to properly evaluate their performance. These metrics will help to understand the advantages and disadvantages of the different TDC architectures.

2.1.1 Dynamic Range

Dynamic range is a measure of a TDC's maximum time interval that can be accurately measured before it overflows or becomes unable to provide accurate results. This metric is particularly important for applications such as time-based accelerometers [11] and LiDAR sensors used in avionics for geo-mapping [12], which require large measurement ranges and high resolution.

2.1.2 Resolution

The static input-output behavior of a TDC is determined by its quantizer characteristic, which maps continuous time intervals at the TDC input to discrete output values. This means that there is a range of time intervals that are mapped to the same output value [13, Chap. 3]. The resolution or least significant bit (LSB) of a TDC is the minimum amount of time that can be distinguished by the device, or the minimum step increment in its transfer curve.

2.1.3 Precision

The precision of a TDC is usually measured as a standard deviation and represents the error from the expect measurement. According to [8], the precision root mean square (RMS) value of a TDC, σ_{TDCrms}, can be calculated following equation 2.1, where σ_q is the quantization error, σ_{INL} is the TDC integral nonlinearity (INL) standard deviation, σ_{clk} is the jitter of the system clock, and σ_{extra} represents the contributions from the external sources of jitter.

$$\sigma_{TDCrms} = \sqrt{(\sigma_q^2 + \sigma_{INL}^2 + \sigma_{clk}^2 + \sigma_{extra}^2)} \tag{2.1}$$

The classic dynamic measurement of a TDC involves conducting a single shot experiment, where a fixed time interval is repeatedly applied to the TDC. In the absence of noise, each measurement should yield the same result. However, the presence of noise causes variations in the measured values. The standard deviation of these measurement values is called single-shot precision. It describes how reproducible a TDC measurement is in the presence of noise [13, Chap. 3]. Throughout this document, every time the term precision is used, it will be referring to the single-shot precision.

2.1.4 Nonlinearities

Nonlinearities in a TDC are defined as the deviations in quantization steps from its expected shape. PVT conditions are one of the main causes of nonlinearities. Other sources of nonlinearities include delay errors of the delay elements, signal crosstalk, and layout mismatch represent. The architecture and layout of a TDC can greatly affect the extent of nonlinearities [8].

The most common metrics used to measure TDC nonlinearities are differential nonlinearity (DNL) and integral nonlinearity. DNL describes the deviation of each step from its ideal value, while INL describes the deviation of the overall converter characteristic from its ideal shape [13, Chap. 3]. DNL provides a detailed view on the nonlinearities, while INL offers a more general overview. Usually, both DNL and INL are normalized to one LSB.

2.1.5 Dead Time

The measurement of a time interval is not instantaneous. The dead time of a TDC system is defined as the minimum time required to complete a conversion and be ready to perform a new measurement [10]. This characteristic determines the maximum measurement rate that the TDC can operate. The lower the TDC dead time the higher the sample rate.

To improve sampling rate, multiple TDCs in an interleaved scheme can be used [2]. This allows the TDCs to take measurements in parallel, effectively increasing the overall measurement rate. However, this approach also increases the complexity of the system and may not be feasible in all cases.

2.1.6 Power Consumption and Resource Usage

Power consumption of digital devices corresponds to the sum of dynamic power and static power. Dynamic power is associated with the clock operating system, while static power is related to the technology being used. In FPGA platforms, it is usual to refer to the resource's usage as a quantification factor of the amount of FPGA resources' utilization, which is tied to the FPGA's architecture being used.

It is important to carefully consider power consumption when designing digital systems, as it can have a significant impact on the overall performance and efficiency of the system. By optimizing the FPGA architecture and reducing resource usage, it is possible to reduce power consumption and improve the overall performance of the system.

2.2 FPGA-based TDC Architectures

In this section, the different main architectures of FPGA-based TDCs are present, following the proposed taxonomy in [10]. The limitations and implementation issues of each architecture are also discussed. Through this document, the input signal, corresponding to the signal to be measured, will be denoted by *hit*. This signal is asynchronous to the reference clock.

2.2.1 Course Counters

The basic method of TDC is the countering method. This method simply involves using a counter that increments at each system clock cycle. It can be implemented by using half-adders and a set of registers to store and update the counter's value. There are two variants of this architecture. In the first variant, the counter always starts at zero and increments while the *hit* signal is set. In the second variant, timestamps are captured at each *hit* event and the time interval between the two events can be calculated by subtracting the two timestamps.

Course counters architecture is popular for its simplicity and low resources usage. However, its main drawback is the limited resolution, which is determined by the system clock frequency, as illustrated in figure 2.2. The time interval can be calculated following equation 2.2, where T_{clk} is the period of the system clock, and N_1 and N_2 are time snapshots taken at the rising edge of the *start* and *stop* signals, respectively. The range is given by equation 2.3, where n is the number of bits of the counter register. The quantization error depends on the phase difference between the arrival of the *hit* signal and the reference clock, and its maximum value is equal to one system clock period.

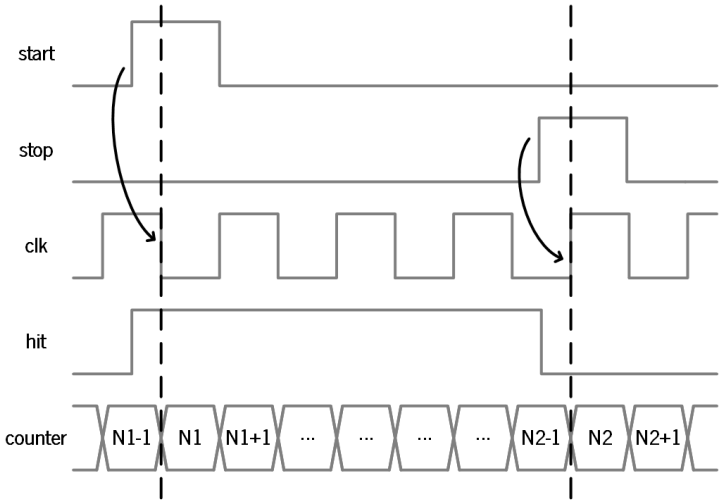

Figure 2.2: Course counter architecture waveforms. [based on [14]]

$$T = (N_2 - N1) * T_{clk} \tag{2.2}$$

$$range = 2^n \tag{2.3}$$

As the performance of FPGAs continues to improve, the maximum operating frequency also increases. In [15], a 710 MHz system clock (i.e., a 1.4 ns resolution) was reported to be used. Nevertheless, to achieve resolutions below some hundreds of picoseconds, a system clock frequency of 10 GHz or higher is required. For this reason, course counters should only be employed when a resolution of a few nanoseconds and a high-measurement range are required, or in combination with other architectures to improve their dynamic range with only minor hardware modifications.

When implementing this architecture, special attention must be paid to the routing of the enable signals for the sampling registers. If this is not properly considered, errors larger than 1 LSB may occur. Counting errors can also be influenced by metastability caused by clock skew. As the clock frequency increases, the effect of the clock skew becomes more pronounced. In addiction, increasing the number of bits of the counter makes it more challenging to achieve low clock skews between the signals fed to the counter registers.

2.2.2 Phased Clocks

The main disadvantage of course counter architectural group is its limited resolution. A Phased clock TDC reduces the LSB to less than the sampling clock period. Phased clock architectures typically use a PLL

or a clock manager block, which are primitives of most FPGAs. Another advantage of this architecture is its high linearity, which eliminates the need for complex calibration mechanisms to achieve good performance. Phased clocks architectures are based on two main techniques: oversampling and phase detection.

Oversampling architecture uses phased clocks as clock signals to independent course counters and the *hit* signal as the counter's enable. Basically, this architecture consists of *m* course counters, where *m* is the number of phase clocks used. The final measurement is calculated following equation 2.4, where n_0-n_m represents the number of counts in each counter, and T_{clk} is the base clock period. In [16] a PLL was used to create a 250 MHz quadrature clock with 0-, 90-, 180- and 270-degrees, making the equivalent of a 1 GHz clock (i.e., a 1 ns resolution). When implementing this architecture, the main challenge is routing the signal to be measured with the minimum clock skew to avoid degrading measurements. Use a low-jitter PLL to avoid phase overlap is also recommended.

$$t_{oversampling} = (n_0 + n_1 + ... + n_n) * \frac{T_{clk}}{m} \tag{2.4}$$

In Phase Detection architecture, the *hit* signal is sampled with flip-flops (FFs) by a set of equidistant phase-shifts clocks. The higher the number of clocks phases, the higher the resolution (see equation 2.5, where N_{phases} is the number of phases used). However, this increase in resolution also leads to more pronounced errors associated with the clock's phase generation and routing paths, which can degrade the TDC's linearity. Figure 2.3a depicts the basic structure of this architecture. The *hit* signal is divided into four and detected by four D-type FFs. The outputs from these FFs are aligned step by step in the chains of additional FFs, where metastable states are suppressed, creating a common clock domain for further measurement code processing. This synchronization step will be as large as the number of phases used. Figure 2.3b shows a waveform diagram of an *hit* signal and the quad-phase clocks. A rising edge is detected and the timing is extracted from the pattern "0111". The main challenge while implementing this architecture is related to the jitter associated with the different phases that degrade the TDC's' performance. The jitter values from the phase shift generators and the routing skew can lead to situations where the *n* phase clock rising edge arrives before the *n* – 1 phase-clock rising edge, creating a code pattern with bubbles. In [17] a 280 ps TDC based on phase detection with a DNL of less than half of a system LSB was reported.

$$\tau = \frac{T_{clk}}{N_{phases}} \tag{2.5}$$

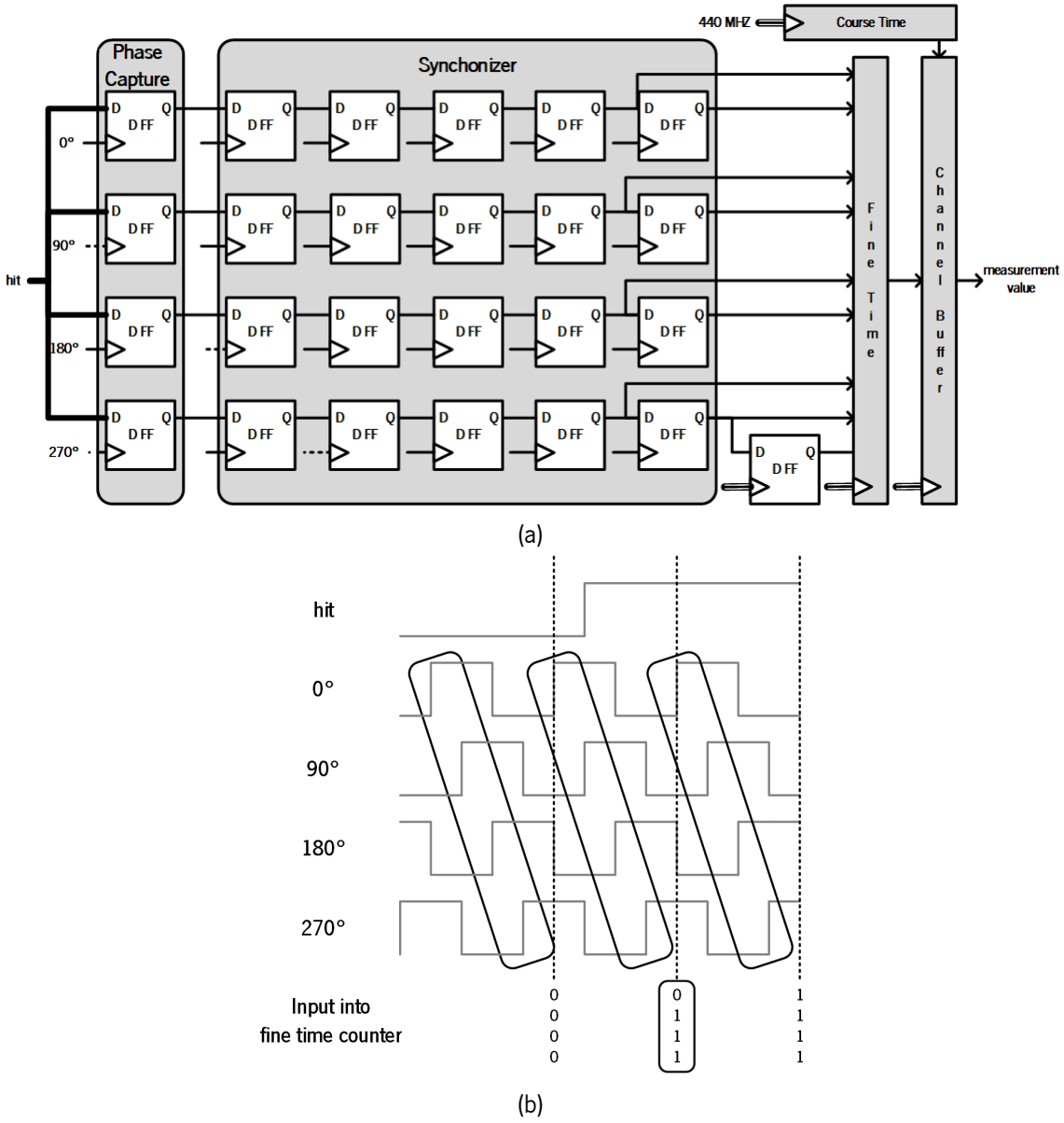

Figure 2.3: Phase detection architecture: (a) block diagram; (b) waveform diagram (adapted from [17]).

2.2.3 Tapped-Delay Lines

Tapped delay lines are the most widely employed technique to realize high-resolution TDCs. TDCs based on this architecture can achieve picosecond resolutions, which is significantly higher than what is possible with counter-based architectures. The the basic structure of a TDL-TDC is shown in figure 2.4. The input stage is often used to manipulate the *hit* signal to make it easier for the rest of the system to handle and to increase the system's resolution. The manipulated *hit* signal is then propagated along the delay line for time interpolation. The TDL status is latched out by the sample stage which outputs a thermometer code. This code is then interpreted by a thermometer-to-binary decoder to produce the interpolator timestamp. The decoding stage can have a significant impact on the TDC's dead time. The

thermometer code is as big as the TDL's number of delay elements. A TDL implemented in FPGA can easily reach a few hundred logic cells. The decoding block will, therefore, be composed of multiple stages of combinational blocks. If no special care is taken, the time needed to reach a conversion can surpass the system clock cycle. To minimize the system's nonlinearities, a calibration block is often implemented.

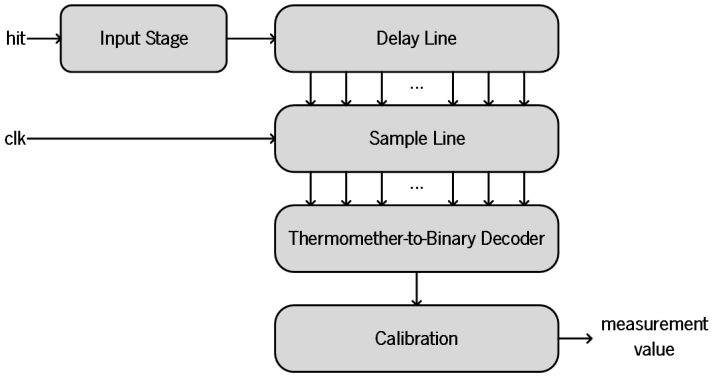

Figure 2.4: TDL-TDC block diagram (adapted from [10]).

Figure 2.5 presents the basic architecture of the delay line, which is the core of the TDL architecture. TThe delay line must ensure that the full measurement range is covered. Usually, the stop signal is the system clock. Therefore, the delay line must be long enough to comprise an entire clock cycle. The maximum achievable resolution by a TDL is determined by the intrinsic delay value of the cells used to build the delay line. For a single TDL channel, the time interval measure value can be calculated according to equation 2.6, where τ is the propagation delay of each element and n is the number of cells traversed by the delayed signal. In FPGA platforms, the most used delay elements are the carry chains cell primitives, as they have dedicating routing with the smallest internal propagation delay. However, there are research works that employed lookup table (LUT) cells primitives [18] and FFs [19] to build the delay line.

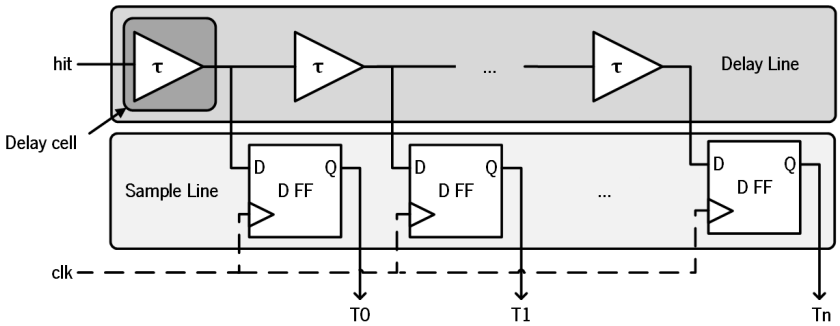

Figure 2.5: TDL architecture.

$$t_{fine} = n * \tau \tag{2.6}$$

As FPGA manufacturing technology improves, the intrinsic propagation delay of the cells used to build the delay line becomes smaller. This, combined with the TDL-TDC operation principle, suggests that a TDL implemented in a FPGA made with more advanced processing technology should naturally improve its precision. However, this is not necessarily true. The *hit* signal should transmit sequentially from one delay element to the next one, and be sampled by the bank of registers according to the its hard-wired connection, as shown in figure 2.6a. However, the sampling clock that reaches each sample stage FF is not simultaneous, which makes the order of real delays times in the taps inconsistent with the order of their physical locations, leading to bubble codes (see figure 2.6b). This problem is particularly evident in FPGAs made with 28 nm and more advanced technologies [20]. As the tap intervals become shorter, the bubbles become more severe. There are several solutions to address this problem. One solution consists of reordering the taps [21], which can minimize the bubble occurrence and reduce the complexity of decoding stage. This is typically done with the help of a histogram to detect zero delay cells. Won and Lee [22] proposed a bin-width tuning method that involves adjusting the *hit* transitions and sample patterns of the carry chain while taking into account the delays of the sum and carry-out bins. This method can improve the uniformity of the bin width, resulting in improved measurement precision. Another approach consists of counting the number of "1" in the TDL instead of determining the TDL's bin in which the signal transition occurs [23]. This method produces the same result as determining the position of the *hit*, with the advantage of allowing the bubble occurrences to be ignored.

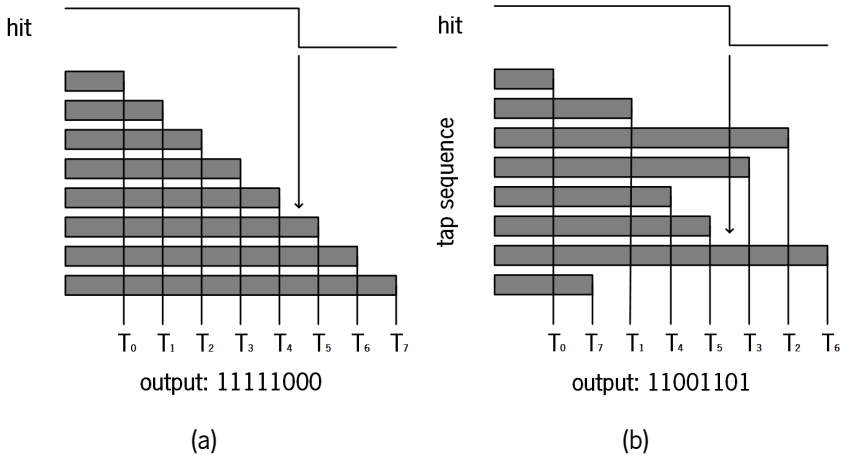

Figure 2.6: TDL output: (a) tap sequence consistent with the order of the real delay time of cells; (b) tap order not consistent with the order of the real delay time of cells (adapted from [23]).

In many TDC applications, the resolution is limited by the presence of ultra-wide bins, which are significantly wider quantization steps that occur due to the grain architecture and clock distribution scheme of FPGAs. Constraining the length of the entire delay line to a single basic logic block can help to alleviate ultra-wide bins problems, but this requirement is impossible to accomplish in a practical TDC design since

the fine time interpolator must cover an entire period of the system clock. A novel method called wave-union (WU) TDC, proposed by Wu and Shi [20] in 2008, significantly reduces the bin width. WU launchers are design to make multiple measurements with a single delay structure, effectively subdividing the ultra-wide bins in each measurement. Figure 2.7 presents the basic structure of the traditional WU TDC. The measurements of the multiple transitions reduce the nonlinearities in the delay line, improving the overall performance of the TDC, although increasing dead time and requiring a more complex decoder scheme. In [24], a WU-A TDC achieved a 1.77 ps resolution and a 3.0 ps precision. In 2016, Wang and Liu [25] concluded that WU TDCs were not suitable for improving time precision due to bubble errors in UltraScale FPGAs. Therefore, during many years there were no efficient WU TDC reported to such devices. Only in 2022, an efficient TDC in 20 nm FPGAs with WU methods was proposed by Xie et al. [26]. The authors conclude that the WU methods are still efficient in improving the resolution with maintained linearity in UltraScale FPGA when a sub-TDL structure is also integrated. By combining a dual sample (DS) structure, the WU method and the sub-TDL architecture a DSWU TDC with 1.23 ps resolution was implemented. A brief review of wave union TDCs can be found in [27].

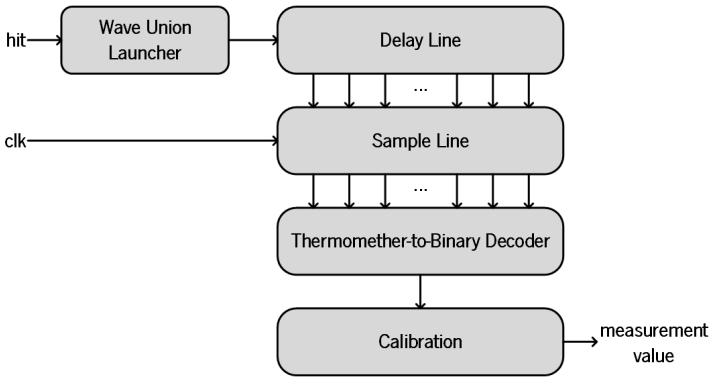

Figure 2.7: Traditional WU block diagram (adapted from [27]).

The non-uniformity of delay elements in the TDL caused by manufacturing process technology and ultra-wide bins is another considerable problem. In literature there are two main solutions to mitigate this issue: bin-by-bin calibration and bin decimation. Bin-by-bin calibration [28] is more suitable for TDCs with higher linearity and resolution requirements. It consists of a statistical approach, and it is performed through code density tests. To perform this test, a periodic signal with frequency that is unrelated to the system clock frequency should be chosen as the *hit* signal. The results from multiple measurements are recorded together with the last cell to be sampled. Considering that every cell on the delay line has the same propagation delay, and because the frequency of the *hit* signal is unrelated to the frequency of the system clock, the probability for each cell to be the last one to be sampled is the same. These measurements results can be represented in a histogram, and an estimate of the cells' actual delay can

be obtained by using equation 2.7, where τ_i is the *ith* cell's delay, n_i is the number of times the *ith* delay cell was recorded, T_{clk} is the system clock period, and N is the number of measurements performed. This histogram is stored in an embedded read access memory (RAM) to calibrate the TDC measurements during its operation. In bin decimation [29], the linearity of the TDL can be improved at the cost of resolution. This solution also achieves good results when multiple TDLs are used, as it does not increase the utilization of hardware resources. It consists of a reorganization of the current bins into several groups bins as a new one. The purpose is to minimize the INL of the new line enabling the achievement of bins with more uniform sizes, increasing the linearity of the chain so that bin-by-bin calibration may not be needed. A less usual technique based on load-regulation technique in proposed in [30]. The load regulation depends on connecting an appropriate number of unused three-state-buffers or configurable logic block (CLB) inputs to the wire which delay is adjusted. Depending on the number of inputs connected to the wire, its capacitance changes which influences its time-constant and finally changes its time delay. This method considerably uses fewer resources than bin-by-bin calibration technique at a cost of a more complex implementation.

$$\tau_i = n_i * \frac{T_{clk}}{N} \tag{2.7}$$

To improve the resolution and linearity of TDL, multiple-chain TDL architectures can be used. In this architecture, the *hit* signal is propagated through the parallel chains simultaneously, and the arrival time is measured N times, where N is the number of parallel carry chains. The TDC resolution can be theoretically improved by a factor of $\sqrt{N}$ compared to a single chain TDC [31]. Additionally, different TDLs implementations in the same FPGA will have different transfer curves. Averaging the different thermometer codes obtained from the different chains reduces the ultra-wide bins effect increasing the overall TDC linearity, as illustrated in figure 2.8. In [32] a multiple-chain TDC with 20 carry chains was implemented achieving a 1.15 ps resolution and a 3.5 ps precision. The disadvantage of multiple-chain architecture is related to the resources utilization since each TDL requires a considerable amount of resources. When implementing this architecture, the routing of the *hit* signal must be done in a way that the offset between channels is minimized.

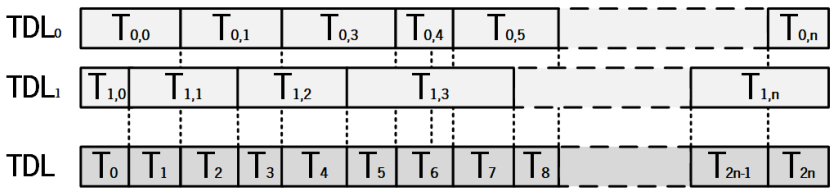

Figure 2.8: Reduction of ultra-wide bins effect (adapted from [33]).

The delay time of a carry chain is also sensitive to PVT conditions. Thus, the measurement precision and resolution can deteriorate due to voltage and temperature [32]. Solutions to this problem will be addressed in subsection 2.3.

A recent trend is to pair a TDL with phase clocks architectures to shrink the TDL length, reducing hardware utilization and the effects of nonlinearities. Because the effects of nonlinearities are propagated through the delay line, it is desirable to have a delay line as short as possible. This architecture is based on a two-stages interpolation within a single period of the system clock signal. Figure 2.9 shows the measurement of a time interval by this architecture, where a four-phase clock (FPC) is used. The first interpolation stage involves the use of phased clock to detect the nearest edge of the phased clock after the start and signals arrive. Since the widths of the phase clock time segments are known T_{ST1} and T_{SP1} can be calculated accurately. The second interpolation stage uses a TDL to cover the period between two phases of the phased clocks, T_{ST2} and T_{SP2}. The fine measure is calculated following equation 2.8. Hybrid TDLs using eight-clock and four-clock phases achieved resolutions of 1.9 ps and 2.9 ps in [33] and [34], respectively.

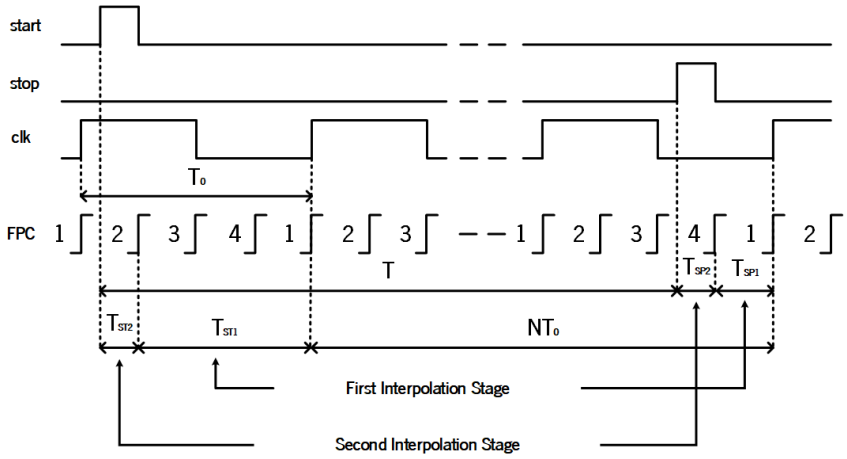

Figure 2.9: Hybrid TDL waveforms (adapted from [34]).

$$t_{fine} = (T_{ST1} + T_{ST2}) - (T_{SP1} + T_{SP2}) \tag{2.8}$$

2.2.4 Differential Delay Lines

The maximum achievable resolution of TDL architectures is limited by the intrinsic delay of the individual cells, and cannot be improved beyond this limit. To overcome this limitation, differential TDC architectures were proposed. Differential delay lines can be implemented using tapped delay lines and ring oscillators (ROs), and can provide picosecond time resolution when carefully designed and operated.

The 2-D TDL architecture is a variation of the traditional TDL architecture that uses two delay lines with different intrinsic cell delays for both the start and stop signals. This allows for a higher resolution time measurement, as the resolution is determined by the difference between the two delay elements rather than the absolute value of a single delay element (see equation 2.9, where τ_1 and τ_2 are the propagation delay of each delay element of slow and fast delay lines, respectively). Figure 2.10 presents a schematic of a 2-D TDL architecture. The fine measure is calculated according to equation 2.10, where n is the number of the traversed delay elements of the slow delay line. In order to accurately measure the time difference, it must be guaranteed that the clock delay chain has a shorter propagation delay than the hit delay chain, so that the *clk* signal can catch up to the *hit* signal. Otherwise, the *clk* signal will never be able to catch up with the *hit* signal and the TDC will always return the maximum value. In FPGA platforms, the limited range of available cells with different delays can make it challenging to implement this architecture. The same cell can be used to both start and delay chains and the difference between each stage of the two delay lines is obtained by their routing. The 2-D TDL architecture suffers from the same problems as the TDL architecture. The delay line tends to be much larger than in the normal TDL architecture, increasing the resources usage and nonlinearities across the chain. These problems cause RO implementations to be more popular than 2-D TDL architecture regarding to FPGA platforms. Nevertheless, in [35] a 2-D TDL, based on FPGA internal routing resources, achieved a 9 ps resolution and a 6.5 ps precision.

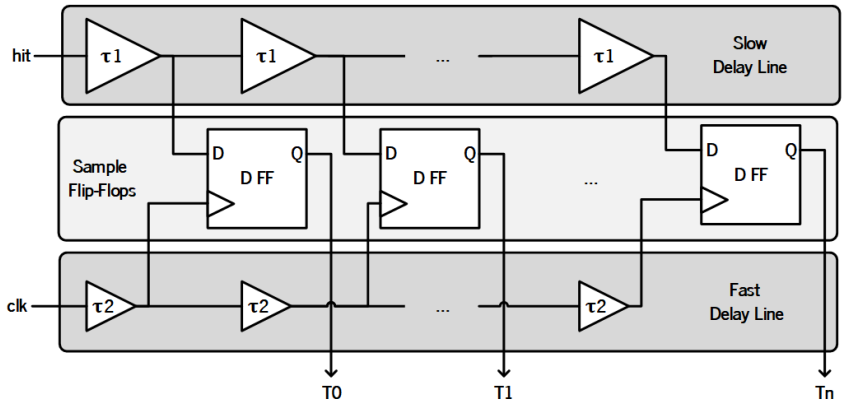

Figure 2.10: Differential delay line architecture (adapted from [36]).

$$\tau = \tau_1 - \tau_2 \tag{2.9}$$

$$t_{fine} = n * \tau \tag{2.10}$$

The RO architecture is a type of differential delay line that uses a dual ring oscillator schema paired

with a coincident detector. The resolution of the TDC is given by the difference in frequency between the two oscillator (see equation 2.11, where T_1 and T_2 correspond to the slow and fast oscillators' periods, respectively). This architecture solves the cell delay mismatch issue that can affect delay line architectures, since the resolution is no longer dependent on the intrinsic delay of individual cells. The RO architecture is essentially a TDL whose output loops back to its input, allowing for repeated measurements of the same time interval. Smaller DNL and INL will be obtained due to the disappearance of the ultra-wide bins [37]. However, the RO architecture can be more complex to implement and require more resources than a TDL. There are two main variants of RO-TDC: ROs with two independent counters and ROs with a single counter. The use of two independent counters allows for more flexibility and better performance, but requires more resources. In contrast, ROs with a single counter are simpler to implement and require fewer resources, but may have lower performance.

$$\tau = T_1 - T_2 \tag{2.11}$$

The RO architecture with two independent counters uses two counters, each incremented by one of the oscillators, and a coincident detector [38]. The block and waveform diagrams of this architecture are illustrated in figure 2.11. The measure time interval for this architecture is given by equation 2.12, where n_1 and n_2 correspond to the slow and fast counter's values, respectively. The RO architecture with a single counter employs only one counter that is clocked by the slow oscillator and stops counting once the fast oscillator can surpass it [39]. Figure 2.12 depicts this variant architecture. The pulse width reshaping module is responsible to regenerate the pulse width to a constant value so that it can sustain stable oscillation, and the ctrl2generator module is used to indicate the proper latching moment for the fine counter content. In [38], a RO with two counter achieved a resolution of 3 ps. In [36], a RO with a single counter achieved a resolution of 31 ps and a maximum dead time value of 256 ns.

One advantage of RO architecture is that it can directly obtain a fine time by reading the content of the counter, which is a natural binary code, without the need for a decoder. The fine measure is obtained from equation 2.13, where n_{fine} is the number of counts in the counter until the fast oscillator is able to overtake the slow one. The greatest disadvantage of RO architecture is related to its dead time that can reach several microseconds, which limits the maximum measurement rate of the system. According to equation 2.14, this problem can be surpassed by decreasing the TDC resolution, which is not desirable, or by increasing the oscillation frequency.

$$t_{two\_counters} = (n_1 - 1) * T_1 - (n_2 - 1) * T_2 \tag{2.12}$$

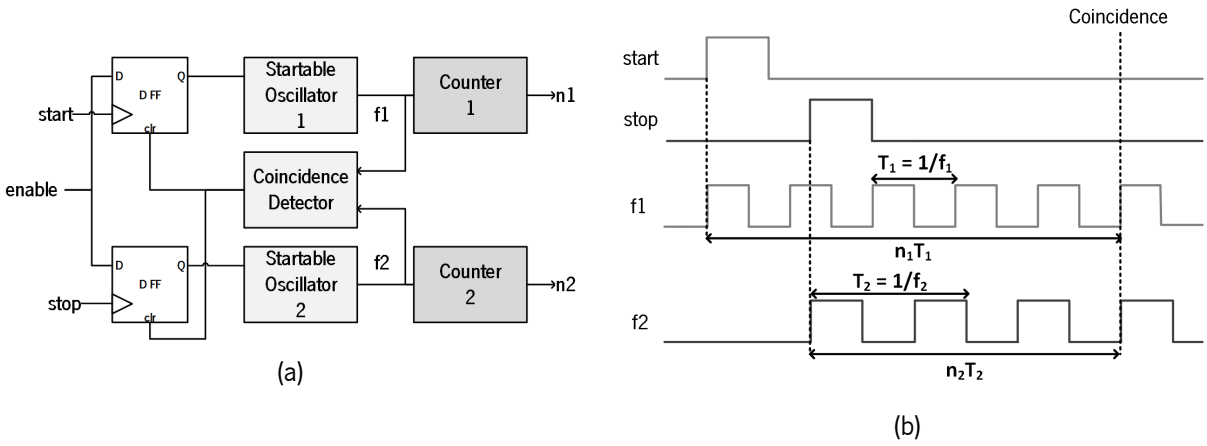

Figure 2.11: RO with two independent counters: (a) block diagram; (b) waveform diagram (adapted from [38]).

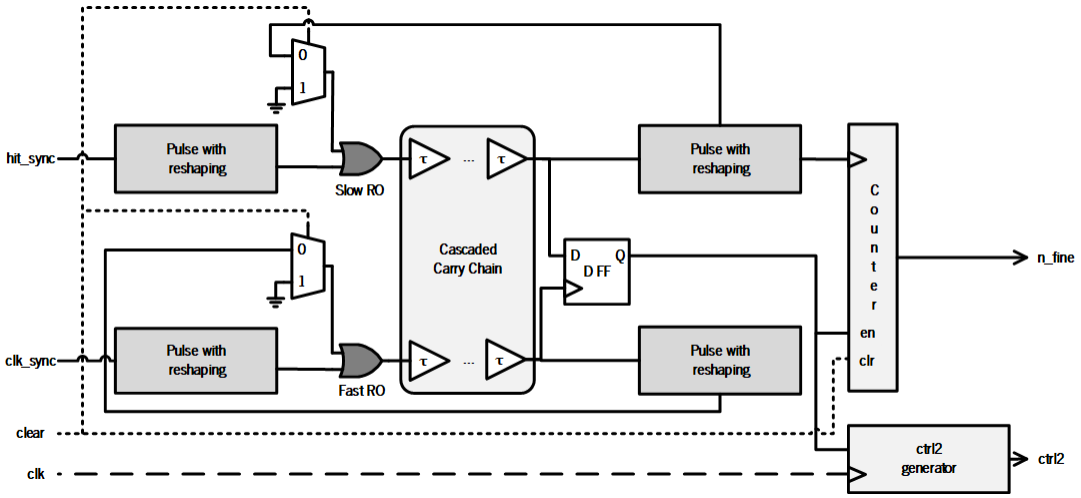

Figure 2.12: RO with a single counter (adapted from [39]).

$$t_{one\_counter} = n_{fine} * \tau \tag{2.13}$$

$$t_{max\_counv} = \frac{T_1 - T_2}{\tau} \tag{2.14}$$

In 2022, Xu et al. [37] proposed a novel approach that uses a bi-time interpolation scheme to address resolution problems without adding extra resource consumption and dead time. This approach uses the system clock as a reference and only requires one ring oscillator, which can help avoid factors that cause metastability and reduce resource consumption. To integrate this architecture in the taxonomy proposed in [10], and following the authors' approach, a new sub-architecture named hybrid is included in differential delay lines architectural group. The bi-time schema for fine time interpolation is illustrated in figure 2.13. The phased clock module uses a FPC (as present in subsection 2.2.2). The ring oscillator module is

composed by a RO, a counter, and a coincidence detector circuit. The RO is triggered by the *hit* signal to start oscillation. The rising edge of the oscillation signal will gradually moves from one region of the clock signal to an adjacent one. The coincidence detector circuit determines whether the rising edge of the oscillation signal crosses over any region boundaries of the clock signal. The counter value indicates the period difference between the oscillation signal and the reference clock signal. The proposed approach achieved a time resolution of 20 ps, dead time of 58 ns, and a precision of 15 ps to 20 ps.

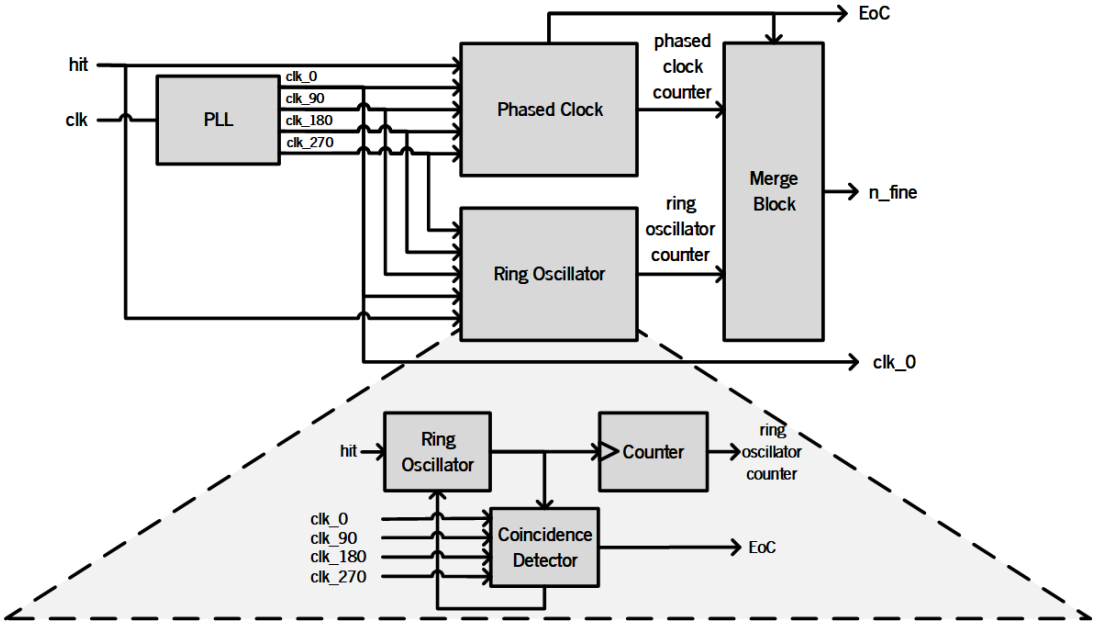

Figure 2.13: Hybrid differential delay line (adapted from [37]).

2.2.5 Pulse-Shrinking

The principle of operation of pulse-shrinking TDCs is based on mismatch between the rising and falling times of delay cells. The basic idea is to construct a propagation delay line such that the time its takes for a signal to go from low to high (T_{PHL}) is greater than that the time it takes to go from high to low (T_{PLH}). As a result, the time pulse shrinks as it cycles through the delay line. Figure 2.14 depict the concept of cyclic pulse shrinking. The pulse width can be calculated using equation 2.15, where n is the number of cycles taken until the pulse disappears. This number is proportional to the original time pulse. The minimum resolution corresponds to the amount of time the pulse shrinks per cycle.

$$t_{in} = n * (t_{PLH} - t_{PHL}) \tag{2.15}$$

The main disadvantage of pulse-shrinking architecture is that it can suffer from measurement offset when the input pulse becomes too narrow, resulting in an invalid output signal. This can limit the accuracy

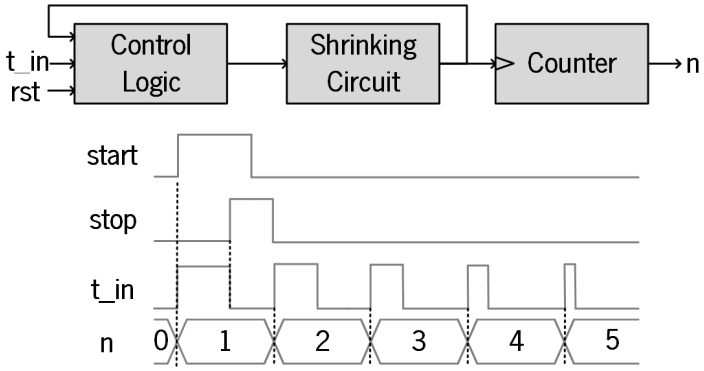

Figure 2.14: Pulse shrinking principle (adapted from [40]).

of the measurement. To overcome this issue, wide dynamic range and improve precision, Chen et al. [41] proposed a pulse-shrinking variant using offset error cancellation circuitry. Xiang et al. [42] reported a pulse-shrinking TDC with a 2.38 ps resolution and both DNL and INL less than a quarter of LSB. However, the measure range is limited to 80 ps.

Pulse-shrinking FPGA-based TDCs have several advantages, such as low resource usage and high precision. However, they are only suitable for single-shot and low-sampling rate applications [40]. In fact, Machado et al. [10] do not consider pulse-shrinking architectures to be a promising approach for high-performance FPGAs-based time measurement systems. These limitations should be considered when choosing a pulse-shrinking TDC for a specific application.

2.2.6 Gray Code

Modern applications demanding for multiple ToF measurement channels require not only high performance but also low resource and power consumption. In fact, there are applications such as mobile and wearable devices where resources and power concerns are prioritized over resolution.

In 2019, Wu and Xu [43] introduced a novel architecture that focuses on low power consumption and low resource usage, while offering high scalability and portability. The proposed architecture achieved a resolution ranging from 256 ps to 271 ps for the two TDC channels implemented, and a 160 ps precision using only 8 LUTs and 8 FFs per channel. The proposed TDC, illustrated in figure 2.15, consists of two primary parts: a combinatorial gray code oscillator and D-type FFs for sampling. The combinatorial stage is responsible to calculate the next value in the count schema, while the sampling stage is responsible for latching the value of the counter at each clock cycle, ensuring a stable value for the combinatorial stage, so that the next value can be correctly calculated and latched in the next clock cycle. The sequence generator is not driven by a periodic clock. In gray code sequence, there is only a single bit transition between two consecutive states. Since only a path is relevant at a time, the difference of propagation delays in

various feedback paths is not harmful, so the combinatorial feedback loops will not cause glitches in the system. This enables the implementation of a counter with a resolution that is no longer limited by the system clock, but by the datapath delay between values. In the reflected binary code (RBC), the lowest bit has no dependency on itself and therefore it is unnecessary to feedback *B0* to *LUT0*. The saved input is used for finish input command, *FIN*, preventing the oscillator from running indefinitely and reducing power consumption. The dynamic range is extended using a 3-bit cycle counter, which counts the number of times the gray code counter reaches overflow.

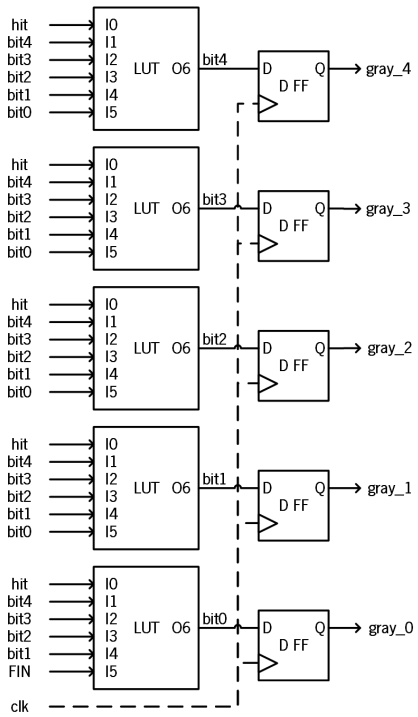

Figure 2.15: Gray code oscillator TDC (adapted from [43] and [44]).

Machado et al. [44] proposed an improved version of the gray code oscillator TDC that incorporates manual routing to improve linearity and precision. This reduces the need for calibration mechanisms and enables the use of the same calibration mechanism across multiple channels. The proposed architecture achieved a 380 ps resolution and a maximum DNL of 0.38 LSB and a INL of 0.69 LSB.It also uses only 16 FPGA logic resources per channel. The main difference between this architecture and the previous one is the use of an external binary counter to extend the measurement range of the fine measurement stage, simplifying its design. Figure 2.16 depicts the gray code oscillator schematic of a TDC channel. The gray code counter is used to implement the TDC channel for start and stop times, providing the system fine measurement. An input stage is also included to reduce power consumption by ensuring that the gray counters are only enabled for a single system clock cycle. The Merge Block concatenates the values from the coarse measurement and both TDC channels.

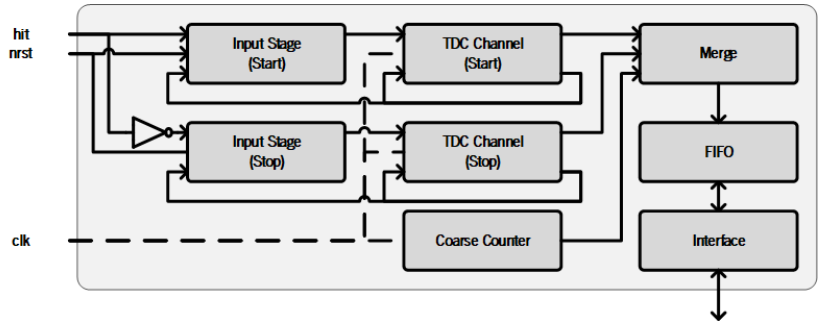

Figure 2.16: Gray code TDC block diagram (adapted from [44]).

In 2021, Araujo et al. [45] presents a gray code TDC architecture that incorporates a double-sampling to improve resolution and precision. The second sampling stage is routed with a delay that is at least the double that of the first stage, allowing for the previous gray code value to be stored in the second stage when a new value arrives at the first stage. After the delay difference, the new value arrives at the second stage, resulting in both stages containing the same value. Adding the values from both stages produces an incremental sequence with improved resolution. Using a Zynq Ultrascale+ MPSoC, the proposed TDC achieved a 69 ps resolution and a 59 ps precision using only 7 LUTs and 20 FFs, with a maximum DNL and INL of 1.76 LSBs and 1.50 LSBs, respectively. The architecture is scalable, allowing for multiple TDC channels to be implemented by replicating a single channel's placement and routing. Figure 2.17 shows the double-sampling gray TDC channel schematic.

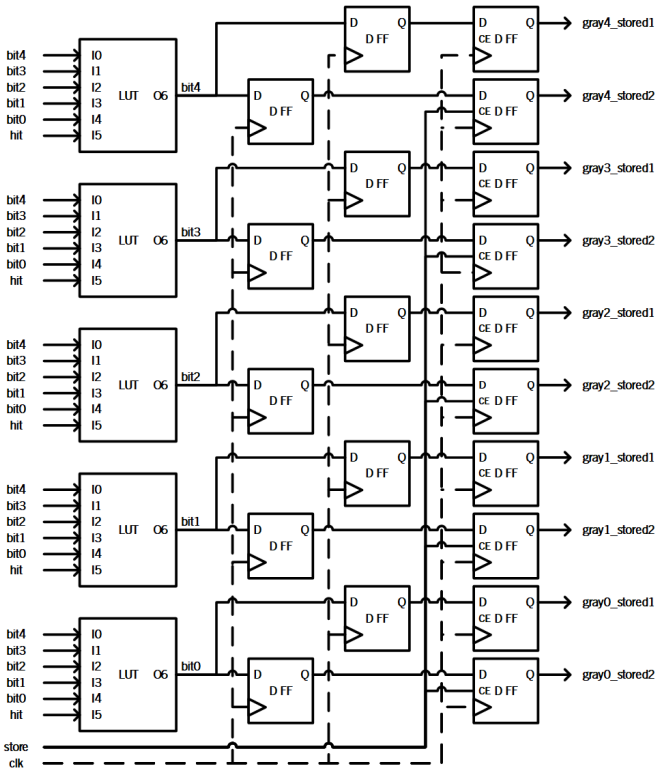

Figure 2.17: Double-sampling gray code TDC channel schematic (adapted from [45]).

2.3 Self Calibration Mechanisms

FPGA-based TDCs offers many benefits and advantages, but they also face several challenges. One significant problem is the high nonlinearity of the carry units in FPGA devices due PVT variations. The delay units of ASIC-based TDC also suffer from PVT variations. However, addressing nonlinearities in FPGAs cannot be done by using the same methods employed in ASIC platforms since the resources available in FPGA devices are predetermined from the start.

Over the years, various solutions to compensate the impact of PVT variations on delay units in both ASIC and FPGA platforms has been proposed. In ASIC-based TDC, analog delay-locked loop (DLL) architectures are commonly used. Figure 2.18 shows the basic block diagram of a typical analog DLL. This architecture consists of a phase detector, a charge pump, a loop filter and a voltage-controlled delay line (VCDL). Its operating principle is based on the detection of environmental changes and adjustment of the control voltage to maintain the a constant delay of the delay cells in the VCDL, regardless of PVT variations. In [46] a DLL architecture implemented in 0.35 µm digital complementary metal–oxide–semiconductor (CMOS) technology achieved a temperature drift of less than 0.4 ps/°C over a range from -40 °C to +60 °C. Using the same CMOS technology, [47] reported a temperature drift of below 0.05 ps/°C.

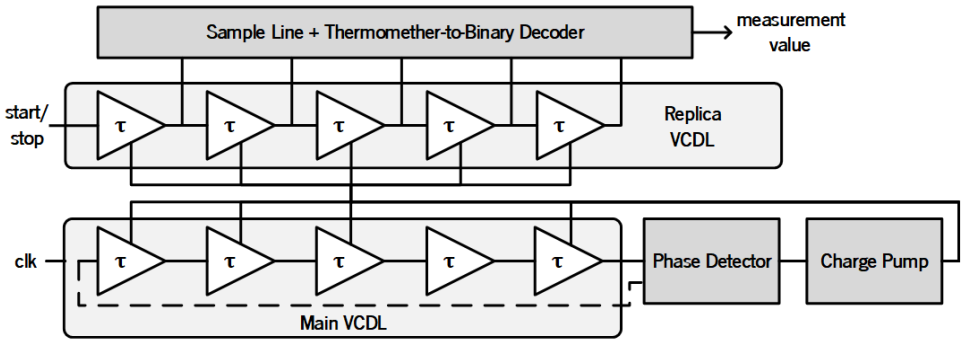

Figure 2.18: General DDL architecture block diagram (adapted from [48]).

Analog DLL have high power consumption, long lock times and require large area. To overcome these limitations, improvements aimed at replacing analog components began to emerge. Semi-digital DLLs replace the charge pump and loop filter with a counter and a digital-to-analog converter (DAC), but they still use a VCDL. In all-digital delay-locked loops (ADDLLs), the VCDL is replaced with a digital-controlled delay line (DCDL), eliminating the need for a DAC. The counter digitally controls the DCDL to reach a lock state. The optimal value of the counter must be continuous tracked to compensate the phase drift due PVT in the lock state. Compared to analog DLLs, ADDLLs have faster locking times, easier migration, higher power efficiency, and improved tolerance to PVT variations. In [49], an ADDLL implemented in 55 nm

CMOS technology achieved a 10.7 ps resolution while maintaining stable resolution with PVT variations.

Different approaches to compensate for PVT variations in FPGA-based TDCs can be found in the literature. However, despite their differences, they all use calibration tables (histograms/LUTs) to achieve this compensation. Pan et al. [50] performed bin-by-bin calibrations at different temperatures to determine the temperature coefficient of the carry chain. These calibrations are performed for both a single-chain TDL and a WU TDL. Based on the results, the authors developed a simplified temperature correction scheme that uses a dedicated correction channel to measure the temperature coefficient and correct the fine time result for all TDC channels. The experimental results show that the TDC has a 21 ps precision and is able to operate over a wide ambient temperature range from 0 °C to 60 °C.

Qin et al. [32] implemented an eight-channel, 20 carry-chains TDL, analyzed the temperature-dependent delay variation function, and design an on-board cancel to ensure stable performance over a wide temperature range. This canceler is capable of effectively correct the delay offset over temperature for the carry chain as well as for the signal transmission path. The block diagram of the proposed offset canceler is shown in figure 2.19. A temperature sensor is located near the FPGA chip to measure the operating temperature for both the FPGA and the signal transmission path. The INL data of all the TDC channels is stored in the INL LUT. INL error and chain delay offset of the encoder outputs from N carry chains are corrected in parallel by the offset canceler. After the chain delay offset is corrected, the data from multiple carry chains are averaged, and then the transmission delay is also corrected. To test the performance of the TDC with offset canceler, the system was tested at temperatures raising from −20 °C to +60 °C with a rate of 1 °C per minute. The use of offset correction allowed for a significantly improved resolution of 4.4 ps, compared to 9.3 ps without offset correction. Additionally, a precision of 3.5 ps for 20 carry-chains was obtained. The approach just presented uses multiple chain measurements which are averaged to compensate PVT variations. This approach requires calibrations LUTs for each chain and for the delay between chains before averaging, resulting in the need for additional calibration steps to ensure accuracy. In contrast, a multiple-chain TDL (as presented in subsection 2.2.3) allows to reduce the impact of temperature fluctuations on the precision, and only requires a single LUT for the equivalent chain, eliminating the need for multiple LUTs and additional calibration steps. The bin size of plain chain is affected by temperature fluctuations, which cannot be reduced by averaging. However, by segmenting the bin size variation of the plain chain, the equivalent chain becomes insensitive to temperature fluctuations, eliminating the need for a dedicated temperature. The resolution of the 10 chain TDL implemented in [31] is stable with a temperature coefficient of 0.0002 ps/°C over an operating temperature range from 25 °C to 70 °C.

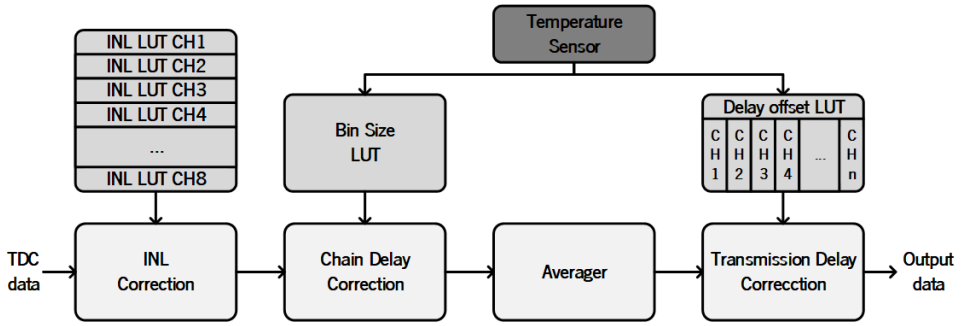

Figure 2.19: Block diagram of the offset canceler (adapted from [32]).

In 2022, Zhang et al. [51] proposed a novel method of compensating the temperature effect on the delay line. This design uses a ring oscillator, consisting of 31 NOT and one AND gates, placed next to the tapped delay line. Two calibration tables are used to calibrate automatically and online in the hardware. The frequency of the RO is measured and compared with the frequency acquired at the beginning of the measurements. The compensation is performed by scaling the lookup table coefficients evaluated in the bin-by-bin calibration phase, $T(i)_{bybline}$, according to the equation 2.16, where $f_{bybline}$ is the frequency counter of bin-by-bin calibration and f_{online} is the frequency counter of online calibration. The results shows that the frequency count value decreases linearity with the increase of temperature, about 4 °C. To test the online temperature compensation circuit, the operating temperature is increased from 30 °C to 70 °C. The TDC RMS precision without calibration increases linearly with the increase of temperature, by about 0.6 ps/°C, whereas the TDC with calibration circuit remains below 19 ps.

$$T(i)_{online} = \frac{f_{bybline}}{f_{online}} * T(i)_{bybline} \tag{2.16}$$

Currently, the calibration of TDLs mainly depends on the calibration module built in FPGAs based on code density tests. These tests have a long calibration time, which can worsen the system's dead time. Additionally,the problems cause by PVT variations often require frequent calibrations to maintain working accuracy, which can further aggravate the aforementioned problems. To address these problems, Xu et al. [52] proposed a novel TDL calibration method based on a neural network. The method uses an on-chip calibration module on an FPGA and a network calibration module on a host computer to collect delay time data and corresponding temperature information for each TDL bin. The delay time and temperature data are used as raw data samples for training, and the trained network structure is used as the result of the network calibration module. Based on this paper, it can be concluded that a neural network calibration module built on a host computer can be used on different FPGA platforms and can compensate the influence of temperature on TDC.

2.4 Conclusion

The goal of improving the PVT calibration mechanisms for TDCs is to maintain high performance levels in the face of variations in PVT conditions. As TDCs are integrated into more applications, the impact of PVT variations on TDC linearity will become more significant. Therefore, it is important to develop effective calibration mechanisms and methods that can reduce these variations and maintain the high performance levels levels required by modern applications.

Recent advances in TDC technology have made it possible to achieve high performance levels in a variety of applications. The rapid pace of technological change and the need for quick time-to-market had led to a focus on reconfigurable and customizable TDC architectures. The integration of microprocessors on most FPGA also presents an opportunity for automatically generated TDCs. An algorithm can be implemented on the microprocessor to analyze the non-linearity of the TDC, and the results can be used to automatically rearrange the hardware to improve its linearity and reduce missing codes. Furthermore, the use of machine learning techniques could potentially enable TDCs to automatically optimize their performance based on real-time data.

In addition to these advances, higher sampling rate architectures are required to meet the demands of modern applications. TDC architectures based on TDLs typically have sampling rates equal to the frequency of the reference clock being used. An alternative to reduce other architectures dead time, such as pulse shrinking and ring oscillators, is to have multiple TDC channels operating in an interleaved schema. However, this solution can have a negative impact on resource utilization. Therefore, phased clocks and TDLs are more appropriate for applications with high input event rates.

Furthermore, as technology continues to scale down and FPGA platforms improve, it is expected that TDL architectures will achieve higher resolutions due to reductions in the cells propagation delays. However, this will also exacerbate the negative effects of PVT variations on the linearity of TDLs. A shorter delay line ensures better linearity and is less susceptible to changes of supply voltage and temperature, so hybrid TDLs and differential delay lines architectures can help to mitigate these problems, although they increase implementation complexity. Counter based TDC architectures offer great linearity. Even phased clock architectures do not significantly suffer much from PVT variations since the use of an internal PLL provides automatic stabilization against changes of ambient temperature and supply voltage. However, while these architectures have great linearity against PVT variations, the maximum achievable resolution is their main drawback, as it may not met the requirements of many applications.

In conclusion, the evolution of TDC technology will continue to be driven by the requirements of appli-

cations. FPGA-based TDCs have recently demonstrated performance levels that can compete with those of ASIC-based TDCs, and it is expected that they will become more popular and start to be used in commercial products. This will increase the popularity and usability of TDCs, and reduce production costs.

References

[1] M. Zanuso, P. Madoglio, S. Levantino, C. Samori, and A. L. Lacaita, "Time-to-digital converter for frequency synthesis based on a digital bang-bang dll," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 3, pp. 548–555, 2010.

[2] M. Arkani, "A high performance digital time interval spectrometer: An embedded, fpga-based system with reduced dead time behaviour," *Metrology and Measurement Systems*, vol. 22, pp. 601–619, 12 2015.

[3] K. Karadamoglou, N. Paschalidis, N. Stamatopoulos, G. Kottaras, V. Paschalidis, and E. Sarris, "A cmos time to digital converter for space science instruments," in *Proceedings of the 28th European Solid-State Circuits Conference*, 2002, pp. 707–710.

[4] D. Tyndall, B. R. Rae, D. D. U. Li, J. Arlt, A. Johnston, J. A. Richardson, and R. K. Henderson, "A high-throughput time-resolved mini-silicon photomultiplier with embedded fluorescence lifetime estimation in 0.13 m cmos," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, pp. 562–570, 2012.

[5] Y. Li, H. Yu, S. Liu, X. Huang, and L. Jiang, "A cmos time-to-digital converter for real-time optical time-of-flight sensing system," *IEEE Communications Magazine*, vol. 56, no. 8, pp. 113–119, 2018.

[6] "Sae levels of driving automation™ refined for clarity and international audience," May 2021. [Online]. Available: https://www.sae.org/blog/sae-j3016-update

[7] S. Royo and M. Ballesta-Garcia, "An overview of lidar imaging systems for autonomous vehicles," *Applied Sciences (Switzerland)*, vol. 9, 10 2019.

[8] Z. Cheng, X. Zheng, M. J. Deen, and H. Peng, "Recent developments and design challenges of high-performance ring oscillator cmos time-to-digital converters," *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 235–251, 2016.

[9] H. Chen, D. Day, and U. Li, "Multichannel, low nonlinearity time-to-digital converters based on 20 and 28 nm fpgas," *IEEE Transactions on Industrial Electronics*, vol. 66, p. 3265, 2019. [Online]. Available: http://ieeexplore.ieee.org.

[10] R. Machado, J. Cabral, and F. S. Alves, "Recent developments and challenges in fpga-based time-to-digital converters," *IEEE Transactions on Instrumentation and Measurement*, vol. 68, pp. 4205–4221, 11 2019.

[11] R. A. Dias, F. S. Alves, M. Costa, H. Fonseca, J. Cabral, J. Gaspar, and L. A. Rocha, "Real-time operation and characterization of a high-performance time-based accelerometer," *Journal of Microelectromechanical Systems*, vol. 24, no. 6, pp. 1703–1711, 2015.

[12] N. Cao, H. Lee, E. Zaugg, R. Shrestha, W. Carter, C. Glennie, G. Wang, Z. Lu, and J. C. Fernandez-Diaz, "Airborne dinsar results using time-domain backprojection algorithm: A case study over the slumgullion landslide in colorado with validation using spaceborne sar, airborne lidar, and ground-based observations," *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing*, vol. 10, no. 11, pp. 4987–5000, 2017.

[13] S. Henzler, *Time-to-Digital Converters*. Springer Netherlands, 2010, vol. 29. [Online]. Available: http://link.springer.com/10.1007/978-90-481-8628-0

[14] Q. Guo, R. Feng, Y. Wu, and N. Yu, "Measurement of the afdx switch latency based on fpga." Institute of Electrical and Electronics Engineers Inc., 11 2016, pp. 45–49.

[15] C. Liu and Y. Wang, "A 128-channel, 710m samples/second, and less than 10ps rms resolution time-to-digital converter implemented in a kintex-7 fpga," *IEEE Transactions on Nuclear Science*, vol. 62, no. 3, pp. 773–783, 2015.

[16] Z. Li, Q. Li, J. Chang, Y. Ma, P. Liu, Z. Wang, M. Y. Hu, J. Zhao, E. E. Alp, W. Xu, Y. Tao, C. Wu, and Y. Zhou, "Development of an integrated four-channel fast avalanche-photodiode detector system with nanosecond time resolution," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 870, pp. 43–49, 10 2017.

[17] Y. Sano, Y. Horii, M. Ikeno, O. Sasaki, M. Tomoto, and T. Uchida, "Subnanosecond time-to-digital converter implemented in a kintex-7 fpga," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 874, pp. 50–56, 12 2017.

[18] H. Y. T. To, C. Su, S. Long, J. Wang, N. Na, D. Klokotov, and Y. Wang, "A novel programmable on-chip voltage droop detector for fpga applications," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 2009–2015.

[19] Y.-C. Chen, H.-C. Chang, and H. Chen, "Two-dimensional multiply-accumulator for classification of neural signals," *IEEE Access*, vol. 6, pp. 19 714–19 725, 2018.

[20] J. Wu and Z. Shi, "The 10-ps wave union tdc: Improving fpga tdc resolution beyond its cell delay," 2008, pp. 3440–3446.

[21] Y. Wang and C. Liu, "A nonlinearity minimization-oriented resource-saving time-to-digital converter implemented in a 28 nm xilinx fpga," *IEEE Transactions on Nuclear Science*, vol. 62, pp. 2003–2009, 10 2015.

[22] J. Y. Won and J. S. Lee, "Time-to-digital converter using a tuned-delay line evaluated in 28-, 40-, and 45-nm fpgas," *IEEE Transactions on Instrumentation and Measurement*, vol. 65, pp. 1678–1689, 7 2016.

[23] Y. Wang, J. Kuang, C. Liu, and Q. Cao, "A 3.9-ps rms precision time-to-digital converter using ones-counter encoding scheme in a kintex-7 fpga," *IEEE Transactions on Nuclear Science*, vol. 64, pp. 2713–2718, 10 2017.

[24] Y. Wang, X. Zhou, Z. Song, J. Kuang, and Q. Cao, "A 3.0-ps rms precision 277-msamples/s throughput time-to-digital converter using multi-edge encoding scheme in a kintex-7 fpga," *IEEE Transactions on Nuclear Science*, vol. 66, pp. 2275–2281, 10 2019.

[25] Y. Wang and C. Liu, "A 3.9 ps time-interval rms precision time-to-digital converter using a dual-sampling method in an ultrascale fpga," *IEEE Transactions on Nuclear Science*, vol. 63, 2016. [Online]. Available: http://www.ieee.org/publications_standards/publications/rights/index.html

[26] W. Xie, H. Chen, and D. D. U. Li, "Efficient time-to-digital converters in 20 nm fpgas with wave union methods," *IEEE Transactions on Industrial Electronics*, vol. 69, pp. 1021–1031, 1 2022.

[27] P. Kwiatkowski, D. Sondej, and R. Szplet, "A brief review of wave union tdcs." Institute of Electrical and Electronics Engineers Inc., 6 2021.

[28] H. Chen, Y. Zhang, and D. D. U. Li, "A low nonlinearity, missing-code free time-to-digital converter based on 28-nm fpgas with embedded bin-width calibrations," *IEEE Transactions on Instrumentation and Measurement*, vol. 66, pp. 1912–1921, 7 2017.

[29] Y. Wang and C. Liu, "A 4.2 ps time-interval rms resolution time-to-digital converter using a bin decimation method in an ultrascale fpga," *IEEE Transactions on Nuclear Science*, vol. 63, pp. 2632–2638, 10 2016.

[30] D. Chaberski, R. Frankowski, M. Zieliński, and Łukasz Zaworski, "Multiple-tapped-delay-line hardware-linearisation technique based on wire load regulation," *Measurement: Journal of the International Measurement Confederation*, vol. 92, pp. 103–113, 10 2016.

[31] X. Mao, F. Yang, F. Wei, J. Shi, J. Cai, and H. Cai, "A low temperature coefficient time-to-digital converter with 1.3 ps resolution implemented in a 28 nm fpga," *Sensors*, vol. 22, 3 2022.

[32] X. Qin, L. Wang, D. Liu, Y. Zhao, X. Rong, and J. Du, "A 1.15-ps bin size and 3.5-ps single-shot precision time-to-digital converter with on-board offset correction in an fpga," *IEEE Transactions on Nuclear Science*, vol. 64, pp. 2951–2957, 12 2017.

[33] R. Szplet, Z. Jachna, P. Kwiatkowski, and K. Rozyc, "A 2.9 ps equivalent resolution interpolating time counter based on multiple independent coding lines," *Measurement Science and Technology*, vol. 24, 2013.

[34] R. Szplet, P. Kwiatkowski, Z. Jachna, and K. Rozyc, "An eight-channel 4.5-ps precision timestamps-based time interval counter in fpga chip," *IEEE Transactions on Instrumentation and Measurement*, vol. 65, pp. 2088–2100, 9 2016.

[35] H. Wang, M. Zhang, and Q. Yao, "A new realization of time-to-digital converters based on fpga internal routing resources," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 60, pp. 1787–1795, 2013.

[36] "A high-linearity, ring-oscillator-based, vernier time-to-digital converter utilizing carry chains in fpgas," *IEEE Transactions on Nuclear Science*, vol. 64, pp. 697–704, 1 2017.

[37] G. Xu, B. Zha, T. Xia, Z. Zheng, and H. Zhang, "A high-throughput vernier time-to-digital converter on fpgas with improved resolution using a bi-time interpolation scheme," *Applied Sciences (Switzerland)*, vol. 12, 8 2022.

[38] M. Maamoun, I. S. Arami, R. Beguenane, A. Benbelkacem, and A. Meraghni, *A 3 ps resolution time-to-digital converter in low-cost FPGA for laser rangefinder*. Proceedings of the World Congress on Engineering, 2017, vol. 1.

[39] K. Cui, Z. Liu, R. Zhu, and X. Li, *FPGA-Based High-Performance Time-to-Digital Converters by Utilizing Multi-Channels Looped Carry Chains*, 2017.

[40] "Time-to-digital converters—a comprehensive review," *International Journal of Circuit Theory and Applications*, vol. 49, pp. 778–800, 3 2021.

[41] C. C. Chen, C. S. Hwang, Y. Lin, and G. H. Chen, "Note: All-digital pulse-shrinking time-to-digital converter with improved dynamic range," *Review of Scientific Instruments*, vol. 87, 4 2016.

[42] L. Xiang, P. Yang, T. Wu, and M. Zhou, "Ultra compact pulse shrinking tdc on fpga," *Measurement: Journal of the International Measurement Confederation*, vol. 203, 11 2022.

[43] J. Wu and J. Xu, *A Novel TDC Scheme: Combinatorial Gray Code Oscillator Based TDC for Low Power and Low Resource Usage Applications; A Novel TDC Scheme: Combinatorial Gray Code Oscillator Based TDC for Low Power and Low Resource Usage Applications*, 2019.

[44] R. Machado, F. S. Alves, and J. Cabral, 9.

[45] S. Araujo, R. Machado, and J. Cabral, "Double-sampling gray tdc with a ros interface for a lidar system." Institute of Electrical and Electronics Engineers Inc., 6 2021.

[46] J. P. Jansson, A. Mäntyniemi, and J. Kostamovaara, "Synchronization in a multilevel cmos time-to-digital converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, pp. 1622–1634, 2009.

[47] J. Jansson, A. Mäntyniemi, and J. Kostamovaara, "A delay line based cmos time digitizer ic with 13 ps single-shot precision," 2005, pp. 4269–4272.

[48] M. R. U. Rehman, A. Hejazi, I. Ali, J. J. Lee, S. J. Oh, Y. Pu, and K. Y. Lee, "A design of 6.8 mw all digital delay locked loop with digitally controlled dither cancellation for tdc in ranging sensor," *IEEE Access*, vol. 8, pp. 57 722–57 732, 2020.

[49] J. Tong, S. Wang, S. Zhang, M. Zhang, Y. Zhao, and F. Zhao, "A low-jitter harmonic-free all-digital delay-locked loop for multi-channel vernier tdc," 2021. [Online]. Available: https://doi.org/10.3390/s22010284

[50] W. Pan, G. Gong, and J. Li, "A 20-ps time-to-digital converter (tdc) implemented in field-programmable gate array (fpga) with automatic temperature correction," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 1468–1473, 2014.

[51] M. Zhang, Y. Zhao, Z. Han, and F. Zhao, "A 19 ps precision and 170 m samples/s time-to-digital converter implemented in fpga with online calibration," *Applied Sciences (Switzerland)*, vol. 12, 4 2022.

[52] Y. Xu, J. Xie, Z. Xing, W. Yuan, G. Yu, Z. Zeng, B. Zhang, and D. Wu, "A bin-by-bin calibration with neural network for fpga-based tapped-delay-line time-to-digital converter," *2022 IEEE International Conference on Real-Time Computing and Robotics, RCAR 2022*, pp. 681–686, 2022.