Accelerated Aging System for Prognostics of Power Semiconductor Devices

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Abstract— **Prognostics is an engineering discipline that focuses on estimation of the health state of a component and the prediction of its remaining useful life (RUL) before failure. Health state estimation is based on actual conditions and it is fundamental for the prediction of RUL under anticipated future usage. Failure of electronic devices is of great concern as future aircraft will see an increase of electronics to drive and control safety-critical equipment throughout the aircraft. Therefore, development of prognostics solutions for electronics is of key importance. This paper presents an accelerated aging system for gate-controlled power transistors. This system allows for the understanding of the effects of failure mechanisms, and the identification of leading indicators of failure which are essential in the development of physics-based degradation models and RUL prediction. In particular, this system isolates electrical overstress from thermal overstress. Also, this system allows for a precise control of internal temperatures, enabling the exploration of intrinsic failure mechanisms not related to the device packaging. By controlling the temperature within safe operation levels of the device, accelerated aging is induced by electrical overstress only, avoiding the generation of thermal cycles. The temperature is controlled by active thermal-electric units. Several electrical and thermal signals are measured *in-situ* and recorded for further analysis in the identification of leading indicators of failures. This system, therefore, provides a unique capability in the exploration of different failure mechanisms and the identification of precursors of failure that can be used to provide a health management solution for electronic devices.**

Keywords-prognostics; electronics prognostics; accelerated life testing

I. INTRODUCTION

Prognostics and health management (PHM) is an engineering discipline that focuses on the estimation of the health state of a system and the prediction of the remaining life before failure. The health state estimation is based on the actual condition of the system and it is fundamental for the prediction of remaining life under anticipated future usage. This information can be vital in increasing the safety of operations and can contribute significantly in improving mission success rate as well as reducing the cost of unscheduled maintenance. Most of today's complex systems contain significant amount of electronics. In the aerospace domain, flight and ground crews require health state awareness and prediction technologies across all systems that can accurately diagnose faults, anticipate failures, and predict the remaining life. This includes those from avionics, where electronic components have an increasingly critical role in on-board, autonomous functions for vehicle controls, communications, navigation and radar systems.

Power electronics devices such as power MOSFETs (metal oxide semiconductor field effect transistors) and IGBTs (insulated gate bipolar transistors) are semiconductor devices employed in a variety of switch mode power supplies and electrical motor drivers where high frequency switching of high electrical power is required. These devices are critical components of electronic power systems like switch mode power supplies and electrical motor drivers, where high-speed switching of high currents is standard operation Requirement. Research interest in this area has increased in recent years and the notion that electronic devices fail without any previous indication of damage progression has changed as the research community continues to identify precursors of failure in a variety of electronic components. Current research efforts in prognostics for these power devices focuses on: a) identification of the failure modes and mechanisms [1, 2]; b) identification of precursors of failure which serve as leading indicators of failure and play an essential role in the prediction of RUL [1-3]; c) development of accelerated aging methodologies and systems to accelerate the aging process of test devices by accelerating the aging process while continuously measuring key electrical and thermal parameters

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[1, 3, 4]; d) development of physics based degradation models to enable model-based prognostics [3]; and e) development of remaining life prediction algorithms with proper understanding and modeling of the different sources of uncertainty affecting the RUL estimate [5].

This paper describes an accelerated aging system that allows for the understanding of the effects of failure mechanisms and the identification of leading indicators of failure which are essential in the development of physics-based degradation models and prediction of remaining useful life. The accelerated aging system is designed for the exploration of intrinsic degradation mechanisms of component level devices which are crucial for the adoption and application of health management for electronic systems. Knowledge of semiconductor degradation under various system and environmental scenarios can be coupled with prognostic algorithms to predict future health state and time-to-failure of semiconductor components. The existence of measurable extrinsic degradation precursors, pertaining to device packaging, has been well established in literature for power transistor devices, and recently, intrinsic degradation precursors related to the physical properties of the semiconductor have also been observed. However, it is not widely known how degradation mechanisms propagate as a function of environmental conditions and various stressors. The accelerated aging system allows for the attainment of such knowledge which is critical for advancements in the field of power electronics health management and prognostics. Furthermore, it enables large scale experiments on power devices for characterization of failure precursors under various scenarios which play an essential role in managing the different sources of uncertainties present in the RUL prediction process.

In particular, this accelerated aging system for power semiconductors isolates electrical overstress from thermal overstress. The system controls the internal temperature of the test sample in order to avoid invoking failure mechanisms specific to the packaging of the device. The temperature is controlled by active thermal-electric units. Several electrical signals as well as temperatures are measured *in-situ* and recorded for further analysis in the identification of leading indicators of failures and degradation process modeling. This system provides a unique capability in the exploration of different failure mechanisms and the identification of precursors of failure that can be used to provide practical models for a health management solution for these types of devices. Preliminary results of accelerated aging test on a commercial power MOSFET in a TO-220 packages are presented. The purpose of this study is to explore failure mechanisms related to the gate region, the identification of the appropriate aging test for a particular failure mechanism and the intensity levels required on the stressor factors to accelerate the life of the device to the point that degradation process is still observable.

II. RELATED WORK

In terms of aging of power electronics, several approaches have been employed in reliability studies where the main objective is the estimation of the mean time to failure of a population of devices. Thermo-electrical stress is the most common accelerated aging methodology used for electronics devices. Thermal cycling and chronic temperature overstress are prevalent thermal stress methods where the devices are subjected to rapid changes in temperature differentials causing thermal expansion and contraction. The most common failure mechanism from such aging methodologies is various forms of package failure such as die solder degradation and wire lift.

One such method involves electrical pulsing of power MOSFETs under controlled temperatures to cause electro-thermal fatigue [6, 7]. These experiments induced stresses and hence aging conditions typically experienced by automotive components with current levels of 120A and a duty cycle of 5-10%. The experimental results showed that the accelerated aging led to an increase in the drain-source ON-state resistance of the power MOSFET. This increase was shown to be a result of die attachment de-lamination and bond-wire lift-off at the source terminal. A reliability assessment of power MOSFETs under high temperatures was performed by the authors in [8] where the devices were power cycled with a drain current of 150A and duty cycle of 30%. Junction temperatures up to 175°C were reported in this work. It was observed that when the change in junction temperature (ΔT_j) was high, it resulted in high drain to source leakage current, while high ON-state resistance due to bond wire lift-off was observed when the ΔT_j was low. Thermal cycling experiments on MOSFETs cycled 7000 times from -50°C to 100°C showed void formation in over 30% of the die solder attachment [9]. Similar results were demonstrated for IGBTs undergoing power cycling [10-12]; these results also showed the occurrence of wire lift in the devices. It should be noted that this effect is solder dependent. Typically lead-free packages provide a better material resistance to solder degradation [11]. Another form of thermal overstress involves subjecting devices to high temperatures for extended periods of time which is essentially a reliability based method. This kind of aging accelerates Time Dependent Dielectric Breakdown (TDDB) [13] and transistors have exhibited temperature dependant lifetimes [14]. In [15] a high bias stress was applied at the gate. With the gate bias ranging from 88V to 94V and the drain source grounded for 2 hours; the lowering of threshold voltage and mobility reduction were observed.

One of the experimentally identified precursors to failure has been reported in [3], IGBTs were aged with self heating. The changes in current ringing characteristics during switching were observed. An accelerated aging methodology for power MOSFET prognostics along with the identification of on resistance as a precursor of failure is presented in [1].

III. ACCELEARTED AGING

Accelerated aging approaches provide a number of opportunities for the development of physics-based prognostics models for electronics components and systems. The methodology is frequently used to assess the reliability of products with expected lifetimes is in the order of thousands of hours like electronics components and systems [16]. Accelerating the life of electronics, allows for the assessment of reliability in a considerably shorter amount of time. The development of prognostics algorithms face the same constrains as reliability in the sense that run to failure data of

critical electronics systems is rarely or never available. Furthermore, prognostics is concerned not only with time to failure of devices but with the degradation process leading to an irreversible failure as well. Therefore, it is necessary to include *in situ* measurements of key output variables and observable parameters in the accelerated aging process in order to develop and learn failure progression models. Thermal, electrical and mechanical overstresses are regularly used for accelerated aging tests of electronics. This acceleration is important as it allows for an assessment of the component health state in a considerably reduced lifetime.

Some failure mechanisms of power transistors are related to the packaging of the devices, particularly due to mechanical stresses due to thermal cycling. Thermal cycling, as an aging methodology, is regularly used to accelerate the aging of the devices by cycling among temperatures considerably larger than those seen in normal operation. The purpose of the accelerated aging system presented in this study, is to allow for a precise control of device temperatures, thus enabling the exploration of intrinsic failure mechanisms unrelated to the packaging by avoiding the application of thermal cycles. Intrinsic failure mechanisms are related to the semiconductor and gate structures. Particularly, these are changes to the semiconductor structure and gate oxide damage. By controlling the temperature within the safe operation levels of the device, the accelerated aging is induced by electrical overstress only.

A. Accelerated aging test strategy

The system operation has been validated using commercially available power MOSFETs and IGBTs discrete transistors released in a TO-220 package. The main strategy is the application of electrical overstress at fixed junction temperature (T_j) in order to avoid thermal cycles which generate package related failures. The accelerated test conditions are achieved by electrical operation regime of the devices at temperatures within the range below maximum ratings and above the room temperatures.

The junction temperature can be estimated by the following thermal conduction model,

$$T_j = T_c + I_d V_{ds} R_{\theta jc}, \quad (1)$$

where T_j is the junction temperature of the device, T_c is the device case (flange) temperature, V_{ds} is the drain to source voltage, I_d the drain current and $R_{\theta jc}$ the junction to case thermal resistance.

A measurement of the transistor case (flange) temperature is needed as well as the drain current and drain to source voltage. This estimation applies for cases where the gate voltage is held constant therefore the device is not operated as a switch. The junction temperature is controlled by keeping T_c fixed by external means and by keeping the power controlled by adjusting the gate voltage (V_{gs}) or V_{ds} depending on the load used for the device.

It is important to balance the dissipated power in the device to achieve the desired high junction temperature within the maximum rating limits for the package case temperature. In addition, it is imperative to avoid thermal cycles since this has been proven to damage the die-attachment composite (solder) diminishing then thermal dissipation performance [1]. This means thermal resistance from junction to case will increase and the operating junction temperatures will be considerably higher than the estimated ones.

The highest acceleration factor for aging can be achieved in the proximity of the safe operating area boundary of the device. Examples of the simulated I-V characteristics at different values of V_{gs} for power MOSFET with parameters similar to IRF520Npbf at 300°K are presented in Fig. 1.

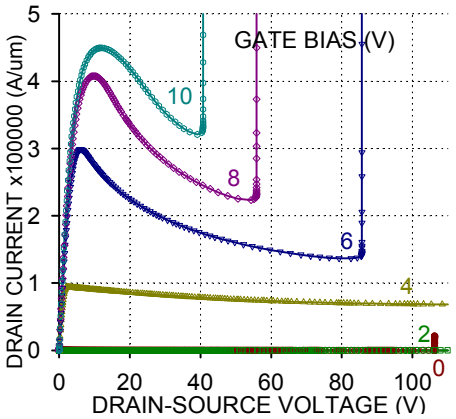

Figure 1. Simulated I-V characteristics and instability boundary at 300°K for power MOSFET.

This electrical response was obtained with a mixed-mode circuit-device simulation using software DECIMM™ from Angstrom Designs Automation [17]. The observed instability points represent the critical voltages and currents limiting the safe operation area of the electrical regime. An electrical regime close to the safe operation area boundary, the life of the device serves as the accelerator factor (stressor) for this device and it is expected to reduce the life of the device. The safe operation area boundary shifts closer to the origin as the temperature increases. Fig. 2 presents the I-V characteristics at 450°K (~175°C) which is the maximum T_j for this device as defined in the specifications.

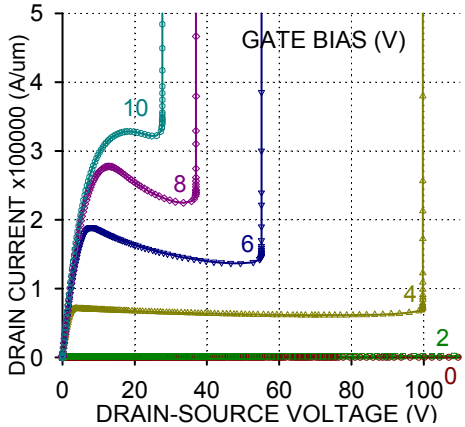

Figure 2. Simulated I-V characteristics and instability boundary at 450°K for power MOSFET.

This indicates that a constant high junction temperature can be used in conjunction with the electrical regime in order to operate the device close to the safe operation area boundary. The drain current in the electrical regime can be selected in the vicinity of the maximum rating and the same can be done with the drain to source voltage.

Electrical overstress could be applied to the gate too. By keeping the temperature of the device as well as the electrical regime within the safe operation regimes boundary, the gate voltage can be increased beyond its maximum rating value to provide a high intensity potential which will accelerate the degradation of the gate structure and trigger different types of failure mechanisms related to the gate

IV. AGING SYSTEM DESCRIPTION

The accelerated aging system supports electrical overstress of gate controlled power transistors. A series of *in-situ* measurements are available for transistor state monitoring and for prognostics modeling. These include measurements of voltages and currents, measurements of electrical transient response, measurement of thermal transients all conducted at varying gate and drain voltage levels.

In general, there three main functional components for the aging system in terms of hardware:

- the **electrical operation** unit of the device which consist of custom made printed circuit boards for the instrumentation circuitry and gate drivers, as well as commercially available power supplies and function generator to control the operation of the device under test (DUT) as indicated in Fig. 3;
- the **in-situ measurement** unit of key electrical and thermal parameters by means of commercially available measurement and data acquisition for slow and high speed measurements; and
- a **thermal block** section (Fig. 5) which allows for monitoring and control of the temperature of the DUT.

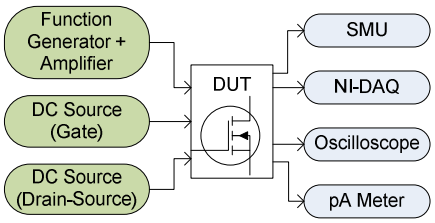

Figure 3. High level electrical functional diagram of the system.

A. Test circuit configuration

Fig. 4 shows the schematic of the circuit following the notation of a power MOSFET with three terminals, gate, source and drain. The gate can be controlled via a DC voltage or an arbitrary periodic signal using a function generator. Power supply V_{sig} is used under DC operation, this supply is an Agilent DC power supply of 60V and 1.3A rating. The typical maximum gate voltage rating of the devices tested is in the order of 20V. This power supply allows for high potential overstress of the gate structure up to 60V. When operated in switching mode, the Agilent 33220A arbitrary waveform generator is used. This allows the generation of square pulse signals up to 20Mhz. The function generator cannot source sufficient current to charge the gate of the device when switched at moderate speeds and it also cannot provide voltages of more than 5V peak to peak. An amplification stage is used based on an LM7171 operational amplifier in a non-inverting configuration. This amplifier serves as a gate driver and it is implemented in a custom made printed circuit board (PCB).

The circuit in Fig. 4 is implemented in a custom PCB (with exception of the gate driver state with is implemented in a different PCB). This circuit includes a Hall effect sensor to measure the drain current Id and provide different sets of connectors for the measurement instruments. On the power side of the device, the board includes a load bank where different loads can be installed, the rail voltage V_{dd} is provided by a Xantrex XDC-150-40 DC power supply able to supply up to 150V and 40A. This power supply can provide enough power to overstress the drain-source section of the device, the power MOSFET under test (IRF520Npbf) has a rated V_{ds} of 100V and continues I_d of 9.7A at room temperature.

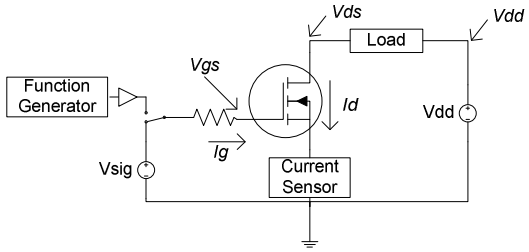

Figure 4. Schematic of aging circuit configuration and identification of electrical measurement.

B. In-situ measurements

As described earlier, one of the requirements for accelerated aging systems for prognostics is the availability of *in-situ* measurement of key electrical outputs and parameters. The aging system includes two sets of measurements, low-speed measurements for experiment monitoring and control and high speed measurements for parameter extraction and degradation process analysis. *Low speed measurements* include different voltages as described in Fig. 4 (V_{gs}, V_{dd}, V_{ds} and V_{sig}). In addition, the voltage output of the Hall effect sensor is also measured and scaled to a current value as a measurement of I_d. The gate current I_g is measured with a pico Ampere meter Keithley 6485. Thermal measurements consist of 4 temperature measurements using thermocouples. *High speed measurements* are done using an Agilent DSO5934A 4-channel oscilloscope. The voltages measured are V_{gs}, V_{ds} and V_{sig}. The drain current can be measured with the Hall effect sensor installed in the aging board or with the Agilent N-2783A current probe. These measurements are particularly important when the device is aged under a switching control signal. The transient response is captured with these measurements.

1) Low speed data acquisition equipment

A National Instrument PXI-1033chasis and controller is used to host the data acquisition card and to interface to the

computer running the aging software. NI PXI-6259 is a 16-Bit, 1MS/s multichannel data acquisition card compatible with the PXI-1033 chassis. It has 32 analog inputs, 4 analog outputs, 48 digital input/outputs. The NI SCC-68 connector block is used to make all the electrical connections to the aging board and to host 4 SCC-TC02 thermocouple modules. The SCC-TC02 modules are single-input modules for conditioning of thermocouple signals, they include a 2 Hz low-pass filter and an onboard thermistor for cold junction temperature compensation. Four T-type thermocouples are used to measure different temperatures (Fig. 5) including the case temperature T_c and the package temperature T_p.

C. *Thermal block description*

The principal characteristic of the aging system is the ability to apply electrical overstress to devices without inducing thermal cycles that generate package related failure mechanisms [1]. This is achieved by the thermal block which can be used as a hot or cold plate depending on the configuration. The thermal block allows the flow of heat in a controlled fashion in order to control the temperature of the device. The thermal block configuration (not to scale) is presented in Fig. 5. This configuration considers the removal of heat from the DUT to the environment. A thermal-electric unit is used to control the heat flow. A Custom Thermoelectric unit capable of handling 226 W and a temperature difference of 67°C is used. The heat flow in this unit is controlled by an electrical current with a maximum rating of 24A. A Tenma 72-5861 DC power supply rated to 35V and 10A is used in the current controlled mode to regulate the heat flow and control temperature T_c. The copper block serves as a large thermal mass with large thermal capacitance that allows for stable temperature. This heat sink is used to direct the heat flow to the environment by means of force convection.

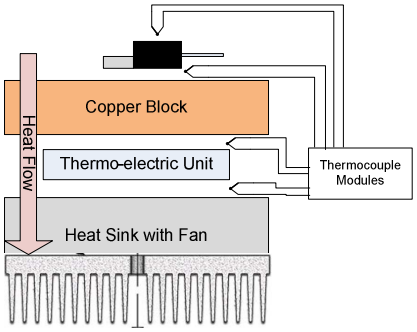

Figure 5. Thermal block for measurement and control of device temperature.

D. *Device characterization and sofware*

Parameter characterization is done via a source measurement unit. Threshold voltage ($V_{gs(th)}$), breakdown voltage ($V_{(br)ds}$) and drain to source leakage current (I_{dss}) are device parameters measured periodically during the aging process as an additional method to monitor device degradation. These measurements are not in-situ and they are done using a Keithley 2410 1100V source and measurement unit.

The software used to control the experiment and data display and logging was developed in LabView. This software allows for continuous visualization of measured values as well as data logging for further off-line analysis. Images of the implemented aging system are presented in Fig. 6.

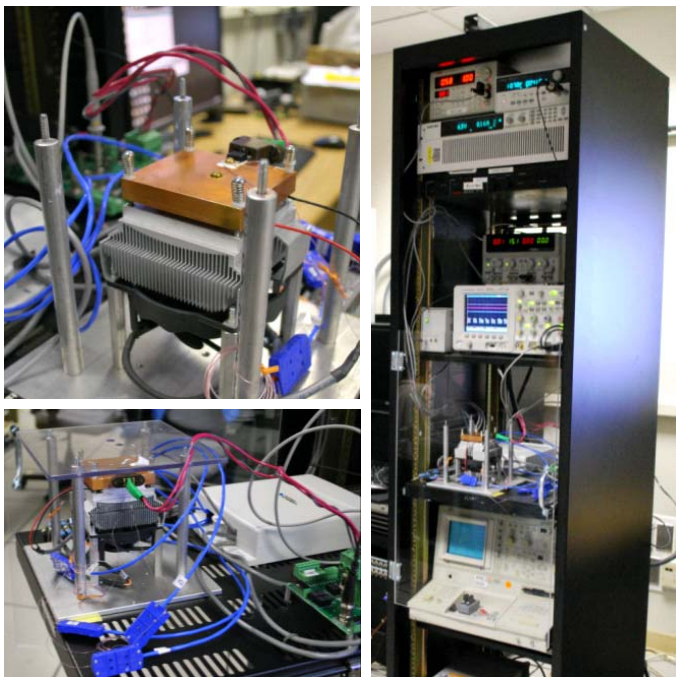

Figure 6. Images of accelerated aging system. Thermal block is shown in the left images.

V. EXPERIMETAL RESULTS

This section presents results on accelerated aging of a power MOSFET (IRF520Npbf) under electrical overstress to demonstrate de systems operation and capability. A high potential from gate to source is selected as the stress accelerating factor. The objective of this test is to apply the gate bias above the maximum rating voltage of 20V. Basically, this will induce a failure mechanism in the gate structure which in turn will affect the switching capabilities of the device. The performance of the device as observed by measured or extracted device parameters is expected to diminish as aging time increases. This decrease in performance can be observed from the measurement of internal parameters like switching time or threshold voltage.

Fig. 7 shows results from a preliminary aging experiment with V_{gs}=50V, V_{dd}=2.4V with no load. The threshold voltage is being monitored periodically to assess degradation. This is not an *in-situ* measurement and the aging is stopped to take this measurement at room temperature using the source and measurement unit.

It can be observed that the device undergoes a continuously monotonic degradation process. This observation is based on the increasing value of the threshold voltage V_{th} as the aging time increases. The threshold voltage parameter measurement conditions are based on specifications from manufacturer as the gate voltage at which the I_d=250uA having the drain and the gate shorted. The minimum rated V_{th} is 2V and the maximum is 4V based on manufacturer specifications at room temperature. It is observed that the maximum rated V_{th} is reached and

surpassed during the aging process. Threshold voltage keeps increasing until the device looses gate control and cannot turn on anymore as observed in measurement (Aging 10). The failure mode observed is an increase in V_{th}. This can be attributed to the gate trapped charge failure mechanism in which electric charge accumulates in the gate structure. These charges can lead to severe gate damage which will ultimately lead to early failure of the device.

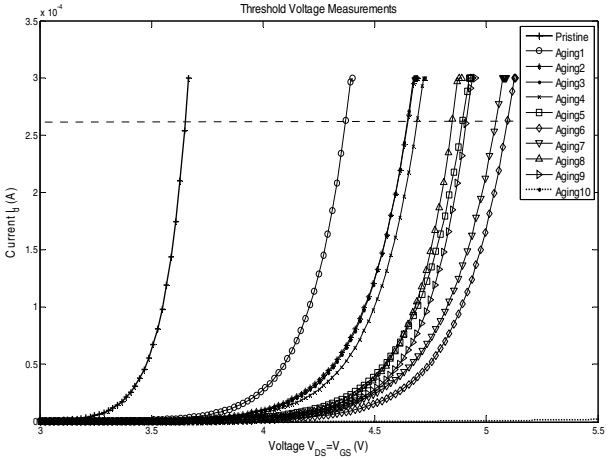

Figure 7. Degradation progress as observed on threshold voltage.

VI. CONCLUSSION

An accelerated aging test system for prognostics and health management algorithm development has been presented. The system is compatible with gate controlled Field Effect Transistors and IGBT discrete power devices. The aging system provides electrical overstress of devices while avoiding the generation of thermal cycles to eliminate package related failure mechanisms. Electrical overstress aging, realized using the system, allows the exploration of intrinsic failure mechanism, identification of precursors of failure and degradation model development by analysis of the degradation process as observed from measurements of key electrical parameters.

This system provides a unique capability in the exploration of different failure mechanisms and the identification of precursors of failure that used to provide a health management solution for these types of devices. There is no commercially available system with the capabilities required for the development of physics based prognostics solutions for discrete electronic devices. This aging system was particularly designed and built to serve as a prognostics accelerated life test vehicle where the isolation of failure mechanism and *in-situ* measurements of electro-thermal parameters are required.

The results presented for an accelerated aging test using high potential field at the gate of a commercial power MOSFET in a TO-220 package, demonstrate the aging systems capabilities. Appropriate monitoring of the degradation progression up to irreversible failure has been demonstrated for the device under test.

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