**School of Engineering**

**FAR WESTERN UNIVERSITY**

**Mahendranagar, Kanchanpur**

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**Lab Report**

**“**Interfacing with 8086”

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# ABSTRACT

This project focuses on the design and implementation of an 8-bit Arithmetic Logic Unit (ALU) using VHDL (VHSIC Hardware Description Language). The ALU is a fundamental component of digital computing systems, responsible for performing arithmetic and logical operations on binary data. The primary objective of this project is to design a versatile and efficient ALU capable of executing various arithmetic and logical operations, including addition, subtraction, bitwise AND, bitwise OR, and bitwise XOR.

The project involves the development of VHDL code for the ALU architecture, including entity and behavioral description. A comprehensive testbench is also designed to verify the functionality of the ALU through simulation. Various test cases are implemented to validate each operation of the ALU and ensure correct functionality under different input conditions.

Implementation details, including challenges faced and design considerations made during the project, are discussed. The report also presents simulation results, showcasing the ALU operation and verifying its correctness.

Overall, this project contributes to the understanding of digital logic design principles and provides hands-on experience in VHDL programming and simulation. The successful implementation of the ALU demonstrates the feasibility of designing complex digital circuits using VHDL and lays the foundation for future enhancements and applications in digital system design.

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# ACKNOWLEDGEMENT

We would like to express our sincere gratitude to Er. Kamal Lekhak, our subject teacher, for his invaluable guidance and support throughout the duration of this project. His expertise, encouragement, and insightful feedback were instrumental in helping us navigate through the complexities of digital logic design and VHDL programming.

We extend our heartfelt thanks to the Head of the Department (HOD) for providing us with the opportunity to undertake this project and for fostering an environment conducive to learning and innovation.

We would also like to acknowledge our friends and classmates for their camaraderie and encouragement, which motivated us to strive for excellence.

Special thanks are due to our project team members for their dedication, collaboration, and contributions towards the successful completion of this project. Each team member played a crucial role in various aspects of the project, and their collective effort has been invaluable.

Finally, we are grateful to all those who have supported us in any way during the course of this project. Your encouragement and assistance have been deeply appreciated.

# Introduction

### **Overview of the Project:**

The project revolves around the design and implementation of an 8-bit Arithmetic Logic Unit (ALU) using VHDL. This endeavor was assigned to us by our subject teacher, Er. Kamal Lekhak, as part of our coursework in digital logic design. The project entails developing a versatile ALU capable of executing various arithmetic and logical operations on binary data.

### **Importance of Arithmetic Logic Unit (ALU) in Computing Systems:**

The Arithmetic Logic Unit (ALU) is a critical component of digital computing systems, responsible for performing arithmetic operations (such as addition and subtraction) and logical operations (such as AND, OR, and XOR) on binary data. ALUs are integral to the functioning of central processing units (CPUs) and play a vital role in executing instructions, processing data, and performing mathematical computations in electronic devices.

### **Objectives of the Project:**

1. The primary objective of this project is to design and implement a robust 8-bit ALU architecture using VHDL. Specifically, the project aims to:
2. Develop VHDL code for the ALU architecture, including entity and behavioral descriptions.
3. Design a comprehensive testbench to verify the functionality of the ALU through simulation.
4. Validate the ALU's performance by implementing various test cases to cover different arithmetic and logical operations.
5. Gain practical experience in digital logic design, VHDL programming, and simulation techniques.
6. Enhance understanding of ALU functionality, digital system design principles, and computational concepts.

# Design Description

### Overview of the ALU Design:

The Arithmetic Logic Unit (ALU) serves as the computational heart of digital systems, responsible for executing arithmetic and logical operations on binary data. Our project focused on designing an 8-bit ALU capable of performing a variety of operations, including addition, subtraction, bitwise AND, bitwise OR, and bitwise XOR. The ALU architecture was implemented using VHDL, a hardware description language that allows for the specification and simulation of digital circuits.

### **Explanation of the VHDL Code Structure:**

The VHDL code for our 8-bit ALU comprises two main sections: the entity declaration and the behavioral architecture. The entity declaration defines the inputs and outputs of the ALU, including the data inputs A and B, the operation opcode, the result output, and various flags indicating the status of the operation (e.g., zero flag, carry flag, sign flag). The behavioral architecture describes the functional behavior of the ALU, specifying how the inputs are processed to produce the desired output.

### **Description of Each Component (Entity and Architecture):**

The entity declaration provides a high-level overview of the ALU's interface, defining the input and output ports required for communication with other components in the system. The architecture section contains the implementation details of the ALU, including the logic for performing arithmetic and logical operations based on the provided inputs and opcode.