END-SEMESTER EXAMINATION, January-2024
Digital Logic Design (EET1211)

Programme: B.Tech(CSE,CSIT) **Semester:3rd**
Full Marks: 60 **Time: 3 Hours**

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Able to State and explain different number systems, binary codes.	L2	1	6
Able to apply the principles of Boolean algebra, Karnaugh map and Quine McCluskey Method to simplify logic expressions.	L3	2,3,4b,4c	16
Able to Analyze and design various combinational circuits.	L3	5,6,7a,8a,8b,9a,9b	22
Able to Analyse and design Memory and Programmable Logic Devices.	L3	4a,7c	4
Able to Analyse and understand latches, flip-flops, registers and counter operations.	L3	9c,10	8
Able to implement various digital circuits using HDL and Standard ICs.	L3	7b,8c	4

*Bloom's taxonomy levels: Remembering (L1), Understanding (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1. (a) Convert $(757.25)_{10}$ to hexadecimal and then to binary. 2

   (b) Add the following numbers in binary using 1's complement to represent negative numbers. Use a word length of 6 bits (including sign bit). 2
   (-18)+25

   (c) Represent $(753)_{10}$ in 6 3 1 1 and Gray code. 2

2. (a) 

2

Write the expression for output Y.

(b) Simplify the following Boolean expression to a minimum number of literals. 2

F= (yz' + x'w)(xy' + zw')

(c) Implement the Boolean function (AB+CD) using 2-input NAND gates. 2

3. (a) Simplify the following Boolean function F, together with the don't-care conditions d. 2

F(A,B,C,D)= ∑(0,3,7,8,9,11,12,13)

d(A,B,C,D) =∑(1,4,14,15)

(b) Implement the following Boolean function using exclusive-OR and AND gates. 2

F=A'B'CD+A'BCD'+AB'C'D+ABC'D'

(c) Find the minimum product of sum expression for F=∑m (1, 3, 4, 5, 6, 7, 9, 12, 13) using Karnaugh map. 2

4. (a) Draw a PLA circuit to implement the function 2

F1= (AB + AC + BC)'

F2= AB + AC + ABC'

(b) Find all prime implicants of the following function using Quine-McCluskey procedure: 2

F(A,B,C,D) =∑m (1,3,5,6,8,9,12,14,15)+ ∑d(4,10,13)

(c) Using the method of map-entered variables, use four-variable maps to find a minimum sum-of-products expression for F(A,B,C,D,E) = ∑m(0,4,5,7,9) + ∑d(6,11) + E(m1+m15). 2

5. Design a 4 bit Excess-3 to BCD code converter.

(a) Write the truth table for the circuit. 2

(b) Derive the Minimized Boolean expression for each output of 2

the circuit.

(c) Draw the logic diagram for the circuit. 2

6. Design a combinational circuit with four inputs and four outputs that converts a 4bit binary number into the equivalent 4bit Gray code.

(a) Write the truth table for the circuit. 2

(b) Derive the Minimized Boolean expression for each output of the circuit. 2

(c) Draw the logic diagram for the circuit. 2

7. (a) Design a full adder circuit. 2

(b) Write the HDL description of a full adder circuit. 2

(c) Implement full adder using Programmable Array Logic. 2

8 Design a 4 bit priority encoder with inputs D_3 (MSB), D_2, D_1 and D_0 (LSB) and outputs X, Y and V. The priority assigned to inputs is $D_0 > D_1 > D_2 > D_3$.The output V shows a value 1 when one or more inputs are equal to one. If all inputs are 0, V is equal to 0. When V=0, then other two outputs are not inspected and are specified as don't care conditions.

(a) Write truth table of the encoder and find the minimized expression for the outputs X, Y and V. 2

(b) Draw logic diagram of the priority encoder. 2

(c) Write the HDL description of the 4bit priority encoder circuit. 2

9 (a) Design a 2 X 1 Multiplexer that will select the binary information from one of the two input lines and direct it to a single output line based on the value of a selection line. 2

(b) Design a full subtractor circuit using 3 to 8 line decoder and external OR gates. 2

(c) Write the characteristic table and Excitation table for D Flip Flop. 2

10 Design a 3-bit synchronous down counter with T Flip-Flops.

(a) Write state diagram and state table of the binary counter. 2

(b) Find the simplified flip flop input equations for the counter. 2

(c) Draw logic diagram of the 3-bit counter. 2

End of Questions