(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

THIRD SEMESTER [B.TECH] JANUARY-FEBRUARY 2023

Paper Code: ICT-219 **Subject: Digital Electronics**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt five questions in all including Q. No. 1 which is compulsory. Select one question from each unit.

Q1 Answer the following:-

(a) Differentiate between analog and digital signals (1)
(b) Implement an XOR gate using NAND gates only (2)
(c) State De Morgan's Laws (2)
(d) Differentiate between ring counter and Johnson counter (2)
(e) What is a Synchronous counter? (2)
(f) What are the advantages of R-2R ladder over a weighted resistor network? (2)
(g) State Nyquist sampling theorem (2)
(h) Which logic family out of TTL, ECL and CMOS has least power dissipation? (1)
(i) What do you understand by access time of a memory? (1)

UNIT-I

Q2 (a) Reduce the following Boolean functions using K-maps: (9)
(i) $F(A,B,C)=\sum(0,2,3,4,5,6)$
(ii) $F(A,B,C,D)=\sum(1,4,7,10,13)+d(5,14,15)$
(b) Using laws of Boolean algebra prove the following: (6)
(i) AB+A'C+BC=AB+A'C
(ii) A+B[AC+(B+C')D]=A+BD
(iii)AB'C + B+ BD' + ABD' + A'C=B + C

OR

Q3 (a) Reduce the following Boolean Function F(A, B, C, D) = $\sum(1, 2, 8, 9, 10, 12, 13, 14)$ using Quine McClusky(Tabulation) method. (10)
(b) Simplify the Boolean Function and then implement using only NAND gates F=BD+BCD'+AB'C'D'. (5)

UNIT-II

Q4 (a) Design a BCD to Excess-3 Code Converter. (8)
(b) What is Gray code? Give applications of Gray code. Design a 4-bit Gray to Binary code convertor. (7)

OR

Q5 (a) What is race condition in Flip-Flops? Draw circuit diagram of a JK master slave Flip Flop and explain how it removes race condition. (5)
(b) Implement a Full adder using two half adders and an OR gate. (4)
(c) Draw and explain the working of 4-bit Universal shift register. (6)

UNIT-III

Q6 Design a sequence detector to detect the 4-bit sequence 0110. Draw the state diagram, state table and implement the circuit using T flip-flops. (15)

OR

P.T.O.

Q7 (a) Explain the working of a dual slope Analog to Digital convertor. **(8)**

(b) A counter type A to D converter is driven by a 500 KHz clock. Find the average conversion time, maximum conversion time and maximum conversion rate. **(3)**

(c) What are the output voltages caused by each bit in a binary ladder if input logic 0= 0 volts and logic 1 =10volts. **(4)**

UNIT-IV

Q8 (a) Explain the following terms with respect to logic families Figure of merit , Fan out , noise immunity. **(6)**

(b) Draw the diagram of a TTL NAND gate with active pull up and explain its behaviour qualitatively. **(9)**

OR

Q9 (a) Suppose we have two 16 X 4 RAM chips and we need a memory that can store 16 eight bit words. Draw a neat diagram to show how we can obtain the desired memory using two 16 X 4 RAM chips. **(4)**

(b) The capacity of a memory is 8K X 16. How many bits are in each word? How many words are being stored? How many cells does this memory contain? **(3)**

(c) What is a PLA? How does it differ from a PAL. Explain through suitable block diagrams. **(4)**

(d) What is an FPGA? Draw the structure of a typical FPGA. **(4)**

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