# *EET1211: Digital Logic Design*

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| | **ITER, SIKSHA 'O' ANUSANDHAN**<br>**(Deemed to be University)** | | **LESSON PLAN** |
| Programme | **B.Tech.** | Academic Year | **2024-25** |
| Department | **CSE/CSIT** | Semester | $3^{rd}$ |
| Credit | **4** | Grading Pattern | **1** |
| Subject Code | **EET1211** | | |
| Subject Name | **Digital Logic Design** | | |
| Weekly Course Format | **3L - 2P** | | |
| Subject Coordinator (s) | **Dr. Sunita Samant, Dr. Manoj Naik & Dr. Monalisa Mohanty** | | |

## Text Books(s):

(1) Fundametals of Logic Design by Roth, Kinney and Raghunandan, Cengage.

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| **Course Outcomes** | Students will be able to | |
| | **CO1** | Able to state and explain different number systems, binary codes. |
| | **CO2** | Able to apply the principles of Boolean algebra, Karnaugh map and Quine-McCluskey Method to simplify logic expressions and implement it using gates. |
| | **CO3** | Able to analyse and design various combinational circuits. |
| | **CO4** | Able to analyse and design Memory and Programmable Logic Devices. |
| | **CO5** | Able to analyse and understand latches, flip-flops, registers and counter operations. |
| | **CO6** | Able to implement various digital circuits using HDL and standard ICs. |

# *EET1211: Digital Logic Design*

| Sl.No. | Lessons/Topics to be covered | Book Reference (sections) | Mapping with COs | Home Work/ Assignments/ Quizzes |
|---|---|---|---|---|
| **1** | Digital Systems and Switching Circuits. | RK_1.1 (pg.2-4) | **CO1** | |
| **2** | Number Systems and Conversion. | RK_1.2 (pg.4-7) | **CO1** | |
| **3** | Binary Arithmetic and Representation of Negative Numbers. | RK_1.3-1.4 (pg.8-17) | **CO1** | |
| **4** | **Lab#1:** Introduction to different ICs and examine the operation of logic gates. | | **CO6** | |
| **5** | Binary Codes. | RK_1.5 (pg.17-18) | **CO1** | |
| **6** | Introduction to Boolean Algebra, Basic Operations, Boolean Expressions, Basic theorems and Laws. | RK_2.1-2.5 (pg.26-35) | **CO2** | |
| **7** | Simplification Theorems, Multiplying Out and Factoring, Multiplying Out and Factoring Expressions | RK_2.6-2.7,3.1 (pg.35-40,50-51) | **CO2** | |
| **8** | **Lab#2:** Examine and analyze the gate level minimization for boolean function. | | **CO6** | |
| **9** | Complimenting Boolean Expression<br>Problem Solving | RK_2.8 (pg.41-42) | **CO2** | |
| **10** | Exclusive-OR and Equivalence Operations. The Consensus Theorem | RK_3.2-3.3 (pg.51-55) | **CO2** | **Assignment-1: Introduction to Electronics Number System and Conversion, Boolean Algebra** |
| **11** | Algebraic Simplification of Switching Expressions and Proving Validity of an Equation<br>Problem Solving | RK_3.4-3.5 (pg.55-58) | **CO2** | **Quiz-1** |
| **12** | **Lab#3:** Design, construct & examine the combinational circuit to solve a given oroblem | | **CO6** | |

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|---|---|---|---|---|
| **13** | Canonical Form: Minterm and Maxterm Expansions, | RK_4.2 (pg.71-74) | **CO2** | |
| **14** | Generation of Switching Equation From Truth Table, General Minterm and Maxterm Expansions, and Incompletely Specified Functions | RK_4.3-4.5 (pg.74-81) | **CO2** | |
| **15** | Examples of Truth Table Construction<br>Problem Solving | RK_4.6 (pg.81-83) | **CO2** | |
| **16** | **Lab#4:** Introduction to VHDL and Design of combinational circuits using VHDL | | **CO6** | |
| **17** | Examples of Truth Table Construction<br>Problem Solving | RK_4.6 (pg.81-83) | **CO2** | **Assignment-2: Application Of Boolean algebra Minterm and Maxterm Expansions, K-maps** |
| **18** | Minimum form of switching functions, Two- and Three-Variable Karnaugh Maps | RK_5.1-5.2 (pg.94-100) | **CO2** | |
| **19** | Four-Variable Karnaugh Maps | RK_5.3 (pg.100-103) | **CO2** | |
| **20** | **Lab#5:** Design and Examine different Decoder, Encoder, and Multiplexer circuits using VHDL Circuits | | **CO6** | |
| **21** | Design of Half Adder, Full Adder, Half Subtracter, Full Subtracter, and Binary Adder and Subtracters | RK_9.9 (pg.233-237) | **CO2** | |
| **22** | Design of Binary Comparator | RK_9.10 (pg.240-244) | **CO2** | |
| **23** | Quine-McCluskey Methods: Determination of Prime Implicants and the Prime Implicant Chart | RK_6.1-6.2 (pg.128-134) | **CO2** | **Quiz-2** |

| Sl.No. | Lessons/Topics to be covered | Book Reference (sections) | Mapping with COs | Home Work/ Assignments/ Quizzes |
|---|---|---|---|---|
| **24** | **Lab#6:** Examine the operation of various Flip-Flop circuits using VHDL | | **CO6** | |
| **25** | Quine-McCluskey Methods: Determination of Prime Implicants and the Prime Implicant Chart | RK_6.1-6.2 (pg.128-134) | **CO2** | |
| **26** | Simplification of Incompletely Specified Functions and Simplification Using Map-Entered Variables<br>Problem Solving | RK_6.4-6.5 (pg.136-139) | **CO2** | |
| **27** | Multi-Level Gate Circuits, NAND and NOR Gates, Design of Two-Level NAND and NOR Gate Circuits | RK_7.1-7.2 (pg.148-154) | **CO2** | |
| **28** | **Lab#7:** Examine the operation of various Flip-Flop circuits using basic logic gates | | **CO6** | |
| **29** | Design of Two-level, Multi-Level NAND- and NOR-Gate Circuits, Circuit Conversion Using Alternative Gate Symbols | RK_7.3-7.5 (pg.154-162) | **CO2** | |
| **30** | Design of Two-level, Multi-Level NAND- and NOR-Gate Circuits, Circuit Conversion Using Alternative Gate Symbols<br>Problem Solving | RK_7.3-7.5 (pg.154-162) | **CO2** | **Assignment3: Quine-McCluskey Method, Design of Multi-Level circuits using NAND- and NOR-Gate, Design of Combinational Circuits** |
| **31** | Multiplexers and design of Boolean functions using MUX | RK_9.2 (pg.202-211) | **CO3** | |
| **32** | **Lab#8:** Design and Examine Synchronous and Asynchronous counter circuits using basic logic gates | | **CO6** | |

| Sl.No. | Lessons/Topics to be covered | Book Reference (sections) | Mapping with COs | Home Work/ Assignments/ Quizzes |
|---|---|---|---|---|
| **33** | Multiplexers and design of Boolean functions using MUX | RK_9.2 (pg.202-211) | **CO3** | |
| **34** | Three-State Buffers, Decoders and Encoders, Cascading of Decoders and Design of Boolean Function using Decoder | RK_9.4 (215-217) | **CO3** | |
| **35** | Three-State Buffers, Decoders and Encoders, Cascading of Decoders and Design of Boolean Function using Decoder | RK_9.4 (pg.215-217 | **CO3** | **Assignment-4: Multiplexers, Decoder and Encoder, VHDL** |
| **36** | **Lab#9:** Design and Examine different Shift Register circuits using basic logic gates | | **CO6** | |
| **37** | Set-Reset Latch. Gated Latches. | RK_11.1-11.3 (pg.294-304) | **CO5** | **Quiz-3** |
| **38** | D, S-R and J-K Flip-Flop,T Flip-Flop | RK_11.5-11.7 (pg.307-311) | **CO5** | |
| **39** | Analysis of clocked Sequential Circuits | RK_13.1–13.3 (pg.374-386) | **CO5** | |
| **40** | **Lab#10:** Design and examine synchronous skip counter circuit using basic logic gates | | **CO6** | |
| **41** | Registers | RK_12.1-12.2 (pg.332-341) | **CO5** | |

| Sl.No. | Lessons/Topics to be covered | Book Reference (sections) | Mapping with COs | Home Work/ Assignments/ Quizzes |
|---|---|---|---|---|
| **42** | Design of Binary Counters, Counters for Other Sequence, Counter Design Using S-R and J-K Flip-Flops, and Binary Ripple Counter | RK_12.3-12.6 (pg.341-358) | **CO5** | |
| **43** | Design of Binary Counters, Counters for Other Sequence, Counter Design Using S-R and J-K Flip-Flops, and Binary Ripple Counter | RK_12.3-12.6 (pg.341-358) | **CO5** | |
| **44** | **Lab#11:** Design and examine sequence detector circuit using basic logic gates | | **CO6** | |
| **45** | Read-Only Memories | RK_9.5 (pg.1-4)2 7-222 | **CO4** | |
| **46** | Programmable Logic Devices: Programmable Array Logic, Programmable Logic Array | RK_9.6 (pg.222-227) | **CO4** | **Assignment-5: Latches and Flip-Flops, Registers and Counters, Analysis of Clocked Sequential Circuits, Programmable Logic Devices** |
| **47** | Programmable Logic Devices: Programmable Array Logic, Programmable Logic Array | RK_9.6 (pg.222-227) | **CO4** | |
| **48** | **Lab#12:** project evaluation | | **CO6** | |