MID-SEMESTER EXAMINATION, April-2024
Computer Organization and Architecture (EET2211)

Programme: B.Tech.(CSE/CSIT) **Semester: 4th**
Full Marks: 30 **Time: 2 Hours**

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Able to explain the concepts that underline the modern computer's evolution, function, and organization.	L1	1	6
Able to identify the appropriate organization of a computer for achieving the best performance.	L2	2	6
Able to analyze and demonstrate the computer function and interconnection.	L2	3	6
Able to understand and analyze the computer memory system.	L2	4	6
Able to interpret low-level processor operations using a series of computer instructions.	L4	5	6

*Bloom's taxonomy levels: Remembering (L1), Understanding (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries an equal mark.

1. (a) List and briefly define the main structural components of the single-processor computer. 2
   (b) What is the difference between a microprocessor and a microcontroller? Also, draw a block diagram to indicate the microcontroller chip elements. 2
   (c) Briefly explain the different services provided by cloud computing 2

2. (a) Explain the possible approaches to increase processor speed, as well as the obstacles to doing so. 2
   (b) Let a program have 30 percent of its code enhanced to run 2.5 times faster. What will be the overall system speedup? 2

(c) Consider the execution of a program that result in the execution of 2 million instructions on a 400-MHz processor. The instruction mix and the CPI for each instruction type are given below, based on the result of a program trace experiment. Then determine the effective CPI and MIPS rate. 2

Instruction Type	CPI	Instruction Mix (%)
Arithmetic/logic	1	50
Load/store	2	20
Branch	4	10
Memory reference	8	20

3. (a) Briefly describe the instruction cycle state diagram. 2

(b) Explain the memory module of a computer. Also, find out the maximum memory capacity if the width of the address bus is 20 lines and the data bus is 8 lines. 2

(c) Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 30% of the operands and instructions are 32 bits long, 30% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor. 2

4. (a) Explain the performance parameters: Access time, Memory cycle time, and Transfer rate of memory. 2

(b) Explain the cache read operation through a flowchart. 2

(c) Consider a machine with a byte-addressable main memory of 64KB and a block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with the machine. Then, how is a 16-bit memory address divided into tag, line number, and byte number, and show the format of how the processor's addresses are interpreted? 2

5. (a) Explain the different addressing modes of the 8086 microprocessor with suitable examples. 2

(b) Determine the output memory location (data location) and the content of that location for the following code: 2

```
MOV AX, 23F0H
MOV BX, AX
MOV [BX], AX
MOV CX, 503FH
MOV AX, CX
SUB AX, [BX]
INC BX
INC BX
MOV [BX], AX
HLT
```


(c) Write an assembly language program using assembler directive in 8086 to find the smallest number among an array of 8-bit data. 2

End of Questions