United International **University** (UIU)
Dept. of Electrical & Electronic Engineering (EEE)
EEE 442: VLSI Design Laboratory

Design of local minima/maxima circuit

The purpose of this project is to design a simple digital circuit that accumulates and finds the maximum and minimum of a series of input numbers.

The inputs are: a 32-bit ***in****,* and single bit ***clear****,* and ***clk****.*
The outputs are 32-bit ***max****,* ***min****,* and ***acc****.*

Operation of the chip begins by setting *clear*=1 for at least one clock cycle to clear all three outputs. The output *acc* is the accumulated sum, *max* is the current maximum, and *min* is the current minimum of all inputs since the last clearing operation.

Write RTL code for the circuit, simulate, synthesize and place & route the design. Your design needs to run at 1 GHz frequency. Must be clean of violations, minimizing the area; must have balanced clock tree with less than 50ps skew.

Bonus: Sample the input every millisecond and calculate the local maxima/minima for every 10 seconds.