Mid Term Question Paper

IE 501; Microprocessor & Microcontrollers; Total Marks: 25

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Multiple Choice Questions [15-marks]

a) Q1 to Q12 has only one correct answer;

b) Q13 to Q15 have more than one correct answers;

c) There is no negative marking.

Q1: Which of the following is not a data transfer instruction? *   1 point

○ MOV A,M

○ LDA 2600H

○ RAL

○ SPHL

⦿ Other: DAS

Q2: In the instruction DCR & INR, which of the following flag bit is not   1 point
affected? *

○ Zero

○ Sign

○ Parity

⦿ Carry

Q3: 8085 enters into a wait state after the recognition of * 1 point

- ○ HOLD
- ○ READY
- ○ RESET
- ● INTR

Q4: Which of the following is not an example of 8085 instruction category? 1 point
*****

- ○ Data transfer
- ○ Arithmetic and Logic
- ○ Branching
- ● Cache memory transfer

Q5: In memory mapped I/O, which of the following instructions will not be 1 point
there? *

- ● LDA
- ○ STA
- ○ ADD M
- ○ IN

Q6: Which one of the following instructions may be used for clearing accumulator content? * 1 point

- ◯ XRA A
- ⦿ SUB A
- ◯ MVI A,00H
- ◯ All of these

Q7: Which of the following instruction requires the highest number of T-states for execution? * 1 point

- ⦿ XTHL
- ◯ CALL
- ◯ STAX D
- ◯ DAD H

Q8: Which of the following is not a type of computer language? * 1 point

- ⦿ Medium level language
- ◯ High level language
- ◯ Low level language
- ◯ All of these

Q9: The only language which can be understood by the computer is * 1 point

- ⦿ Machine language
- ○ High level language
- ○ Assembly language
- ○ None of these

Q10: (FE35 H) XOR (CB15 H) is equal to * 1 point

- ○ 3320 H
- ○ FF35 H
- ○ FF50 H
- ⦿ 3520 H

Q11: The output of a logic gate is "1" when all of its input is at logic "0". Then the gate is either * 1 point

- ○ A NAND or an EX-OR gate
- ⦿ A NOR or an EX-NOR gate
- ○ An OR or an EX-NOR gate
- ○ An AND or an EX-OR gate

Q12: For how many T-states ALE will be high during a machine cycle? *   1 point

○ 1 T-state

○ 2 T-state

● 3 T-state

○ 4 T-state

Q13: Which of the following instruction's opcode fetch consists of 6-T states? *   1 point

☐ STA

☑ CALL

☑ PUSH

☐ LDA

Q14: Which of the following instruction's size is 2-byte? *   1 point

☐ ANI

☐ ADI

☐ ADD M

☐ ADD C

Q15: In memory mapped I/O, the instruction(s) used to transfer the data of accumulator is/are: *   1 point

- [ ] IN instruction
- [x] STA instruction
- [x] LDA instruction
- [ ] All of these

Short type questions [10-marks]
Write the answers in paper and attach the scan copy in pdf or image format

Q16: State the need to demultiplex the bus AD0-AD7. How is demultiplexing done?   2 points

⬆ **Add file**

Q17: The memory address of the last location of an 16kB memory chip is FFFF H. Find the starting address.   2 points
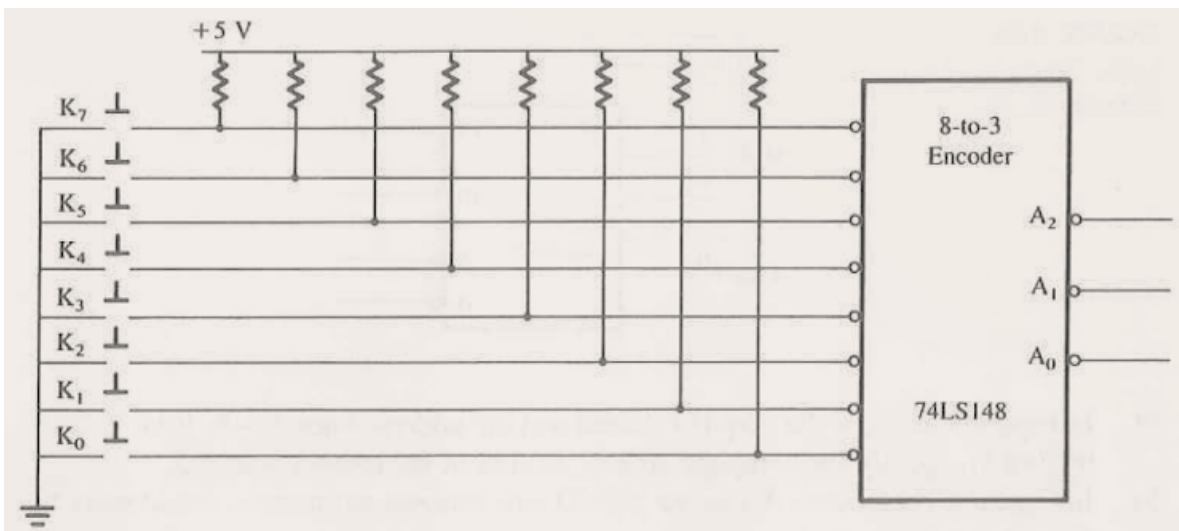
⬆ **Add file**

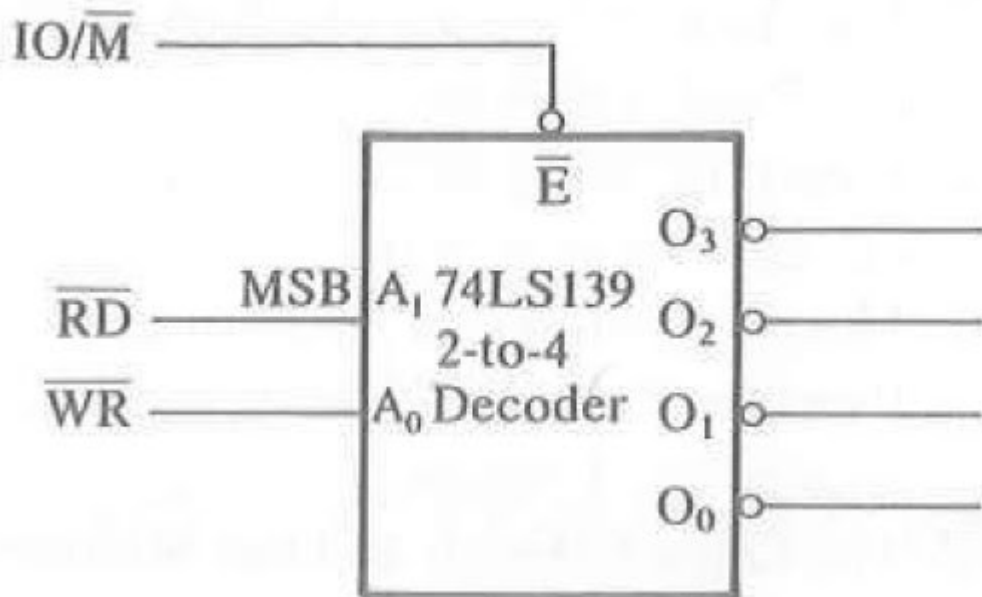**Q18: What is the output of the encoder if the key K3 is pushed?** 2 points

↑ Add file

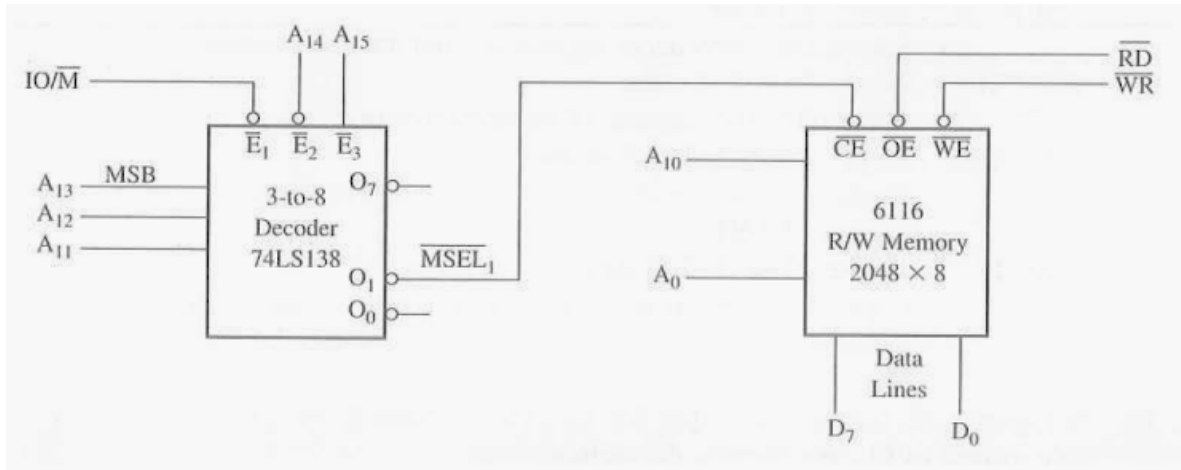**Q19: Identify the appropriate control signals that are generated at the output of the 2 to 4 decoder.** 2 points

↑ Add file

Q20: In the following figure, exchange the address lines A12 and A14, and identify the memory map. **2 points**

A14 A15

IO/$\overline{M}$

$\overline{RD}$
$\overline{WR}$

$\overline{E}_1$ $\overline{E}_2$ E3

A13 — MSB
A12 —
A11 —

3-to-8
Decoder
74LS138

O7

O1
O0

$\overline{MSEL}_1$

A10

CE OE WE

6116
R/W Memory
2048 × 8

A0

Data
Lines

D7   D0

Add file

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