BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

I Semester 2019-2020

CS F342 Computer Architecture

Lab Exam

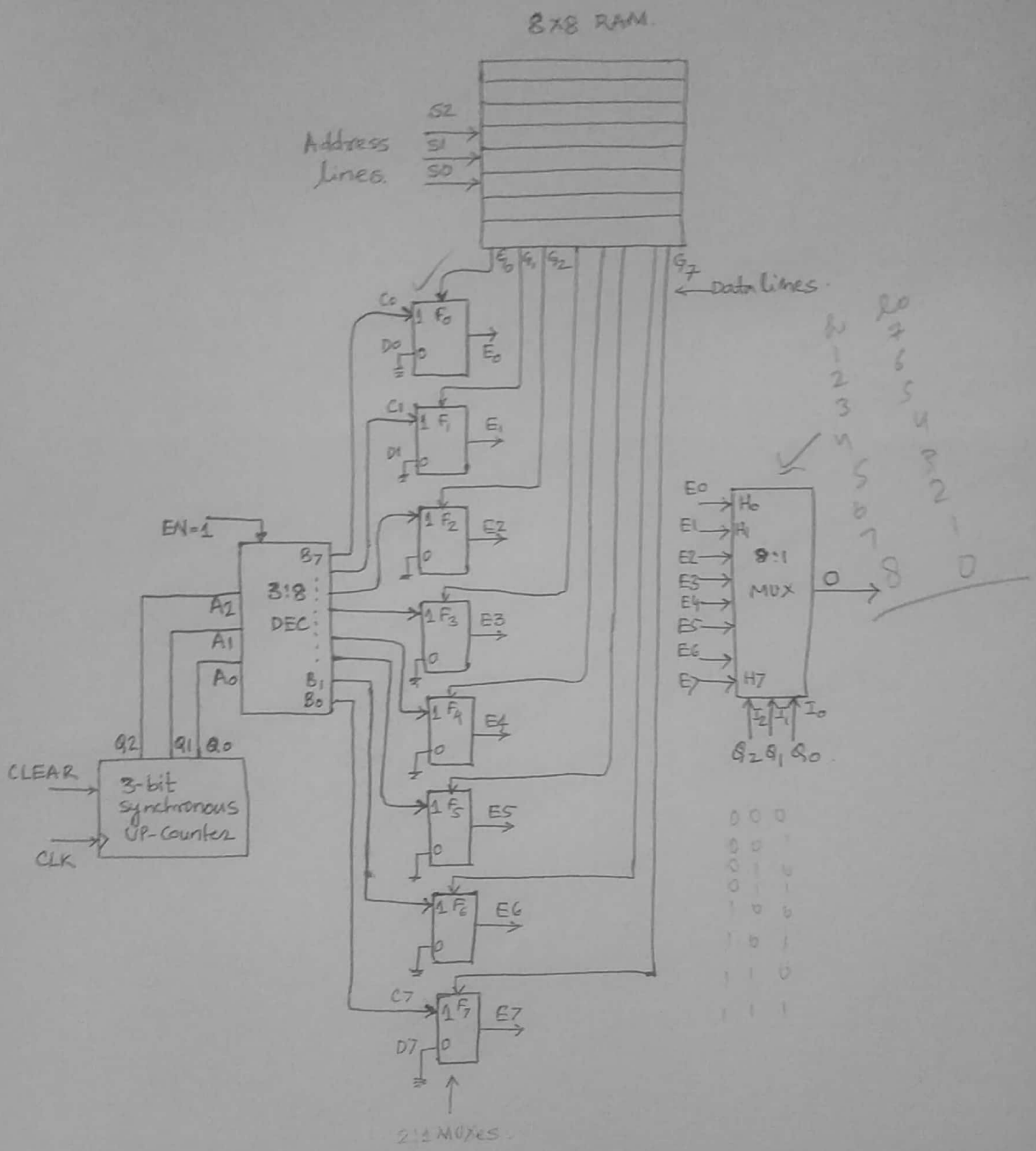
Date: 10/11/2019 TIME: 90 Minutes MM: 33

INSTRUCTIONS: (i) Create a folder on desktop, rename it to your IDNO. (ii) Rename the project with your IDNO (iii) Write your IDNO and name in .v file. Write all modules in a single .v file. Put this .v file in the folder you created on desktop.

On command prompt type and run the following command to set the path:

set path=%PATH%;C:\iverilog\bin;C:\iverilog\gtkwave\bin

Q. Implement the digital circuit as shown below:



PTO→

The circuit consists of one binary counter, one memory of size 8x8, one MUX of size 8:1, eight MUXes of size 2:1 and one decoder of size 3:8. Use the following modules to implement the above circuit (use all signal names as shown in circuit above):

1. **MUX_2x1:** This module implements the functionality of a 2:1 MUX. Implement this module using dataflow modeling.
2. **MUX_8x1:** This module implements the functionality of an 8:1 MUX. Build this module using dataflow modeling. Preferably use only a single assign statement.
3. **MUX_ARRAY:** This module uses the 8, 2:1 Muxes as shown in the figure. Build this module using generate statement.
4. **COUNTER_3BIT:** This module implements the functionality of a 3-bit synchronous binary UP counter with an asynchronous clear. Implement this module using behavioral modelling.
5. **DECODER:** This module implements the functionality of a 3:8 decoder with active high outputs and active high enable. Implement the decoder using behavioral modelling.
6. **MEMORY:** This module implements the functionality of an 8x8 memory. Initialize the 8 memory registers with values 0x01, 0x03, 0x07, 0x0F, 0x1F, 0x3F, 0x7F, 0xFF respectively. i.e. Register0 is initialized with value 0x01, Register1 is initialized with value 0x03, Register2 is initialized with value 0x07 and so on. Build this module using behavioral modelling.
7. **TOP_MODULE:** This module integrates all above modules into a working circuit.

Also write a **test bench module** which:

a. Clears the counter
b. Applies a clock of 1 KHz at the input of the 3- bit counter.
c. Increments the value of S2S1S0 every 8msec. Assume the starting value of S2S1S0 as 000 and increment it to 111 in steps.
d. Show the output O