IIIT Vadodara

CS203: Design and Analysis of Algorithms

Marks: 45

Endterm

Course Instructor: Dr. Dibyendu Roy

Instructions: Clearly write your name and roll number. Solutions must be argued properly for getting credits. Scientific calculator is allowed.

(Q1) **[9 marks]**

Describe Insertion sort algorithm. Prove its correctness. Finally derive its complexity for worst case and best case.

(Q2) **[9 marks]**

State and prove Master theorem for solving recurrences.

(Q3) **[9 marks]**

(a) **(4 marks)** Let $X =< x_1, x_2, \ldots x_m >$ and $Y =< y_1, y_2, \ldots, y_n >$ be sequences and let $Z =< z_1, z_2, \ldots, z_k >$ be any longest common subsequence (LCS) of X, Y. Then prove the followings.

1. If $x_m = y_n$ then $z_k = x_m = y_n$ and $< z_1, z_2, \ldots, z_{k-1} >$ is an LCS of $< x_1, x_2, \ldots, x_{m-1} >$ and $< y_1, y_2, \ldots, y_{n-1} >$.
2. If $x_m \neq y_n$ then $z_k \neq x_m$ implies $< z_1, z_2, \ldots, z_k >$ is an LCS of $< x_1, x_2, \ldots, x_{m-1} >$ and $< y_1, y_2, \ldots, y_n >$.
3. If $x_m \neq y_n$ then $z_k \neq y_n$ implies $< z_1, z_2, \ldots, z_k >$ is an LCS of $< x_1, x_2, \ldots, x_m >$ and $< y_1, y_2, \ldots, y_{n-1} >$.

(b) **(5 marks)** Using the above result derive a recursive solution to find the length of LCS of X, Y. Finally describe an efficient algorithm to find the length of LCS of X, Y.

(Q4) **[9 marks]**

(a) **(5 marks)** Write down the the Huffman algorithm for finding optimal code. Prove its correctness.

(b) **(4 marks)** What is an optimal Huffman code for the following set of frequencies, based on the first 8 Fibonacci numbers `a:1 b:1 c:2 d:3 e:5 f:8 g:13 h:21`? Can you generalize your answer for any general n Fibonacci numbers?

(Q5) **[9 marks]**

Describe the BFS algorithm. Prove that upon termination of BFS on a graph $G = (V, E)$ with a source vertex $s \in V$ it will produce the minimum distance of every vertex $v \in V$ from s if it is reachable. Queue is used.

Indian Institute of Information Technology – Vadodara
End-Semester Examination Autumn 2023-24
B. Tech. (IT & CSE)
EC-201: Digital Logic Design

Time: 3:0 hrs. **Max. Marks: 70**

Attempt all questions

Q. 1 Do the following

(a) $(AC)_{16} = (?)_8$ 2

(b) $(1EF)_{16} = (?)_8$ 2

(c) Simplify the Boolean Function F together with the don't-care conditions in (1) sum-of-products form and (2) product-of-sums form 4

$$F(w, x, y, z) = \Sigma m(0, 1, 2, 3, 7, 8, 10) + \Sigma d(5, 6, 11, 15)$$

(d) The minimum number of 2-input NAND gates required to implement a Half Adder is 2

(e) $(1245)8 = (?)_{16}$ and $(?)_{10}$ 5

Q. 2

(a) A sequential circuit has two D flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and the circuit output are as follows: 5

$$D1 = x'y + xA$$
$$D2 = x'B + xA$$
$$z = B$$

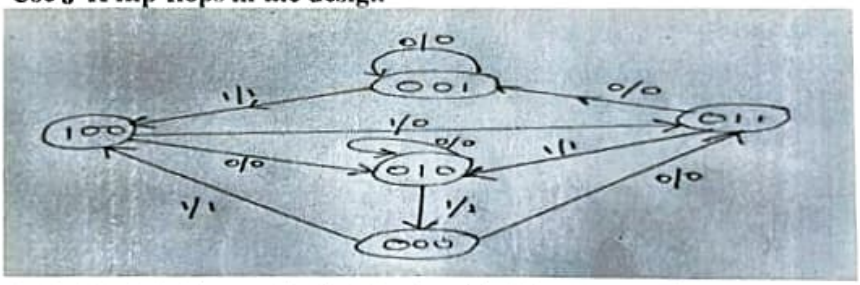
1) Draw the logic diagram of the circuit
2) Tabulate the state table

(b) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift? 5

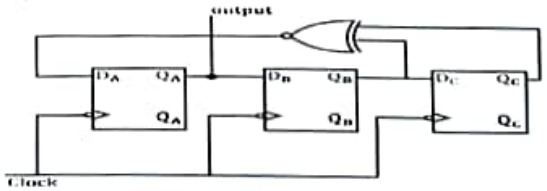
Q. 3

(a) A sequential circuit has three flip-flops A, B, C; one input x; and one output, y. The state diagram is shown in below Figure. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states 15

1) **Use D flip-flops in the design**
2) **Use J-K flip-flops in the design**



(b) Assuming that all flip-flops are in reset condition initially, the count sequence observed at QA in the circuit shown is 5



Q. 4

(a) A combinational circuit using a 8-to-1 multiplexer is shown in the following 5

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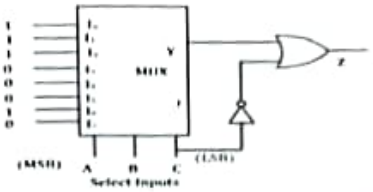
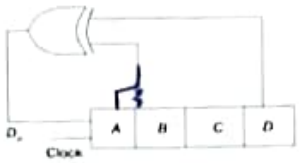
figure. The minimized expression for the output (Z)

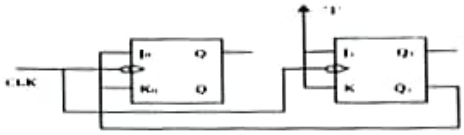


(b) A 4-bit shift register circuit configured for right-shift operation, i.e., Din →A, A→B, B→C, C→D is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 is 5



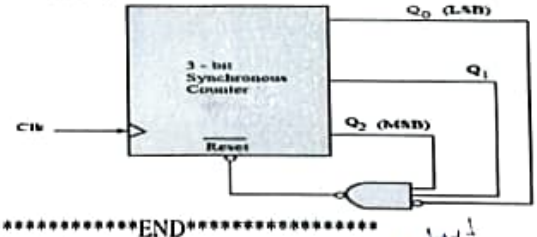
Q. 5 (a) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift? 5

(b) Given that the initial state (Q_1Q_0) is 00, the counting sequence of the counter after six clock is? 5



Q. 6 (a) Design: SR latch using NAND Gate and NOR Gates & SR flip-flop Using NOR Gates. 5

(b) For the circuit shown in the figure, the delay of the bubbled NAND gates is 2 ns and that of the counter is assumed to be zero. If the clock (Clk) frequency is 1 GHz, then find the mod of counter? 5



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End Semester Exam: SC201: Environmental Sciences (B tech 3rd Sem)
Time: As per the institute rules
You are required to submit handwritten copies.

Total Marks: 70
Question paper

Q1: What are some of the contentions related to the concept of sustainable development? (10)
Q2: Explain some of the values, ideologies and philosophies that are associated with environment. (10)
Q3: Elaborate on the role of an individual in environmental problems. (10)
Q4: Explain two environmental protection legislations in India? (10)
Q6: What are common pool resources and elaborate on the management of commons.(10)
Q7:Write short notes on: (20 Marks: 5 marks each)
1. In situ conservation
2. Endangered species in India
3. Renewable and non-renewable energy sources
4. Any environmental movement