



Parameter

Dr. Yash Agrawal
Visiting Faculty, IIIT Vadodara
Associate Professor, DA-IICT Gandhinagar

Introduction

What is
parameter...?

Introduction

- **parameter**
- **defparam**
- **localparam**
- **specparam**
- **genevar**
- **event**

Parameter

Syntax

parameter <parameter name> = <default value>;

Examples

parameter word_size = 16;

parameter factor = word_size/2;

parameter [word_size-1 : 0] bus;

parameter c = 3.0;

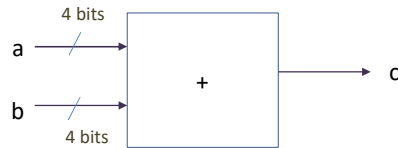
parameter d = 3.0e2;

parameter integer f = 3;

parameter real g = 3;

parameter message = "Hello World";

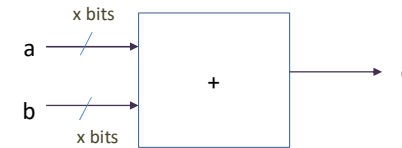
Parameter



For the Block and Verilog HDL, assess its output...

```
module logic1 (c, a, b);
  input [3:0] a, b;
  output [4:0] c;
  assign c = a + b;
endmodule
```

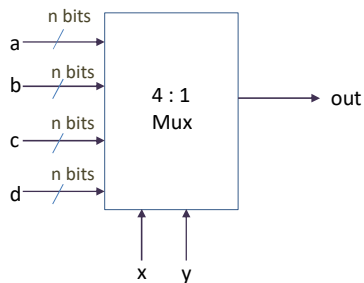
Parameter



Check the same block implementation using
Parameter, defparam, localparam

Parameter

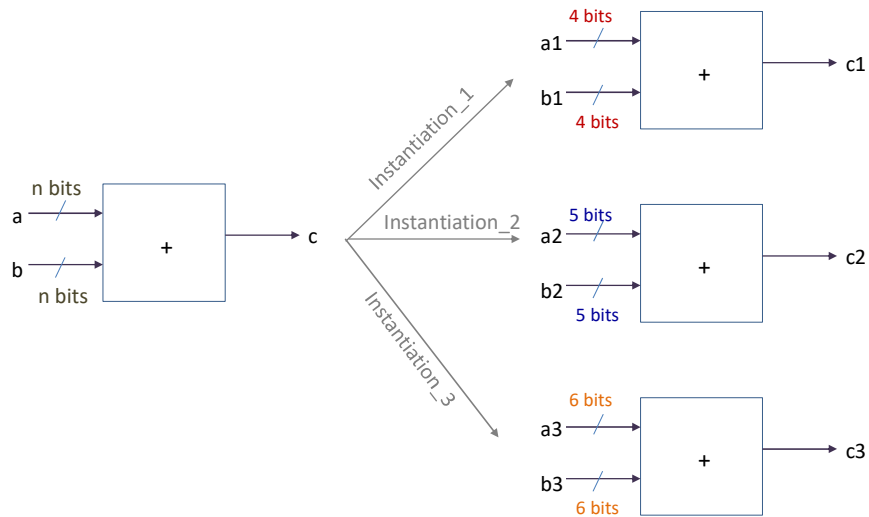
Implementation n-bit wide 4:1 Mux using Parameter



x	y	Out
0	0	a
0	1	b
1	0	c
1	1	d

Instantiation

Instantiation



Instantiation

1) Implementation without using parameter

```
module adder1 (c, a, b);
input [4:0] a, b;
output [5:0] c;
assign c = a + b;
endmodule
```

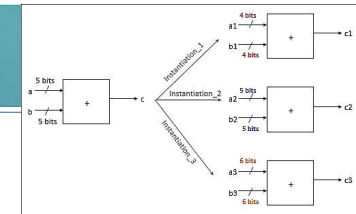
Instantiation

```
module half_adder_tst1 ();
reg [3:0] a1, b1;
wire [4:0] c1;
reg [4:0] a2, b2;
wire [5:0] c2;
reg [5:0] a3, b3;
wire [6:0] c3;

adder1 inst1(c1, a1, b1);
adder1 inst2(c2, a2, b2);
adder1 inst3(c3, a3, b3);
endmodule
```



Identify the output values...!



Instantiation

Parameter Instantiation can be done using the following ways

- Instantiation parameter - Passing by Name
- Instantiation parameter - Passing by Order
- Instantiation parameter - Passing by Namelist

Instantiation

Parameter Instantiation

- Instantiation parameter - Passing by Name

Syntax

```
defparam <instance name>.<parameter name> = <value>;
```

Examples

```
reg [inst1.width : 0] a1, b1;
defparam inst1.width = 3;
```

Instantiation

Parameter Instantiation

- Instantiation parameter - Passing by Order

Syntax

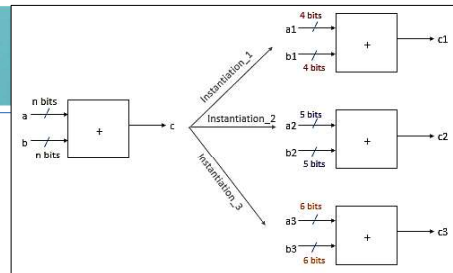
<module called name> #(Sequential list of parameter values) <instance name> (list of variables);

Examples

```
reg [inst1.width : 0] a1, b1;
```

```
adder1 # (3) inst1 (c1, a1, b1);
```

Instantiation



```
module adder1 (c, a, b);  
parameter width = 4;  
input [width:0] a, b;  
output [width+1:0] c;  
assign c = a + b;  
endmodule
```



Instantiate the Module using Parameter

- Passing by Name
- Passing by Order
- Passing by NameList

Instantiation

Parameter Instantiation

- Instantiation parameter - Passing by Namelist

Syntax

<called module name> #(.parameter_name(parameter_value)) <instance name> (list of variables);

Examples

```
reg [inst1.width : 0] a1, b1;
```

```
adder1 # (.width(3)) inst1 (c1, a1, b1);
```

```
adder1 # (.width(3)) inst1 (.a(a1), .b(b1), .c(c1));
```

I am available/approachable at

email: yash_agrawal@iiitvadodara.ac.in
yash_agrawal@daiict.ac.in