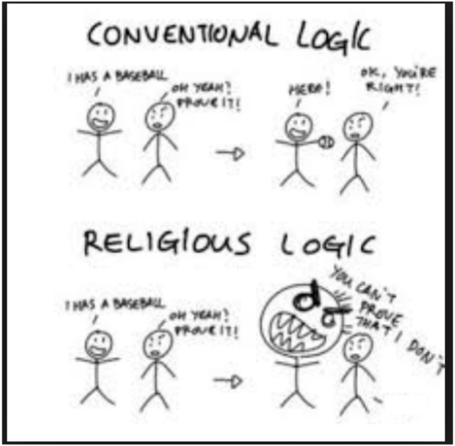


Figure Source:Google

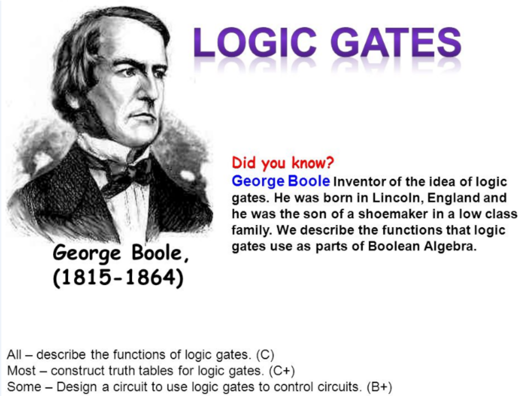


Figure Source:Google

- **Positive and Negative Logic:**

    - Binary: Logic "0" state and Logic "1" state.
    - Digital systems use two different voltage levels to represent the two states.

    $\Rightarrow$ Example: Two voltage levels 0 volts and +5 volts system,

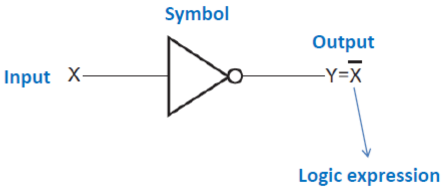
    - Positive logic system: "0" state => 0 volts
      "1" state => +5 volts
    - Negative logic system: "0" state => +5 volts
      "1" state => 0 volts

- **Logic Gate: Quite similar to your home door gate.**
- **Transistor is used as a switch to get functionality like gate.**
- **The most basic building blocks of any digital system including computers.**
- **The logic Gates are used to represents the logic functions to design an digital system.**

- **Basic building blocks:**
- **Basic Gates:**
- NOT Gate
- AND Gate
- OR Gate
- **Universal Gates:**
- NAND Gate
- NOR Gate

- **Other Gates:**
- XOR Gate
- XNOR Gate
- **XOR and XNOR Gates are used in air thematic circuits, Comparator circuits, code converter etc.**

- **NOT Gate:**



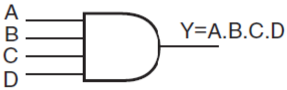
Truth-table

X	Y
0	1
1	0

- **AND Gate:**

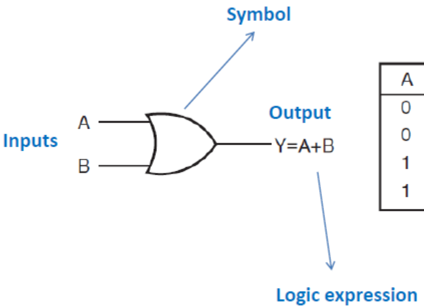
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- **3-input and 4-input AND Gate:**



A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

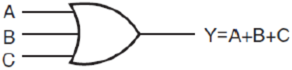
- **OR Gate:**

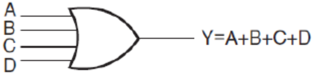


Truth-table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- **3-input and 4-input OR Gate:**



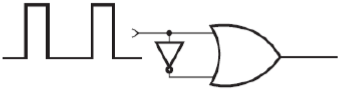


Truth-table of 3 input OR gate

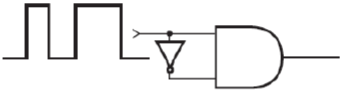
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

- **Exercise:**
- **Design an 3-input AND gate logic circuit using only 2-input AND gates.**
- **Design an 4-input OR gate logic circuit using only 2-input OR gates.**
- **Design an 4-input AND gate logic circuit using only 2-input AND gates.**
- **Design chain of two inverter logic circuit.**

- **Exercise:**



Output waveform ?

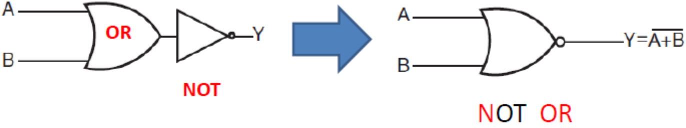


Output waveform ?

- **NAND Gate:**

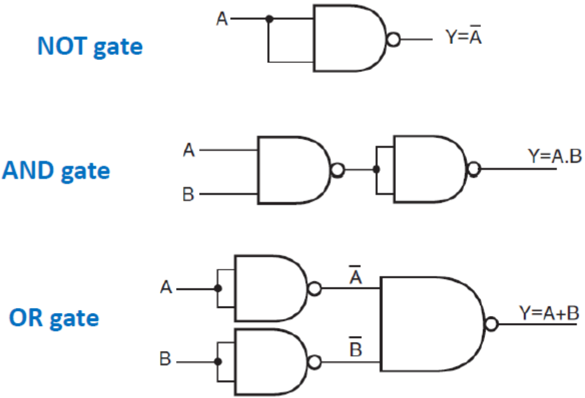
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- **NOR Gate:**

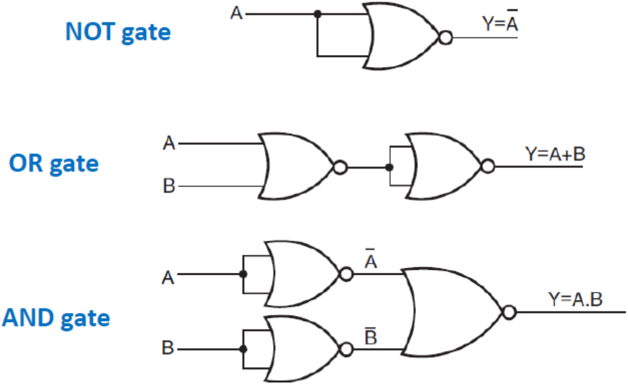


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

- **NAND Gate: Universal**

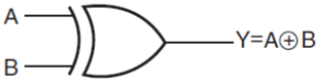


- **NOR Gate: Universal**



- **Exercise:**
- **Design an 3-input AND gate logic circuit using only 2-input NAND gates.**
- **Design an 4-input OR gate logic circuit using only 2-input NOR gates.**
- **Design an 4-input NAND gate logic circuit using only 2-input NAND gates.**
- **Design an 4-input OR gate logic circuit using only 2-input NAND gates.**

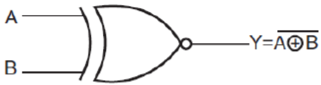
- **Exclusive-OR Gate or X-OR GATE:**



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$Y = (A \oplus B) = \overline{A}B + A\overline{B}$$

- **Exclusive-NOR Gate or X-NOR GATE:**



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

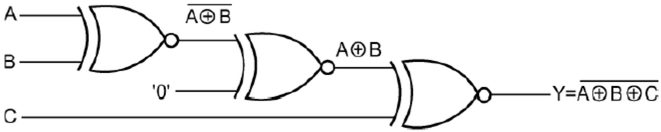
$$Y = (\overline{A \oplus B}) = (A.B + \overline{A}.\overline{B})$$

- **Problem (0):**
- **Design an NOT logic circuit using a 2-input Ex-OR gate.**

- **Solution(0):**

- **Problem(1):**
- **Design an 3-input Ex-NOR logic circuit using 2-input Ex-NOR gates.**

- **Solution(1):**



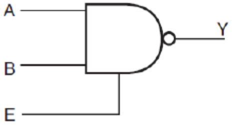
- **Exercise:**
- **Design an 3-input X-OR gate logic circuit using only 2-input X-OR gates.**
- **Design an 4-input X-OR gate logic circuit using only 2-input X-OR gates.**
- **Design an 3-input X-NOR gate logic circuit using only 2-input X-NOR gates.**
- **Design an 4-input X-OR gate logic circuit using only 3-input X-OR gates.**

- **Tristate Gates:**
- **high-impedance state 'Z'.**
- **Active states : Logic '1' and logic '0'.**
- **high-impedance state 'Z' is controlled by an external input known as ENABLE.**

- **ENABLE decides whether the gate is in active or high-impedance state.**
- **An advantage: Inputs and Outputs can be connected in parallel to a common bus line.**

- **Active HIGH ENABLE:**

Active HIGH ENABLE NAND gate

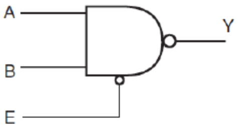


A	B	E	Y
0	0	0	Z
0	0	1	1
0	1	0	Z
0	1	1	1
1	0	0	Z
1	0	1	1
1	1	0	Z
1	1	1	0

Z= High Impedance state

- **Active LOW ENABLE:**

Active LOW ENABLE
NAND gate



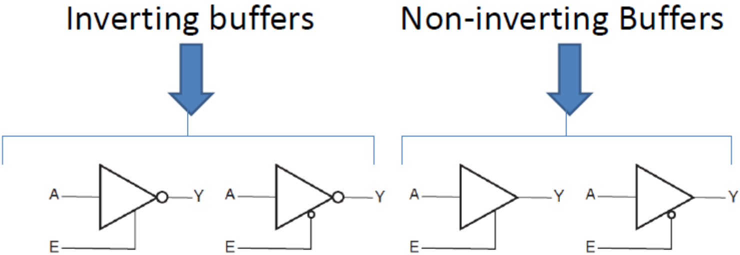
A	B	E	Y
0	0	0	1
0	0	1	Z
0	1	0	1
0	1	1	Z
1	0	0	1
1	0	1	Z
1	1	0	0
1	1	1	Z

Z= High Impedance state

- **Buffer Circuit:**
- **Load driving capability.**
- **Useful in bus-oriented systems.**
- **Driving capability is higher than logic Gates.**
- **Useful in bus-oriented systems.**
- **Normally, the buffers are tristate devices.**

- **Types: Inverting and Non-inverting.**
- **Driver is even larger load-driving capability than a buffer.**

- **Example:**



A	E	Y
X	0	Z
0	1	1
1	1	0

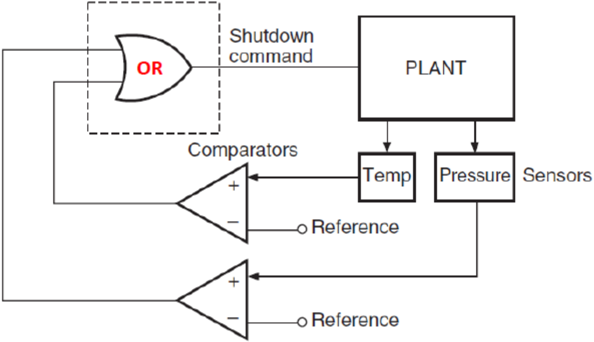
A	E	Y
X	1	Z
0	0	1
1	0	0

A	E	Y
X	0	Z
0	1	0
1	1	1

A	E	Y
X	1	Z
0	0	0
1	0	1

Z = High Impedance State

- **Application:**



- **Application:**