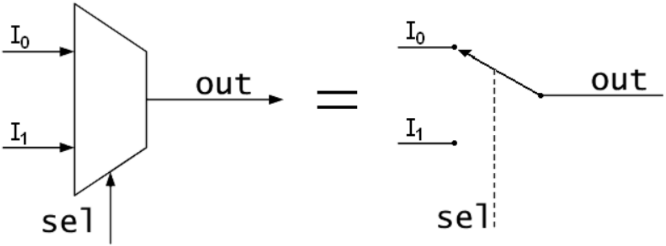
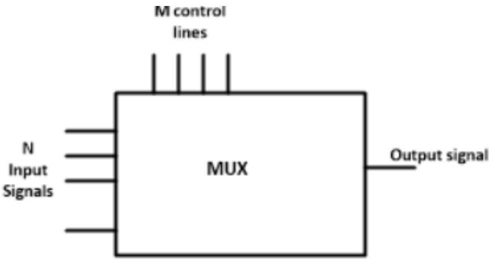
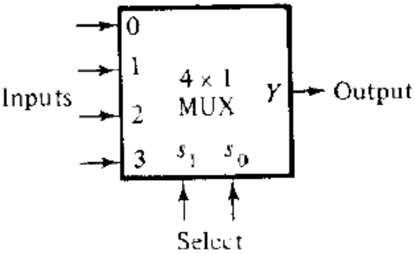
- **Multiplexer (MUX):**
- **MUX is combinational circuit.**
- **Many I/P and one O/P.**
- **Depending on the control I/P or select signal I/P one of the I/P is transferred to the O/P line.**
- **We need n select lines for selecting one of the 2^n inputs.**
- **Example: 2:1 line MUX.**


I_0
I_1
out
sel
=
I_0
I_1
out
sel

- **Multiplexer can deal with two types of data that is analog and digital.**
- **The multiplexer used for digital applications, also called digital multiplexer.**

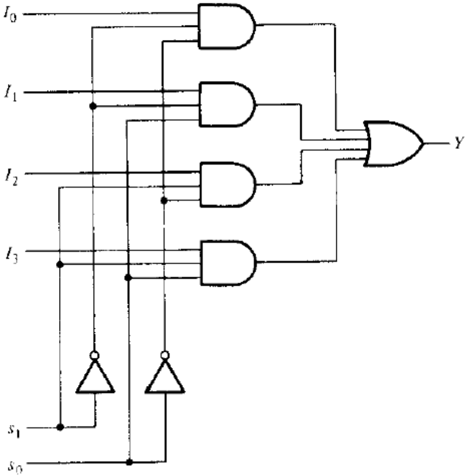

M control
lines
N
Input
Signals
MUX
Output signal

Ex.: 4-to-1 MUX

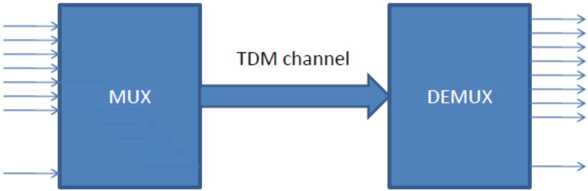


s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

4-to-1 MUX logic circuit

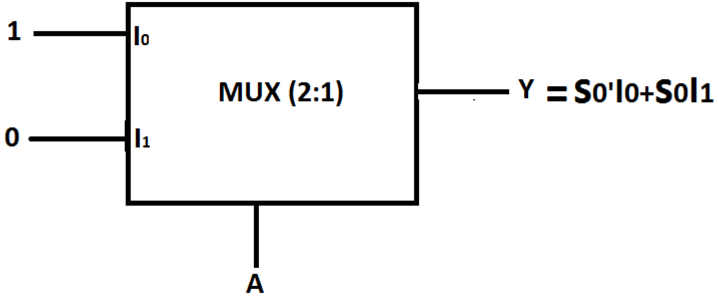


- **Mux applications:**
- **Communication system:**

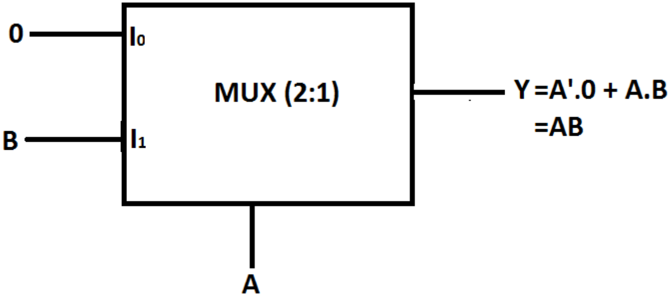


- **Telephone network:**
- **Computer memory:**
- **Computer to satellite:**

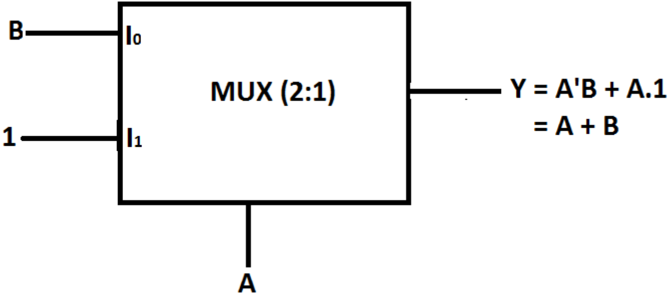
- **MUX as logic Gates:**
- **2:1 MUX as NOT Gate**



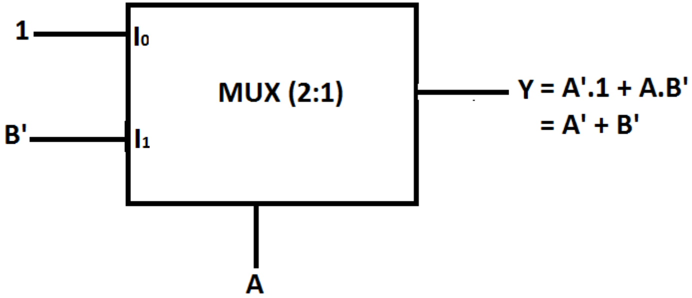
- **2:1 MUX as AND Gate**



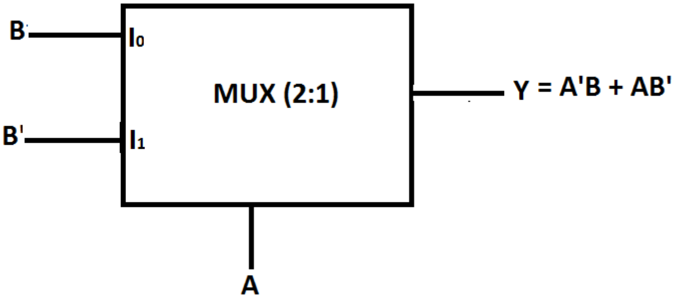
- **2:1 MUX as OR Gate**



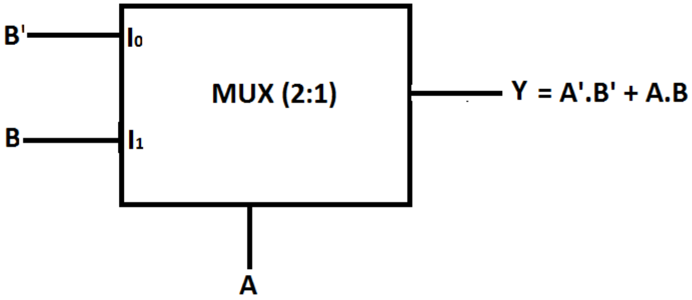
- **2:1 MUX as NAND Gate**



- **2:1 MUX as Ex-OR Gate**

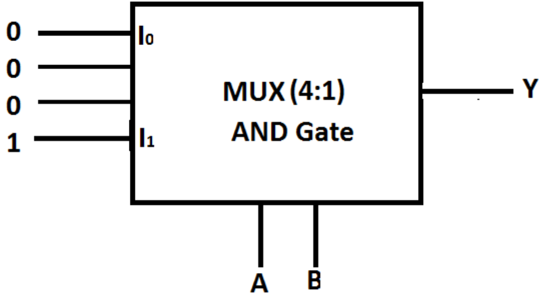

B
B'
I0
I1
MUX (2:1)
Y = A'B + AB'
A

- **2:1 MUX as Ex-NOR Gate**


B'
I0
MUX (2:1)
Y = A'.B' + A.B
B
I1
A

- **Exercise:**
- **No. of 2:1 MUX required for HA.**
- **No. of 2:1 MUX required for HS.**

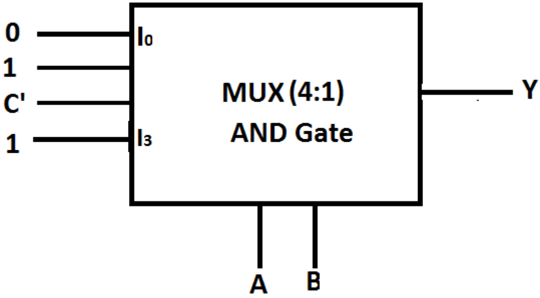
- **4:1 MUX as AND Gate**



- **Exercise:**
- **4:1 MUX as OR Gate.**
- **4:1 MUX as NAND Gate.**
- **4:1 MUX as EX-OR Gate.**
- **4:1 MUX as EX-NOR Gate.**

- **Problem: minimize the function and implement using MUX**

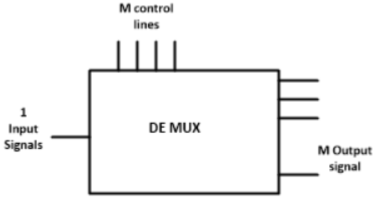
$f(A, B, C) = minterm(0, 1, 4, 6, 7)$


0
1
C'
1
I0
I3
MUX (4:1)
AND Gate
Y
A
B

- **Implementation of higher order MUX using lower order MUX:**
- **4:1 MUX using 2:1 MUX**
- **8:1 MUX using 2:1 MUX**
- **16:1 MUX using 2:1 MUX**

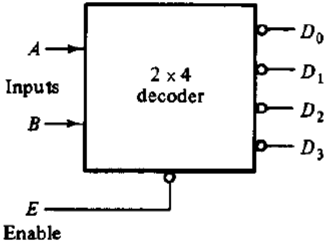
- **16:1 MUX using 4:1 MUX**
- **32:1 MUX using 4:1 MUX**

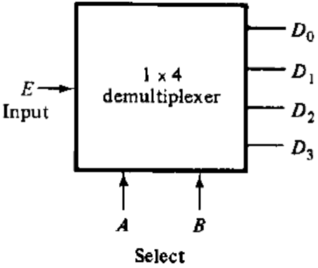
- **De-Multiplexer (DMUX):**
- **DMUX is combinational circuit.**
- **One I/P and many O/P.**
- **By applying control signal, we can steer any input to the output.**

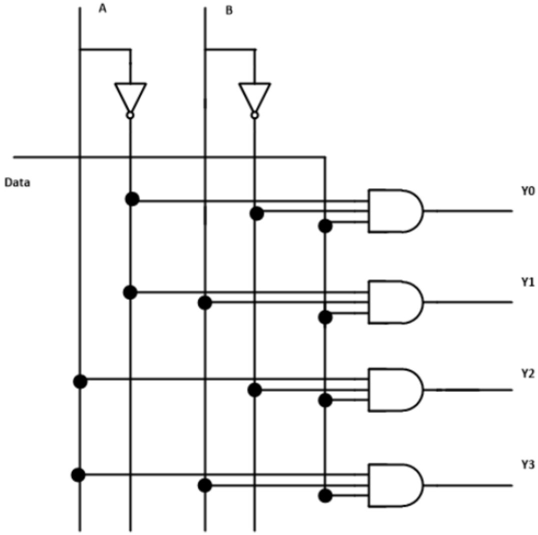

M control lines
1 Input Signals
DE MUX
M Output signal

Demultiplexer

a decoder with an Enable input






A
B
Data
Y0
Y1
Y2
Y3

- **Implementation of higher order DMUX using lower order DMUX:**
- **1:4 DMUX using 1:2 DMUX**
- **1:8 DMUX using 1:2 DMUX**
- **1:16 DMUX using 1:2 DMUX**

- **1:16 DMUX using 1:4 DMUX**
- **1:32 DMUX using 1:8 DMUX**