Experiment No:3

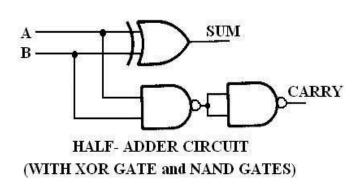
Construction of half adder and full adder using XOR and NAND gates and verification of its operation.

Apparatus: Logic trainer kit, Logic gates: XOR (IC 7486), NAND(7400).

Theory:

A half adder can add two bits at a time. Its outputs are SUM and CARRY. For two bit addition-SUM will be 1, if only one input is 1(X-OR operation). CARRY will be one, when both inputs are 1 (AND operation). So, by using one AND gate and one X-OR gate, a half adder circuit can be constructed. Boolean expressions for the outputs are: SUM = AB' + A'B CARRY = AB. Full adder sum and carry expressions can be found out with help of its truth table.

\mathbf{A}	В	SUM	CARRY	$SUM = A'B + AB'$ $SUM = A \oplus B$ $CARRY = AB$
0	0	0	0	
0	1	1	0	
1	0	1	0	
1	1	0	1	
В –				· ·
		101		CARRY
		HALI	- ADDER	CIRCUIT
ТН	on	e AND	GATE at	d ONE XOR GATE)



Procedure:

- 1. Connect the trainer kit to AC power supply.
- 2. Connect logic sources to the inputs of the adder.
- 3. connect output from SUM and CARRY to logic indicators.
- 4. Apply various input combinations to the adder.
- 5. Observe the SUM and CARRY outputs, verify the truth table for each input/ output combination.
- 6. Switch off the ac power supply.