Indian Institute of Information Technology – Vadodara
End-Semester Examination Autumn 2022-23
B. Tech. (IT & CSE)
EC-201: Digital Logic Design

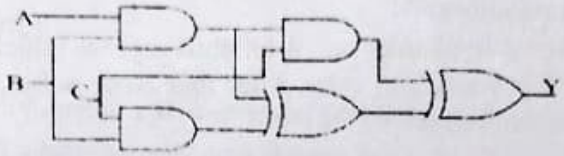
Time: 3:0 hrs | Max. Marks: 75

Attempt all questions

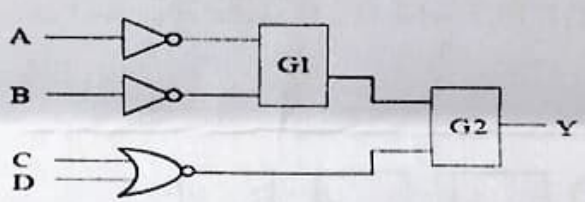
Q. 1 Do the followings

(a) $(110110001)_2 = (\ ?\ )_{10}$ 2

(b) The output of the combinational circuit given below is: 3



(c) In the figure shown, the output is required to be $Y = AB + \overline{C}\,\overline{D}$. The gates G1 and G2 must be, respectively, 2



(d) Simplify the Boolean function F together with the don't-care conditions in (1) sum-of-products form and (2) product-of-sums form: 3

$F(w, x, y, z) = \Sigma\, m(0, 1, 2, 3, 7, 8, 10) + \Sigma\, d(5, 6, 11, 15)$

Q. 2 (a) A sequential circuit has two D flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and the circuit output are as follows: 5

$D1 = x'y + xA$

$D2 = x'B + xA$

$z = B$

a. Draw the logic diagram of the circuit

b. Tabulate the state table

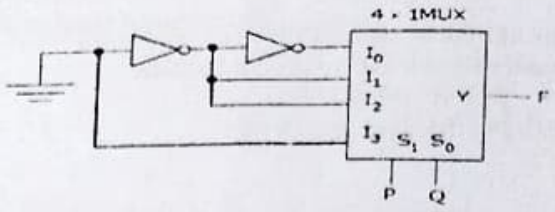
(b) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift? 5

Q. 3 (a) Minimize the function using K-Map $F(A, B, C) = \Sigma m(1, 2, 5, 7) + \Sigma d(0, 4, 6)$ and what are the limitations of K-map? 5

(b) What is the minimum number of 2-input NOR gates required to implement a 4-variable function, expressed in sum-of-minterms form as $f = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$? Assume that all the inputs and their complements are available. 5

Q. 4 (a) The logic function implemented by the circuit below is (ground implies logic 0)? 5

P. T. O



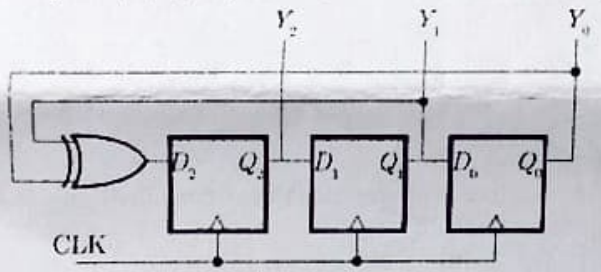
(b) Conditionals in a continuous assignment are specified through the "?:" operator. Conditionals get inferred into a multiplexer. For example, the following is the code for a simple multiplexer 5

assign wire1 = (sel==1'b1) ? a : b;

What is the meaning of above statement and also draw the circuit diagram and out put waveform ?

(c) A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, what is the content of the register after each shift? 5

Q. 5 A three bit pseudo random number generator is as shown in the figure. Initially, the value of output $Y(Y_2 Y_1 Y0)$ is set to 111. The value of output Y after 8th clock cycles is ? 5



Q. 6

(a) How to design Synchronous Counter? Give its necessary steps. 5

(b) Design a 3-bit Asynchronous up Counter. Draw the output diagram/Timing Diagram. 5

(c) Convert SR flip-flop to JK flip-flop and draw the state diagram of SR flip-flop and JK flip-flop. 5

(d) Define Ring counter and Johnson counter and find usable state and no usable state. 5

(e) A 4-bit Modulo-6 ripple counter uses J-K flip-flop. If the propagation delay of each FF is 50 ns, the maximum clock frequency that can be used is equal to ___MHz. 5

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