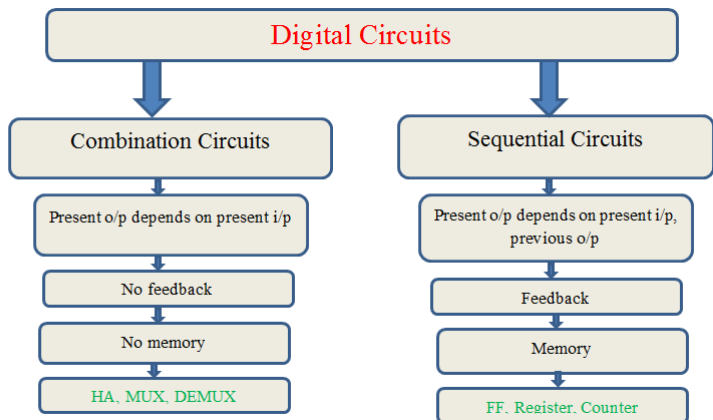
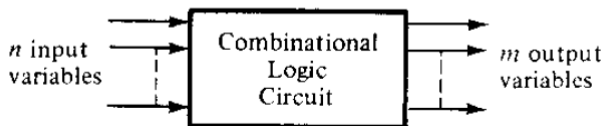


- **Combination circuits:**
- **Sequential circuits:**

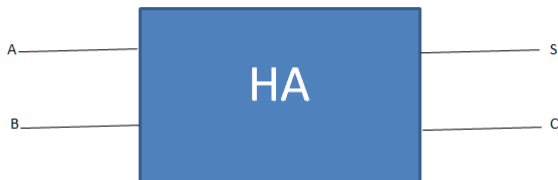


Block schematic



- **Procedure to design combination circuits:**
- **Identify the I/O and O/P.**
- **Truth Table.**
- **Logical expression.**
- **Minimize the logical expression if possible.**
- **Implement the logic circuit.**

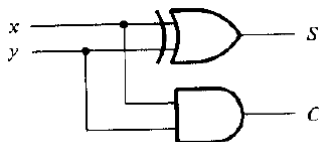
- **HALF ADDER (HA):**



- **Truth Table:**

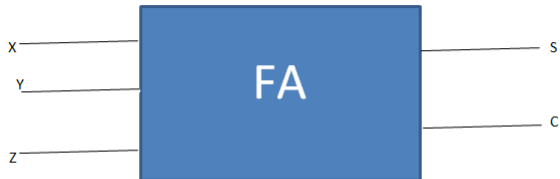
x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

- **Logical Expression:**
- $SUM = X'Y + XY'$
- $CARRY = XY$
- **HA Circuit:**



- **Important points:**
- **Minimum No. of NAND Gates: 5**
- **Minimum No. of NOR Gates: 5**
- **Minimum No. of MUX: 3**
- **No. of decoder: 1**

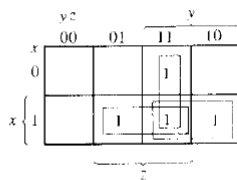
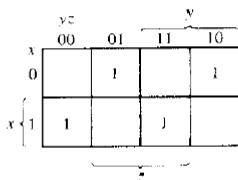
- **FULL ADDER (FA):**



Full Adder

To add three bits, i.e., including a carry

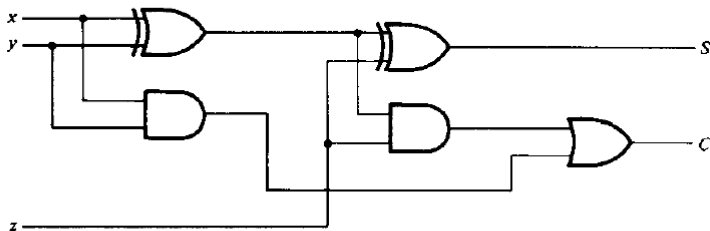
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



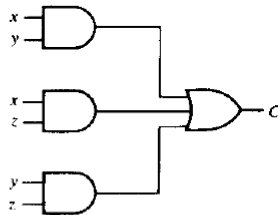
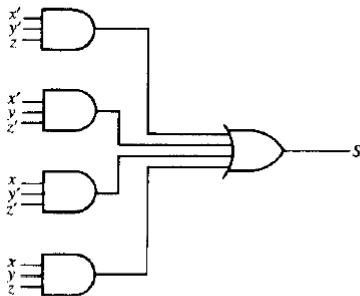
$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$C = xy + xz + yz$$

Full Adder with two half-adders and an OR gate



Full Adder in SOP form



- **Exercise:**
- **No. of HA and other combination circuit required to design the FA.**
- **Minimum No. of NAND Gates required to design the FA.**
- **Minimum No. of NOR Gates required to design the FA.**

- **Half Sub-tractor (HS):**

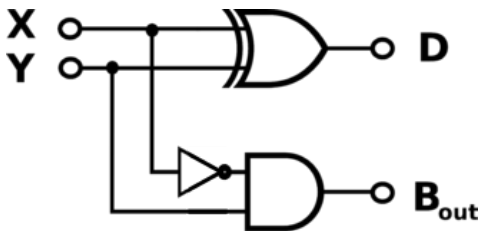


Half-subtractor

x	y	B	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

$$D = x'y + xy'$$

$$B = x'y$$



- **Exercise:**
- **Minimum No. of NAND Gates required to design the HS.**
- **Minimum No. of NOR Gates required to design the HS.**

Full-subtractor

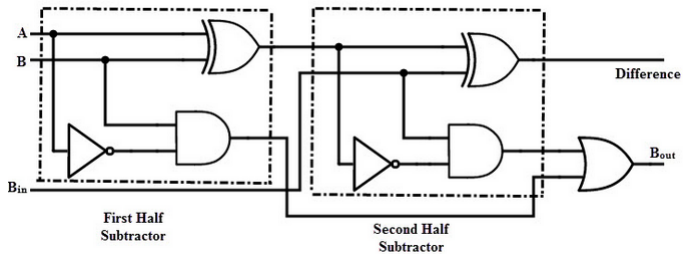
x	y	z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = x'y'z + x'yz' + xy'z' + xyz$$

$$B = x'y + x'z + yz$$

Please draw the logic diagram.

- **Logic Diagram:??**



- **Adder Types:**
- **Parallel Adder**
- **Serial Adder**
- **Look ahead carry adder**

- 4-bit parallel adder:
- 3 FA and 1 HA.
- or 4 FA are required.

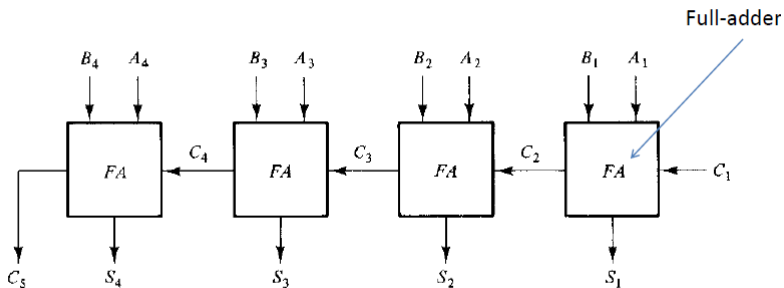
	FA	FA	FA	HA
	1	1	0	1
	1	0	1	1
	<u>1</u>	<u>1</u>	<u>1</u>	
1	1	0	0	0

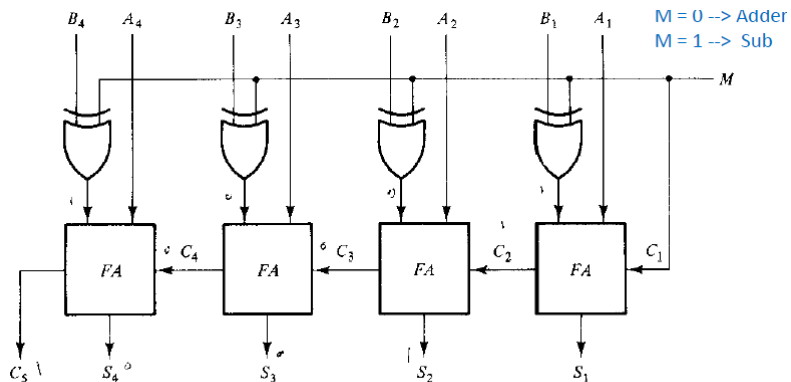
- **Parallel adder is used to add groups of bits.**
- **To add two n -bit No. it requires the $(N-1)$ FA and one HA or N FA.**

Or

- **$(2N-1)$ HA and $(N-1)$ OR Gates required.**

4-bit binary adder

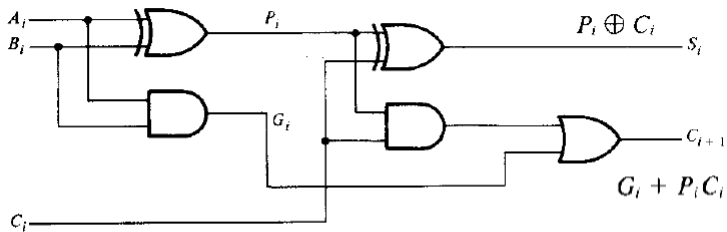




- PA is also known as ripple carry adder.
- Propagation delay from i/p carry to o/p carry.
- In PA each FA will provide 2 logic gate delay.
- The N-bit PA propagation delay.

$$T_{delay} = 2Nt_{pd}$$

- **Look Ahead Carry Adder:**
- **Propagation delay in PA.**
- **No. of bits increases, speed of the circuit becomes slow.**
- **To avoid this look ahead carry generator is used.**



$$G_i = A_i B_i \quad \text{Carry generate}$$

$$P_i = A_i \oplus B_i \quad \text{Carry propagate}$$

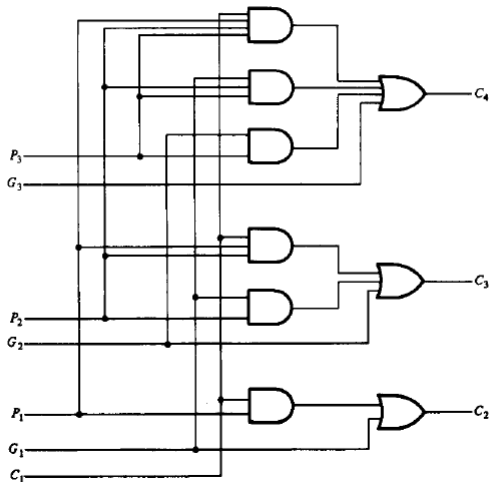
Carry outputs for each stage from the 4-bit adder

$$C_2 = G_1 + P_1 C_1$$

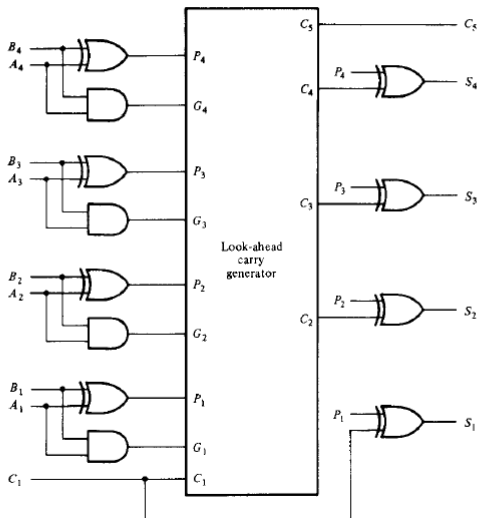
$$C_3 = G_2 + P_2 C_2 = G_2 + P_2(G_1 + P_1 C_1) = G_2 + P_2 G_1 + P_2 P_1 C_1$$

$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_1$$

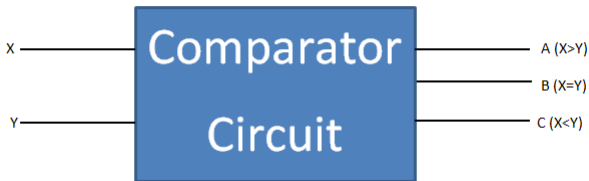
Carry Look-Ahead (CLA) generator



4-bit adder with CLA



- **Comparator:**



Truth Table:

X	Y	A	B	C
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Logic Expression:

$$A = XY'$$

$$B = X'Y' + XY$$

$$C = X'Y$$

- **Exercise:**
- **Implement the comparator circuit using basic Gates.**
- **Implement the comparator circuit using NAND Gates only.**