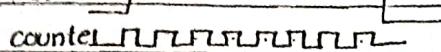


## ★ COUNTERS:-

⇒ Counters are basically used to count no of clock pulse applied: it can also be used for frequency divider, & time measurement, frequency measurement, Range measurement, pulse width.

Pulse.



$$16 \times \text{Pulse width} = \text{Total width.}$$

⇒ Also used for waveform generator.

⇒ with  $n$ -ff, max. possible stage in the counter is  $2^n$ .

$$N \leq 2^n$$

$$\text{or, } n \geq \log_2 N.$$

where  $N$  = no. of stages

$n$  = no. of FF.

Depending on clock pulse applied counters of two types:-

(i) Asynchronous

(ii) Synchronous

Asynchronous	Synchronous
1. Different FF are applied with different clock.	1. All FF are applied same clock.
2. It is slower.	2. It is faster.
3. Fixed count sequence ie. up or down.	3. Any count sequence is possible.
4. Decoding errors will present.	4. No decoding error will present.
5. Ripple counter	5. Ring counter

- ⇒ No. of stage use in counter mean modulus of counter.  
 i.e. if MOD 5 counter = 5 stage.  
 MOD n counter = n stage

$$f \rightarrow \text{Mod}_N \rightarrow f/N$$

- Q. Q1. A decade counter is applied with frequency of 10MHz then O/P frequency is ...

$$\text{Sol} : f_{\text{out}} = f_{\text{in}} = \frac{10 \text{ MHz}}{10} = 1 \text{ MHz}$$

⇒ let MOD M and MOD N are cascaded then it will act as MOD MN counter.

$$f_{\text{in}} \rightarrow \text{MOD M} \rightarrow \text{MOD N} \rightarrow f_{\text{out}} \Rightarrow f_{\text{in}} \rightarrow \text{MOD MN} \rightarrow f_{\text{out}}$$

content :-

Basic

Ripple counter

Non binary ripple counter

Ring counter

Johnson counter

Synchronous series carry

Synchronous parallel carry

Synchronous counter design and Analysis.

#### (A) Ripple counter :-

- ⇒ It is a Asynchronous counter.
- ⇒ Different FF used different clock pulse.
- ⇒ Toggle mode.
- ⇒ Only one FF is applied with external CLK and other FF's are CLK is from previous FF O/P. (whether Q or  $\bar{Q}$ ).
- ⇒ The FF applied with external CLK will acts as LSB bit.

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(3)

⇒ In  $n$  bit ripple counter propagation delay of each ff is  $t_{pdff}$ . then. time period of CLK is,

$$t_{clk} \geq n t_{pdff}$$

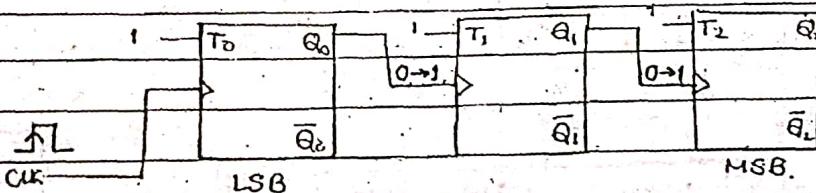
$$f_{clk} \leq \frac{1}{n t_{pdff}}$$

$$t_{max} = \frac{1}{n t_{pdff}}$$

Note:-

- (i) -ive edge trigger  $\rightarrow Q$  as clock  $\rightarrow$  up counter
- (ii) +ive " "  $\rightarrow \bar{Q}$  as clock  $\rightarrow$  up counter.
- (iii) -ive " "  $\rightarrow \bar{Q}$  as clock  $\rightarrow$  down counter.
- (iv) +ive " "  $\rightarrow Q$  as clock  $\rightarrow$  down counter.

### 3-Bit Ripple counter (Down counter):-



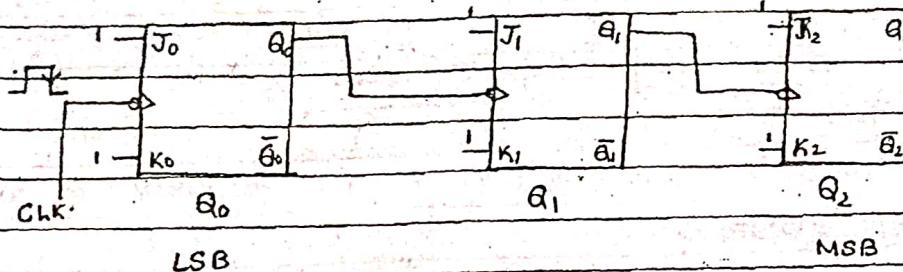
#### (i) Explanation :-

- ⇒ The ckt shown in fig. Q<sub>0</sub> toggles for every clock pulse.
- ⇒ Q<sub>1</sub> toggles when Q<sub>0</sub> changes from 0 to 1.
- ⇒ Q<sub>2</sub> toggles when Q<sub>1</sub> changes from 0 to 1.

#### (ii) Truth table:-

CLOCK	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1

### 3 bit ripple counter :- (up counter)



i) Explanation :-

- ⇒ The ckt. shown in fig.  $Q_0$  toggle for every clk pulse
- ⇒ An change when  $Q_{n-1}$  change from 1-0. i.e.  $Q_1$  changes when  $Q_0$  changes from 1-0.

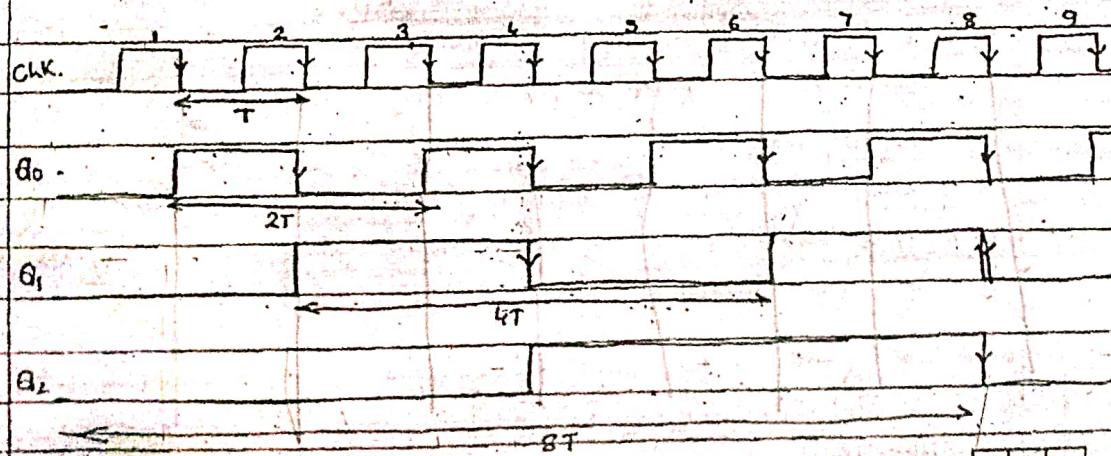
ii) Truth table :-

CLK	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

⇒ This is up counter.

⇒ It is also called MOD 8 ripple counter.

iii) Timing Diagram :-



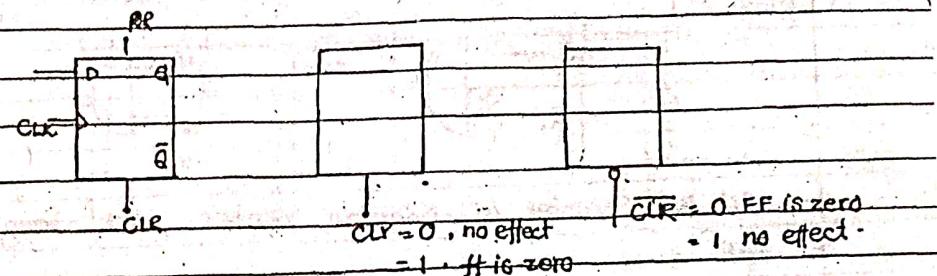
clock  $\Rightarrow$  Clear and preset are known as Asynchronous I/P.

like S, R, J, K, D, T are Synchronous I/P.

Clear:- clear is used to reset our FF or counter.

Preset:- preset is used to set our FF or counter.

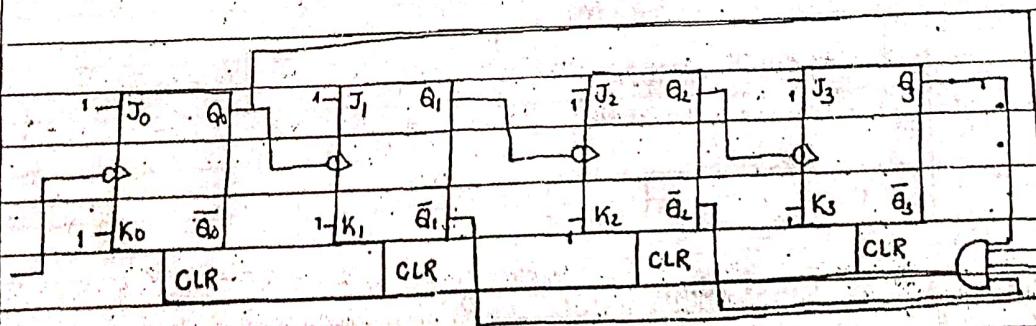
is delay



(B) Non Binary Ripple counter:-

(B) BCD Counter  $\Rightarrow$  (Decade counter)

$\Rightarrow$  4 flip flop used.



CLK Q<sub>3</sub> Q<sub>2</sub> Q<sub>1</sub> Q<sub>0</sub>

0 0 0 0 0

1 0 0 0 1

2 0 0 1 0

3 0 0 1 1

4 0 1 0 0

5 0 1 0 1

6 0 1 1 0

7 0 1 1 1

8 1 0 0 0

9 1 0 0 1

10 1 0 0 0

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(1010)

PAGE [ ] [ ]

Q<sub>3</sub> Q<sub>2</sub> Q<sub>1</sub> Q<sub>0</sub>

⇒ This is called ripple counter. because the input clock is the o/p of previous FF output. this is just like ripple. then called Ripple counter.

⇒ if the o/p is (000) and clock is applied then  $t_{pd़t}$  is delay

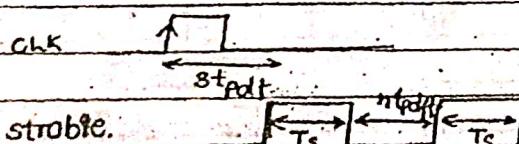
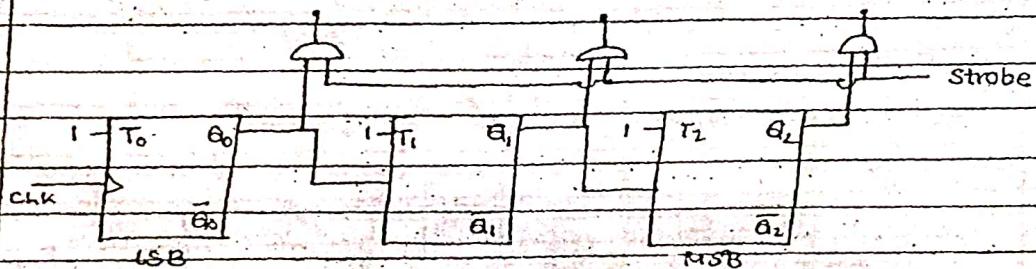
000

$t_{pd़t} \rightarrow \{ 001 \}$  unwanted or decoding error.  
 $t_{pd़t} \rightarrow \{ 011 \}$  also called transient state.

111

⇒ Decoding errors or transient state present in ripple counter due to propagation delay.

⇒ To avoid decoding error strobe signal is used.



⇒ i.e. strobe signal is zero for  $t < t_{pd़t}$  and after that it is one for next clock. then all the o/p is zero for the transient time therefore due to strobe signal we can remove decoding error.

$$T_{clk} \geq n t_{pd़t} + T_s$$

⇒ In ripple counter with  $n$  ff. max. possible state is  $2^n$ .

⇒ frequency after  $n$  8FF in the Ripple counter is  $f/2^n$ . (i.e. for 3-FF o/p is  $f/8$ )

$$\Rightarrow n \text{ bit} \Rightarrow n \text{ state}$$

$$\Rightarrow t_0 = \frac{t}{n}$$

$\Rightarrow$  Phase shift b/w generated waveform is  $360/n$ .

$$\phi = \frac{360}{n}$$

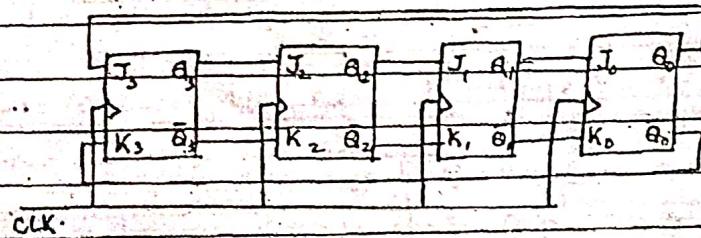
Application :-

$\Rightarrow$  used in stepper motor control.

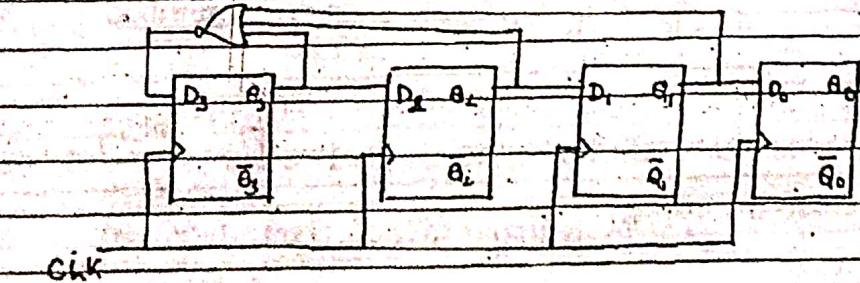
$\Rightarrow$  in Analog to Digital converter

$\Rightarrow$  No. of unused state in ring counter is  $2^n - n$ .

ring counter using J-K :-



\* self starting Ring counter! -

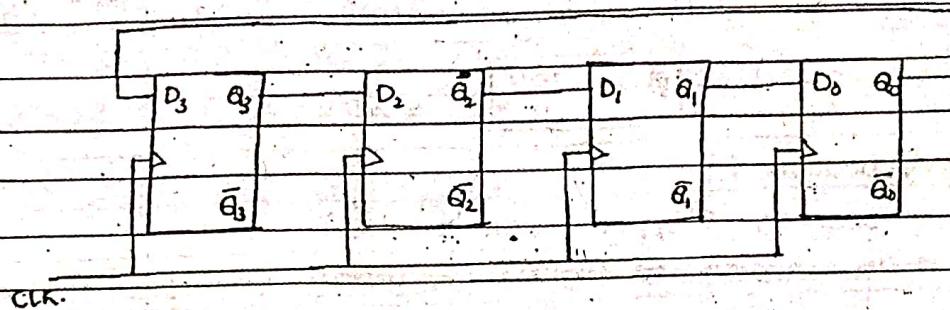


$\Rightarrow$  Advantage of Ring counter is decoding is simple. to decode no logic gate are required.

$\Rightarrow$  Last o/p can not be connected in the J/P of self start ring counter.

## (i) Ring Counter :- (Synchronous counter)

⇒ The last ff o/p is connected to first ff E/P.



## (ii) Explanation:-

⇒ Only one ff o/p is high and remaining FF are low.

⇒ In 4 bit ring counter 4 states are there. (i.e. For n FF is n states).

## (iii) Truth table :-

CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

↳ 4 states.

⇒ In synchronous counter the +ive edge or -ive edge o/p remains same.

## (iv) Time Diagram:-



CLOCK	$Q_3\ Q_2\ Q_1\ Q_0$	$\rightarrow$	$\bar{Q}_3\ \bar{Q}_0$
0	0 0 0 0	$\rightarrow$	$\bar{Q}_3\ \bar{Q}_0$
1	1 0 0 0	$\rightarrow$	$Q_3\ \bar{Q}_2$
2	1 1 0 0	$\rightarrow$	$Q_2\ \bar{Q}_1$
3	1 1 1 0	$\rightarrow$	$Q_1\ \bar{Q}_0$
4	0 1 1 0	$\rightarrow$	$\bar{Q}_3\ Q_0$
5	0 1 1 1	$\rightarrow$	$\bar{Q}_3\ Q_2$
6	0 0 1 1	$\rightarrow$	$\bar{Q}_2\ Q_1$
7	0 0 0 1	$\rightarrow$	$\bar{Q}_1\ Q_0$
8	0 0 0 0		

$\Rightarrow$  In Johnson counter to decode each state one two I/P. AND / NOR gate used.

Disadvantage:

$\Rightarrow$  lock out may occur. (when counter enter into unused state)

Note:- In synchronous counter propagation delay of each counter is  $t_{pdff}$ . then.

$$f_{clk} \geq t_{pdff}$$

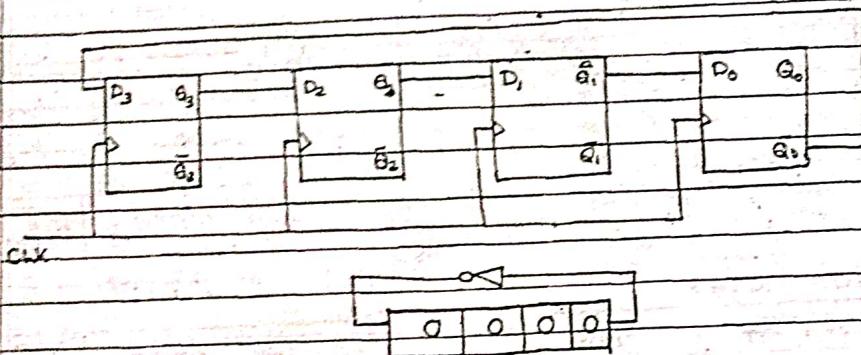
$$f_{clk} \leq \frac{1}{t_{pdff}}$$

$$f_{max} = \frac{1}{t_{pdff}}$$

} In synchronous counter.

## (i) Johnson Counter :-

- ⇒ Symmetric o/p waveform.
- ⇒ 2-stages are there for 4 bit counter.
- ⇒ phase shift =  $\frac{360}{4} = 90^\circ$
- ⇒ It is just like SISO register.



## (ii) Truth Table :-

CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

8 state

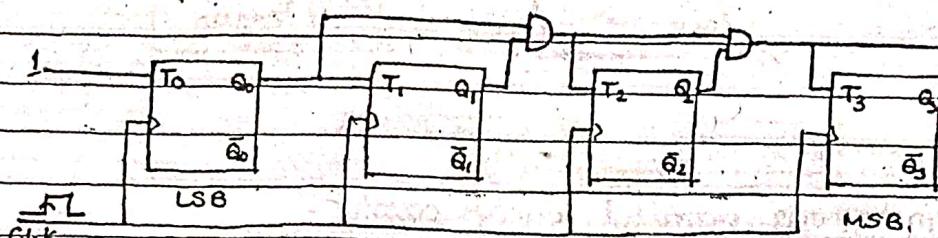
⇒ Total no. of used state = 8

⇒ Total no. of unused state =  $2^n - 8 = 2^4 - 8 = 8$  state.

⇒ Also called Twisted counter, Mabes counter or, creeping counter or, Walking counter or, switch tail counter.

(12)

(1)

(A) Synchronous Series carry counter :-

## ii) Explanation :-

- ⇒ CKt shown in fig. is Synchronous series carry up counter.
- ⇒ In this counter  $Q_0$  toggles for every clock pulse.
- ⇒  $Q_1$  toggles when  $Q_0 = 1$  and clock is applied.
- ⇒  $Q_2$  toggles when  $Q_1 = Q_0 = 1$  and clock applied.
- ⇒  $Q_3$  will toggles when  $Q_2 = Q_1 = Q_0 = 1$  and clock applied.
- ⇒ This CKt may be down counter when  $\bar{Q}$  is connected to T.

## iii) Truth table :-

CLOCK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

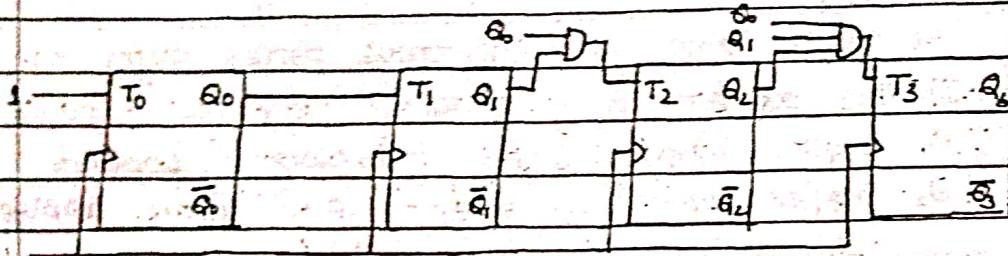
⇒ To provide down counter used  $\bar{Q}$  o/p to provide next stage.

Sip.

$$T_{CLK} \geq t_{PDFF} + (n-2) t_{PDAND}$$

Prob  
Sett

(B) Synchronous parallel carry counter :-



Sol:

⇒ Faster than series carry counter.

⇒ Disadvantage is increased I/P pin of AND Gate.

$$T_{CLK} \geq t_{PDFF} + t_{PDAND}$$

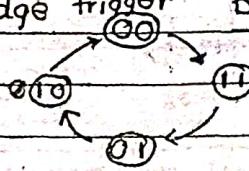
⇒ Sgno

⇒ Ripple counter < Synchronous serial carry < Synchronous parallel carry counter, for faster logic.

Synchronous counter design for the given sequence :-

Problem: Design a synchronous counter for the count sequence  $0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 0$

Sol:- Using +ive edge trigger D-FF.



STATE DIAGRAM.

Sol:- Procedure :-

- (i) Identify no. of FF and I/p and O/p.
- (ii) construct state table.
- (iii) logical expression for I/p.
- (iv) Minimize.
- (v) Implement the ckt.

Now,

(i)	$D_1$	$Q_1$	$D_0$	$Q_0$
		$\bar{Q}_1$		$\bar{Q}_0$

CLK.

(ii) State table:-

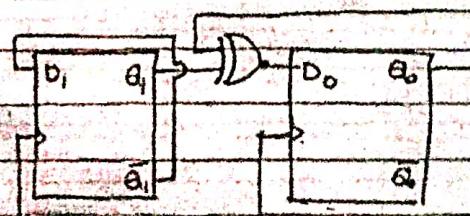
Present state Synchronous	Next state		$D_1$ , $D_0$
	$Q_1$ , $Q_0$	$Q_1, Q_0$	
00	11	11	1 01
11	01	01	0 1
01	10	10	1 0
10	00	00	0 0

(iii) logical expression :-

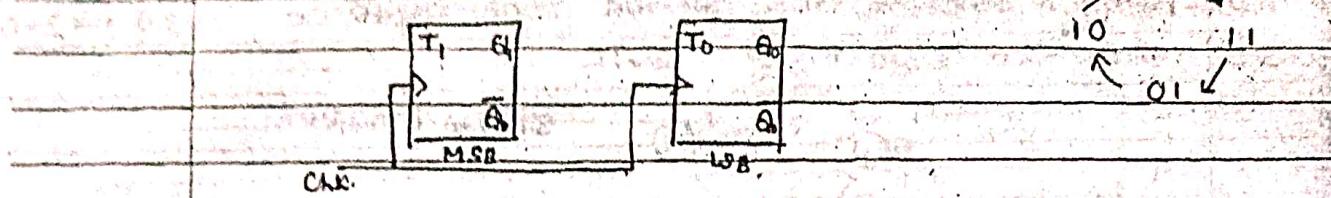
$$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0 = \bar{Q}_1 (Q_0 + \bar{Q}_0) = \bar{Q}_1$$

$$D_0 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0 = Q_1 \oplus Q_0 = Q_1 \otimes Q_0$$

(iv) Implementation :-



Soln. (v)



(vi) State table:

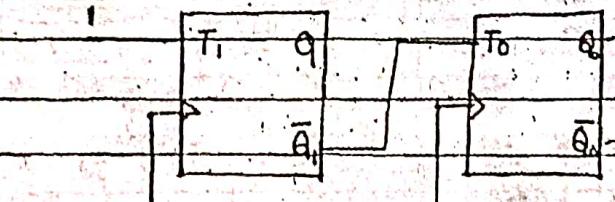
$Q_1, Q_0$	$Q_{1+}, Q_{0+}$	$T_1$	$T_0$
0 0	1 1	1	1
1 1	0 1	1	0
0 1	1 0	1	1
1 0	0 0	1	0

(vii) Logical expression:

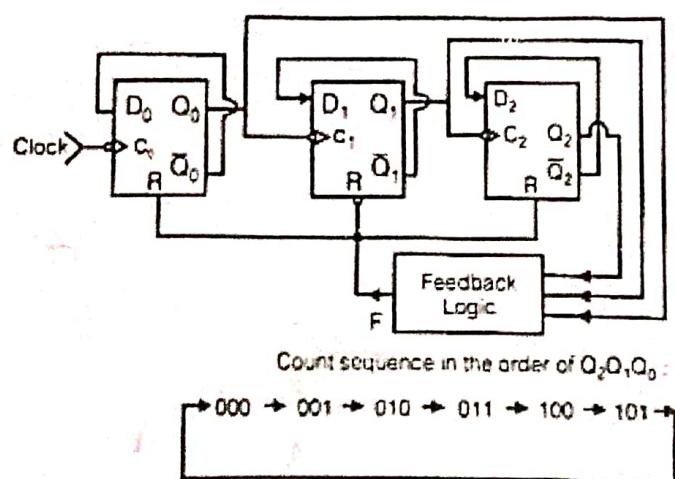
$$T_1 = 1$$

$$T_0 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0 + \bar{Q}_1$$

(viii) Implementation:-



1. A ripple counter using negative edge triggered D flip-flops is shown below. The flip-flops are cleared to '0' at the R input. The feedback logic is to be designed to obtain the count sequence shown in the same figure. The correct feedback logic is :



- (a)  $F = \overline{Q_2} Q_1 \overline{Q_0}$       (b)  $F = Q_2 \overline{Q}_1 \overline{Q}_0$   
 (c)  $F = \overline{Q}_2 \overline{Q}_1 Q_0$       (d)  $F = \overline{Q}_2 \overline{Q}_1 \overline{Q}_0$

(16)

2. The digital block in the figure, realized using two positive edge triggered D flip-flops. Assume that for  $t < t_0$ ,  $Q_1 = Q_2 = 0$ . The circuit in the digital block is given by

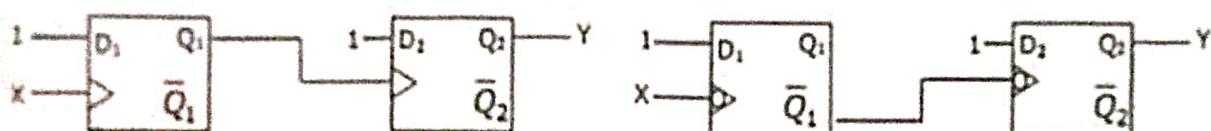
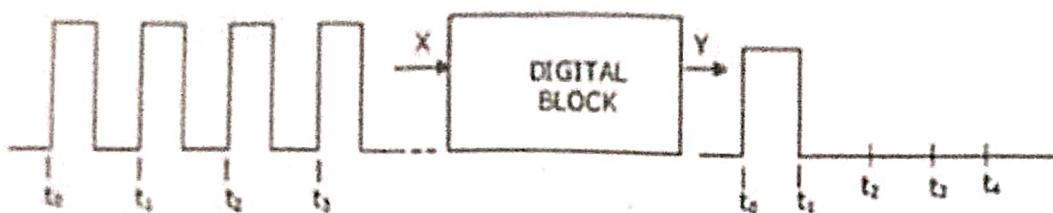


Figure (a)

Figure (b)

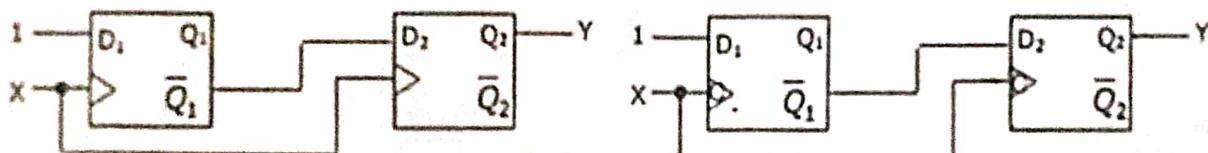


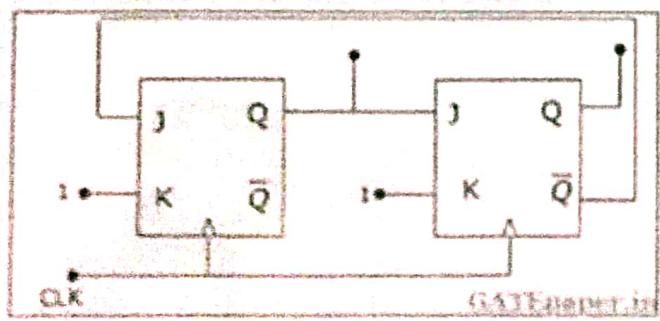
Figure (c)

Figure (d)

GATEpaper.in

Answer: C

1. The figure is shows a mod - K counter, here K is equal to



- a. 1
- b. 2
- c. 3
- d. 4

Answer: C