Indian Institute of Information Technology Vadodara

CS/IT 429

Signal Strength

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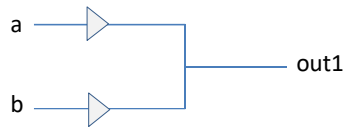
Introduction

What is
Signal Strength…?

Introduction



For the Block and Verilog HDL, assess it output…

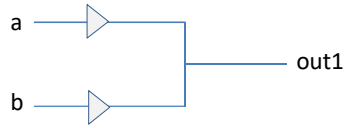
```
module logic (out1, a, b);

input a, b;
output out1;

buf b1(out1, a);
buf b2(out1, b);

endmodule
```


Introduction

Signal Strength

Strength	Mnemonics (%u)	Drive/Capacitive	Strength Value
Supply	Su	Drive	7
Strong	St	Drive	6
Pull	Pu	Drive	5
Large	La	Capacitive	4
Weak	We	Drive	3
Medium	Me	Capacitive	2
Small	Sm	Capacitive	1
High Impedance	Hiz	Drive	0

Introduction




```
module logic (out1, a, b);

input a, b;
output out1;

buf (weak1, weak0)     b1(out1, a);
buf (strong1, strong0)  b2(out1, b);

endmodule
```

⇨ Identify the output values…!

I am available/approachable at

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