Indian Institute of Information Technology Vadodara

CS/IT 429

Constructs and Convention

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Constructs and Convention

- Comments
- Identifier
- Keywords
- Whitespace
- Number System
- Operator
- Strings

Comments

Short/Single-line Comment
//

Long Comment
/*
……
…..

*/

Examples (Identify the correct ones)

// This is a comment line

/* Do this is a valid commenting …? */ Yes or No */

Identifiers

Identifiers are the names given to the objects so that they can be referred in the design

- First Character can be alphabet or underscore (_).
- Subsequent Characters can be albhanumeric (A, a , 1, 2,…) or underscore (_) or dollar ($).
- May be 1024 characters long.

Examples (Identify the correct ones)

Name aa

$name, 1_name, @name

A+B

module, logic, and, or, ….

Logic1, syst, A123, abc_, xyz$2

Concept of Escape Characters (\)

\A+B

\$name, \1_name, \@name

Keywords

Keywords are the terms whose functionality is already defined/known to the simulator

Examples

module, endmodule, initial, always, primitive, input, output, etc.

Whitespace

Whitespace characters are used to improve the readability

Examples

Blank space (\b)

Tab space (\t)

New line (\b), etc…

Number System

What is Number System…?

Number System

Verilog supports following radix system

- Binary
- Octal
- Decimal
- Hexadecimal

Can you represent 'Ten' in different radix system

- Binary - $(1010)_2$
- Octal - $(12)_O$ or $(12)_8$
- Decimal - $(10)_D$ or $(10)_{10}$
- Hexadecimal - $(A)_H$ or $(A)_{16}$

0 to 15 in different radix systems

Decimal	Binary	Octal	Hexadecimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

Binary to Decimal

6'b110111

2^5	2^4	2^3	2^2	2^1	2^0
1	1	0	1	1	1

$(1x2^5) + (1x2^4) + (0x2^3) + (1x2^2) + (1x2^1) + (1x2^0)$

$= 55_{10}$

Hexadecimal to Decimal and Binary

16'HA5E9

16^3	16^2	16^1	16^0
A	5	E	9

$(10x16^3) + (5x16^2) + (14x16^1) + (9x16^0)$

$= 42473_{10}$

Decimal: 42473

A	5	E	9
1010	0101	1110	1001

Binary: 1010 0101 1110 1001

Octal to Decimal and Binary

9'O730

8^2	8^1	8^0
7	3	0

$(7x8^2) + (3x8^1) + (0x8^0)$

$= 472_{10}$

Decimal: 472

7	3	0
111	011	000

Binary: 111 011 000

Number System

Syntax

Number of bits ` radix value

Examples

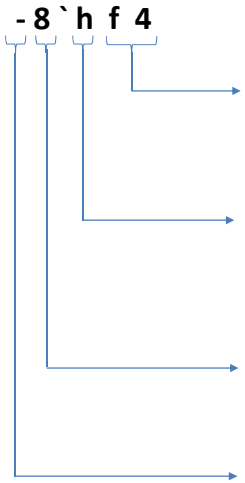
8`b10101111

8_`b_1010_1111

16`habcd

Number System

Example



Represents value of number
For Binary, 0, 1, x, z can be used
For Octal, 0 to 7, x, z can be used
For Decimal, 0 to 9, x, z can be used
For Hexadecimal, 0 to 9, a/A to f/F, x, z can be used
? can be used in place of z

Represents base of the number
For Binary, b/B is used
For Octal, o/O is used
For Decimal, d/D is used (Default)
For Hexadecimal, h/H is used

Represents bit width of the number
If absent, the width is defined as default value of the compiler

Represents Sign of the number (optional)
For a no. with neg. sign, its 2's comp form binary is represented
If sign bit is absent, number is taken as positive

Number System

Example

-4 ` d 2

Represent the number in decimal and binary format

Decimal: -2

Binary: Its 2's Complement is considered
+2 → 0010
1's Comp → 1101
2's Comp → 1110 → (-2)

Number System

Different ways of Number Representation in Verilog

1) 33
`d33

⇨ Identify the Binary Number.....!

2) 9`d439
9`D439
9`D4_39

3) 9`b110111x01
9`b1_101_1x01
9`B110111x01

Number System

Different ways of Number Representation in Verilog

4) 9`o123
   9`O123
   9`o1x3
   9`O12z

⇨ Identify the Binary Number…..!

5) `O123

6) 8`ha5
   8`HA5
   8`hA5
   8`ha_5

⇨ Identify the Binary Number…..!

7) 9`hza
   9`h?A

⇨ Identify the Binary Number…..!

Number System

Example

```
module logic1 (out1,out2,out3,
               out4,out5,out6,
               out7,out8,out9);

output [8:0]  out1,out2,out3,
              out4,out5,out6,
              out7,out8,out9;

assign out1 = 8'hx1;
assign out2 = 9'hx1;
assign out3 = 10'hx1;

assign out4 = 8'hz1;
assign out5 = 9'hz1;
assign out6 = 10'hz1;

assign out7 = 8'hF1;
assign out8 = 9'hF1;
assign out9 = 10'F1;

endmodule
```

⇨ Identify the output values…!

Number System

Example

```
module logic2 (a, b, c, d, e, f, g, h, i, j, k);

output [7:0] a, b, c, d, e, f, g, h, i, j, k;

assign   a = 7'b1011011,
         b = 8'b11011011,
         c = 9'b111011011;

assign   d = 7'hx1,
         e = 8'hx1,
         f = 9'hx1;

assign   g = 7'dx3,
         h = 8'dx3,
         i = 9'dx3;

endmodule
```

⇨ Identify the output values…!

Operators

Verilog supports different Operators as:

- Arithmetic
- Bitwise
- Logical
- Reduction
- Relational and Equality
- Shift
- Concatenation
- Ternary

String

String can represent group of characters

Each character in the string takes upto 8 bits (1 byte)

Examples

```
reg [8 * 18:1]    string_value;
initial
string_value = “Hello Verilog World” ;
```

```
integer    count;
initial      count = 1’b0
always@(posedge clk)
    while  (count < 10)
    begin
    #1 $display(“count = %d”, count);
    count = count+1;
    end
```


I am available/approachable at

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