Indian Institute of Information Technology Vadodara

Mid-Semester-Examination-Autumn-2024-25

Specialization: B. Tech. (IT & CSE)

Course Code: EC-201 (Digital Logic Design)

Time: 2.0 Hours **MM: 60**

Read the instructions carefully.

- Attempt ALL the questions.
- Make point wise answers for the required part.

Question 1: (2+2+2+2+2=10 Points)

State whether the following statements are TRUE [T] or FALSE [F] and write a few lines to justify your answer.

(a) Moore's Law related to the speed of electrons in a VLSI chip?

(b) $F(w, x, y, z) = \Sigma m (0, 1, 2, 3, 7, 8, 10) + \Sigma d ((5, 6, 11, 15)$ is POS form?

(c) The minimum number of 2-input NAND gates required to implement a Full Adder are 10.

(d) Flip flop is edge sensitive and latch is level sensitive.

(e) Lower execution time of any logic circuit can be achieved by using the minimized logical expression.

Question 2: (2+2+2+2+2=10 Points)

(a) Prove that $A \oplus B \oplus AB = A+B$

(b) Convert binary code 1001 into gray code.

(c) Find the 1's and 2's complement of the binary number 111101.

(d) What will be the BCD sum of $A= (184)_{10}$ and $B= (576)_{10}$?

(e) Perform a binary subtraction of A= 10011 and B= 11101.

Question 3: (2+2+2+2+2=10 Points)

(a) F(A,B,C)=ABC+A'B'C+ABC',find the minimum numbers of NAND gates required to implement the function.

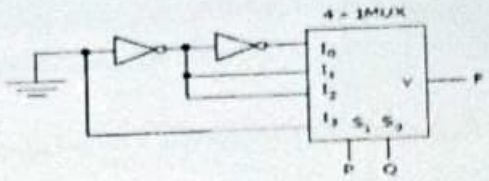
(b)Simplify the function F (A, B, C) = A'B + AC + BC redundant theorem.

(c) Implement the half subtractor circuit by using the minimum number of NAND gates.

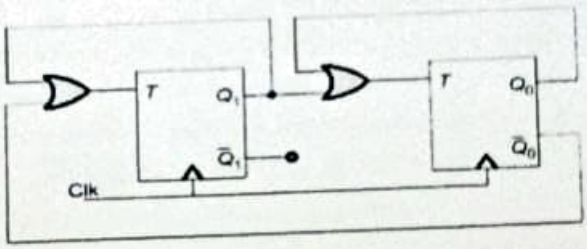
(d) Minimize the function $F (A, B, C) = \sum m (0,1,6,7) + \sum d (3,4,5)$ using K-map.

(e) Minimize the function F (A, B, C, D) =A'+AB'+ABC' using K-map.

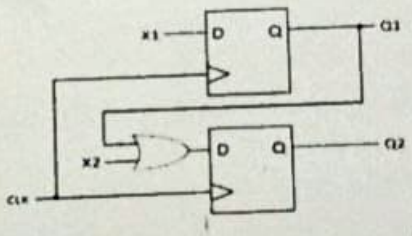
Q. 4 (a) The logic function implemented by the circuit below is (ground implies logic 0)? Give the optimized solution. 5



(a) The sequence of states (Q_1, Q_0) of the given is? Give a step by step solution for the circuit. 5



Q. 5 (a) Analyze the circuit containing D flip-flops shown below by giving the value for Q1 and Q2 that result from each clock trigger. The flip-flops are positive-edge triggered so the question will ask about the values at the negative edges, by which time the flip-flop outputs should have settled. At time t=0, Q1=0 and Q2=0. Note that the flip-flops are commonly-clocked. 5



(b) A 4-bit priority encoder has inputs D3, D2, D1 and D0 in descending order of priority. The two-bit output AB is generated as 00, 01, 10, and 11 corresponding to inputs D3, D2, D1 and D0, respectively. The Boolean expression of the output bit B is..... 5

Q. 6 (a) Define race around condition. How to remove race around conditions?. 5

(b) Design a 3-bit asynchronous up-counter. Draw the output diagram/Timing Diagram. 5

(c) Convert S-R flip-flop to J-K flip-flop and draw the state diagram of S-R flip-flop and J-K flip-flop. 5

(d) Define Ring counter and Johnson counter and find usable states and no unusable states. 5

(e) Implement half adder using 2x4 Decoder.

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