Started on	Saturday, 5 November 2022, 11:00 AM
State	Finished
Completed on	Saturday, 5 November 2022, 11:08 AM
Time taken	7 mins 58 secs
Marks	4.00/5.00
Grade	**8.00** out of 10.00 (**80**%)

Question **1**

Complete

Mark 1.00 out of 1.00

The bit sequence 10011100 is serially entered (right-most bit first) into an 8-bit parallel out shift register that is initially clear. What are the Q outputs after four clock pulses?

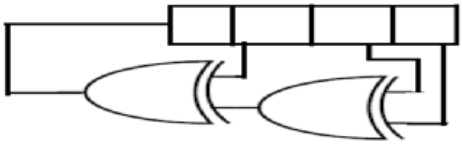
- a. 11110000
- b. 11000000
- c. 10011100
- d. 00001100

Question **2**

Complete

Mark 0.00 out of 1.00

The circuit shown in figure below, 4-bit SIPO register which is initially loaded with 1011. If clock pulse applied continuously after how



many clock pulses again the data becomes 0111?

- a. After 6 CLK
- b. After 9 CLK
- c. After 11 CLK
- d. After 5 CLK

Question **3**

Complete

Mark 1.00 out of 1.00

With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____

- a. 4 µs
- b. 44 µs
- c. 40 µs
- d. 8 µs

Question **4**

Complete

Mark 1.00 out of 1.00

What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?

- a. SISO
- b. SIPO
- c. DIPO
- d. **PIPO**

Question **5**

Complete

Mark 1.00 out of 1.00

The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____

- a. 00101
- b. 01110
- c. 00001
- d. 00110

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