Ques-1 **Consider a Boolean gate (D) where the output Y is related to the inputs A and b as, Y =A +$\bar{B}$, where + denotes logical OR operation. The Boolean inputs '0' and '1' are also available separately. Using instances of only D gates and inputs '0' and '1', _____ (select the correct options).**

a. NAND logic can be implemented

b. OR logic cannot be implemented

c. NOR logic can be implemented

d. AND logic cannot be implemented

Correct option is (a, c).

Explanation.

F(A, B) = A +$\bar{B}$

As 0 and 1 are available.

F(0, B) = A +$\bar{B}$ = 0 +$\bar{B}$

= $\bar{B}$ (NOT)

F(A +$\bar{B}$) = A + $\bar{\bar{B}}$ = A + B

F(A + $\bar{B}$= A + B (OR)

With the combination of OR and NOT, NOR gate can be implemented.

Since NOR gate is universal logic gate, so all the functions can be implemented.

So**, correct option is (a, c).**

Ques-2 The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

a. 4

b. 5

c. 6

d. 7

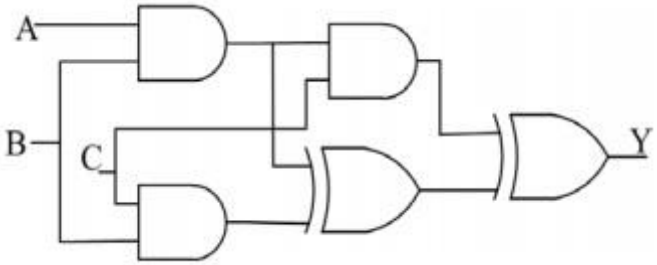
Correct option is (a)

Important-

Logic Gates	Min. number of NOR Gate	Min. number of NAND Gate
NOT	1	1
AND	3	2
OR	2	3
EX-OR	5	4
EXNOR	4	5
NAND	4	1
NOR	1	4
Half-Adder	5	5
Half-Subtractor	5	5
Full-Adder	9	9
Full-Subtractor	9	9

Ques-3

The output of the combinational circuit given below is:



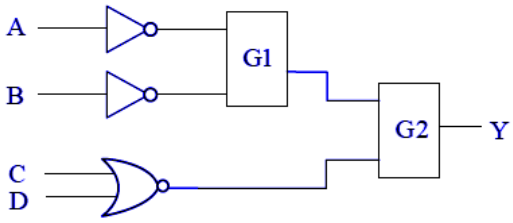
a. A+B+C
b. A(B+C)
c. B(C+A)
d. C(A+B)

Correct option is (c)

Explanation.

$$Y = ABC \oplus AB \oplus BC = AB\,(C \oplus 1) \oplus BC$$
$$= AB\,\overline{C} \oplus BC = B\,(A\,\overline{C} \oplus C) = B[\,\overline{A\overline{C}}\,C + A\,\overline{C}\,.\,\overline{C}\,]$$
$$= B[(\overline{A} + C)\,C + A\,\overline{C}\,] = B\,[\,\overline{A}\,C + C + A\,\overline{C}\,]$$
$$= B\,[C + A\,\overline{C}\,] = B\,[C + A] \rightarrow Y = B\,(A + C)$$

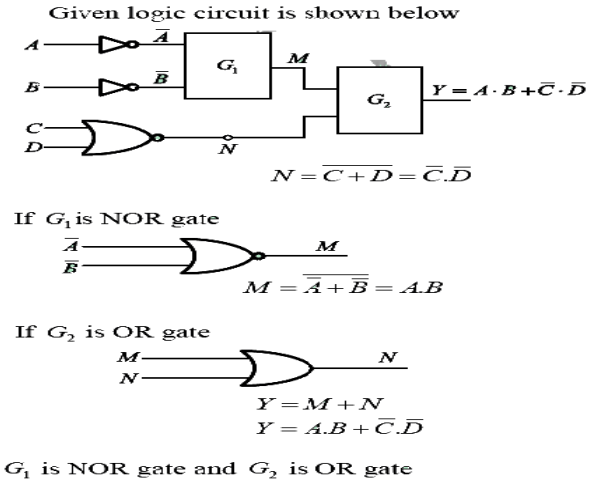
Ques-4 In the figure shown, the output is required to be Y=AB+ $\bar{C}\bar{D}$. The gates G1 and G2 must be, respectively,



a. NOR, OR
b. OR, NAND
c. NAND, OR
d. AND, NAND

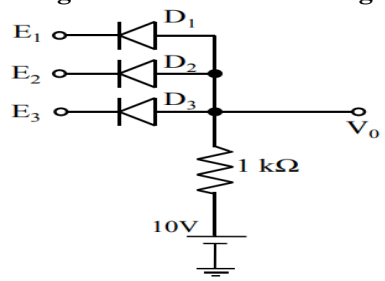
Correct option is (a)

Solutions



Ques-5

In the circuit shown, diodes D1 ,D2 and D3 are ideal, and the inputs E1 , E2 and E3 are "0 V" for logic '0' and "10 V" for logic '1'. What logic gate does the circuit represent?



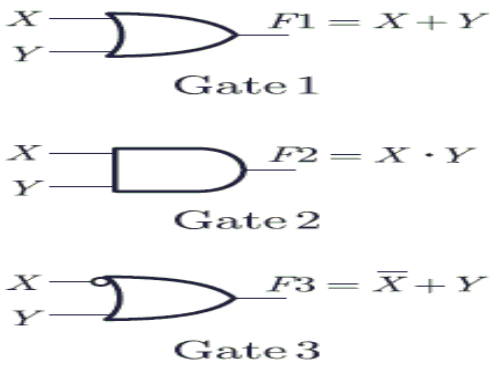
a. 3-input OR gate
b. 3-input NOR gate
c. 3-input AND gate
d. 3-input XOR gate

Correct option is (c)

Explanation. If any of the inputs from E1, E2, E3 is logic 0 (means OV) then the corresponding diode will be "ON" resulting in OV at the output and only when all the inputs are logic 1 (means V_{DD}) then Vo (output voltage) will be high, hence, resulting into 3 input AND-gate. Truth table for the logic circuit is shown below. E1 E2 E3 V_O.

E1	E2	E3	Vo
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Ques-6 A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. The three gates are as follows:



Which of the following statements is TRUE?

a. Gate 1 is a universal gate.

b. Gate 2 is a universal gate.

c. Gate 3 is a universal gate.

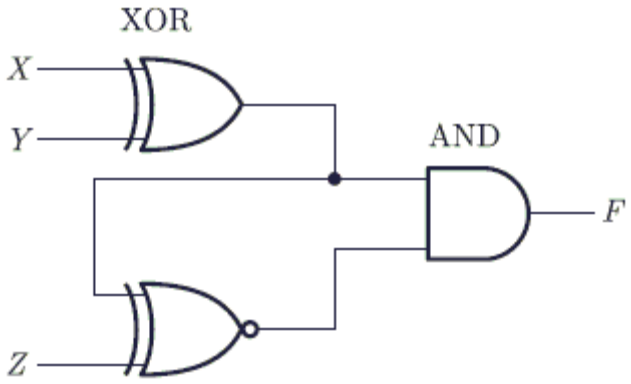
d. None of the gates shown is a universal gate.

Correct Option: C

Explanation. In general, the only universal gates are NAND and NOR gates, but none of the given gates is NAND or NOR gate. However, we must observe gate 3. All the Boolean functions can be implemented by using this gate. Hence, it is a universal gate.

Ques-7

The output F in the digital logic circuit shown in the figure is

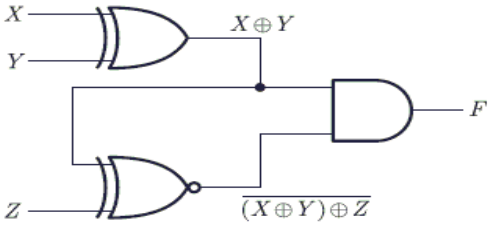


1. F = $\overline{X}$YZ + X$\overline{Y}$Z
2. F = $\overline{X}$Y$\overline{Z}$+ X$\overline{YZ}$
3. F = $\overline{XY}$Z + XYZ
4. F = $\overline{XYZ}$ + XYZ

Correct Option: A

Explanation:

We have the digital logic circuit as

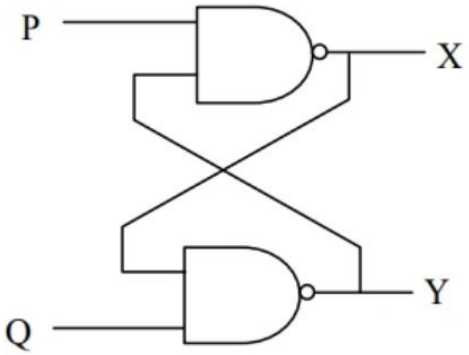


In the logic circuit, the two inputs to the output AND gate are $X \oplus Y$ and $\overline{(X \oplus Y) \oplus Z}$

So, we have the output

$$F = (X \oplus Y)[\overline{(X \oplus Y) \oplus Z}]$$
$$= (X \oplus Y)[\overline{X \oplus Y}\ \overline{Z} + (X \oplus Y)Z]$$

Ques-8 In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is : P = Q = "0". If the input condition is changed simultaneously to P = Q = "1", the outputs X and Y are



a. X = '1', Y ='1'
b. Either X = '1', Y = '0' or X ='0', Y = '1'
c. Either X = '1', Y = '1' or X ='0', Y = '0'
d. X = '0', Y ='0'

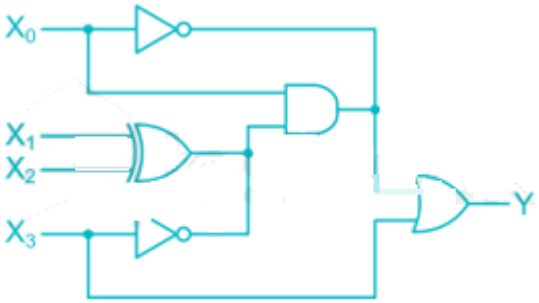
Correct Option: b

Explanation:

When p = 0, Q = 0 ⇒ x = 1, y = 1
When p = 1, Q= 1 ⇒ x = 1, y = 0
(Or)

When p = 1, Q = 1 ⇒ x = 0, y = 1
Hence, the correct option is (b)

Ques 9: The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose



outputs are shorted are HIGH.

The number of distinct values of $X_3X_2X_1X_0$ (out of the 16 possible values) that give $Y = 1$ is

a. 1
b. between **16** and **16**
c. between **8** and **8**
d. between **16** and **8**

Correct Option: c
Explanation:

From figure, M = $(X1 \oplus X2)\overline{X_3}$

N = $(A.X)\ )\overline{X_0}$

= 0 [as $X.\overline{X_0} = 0$]

Y = $(N + X_3) = X_3$

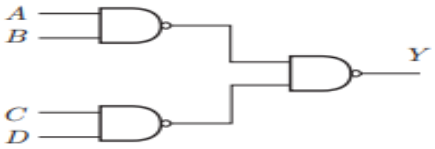
The number of distinct values possible with $X_3X_2X_1X_0 = 16$. And out of 16 **combinations 8 such combination** present when $X_3 = 1$ and gives output Y = 1.

Ques 10: The Boolean function Y = AB + CD is to be realized using only two-input NAND gates. The mini mum number of gates required is

(a) 2 (b) 3 (c) 4 (d) 5

Correct Option: b
Explanation:

Solution. $A \cdot B + C \cdot D = \overline{[(\overline{A \cdot B}) \cdot (\overline{C \cdot D})]}$.
The following figure shows the NAND implementation and it requires three NAND gates.

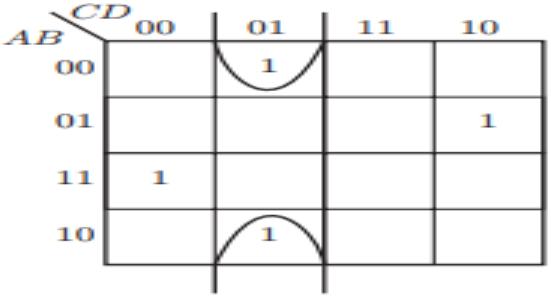


Ques 11:

The Boolean expression $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D}$ can be minimized to

(a) $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C} + A\bar{C}D$
(b) $Y = \bar{A}\bar{B}\bar{C}D + BC\bar{D} + A\bar{B}\bar{C}D$
(c) $Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + A\bar{B}\bar{C}D$
(d) $Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + AB\bar{C}\bar{D}$

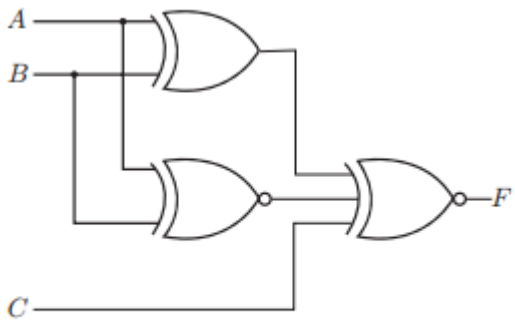
Solution. The K-map corresponding to given Boolean expression is shown in the following figure:



The simplified expression from the K-map is given by

$$Y = \bar{A}BC\bar{D} + AB\bar{C}\bar{D} + \bar{B}\bar{C}D$$

Ques 12: For the output F to be 1 in the logic circuit shown in the following figure, the input combination should be



(a) $A = 1, B = 1, C = 0$ (b) $A = 1, B = 0, C = 0$
(c) $A = 0, B = 1, C = 0$ (d) $A = 0, B = 0, C = 1$

Correct Option: d
Explanation:

For F = 1, even number of inputs to the EX-NOR gate at the output should be in logic `1' state. In the given logic circuit, other than C input, the other two inputs cannot be simultaneously in logic

`1' state. Only one of them can be `1' at a time. Therefore, C must be in logic `1' state and hence the answer.

Ques 13: Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
a) Two 2 input AND gates
b) Two 3 input AND gates
c) Two 2 input OR gates
d) Two 3 input OR gates

Correct Option: a
Explanation:

Two 2 input AND gates are placed with a NOR – based S – R latch to convert it to an S – R flip – flop. One AND gate is given R in one input and clock in the other. Similarly the second AND gate is given S in one input and clock in the other.

Ques 14:

When does a negative level triggered flip-flop in Digital Electronics changes its state?
a) When the clock is negative
b) When the clock is positive
c) When the inputs are all zero
d) When the inputs are all one

Answer: **a**
Explanation:

A negative level triggered flip – flop has a NOT gate present between clock input and the input of AND gate. Thus, the negative level triggered flip – flop change its state when the clock is negative.

Ques 15: How many AND, OR and EXOR gates are required for the configuration of full adder?
a) 1, 2, 2
b) 2, 1, 2
c) 3, 1, 2
d) 4, 0, 1

Correct Option: b
Explanation: There are 2 AND, 1 OR and 2 EXOR gates required for the configuration of full adder, provided using half adder. Otherwise, configuration of full adder would require 3 AND, 2 OR and 2 EXOR.

Ques 16:

Let A and B is the input of a subtractor then the output will be
a) A XOR B
b) A AND B
c) A OR B
d) A EXNOR B

Correct Option: **a**
Explanation:

The subtractor has two outputs BORROW and DIFFERENCE. Since the difference output of a subtractor is given by AB' + BA' and this is the output of a XOR gate. So, the final difference output is AB' + BA'.

Ques 17: Let A and B is the input of a subtractor then the borrow will be _____
a) A AND B'
b) A' AND B
c) A OR B
d) A AND B

Correct Option: **b**
Explanation
The borrow of a subtractor is received through AND gate whose one input is inverted. On that basis the borrow will be (A' AND B).

Ques 18:

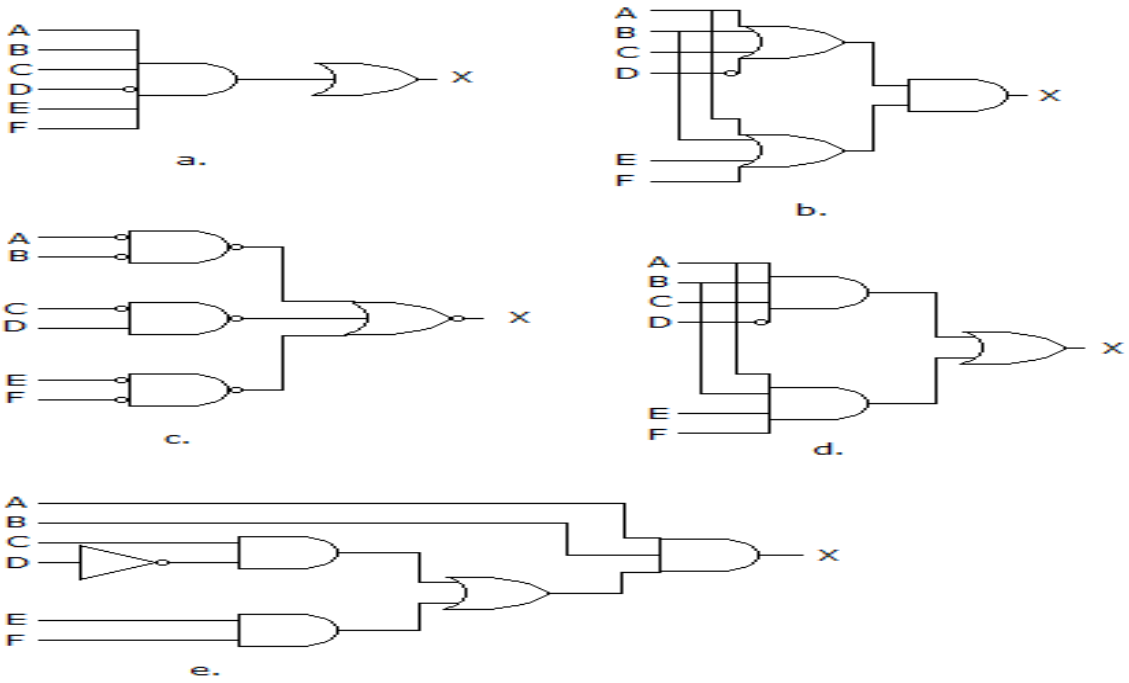
The design of an ALU is based on
a) Sequential logic
b) Combinational logic
c) Multiplexing
d) De-Multiplexing

Correct Option: **b**
Explanation
The design of an ALU is based on combinational logic. Because the unit has a regular pattern, it can be broken into identical stages connected in cascade through carries.

Ques 19: Why XOR gate is called an inverter?
a) Because of the same input
b) Because of the same output
c) It behaves like a NOT gate
d) It behaves like a AND gate

Correct Option: **c**
ExplanationThe XOR (Exclusive Or) gate has a true output when the two inputs are different. When one input is true, the output is the inversion of the other. When one input is false, the output is the non-inversion of the other.

Ques 20: Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



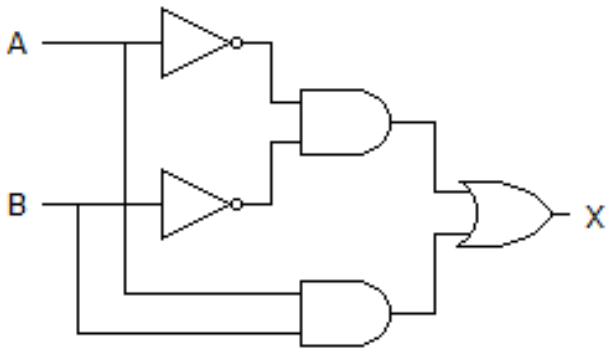
a. a
b. b
c. c
d. d

Correct Option: d

Explanation

SOP means Sum Of Products form which represents the sum of product terms having variables in complemented as well as in uncomplemented form. Here, the diagram of d contains the OR gate followed by the AND gates, so it is in SOP form.

Ques 21. Which of the following logic expressions represents the logic diagram shown?

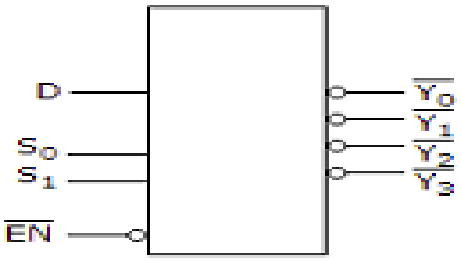


a. X=AB'+A'B
b. X=(AB)'+AB
c. X=(AB)'+A'B'
d. X=A'B'+AB

Correct Option: d

Explanation
1st output of AND gate is = A'B'
2nd AND gate's output is = AB and,
OR gate's output is = (A'B')+(AB) = AB + A'B'.

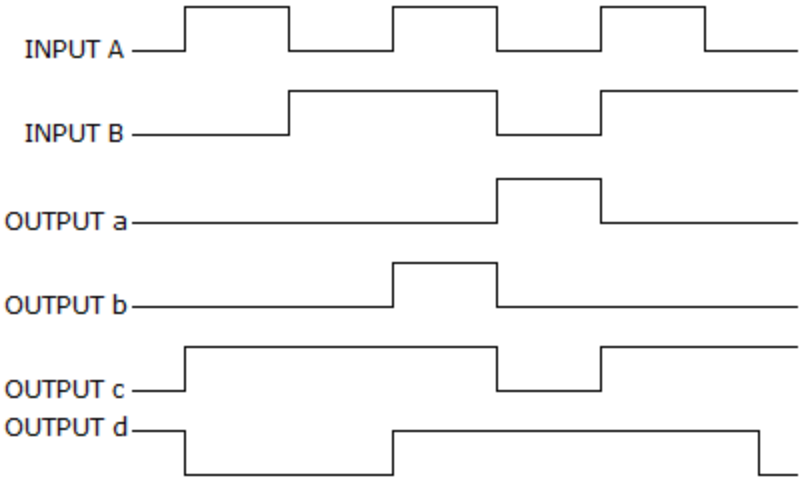
Ques 22: The device shown here is most likely a



a) Comparator
b) Multiplexer
c) Inverter
d) Demultiplexer

Correct Option: d
Explanation
The given diagram is demultiplexer, because it takes single input & gives many outputs. A demultiplexer is a combinational circuit that takes a single output and latches it to multiple outputs depending on the select lines.

Ques 23: For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?



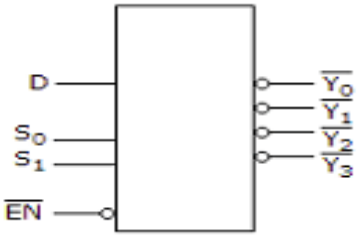
a) d
b) a
c) c
d) b

Correct Option: a

Explanation

Explanation: When both inputs are same then the o/p is high for a XNOR gate.
i.e., A B O/P
0 0 1
0 1 0
1 0 0
1 1 1.
Thus, it will produce 1 when inputs are even number of 1s or all 0s, and produce 0 when input is odd number of 1s.

Ques 25 : For the device shown here, assume the D input is LOW, both S inputs are LOW and the input is LOW. What is the status of the Y' outputs?



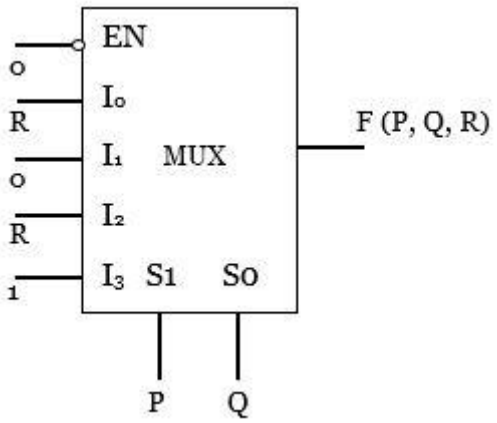
a) All are HIGH
b) All are LOW
c) All but Y0 are LOW
d) All but Y0 are HIGH

Correct Option: a

Explanation

In the given diagram, S0 and S1 are selection bits. So,
I/P S0 S1 O/P
D = 0 0 0 Y0
D = 0 0 1 Y1
D = 0 1 0 Y2
D = 0 1 1 Y3
Hence, inputs are S0 and S1 are Low means 0, so output is Y0 and rest all are HIGH.

Ques 26: The figure below shows a multiplexer where S1 and S2 are the select lines, I0 to I3 are input data lines, EN is enabled line and F (P, Q, R) is the output. So F is



a. PQ + Q'R
b. P + QR'
c. PQ'R + P'Q
d. Q' + PR

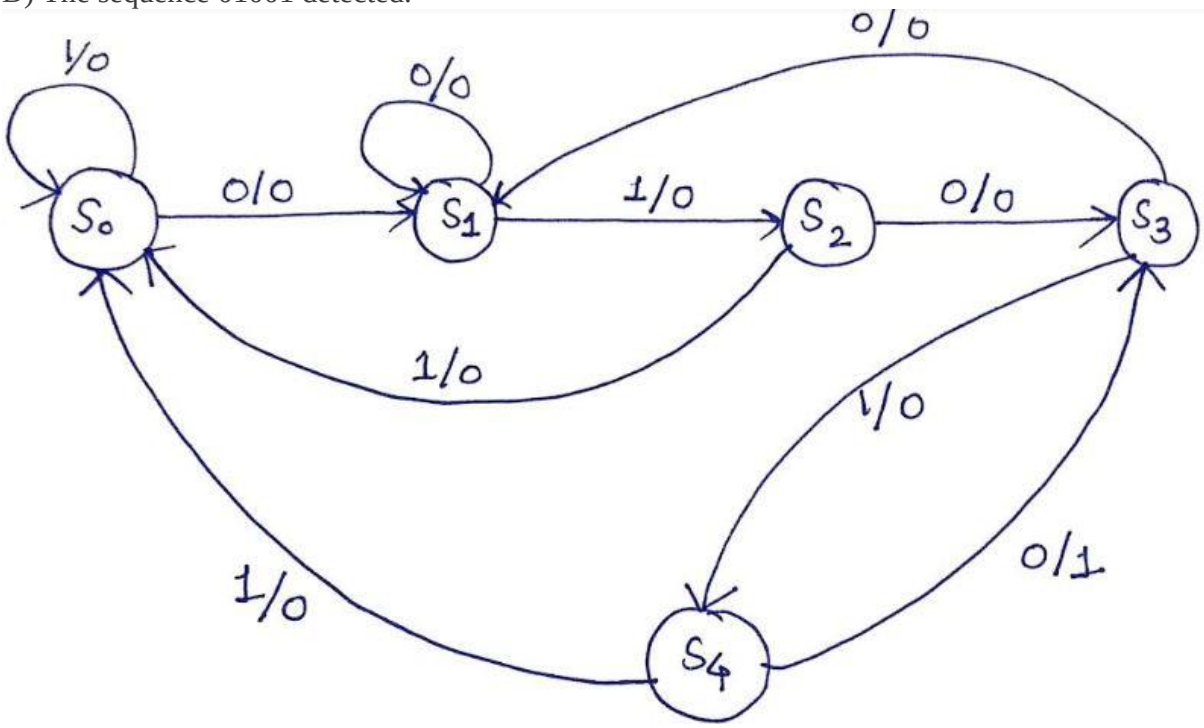
Correct Option: a

Explanation

Mux is combinational circuits. here EN is EN' and the value of **EN' = 0, And EN = 1**, so this mux is in working condition.

The output equation for 4:1 mux is if enable is present:
F = EN'. (S1'S0'I0 + S1'S0I1 + S1S0'I2 + S1S0I3)
F = 1 (P'Q'R + P'Q.0 + PQ'R + PQ.1)
F = P'Q'R + PQ'R + PQ
F = Q'R (P' + 1) + PQ
F = Q'R + PQ : (P' + 1) =1

Ques27: The state diagram of the sequence detector is shown below, state S0 is the initial state of the sequence detector. If the output is 1 then
A) The sequence 01010 detected.
B) The sequence 01011 detected.
C) The sequence 01110 detected.
D) The sequence 01001 detected.



Correct Option: 01010 (option A)

Explanation

Sequence detector is a sequential circuit that is used to detect the particular sequence as soon as the output is going to be 1. It means the complete sequence is detected then only the output is going to be 1 if the sequence is not detected the output is zero.

At S0 stage: There are two possibilities, when input is 1 then it stayed on S0 (same state) only and if the input is 0 then it is going to next state S1 and still, the output is 0. **So** 0 **is detected here.**

At S1 stage: There is a two possibilities, when input is 0 then it stayed on S1 (same state) only and if the input is 1 then it is going to next state S2 and still, the output is 0. **So 1 is detected here.**

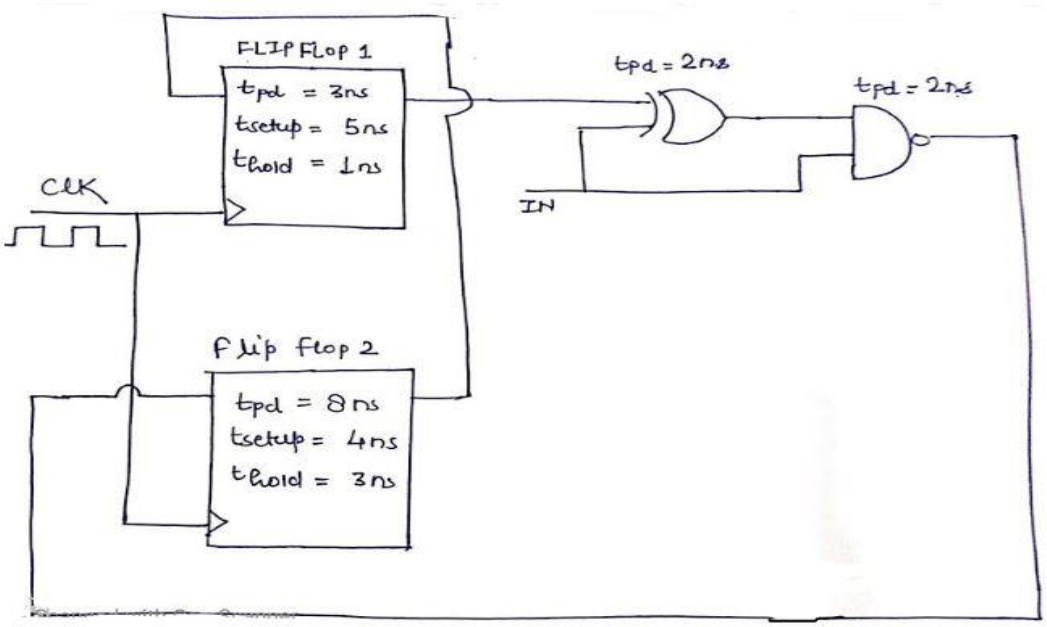
At S2 stage: There are two possibilities when input is 1 then S2 goes to the S0 state (initial state) and what we detected previously it will go, the sequence again started and if the input is 0 then it is going to next state S3 and still, the output is 0. **So 0 is detected here.**

At S3 stage: There are two possibilities when input is 0 then S3 goes to the S1 state and what we detected previously it will go the sequence again started from S1 and if the input is 1 then it is going to next state S4 and still, the output is 0. **So 1 is detected here.**

At S4 stage: There are two possibilities, when input is 1 then S4 goes to the S0 state (initial state) and what we detected previously it will go the sequence again started from S0 (initial state) and if the input is 0 then it is going to state S3 and here we got the output is 1. So 0 is detected here.

So the sequence we detect here is: **01010 (option A)**

Ques 29: For the component in the sequential circuit shown below, t_{pd} is the propagation delay t_{setup} is the setup time and t_{hold} is the hold time. The maximum clock frequency (rounded off to the nearest integer) at which the given circuit can operate reliably, is …… MHz.



Setup time :
The minimum time for which the data (D) should be stable at the input before the active edge of clock arrival, that minimum time is called setup time. If the data is not stable before that minimum time the setup violation occurs and we will not get the correct output.

Hold time:
The minimum time for which the data (D) should be stable at the input after the active edge of the clock has arrived.

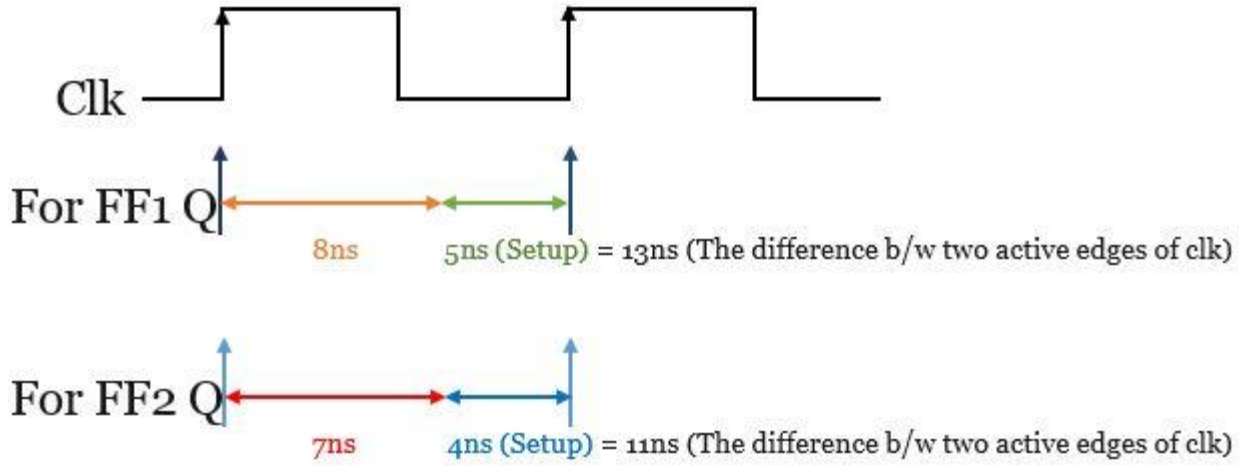
So here we have to find the time between two active edge of a clock or after how much time the next clock edge arrives and we get data reliably. Initially we assume the data we get is stable.

Here input (IN) is externally applied to the EXOR and NAND gate so it has 0 (zero) delay.

When the clock is applied to both flip flop, the FF2 gets output after 8ns (propagation delay of FF2) and this output is the input to the FF1 and the FF1 gets output after 3ns (propagation delay of FF1) and this output is the input to the EX-OR gate. The output of the XOR gate is available after 5ns (3+2). Now the output of the XOR gate is the input to the NAND gate so the output of the NAND gate available after 7ns (3+2+2). The NAND gate output is the input to the FF2 means at 7ns.

For FF1 the after the first clock edge is arriving, the data is available at 8ns and stable for 5ns time (setup time of FF1) till the next clock has arrived so the time between two active clock edge is 13ns (8+5) i.e. the data must be stable until the next clock edge arrives.

For FF2, after the first clock edge is arriving, the data is available at 7ns and stable for 4ns time (setup time of FF2) till the next clock has arrived so the time between two active clock edge is 11ns (7+4) i.e. the data must be stable until the next clock edge arrives.



So here are two times between two active edges of the clock for FF1 and FF2 is 13ns and 11ns respectively, but we will consider the maximum time i.e. 13ns because for 13ns both the flip flop will work properly and we get reliable and stable output. If we consider 11ns time between two active edges of the clock then FF2 will work properly but FF1 will not work properly and get unstable output so we consider the maximum time 13ns. so T should be greater or equal to the 13ns.

So T >= 13 ns
And f < = 1/13ns
<= 76.923 MHz
And $f_{max} = 76.923$ MHz

Answer : $f_{max} = 76.923$ MHz

Ques 30: A function F (A, B, C) defined by three Boolean variables A, B and C when expressed as sum of products is given by
F = A' B' C'+ A' B C'+ A · B'· C'
where, A', B', and C' are the complements of the respective variables. The product of sums (POS) form of the function F is
A) F = (A + B + C) · (A + B'+ C) · (A'+ B + C)
B) F = (A'+ B' + C') · (A'+ B + C') · (A + B' + C')
C) F = (A + B + C') · (A + B'+ C') · (A'+ B + C') · (A'+ B' + C) · (A'+ B' + C')
D) F = (A'+ B' + C) · (A'+ B + C) · (A + B' + C) · (A + B + C') · (A + B + C)

Correct Option: (c)

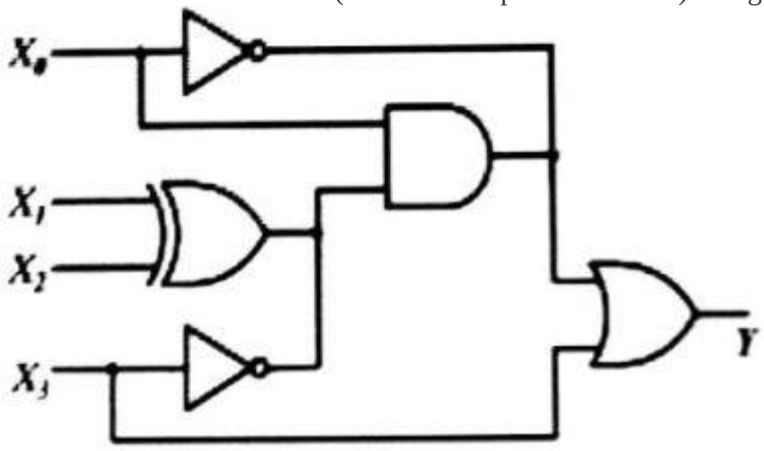
Explanation. : Given expression is SOP form i.e. min terms
F = A' B' C'+ A' B C'+ A · B'· C'
A' B' C'-> 000 = 0
A' B C' -> 010 = 2
A B' C' -> 100 = 4

We can also write SOP (min terms) as F = ∑m (0, 2, 4)
And F=∑m (0, 2, 4) = ∏M (1, 3, 5, 6, 7) (max term)
F = ∏M (1, 3, 5, 6, 7) (max term)

Convert in to POS form
1 -> 001 -> A + B + C'
3 -> 011 -> A +B' + C'
5 -> 101 -> A' + B + C'
6 -> 110 -> A' + B' + C
7 -> 111 -> A' +B' + C'
So F = (A + B + C'). (A +B' + C'). (A' + B + C'). (A' + B' + C). (A' +B' + C')
Option (C) is the correct answer.

Ques 31: The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for the LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.

The number of distinct values of X3X2X1X0 (out of the 16 possible values) that give Y = 1 is.



Sol: At the output, there is OR gate and OR gate output is 1 if any one of the inputs is 1.

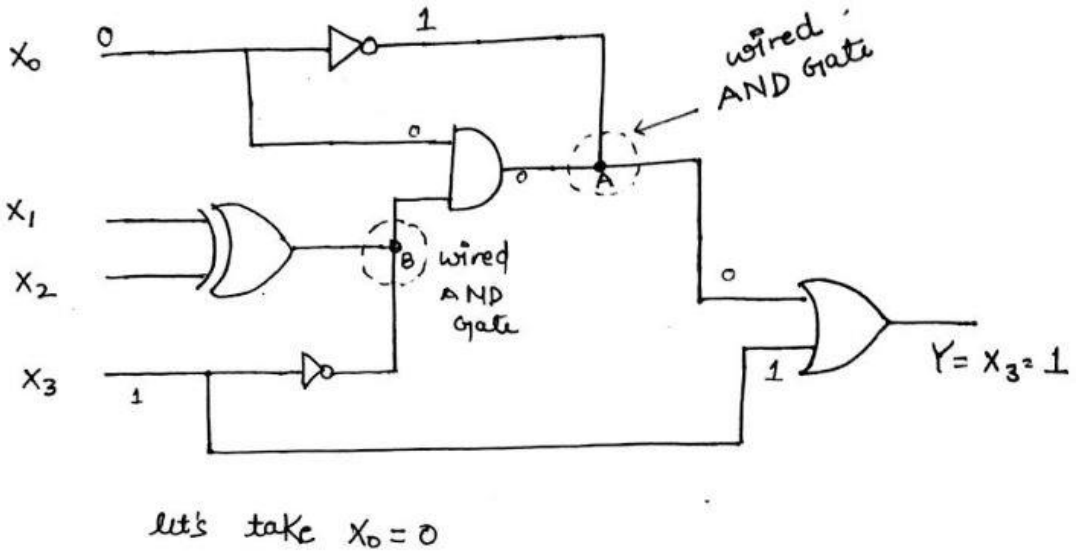
Truth table of OR gate is

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

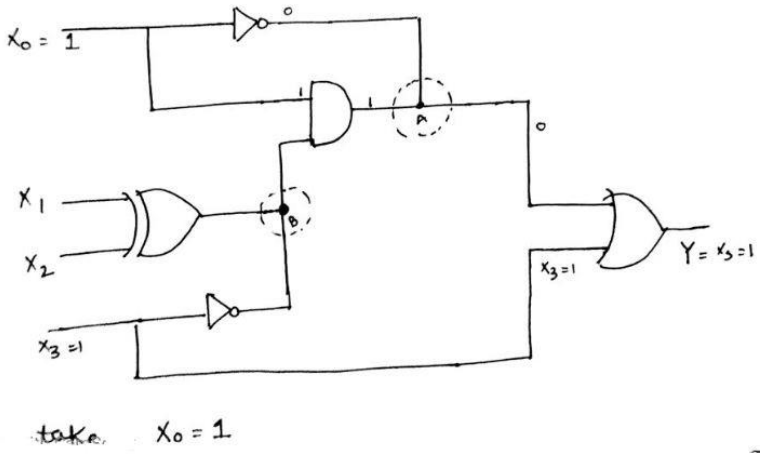
From the fig. there are 4 inputs so 16 possible states will come into the picture and out of 16 how many states give the output 1 at the OR gate.

There is two wired logic (shorted nodes) at point A and B and it acts as AND gate. So only X3 we will keep 1 always to get the OR gate output is 1. If we take X3 is zero then we will not get the OR gate output Y equal to 1.

Let's take X0 = 0 from the figure we see that OR gate has one input is 0 and other is X3 i.e. 1 so we got 1 output. X1, X2, and X3 we consider any value it does not affect the OR gate output.



Let's take X0 = 1 from the figure we see that OR gate has one input is 0 and other is X3 i.e. 1 so we got 1 output. X1, X2, and X3 we consider any value it does not affect the OR gate output.



If X3 is zero (0) then the **output will be zero** irrespective of the values of X1, X2, and X3.

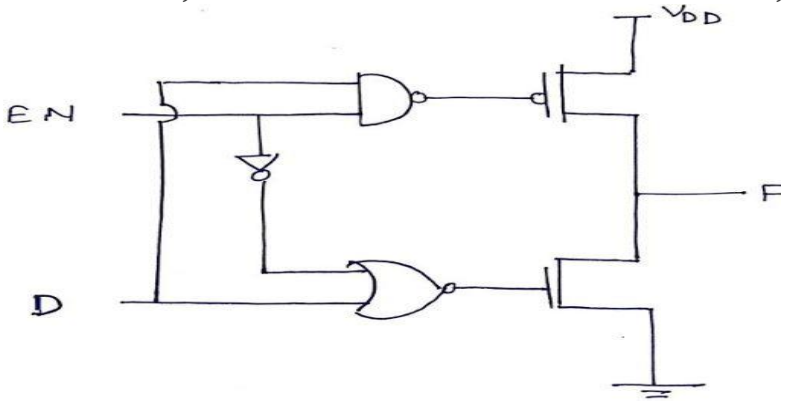
X3	X2	X1	X0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

If X3 is 1 then the **output will be 1** irrespective of the values of X1, X2, and X3.

X3	X2	X1	X0	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

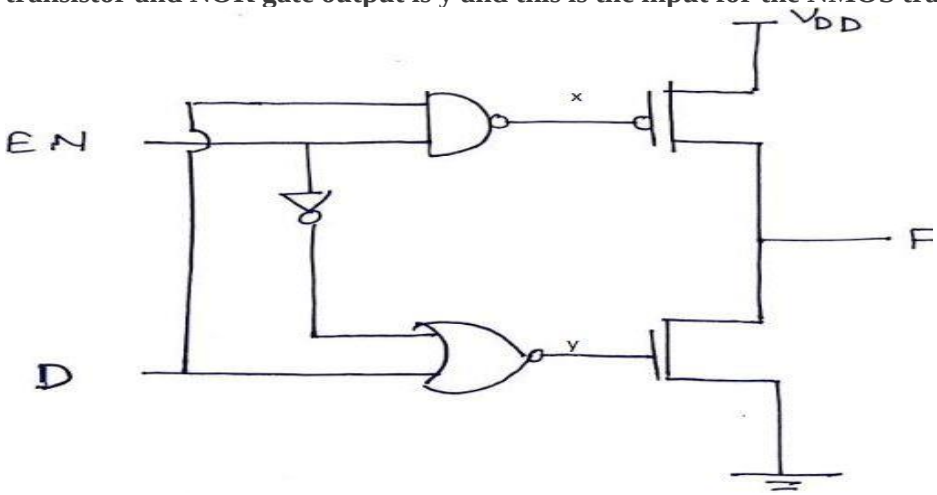
So out of 16 possible values, the number of distinct values of X3X2X1X0 that gives Y =1 is 8.

Ques 33: In the circuit shown, what are the values of F for EN = 0 and EN =1, respectively.



A) 0 and D
B) Hi-z and D

C) 0 and 1
D) Hi-z and D'
Correct Option: B
Explanation. Let's consider the NAND gate output is x and this is the input for PMOS transistor and NOR gate output is y and this is the input for the NMOS transistor.



So x = (EN.D)' and y = (EN' + D)'

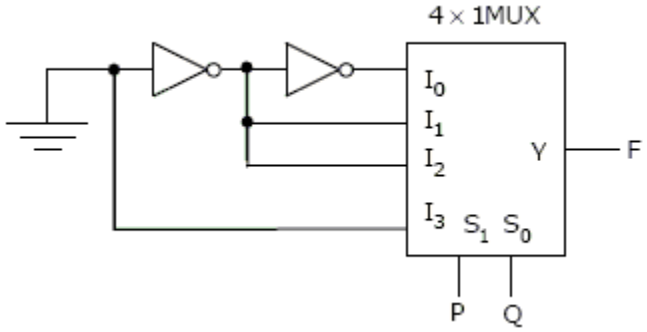
So there are two inputs EN and D then 4 combinations are present. We all know that PMOS will conduct at logic 0 and NMOS will conduct at logic 1. The truth table is

EN	D	x= (EN.D)'	y=(EN'+D)'	PMOS(x)	NMOS (y)	F (output)
0	0	1	0	OFF	OFF	Hi-z (High impedance state)
0	1	1	0	OFF	OFF	Hi-z (High impedance state)
1	0	1	1	OFF	ON	GND = 0
1	1	0	0	ON	OFF	VDD = 1

From the truth table when EN=0, both the transistors are OFF and not connected to ground and supply (VDD) so the transistor is in high impedance state.

From the truth table when EN=1, the output is equal to D value.
Option (B)

Ques 1: The logic function implemented by the circuit below is (ground implies logic 0)



a. F = AND (P,Q)
b. F = OR (P,R)
c. F = OR (P,Q)
d. F = XOR (P,Q)

Correct Option: D

Explanation:

$$F = \overline{S_1}\,\overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

$$I_0 = I_3 = 0$$

$$F = \overline{P}Q + P\overline{Q} = \mathrm{XOR}(P,\ Q)\ \ (\ S_1 = P, S_0 = Q\ )$$

Ques 2 - Two D flip-flops are connected as a synchronous counter that goes through the following Q_BQ_A sequence 00→→11→→01→→10→→00→→… The combination to the inputs D_A and D_B are

a. $D_A = Q_B$; $D_B = Q_A$
b. $D_A = \overline{Q_A}$; $D_B = \overline{Q_B}$
c. $D_A = (\overline{Q_A}Q_B + Q_A\overline{Q_B})$; $D_B = \overline{Q_A}$
d. $D_A = (\ \overline{Q_AQ_B} + Q_AQ_B)$; $D_{B=}\ \overline{Q_B}$

Option d is correct

Explanation

The sequence is Q_BQ_A

$00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \ldots$

Q_B	Q_A	$Q_B(t+1)$	$Q_A(t+1)$
0	0	1	1
1	1	0	1
0	1	1	0
1	0	0	0

$Q_B(t+1)$

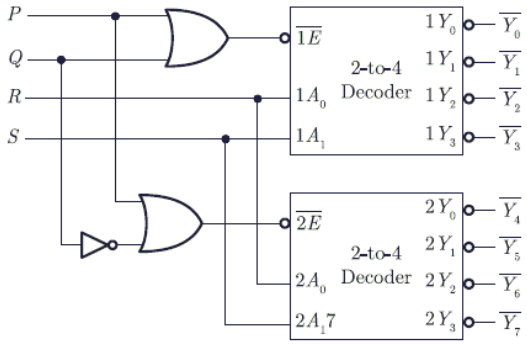
Q_A \ Q_B	0	1
0	1	1
1	0	0

$Q_B(t+1) = \overline{Q_A}$

Q_A \ Q_B		
	1	0
	0	1

$$D_A = \overline{Q_A}\,\overline{Q_B} + Q_AQ_B$$

Ques 3: A 1-to-8 demultiplexer with data input D_{in}, address inputs S_0, S_1 and S_2 (with S_0 as the LSB) and $\overline{Yo}$ to $\bar{Y}7$ as the eight demultiplexed output, is to be designed using two 2 - to - 4 decoders (with enable input $\overline{E}$ and address input A_0 and A_1). As shown in the figure, D_{in}, S_0, S_1 and S_2 are to be connected to P, Q, R and S, but not necessarily in this order. The respective input connections to P, Q, R and S terminals should be

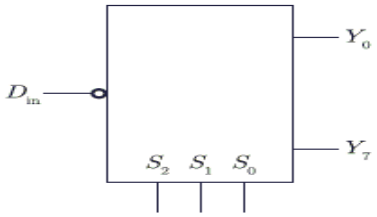


a. S_2, D_{in}, S_0 and S_1
b. S_1, D_{in}, S_0 and S_2
c. D_{in}, S_0, S_1 and S_2
d. D_{in}, S_2, S_0 and S_1

Correct Option: D

Explanation:

We need to implement 1:8 DEMUX



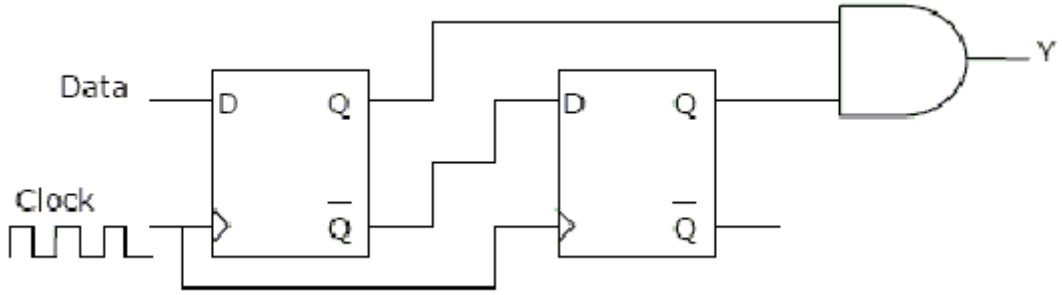
As input to both the decoder should be same. So from figure only line P is acting same to both 2×4 decoder. Hence, P is mapped with D_{in}. Again, we have

S_2	S_1	S_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Here, we observe that S_2 is '0' in 4 cases then '1' logic. From figure, it can be seen only line Q is connected to NOT gate to OR gate.So Q is mapped to S_2 and remaining two line should be mapped in same order because select lines of 1:8 DEMUX should be mapped with address line of decoder. Hence, the mapping is

$P \rightarrow D_{in}$
$R \rightarrow S_0$
$Q \rightarrow S_2$
$S \rightarrow S_1$

Ques4 -When the output Y in the circuit below is '1', it implies that data has



a. changed from 0 to 1
b. changed from 1 to 0
c. changed in either direction
d. not changed

Correct Option: A

Explanation

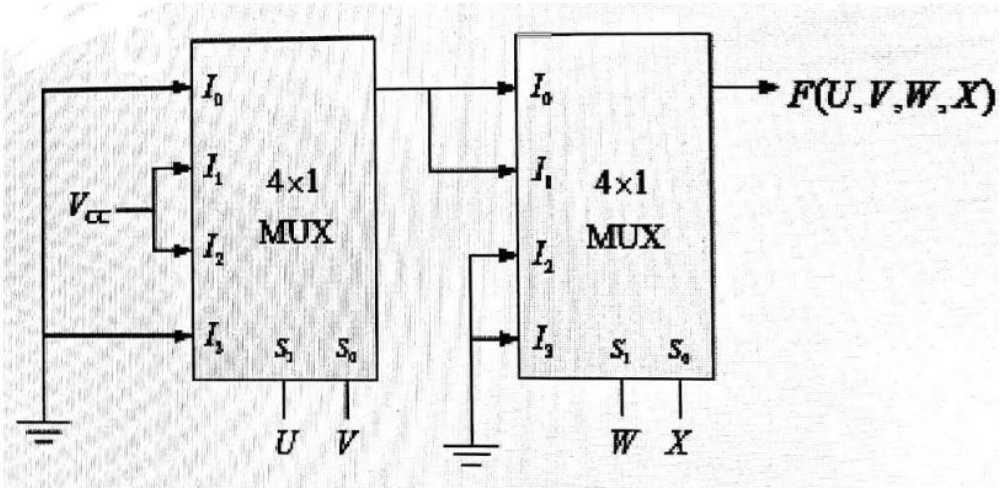
For the output to be high, both inputs to AND cute should be high.
The D-Flip Flop output is the same, after a delay.
Let initial input be 0; then $\bar{Q} = 1$ (For 1' D-Flip Flop). This is given as input to 2nd FF.
Let the second input be 1. Now, considering after 1 time interval; The output of 1st Flip Flop Is l and 1nd FF is also I. Thus Output = 1.

Ques 5: A four-variable Boolean function is realized using 4:1 multiplexers as shown in the figure. The minimized expression for F (U V W X) is

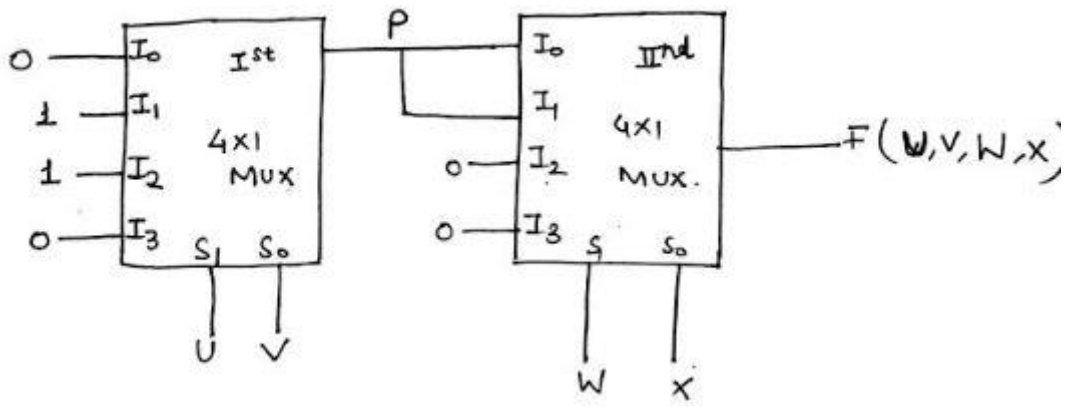
A) (U V+ U' V') W'
B) (U V +U' V') (W' X' + W' X)
C) (U V' + U' V) W'
D) (U V' +U' V) (W' X' + W' X)

Correct Option: C

Explanation



Sol: From the first MUX, we consider



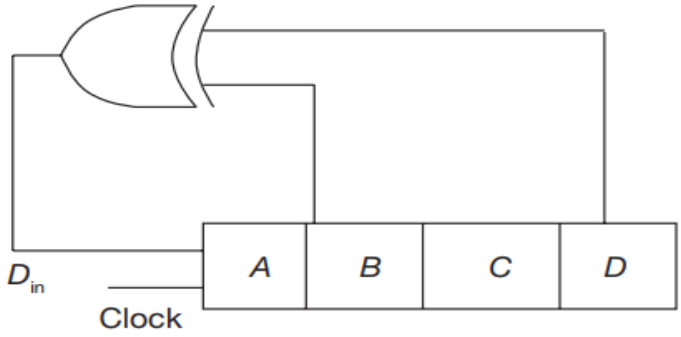
, <u>the output P is</u>

P = S1' S0' I0 + S1' S0 I1 + S1 S0' I2 + S1 S0 I3
P = U' V'.0 + U' V .1 + U V' .1 +U V .0
P = U' V + U V'----------(i)

<u>From the second MUX, the output F is</u>
F = W' X' P + W' X P
= P W' (X + X')
= P W' :: (X+ X')=1

Put the value P from equation (i) then,
F = (U' V + U V') W'
Option (C) is the correct answer.

Ques 6: A 4-bit shift register circuit configured for right-shift operation, i.e., D_{\text {in }} \right arrow A, A \right arrow B, B \right arrow C, C \right arrow D *D*in →*A*,*A*→*B*,*B*→*C*,*C*→*D* is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 is _____.



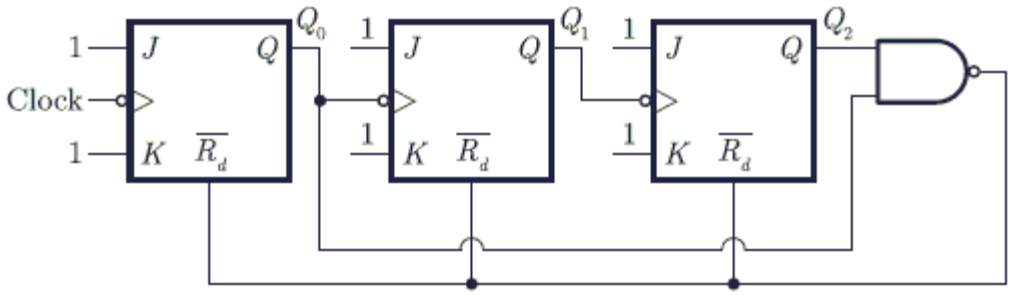
a. 1
b. 0
c. 2.5
d. 10
Correct Option: d
Explanation

$$D_{in} \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$$

	A		B		C		D
	1		1		0		1
1	0		1		1		0
2	0		0		1		1
3	1		0		0		1
4	0		1		0		0
5	0		0		1		0
6	0		0		0		1
7	1		0		0		0
8	1		1		0		0
9	1		1		1		0
10	1		1		1		1

∴ 10 clock pulses are required to get state of ABCD = 1111
Hence, the correct answer is (10).

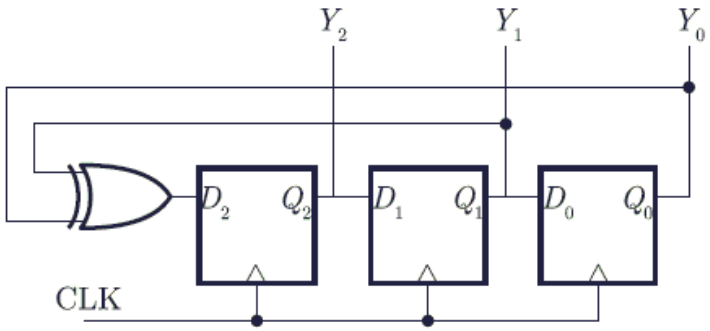
Ques-7
The circuit shown below consists of *JK* flip-flops, each with an active low asynchronous reset ($\overline{Rd}$ input). The counter corresponding to this circuit is



1. a modulo-5 binary up counter
2. a modulo-6 binary down counter
3. a modulo-5 binary down counter
4. a modulo-6 binary up counter

Correct Option: A
Explanation:
From the figure, it can be seen that it is a basic modulo up-counter configuration because clock is negative edge triggering at modulo-5.

Ques-8: A three bit pseudo random number generator is as shown in the figure. Initially, the value of output $Y_{\pm\pm} Y_2 Y_1 Y_0$ is set to 111. The value of output *Y* after three clock cycles is



1. 000
2. 001
3. 010
4. 100

Correct Option: D
Explanation:

For D-flip flop

$$Q(t+1) = D(t)$$

or next state = input

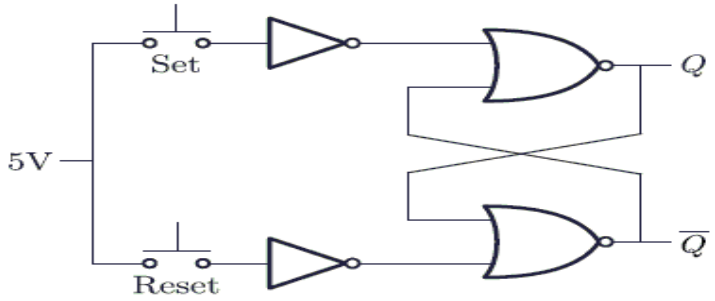
So, we may write

$$Q_2(t+1) = Q_1(t) + Q_0(t)$$
$$Q_1(t+1) = Q_2(t)$$
$$Q_0(t+1) = Q_1(t)$$

The resulting output is illustrated in the truth table below.

	Q_2	Q_1	Q_0
Given initial	1	1	1
1st clock	0	1	1
2nd clock	0	0	1
3rd clock	1	0	0

Ques-9: An SR latch is implemented using TTL gates as shown in the figure. The set and reset inputs are provided using the push-button switches. It is observed that the circuit fails to work as desired. The SR latch can be made functional by changing



a. NOR gates to NAND gates
b. inverters to buffers
c. NOR gates to NAND gates and inverters to buffers
d. 5 V to ground

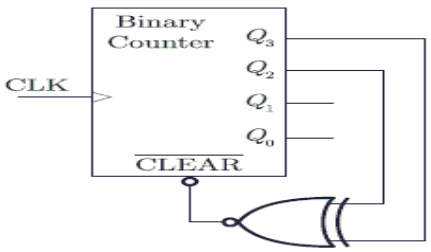
Correct Option: D
Explanation:

SR latch truth table is shown below.

S	R	Q
0	0	hold
0	1	reset
1	0	Set
1	1	Not Defined

The above truth table can be obtained from the given circuit, if we change 5 V to ground.

Ques-10: The figure shows a binary counter with synchronous clear input. With the decoding logic shown, the counter works as a



a. mod-2 counter
b. mod-4 counter
c. mod-5 counter
d. mod-6 counter

Correct Option: C

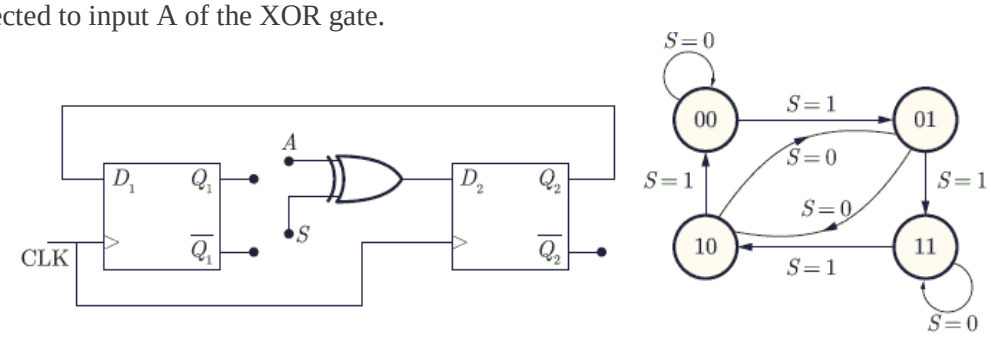
Explanation:

From figure, it can be observed that once the Ex-NOR gate output is '0' login counter will be reset to initial stage.

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	→ Here $Q_3 = 0$ $Q_2 = 1$ for first time at this time output of Ex NOR gate = '0' Counter will be reset. Hence it is modulo 5 counter
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	

Hence, it is modulo 5 counter.

Ques-11: The digital logic shown in the figure satisfies the given state diagram when Q1 is connected to input A of the XOR gate.



Suppose the XOR gate is replaced by an XNOR gate. Which one of the following options preserves the state diagram?

1. Input A is connected to $\overline{Q2}$
2. Input A is connected to $\overline{Q2}$
3. Input A is connected to $\overline{Q1}$and S is complemented
4. Input A is connected to $\overline{Q1}$

This input satisfies the state-diagram. Now, the XOR gate is replaced by XNOR gate. So, the output D_2 is

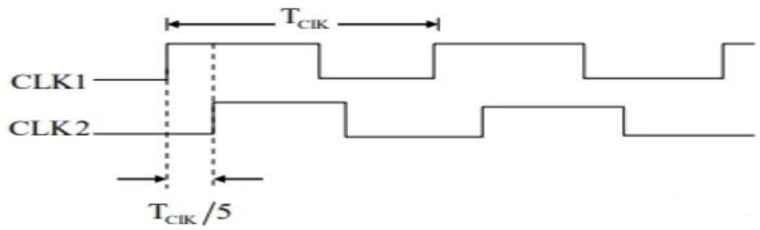
$$D_2 = \overline{A \oplus S}$$
$$= \overline{A}\,\overline{S} + AS$$

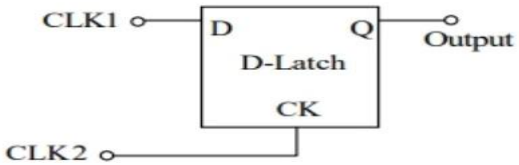
To preserve the state diagram, the D_2 must be same as obtained in previous case. Hence, the input A should be

$$A = \overline{Q}_1$$

i.e. input A is connected to $\overline{Q}_1$.

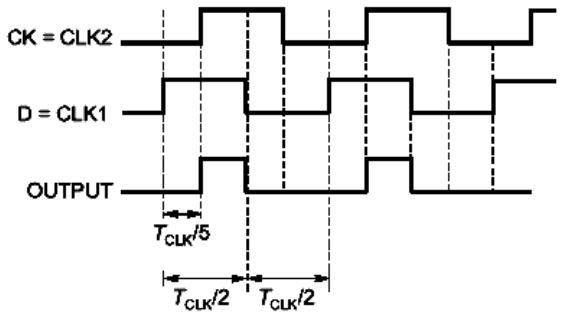
Ques-12: Consider the D-Latch shown in the figure, which is transparent when its clock input CK is high and has zero propagation delay. In the figure, the clock signal CLK1 has a 50% duty cycle and CLK2 is a one-fifth period delayed version of CLK1. The duty cycle at the output latch in percentage is





a. 25
b. 30
c. 35
d. 40

Correct Option: b
Explanation:

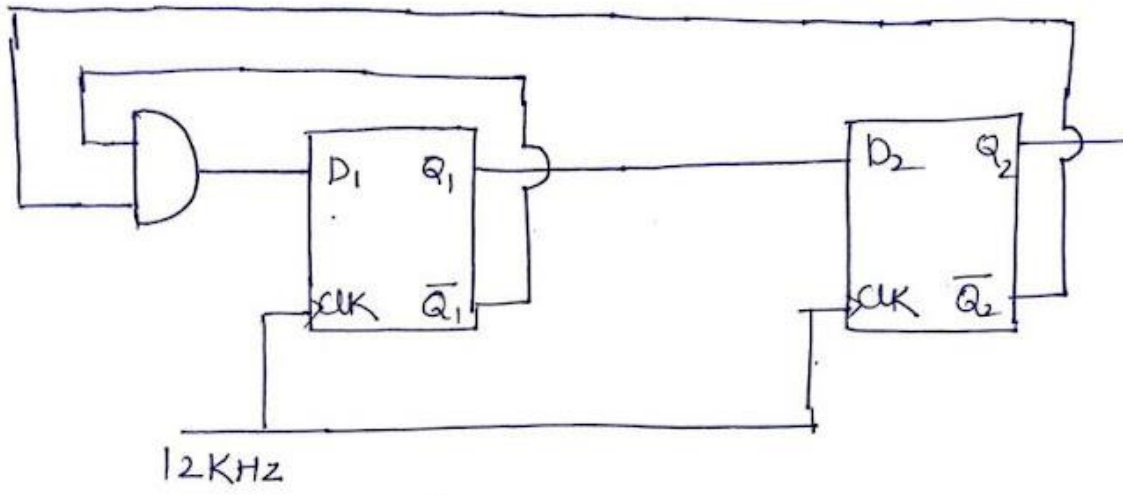


$$\text{Duty cycle of output} = \frac{\frac{T_{CLK}}{2} - \frac{T_{CLK}}{5}}{T_{CLK}} \times 100$$

$$= \frac{3}{10} \times 100 = 30\%$$

So duty cycle is 30%

Ques13 **: In the circuit shown, the clock frequency, i.e. the frequency of clk signal, is 12 kHz. The frequency of the signal at Q2 is …….kHz**.

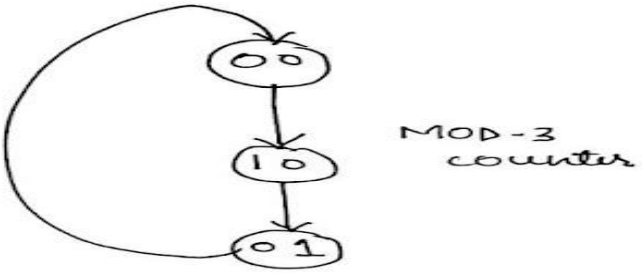


Solution : from the fig**.**
D1 = Q1'Q2'
D2 = Q1
Q1 = D1
Q2 = D2

State table:
Initially assume FF in reset mode i.e. Q2 and Q1 are zero.

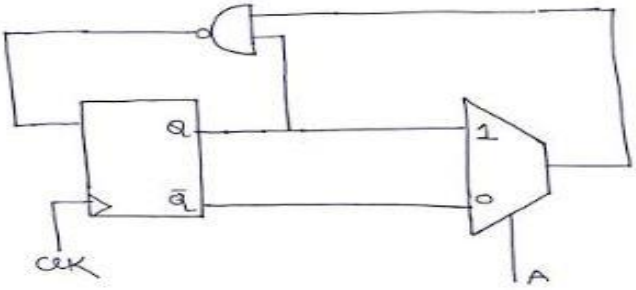
$D_1 = Q_1'Q_2'$	$D_2 = Q_1$	$Q_1 = D_1$ $Q_1 = 0$	$Q_2 = D_2$ $Q_2 = 0$	
1	0	1	0	← Initially (assume)
0	1	0	1	
0	0	0	0	← State repeated

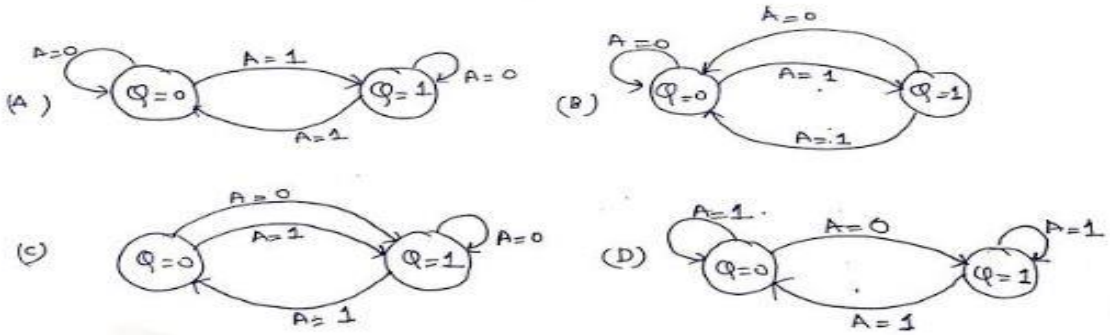
So this is the MOD-3 counter.



NOTE: In MOD-N counter, if the applied frequency is "f" then **output frequency is f/N.**
"MOD N" indicates the number of states in the counting sequence.

fout = fclk/3
= 12/3
= 4 kHz
Answer = 4 kHz
Ques14: The state transition diagram for the circuit shown is.





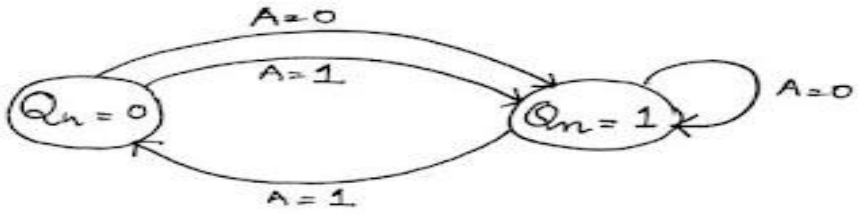
Correct Option: C
Explanation:

Solution : let's take mux output is Y.
$Y = A'Q_n' + AQ_n$ ……. (i)
And $D = (Q_nY)'$……. (ii)
Put Y value in equation (ii),

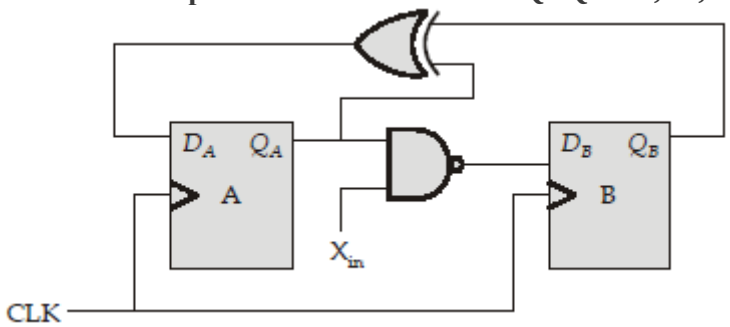
D = (Q_n. (A'Q_n' + AQ_n))'
On solving D = (AQ_n)'
And we know the next state equation of D FF is Q_{n+1} = D

Q_n (Present state)	A	Q_{n+1} =D = (AQ_n)' (Next state)
0	0	1
0	1	1
1	0	1
1	1	0

From the table, it is clear that it is NAND gate so state diagram is:
When Q=0 and A=0 then it goes to the Q=1
When Q=0 and A=1 then it goes to the Q=1
When Q=1 and A=0 then it goes to the Q=1 (same state)
When Q=1 and A=1 then it goes to the Q=0
option (c)



Ques15: A Finite State Machine (FSM) is implemented using the D-FFs A and B with logic gates as shown below. The four possible states of FSM are QAQB=00, 01, 10, 11.



Assume that Xin is held at constant logic level throughout the operation of FSM. Where the FSM is initialized to the QAQB=00 and clocked, after a few clock cycle, it starts cycling through.
A) All of the four possible states if Xin=1
B) Only two of the four possible states if Xin=0
C) Only two of the four possible states if Xin=1
D) All of the four possible states if
There are two cases, first if Xin=0 and second if Xin=1 And its given that state of Xin does not change in the middle of its working.

<u>Case 1 : Xin=0</u>
If one input of NAND gate is 0, then its output will be always 1. Hence in this case, DB would always receive 1 as input. We should make truth table accordingly as below :

Clock	QB	QA	DB=1	DA=QA⊕QB (calculated from previous states)
0 (initial)	0	0	1	0
1	1	0	1	1
2	1	1	1	0
3	1	0	1	1
4	1	1		

We can see that the output QBAA "after a few clock cycles" is like 10-11-10-11 and so on. Only two states 10 and 11 are in cycle.
Now see the options B and D. Option B matches here. But still we will take case 2 also to check what happens :

Case 2 : Xin=1

If one input of NAND gate is 1, then its output will be compliment of other input. Hence in this case, DB would always receive QA^{-} as input. We should make truth table accordingly as below :

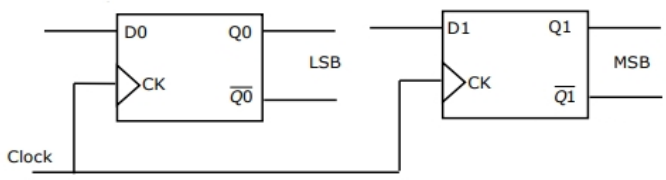
Clock	QB	QA	DB=QA^{-} (calculated from previous states)	DA=QA⊕QB (calculated from previous states)
0 (initial)	0	0	1	0
1	1	0	1	1
2	1	1	0	0
3	0	0	1	0
4	1	0	1	1
5	1	1	0	0
6	0	0		

We can see that the output QBAA 00-10-11-00-10-11 and so on. Three states 00, 10 and 11 are in cycle. Check the options A and C, Both are incorrect. **Hence considering both Cases, Correct answer is OPTION B.**

Ques 16:

Two D-flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following Q_1Q_0 sequence 00→01→11→10→00→.....

The inputs D_0 and D_1 respectively should be connected as



A) $\overline{Q_1}$ and Q_0

(B) $\overline{Q_0}$ and Q_1

(C) $\overline{Q_1}Q_0$ and $\overline{Q_1}Q_0$

(D) $\overline{Q_1}\ \overline{Q_0}$ and Q_1Q_0

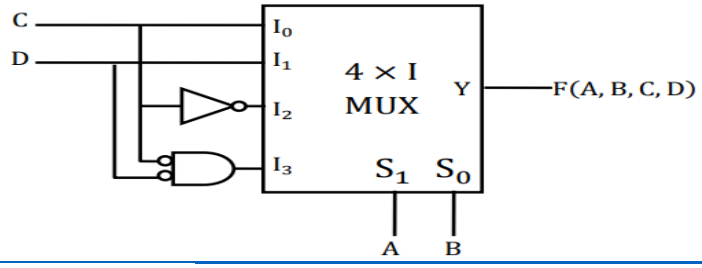
Correct Option: A
Explanation:

Present State		Next State			
Q_1	Q_0	Q_1^+	Q_0^+	D_1	D_0
0	0	0	1	0	1
0	1	1	1	1	1
1	1	1	0	1	0
1	0	0	0	0	0

So $D_1 = Q_0$ and $D_0 = \overline{Q_1}$

Ques 17 :

The Boolean function realized by the logic circuit shown is



a. **F = ∑ m (0,1,3,5,9,10,14)**
b. **F = ∑ m (2,3,5,7,8,12,13)**
c. **F = ∑ m (1,2,4,5,11,14,15)**
d. **F = ∑ m (2,3,5,7,8,9,12)**

Correct Option: d
Explanation:

$$Y = \overline{A}\,\overline{B}C + \overline{A}BD + A\overline{B}\,\overline{C} + AB\overline{C}\,\overline{D}$$

$$Y = \overline{A}\,\overline{B}C(D + \overline{D}) + \overline{A}B(C + \overline{C})D$$

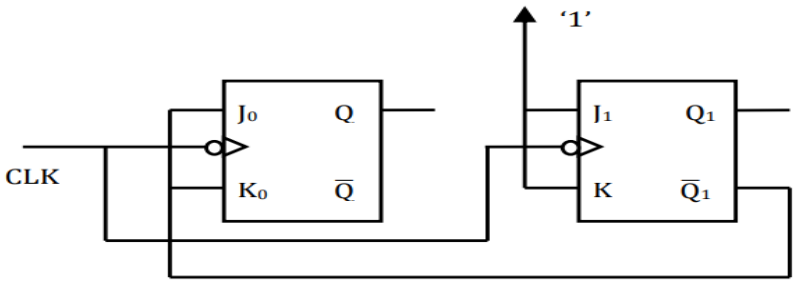
$$+ A\overline{B}\,\overline{C}(D + \overline{D}) + AB\overline{C}\,\overline{D} \left[\because x + \overline{x} = 1 \ \&\ x.1 = x\right]$$

$$= \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\overline{D} + \overline{A}BCD + \overline{A}B\overline{C}D + A\overline{B}\,\overline{C}D + A\overline{B}\,\overline{C}\,\overline{D} + AB\overline{C}\,\overline{D}$$

$$Y = \Sigma(2,3,5,7,8,9,12)$$

Ques 18:

Given that the initial state (Q_1Q_0) is 00, the counting sequence of the counter shown in the following figure is, Q_1Q_0 =



a. 00-11-01-10-00

b. 00-01-11-10-00

c. 00-11-10-01-00

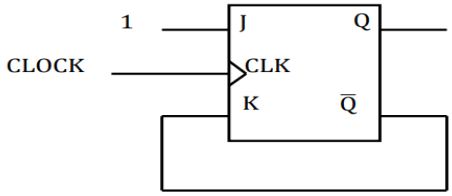
d. 00-10-01-11-00

Correct Option: a

Explanation: 00-11-01-10-00

Clock	J_1	K_1	J_0 K_0 ($\overline{Q}_1$ $\overline{Q}_1$)		Q_1	Q_0
	1	1	–	–	0	0
	1	1	1	1	1	1
	1	1	0	0	0	1
	1	1	1	1	1	0
	1	1	0	0	0	0

Ques 19: In the figure shown, the initial state of Q is 0. The output is observed after the application of each clock pulse. The output sequence at Q is



OPTIONS

a. 0 0 0 0 . . .

b. 1 0 1 0 . . .

c. 1 1 1 1 . . .

d. 1 0 0 0 . . .

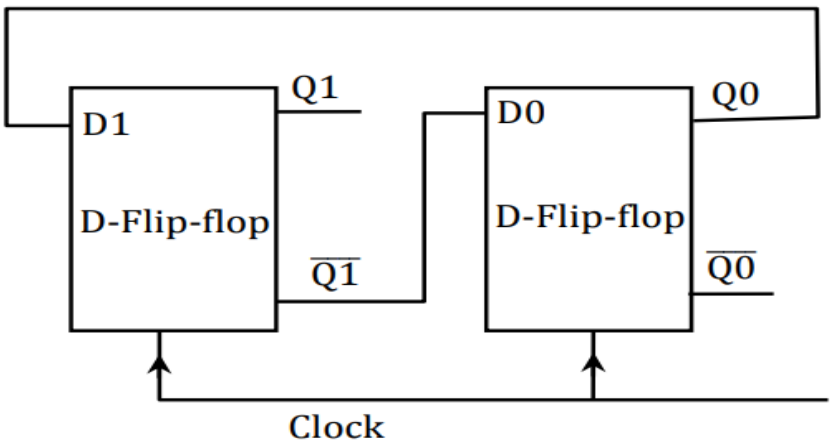
Correct Option: c

Explanation:

$J = 1$ & $K = \overline{Q}$ *Also the truth table*

J	K($\bar{Q}$)	$\bar{Q}_{n+t}$
1	1	0
1	0	1
1	0	1
–	–	1

Ques 20: The digital circuit shown below uses two negative edge - triggered D flip-flops. Assuming initial condition of Q1 and Q0 as zero, the output Q1 Q0 of this circuit is



OPTIONS

a. **00, 01, 10, 11, 00 ... .**

b. **00, 01, 11, 10, 00 ... ...**

c. **00, 11, 10, 01, 00 ... ...**

d. **00, 01, 11, 11, 00 ... ...**

Correct Option: b

Explanation

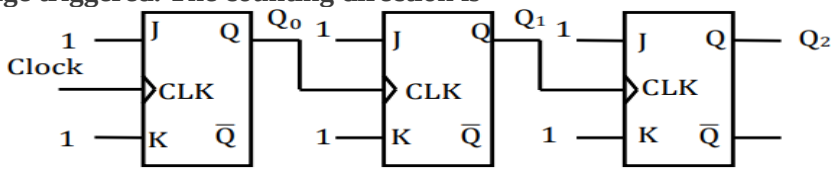
00, 01, 11, 10, 00 ... .

State table

Present state		Next state		$D_1 = Q_0$	$D_0 = Q_1$
Q_1	Q_0	Q_1	Q_0		
0	0	0	1	0	1
0	1	1	1	1	1
1	1	1	0	1	0
1	0	0	0	0	0

00, 01, 11, 10, 00

Ques 21: The figure below shows a 3-bit ripple counter, with Q_2 as the MSB. The flip-flops are rising-edge triggered. The counting direction is



a. **always down**

b. **always up**

c. **up or down depending on the initial state of Q0 only**

d. **up or down depending on the initial states of Q2, Q1 and Q0**

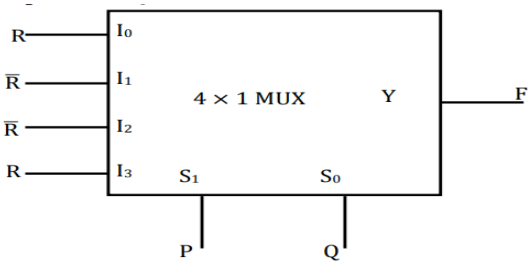
Correct Option: a

Explanation

Since triggering in positive edge triggering & Q of pervious flip-flop is input to next hence always down.

Ques 22:

The output F of the multiplexer circuit shown below expressed in terms of the inputs P, Q and R is



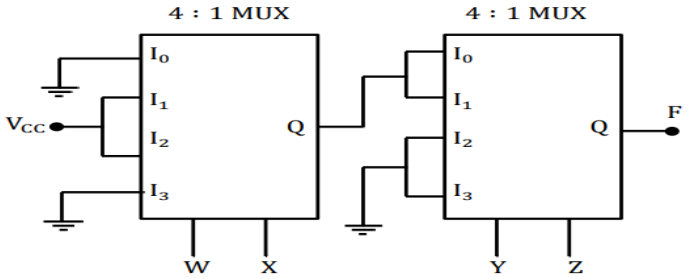
(A) F = P Θ Q Θ R
(B) F = PQ + QR + RP
(C) F = (P Θ Q) R
(D) F = (P Θ Q) R

Correct Option: a
Explanation

$$\begin{aligned} F &= \overline{PQ}R + \overline{P}Q\overline{R} + P\overline{QR} + PQR \\ &= P(\overline{QR} + QR) + \overline{P}(\overline{Q}R + Q\overline{R}) \\ &= P(\overline{Q \oplus R}) + \overline{P}(Q \oplus R) \\ &= P \oplus Q \oplus R \end{aligned}$$

Ques 23 :

In the circuit shown, W and Y are MSBs of the control inputs. The output F is given by



(A) $F = W\overline{X} + \overline{W}X + \overline{Y}\,\overline{Z}$

(B) $F = W\overline{X} + \overline{W}X + \overline{Y}Z$

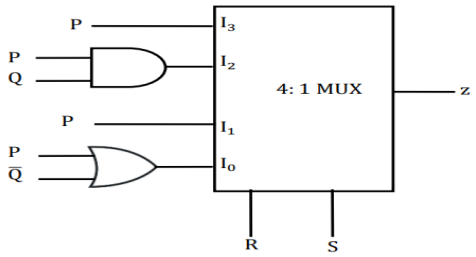
(C) $F = W\overline{X}\,\overline{Y} + \overline{W}X\overline{Y}$

(D) $F = (\overline{W} + \overline{X})\overline{Y}\,\overline{Z}$

Correct Option: C
Explanation

$$\begin{aligned} F &= \overline{W}X\overline{Y}\,\overline{Z} + W\overline{X}\,\overline{Y}\,\overline{Z} + \overline{W}X\overline{Y}Z + W\overline{X}\,\overline{Y}Z \\ &= \overline{W}X\overline{Y} + W\overline{X}\,\overline{Y} \end{aligned}$$

Ques 24 :
For the circuit shown in the following figure, I_0 - I_3 are inputs to the 4:1 multiplexer. R(MSB) and S are control bits.



The output Z can be represented by

(A) $PQ + P\overline{Q}S + \overline{Q}\,\overline{R}\,\overline{S}$

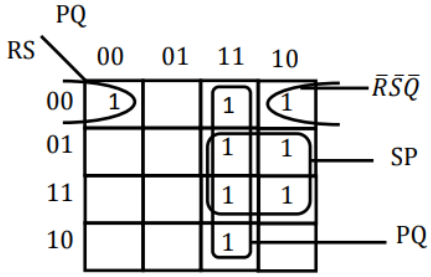
(B) $P\overline{Q} + PQ\overline{R} + \overline{P}\,\overline{Q}\,\overline{S}$

(C) $P\overline{Q}\,\overline{R} + \overline{P}QR + PQRS + \overline{Q}\,\overline{R}\,\overline{S}$

(D) $PQ\overline{R} + PQR\overline{S} + P\overline{Q}\,\overline{R}S + \overline{Q}\,\overline{R}\,\overline{S}$

Correct Option: A

Explanation



$$Z = \overline{R}\,\overline{S}(P+\overline{Q}) + \overline{R}\,SP + R\overline{S}\,PQ + RSP$$

$$\Rightarrow Z = \overline{R}\,\overline{S}(P+\overline{Q}) + \overline{R}SP + R\overline{S}\,PQ + RSP$$

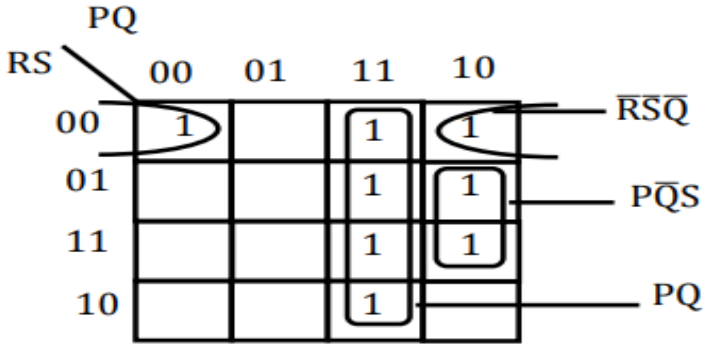
$$\Rightarrow Z = \overline{R}\,\overline{S}P + \overline{R}\,\overline{S}\,\overline{Q} + \overline{R}SP + R\overline{S}\,PQ + RSP$$

Its k map

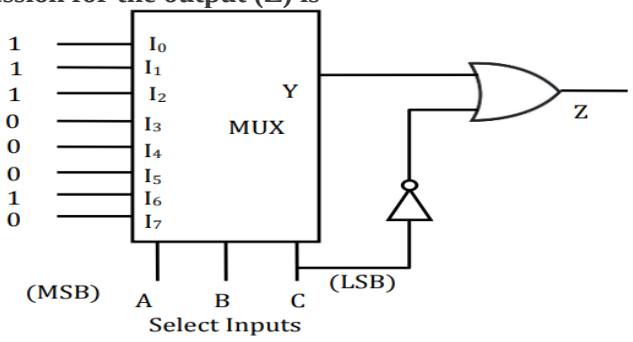
$$So\ Z = PQ + SP + \overline{R}\,\overline{S}\,\overline{Q}$$

Now only option (A) has two similar terms, we can say that option A is not most simplified version of Z it can be obtained as

So option A is correct choice



Ques 25: A combinational circuit using a 8-to-1 multiplexer is shown in the following figure, The minimized expression for the output (Z) is



(A) $C\ (\overline{A}+\overline{B})$

(B) $C\ (A\ +\ B)$

(C) $\overline{C}\ +\ \overline{A}\,\overline{B}$

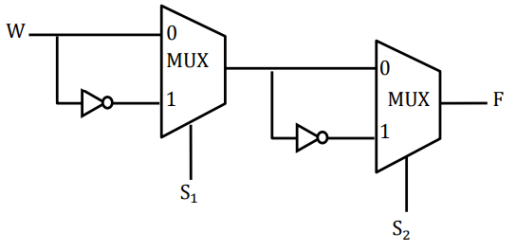
(D) $\overline{C}\ +\ AB$

Correct Option: C

Explanation

$$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + AB\overline{C}$$
$$Z = Y + \overline{C}$$
$$Z = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + AB\overline{C} + \overline{C}$$
$$= \overline{C}(1 + \overline{A}\,\overline{B} + \overline{A}B + AB) + \overline{A}\,\overline{B}C$$
$$= \overline{C} + \overline{A}\,\overline{B}C$$
$$= (\overline{C} + C)(\overline{C} + \overline{A}\,\overline{B})$$
$$= \overline{C} + \overline{A}\,\overline{B}$$

Ques 26: Consider the multiplexer based logic circuit shown in the figure;



Which one of the following Boolean functions is realized by the circuit?

(A) $F\ =\ W\overline{S}_1\overline{S_2}$

(B) $F\ =\ WS_1\ +\ WS_2\ +\ S_1S_2$

(C) $F\ =\ \overline{W}\ +\ S_1\ +\ S_2$

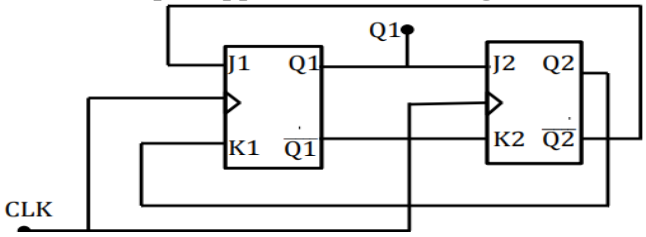
(D) $F\ =\ W \oplus S_1 \oplus S_2$

Correct Option: d

Explanation

$$Output\ of\ first\ MUX = W\overline{S}_1 + \overline{W}S_1 = W \oplus S_1$$
$$Let\ Y = W \oplus S_1$$
$$Output\ of\ second\ MUX = Y\overline{S}_2 + \overline{Y}S_2$$
$$= Y \oplus S_2$$
$$= W \oplus S_1 \oplus S_2$$

Ques 27: The outputs of the two flip-flops Q1, Q2 in the figure shown are initialized to 0, 0. The sequence generated at Q1 upon application of clock signal is



a. **01110...**

b. **00110...**

c. **01010...**

d. **01100...**

Correct Option: d

Explanation

This is a figure of Johnson counter

So

Q_1	Q_2
0	0
1	0
1	1
0	1
0	0
1	0

So = Q_1 = 01100