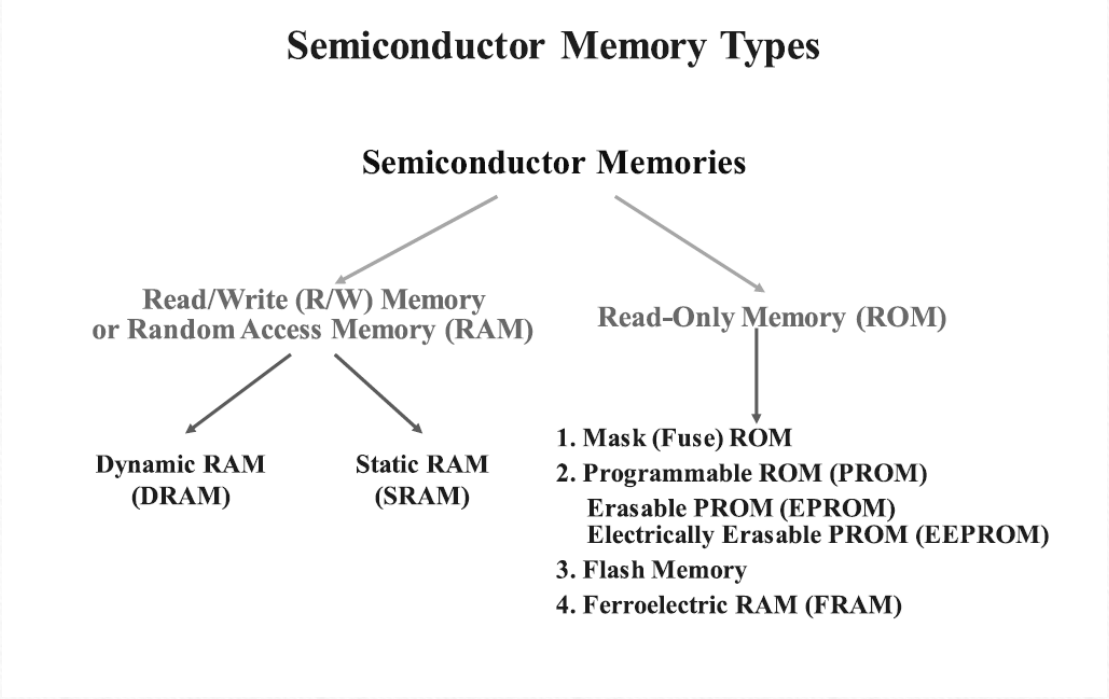
Semiconductor Memories

Semiconductor Memory Types

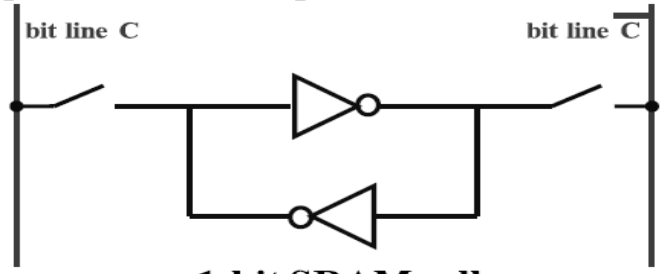


Semiconductor Memory Types(Cont.)

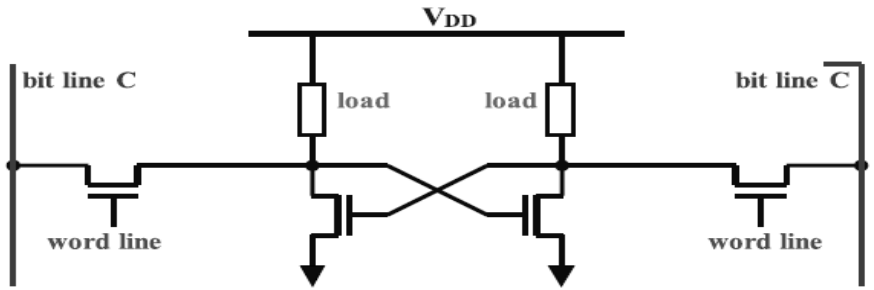
- **Design Issues**
  - **Area Efficiency of Memory Array:** # of stored data bits per unit area
  - **Memory Access Time:** the time required to store and/or retrieve a particular data bit.
  - **Static and Dynamic Power Consumption**
- **RAM: the stored data is volatile**
  - ***DRAM***
    - » A capacitor to store data, and a transistor to access the capacitor
    - » **Need refresh operation**
    - » **Low cost**, and **high density** ⇒ it is used for main memory
  - ***SRAM***
    - » Consists of a latch
    - » **Don't need the refresh operation**
    - » **High speed** and **low power consumption** ⇒it is mainly used for cache memory and memory in hand-held devices

Static Random-Access Memory (SRAM)

- **SRAM:** The stored data can be retained indefinitely, without any need for a periodic refresh operation.

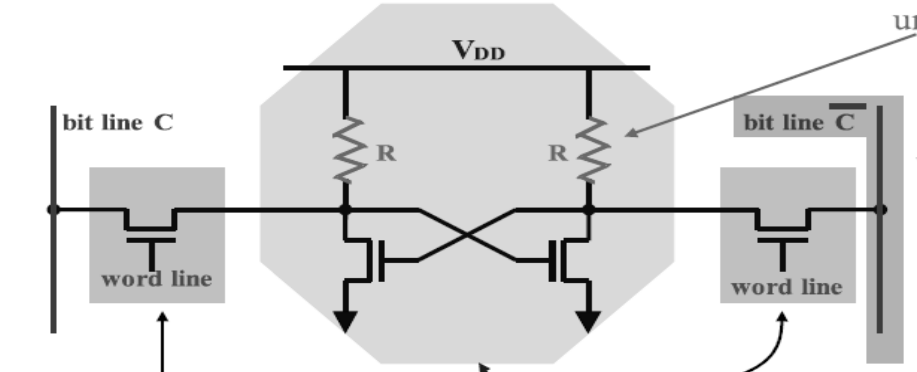


1-bit SRAM cell



- **Complementary Column** arrangement is to achieve a more reliable SRAM operation

Resistive-Load SRAM Cell



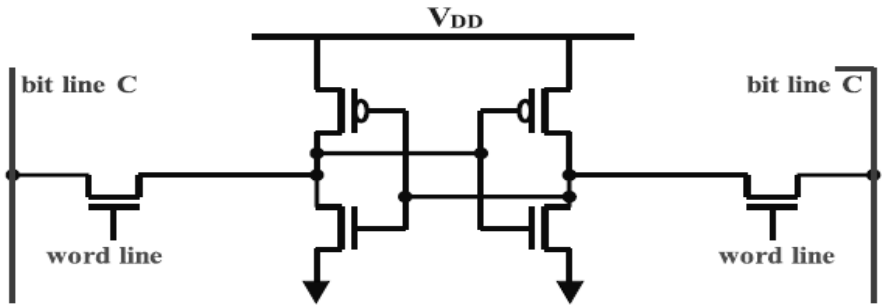
undoped polysilicon resistor

SRAM cell is accessed via two bit (column) lines C and its complement for reliable operation

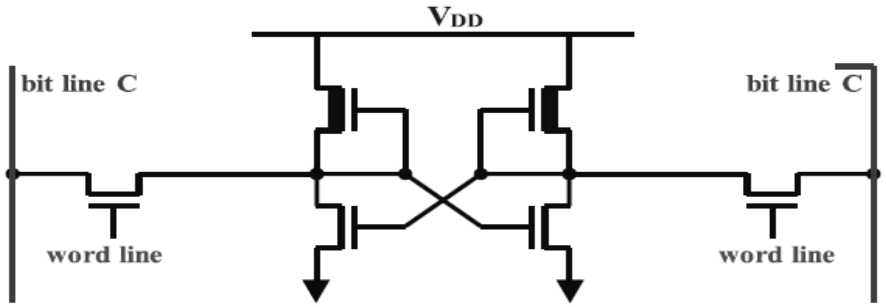
pass transistors to activated by a row select (RS) signal to enable read/write operators

Basic cross-coupled 2-inverter latch with 2 stable op points for storing one-bit

Full CMOS Depletion-Load SRAM Cell

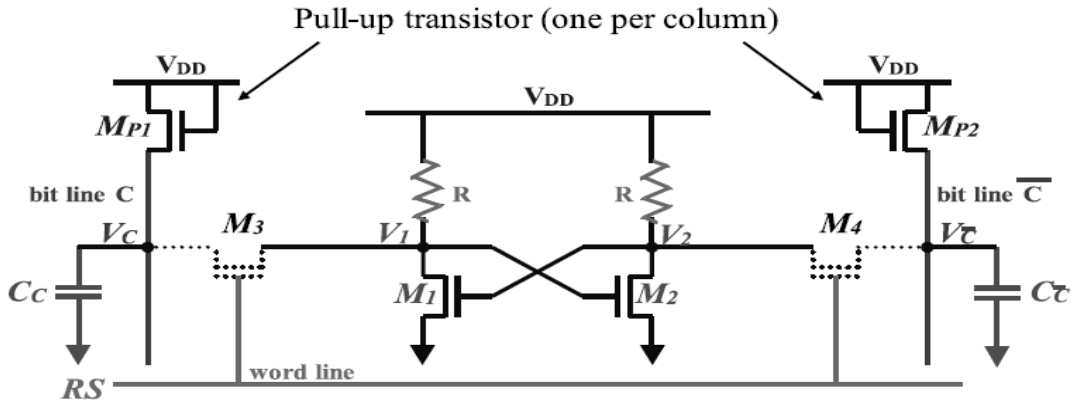


Full CMOS SRAM Cell



Depletion-Load SRAM Cell

SRAM Operation Principles

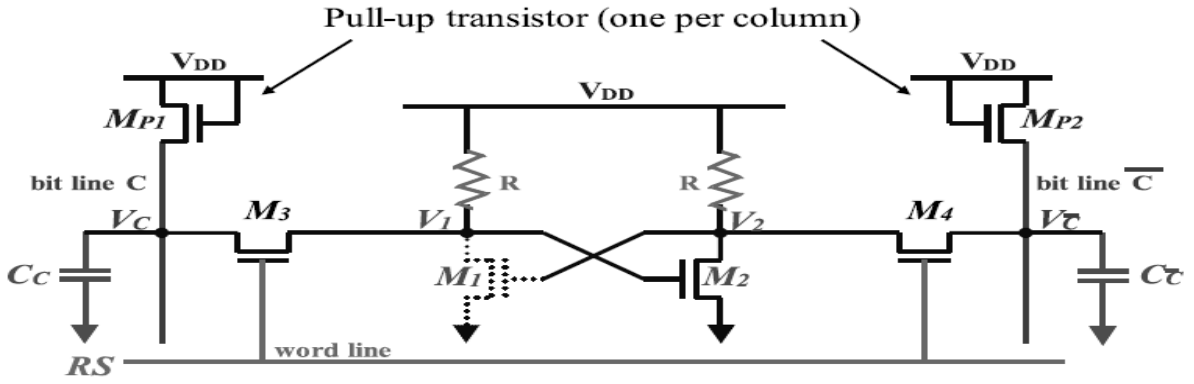


- ***RS=0***: The word line is not selected. M_3 and M_4 are OFF
  - One data-bit is held: The latch preserves one of its two stable states.
  - ***If RS=0 for all rows***: C_C and $C_{\bar{C}}$ are charged up to near V_{DD} by pulling up of M_{P1} and M_{P2} (both in saturation)

$$V_{\bar{C}} = V_C = V_{DD} - \left(V_{T0} + \gamma\sqrt{|2\phi_F| + V_C} - \sqrt{|2\phi_F|}\right)$$

  - Ex: $V_C = V_{\bar{C}} = 3.5\text{V}$ for $V_{DD} = 5\text{V}$, $V_{T0} = 1\text{V}$, $|2\phi_F| = 0.6\text{V}$

SRAM Operation Principles (Cont.)

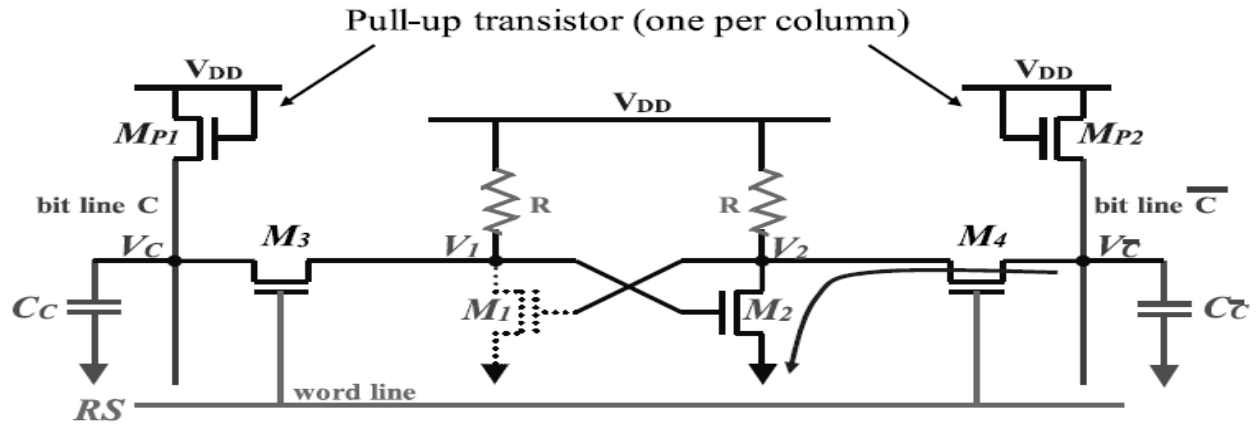


- *RS=1*: The word line is now selected. M_3 and M_4 are ON

Four Operations

1. **Write "1" Operation** ($V_1=V_{OL}$, $V_2=V_{OH}$ at $t=0^-$):
   $V_{\overline{C}} \Rightarrow V_{OL}$ by the *data-write circuitry*. Therefore, $V_2 \Rightarrow V_{OL}$, then M_1 turns ***off*** $V_1 \Rightarrow V_{OH}$ and M_2 turns on pulling down $V_2 \Rightarrow V_{OL}$.

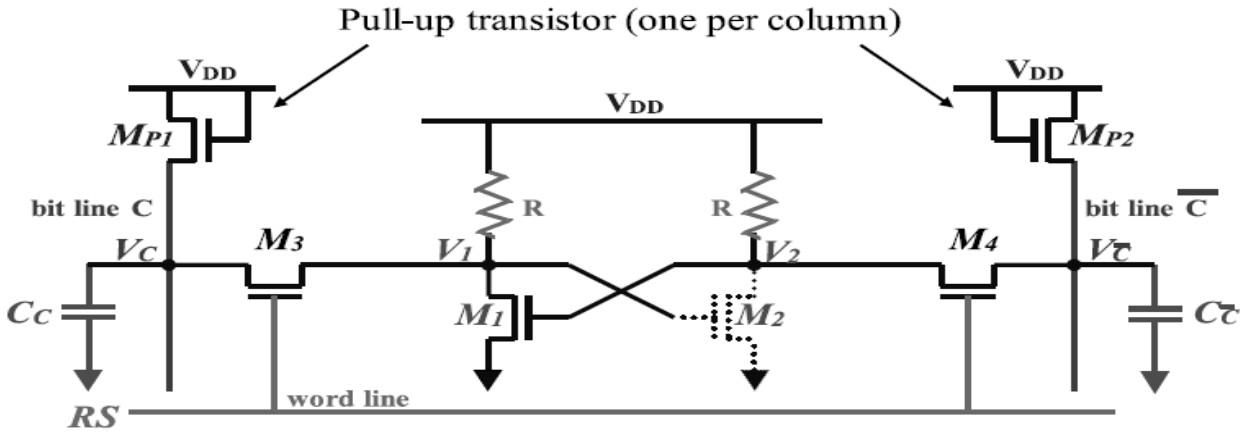
SRAM Operation Principles (Cont.)



2. **Read "1" Operation** ($V_1=V_{OH}$, $V_2=V_{OL}$ at $t=0^-$):

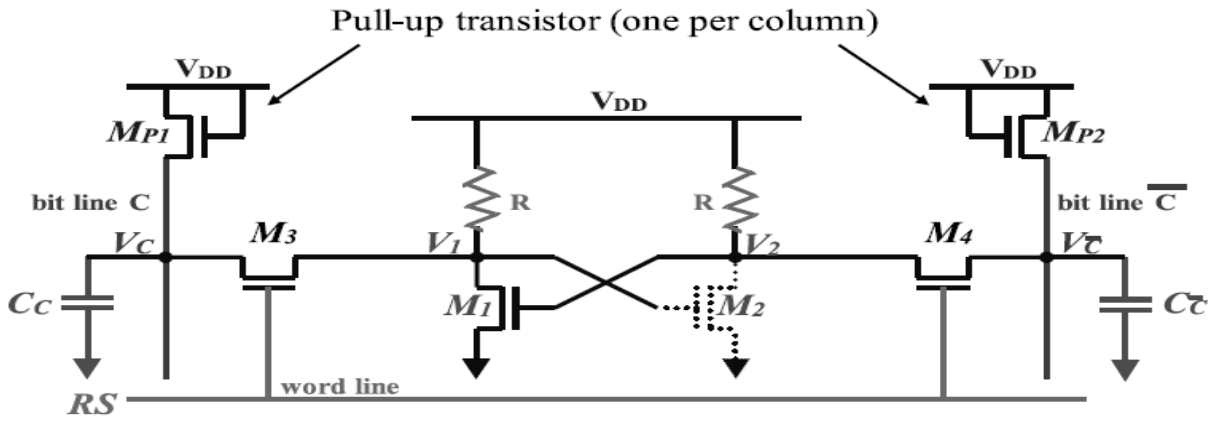
   V_C retains pre-charge level, while $V_{\overline{C}} \Rightarrow V_{OL}$ by M_2 ON. *Data-read circuitry* detects small voltage difference $V_C - V_{\overline{C}} > 0$, and amplifies it as a "*1*" data output.

SRAM Operation Principles (Cont.)



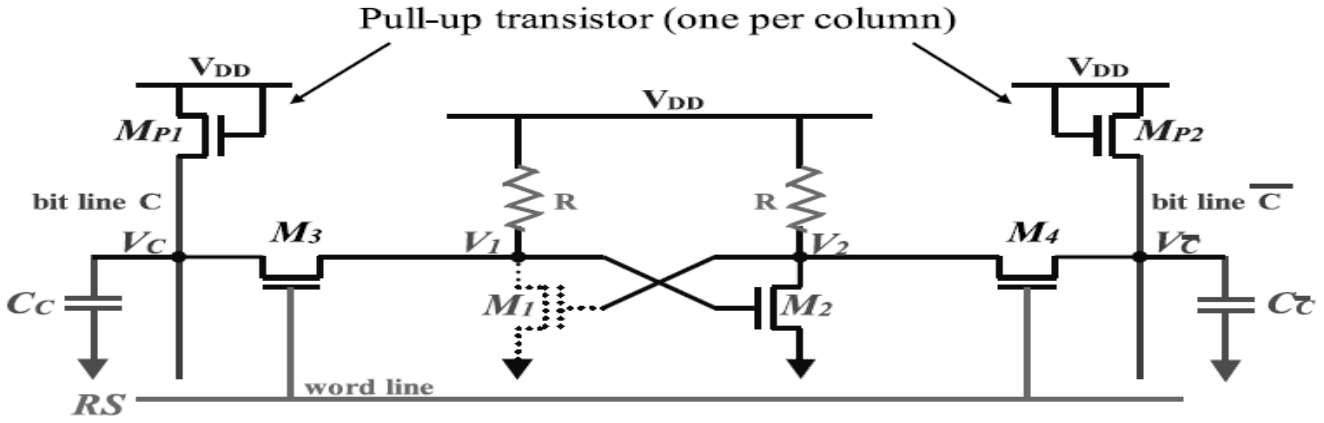
3. **Write "0" Operation** (V_1=V_{OH}, V_2=V_{OL} at $t=0^-$):
   $V_C \Rightarrow V_{OL}$ by the *data-write circuitry*.
   Since $V_1 \Rightarrow V_{OL}$, M_2 turns off, therefore $V_2 \Rightarrow V_{OH}$.

SRAM Operation Principles (Cont.)



4. **Read "0" Operation** ($V_1=V_{OL}$, $V_2=V_{OH}$ at $t=0^-$):
   $V_{\bar{C}}$ retains pre-charge level, while $V_C \Rightarrow V_{OL}$ by M_1 *ON*.
   Data-read circuitry detects small voltage difference $V_C - V_{\bar{C}} < 0$, and amplifies it as a "*0*" data output.

Static or "Standby" Power Consumption

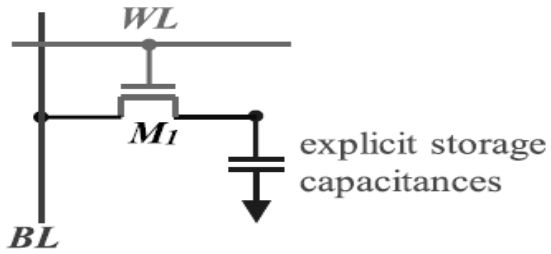


- ***Assume:*** 1 bit is stored in the cell $\Rightarrow M_1$ *OFF,* M_2 *ON* $\Rightarrow V_1 = V_{OH}$, $V_2 = V_{OL}$. *I.E. One load resistor is always conducting non-zero current.*

$$P_{standby} = (V_{DD} - V_{OL})^2 / R$$

with $R = 100\text{M}\Omega$ (undoped poly), $P_{standby} \approx 0.25\ \mu\text{W}$ per cell for $V_{DD} = 5\text{V}$

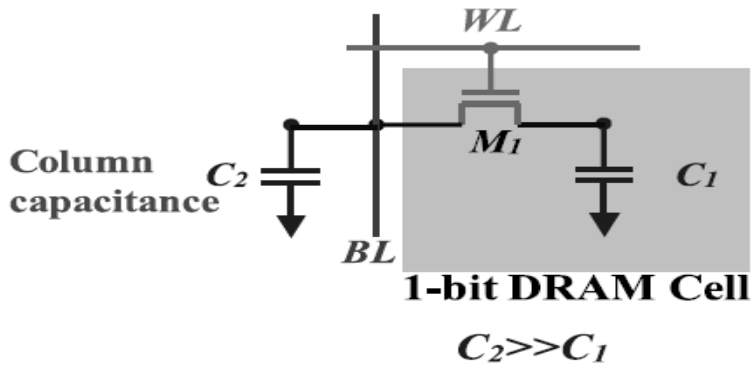
1-T DRAM Cell



One-Transistor DRAM Cell

- **Industry standard** for high density dram arrays
- **Smallest** component count and silicon area per bit
- Separate or "**explicit**" capacitor (dual poly) per cell

Operation of 1-T DRAM Cell



$C_2 >> C_1$

- **Write "1" OP:** $BL = 1$, $WL = 1$ (M_1 **ON**)$\Rightarrow C_1$ charges to "1"
- **Write "0" OP:** $BL = 0$, $WL = 1$ (M_1 **ON**)$\Rightarrow C_1$ discharges to "0"
- **Read OP:** destroys stored charge on $C_1 \Rightarrow$ destructive refresh is needed after every data read operation

Thank You