Indian Institute of Information Technology – Vadodara
End-Semester Examination Winter 2022-23
B. Tech. (IT & CSE)
CS-208: Computer Organization & Architecture

Time: 3:0 hrs. Max. Marks: 90
Attempt all questions

Q. 1	Do the followings	

	a) Load / Store operations contains 1 clock cycle; ADDD or SUBD operations contains 1 clock cycle; MULTD operation contains 3 clock cycles; DIVD operation contains 4 clock cycles; Pipeline has forwarding hardware for ***all FUs, except FP-Load / Store where operand is ready after W-stage;***
	LD F6, 20(R5)
	LD F2, 28(R5)
	MULTD F0, F2, F4
	SUBD F8, F6, F3
	DIVD F10, F0, F6
	ADDD F6, F8, F2
	SD F8. 50(R5)
	Show timing diagram:
	I. In which clock cycle does the second SD instruction complete? 18
	II. In which clock cycle does the second MULTD instruction complete? 19
	III. In which clock cycle does the second DIVD instruction complete? 22
	IV. Which kind of hazards present in between MULTD F0, F2, F4 and SDF8, 50(R5) RAW
		10

	b) // ADD TWO INTEGER ARRAYS// each stage requires one clock cycle
	LW R4 # 400
	L1: LW R1, 0 (R4
	LW R2, 400 (R4
	ADDI R3, R1, R2
	SW R3, 0 (R4)
	SUB R4, R4, #4
	BNEZ R4,
		10

	Calculate: (I) How many clock cycles will take execution of this segment on the regular (non-pipelined) architecture? 30 (II) How many clock cycles will take execution of this segment on the simple pipeline without forwarding or bypassing when the result of the branch instruction (new PC content) is available after WB stage? Show timing diagram 19 (III) Speedup 1.58	
	c) The stage delays in a 4 stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. Calculator (a) Execution Time in 4 Stage Pipeline, (b) Throughput in 4 Stage Pipeline, (c) Execution Time in 2 Stage Pipeline, (d) Throughput in 2 Stage Pipeline and (e) Throughput Increase% 33.33%	5 (5)

	d) System contains 3 ALUs for Integer operations, FP-addition and FP-multiplication: EX-stage for Integer operations contains 1 clock cycle; EX-stage for ADDD operation contains 2 clock cycles EX-stage for MULTD operation contains 4 clock cycles: // Formula calculation: Y (I) = K*X (I) + B
	Loop: LD F3, 0(R1
	LD F4, 8(R1)
	LD F2, 100(R0)
	MULTD F1, F2, F3
	ADDD F1, F1, F4
	SD F1, 200(R0)
	SUBI R0, R0, # 8
	BNEZ R0, Loop
	Calculate how many clock cycles will take loop execution **(from IF to IF of LD F2, ...)** of this segment on the this FP-pipeline with normal forwarding and bypassing when result of branch instruction (new PC content) is available after completion of the ID stage. Show timing diagram?
		5

Q. 2	a) Consider a pipelined processor with five stages, Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for SUB instruction and the register read is performed in the EX stage, The EX stage takes one cycle for SUB instruction and two cycles for DIV instruction. Ignore pipeline register latencies. Consider the following sequence of six instructions: SUB, DIV, SUB, DIV, SUB, DIV	5 (5)

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	Assume that every MUL instruction is data-dependent on the SUB instruction just before it and every SUB instruction (except the first SUB) is data-dependent on the DIV instruction just before it. Find the speed-up? b) A program has 2000 instructions in the sequence L.D, ADD.D, L.D, ADD.D, L.D, and ADD.D. The ADD.D instruction depends on the L.D instruction right before it. The L.D instruction depends on the ADD.D instruction right before it. If the program is executed on the 5-stage pipeline what would be the actual CPI with and without operand forwarding technique?	5
Q. 3	a) There is a 5 stage processor having the stages Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO).If the phases IF, ID, OF, and WO stages take 1 clock cycle. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Operand forwarding is used in the pipeline (for data dependency, OF stage of the dependent instruction can be executed only. I0: MUL R2, R0, R1 I1: DIV R5, R3, R4 I2: ADD R2, R5, R2 I3: SUB R5, R2, R6	5
	b) An instruction in the pipeline has five stages without any branch prediction and these stages are Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Operand Write (OW). The stage delays for IF, ID, OF, EX and OW phases are 5 nsec, 7 nsec, 10 nsec, 8 nsec and 6 nsec, respectively.There are intermediate storage buffers after each stage and the delay of each buffer is 1 nsec. A program consisting of 12 instructions I1, I2,. …, I12 is executed in the pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time needed to complete the program is:	5
Q. 4	Loop: L.D F4, 0 (R1) MUL.D F8, F4, F0 L.D F6, 0 (R2) ADD.D F10, F6, F2 ADD.D F12, F8,F10 S.D F12,0 (R3) DADDUI R1, R1, #8 DADDUI R2, R2, #8 DADDUI R3, R3, #8 DSUB R5, R4, R1 BNEZ R5, Loop a) Consider the role of the compiler in scheduling the code. Rewrite this loop, but let every row take a cycle. If an instruction cannot be issued on a given cycle (because the current instruction has a dependency that will not be resolved in time), write STALL instead, and move on to the next cycle to see if it can be issued then. Assume that a NOP is scheduled in the branch delay slot (effectively stalling 1 cycle after the branch). Explain all stalls, but don't reorder instructions. How many cycles elapse before the second iteration begins? Show your work. b) Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches whereas five cycles for memory operations.Assume that the relative frequencies of these operations are 40%.20% and 40% respectively. Due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from the pipeline ? c) Consider the following instruction sequence executed on a MIPS floating point pipeline. Operand forwarding is implemented. [R indicates integer registers and F indicates floating point registers]. Find the clock cycle in which STORE instruction reaches MEM stage. If 8(R2) contains value 'X' and F2 contains value 'A', then what is stored in 16(R3) LOAD F4, 8(R2): FMUL F0, F4, F2; FADD F3, F0, F2; **STOR F3, 16(R3)?**	5 5 10
Q. 5	1) Difference between PC relative and direct addressing mode. 2) Explain Tomasulo's Algorithm with an example. Draw necessary steps. 3) What is the TLB? Explain its role in virtual memory. 4) What are data hazards? Explain elimination techniques with suitable examples.	5x4=20

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