EC261 Experiment:5

Implementation of a D and JK flip flop and verification of its operation.

Apparatus: Logic trainer kit, IC 74LS173, IC 74HC73, wires.

Operation of D Flip Flop

1. D=1: Flip flop will be in set state(Q=1), D=0: Flip flop will be in reset state (Q=0) given that Clk (Clock is positive edge triggered).

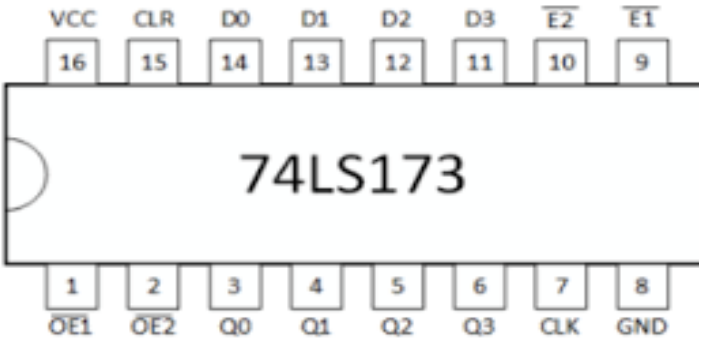

Fig-1 Quad D Flip Flop IC

Operation of JK Flip Flop

1. J=0, K=0: there will be no change in the state means present state will be same as next state.
2. J=0, K=1: flip flop will be in reset state.
3. J=1, K=0: flip flop will be in set state.
4. J=1, K=1: Flip flop will be in Toggle mode.

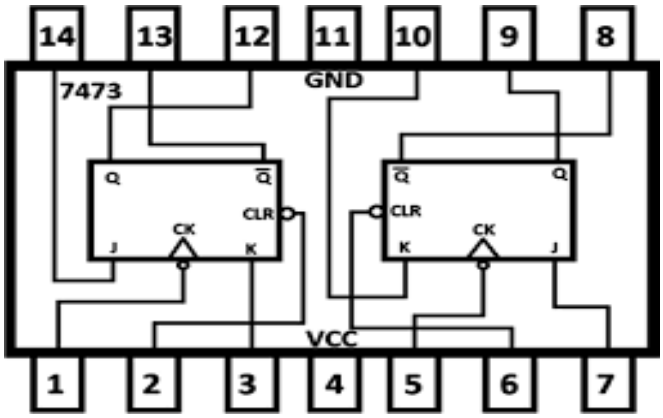

Fig-2 Dual JK Flip Flop IC 74HC73

Note:- **In addition to the implementaion of all of these given IC on hardware kit, it is mandatory to write and simulate the verilog code for the experiment.**