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☆ REGISTER :-

⇒ Register are used to store group of bits.

⇒ To store n bit n FF are cascaded in register.

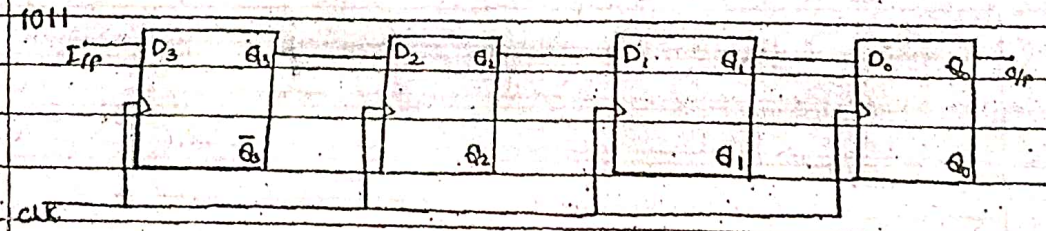
⇒ Register are four type (Depending on I/P and O/P) :-

(i) SISO (Serial in serial out).
(ii) SIPO (most Imp).
(iii) PISO
(iv) PIPO

⇒ Depending on application the register are two type:-

(i) Shift register
(ii) Storage register.

(A) SISO (Serial in Serial out) :-



Data	Q_3 Q_2 Q_1 Q_0	CLK.
1011	0 0 0 0	0
	1 0 0 0	1
	1 1 0 0	2
	0 1 1 0	3
	1 0 1 1	4

⇒ For serial in register the n bit data storage requires n clock pulse.

⇒ In SISO register to store n bit data is require n clock pulse.

⇒ SISO register used to provide n clock pulse delay to I/P data.

$$\text{delay} = n\,T_{CLK}$$

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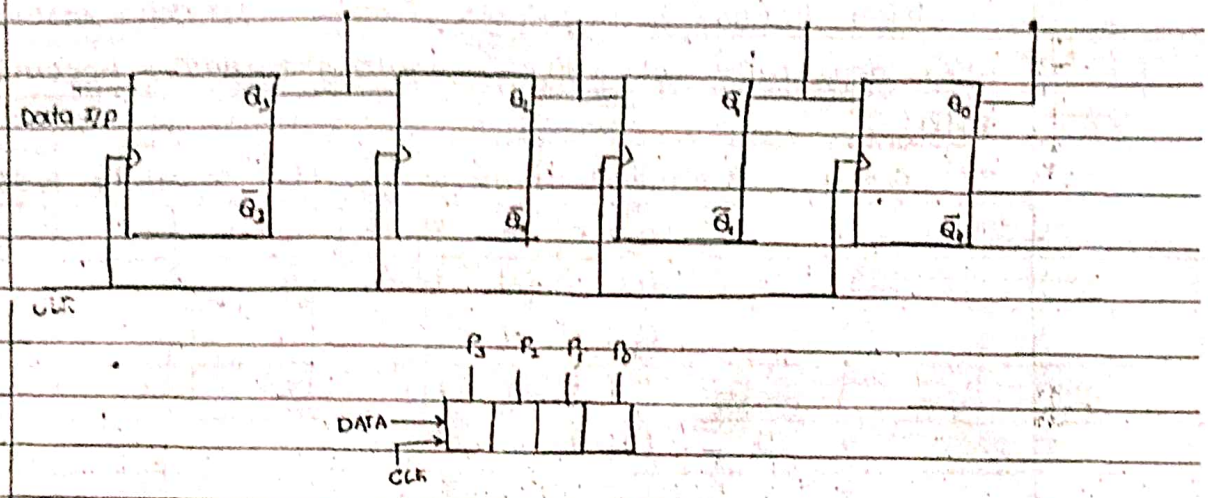
⇒ To provide n bit data serially out it requires (n-1) clock pulse.

(3) SIPO (Serial in parallel out) :-



⇒ In SIPO register to provide n bit data serially in it requires n clock pulse and provide parallel o/p it requires 0 clk pulse, required.

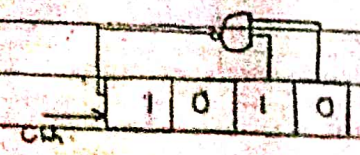
⇒ It is used to serial to parallel converter.

⇒ SIPO is used to convert Temporial code to spacial code.

⇒ Slow to fast converter.

serial, t =
Parallel = Spacial code.

Q:- The ckt shown in the fig. if 4 bit SIPO register which in initially loaded with 1010. If store three clk pulses applied then the data if the system is.



(a) 1010
(b) 1101
(c) 1111
(d) 0000

1 0 1 0 0
1 1 0 1

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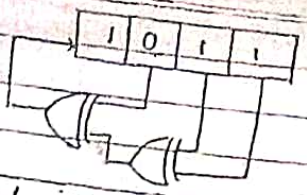
Q:-



(a) 4
✓(b) 7
(c) 11
(d) 15

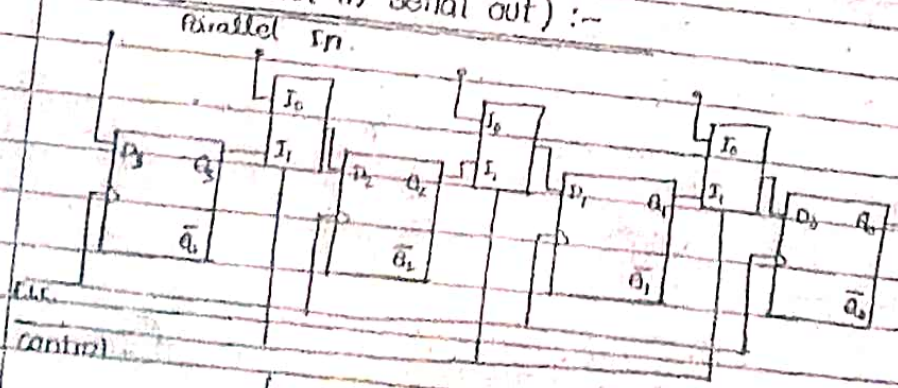
Initially loaded 1011. if CLK pulse applied continuously after how many clk pulse again the data become 1010.

Sol: O/P of 3 variable X-OR is 1 if no. of 1's is odd.

CLK	Q_3	Q_2	Q_1	Q_0
1	0	1	0	1
2	0	0	1	0
3	1	0	0	1
4	1	1	0	0
5.	1	1	1	0
6.	0	1	1	1
7	0	0	1	1 ✓
8	0	0	0	1
9.	1	0	0	0
10	0	1	0	0
11	1	0	1	0

after 7-clock

(c) PISO (Parallel In serial out) :-



Control = 0	= Parallel In
Control = 1	= Serial out

→ In PISO register to provide parallel in it require 1 clock pulse and to provide serial out (n-1) clock pulse.

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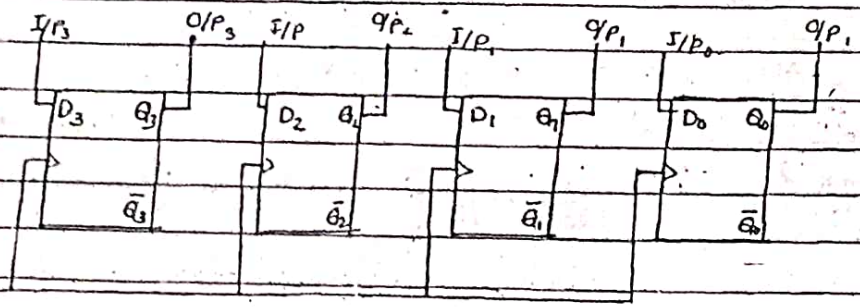
⇒ PISO is also used to convert spacial code to temporial code.

(D) PIPO (Parallel in parallel out) :-

⇒ PIPO is used as storage register.
⇒ for Parallel in it requires 1 clock pulse.
⇒ for parallel out it requires 0 clock pulse.



Important :-

	I/P	O/P
SISO	n	n-1
SIPO	n	0
PISO	1	n-1
PIPO	1	0

⇒ Each shift left register operation provide multiplication by 2.
⇒ If n shift left operation performed then data is multiplied by 2^n.
⇒ Each shift right operation performed then data is divided by 2.
⇒ If n shift right operation performed then data is divided by 2^n.