Indian Institute of Information Technology Vadodara

CS/IT 429

Switch Level Modeling

Dr. Yash Agrawal
Visiting Faculty, IIIT Vadodara
Associate Professor, DA-IICT Gandhinagar

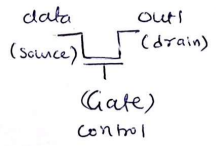
Introduction

What is Switch Level Modeling…?

Primitives

Gate Level Primitive			Switch Level Primitive		
Multi Input Gates	Multi Output Gates	Tristate Gates	Unidirectional	Bidirectional	Pull Gates
and nand or nor xor Xnor	buf not	bufif0 bufif1 notif0 notif1	nmos pmos cmos rnmos rpmos rcmos	tran tranif0 tranif1 rtran rtranif0 rtranif1	pullup pulldown

Switch Level Primitive



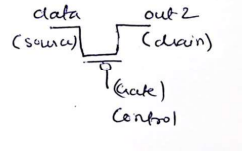
nmos

Syntax

nmos <instance name> (<drain>, <source>, <gate>);

Example

nmos n1(out1, data, control);



pmos

Syntax

pmos <instance name> (<drain>, <source>, <gate>);

Example

pmos n1(out2, data, control);

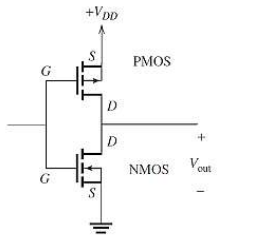
nmos		control			
data		0	1	x	z
	0	z	0	x (L)	x (L)
	1	z	1	x (H)	x (H)
	x	z	x	x	x
	z	z	z	z	z

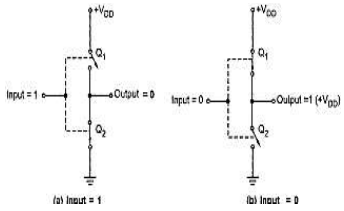
L → 0 or z
H → 1 or z

pmos		control			
data		0	1	x	z
	0	0	z	x (L)	x (L)
	1	1	z	x (H)	x (H)
	x	x	z	x	x
	z	z	z	z	z

Switch Level Modeling

$$\text{out} = \overline{\text{in}}$$

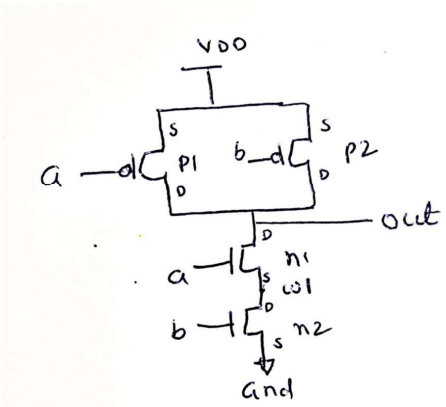




⇨ Implement using Switch Level Model

Switch Level Modeling

$$\text{out} = \overline{\text{a} \cdot \text{b}}$$



⇨ Implement using Switch Level Model

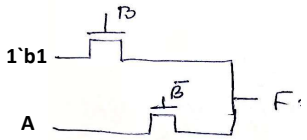
Switch Level Modeling

$$\text{F} = \text{A} + \text{B}$$

B	A	F
0	0	0
0	1	1
1	0	1
1	1	1

A

1



⇨ Implement using Switch Level Model

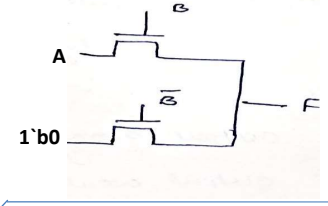
Switch Level Modeling

$$\text{F} = \text{A} \cdot \text{B}$$

B	A	F
0	0	0
0	1	0
1	0	0
1	1	1

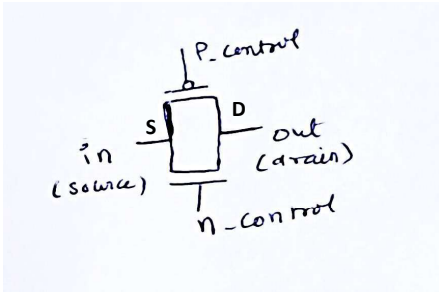
0

A



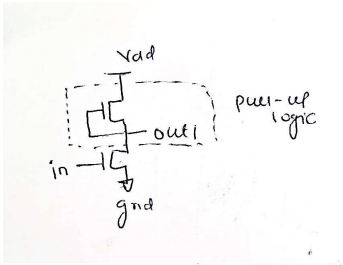
⇨ Implement using Switch Level Model

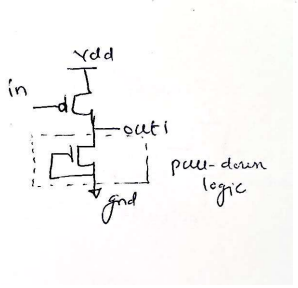
Switch Level Modeling



⇨ Implement using Switch Level Model

Switch Level Modeling

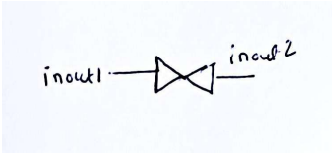




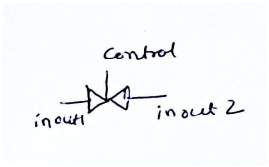
⇨ Implement using Switch Level Model

Switch Level Modeling

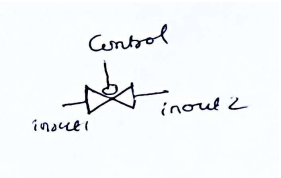
Bidirectional switches



tran t1(inout1, inout2);

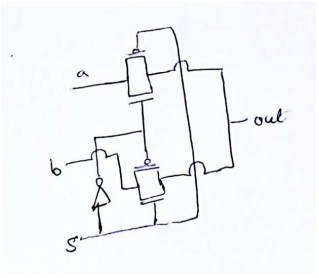


tranif1 t2(inout1, inout2, control);

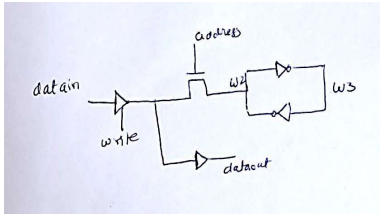


tranif0 t3(inout1, inout2, control);

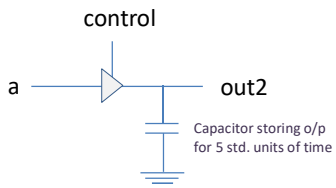
Switch Level Modeling

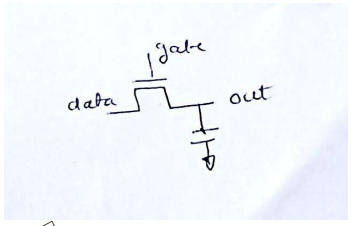


⇨ Implement the circuits using Switch Level Model



Usage of 'nmos' logic





Implement such as above circuits act as capacitor/storing element

I am available/approachable at

email: yash_agrawal@iiitvadodara.ac.in
yash_agrawal@daiict.ac.in