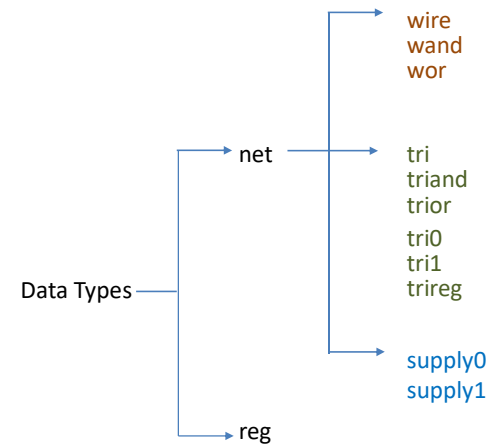




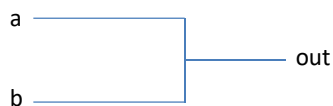
Data Types

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Data Types



Data Types



Can you write the Verilog HDL code

```

module logic1 (out, a, b);
input a, b;
output out;
assign out = a;
assign out = b;
endmodule
    
```



a = 1'b0;	b = 1'b0;	out = 0	} Logic contention
a = 1'b0;	b = 1'b1;	out = x	
a = 1'b1;	b = 1'b0;	out = x	
a = 1'b1;	b = 1'b1;	out = 1	

Data Types

How to avoid Logic Contention...?

Use wand/wor logics...

wor → If any input is 1, o/p is 1

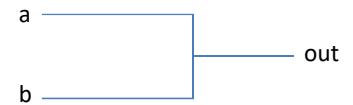
wand → If any input is 0, o/p is 0

```

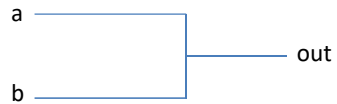
module logic2 (out, a, b);
input a, b;
output out;
wand out;
assign out = a;
assign out = b;
endmodule
    
```



Identify the output values...!



Data Types



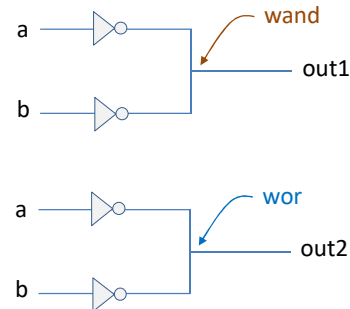
```
module logic3 (out, a, b);
input a, b;
output out;
wire/wand/wor out;

assign out = a;
assign out = b;

endmodule
```

Identify the output values for all cases...!

Data Types



Write the HDL for the defined modules..!

Data Types

```
module logic6 ();
wire w1, w2, w3, w4;
tri0 t01, t02, t03, t04;
tri1 t11, t12, t13, t14;

assign w1 = 0,
       w2 = 1'bz,
       w3 = 1'b1;

assign t01 = 0,
       t02 = 1'bz,
       t03 = 1'b1;

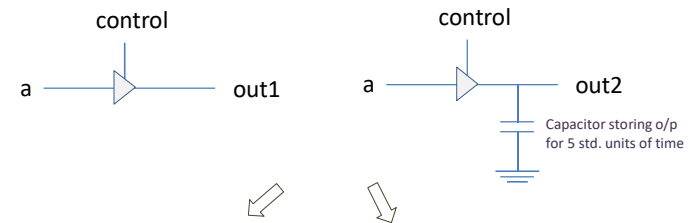
assign t11 = 0,
       t12 = 1'bz,
       t13 = 1'b1;

initial begin
#1 $display (w1, w2, w3, w4);
   $display (t01, t02, t03, t04);
   $display (t11, t12, t13, t14);
end

endmodule
```

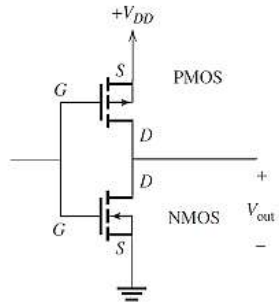
Identify the output values...!

Data Types



Write the HDL for the defined modules..!

Identify the output values for all cases...!



Write the HDL for the defined modules..!

- reg
- integer
- time
- real
- realtime

```
module logic7 (v1, v2, v3, v4);
output wire v1;
output reg v2;
output integer v3;
output real v4;
```

```
assign v1 = 5;
```

```
initial
begin
v2 = 5;
v3 = 5;
v4 = 5;
end
endmodule
```

Identify the output values...!

```
module logic8 (v1, v2, v3, v4);
output wire v1;
output reg v2;
output integer v3;
output real v4;
```

```
assign v1 = -5;
```

```
initial
begin
v2 = -5;
v3 = -5;
v4 = -5;
end
endmodule
```

Identify the output values...!

Variable Data Types

```
module logic9 (a, b, c, d, e, f);
```

```
output real a, b, c, d;
```

```
output integer e, f;
```

```
initial
```

```
begin
```

```
  a = 2.2e2;
```

```
  b = -2.10;
```

```
  c = a+b;
```

```
  d = a * b;
```

```
  e = c;
```

```
  f = d;
```

```
end
```

```
endmodule
```



Identify the output
values...!

Variable Data Types

```
module logic10 ();
```

```
time a, b;
```

```
realtime c, d;
```

```
initial
```

```
begin
```

```
  a = -5;
```

```
#1 b = $time;
```

```
  c = -5;
```

```
#1 d = $realtime;
```

```
end
```

```
endmodule
```



Identify the output
values...!

I am available/approachable at

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