Indian Institute of Information Technology – Vadodara

Mid-Semester Examination Autumn 2022-23

B. Tech. (IT & CSE)

EC-201: Digital Logic Design

Time: 2:0 hrs **Max. Marks: 60**

Attempt all questions

Q. 1 Do the followings

(a) $(110110)_2 = (\ ?\ )_{10}$ 2

(b) For function AB+AB'C+AB'C', find the minimum no. of NAND Gates? 2

(c) Minimize the logical expression (A+B+C) (A+B'+C) (A+B+C') using Boolean theorems. 2

(d) Identify and remove the redundant term from the logical expression AB+A'C+BC 2

(e) Minimize the function using K-Map $f(A,B) = \Sigma m(0,2,3)$. 2

Q. 2

(a) Implement the full subtractor circuit using minimum number of NAND gate only. 5

(b) Explain carry look ahead adder with suitable diagram and drive the expression for it. 5

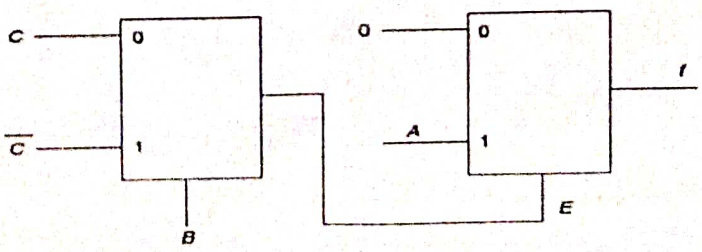
Q. 3

(a) Minimize the function using K-Map $f(A,B,C,D)=\Sigma m(0,1,2,3,5,7,9,10,11,13,15)$ 5

(b) Take your roll number and write it in the 4-variable SOP function (for eg. If roll no is 201411012 the SOP function will be $f(A,B,C,D)=\Sigma m(2, 0, 1, 4, 1, 1, 0, 1, 2)= \Sigma m(0, 1, 2, 4)$. And also take don't care conditions for 10, 11, 12, 13, 14, 15. Now make its 4-variable K-map. And implement it using basic Gates only. 5

Q. 4

(a) Find the output f of the following circuit. 5



(b) Consider the two cascaded 2-to-1 multiplexers as shown in the 5

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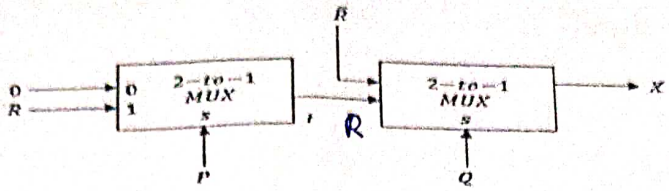
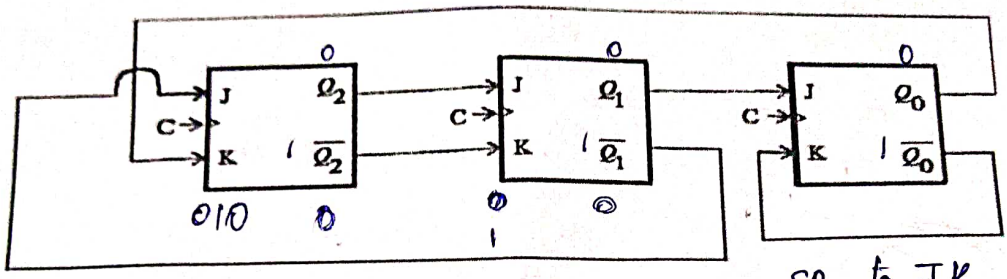
figure.The minimal sum of products form of the output X is ?



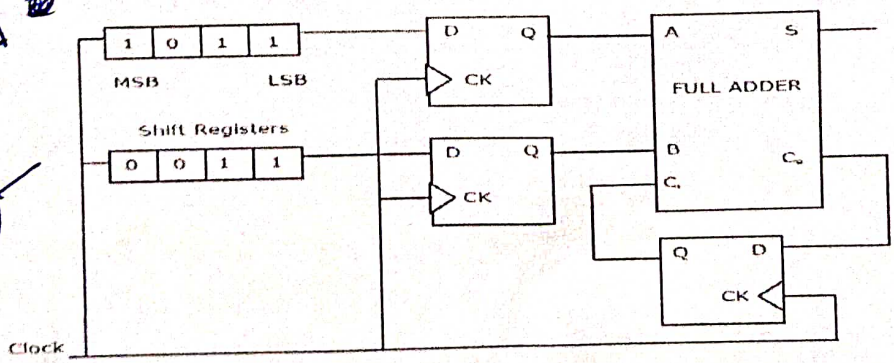
Q.5 (a) The below sequential circuit is design using JK flip-flops is initialized with Q2 Q1 Q0 = 000. The state sequence for this circuit for the next 5th clock cycle is? 5



(b) Convert the S-R flip flop using J-K flip flop.

Q. 6 (a) Design a circuit that accept binary numbers between 1 & 5 and generates an output, equals to the numbers of 1's in the input. Use only 2-input logic gates for implementation. **(5 Marks)**

(b) The circuit shown in figure below, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in clear state. After applying two clock pulses, find out the outputs of the full-adder S and C0. **(5 Marks)**



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