Indian Institute of Information Technology – Vadodara
Mid-Semester Examination Winter 2022-23
B. Tech. (IT & CSE)
CS-208: Computer Organization & Architecture

Time: 2:0 hrs. Max. Marks: 50

Attempt all questions. Follow the instructions as circulated via email.

Q. 1 Do the followings

a) Consider a 5-stage pipeline with segment delay of segment as 14ns, 20ns, 21ns, 22ns & 19ns. Calculate the speedup of pipeline as compared to corresponding non-pipeline system for 200 input. 10

b) The stage delay in 4-stage pipeline are 5ns,6ns,4ns, 5ns.The 2nd stage (with delay 6ns) is replaced with functionally equivalent design involving two stages with respective delay 4ns,3ns. The throughput increase of the pipeline is ..... %

c) Consider a 5- stage pipeline with cycle time of 20ns. Calculate processing time of the pipeline of 200 tasks.

d) A four-stage pipeline has stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to process 1000 data items on the pipeline will be

e) Multiply -9 x -13 using Booth Algorithm.

Q. 2 10

a) A processor X1 operating at 2 GHz has a standard 5-stage RISC instruction pipeline having a base CPI (cycles per instruction) of one without any pipeline hazards. For a given program P that has 30% branch instructions, control hazards incur 2 cycles stall for every branch. A new version of the processor X2 operating at the same clock frequency has an additional branch predictor unit (BPU) that completely eliminates stalls for correctly predicted branches. There is neither any savings nor any additional stalls for wrong predictions. There are no structural hazards and data hazards for X1 and X2. If the BPU has a prediction accuracy of 90%, the speed up (rounded off to two decimal places) obtained by X2 over X1 in executing P is .....

b) The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write-back (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take three clock cycles each, 35 instructions take two clock cycles each, and the remaining 25 instructions take one clock cycle

each. Assume that there are no data hazards and no control hazards. The number of clock cycles required for completion of execution of the sequence of instruction ?

Q. 3 a) A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is ? 10

b) Consider a pipelined processor with 5 stages, Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and the register read is performed in the EX stage, The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies. Consider the following sequence of 8 instructions:
ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL
Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. Find the speed-up?

Q. 4 a) Consider a pipelined processor with the following four stages- 10

IF
ID & OPERAND
Fetch Execute (EX)
Write Back (WB)

The IF, ID & WB stages take one clock cycle each to complete the operation. The number of clock cycles for the execution state depends on the instruction. The ADD & SUB Instruction need 1 cycle and MUL Instruction needs 3 clock cycle in the execution state, Operand forwarding used in the pipelined processor. What is the number of clock cycles taken to compute the following Sequence of Instruction?

ADD R2 R1 R0
MUL R4 R3 R2
SUB R6 R5 R4

b) What are data hazards? explain elimination techniques with suitable examples?

Q. 5 a) Difference between PC relative and direct addressing mode. 10

b) Difference between stack based and accumulator based ISA.

**********End **********