Indian Institute of Information Technology Vadodara

CS/IT 429

Basics of Hardware Description Language (HDL)

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Verilog Hardware Description Language

Verilog was developed by Gateway Design Automation in 1984.

Verilog was inducted as the IEEE 1364 standard in 1995.

Verilog HDL is easy to learn and easy to use. It is similar to the C programming language.

Verilog HDL allows different levels of abstraction to be mixed in the same model.

Most popular logic synthesis tools support Verilog HDL.

Verilog is a case-sensitive language.

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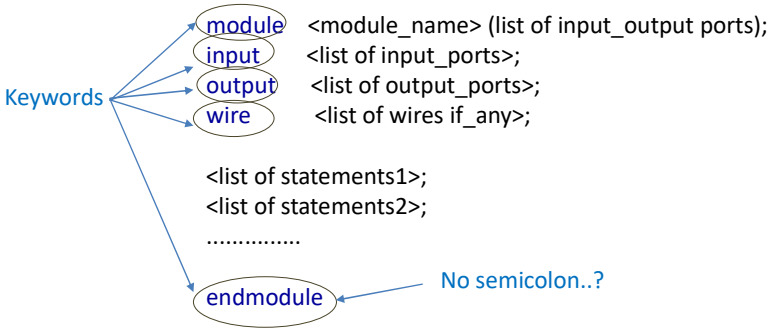
Anatomy of a Module in Verilog HDL



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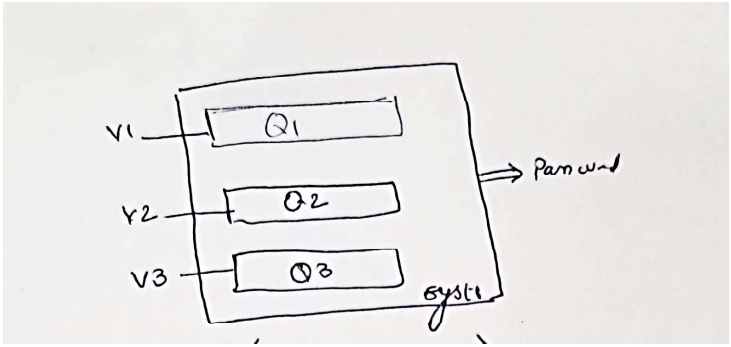
Implementation of a design at different levels of abstraction:

- Structural
- RTL/Data Flow
- Behavioral

Contd…

Implementation of a design at different levels of abstraction:

Example: Password Retrieval System



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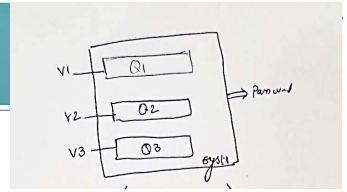
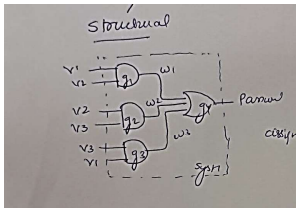


Example: Password Retrieval System

Structural

Schematic is known




```
module system1 (password, v1,v2,v3);
input v1,v2,v3;
output password;
wire w1, w2, w3;
and g1(w1,v1,v2), g2(w2,v2,v3),
      g3(w3, v3,v1);
or   g4(password,w1,w2,w3);
endmodule
```

RTL/Data Flow

Boolean Expression is known

```
module system1 (password, v1,v2,v3);
input v1,v2,v3;
output password;
assign password = (v1&v2) | (v2&v3) | (v3&v1);
endmodule
```

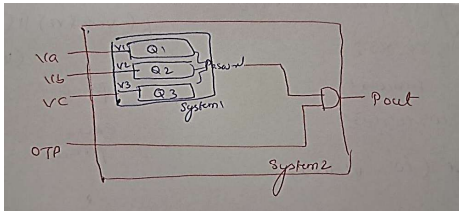
Behavioral

Functionality or logical statement is known

```
module system1 (password, v1,v2,v3);
input v1,v2,v3;
output reg password;
always@(v1,v2,v3);
if (v1&&v2) || (v2&&v3) || (v3&&v1);
password = 1;
else
password = 0;
endmodule
```


Contd…

Concept of Instantiation…

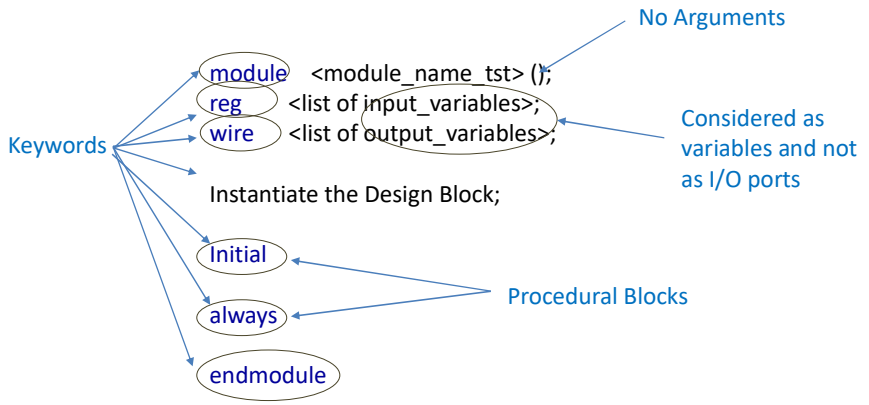



```
module system1 (password, v1,v2,v3);
input v1,v2,v3;
output password;
wire w1, w2, w3;
and g1(w1,v1,v2), g2(w2,v2,v3),
      g3(w3, v3,v1);
or   g4(password,w1,w2,w3);
endmodule
```

```
//Instantiating system1 in system2
module system2 (pout, va, vb, vc, OTP);
input va, vb, vc, OTP;
output pout;
wire password;
wire w1, w2, w3;
system1 s1(pout, va, vb, vc);
and   g5(pout, password, OTP);
endmodule
```


Test Bench

Anatomy of Test Bench



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Test Bench Application

- To check functionality of module (provide test values to the system).

- To generate signals.