# Embedded Microchannel Cooling for High Power-Density GaN-on-Si Power Integrated Circuits

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## ABSTRACT

In this work, we demonstrate a new thermal management approach for direct cooling of GaN-on-Si power integrated circuits (ICs), in which the Si substrate functions as a microfluidic heat sink, turning Si into a cost-effective, high thermal performance substrate. Flowing coolant through microchannels etched in the backside of the substrate enables a much denser integration of GaN power devices in a single chip. As a proof of concept, an integrated full-wave bridge rectifier (FWBR) was realized based on high-performance tri-anode GaN Schottky barrier diodes (SBDs), together with a novel hybrid printed circuit board (PCB) that provides fluidic and electric connections to the liquid-cooled power IC. A device-level heat flux of 417 W/cm$^2$ was cooled using only 60 mW of pumping power. Compared to natural-convection air-cooling, the temperature rise was reduced by 98% and the converter output power was increased by 30 times, up to 120 W, by eliminating self-heating degradation. The high cooling efficiency, large heat extraction capabilities and low-cost fabrication process of embedded microchannels on GaN-on-Si, in combination with new PCB-based coolant delivery, can be an enabling technology for the next generation of ultra-high power-density ICs.

**KEY WORDS:** microchannels, direct cooling, thermal management, Power IC

## NOMENCLATURE

| Variable | Description | unit |
|---|---|---|
| COP | Coefficient of performance | - |
| $f$ | Flow rate | ml/s |
| $h$ | Heat transfer coefficient | W/m$^2$K |
| $k$ | Thermal conductivity | W/mK |
| $\Delta p$ | Pressure drop | Pa |
| $P_{pump}$ | Pumping power | W |
| $q$ | Heat flux | W/m$^2$ |
| $Q$ | Power dissipation | W |
| $R$ | Thermal resistance | K/W |
| Re | Reynold's number | - |
| $\Delta T$ | Temperature rise | K |
| $v$ | Velocity | m/s |

## INTRODUCTION

Wide band-gap semiconductors, such as GaN and SiC, have the potential to dramatically reduce the footprint of power devices, such as transistors and diodes, due to their larger voltage blocking capabilities [1]. Ongoing developments in lateral GaN power devices, such as improved epi-layers, field plates and tri-gates, are resulting in reduced specific on-resistance for a given voltage rating [2], [3]. Especially with the introduction of new power transistors and diodes based on GaN superlattice heterostructures, recently proposed in the literature [4], [5], major improvements in the $V_{br}^2/R_{on}$ figure of merit has been realized. The subsequent reduction in device size in combination with the lateral nature of GaN power HEMTs enable monolithic integration of multiple components into compact power ICs with considerably lower parasitic inductance [6], thus allowing much higher frequency operation as well as high power density. These advances open doors to a future where a complete high power converter can be integrated on a single chip [7], [8], by following the same path that logic ICs have taken over the last six decades. However, such converters require orders of magnitude higher currents compared to logic ICs. In combination with the reduced die size and the higher level of integration, this results in a significantly higher heat flux, which ultimately degrades device performance due to self-heating, limiting miniaturization and integration of these power devices.

The absence of efficient and cost-effective thermal management solutions makes massive integration of high power devices unattainable. Current successful solutions for handling extreme heat fluxes in GaN devices, relying on high thermal conductivity substrates such as SiC (380 W/mK) and Diamond (2200 W/mK) [9], are prohibitively expensive (Table I), which prevents widespread adoption of this technology. The

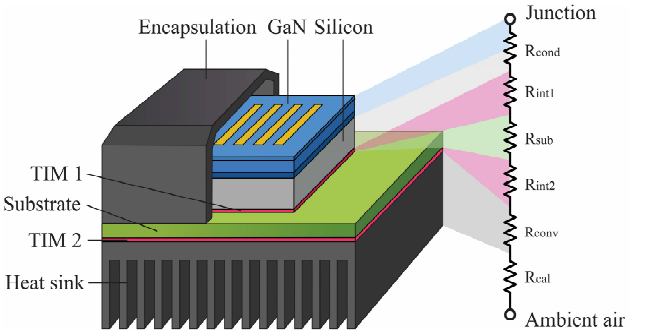



Fig. 1. Schematic illustration of an indirect cooling approach, where a chip is mounted on a PCB, and separated from a heat sink using a thermal interface material.

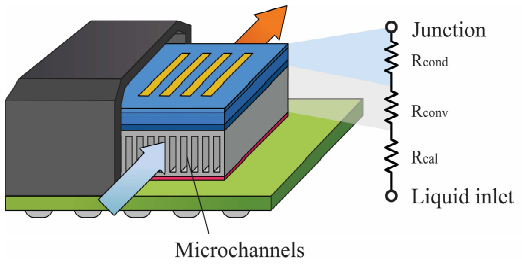



Fig. 2. Schematic illustration of a direct cooling approach, where the coolant flows in direct contact with the semiconductor die.

TABLE I
PROPERTIES OF NON-NATIVE SUBSTRATES FOR GAN ELECTRONICS

| *Substrate* | *k* [W/mk] | *Cost* [$/cm$^2$] |
|---|---|---|
| Si | 150 | $10^0$ |
| SiC | 380 | $10^1$ |
| Diamond | 2200 | $10^3$ |

silicon substrate has a significantly lower thermal conductivity (150 W/mK), but is orders of magnitude more cost effective. As such, most successfully commercialized GaN devices for power electronics applications have focused on using a silicon substrate [10]. Yet, the substrate provides no functionality to the electronic device, other than carrying the few micrometers of AlGaN/GaN epilayer that provides the active surface for the electronics.

In a conventional indirect cooling configuration (Fig. 1), the heat flux generated in the active layer propagates through multiple materials and interfaces before reaching the ambient air, resulting in a large thermal resistance. A more efficient structure has the heat sink directly embedded inside the chip, called direct cooling (Fig. 2), which removes most of the thermal resistance components. Direct cooling approached based on microchannels [11], [12], pin fins [13]–[15], impinging jets [16] and manifold microchannels [17]–[20] have been successfully demonstrated to very high heat fluxes, surpassing 1 kW/cm$^2$. The well-established, low-cost MEMS micro-fabrication processes developed for silicon can be used to turn the substrate into a high-performance liquid-cooled microchannel heat sink [21] with state-of-the art cooling capabilities.

The purpose of this work is to demonstrate a new thermal management approach for direct cooling of GaN-on-Si power ICs, where the Si substrate functions as a microchannel heat sink (Fig. 3(a)). This approach turns GaN-on-Si into a cost-effective, high thermal performance substrate, allowing a much denser integration of power devices in a single chip. As a proof of concept, we demonstrate the thermal and electrical performances of an integrated FWBR, based on high performance tri-anode GaN SBDs, with embedded microfluidic cooling, which is compared to conventional cooling methods. To showcase the feasibility of direct cooling on high power-density converters, this liquid-cooled power IC is integrated on a novel hybrid coolant-delivery PCB that provides both fluidic and electronic interconnection between the IC and the outside world, using easy-to-use fabrication methods.

## FABRICATION

This section describes the step-by-step procedures to fabricate a GaN-on-Si power IC with substrate-embedded microchannel heat sink, as well as the procedure to assemble a multi-layer PCB with embedded coolant delivery channels which was used to interface the power IC.

### Device fabrication

Tri-anode SBD FWBR were fabricated on an AlGaN/GaN-on-silicon wafer, according the process previously described in [22] and summarized in Fig. 3(b). The silicon substrate was 1 mm-thick, on which a 4.2 µm-thick buffer layer was epitaxially grown. The GaN channel was 420 nm thick, followed by a 20 nm AlGaN barrier and a 2.9 nm GaN cap layer. This structure results in a 2-dimensional electron gas (2-DEG), a high

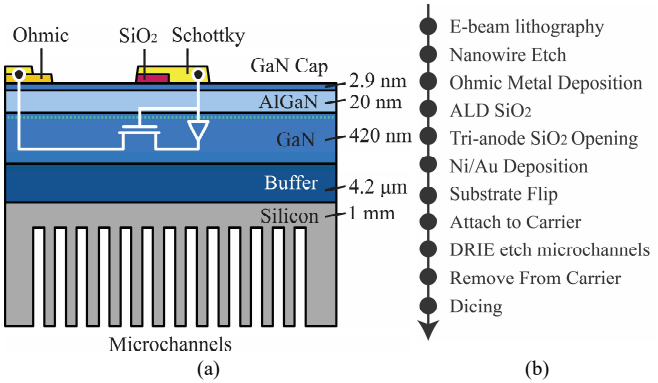



Fig. 3. (a) Schematic illustration of the liquid cooled power IC, where the silicon substrate functions as the cooling layer and the AlGaN/GaN epilayer provides the electronic properties. (b) Overview of the fabrication steps for the liquid-cooled GaN-on-Si power IC.

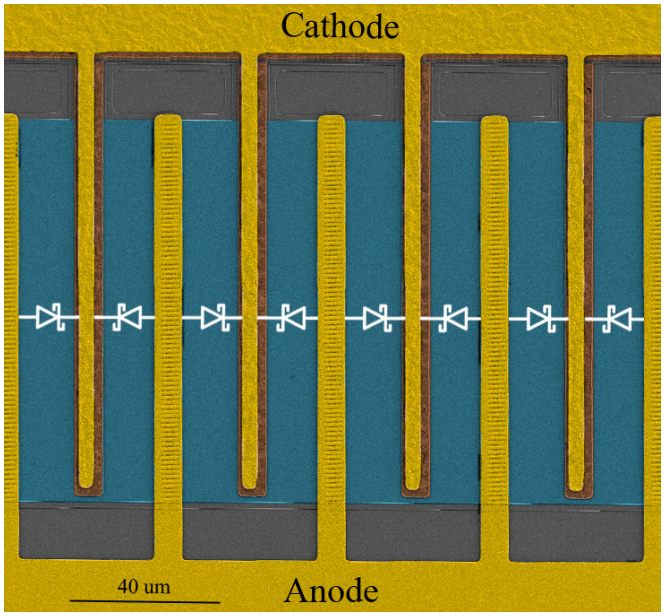



Fig. 4. SEM image of the fabricated GaN SBD. The area marked in yellow indicates the metallization of the anode and cathode region. The area marked in blue indicates the active area of the device where a 2DEG is present, and the area marked in brown indicates the annealed ohmic contact.

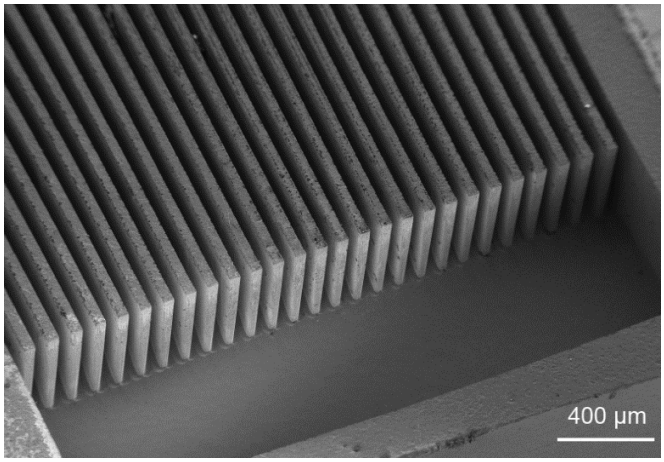



Fig. 5. High aspect ratio microchannels etched in the backside of the power IC.

concentration of electrons ($1.25 \cdot 10^{13} cm^{-2}$) with high mobility ($1700\ cm^2V^{-1}s^{-1}$) at the interface between AlGaN and GaN. A nanowire structure was realized in the anode region of the SBD in order to obtain high breakdown performance and to reduce turn-on voltage, as previously demonstrated in [22], [23]. The nanowires were patterned using E-beam lithography, to reach the desired nanowire width and spacing of respectively 200 nm and 100 nm, followed by an inductively coupled plasma (ICP) etching step. Next, a metal stack (Ti/Al/Ti/Ni/Au) was deposited onto the cathode region using e-beam physical vapor deposition (PVD), followed by an annealing step to form an ohmic contact. A $SiO_2$ dielectric layer was formed on the surface using atomic layer deposition (ALD), followed by an etching step to open the anode and cathode region. Finally, the SBD FWBR was finished by depositing a layer of Ni/Au on the anode region to form a Schottky contact, using PVD. Fig 4 shows a SEM image of a section of a single SBD, part of the FWBR, where the tri-anode and tri-gate regions can be observed on the active area of the anode pad as subtle lines.

The epilayer was coated with a photoresist as a protective layer, before flipping the substrate and temporarily bonding it to a carrier wafer. This enables the fabrication process on the silicon substrate. Microchannel structures with a channel width and spacing of 50 µm were patterned using optical lithography, followed by a deep reactive ion etching step (DRIE) to create high aspect ratio microchannels with a depth of 500 µm. Finally, the substrate was detached from the carrier wafer and diced into individual power ICs. Fig. 5 shows a SEM of the sharp sidewall profile of the microchannels etched in the back of the power IC, as well as the inlet cavity, which was 0.8 mm by 2.7 mm.

**PCB fabrication**

In order to deliver the coolant to the power IC, an interface is required between the small openings of the microchannels and the larger-diameter tubes that supplies the coolant. Multiple strategies have been proposed in the literature such as Poly(methyl methacrylate) (PMMA) or polycarbonate manifolds that can interface with the device, while fluidic connectors as well as sensors can be threaded into such manifolds [24]. However, since the objective is to maximize power density, these approaches add a large volume of unused material. To improve power density, a new approach was explored where the PCB was used to provide both electric and fluidic interface to the power IC. This was achieved by fabricating 3 separate PCBs, as shown in Fig. 6. The top PCB has two cavities that are aligned with the inlet and outlet cavities of the microchannels, with dimensions of 0.7 mm by 2.5 mm. This top PCB also contains the wire-bond pads to create an electrical connection with the device. Coolant inlet and outlet holes with a diameter of 9 mm are surrounded by an exposed soldering pad such that connectors can be soldered onto the PCB. The middle PCB provides 4 electrical input and output terminals, as well as a cutout that functions as a channel to guide the coolant to the chip. All parts of the PCB that are exposed to the coolant are gold-plated to prevent oxidation. The purpose of the bottom layer is to seal the coolant delivery channels in the middle PCB.

The three PCB are bonded together using laser-cut double-sided adhesive, as shown in Fig. 7. First, the PCBs were

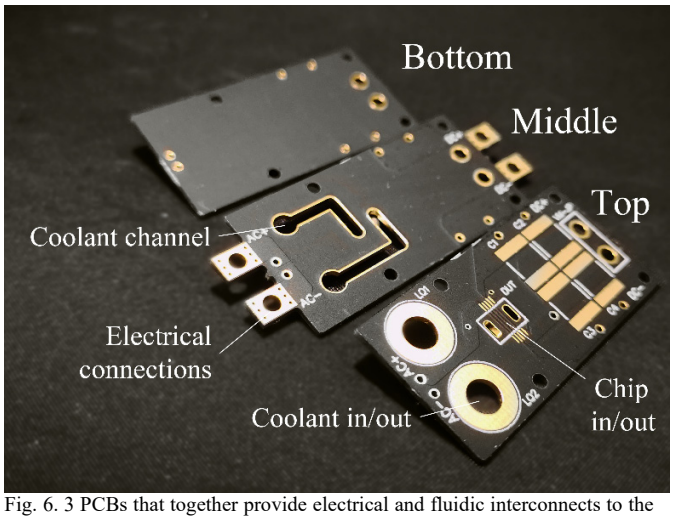


Fig. 6. 3 PCBs that together provide electrical and fluidic interconnects to the power IC

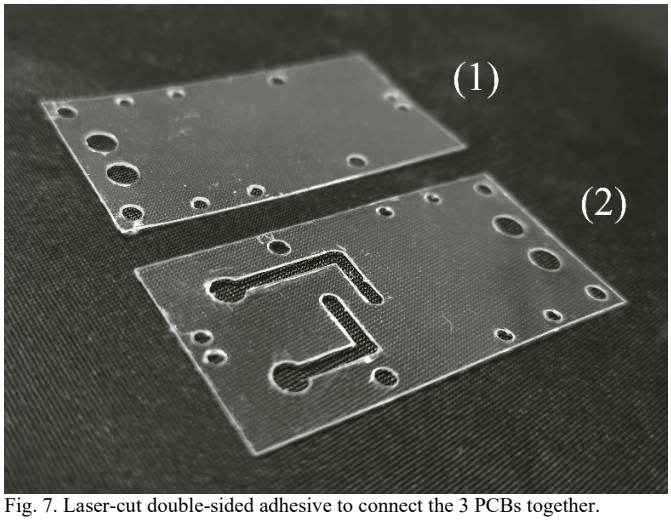


Fig. 7. Laser-cut double-sided adhesive to connect the 3 PCBs together.

thoroughly cleaned using IPA and fiber-free cloth, to ensure a good leak-tight bond. The selected adhesive (Adhesives Research ARseal 90880) can withstand temperatures up to 120°C, rapid thermal cycling and is resistant to dilute solutions of alcohols and organic solvents. After bonding the three layers, the assembly was put in a vice for 30 minutes to ensure a proper seal.

Finally, M3 female threads were soldered onto the inlet and outlet holes to attach barbed connectors, and output capacitors were mounted on the PCB to smoothen the output signal of the power device. Finally, the device was attached to the PCB using double-sided adhesive, and wire-bonded.

**EXPERIMENTAL SETUP**

The assembled power IC with PCB embedded cooling, as shown in Fig. 8, was experimentally evaluated using the setup shown in Fig. 9. The aim of this setup is to investigate the cooling performance of the microchannel heat sink. A regulated DC power supply (TTI QPX1200S) was connected to the diode bridge such that all diodes are conduction. This way, an equal distribution of losses can be generated over the 4 diodes during DC operation, and the amount of dissipated power can be accurately monitored. An open loop, single phase cooling

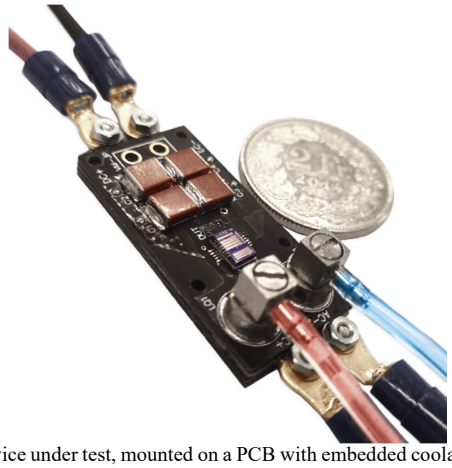


Fig. 8. Device under test, mounted on a PCB with embedded coolant delivery channels. False coloring on the inlet and outlet tubes indicate the cold coolant entering the PCB, and the hot coolant leaving the PCB.

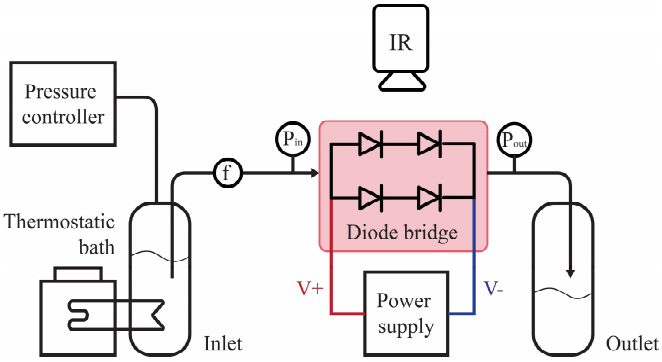



Fig. 9. Schematic illustration of the experimental setup for evaluating the liquid cooled power IC.

system was employed, using de-ionized (DI) water as a coolant. A pressure controller (Elveflow OB1 MK3) was used to pressurize the inlet reservoir of coolant, which was kept at a constant temperature using a thermostatic bath (LAUDA Proline RP845). By pressurizing the inlet reservoir, coolant starts flowing through the PCB, after passing a flowmeter and pressure sensor at the inlet. An infrared (IR) microscope with high resolution (QFI InfraScope) was used to map the temperature profile at the surface of the chip during operation. The power IC was coated with black spray paint to increase emmisivity, and pixel-by-pixel emissivity correction was applied to ensure accurate temperature readings.

## RESULTS AND DISCUSSION

The GaN-on-Si power IC with substrate-embedded microchannel heat sink was hydraulically and thermally evaluated to assess its performance. The results are discussed in this section, and compared to the literature.

TABLE II
MEASUREMENT CONDITIONS AND RESULTS

| $f$ [ml/s] | $v$ [m/s] | $Re$ [-] | $R_{th}$ [K/W] | $\Delta p$ [mbar] | $Q_{max}$ [W] | $P_{pump}$ [mW] | $COP_{60}$ [-] |
|---|---|---|---|---|---|---|---|
| 0.08 | 0.11 | 10 | 4.9 | 32 | 12.2 | 0.26 | 57991 |
| 0.14 | 0.20 | 18 | 3.5 | 73.2 | 17.1 | 1.0 | 19619 |
| 0.30 | 0.43 | 39 | 2.8 | 181 | 21.4 | 5.4 | 4937 |
| 0.52 | 0.74 | 67 | 2.6 | 360 | 23.1 | 19 | 1613 |
| 0.83 | 1.19 | 108 | 2.4 | 733 | 25 | 61 | 537 |

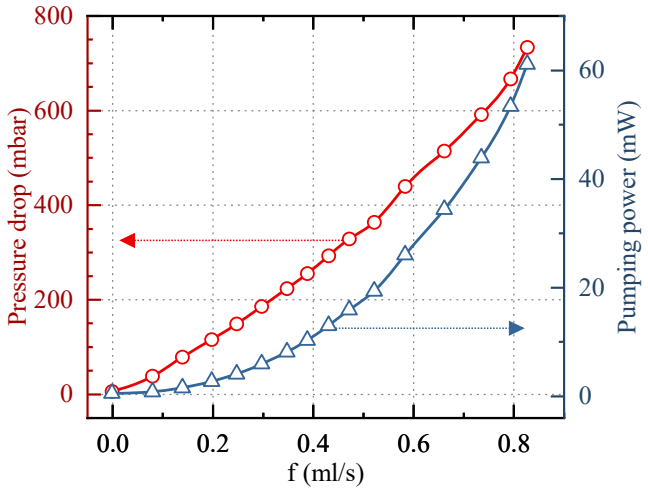



Fig. 10. Pressure drop (left) and pumping power (right) for flow rates up to 0.83 ml/s.

### Pressure drop and pumping power

A range of flow rates from 0.08 ml/s to 0.83 ml/s was experimentally evaluated. Given the dimensions of the microchannels of 50 µm x 500 µm, and a total of 28 parallel channels, this corresponds to an average velocity between 0.11 m/s and 1.19 m/s in the microchannels. These results are summarized in Table II. The hydraulic diameter of the microchannels was 91 µm. Therefore, this range of flow-rates corresponds to a Reynold's number from 10 to 108, well within the limits of laminar flow. The pressure drop increased linearly from 32 mbar at 0.08 ml/s to 733 mbar at 0.83 ml/s, as shown in Fig. 10. These values corresponds to a hydraulic resistance of $8.7 \pm 33 \cdot 10^{10}$ Pa·s·m$^{-3}$. Ideal pumping power was calculated using (1), the product of flow rate and pressure drop, and is shown in Fig. 10, as well as summarized in Table II. To achieve the maximum flow rate of 0.83 ml/s, only 61 mW of pumping power was required, a value that is easily attainable using small-sized micropumps.

$$P_{pump} = f\Delta p \qquad (1)$$

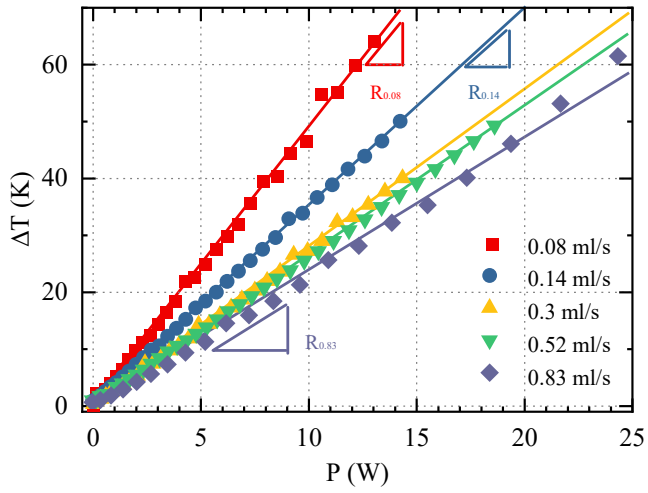



Fig. 11. Surface temperature rise versus power dissipation for flow rates between 0.08 and 0.83 ml/s. Slopes of the linear fit through the data points indicate the thermal resistance at a given flow rate.

**Temperature rise and thermal resistance**

For each condition of flow-rate, the DC power dissipation on the power IC was gradually increased until the surface temperature rise, monitored using the calibrated IR camera, reached a value of 60 K. Surface temperature rise versus power dissipation for varying flow rates is shown in Fig. 11. At a flow rate of 0.83 ml/s, up to 25 W of losses were extracted from the 2.7x3.0 mm$^2$ IC, corresponding to a device-level heat flux of 417 W/cm$^2$, far beyond the capabilities of conventional indirect cooling methods. The surface temperature rise shows a linear relation versus power dissipation, and the slope of the linear fit through these data points yields the thermal resistance at a specific flow rate condition.

The obtained thermal resistance versus inverse flow rate is plotted in Fig. 12, demonstrating a clear linear relationship, defined by the caloric thermal resistance ($R_{cal}$) of the coolant, which here was de-ionized water. The intercept with the y-axis indicates the thermal resistance at infinite flow rate, when $R_{cal}$ approaches zero, which is approximately 2 K/W. This remaining part of the thermal resistance can be accounted to the convective heat transfer between the microchannel wall and the coolant ($R_{conv}$) and to the conductive thermal resistance between the junction and the microchannels ($R_{cond}$). Using (2), an expression for the conductive thermal resistance, under the assumption of 1D heat transfer over a distance of 750 µm, shows that the contribution of $R_{cond}$ is approximately 0.62 K/W. As a result, the remaining 1.4 K/W can be accounted to the convective thermal resistance, as defined in (3). The additional temperature rise because of the thermal boundary resistance was neglected, since based on values form the literature ($10^{-7}$ m$^2$K/W [25]–[27]), this would cause contribute 0.012 K/W to the total thermal resistance. Because of the low Reynolds number (Table II) and the small channel dimensions, the majority of the flow is thermally fully developed. As a result, $R_{conv}$ was not expected to depend strongly on flow rate.

$$R_{cond} = \frac{t}{kA} \qquad (2)$$

$$R_{conv} = \frac{1}{hA} \qquad (3)$$

Using the footprint of the microchannels (2.7x3.0 mm$^2$), this leads to an effective heat transfer coefficient of $h_{eff}$ = 8.8·10$^4$ WK$^{-1}$m$^{-2}$. If the complete surface area of the walls of the microchannels is considered, this leads to an average wall heat transfer coefficient of $h_{wall}$ = 8.0·10$^3$ WK$^{-1}$m$^{-2}$. Although this value is lower than the local heat transfer coefficient expected in typical laminar flow microchannel cooling applications, due to the fact that the limited fin efficiency lowers the effective heat transfer coefficient in high aspect ratio microchannels, it is significantly higher than any heat transfer coefficient that could be obtained using air-cooling or millimeter-sized liquid cooling solutions.

**Cooling coefficient of performance**

The low pumping power in combination with a low thermal resistance leads to high performance cooling of high heat fluxes. The coefficient of performance (COP), given in (4), gives the ratio of heat load that can be applied before reaching a critical surface temperature rise (60 K in this case), to the amount of pumping power required to achieve this level of cooling. Fig. 13 shows the COP versus heat flux. As can be seen, COP decreases rapidly with increasing heat flux. This is due to the fact that $P_{pump}$ scales with $f^2$, whereas $Q_{max}$ only scales with $f^1$. It is therefore required to assess COP at multiple measurement conditions, as efficiency depends on the given flow-rate.

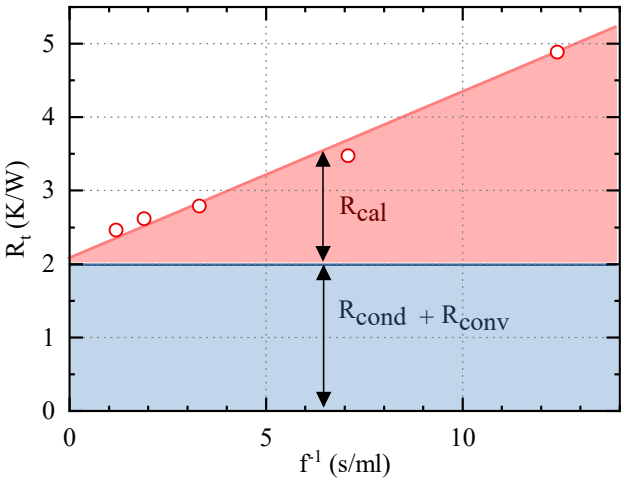



Fig. 12. Thermal resistance versus inverse flow rate. The area marked in red indicates the contribution of the heating of the coolant ($R_{cal}$) on the total thermal resistance, which scales with $f^{-1}$. The area marked in blue indicates the remaining contribution to the thermal resistance due to conductive and convective heat transfer between the junction and the coolant.

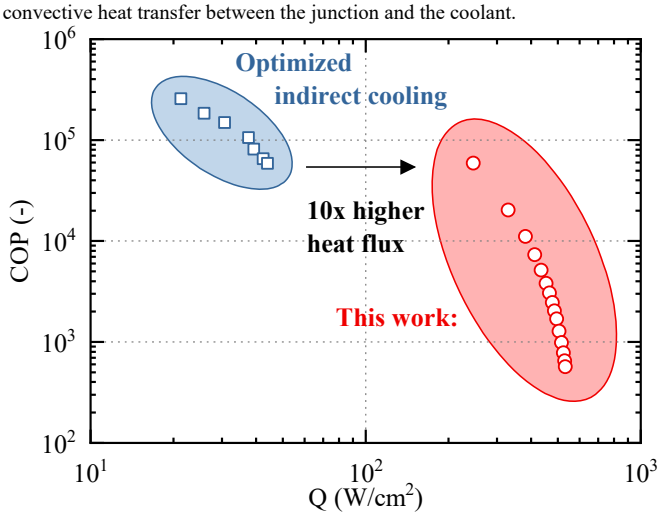
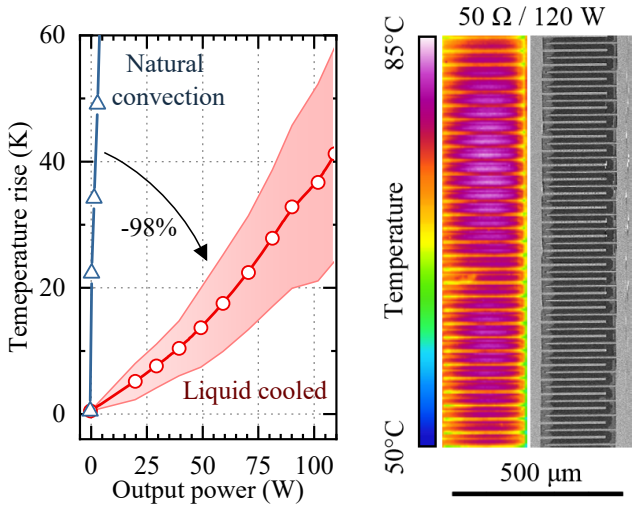



Fig. 13. Coefficient of performance versus maximum heat flux, for a device surface temperature rise of 60 K. Round markers indicate the results presented in this paper, whereas square markers refer to optimized indirect microchannel cooling of GaN power devices, as presented in [28].

$$COP_{60} = \frac{Q_{max}}{P_{pump}} = \frac{60}{f\Delta p R_t} \qquad (4)$$

Fig. 13 also shows data points from a work in the literature that utilized similar 50 µm-wide silicon microchannel cold-plates in an indirect cooling configuration, separated from a GaN transistor using a thermal interface material [28]. The direct cooling approach allows approximately 10x higher heat fluxes, due to the absence of interface thermal resistance and the typical junction-to-case thermal resistance in a packaged device. This clearly highlights the benefits in power density that




(a) (b)

Fig. 14. (a) Maximum surface temperature rise versus output power of the rectifier with substrate-embedded cooling, indicated in red, and an identical device depending solely on natural-convection air-cooling (blue). (b) IR thermograph of the surface of a single diode during 120 W rectification (left), SEM image of the same diode, showing the anode and cathode finger structure (right)

can be achieved by using the silicon substrate as a microchannel heat sink.

### High power rectification

To demonstrate the improved power conversion capabilities of the liquid cooled power IC, an AC waveform up to 125 V was fed into the FWBR at 10 kHz and rectified into a DC output voltage. The surface temperature rise of the liquid cooled converter was compared to the same setup without the presence of liquid cooling, thus depending solely on natural convection. Fig. 14(a) shows the temperature rise of the surface of the chip versus output power of the rectifier. As can be seen, up to 120 W of DC output power could be delivered from the FWBR with substrate-embedded microchannel cooling before reaching a peak temperature of 60 K.

The spread in Fig. 14(a) represents the range of temperatures measured over the entire diode, as shown in Fig. 14(b). Fig 14(b) shows an SEM image of a single diode, and the corresponding IR temperature map. The markers thus represent the mean value, whereas the outer lines represent the minimum and maximum observed temperatures. The FWBR cooled by natural convection shows a significant higher surface temperature rise: Only 4 W of DC output power could be delivered before reaching the same temperature rise of 60 K. By employing substrate-embedded microchannel cooling, a reduction of 98% in thermal resistance was observed, a promising result for the future of highly miniaturized integrated power converters.

## SUMMARY & CONCLUSIONS

In this work, the concept of substrate-embedded microchannel cooling of GaN-on-Si power ICs was demonstrated for the first time. Total device-level heat fluxes of up to 417 W/cm$^2$ were obtained, with a maximum surface temperature rise 60 K. These results show that an order of magnitude higher heat fluxes can be achieved by embedding the cooling directly into the semiconductor die. Furthermore, a new approach of utilizing the PCB as coolant delivery platform was presented as a very compact and low-cost approach to prototype direct-cooled devices. This embedded cooling approach, in combination with the realized GaN power IC, resulted in a 30 times increase of output power. These results demonstrate the potential to realize high-power (kW-range) converters of the size of a USB-stick in the foreseeable future.

### Acknowledgements

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