Hotspot-Limited Microprocessors: Direct Temperature and Power Distribution Measurements

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***Abstract*—An experimental technique is presented, which allows for spatially-resolved imaging of microprocessor power (SIMP). In a first step this method utilizes infrared (IR) thermal imaging, while the processor is effectively cooled using an IR-transparent heat sink. In the second step the underlying power distribution is derived by determining the temperature fields for each individual power source on the chip. The measured chip temperature distribution is represented as a superposition of these temperature fields. The SIMP data reveals *significant* temporal and spatial variations of the microprocessor power/temperature distribution, which can be attributed to the circuit layout as well as to the varying utilization levels across the processor while running full workloads. In this paper we have applied the SIMP method to the dual core PowerPC™970MP microprocessor to measure detailed temperature and power distributions under full operating conditions. In the first part of the paper the impact of power and temperature limitations of high performance CMOS chips is discussed in detail, where we distinguish between hotspot-limited (or temperature-limited) and power-limited chips. The discussion shows the importance of temperature and power distributions for chip floor planning, layout, design and architecture. Second, we present the experimental details of the SIMP method, which is applied to the dual core PowerPC970MP to directly measure the temperature and power fields as a function of workload and frequency. A pronounced movement of the hotspot location is observed. Finally, the hotspot of a competitive microprocessor is compared by measuring temperature efficiencies (temperature increase/performance) for the same workloads and cooling conditions.**

***Index Terms*—Cooling, integrated circuit design, integrated circuit layout, microprocessor testing.**

I. Introduction: Power- and Hotspot-Limited Chips

IT IS WELL KNOWN that excessive power dissipation of state-of-the-art CMOS chips has emerged as a major design constraint [1]–[3]. This phenomenon is commonly referred to as the "power limit" or "power wall," which limits the maximum achievable performance of the digital circuitry. Specifically, a typical CMOS manufacturing line yields a variation of chips with a range of effective gate lengths. Shorter effective gate length translates into faster and higher performing chips while longer effective gate lengths result in slower chips. These different chips are "binned" into different buckets and then sold and marketed accordingly. However, the power consumption increases quite drastically with decreasing gate length, mostly because of increasing source-drain leakage. Because the chip power dissipation cannot be infinite, the power wall limits the performance of the fastest chips by impacting the actual yield for the highest performing chips, which typically account for the largest profits.

In the following, we investigate in more detail this "power wall" or "power limit" by referring to the (steady state) Fourier heat conduction equation, which relates generally the (volumetric) power distribution $(P(x,y,z))$ to the temperature distribution $(T(x,y,z))$ via the thermal package parameters $(k(x,y,z))$:

$$\nabla\left(-k(x,y,z)\nabla T(x,y,z)\right) - P(x,y,z) = 0. \qquad (1)$$

In this equation, the spatial variations of heat flow are described as diffusion process while taking energy conservation into account (net heat flow into an element of the system minus net heat flow out of an element of the system equals the change in energy of the element) [4]. As it is evident from (1), the mean chip temperature is given by the total chip power, but the actual *hotspot temperature* is determined by the *power distribution* (rather than the total dissipated power) on the chip. In other words, it is physically possible that a lower power chip can have a more severe hotspot problem than a higher power chip. With this in mind it is useful to distinguish between two general classes of chips, for which the "power wall" has quite different consequences: 1) *power-limited* chips which are constrained by the power supply such as battery lifetime or current limitations in the interconnects and 2) *hotspot-limited* chips, which are constrained by reliability and cooling capacity. Realistically, most chips fall between these two cases but this distinction is useful for discussion purposes. In order to clarify the terminology used throughout this paper, we note that a hotspot-limited chip is solely constrained by the junction peak temperatures (independent of the total chip power consumption) while a power-limited chip is only limited by the total chip power (regardless of the junction temperatures). In the following, we have a closer look at the limitations for hotspot-limited chips, which are set by reliability and cooling capacity.

Excessive chip temperatures can have a severe impact on failure mechanisms such as electromigration, stress migration and time-dependent dielectric breakdown, all of which are *exponentially* dependent on the chip temperatures. This reliability problem is further aggravated by the general scaling trend, which has led to a higher transistor density on a chip

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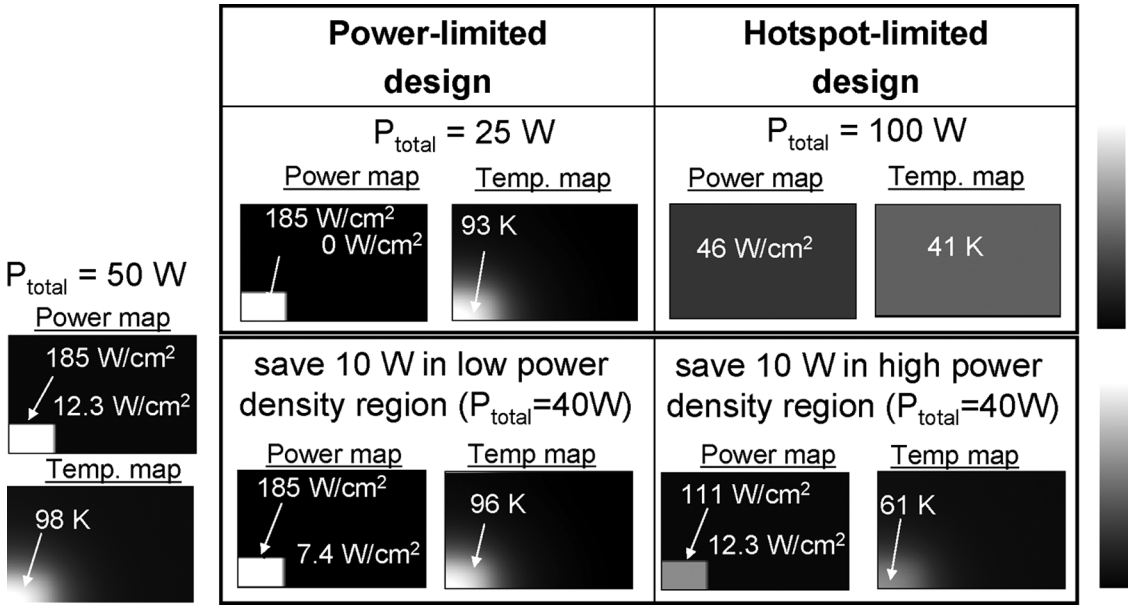

Fig. 1. Example chip power and temperature distribution of different chips, which demonstrate that a power-limited chip should have different design priorities than a hotspot-limited chip. In the upper table, a (25 W) power-limited designed chip is compared to a (100 W) hotspot-limited designed chip. In the lower table, we show the temperature fields for 10 W of power reduction in the lower versus higher power density regions for a (50 W) chip, which is shown on the left next to the table.

(more transistors translates into higher chip-level failure rates), exploding power densities and smaller, even more fragile devices [5].

Naturally, the cooling solution is a very critical component to manage chip temperatures. However, it is important to note that high-end cooling solutions are 1) typically expensive and 2) nonscalable. In fact, cooling technologies have *not* been able to keep up with the increased power dissipation at a given cost. While air cooling can be pushed to ~ 150 W/cm^2 (average) and maybe slightly higher with additional improvements, the introduction of liquid cooling will cause a major cost jump. Traditionally, chip-level cooling solutions were only a small fraction of the total system cost but, recently these expenses have started to become considerably more significant. For example, it is reported that the chip-level cooling solution beyond 60 W will cost $\sim$ \$3.5 per Watt, which excludes further system and datacenter cooling expenses (which can be even higher [6], [7]). Although cooling costs may be lowered by technology advancements, it is clear that package and cooling expenses are starting to have a severe impact on total system costs.

Cooling solutions are generally not scalable. Specifically, it seems to be very difficult to envision (cost effective) solutions, which will be able to handle heat loads in the excess of 750 W/cm^2 (which is close to the upper limit of advanced water cooling solutions). With the current projections of increasing power densities [8], the industry could face a very critical barrier in only a few years, even if additional costs could be absorbed or mitigated through new technologies and innovations.

It is very important to realize that the "power wall" has quite different consequences for the design whether a chip is hotspot- or power-limited. For a power-limited chip, one of the major design considerations is the reduction of total power in the chip. On the other hand however, the details of the power distribution is a second order concern and only to an extent, where excessive temperatures on the die increase the leakage power disproportionately. In contrast, for a hotspot-limited chip the designer is paying a lot of attention to the actual power distribution across the chip in order to minimize the peak junction temperatures. In other words, the difference in the design priorities for a hotspot- or power-limited chip is directly related to the level of granularity of the power, which is considered during chip design. For a power-limited chip, the power granularity equals one while for a hotspot-limited chip the power granularity is larger than one. The minimum required granularity for a hotspot-limited chip is determined by the package parameters, which is discussed in detail elsewhere [9]

Fig. 1 shows examples of different chips of the same die size which demonstrate clearly that a power-limited chip should have very different design priorities than a hotspot-limited chip. The left and right columns in the table of Fig. 1 refer to a power-limited and a hot-spot limited design, respectively. The die size of these illustrative example chips are 18×12 mm^2 and a standard cooling package is assumed [9]. As a first example, the power map with the corresponding temperature distribution for a 25 W (total power) chip is shown in the left column, second row. In this example, the chip has been designed solely with the goal to reduce the total power, but little attention has been paid to the power distribution and thus all the power is concentrated in a small region (i.e., 25 W in 4.5×3 mm^2) of the chip, which could be a high performance microprocessor core. As a result of the high local power density (i.e., 185 W/cm^2), the temperature increase is substantial ($T_{\mathrm{jmax}} \sim 93$ K above room temperature). By way of comparison, one could think about another chip, which has been designed considering the impact of the power distribution rather than the total power. In the right column, second row, the power and temperature distribution of

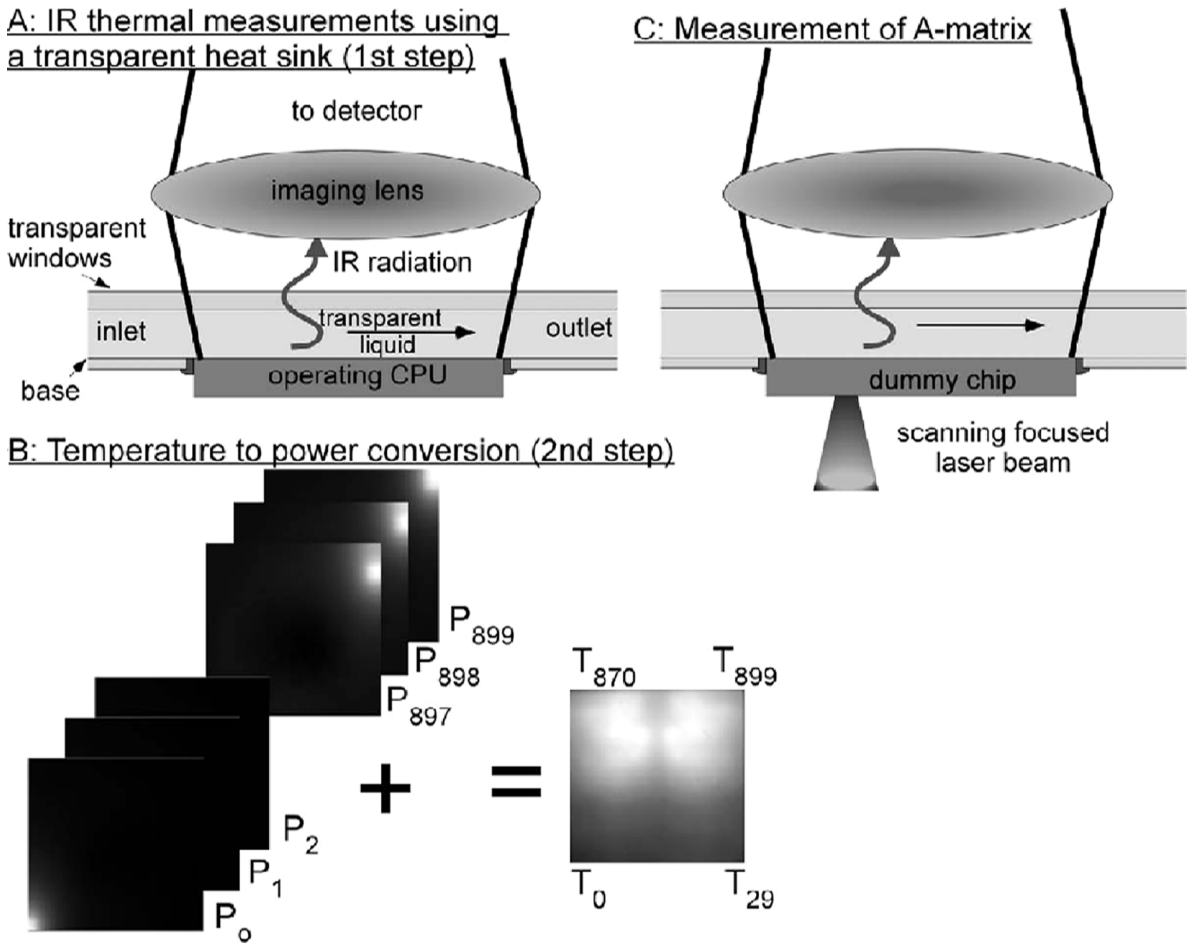

Fig. 2. The SIMP technique. (a) IR thermal measurements using a transparent heat sink (first step). (b) Temperature to power conversion (second step), where the measured chip temperature field is represented as a superposition of the temperature fields for each individual power source. (c) Method for measuring the temperature to power conversion matrix, where a scanning laser beam is focused onto the circuitry side of a dummychip mimicking the individual power sources while the temperature fields for each source are measured.

a 100 W chip is shown, where the power has been uniformly distributed across the chip (46 W/cm^2). Although this 100 W chip has 4$\times$ the power consumption than the previous example chip, it has only half of the hotspot temperature. Clearly, a lower power chip can have more of a hotspot problem than a higher power chip.

Another, more realistic, example is given to the left of the table, which shows the power and temperature distribution of a 50 W chip. This chip has a high power density region (185 W/cm^2 over 4.5 $\times$ 3 mm^2) in the corner, which could be a core and a lower power density region (21 W/cm^2) in the rest of the chip, which could be caches. As it will be shown further below by the experimental data, such a power and temperature distribution is quite typical. The hotspot temperature for this example is 98 K above room temperature. In the following, we discuss the application of power saving techniques such as clock and power gating for a power-limited and hotspot-limited design, respectively. For the power-limited design, it is irrelevant which region of the chip is targeted by the power saving techniques. For example, the result of 10 W power reduction in the low power density region (from 21 W/cm^2 now to 12 W/cm^2) is shown in the left column, third row. Interestingly, although the total power was reduced by 20%, the peak temperatures are only affected by 2%. On the other hand, for a hotspot-limited chip the designer manages to save 10 W of power in the high power density region (because the design distributes the power more evenly), the temperature reduction is substantial as illustrated in the right column, third row.

Although the previous discussion has shown that chip power distributions can be very important—especially if the chip is hotspot-limited—little information about these power distributions is actually available. Currently, one relies on chip power models with various underlying assumptions, which allocate certain amount of power levels over the different units of circuitry based on the chip architecture and processor design [10], [11]. The total chip power can be compared to measurements once hardware is available. Thermal sensors can be used to verify the temperature predictions which are based on these predicted power maps, although the numbers of on-chip thermal sensors is always limited. Generally, power models have not been validated. Furthermore, because power map predictions are lengthy and cumbersome, it is almost impossible to model the respective power distributions for a larger range of realistic workloads (with operating system, etc.), which more accurately represent the actual power distribution during normal operation.

In this paper, we use the SIMP (spatially-resolved imaging of microprocessor power) technique to measure detailed temperature and power distributions of dual core PowerPC970MP for different workloads, voltages and frequencies. A pronounced movement of the hotspot location can be observed for different workloads, which has naturally important consequences for thermal and power management schemes. Finally, we compare competitive microprocessors by measuring directly temperature efficiencies (temperature increase/performance) for the same workload and cooling conditions.

II. Spatially-Resolved Imaging of Microprocessor Power (SIMP)

A. First Step: IR Thermal Measurements Using a Transparent Heat Sink

In order to gain deeper insights into the power and temperature distributions of a fully operational microprocessor, a simple experimental technique was developed, which allows spatially resolved imaging of microprocessor power (SIMP) [12]–[19]. We describe here the details of the SIMP method, which comprises two steps. The first step involves infrared (IR) thermal measurements, while in the second step, the measured temperature fields are de-convoluted to yield the corresponding power distributions. The first step of this technique is illustrated in Fig. 2(a), which shows a microprocessor cooled by a specifically developed transparent heat sink. While the heat sink cools the chip, the temperature-dependent IR emission from the chip is measured.

In order to determine the chip's thermal distribution using IR thermal imaging, a method for cooling is required which allows removing the heat effectively at high cooling rates ($>$ 1 W/cm^{2}K) while being able to simultaneously monitor the temperature distributions. Previous attempts [12], [13] relied on an IR-transparent diamond heat spreader, but the actual cooling rates of this heat sink are typically not sufficient for high power, state of the art microprocessors running full workloads. In addition, this diamond heat spreader involves an interface between the Si chip and the heat spreader, which is naturally difficult to control. In this work, we have implemented an IR-transparent heat sink, which is based on a micro-duct so that an IR-transparent liquid can be flown directly over the chip. As shown in Fig. 2(a), an IR-transparent window is mounted on top of a base plate forming a micro-duct. The duct heights are typically between 0.5 and 2.5 mm.

The temperature dependent blackbody IR radiation is picked up with an imaging lens and projected onto a cooled 500×500 InSb array detector. The spatial resolution of the IR setup can range from 120 μm down to 3 μm depending on the imaging lens. Typically, the backside of the Si die is coated to obtain constant emissivity across the die, which simplifies the conversion from the measured IR signals into actual temperatures. In order to limit the spreading of the heat in the microprocessor die and to enhance the spatial resolution of the temperature image, the microprocessor die is thinned to typically $\sim$100 μm thickness.

The heat removal rates of the IR-transparent sink can be readily adjusted by changing the flow speed, the choice of the IR-transparent liquid and the duct height, thereby emulating different cooling/package conditions and triggering power and thermal management schemes. The range of accessible heat removal rates with this transparent heat sink covers state-of-the-art product cooling solutions as well as future cooling solutions (up to $\sim$ 4 W/cm^{2}K). The ability to realize high heat removal rates is very important because it not only enables measurements of state-of-the-art processors under the specified conditions (right frequencies, temperatures, voltages, workloads) and to mimic the correct transient thermal response, but also limits the thermal spreading of the heat throughout the die (potentially washing out the spatial resolution and thermal contrast during the measurements).

B. Second Step: Temperature to Power Conversion

While the first step of the SIMP technique involves IR thermal measurements of the microprocessor temperature distribution, in the second step, the measured temperature field is de-convolved to obtain the underlying power map. The general concept of this conversion is very simple and based on the fact that the measured chip thermal distributions can be represented as the sum of the individual temperature fields of each individual power source. This concept is illustrated in Fig. 2(b) for a 30×30 power and temperature map. More specifically, the (steady state) chip temperatures are given by

$$\begin{pmatrix} a_{00,00} & a_{00,01} & \cdots & a_{00,n} \\ a_{01,00} & a_{01,01} & & a_{01,n} \\ \vdots & \vdots & & \vdots \\ a_{n,00} & a_{n,01} & \cdots & a_{n,n} \end{pmatrix} \cdot \begin{pmatrix} P_{00} \\ P_{01} \\ \vdots \\ P_n \end{pmatrix} = \begin{pmatrix} T_{00} \\ T_{01} \\ \vdots \\ T_n \end{pmatrix} \quad (2)$$

or

$$\underline{\underline{A}} \cdot \underline{P} = \underline{T} \quad (3)$$

where $\underline{\underline{A}}$ is a thermal resistance matrix, $\underline{P}$ a power vector on circuitry level, $\underline{T}$ a temperature vector for each cell at the die's backside, and n are the numbers of cells (to represent the chip and power maps). The coefficients of the A-matrix are thermal resistances (e.g., in units of K/W). For example, $a_{31,52}$ represents the temperature increase in cell 31 for one unit of power in cell 52, while $a_{12,06}$ is the temperature increase in cell 12 if one unit of power is applied to cell 6.

The A-matrix itself has to be either calculated (e.g., using computational fluid dynamics (CFD) simulations) or measured. Specifically for the measurements, power sources in form of a scan-able focused laser beam are applied to a dummy chip. The chip is cooled under the same conditions as in the actual experiments in the first step of the SIMP technique while the resulting temperature fields are measured. Fig. 2(c) illustrates this experimental approach to determine the A-matrix, where a laser mimics individual power sources of the processor (the absorption depth in Si is less than 1 μm). The spot size of the laser (YAG @ 532 nm) can be readily tuned by the optics and is measured independently by a calibrated CCD camera. In our setup, we have automated the scanning by using a pair of galvo-directing mirrors. Because the absorbed laser power is constant during the A-matrix measurements (as monitored via the back reflection of the laser from the die) and the total chip power is known from electrical measurements (during the first step of the SIMP technique), the exact amount of absorbed laser

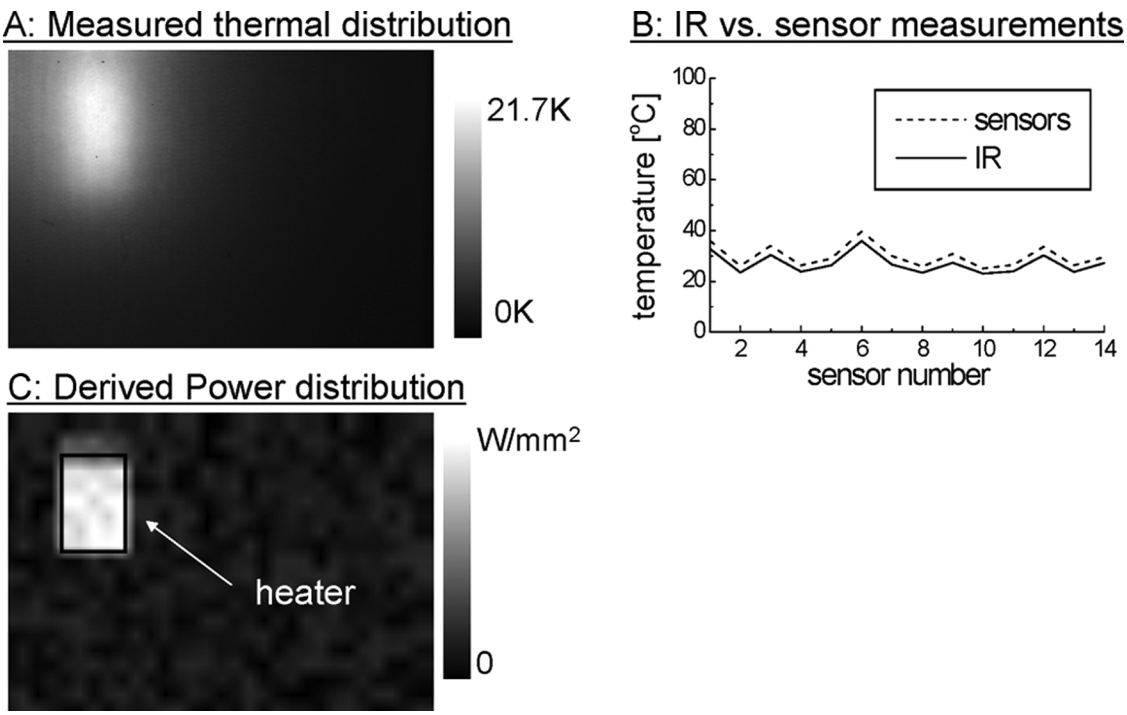

Fig. 3. SIMP validation: (a) Measured temperature distribution using the first step of the SIMP technique. (b) Comparison of the measured IR temperature with 14 resistive thermal sensors on the test chip. (c) Derived power map (granularity 30×20) from the second step of the SIMP technique.

power is not necessarily required for the power to temperature conversion. More specifically and referring to (2) and (3), by measuring the total chip power electrically, we have one more equation ($\Sigma P_i = P_{\text{total}}$), which we can use to solve for the power vector. For this particular study, we employed calculated A-matrixes, which are validated using a thermal test chip as described in more detail below. Once the A-matrix has been determined, the corresponding power vector can be readily calculated for each measured (steady state) temperature distribution. Note that the same (superposition) technique can be applied to transient power and temperature distribution. In some cases when solving for the power distribution, we constrain the solution for the power vector (to certain ranges) in order to get better accuracy for the derived power maps. For this equation (3) is solved using a linear least square fit constraining the solutions to a range of values for the power vector.

C. Validation of SIMP Methodology

In order to benchmark the SIMP technique, we applied it to a fully packaged thermal test chip with a known power distribution. The thermal test chip has 14 resistive sensors distributed throughout the die area and a rectangular heater in the upper left corner. Fig. 3(a) shows the measured thermal distribution of this test chip with the heater powered up (using the first step of the SIMP technique). In Fig. 3(b), we compare the measured temperatures with the readings from the resistive thermal sensors, which are not only in excellent agreement with each other but they also agree with computational fluid dynamics calculations (CFD). As it is evident in Fig. 3(b), the temperatures, which are measured by the resistive sensors, are slightly higher because they are located on the circuitry side while the SIMP technique measures the temperatures at the backside. The difference ($\sim$2%) between the backside and circuitry side temperatures again agrees very well with the CFD modeling predictions. Fig. 3(c) shows the derived power map from the second step of the SIMP technique. The data resolves the rectangular heater shape with very good signal to noise ratio. Although the power map in Fig. 3(c) consists of only 30×20 data points, it still demonstrates clearly that the SIMP technique can measure power distributions with quite high accuracy. Adding up the power sources of the power map in Fig. 3(c), which were derived from a (validated) A-matrix, and comparing this to the total electrically measured chip power, we find an agreement of $\sim$3% demonstrating the accuracy of the A-matrixes deployed in this work.

III. Direct Temperature and Power Distribution Measurements of a Fully Working Microprocessor

A. Temperature and Power Maps of the PowerPC970MP Microprocessor

The SIMP technique is applied to the dual core PowerPC-970MP microprocessor. Fig. 4 shows various temperature and subsequently derived power distributions for the PowerPC970MP microprocessor measured by the SIMP method. Each temperature/power column pair in Fig. 4 refers to a different gray scale bar. The images demonstrate how well the SIMP technique de-convolves the initially measured (and "smeared" out) temperature fields. The image size (including kerfs) is 13.2×11.6 mm^2 and the die thickness of this chip was thinned down to 90 μm to enhance the temperature resolution. While the actual pixel resolution of the camera is $\sim$ 50×50 μm^2, the spatial resolution of the temperature

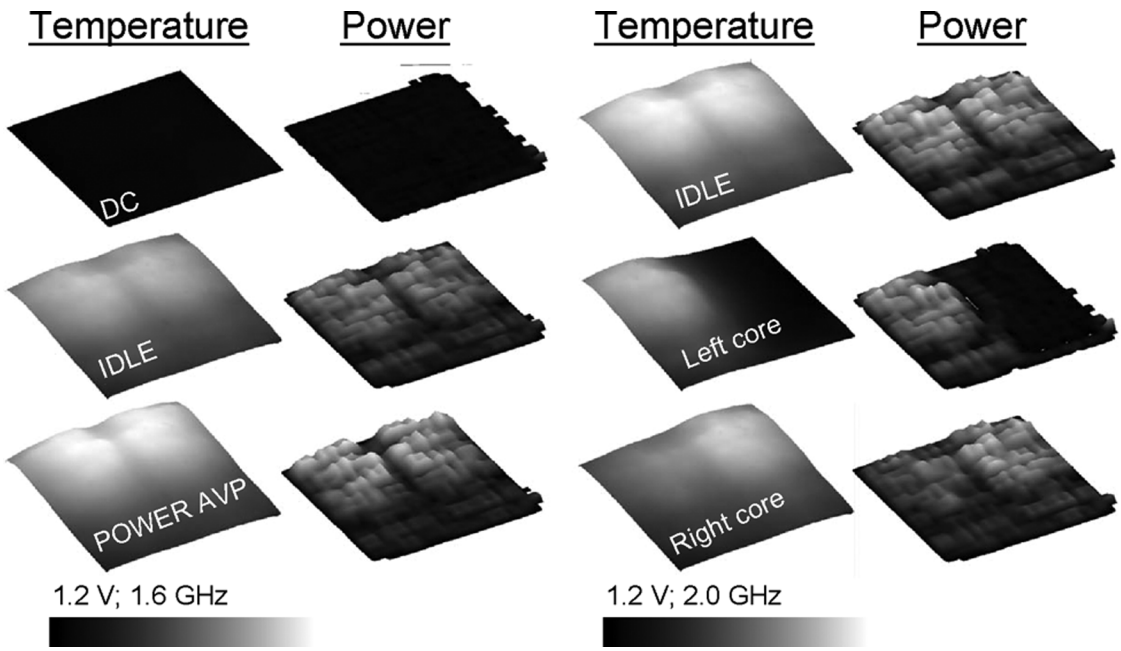

Fig. 4. Temperature and subsequently derived power distributions (granularity: 30 × 30) for the PowerPC970MP microprocessor measured by the SIMP method.

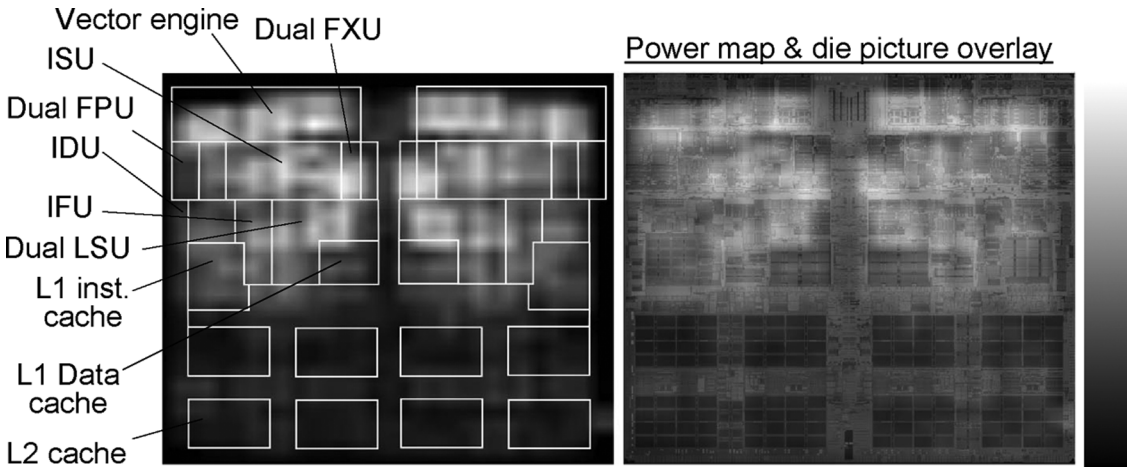

Fig. 5. Power distribution overlaid with the floorplan (left) and a die image (right) of the PowerPC970MP microprocessor running a high power workload.

map is governed by the die thickness (here approximately to 100 μm) as discussed in detail in [9]. In this reference, the minimum required granularity for power distributions has been calculated to predict accurately chip temperature fields. Specifically, transfer functions between initial power distributions and resulting temperature fields for various packages and cooling conditions were derived. Two-dimensional (2-D) Fast Fourier Transform of the temperature profiles were carried out in order to establish spatial cutoff frequencies, which relates to the minimum granularity required for thermal analysis. The resolution of the power maps shown in Fig. 4 are governed by the granularity of the A-matrix (440 × 386 μm^2), which could be in principle much higher (but not higher than the temperature resolution). As demonstrated in [9], this granularity is sufficient to represent the measured temperature distribution within less than 1%.

In the first two columns of Fig. 4, the respective temperature and power distributions are shown for three different workloads: DC, IDLE, and a high power workload (here for 1.6 GHz, $V_{dd} = 1.2$ V). In the third and fourth columns, the temperature and corresponding power maps for the IDLE workload are shown (here for 2.0 GHz and $V_{dd} = 1.2$ V). In the first row, both cores are running and in the second row the left core is running while the right core has been entirely turned off. Finally, in the third row the left core has been powered down.

Fig. 5 allows a closer look at the power distribution during the high power workload, where the measured power map is overlaid with a coarse floorplan (left) and the die picture (right). The data enables us to assign the power levels to the individual units, which is critical to develop more temperature and power efficient chips. Specifically for the PowerPC970MP, sub units of the VMX (SIMD/vector) engine, ISU (instruction sequencing

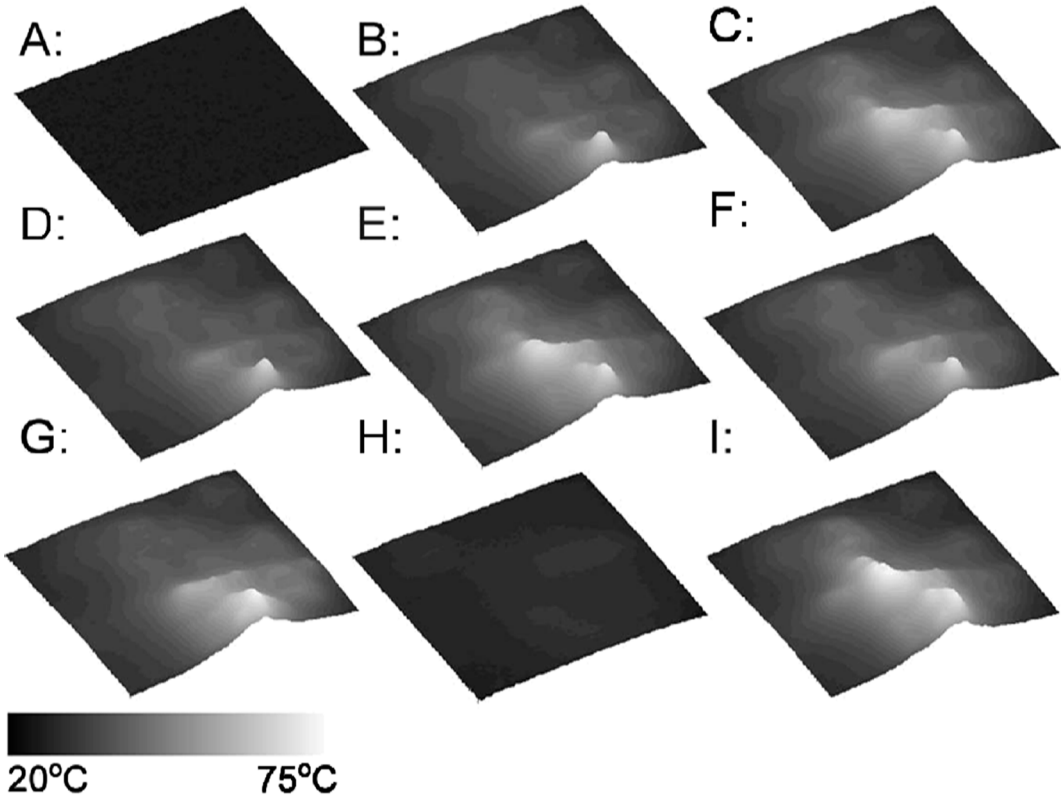

Fig. 6. Thermal distribution of a standard (non-IBM) desktop microprocessor during bootup of the operating system. The dwell time between the images is 10 s.

unit) and FXU (fixed point integer unit) are identified as high power density regions.

B. Hotspot Movements and Dynamic Temperature Distributions

The data in Fig. 4 shows that the actual position of the hotspot moves quite drastically for the different utilization levels. More specifically, a hotspot movement of more than 2 mm is observed from single to dual core operation demonstrating that thermal sensors readings and their actual differences to the peak temperatures (T_{jmax}) are workload dependent. Evidently, this can have a significant impact for the thermal and power management. The hotspot movement can be explained readily by referring to the power map in Fig. 5. With both cores running, the thermal cross-talk between the FXUs governs the hotspot (which is close to the middle of the processor) while with only one core running, the SIMD/vector engine power shifts the hotspot over to the side.

In order to demonstrate how dynamic the chip temperature and power distributions are, we show in Fig. 6 a series of measured thermal distributions for a standard desktop, (non-IBM) microprocessor during bootup of an operating system. The die of this chip is approximately 1 cm^2, which has been thinned down to less than 100 μm. The first thermal image (A) shows the temperature before the initial bootup with the microprocessor at room temperature while the subsequent images in Fig. 4 show the temperature distributions spaced by 10 s. The time of acquiring an individual temperature distribution is less than 50 ms. The data reveals significant temporal and spatial variations of the temperature fields, which is due to the circuit layout as well as the varying utilization levels across the processor during bootup. For example, in most images one or even two very pronounced hotspots are measured. After some very high peak temperatures [see Figs. 6(B)–(G)] during the initial phase of the bootup, lower temperatures can be observed in Fig. 6(H) before suddenly higher temperatures return.

C. Competitive Comparison

As part of the SIMP methodology, the processor has to be re-packaged into the transparent heat sink, which cooling conditions can be controlled very accurately. As a result, SIMP enables us to compare the hotspots of competitive microprocessors under (almost) identical cooling conditions. Specifically, we have investigated several competitive microprocessors by measuring the dynamic temperature distributions for 26 SPEC2000[1] benchmarks. For example, in Fig. 7 we compare the predecessor of the PowerPC970MP (single core) with a competitive microprocessor running the same spec benchmark under identical cooling conditions. In this example, the PowerPC processor dissipates 79 W (*average* power density of 125 W/cm^2) while the competitive processor consumes 85 W (*average* power density of 80 W/cm^2). In order to compare these processors more quantitatively, we have integrated the measured chip peak temperatures (T_{jmax}) over the run time of a series of spec benchmarks and then divided by the total run time (i.e., integrated peak temperatures/performance). Applying this metric for the spec benchmarks, we find that the

[1]http://www.spec.org

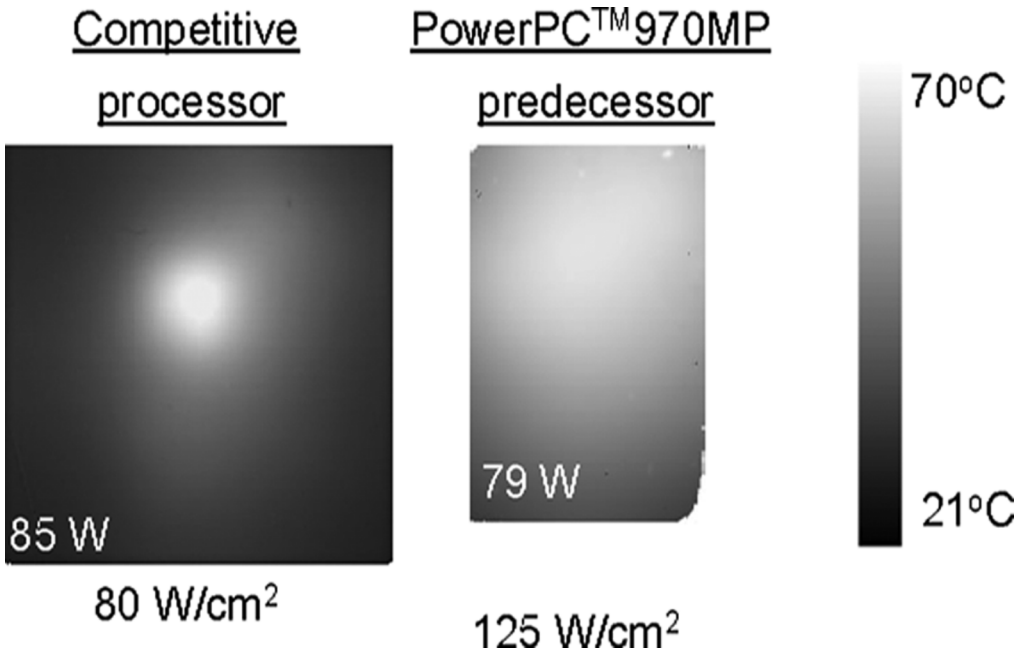

Fig. 7. Comparison of the thermal distribution of the PowerPC970MP predecessor with a competitive microprocessor running the same workload under the same cooling conditions.

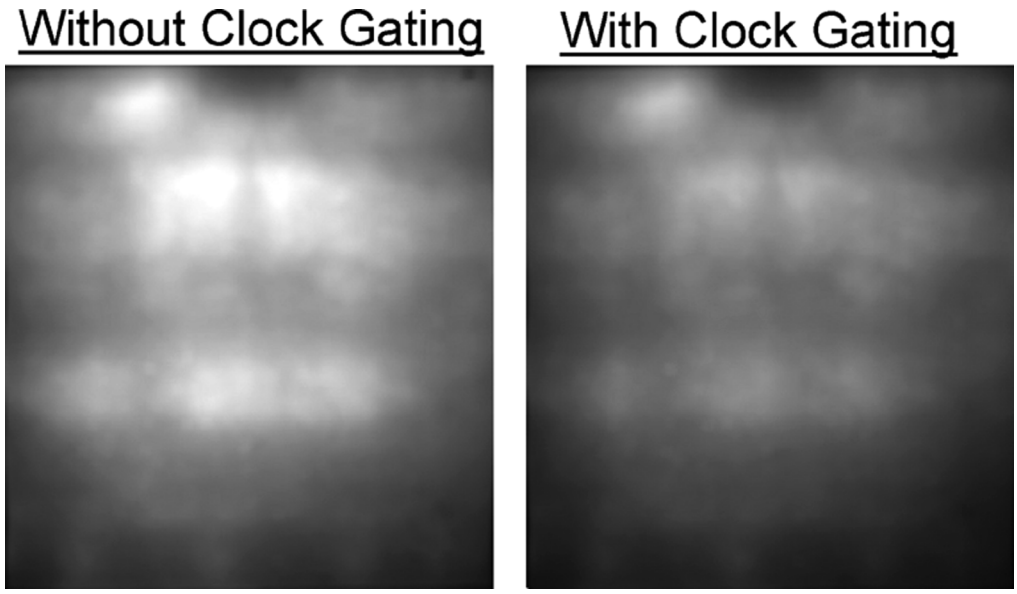

Fig. 8. Temperature distribution of the dual P0WER5 microprocessor with and without clock gating.

PowerPC processor is significantly more temperature efficient (less T_{jmax} for the same performance) than its competitor (although it has a higher *average* power density). The data suggest that the competitive microprocessor has a much higher *local* power density, which disproportionally drives up the peak temperatures. The pronounced hotspot of the competitive microprocessor is also evident during other workloads such as OS bootup. It is interestingly to note that when comparing the measured temperature efficiencies (peak temperature/performance) with simultaneously measured power efficiencies (energy/performance) we find that the differences between processors are significantly larger for the temperature efficiencies than for power efficiencies.

D. Implications for Circuit Design, Chip Floor Planning, and Processor Architecture

The SIMP technique can be quite important for circuit design, floor planning and processor architecture. For example, the power maps can be directly used to benchmark current chip power models by comparing the actual power distributions with

the originally predicted power maps from pre-silicon modeling tools at the various stages of the microprocessor design [20]. Eventually, this will result in improved pre-silicon modeling capabilities, which will be critical to guide the design of more power and temperature efficient microprocessors. In addition, the detailed temperature and power distribution information can have a direct impact on chip floor planning for next generation processors that are under design. Finally, this technique can be very important to understand, in which regions it is most beneficial to apply power saving techniques. For example, we have quantified the temperature benefits of clock gating for the POWER5 microprocessor as shown in Fig. 8. Specifically, we find for a particular workload that clock gating can reduce the hotspot temperature by 14% accompanied with 18% of total power reduction. The SIMP methodology allows us to understand the relative temperature-performance and power-performance efficiencies of alternate execution modes: e.g., the efficacy of running the two POWER5 cores in a two-way shared memory multiprocessor (SMP) configuration (with each core executing in single-thread mode) or in a four-way SMP mode (with each core executing two simultaneously multithreaded tasks). With a parameterized pre-silicon simulator that has been validated and calibrated once using the SIMP technique, one can study various power versus temperature versus performance tradeoffs early in the design cycle of future microprocessors in the same architectural family. Such a facility enables the design team to make the right decisions during the crucial early-stage microarchitectural design phase. In the absence of such accurately validated simulators, the design team is likely to make fundamentally erroneous choices in microarchitecture, circuit design and floor planning.

IV. Conclusion

In this paper, we have discussed the importance of power and temperature distributions for hotspot-limited chips. The details of a new experimental technique—spatially-resolved imaging of microprocessor power, or SIMP—are presented, which can measure detailed power and temperature distributions of microprocessors under full operating conditions. In this paper, we applied this technique to the dual core PowerPC970MP microprocessor to measure detailed temperature and power distributions as a function of workload and frequency. We believe that this methodology is very important to understand and diagnose high power density regions and hotspots in microprocessors, which is vital for designing the appropriate cooling and package solutions. The technique can be used benchmarking chip power models, which will be critical to guide the design of more power and temperature efficient microprocessors. The data presented in this paper show dynamically changing temperature distributions of fully operational chips with significant hotspot movements, which is in particular important for power and thermal management schemes. Finally, we have compared the temperature efficiencies of two competitive microprocessors demonstrating that the PowerPC processor is more temperature efficient than its competitor despite having a higher average power density

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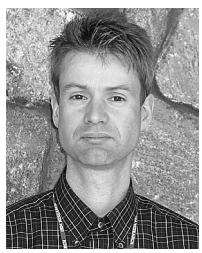

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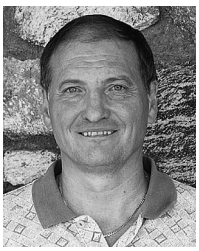

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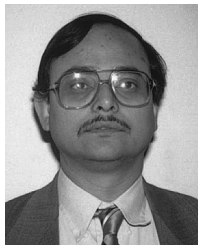

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