

Efficient Microchannel Cooling of Multiple Power Devices With Compact Flow Distribution for High Power-Density Converters

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Abstract—In this article, we describe a new approach for the compact and energy-efficient cooling of converters where multiple miniaturized microfluidic cold plates are attached to transistors providing local heat extraction. The high pressure drop associated with microchannels was minimized by connecting these cold plates in parallel using a compact three-dimensional-printed flow distribution manifold. We present the modeling, design, fabrication, and experimental evaluation of this microfluidic cooling system and provide a design strategy for achieving energy-efficient cooling with minimized pumping power. An integrated cooling system is experimentally demonstrated on a 2.5-kW switched-capacitor dc–dc converter, cooling down 20 GaN transistors. A thermal resistance of 0.2 K/W was measured at a flow rate of 1.2 mL/s and a pressure drop of 20 mbar, enabling the cooling of a total of 300 W of losses in the converter using several milliwatt of pumping power, which can be realized with small micropumps. Experimental results show a tenfold increase in power density compared with the conventional cooling, potentially up to 30 kW/L. This proposed cooling approach offers a new way of coengineering the cooling and the electronics together to achieve more compact and efficient power converters.

Index Terms—Additive manufacturing, electronics cooling, gallium nitride (GaN), high power density, liquid cooling, microchannel cooling, microfluidics, switched-capacitor converter, thermal management, three-dimensional (3-D) printing.

I. INTRODUCTION

OVER the past decades, we have seen an ongoing trend of reduction in the size of power converters, where roughly every decade the power density of converters doubles [1]. The increasingly tight constraints on size and weight for these power electronics systems have pushed a broad range of innovations, spanning from wide-band-gap (WBG) semiconductor devices [2] to new converter topologies [3]. WBG devices, employing

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gallium nitride (GaN) and silicon carbide, have a small footprint and high power density owing to their low specific ON-resistance and high-breakdown electric field [4], [5], enabling a compact converter design. Additionally, GaN high electron mobility transistors can operate at higher frequencies, enabling the use of smaller passive components that further reduces the converter volume. However, the increased switching losses due to higher switching frequencies and reduced die sizes cause high heat fluxes, surpassing 1 kW/cm² [6], [7], which is far beyond the capabilities of conventional cooling methods [8]. Inadequate cooling of these devices causes high junction temperature, which degrades their performance and reliability [9], [10].

The thermal challenges become more pronounced in converter topologies with a large number of active components, such as modular [11], [12] and composite topologies [13]. Uneven temperature rise over multiple devices causes hotspots that limit the system performance. The thermal management of these converters closely resembles that of the 1980s multichip processor modules of mainframe computers, for which elaborate cooling technologies have been developed to simultaneously cool multiple chips [14]. However, such cooling solutions are prohibitively large for contemporary high power-density applications. Several modular air-based cooling topologies have been presented to cool down the converters with a large number of components in a small form factor [15], [16], but the low heat transfer coefficient of air ultimately limits heat fluxes to roughly 300 W/cm² [8]. To achieve higher power density in topologies with a large number of components, high-performance cooling techniques, such as liquid cooling, are required to surpass this limit.

Several high-efficiency liquid cooling strategies have been proposed for cooling of individual power devices, such as impinging coolant on the device [17], [18] as well as flowing coolant through microchannels [19]. The latter can result in state-of-the-art heat fluxes due to its large surface area and high heat transfer coefficient [20]. However, microchannels typically suffer from high-pressure drop. Approaches to reduce the pressure drop over microchannel heat sinks have received considerable attention [21]. A promising method is the use of a manifold structure to distribute the flow over the microchannels [22]. This manifold microchannel (MMC) structure reduces the pressure drop, increases the temperature uniformity, and increases the heat transfer coefficient [23], [24]. However, although these MMC heat sinks demonstrated in the literature

have outstanding capabilities for high heat flux management [25]–[27], the complicated fabrication procedure, consisting of multiple bonding steps, has prevented a large-scale adoption of this technology.

System-level approaches, to employ the easier-to-fabricate parallel straight microchannels in an optimized configuration with minimum pumping requirements, have remained largely unexplored. Yet, this could be a crucial step toward the larger adaption of microchannels in liquid cooling applications. Consequently, there is currently no standard thermal management solution that can be mounted on a converter, such as conventional heat sinks, while providing the high cooling performance of microchannels simultaneously to all active devices.

In this article, we propose a novel compact and energy-efficient microfluidic cooling system for the power converters with multiple power devices by mounting microchannel cold plates on each device. The high-pressure drop usually associated with microchannels was minimized using a customized compact flow distribution manifold that connects these microfluidic heat sinks in parallel to a common inlet and outlet. In Section II, a model is presented to determine the optimal microchannel and manifold geometry that maximizes the cooling capability and minimizes the required pumping power. Cold plates were fabricated on silicon using standard clean-room processes but could easily be replaced by the high-throughput fabrication methods, such as microdeformation processes. We demonstrate flow distribution manifolds realized using the three-dimensional (3-D) printing as well as the conventional fabrication methods to demonstrate the possibility of their mass production in a cost-effective way.

In Section III, the thermal and hydraulic performance of the heat sink is experimentally evaluated. Finally, in Section IV, the cooling module, consisting of 20 silicon microchannel cold plates, is demonstrated on a compact 2.5 kW switched-capacitor dc–dc converter to demonstrate the potential of this new cooling system and its impact on power density. This proposed method provides the high-performance microchannel cooling in a very compact form factor with low pressure drop, making it a promising technology for future power converters. Section V concludes this article.

II. MODELING, DESIGN, AND FABRICATION

In this section, the analytical expressions that describe the hydraulic and thermal performance of the heat sink are derived, which are used to optimize the heat sink geometry for energy-efficient cooling. First, the cooling performance of an individual cold plate is evaluated to obtain an optimum design, followed by the design and fabrication of the distribution manifold.

A. Microchannel Cold Plates

Fig. 1 shows a schematic overview of the proposed cooling method. A packaged device is mounted on a printed circuit board (PCB) and cooled by a microchannel cold plate attached on the top of the device, separated by a thermal interface material (TIM). We investigate the situation where all dissipated power travels upward to the microchannel cold plate, which is the case if the device has a relatively low junction-to-case thermal

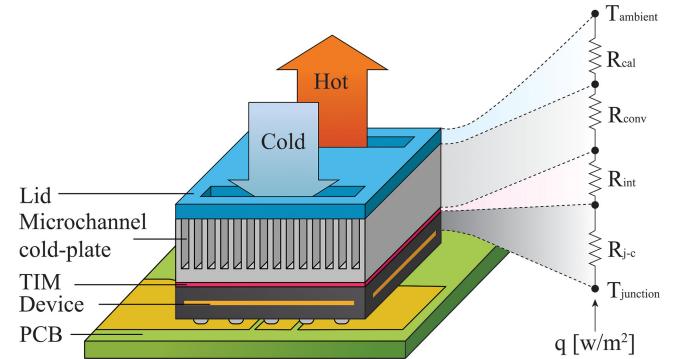


Fig. 1. Schematic cross section of a transistor, cooled by a microchannel cold plate, and an equivalent thermal resistance model.

resistance to the top of the device and a high junction-to-board thermal resistance.

1) Analytical Model: The main design objective is to achieve energy-efficient cooling since a reduced pumping power results in a smaller pump size. Cooling efficiency is described by the coefficient of performance (COP), given in (1), defined as the ratio of dissipated power in the system, Q_{max} , to the pumping power required P to keep the junction at a given maximum junction temperature, ΔT_{max}

$$\text{COP} = \frac{Q_{max}}{P} \quad (1)$$

$$P = f\Delta p \quad (2)$$

$$\Delta T_{max} = Q_{max}R_{tot}. \quad (3)$$

The pumping power, defined in (2), is the product of the flow rate f and the pressure drop Δp . R_{tot} is the total thermal resistance between the junction of the device and the inlet temperature of the coolant, which relates the heat losses to temperature rise, according to (3). From (1)–(3), it is clear that to increase COP, the pressure drop, flow rate, and thermal resistance have to be reduced. However, these values are interdependent, so to determine the optimal microchannel geometry, relations among pressure drop, thermal resistance, and flow rate are required.

The total thermal resistance R_{tot} is the sum of the four components shown in the 1-D thermal resistance network in Fig. 1. The caloric thermal resistance of the coolant R_{cal} , given in (4), describes the temperature rise of the coolant between the inlet (T_{in}) and the outlet (T_{out}) and depends on the flow rate f , the fluid density ρ , and heat capacity C_p

$$R_{cal} = \frac{T_{out} - T_{in}}{Q_{max}} = \frac{1}{\rho C_p f}. \quad (4)$$

The junction-to-case thermal resistance of the device R_{j-e} is given by the device manufacturer, and the thermal interface resistance R_{int} depends on the type of TIM used. The thickness and thermal conductivity of the TIM are important factors that determine R_{int} . The total thermal resistance of the cold plate consists of the thermal resistance between the surface of the cold plate and the base of the microchannels, and a convection component on the microchannel surface. However, due to the high thermal conductivity of silicon, the conduction component is negligibly small (<0.01 K/W). For this reason, the thermal

resistance of the cold plate is modeled as only a convective thermal resistance R_{conv} , as expressed in (5). h is the heat transfer coefficient and A is the total surface area of the microchannels. Using the fin model, previously described in [20] and [28]–[30], an expression was derived for the convective thermal resistance, as shown in (5). The geometry of a microchannel is described by the channel width and fin width. A wider channel is favorable for reducing pressure drop but comes at the cost of a lower fin efficiency. Numerous works in the literature have studied the impact of the proportion of fin to channel width in high aspect ratio microchannels and found a favorable distribution lies generally around 1:1 [31], [32], [33]. For that reason, we define w as both the channel and fin width, which simplifies the analytical expressions. z is the channel depth and Nu is the Nusselt number. ϵ is the fin efficiency, calculated using (6), where k_s is the thermal conductivity of the heat sink material and k_f is the thermal conductivity of the fluid

$$R_{\text{conv}} = \frac{1}{hA} \epsilon^{-1} = \left(1 + \frac{z}{w}\right)^{-1} \frac{w}{LWk_fNu} \epsilon^{-1} \quad (5)$$

$$\epsilon = \tan h \left(z \sqrt{\frac{2h}{k_s w}} \right) \left(z \sqrt{\frac{2h}{k_s w}} \right)^{-1}. \quad (6)$$

For a given design and its corresponding thermal resistances (R_{conv} , R_{int} , R_{j-c}) and heat load, Q_{\max} , the required flow rate to keep the junction temperature rise at ΔT_{\max} can be calculated using (7). The relationship between the pressure drop and flow rate in the microchannel cold plate can be expressed in terms of hydraulic resistance r_h . Considering a cold plate with N parallel channels, the pressure drop can be calculated using (8) [34]. Equation (8) does not account for entrance effects but only considers fully developed laminar flow through the microchannels. The validity of this assumption is investigated later in this work. Combining (1)–(8) results in (9), an expression to calculate COP given a certain geometry and heat load. Equation (9) shows that the coolant requires a high ratio of $\rho^2 C_p^2 / \mu$, which makes water a good candidate, but this expression does not give an intuitive solution for the optimal channel width. This will be the subject of the following section:

$$f = \left(\rho C_p \left(\frac{\Delta T_{\max}}{Q_{\max}} - R_{\text{conv}} - R_{\text{int}} - R_{j-c} \right) \right)^{-1} \quad (7)$$

$$\Delta p = r_h f = \frac{12 \mu L}{N (1 - 0.63 w/z) w^3 z} f \quad (8)$$

$$\text{COP} = \frac{\rho^2 C_p^2 Q_{\max}}{r_h} \left(\frac{\Delta T_{\max}}{Q_{\max}} - R_{\text{conv}} - R_{\text{int}} - R_{j-c} \right)^2. \quad (9)$$

2) Evaluation: Using the aforementioned model, we studied the effect of channel size on the cooling performance of silicon microchannel cold plates with channel depth z fixed at 400 μm and channel width w varying between 10 μm and $w = 300 \mu\text{m}$. Water was chosen as the coolant and a typical value of 0.5 K/W was chosen for both R_{int} and R_{j-c} [35]. The Nusselt number was calculated for a fully developed laminar flow under uniform heat flux conditions using the correlation from the article presented in [34].

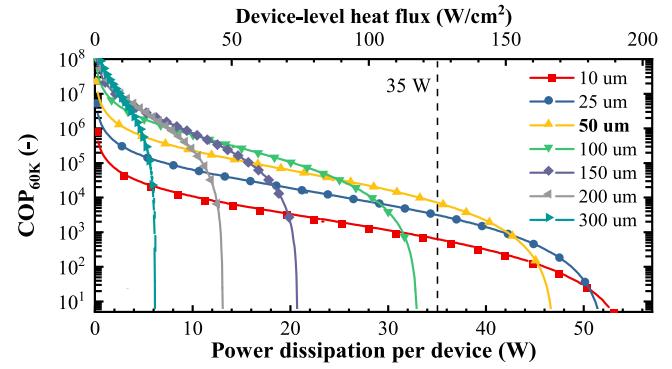


Fig. 2. Calculated COP versus maximum power dissipation per transistor (Q_{\max}) cooled using the proposed microchannel cold plate for channel widths varying between 10 and 300 μm , considering a maximum temperature rise ΔT_{\max} of 60 $^{\circ}\text{C}$ and an inlet temperature of 22 $^{\circ}\text{C}$. Device-level heat flux was calculated based on a 7 mm \times 4 mm device size.

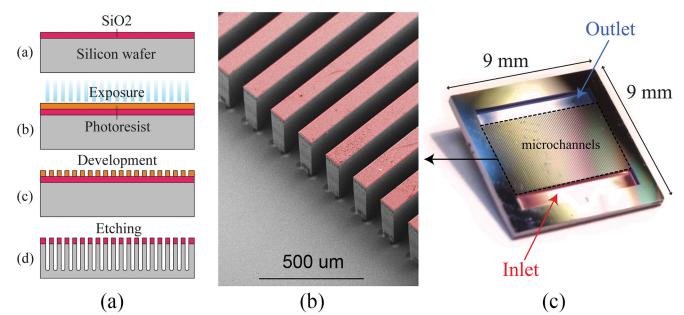


Fig. 3. (a) Fabrication process of the silicon microchannel cold plates. (b) SEM image of the microchannels after etching, where false coloring indicates the presence of SiO₂. (c) Picture of the cold plate after dicing.

Fig. 2 shows the calculated COP versus maximum dissipated power for microchannel cold plates. All curves show the same trend: COP decreases with increasing power due to the higher flow speed required to keep the temperature rise between the junction and the inlet temperature equal to $\Delta T_{\max} = 60 ^{\circ}\text{C}$. After a certain power, a sharp cutoff in COP is observed due to the excessively high flow rates. Reducing the microchannel width results in an increase in Q_{\max} at which this cutoff occurs because of the reduced R_{conv} , however, at the cost of a lower COP at lower heat loads. For example, 25 μm channels can extract approximately a five time higher heat load than 200 μm channels but have ten times lower COP at low heat loads.

This finding reveals that it is important to have an estimation of the power losses in the system to choose the optimal geometry. In our case of a GaN-based soft-switched converter, based on the maximum conduction losses of the used GaN devices [36], Q_{\max} was estimated at 35 W, making 50 μm channels the favorable design choice to obtain the maximum COP based on these assumptions (see Fig. 2).

3) Fabrication: Microchannel cold plates were fabricated on a 4-in silicon wafer in a clean-room environment, as illustrated in Fig. 3(a). A 2- μm -thick layer of SiO₂ was deposited using plasma-enhanced chemical vapor deposition, which functions as a hard mask for dry etching. Channels with widths between 25 and 100 μm were defined using photolithography followed

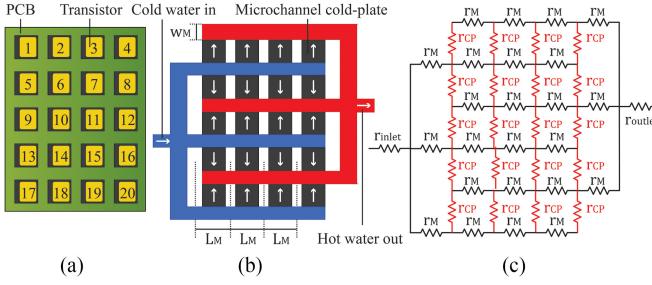


Fig. 4. (a) Layout of the transistors on a PCB. (b) Illustration of the liquid flow through the manifold. Blue and red lines indicate the cold and hot water, respectively. (c) Equivalent hydraulic resistance network of the manifold and the microchannel cold plates.

by a dry etch of the SiO_2 using C_4F_8 chemistry. Finally, $400 \mu\text{m}$ -deep vertical channels were etched in silicon using the Bosch deep reactive-ion etching process. The inlet and outlet ducts were $1 \text{ mm} \times 7 \text{ mm}$ rectangular openings. Fig. 3(b) shows a scanning electron microscope (SEM) image of the microchannels after etching. As a final step, the wafer was diced into individual $9 \text{ mm} \times 9 \text{ mm}$ cold plates, as shown in Fig. 3(c). Due to the inlet and outlet ducts, the cold plate is slightly larger than the transistor. In order to ensure good contact between these two components, no higher parts should be positioned closely to the transistor.

B. Manifold

The purpose of the manifold is to distribute liquid to multiple microchannel cold plates that are in direct contact with the transistors on a PCB, as shown in Fig. 4(a). Individual cold plates can either be connected in series or in parallel. A series connection guarantees a consistent flow rate over all cold plates but suffers from a significantly higher pressure drop as well as a higher temperature rise of the water at an identical flow rate. For this reason, it is favorable to parallelize the cold plates, as illustrated in Fig. 4(b). However, a careful manifold design is required to ensure an equal fluid distribution over all cold plates and avoid local overheating [37], [38].

1) Analytical Model: The cold-plate manifold was modeled as a network of resistors, as illustrated in Fig. 4(c), where each resistor represents the hydraulic resistance of a specific part of the flow path. The hydraulic resistance of each cold plate r_{CP} can be determined using (8), while the hydraulic resistance of the manifold inlet and outlet sections r_M calculated using (10). This equation gives the pressure drop of a square manifold channel section with cross section w_M and length L_M [34]

$$r_M = \frac{12\eta L_M}{0.42 w_M^4}. \quad (10)$$

The currents $I_{\text{CP},i}$ flowing through the resistors, marked in red in Fig. 4(c), represent the flow rate in the cold plates. Good flow uniformity can be guaranteed if r_{CP} is significantly larger than the sum of the hydraulic resistances over the manifold section. The percentage of the variation of current from the mean, E_i , represents the flow nonuniformity, defined according to (11), which is used to assess the quality of the manifold design. A

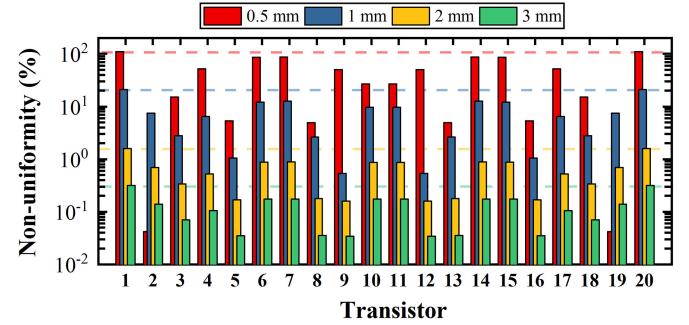


Fig. 5. Flow rate nonuniformity for manifold cross-section width w_M varying from 0.5 to 3 mm, defined as the percentage of absolute deviation of flow rate from the mean for all 20 cold plates.

TABLE I
MICROCHANNEL WIDTH AND THE REQUIRED MINIMUM MANIFOLD CHANNEL WIDTH TO HAVE LESS THAN 1% FLOW NONUNIFORMITY

$w_c [\mu\text{m}]$	N	$z [\mu\text{m}]$	$r_{\text{CP}} [10^{10} \text{ Pa s m}^{-3}]$	$w_M [\text{mm}]$
25	160	300	7.6	1.67
50	80	300	2.0	2.34
100	40	300	0.57	3.20
250	16	300	0.15	4.47
500	8	300	0.08	5.19

good design should have a low value of E_i such that the liquid is equally distributed over all cold plates

$$E_i = \left| \frac{20 \cdot I_{\text{CP},i}}{\sum_{j=1}^{20} I_{\text{CP},j}} \right| - 1. \quad (11)$$

2) Simulation: We investigated the flow uniformity of a manifold delivering coolant to a 4×5 grid of transistors, as illustrated in Fig. 4(a) and (b), using the microchannel cold plates described in Section II-A.3 for each transistor ($N = 80$, $w = 50 \mu\text{m}$, $z = 300 \mu\text{m}$, and $L = 6 \text{ mm}$). The manifold had equal section length L_M of 2 cm [see Fig. 4(b)], and their cross section w_M was varied from 0.5 to 3 mm to study its impact on the flow uniformity. *LTspice* was used to calculate the currents in the resistor network from Fig. 4(c), which corresponds to the flow distribution through all 20 cold plates. Fig. 5 shows the percentage of flow nonuniformity, which strongly depends on the manifold channel size. For $w_M = 0.5 \text{ mm}$, the flow rate nonuniformity is above 100%, whereas for $w_M = 2 \text{ mm}$, the nonuniformity is limited to approximately 1%. This result clearly shows the importance of properly sizing the manifold for obtaining a uniform distribution of coolants to the cold plates.

Table I summarizes the minimum manifold channel cross sections required to have a flow nonuniformity below 1% for various microchannel widths. The strong dependence of the hydraulic resistance on the microchannel width leads to a clear advantage in using small-dimensional cooling channels for this type of flow parallelization, as a 475- μm reduction in microchannel size w_c (from 500 to 25 μm), enables a 3.5-mm reduction in manifold channel cross section. In other words, a small reduction in microchannel width results in a large reduction of the volume of the liquid distribution system. Furthermore, since the manifold channel width also limits the minimum spacing between the

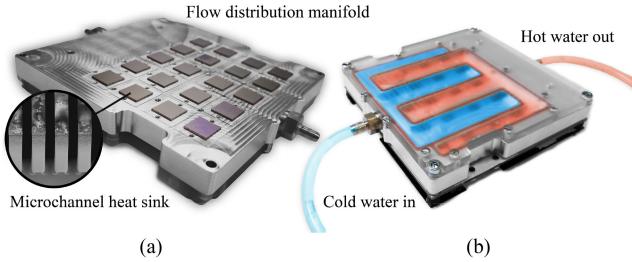


Fig. 6. Aluminum CNC-machined manifold. (a) Bottom side with 20 silicon microchannel cold plates attached to the manifold. (b) Top side with a polycarbonate lid.

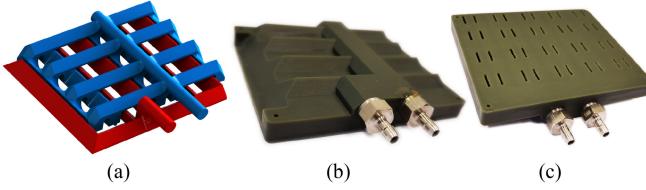


Fig. 7. Manifold of 3-D print. (a) CAD model of the flow path inside the manifold. Blue and red regions indicate the cold and hot water flow, respectively. (b) Top side of the manifold after 3-D printing. (c) Bottom of the manifold which shows the slits that connect the manifold to the microchannel cold plates.

cold plates, this reduction allows the transistors to be positioned closer together.

3) *Fabrication*: Two flow distribution manifolds were fabricated based on the design rules from the previous simulation. The first manifold, as shown in Fig. 6(a), was realized using computer numerical controlled (CNC) machining and consists of three pieces: an aluminum body, a polycarbonate lid, and a silicone gasket to provide a leak-tight seal. This simple design can be easily fabricated by injection molding for low-cost mass manufacturing. The bottom side of the manifold contains 40 slits connected to the inlet and outlet of 20 silicon microchannel cold plates. The cold plates were connected to the manifold using a water-resistant double-sided adhesive, which was laser cut to size. Fig. 6(b) shows the top side of the manifold where the red and blue colors indicate the hot and cold water, respectively.

A more compact manifold was fabricated using stereolithography 3-D printing. The possibility of 3-D-printing the manifold is very interesting for rapid prototyping together with the electronic design. This way, the geometry of the cold plate defines the cooling performance whereas the manifold defines the distribution of the coolant. Additionally, by removing the constraints of the conventional fabrication methods, more compact designs can be realized. A network of overlapping inlet and outlet channels was designed, as shown in the computer-aided design (CAD) model of Fig. 7(a), where the blue and red colored sections indicate the hot and cold water, respectively. Such a design cannot be realized using conventional CNC machining, but additive manufacturing enables the realization of such a monolithic structure. High temperature resist was used (EnvisionTEC HTM140) that can withstand temperatures up to 140 °C. The sidewalls of all channels were angled at 45° to print the structure without the internal support material, as this would be impossible to remove from the monolithic structure. Fig. 7(b) and (c) shows the manifold after printing. The slits visible in Fig. 7(c) connect

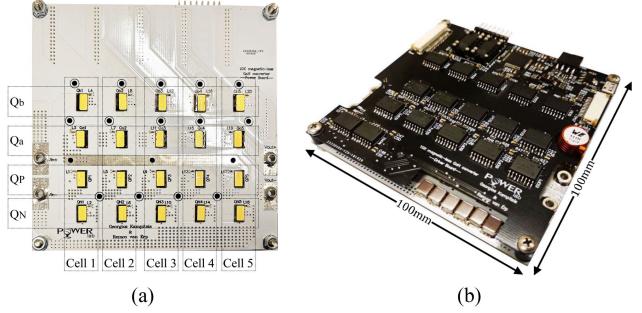


Fig. 8. Ten times step-up dc–dc converter consisting of two board. (a) Power board, containing 20 GaN transistors in a 5×4 grid. (b) Control board.

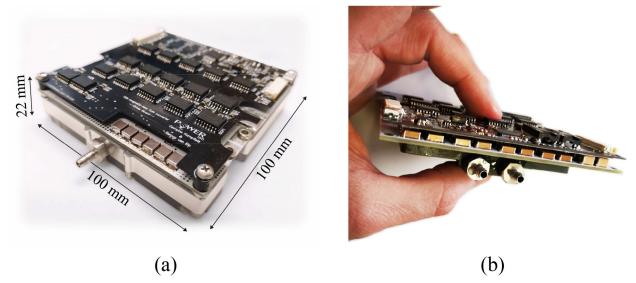


Fig. 9. Full system with (a) aluminum CNC-machined heat sink and (b) 3-D-printed manifold heat sink.

to the inlet and outlet of the silicon microchannel cold plates. The total volume of this manifold is only 35 cm³.

C. Converter

The heat sink was designed together with the switched-capacitor dc–dc converter, as shown in Fig. 8. This nX -converter, earlier described in [39], is a modular multilevel voltage multiplier with a fixed even step-up ratio n , where $n/2$ indicates the number of cells required. Each cell of this converter consists of four transistors, resulting in a total of $2n$ transistors [40]–[42]. In this article, a 10× step-up converter was used with a total of 20 GaN transistors, as shown in Fig. 8(a). This topology is an ideal testbed to evaluate the proposed cooling system, as it contains no magnetic components. The 20 transistors are, therefore, the major power-dissipating components, and the maximum output power is defined by how well these devices are cooled down.

The selected GaN transistors (GS61008T, GS66508T) have a thermal pad on the top side resulting in a low junction-to-top thermal resistance of 0.55 K/W [35], [36]. A temperature sensor was placed directly next to each transistor, sharing the same copper pad, to monitor each individual transistor temperature in real time. The top side of the converter, as shown in Fig. 8(b), contains all gate drivers, isolated power supplies, and a microprocessor to generate the pulsedwidth modulation signals. Fig. 9(a) shows the converter with the aluminum CNC-machined heat sink. An alumina-filled silicone TIM with a thermal conductivity of 12 W/mK (T-Global TGX) was placed on each transistor. The power board was fixed on the heat sink with 15 screws to ensure a good and repeatable thermal contact between each cold plate and transistor. The converter with 3-D-printed manifold heat

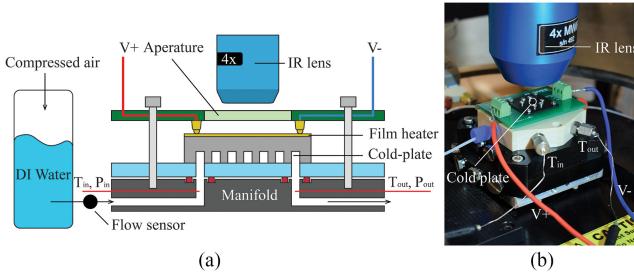


Fig. 10. (a) Schematic illustration of the cooling performance evaluation setup. (b) Picture of the test section underneath an IR camera.

sink is shown in Fig. 9(b). This system is only 200 cm³ and still includes empty space for the future integration of a pump within this volume.

III. EXPERIMENTAL EVALUATION OF THE HEAT SINK

A. Microchannel Cold Plates

A test setup was developed to experimentally investigate the performance of microchannel cold plates of various channel dimensions. This setup, as illustrated in Fig. 10(a), contains a pressure regulator (Elveflow OB1 MK3) that pressurizes a reservoir with deionized (DI) water. The DI water flows through a flow meter into the test section that contains an individual microchannel cold plate. This test setup includes two calibrated thermocouples that measure the water temperature before and after the cold plate and a pressure sensor to determine the pressure drop over the cold plate.

To investigate the properties of each individual cold plate in this setup, a thin metal film was deposited on the backside of the cold plate by electron-beam physical vapor deposition to function as a resistive heating element emulating the power dissipated by each transistor. This heating element allows an easy variation of the dissipated power, and the absence of R_{int} and R_{j-c} enables accurate measurement of the convective thermal resistance.

A PCB connected the heating element to a regulated power supply (TTI QPX1200S) and the temperature at the surface of the cold plate was measured using an infrared (IR) microscope (QFI InfraScope). The IR microscope was pixel-by-pixel calibrated by flowing water at various fixed temperatures through the cold plate using a thermostatic bath. Power dissipation was determined using an energy balance to account for any heat that leaks out of the setup by convection to the ambient or by conduction through the test section. This calculated power was within 95% of the total dissipated electrical power, which confirms a sufficiently isolated test setup. Thermal resistance was determined by taking the slope of the surface temperature rise versus power dissipation. Finally, the COP is calculated using

$$\text{COP} = \frac{\Delta T_{\max}}{R} \frac{1}{\Delta p f}. \quad (12)$$

Fig. 11(a) shows the SEM images of the three cold plates evaluated in this study ($w_c = 25 \mu\text{m}$, $50 \mu\text{m}$, and $100 \mu\text{m}$). The experimental temperature rise between the surface of the cold plate and the inlet temperature of the coolant versus power dissipation for these cold plates at a flow rate of 1 mL/s

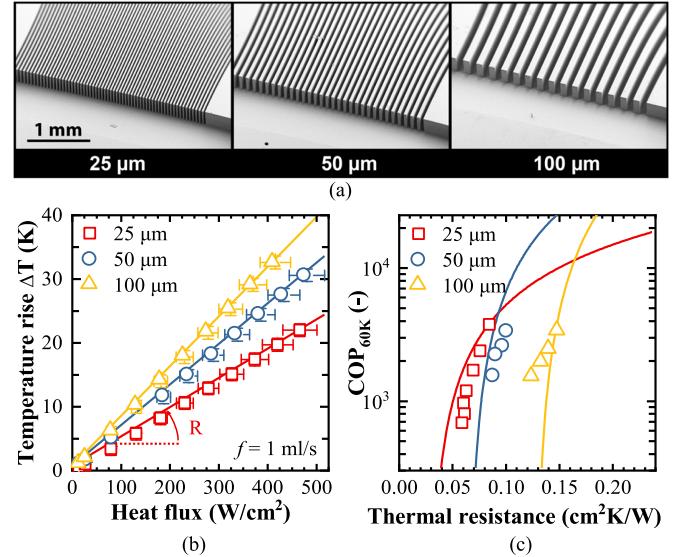


Fig. 11. (a) SEM images of the three evaluated microchannel cold plates. (b) Temperature rise between the inlet temperature of the coolant and the surface of the cold plate versus heat flux. Slope of the linear fit through the data points indicates the thermal resistance R . The coolant inlet temperature was 25 °C. (c) COP versus thermal resistance. Experimental measurements are indicated by the markers and the lines indicate the results using the analytical model from (9).

TABLE II
DIMENSIONS AND MEASUREMENTS OF MICROCHANNEL COLD PLATES

$w [\mu\text{m}]$	$z [\mu\text{m}]$	$D_h [\mu\text{m}]$	$R_{\text{conv}} [\text{cm}^2\text{K}/\text{W}]$	$h_{\text{eff}} [\text{W}/\text{m}^2\text{K}]$
25	400	47	$3.3 \cdot 10^{-2}$	$3.03 \cdot 10^5$
50	400	89	$6.9 \cdot 10^{-2}$	$1.45 \cdot 10^5$
100	400	160	$1.1 \cdot 10^{-1}$	$9.09 \cdot 10^4$

is shown in Fig. 11(b). The slope of the linear fit through these measurement points gives the thermal resistance R . The experimental COP, calculated using (12), is shown in Fig. 11(c) along with the lines corresponding to the analytical model from (9), confirming that smaller sized channels can handle higher heat loads more efficiently. A reasonable match between the experimental results and the model was obtained, which validates our initial design approach. Based on the experimental results, R_{conv} was determined to be approximately $3.3 \cdot 10^{-2}$ cm²K/W, $6.9 \cdot 10^{-2}$ cm²K/W, and $1.1 \cdot 10^{-1}$ cm²K/W for $w_c = 25 \mu\text{m}$, $50 \mu\text{m}$, and $100 \mu\text{m}$, respectively. Table II provides an overview of dimensions, thermal resistances, and base-effective heat transfer coefficients.

B. Junction Temperature Estimation

To properly determine the junction to inlet thermal resistance, the junction temperature has to be estimated. Electrical methods that relate the change in ON-resistance to temperature are commonly used for this purpose [43]. However, these methods cannot be used to monitor the junction temperature in real time during converter operation. Alternatively, IR measurements can provide junction temperature information during normal operation of the device, given that the setup permits visual monitoring and a good correlation between the junction and case temperature is available [44]. In our prototype, however,

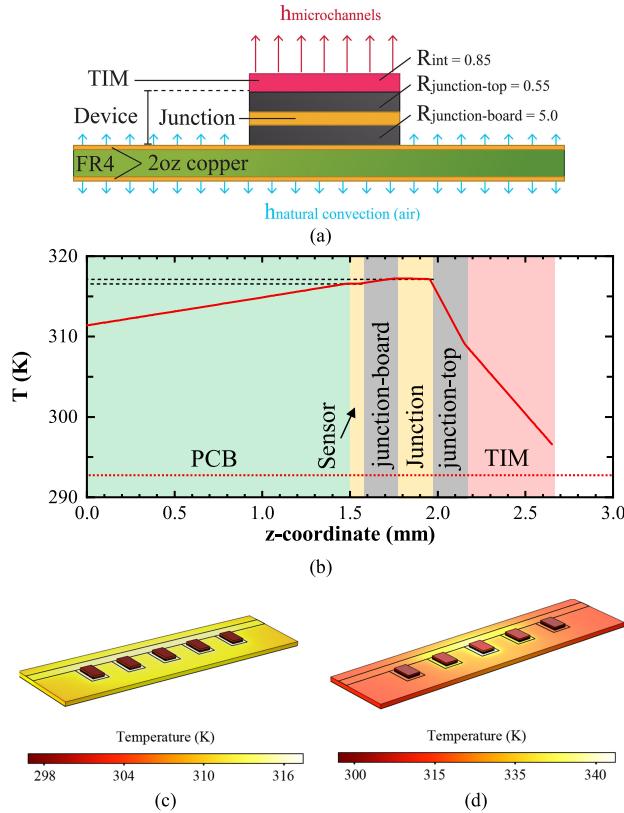


Fig. 12. (a) Schematic model of the numerically simulated structure. (b) Temperature profile through the center of a device and the PCB in scenario 1. (c) Temperature (in K) of the simulated section of the converter in scenario 1. (d) Temperature (in K) of the simulated section of the converter in scenario 2.

the transistors are covered on both sides between the PCB and the heat sink. As such, IR measurements could not be employed here.

To estimate the junction temperature in this article, temperature sensors positioned directly next to the transistor on the same copper pad were utilized. Usually, when a large heat flux travels downward from the device to the PCB, a large temperature difference can be found between the junction and such sensor, determined by the junction-to-board thermal resistance. However, in our design, we neglect the heat flux traveling to the PCB and assume that all heat flux moves upward to the cold plate. In that case, due to the absence of heat flux below the junction, an isothermal region is obtained between the chip and the board such that a temperature sensor accurately represents the junction temperature.

The validity of this approach depends on two assumptions. 1) All heat fluxes travel toward the cold plates. 2) The neighboring transistors do not affect the temperature reading. These assumptions were tested by performing numerical simulations of steady-state conductive heat transfer in COMSOL, by solving Poisson's equation ($-\nabla^2 T = q$) in 3-D. A single row of the converter, consisting of five transistors, was considered. The transistor was modeled as a three-layer structure, as shown in Fig. 12(a). A volumetric heat source represents the junction, and the junction-to-top and junction-to-board thermal resistance were obtained by giving the appropriate thermal conductivity to

TABLE III
SIMULATION RESULTS

S	device	Q [W]	ΔT [K]		ε [%]	R_{th} [K/W]
			Junction	Sensor		
1.	1	15	24.1	23.3	3.3	1.61
	2	15	24.1	23.4	2.9	1.61
	3	15	24.2	23.5	2.9	1.61
	4	15	24.1	23.4	2.9	1.61
	5	15	24.1	23.3	3.3	1.61
2.	1	10	16.4	16.6	1.2	1.64
	2	20	32.1	31	3.4	1.61
	3	30	47.6	45	5.5	1.59
	4	20	32.1	31	3.4	1.61
	5	10	16.4	16.6	1.2	1.64

the top and bottom layer, respectively. The TIM was modeled as a 1-mm-thick solid block on top of the transistor with a thermal conductivity chosen to obtain an R_{int} of 0.85 K/W. The microchannel heat sink was modeled as a convective heat transfer boundary condition of 10^5 W/m²K, corresponding to the values obtained for 100 μ m microchannels (see Table II). The PCB was modeled as a 1.6-mm-thick block of FR4, with 70 μ m of copper on either side. All exposed sides of the PCB were subjected to natural convection with a heat transfer coefficient of 10 W/m²K and 293 K was set as ambient temperature in the simulations. The remaining surfaces, i.e., the sidewalls of the chip were given adiabatic boundary conditions. The heating of the coolant was not considered in this simulation, which corresponds to the hypothetical scenario of an infinitely high flow rate. A mesh with 7×10^5 degrees of freedom (DOF) was used, and further refinement did not result in any change in the obtained values.

Two scenarios were considered in the simulations. *Scenario 1* considers an equal power dissipation of 15 W per transistor. Fig. 12(b) shows the temperature in the cross section through the center of an individual device. As can be seen, a large temperature gradient is observed between the junction and the top of the TIM, whereas the temperature difference between the junction and the top copper layer on the PCB is very small. Table III summarizes the numerical results of this simulation. It shows that in *scenario 1*, which corresponds to the normal operation of the converter, the difference between the junction temperature and the sensor has a maximum value of 3.3%. Fig. 12(d) shows the temperature in *scenario 2*, with a higher temperature in the center as expected. As can be seen in Table III, the maximum discrepancies between the junction and sensor temperature in this worst-case scenario were 5.5%. Given the limitations of available methods, the 5.5% error in worst-case scenario conditions was considered acceptable in estimating the junction temperature.

Scenario 2 considers a worst-case scenario with very uneven power distribution. Transistor 3, in the center, has a power dissipation of 30 W. Transistors 2 and 4 are subjected to a power dissipation of 20 W, whereas transistors 1 and 5 on the outside are subjected to 10 W of losses. The uneven distribution of losses causes a temperature gradient over the PCB, resulting in cross talk between the temperature rises of the individual devices. Fig. 12(d) shows the temperature in *scenario 2*, with a higher temperature in the center as expected. As can be seen in Table III, the maximum discrepancies between the junction and sensor temperature in this worst-case scenario were 5.5%. Given the limitations of available methods, the 5.5% error in worst-case scenario conditions was considered acceptable in estimating the junction temperature.

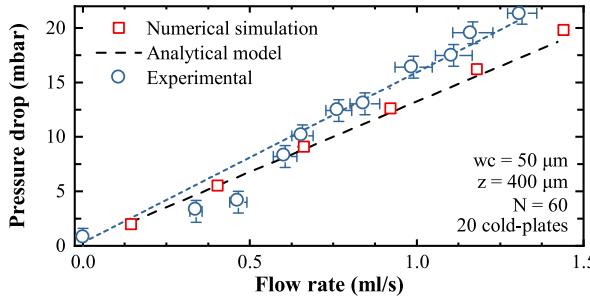


Fig. 13. Experimentally observed and predicted pressure drop versus flow rate of the manifold heat sink. Numerical simulation was performed in COMSOL included the inlet and outlets of the cold plates. Analytical prediction was based on (9), considering fully developed laminar flow without the inlet and outlet effects. Blue dashed line is a linear fit through the experimental results.

C. Manifold Heat Sink

The hydraulic performance of the heat sink was measured using pressure sensors (Elveflow MPS) mounted inside the inlet and outlet manifold region. Fig. 13 shows the experimentally observed pressure drop versus flow rate, as well as the predicted pressure drop based on the analytical model in (8). As indicated before, (8) neglects the pressure drop due to the inlet and outlet contraction and expansion as well as any developing flow phenomena. Numerical simulations were performed in COMSOL to test the validity of (8) by solving the steady-state Navier–Stokes equation on the 3-D domain of an individual microchannel with the inlet and outlet contractions ($\rho(\mathbf{u} \cdot \nabla)\mathbf{u} = \nabla \cdot (-p\mathbf{I} + \mu(\nabla\mathbf{u} + (\nabla\mathbf{u})^T)) + \mathbf{F}$). Laminar flow and incompressibility were assumed, and no-slip boundary conditions on all physical walls, a symmetry boundary condition on the virtual boundaries of the inlet and outlet ducts, as well as a zero-pressure boundary condition on the outlet were applied. A fully developed inflow with varying flow rate was fixed at the inlet of the chip. A mesh with 9×10^5 DOF was used, and further refinement did not result in any change in the obtained values. The results are compared in Fig. 12, showing good correspondence between the numerical and analytical results. The measured flow resistance was $15.7 \pm 0.51 \text{ mbar}\cdot\text{s}/\text{cm}^3$ compared with a predicted $13.0 \text{ mbar}\cdot\text{s}/\text{cm}^3$ based on the analytical model.

The exact power dissipation per transistor must be known to determine the total thermal resistance (as indicated in Fig. 1). For this purpose, the converter was operated such that all transistors were operating in a continuous conduction mode, and all power was equally dissipated over the 20 transistors. By sweeping the power dissipation and measuring the temperature rise of the device, the thermal resistance was obtained from the slope of temperature rise versus power dissipation. This measurement was repeated for multiple flow rates to isolate the flow rate-dependent caloric resistance R_{cal} from the fixed geometry-dependent thermal resistance ($R_{\text{conv}} + R_{\text{int}} + R_{j-c}$). By combining this information with the previously determined R_{conv} and the datasheet values of R_{j-c} , we estimated all thermal resistances in our system, which is valuable for optimization purposes.

Fig. 14 shows the temperature rise between the device and the inlet temperature of the coolant versus power dissipation per device. The temperature rise shows a linear relationship

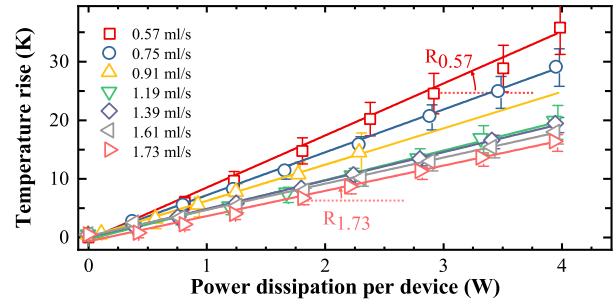


Fig. 14. Temperature rise between the device and the coolant inlet temperature versus power dissipation. Lines indicate a linear fit and the slope gives the total thermal resistance. Flow rates are combined values for all 20 devices, whereas power dissipation was measured per device. Error bars indicate the standard deviation of all 20 temperatures measured on the converter per data point.

TABLE IV
MEASUREMENT CONDITIONS

f [ml/s]	v [cm/s]	Re	R_{th} [K/W]	R'_{th} [cm ² K/W]	Δp [mbar]	COP_{60} [-]
0.57	2.06	3.3	8.93	2.50	9.05	$2.57 \cdot 10^5$
0.75	2.69	4.3	7.35	2.06	11.8	$1.83 \cdot 10^5$
0.91	3.25	5.2	6.20	1.74	14.3	$1.49 \cdot 10^5$
1.19	4.26	6.8	5.07	1.42	18.7	$1.06 \cdot 10^5$
1.39	4.97	8.0	4.86	1.36	21.9	$8.11 \cdot 10^4$
1.61	5.76	9.2	4.46	1.26	25.3	$6.55 \cdot 10^4$
1.73	6.20	9.9	4.33	1.21	27.2	$5.86 \cdot 10^4$

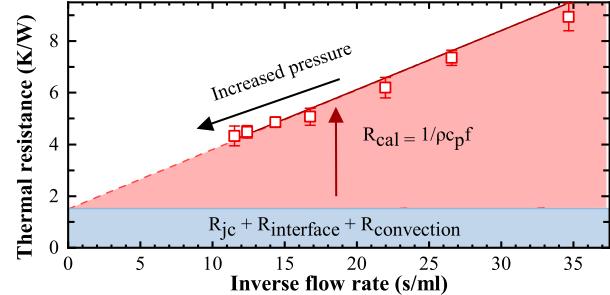


Fig. 15. Thermal resistance versus flow speed per cold plate. The red area indicates the caloric thermal resistance R_{cal} , whereas the blue part under the curve is the fixed part of the thermal resistance at a theoretical infinite flow rate.

with dissipated power, the slope of which represents the thermal resistance. The thermal resistance was determined for seven flow rates between 0.57 and 1.73 mL/s. Table IV gives an overview of all measurement conditions and the obtained values of thermal resistance, pressure drop, and COP calculated using (12), based on a junction temperature rise of 60 K. v is the average velocity of the liquid inside the microchannels and Re is the nondimensional Reynold's number, clearly indicating laminar flow conditions as well as a negligible entrance length.

The flow rate dependent thermal resistances, extracted from the slope of the curves in Fig. 14, are plotted in Fig. 15. The contribution of the thermal resistance marked in red indicates the caloric thermal resistance, showing a clear f^{-1} relation ($R_{\text{cal}} = 1/\rho C_p f$). The contribution marked in blue in Fig. 15 corresponds to the fixed part of the thermal resistance ($R_{\text{conv}} + R_{\text{int}} + R_{j-c}$), which is approximately $1.45 \pm$

TABLE V
BREAKDOWN OF THE TOTAL THERMAL RESISTANCE

THERMAL RESISTANCE	R [K/W]	ε [K/W]
Junction to case	R_{j-c}	0.55
Thermal Interface	R_{int}	0.65
Convection	R_{conv}	0.25
Caloric	R_{cal}	$1/\rho C_p f$
Total	R_{total}	$1.45 + 1/\rho C_p f$
		0.086

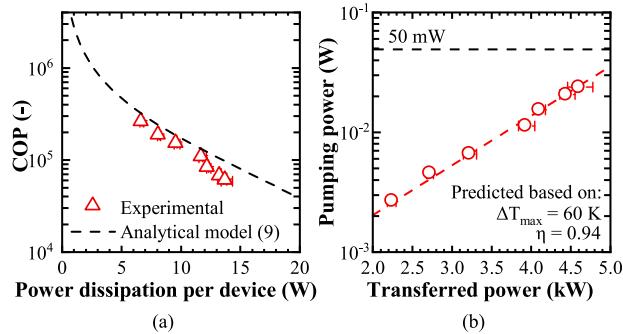


Fig. 16. (a) Comparison of COP versus maximum power dissipation between the predicted COP from (9) and the experimentally derived COP of the fabricated manifold heat sink. (b) Pumping power versus predicted converter output power based on $\Delta T_{max} = 60$ K.

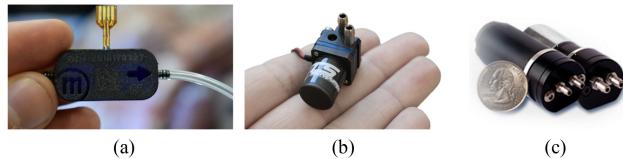


Fig. 17. Representative pumps for selected power ratings. (a) Bartels Mikrotechnik GmbH: 50 mW. (b) TCS Micropumps, Ltd.: 1 W. (c) Flight Works, Inc.: 10 W.

0.086 K/W, which corresponds to the predicted thermal resistance at infinite flow speed. The junction-to-case thermal resistance is provided by the manufacturer (0.55 K/W) and the convective thermal resistance was determined in the section mentioned previously to be approximately 0.25 K/W (see Fig. 11), corresponding to a base-effective heat transfer coefficient of 1.4×10^5 W/m²K. We can now deduce that the interface thermal resistance is approximately 0.65 K/W. All contributions to the total thermal resistance are summed up in Table V.

Fig. 16(a) shows the experimentally obtained COP versus the power dissipation per device for $\Delta T_{max} = 60$ K. The dashed line corresponds to the analytical model of (9). As can be seen, a reasonable correspondence was obtained between the two, thus validating the modeling and optimization approach in Section II. The slightly lower COP at higher power levels can be accounted to a higher pressure drop at high flow rates than predicted by the model (see Fig. 13). Fig. 16(b) shows the required pumping power at different expected loading of the converter based on a 94% efficiency of the converter and assuming an equal distribution of losses. Based on these assumptions, up to 5 kW of transferred power can be delivered while requiring less than 50 mW of pumping power. Fig. 17 shows an overview of commercially available pumps in the low-power range. The high COP and the resulting low pumping power requirements

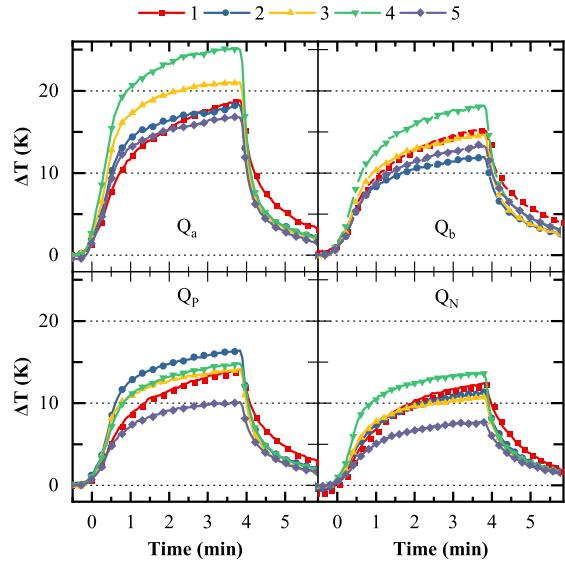


Fig. 18. Transient temperature rises between the device and the coolant inlet temperature at 1 kW transferred power for all 20 transistors.

enable the use of small piezoelectric micropumps, which helps to achieve high system-level power density.

At sufficiently high flow rates, a thermal resistance as low as 1.45 K/W per device could potentially be obtained. For a maximum device temperature rise of 60 K, a predicted 41 W per transistor could be cooled down using this approach, which corresponds to a combined 820 W of losses that can be extracted from this system. If all losses were to be distributed equally over the 20 transistors on a converter with 94% efficiency, this would enable a predicted maximum transferred power of 14 kW. An interesting finding from Table V is that the TIM dominates the thermal resistance, which stresses the importance of improving the thermal interface resistance to achieve a lower R_{total} .

IV. LIQUID COOLED DC-DC CONVERTER

A. Converter Operation

The microchannel cold-plate manifold heat sink was evaluated during the operation of the converter for an output power up to 2.5 kW, while the flow rate was fixed at 1 mL/s. Fig. 18 shows the temperature rise per transistor during the operation of the converter at a loading of 1 kW. Since the total mass of the silicon cold plates is low, the system has small thermal inertia and, thus, steady state is obtained within a few minutes. A large spread in maximum temperature rise was observed among different transistors. At 1 kW, Q_{a4} reached a steady-state temperature rise of 25 K, whereas the temperature rise on Q_{P5} did not surpass 8 K. Fig. 19 shows the steady-state temperature map at 1 kW transferred power. A clear pattern can be seen where the Q_a and Q_b transistors heat up more than the Q_P and Q_N transistors. This is not in agreement with the assumptions from Section III, where all losses were distributed equally over the transistors, as the converter was not designed to have uniform losses. This large spread in temperature can be accounted to the difference between the two types of power devices used and the electrical design of the converter, as well as the uneven stress on the devices due to the selected converter topology [39]. Despite

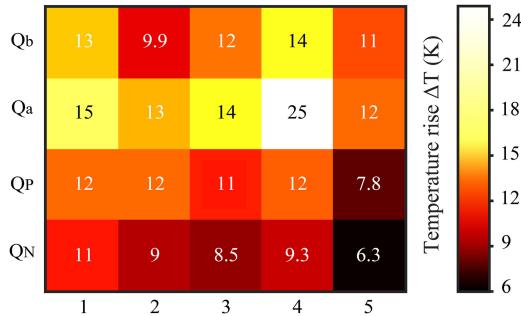


Fig. 19. Temperature map (maximum ΔT between the device temperature and the coolant inlet [K]) of the converter at a transferred power of 1 kW.

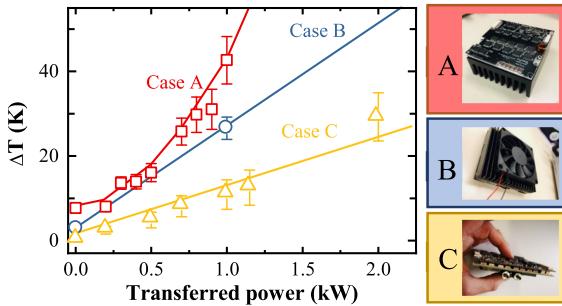


Fig. 20. Temperature rise between the device and the coolant inlet temperature versus converter power for *Case A*: Converter with aluminum heat sink, *Case B*: Converter with heat sink and fan, and *Case C*: Converter with a 3-D-printed microfluidic heat sink. Error bars indicate the standard deviation of all 20 temperatures measured on the converter per data point.

this large temperature spread, the temperature rise of all devices stayed well below the limit of 60 K over the entire range of measured transferred power up to 2.5 kW.

B. Comparison With Conventional Cooling

To compare the thermal performance with conventional heat sinks, we repeated the experiment using a 10 cm \times 10 cm \times 4.5 cm aluminum heat sink on top of the converter with a thermal resistance of 1 K/W at natural convection. Note that this value is 10 \times higher than the thermal resistance of the microfluidic heat sink, whereas its volume is 13 \times larger. This shows that the microfluidic heat sink is 130 \times more volume efficient than conventional heat sinks. Three cases were evaluated, as shown in Fig. 20. In *Case A*, no fan was used; in *Case B*, a fan was added with a flow rate of 1.0 m³/min; and in *Case C*, the 3-D-printed manifold heat sink was evaluated. Fig. 20 shows the average temperature rise for these three scenarios, revealing the much more efficient cooling of the proposed microfluidic heat sink. For a 1 kW of transferred power, *Case A* showed an average temperature rise of 43 K, which was reduced to 26 K in *Case B*, and in *Case C* the average temperature rise was only 10 K. The offset in temperature rise at zero transferred power for *Cases A* and *B* was due to the constant losses in the power supplies that drive the transistors.

Table VI summarizes the volume and thermal resistance of the evaluated designs. The maximum power was calculated using the measured thermal resistances and a maximum temperature rise of 60 K. This extrapolation of converter power is justified since the converter efficiency was constant over the entire range

TABLE VI
DIMENSIONS, PROPERTIES, AND POWER DENSITIES FOR THE
CONSIDERED DESIGNS

Case	V [cm ³]	Measured at 1 kW	Extrapolated for	$\Delta T = 60$ K
		ΔT [K]	Q_{\max} [kW]	ρ_P [kW/l]
A	510	43	1.4	2.7
B	610	26	2.3	3.8
C	200	10	6.0	30

of converter power [39]. As can be seen, by moving from an air-cooled converter to a liquid-cooled converter, the maximum converter power can theoretically be increased from 1.4 to 6 kW, which results in more than tenfold increase in power density ρ_P up to 30 kW/L, revealing the clear benefit of this new cooling technique.

C. Discussion

The microfluidic manifold heat sink can handle higher heat loads in a smaller volume compared with the conventional air-cooled approaches and is, therefore, a promising approach for high power-density application. However, the evaluated converter was not specifically designed to have equal losses over all transistors, causing a large temperature spread as observed in Fig. 19. The single outlier at Q_{a4} limits the maximum power in the current setup, which raises an interesting possibility for design optimization. If the power dissipation per component is known, cold plates with customized geometries can be designed for each transistor to achieve a uniform temperature distribution. Equal temperature distribution can easily be obtained by increasing the number of parallel channels on the devices with high heat loads and by reducing the number of channels on the devices with low heat loads. Changing the number of channels modulates the flow rate at equal pressure drop as well as the effective surface area for heat transfer. Following this approach, heat sinks can be sized in the same way as transistors and passive components to achieve an optimum design, which adds a new layer of coengineering to the design process.

V. CONCLUSION

In this article, we presented a compact microfluidic cooling solution that offers high-performance cooling at low energy consumption, which helps reducing pump size. This cooling system consisted of silicon cold plates with micrometer-sized channels and a manifold that distributes coolants to the hotspots on the PCB. The analytical models demonstrated the importance of optimizing the microchannel size to achieve a high COP. The required manifold channel cross section depends strongly on the selected microchannel width. These findings offer important design guidelines to adapt this technology for practical applications.

Two manifolds have been realized to demonstrate the possibilities of low-cost manufacturing and rapid prototyping. The concept of a microchannel cold plate manifold heat sink was demonstrated on a switched-capacitor dc–dc converter with 20 GaN transistors. Experimental evaluation showed that up to 600 W of dissipated power could be extracted while keeping the junction temperature rise on the transistors below 60 K. By using this microfluidic cooling system, the converter can reach

a power density of 30 kW/cm³ while requiring less than 1 W of pumping power for cooling. This cooling system offers a new design approach, where microchannel cold plates can be selected together with the power devices. We believe that this extra layer of optimization and design flexibility bridges the gap between the electric design and thermal management that helps to increase the power density in future power electronics applications.

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