

Co-designing electronics with microfluidics for more sustainable cooling

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Thermal management is one of the main challenges for the future of electronics^{1–5}. With the ever-increasing rate of data generation and communication, as well as the constant push to reduce the size and costs of industrial converter systems, the power density of electronics has risen⁶. Consequently, cooling, with its enormous energy and water consumption, has an increasingly large environmental impact^{7,8}, and new technologies are needed to extract the heat in a more sustainable way—that is, requiring less water and energy⁹. Embedding liquid cooling directly inside the chip is a promising approach for more efficient thermal management^{5,10,11}. However, even in state-of-the-art approaches, the electronics and cooling are treated separately, leaving the full energy-saving potential of embedded cooling untapped. Here we show that by co-designing microfluidics and electronics within the same semiconductor substrate we can produce a monolithically integrated manifold microchannel cooling structure with efficiency beyond what is currently available. Our results show that heat fluxes exceeding 1.7 kilowatts per square centimetre can be extracted using only 0.57 watts per square centimetre of pumping power. We observed an unprecedented coefficient of performance (exceeding 10,000) for single-phase water-cooling of heat fluxes exceeding 1 kilowatt per square centimetre, corresponding to a 50-fold increase compared to straight microchannels, as well as a very high average Nusselt number of 16. The proposed cooling technology should enable further miniaturization of electronics, potentially extending Moore’s law and greatly reducing the energy consumption in cooling of electronics. Furthermore, by removing the need for large external heat sinks, this approach should enable the realization of very compact power converters integrated on a single chip.

In the USA alone, data centres consume 24 TWh of electricity and 100 billion litres of water to satisfy their cooling demands⁸, corresponding to the residential needs of a city of the size of Philadelphia^{12–14}. The environmental impact of this information technology infrastructure is expected to increase dramatically⁹, for example, accounting for up to 31% of Ireland’s electricity demand by 2027 (ref. ¹⁵), in large part due to the power consumption of cooling systems. This development is accompanied by the constant push to shrink the size of semiconductor devices, which results in higher heat fluxes that become increasingly challenging to extract and require new cooling solutions. A similar need is observed in power electronics, as the electrification of our society demands more powerful, more efficient and smaller energy conversion systems. Wide-bandgap semiconductors, such as gallium nitride (GaN), are promising candidates for this purpose¹⁶. These materials enable much smaller dies than those of traditional semiconductors as well as the monolithic integration of power devices, supporting the miniaturization of complete power converters into a single chip¹⁷. However, to unlock the full potential of GaN, strategies for sustainable cooling of high-heat-flux applications are required.

Substantial research efforts have focused on improving the thermal path between the hotspot and the coolant. However, heat extraction

capability is fundamentally limited by the thermal resistance between the semiconductor die and packaging. Furthermore, relying on large heat sinks reduces the power density and hinders integration, since devices cannot be densely packed. Bringing the coolant in direct contact with the device may be a way to overcome this limiting factor, for example, by impinging coolant on a bare die¹⁸ or by etching micrometre-sized channels directly inside the device to turn the substrate into a heat sink. The latter technique demonstrated state-of-the-art cooling performance due to the highly efficient heat transfer at the microscale^{19–21}. The high pressure drop and large temperature gradients associated with these straight, parallel microchannels (SPMCs) were overcome by splitting the flow into multiple parallel sections, and distributing the coolant over these channels using manifolds²². Early investigations^{23–26} and systematic numerical studies^{27–30} of manifold microchannel (MMC) heat sinks showed a large reduction in pumping power requirements and thermal resistance compared to SPMCs. Excellent heat extraction has been demonstrated with copper MMCs³¹, compact micro-fabricated multilayer silicon structures^{32–35} and by using additive manufacturing^{36,37}. However, in all these approaches, the heat sink and electronic structure and fabrication process are considered separately, either by integrating a simple resistive heater functioning as the heat source, or

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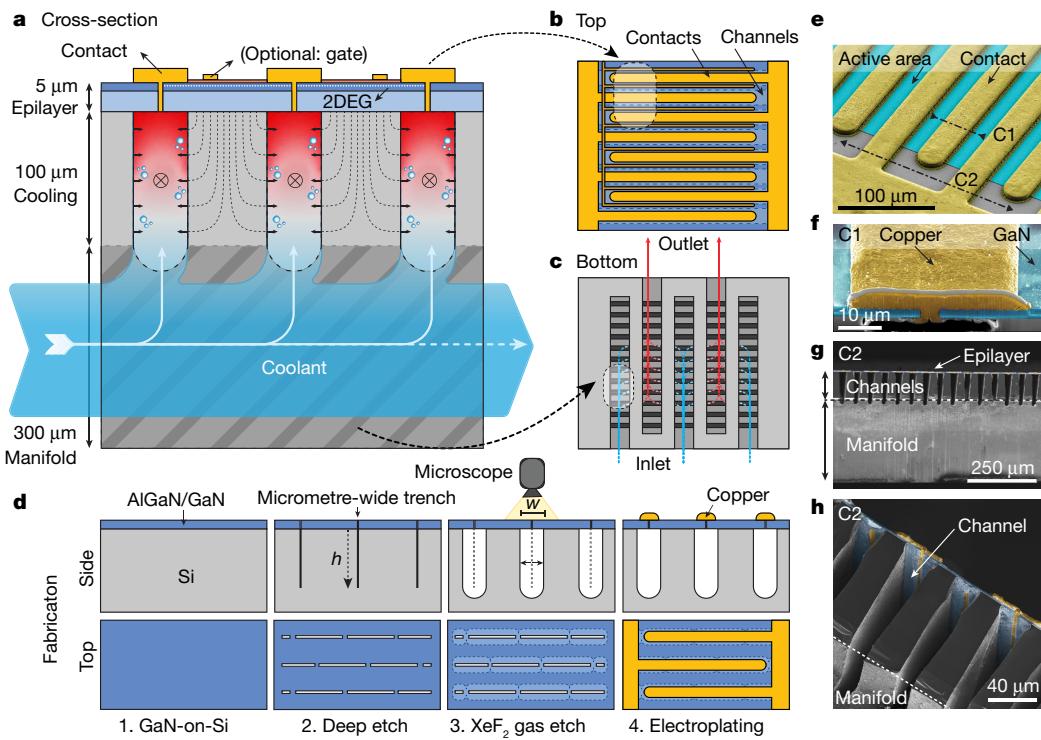


Fig. 1 | Co-designed microfluidically cooled electric device. **a**, Schematic of the device structure, in which the AlGaN/GaN epilayer provides the electronic functions and the silicon functions as cooling and fluid distribution manifold. Metal contacts seal the buried microchannels embedded underneath. Coolant coming from the manifolds flows in the out-of-plane orientation inside the microchannels to remove heat from the device. **b**, Top view of the co-designed device structure: each contact is aligned and seals the buried channel in a scaled-up multi-finger structure. **c**, Bottom view of the co-designed device structure: the manifold structure distributes the flow over the microchannels. **d**, Summary of the proposed cooling method: a staggered pattern of narrow high-aspect-ratio slits is

first etched through the AlGaN/GaN epilayer into the silicon. Next, an isotropic gas etch widens the channels in the silicon, coalescing under the epilayer. The openings in the epilayer are then sealed using electroplating. **e**, SEM image of the AlGaN/GaN surface after sealing the microchannels. Contact pads hermetically seal the incisions in the AlGaN/GaN epilayer. **f**, Cross-sectional SEM image along C1, showing the incision in the epilayer sealed with electroplated copper. **g**, Cross-sectional SEM image along C2, showing an array of buried microchannels, as well as a sidewall of the perpendicular manifold channel. **h**, Close-up of the cross-sectional image along C2, showing the exposed microchannel below the electroplated-copper sealing layer.

by bonding the MMC structure to a commercial device³⁸. This leaves the large potential of MMCs untapped. Improving the thermal coupling between the heat source and cooling has been investigated for hotspot mitigation^{39–41}, but has remained unexplored in a complete device structure. Furthermore, despite much MMC heat sink research, the increasing complexity and associated reliability concerns caused by the multiple bonded layers required for coolant delivery have prevented the adoption of MMCs in commercial devices.

In this work, we address these concerns by combining cooling and device design, using an approach in which a MMC heat sink is designed and fabricated in conjunction with the electronics. We present a monolithically integrated manifold microchannel (mMMC) heat sink in a single-crystalline silicon substrate with an epilayer, produced without the need for cumbersome bonding steps. Here the device design and heat-sink fabrication are combined within the same process, with buried cooling channels embedded directly below the active area of the chip. Coolant thus impinging directly on the heat sources provides local and efficient heat extraction (Fig. 1a). On the back of this same substrate, manifold channels spread the liquid over the die (Fig. 1c) to obtain high temperature uniformity and low pressure drop, leading to a very low pumping-power consumption and vastly improved cooling performance. Since the electronics and microfluidics are fully coupled and aligned (Fig. 1b), we call this approach microfluidic-electronic co-design. We demonstrated microfluidic-electronic co-design on GaN-on-Si, a low-cost platform that is promising for realizing high-power converters on a chip, comprising a GaN epilayer a few micrometres thick on a low-cost silicon substrate. The passive

silicon substrate typically lacks functionality, but by turning it into an active cooling layer, it has the potential to extract extreme heat fluxes, without requiring the added cost of high-thermal-conductivity substrates. Our results show that considering cooling as an integral part of device design can result in orders-of-magnitude improvements in cooling performance. We use this embedded-cooling approach to demonstrate a super-compact GaN-on-silicon integrated alternating-direct current (a.c.–d.c.) converter, containing four power devices on the same microfluidic-cooled chip, and yielding a power density of 25 kW dm^{-3} . A simple multi-layered printed circuit board (PCB) was designed to direct the coolant flow into the semiconductor device.

Co-design concept and fabrication

Our co-design approach, in which each heat source is coupled to an individual buried cooling-channel serving as a local heat sink, is particularly of interest in GaN power electronic applications with a lateral high-electron-mobility transistor (HEMT) structure. Typical source-drain spacing for HEMTs in >1-kV applications matches the optimum dimensions for microchannel cooling of about $20 \mu\text{m}$ (refs. ^{19,42–44}). Therefore, we investigated a GaN-on-Si device structure in which liquid impinges directly onto the epilayer below each contact, ensuring minimum thermal resistance between the hotspot and coolant. In this structure (Fig. 1a), the GaN epilayer provides the power electronics (Fig. 1b), and the silicon functions as a microchannel cooling and fluid-distribution network in a three-dimensional arrangement

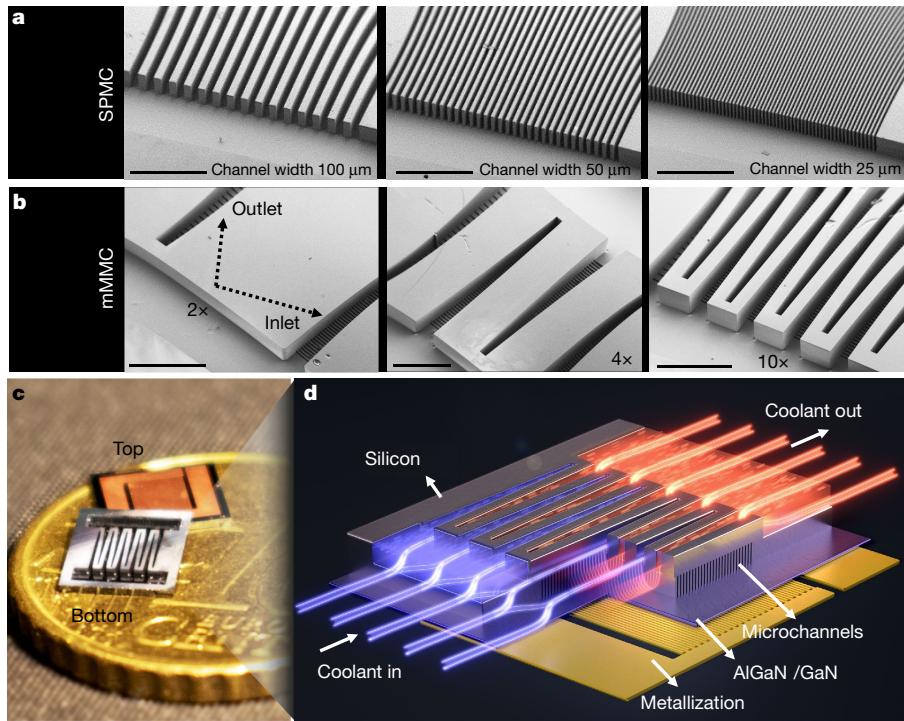


Fig. 2 | Microchannel cooling configurations. **a**, SEM images of the back side of the silicon substrate with SPMCs. Microchannel widths are 100 μm , 50 μm and 25 μm and the scale bars represent 1 mm. **b**, SEM images of the back side of the silicon substrate with mMMCs, with 2 \times -, 4 \times - and 10 \times -manifold sections. Scale bars represent 850 μm . **c**, Picture of the co-designed devices, from the top and bottom sides, with the 10 \times -manifold mMMC cooling. The top side

shows the electronic structure and the bottom shows the manifold etched in the silicon substrate. **d**, Illustration of the fluid flow through the mMMC structure. Blue lines indicate the cold coolant entering the chip, and red lines indicate the hot coolant leaving the chip. The Supplementary Video that visualizes the fluid flow and the three-dimensional render in Fig. 2d were produced by Vytautas Navikas and used with permission.

(Fig. 1c). Figure 1d illustrates the corresponding fabrication method. A staggered pattern of slits was formed in the Si by anisotropic deep etching through narrow incisions in the AlGaN/GaN epilayer to achieve the desired microchannel depth. This pattern provided better structural integrity of the epilayer during fabrication compared to continuous slits. During the subsequent isotropic gas-etch, the channels widened and coalesced in the silicon substrate, while being monitored through the transparent GaN epilayer using an *in situ* optical etch-rate tracking. This two-step etching process provides independent control over channel width and depth, making it suitable to a wide range of contact pitches. The incisions were finally hermetically sealed during the device metallization step. The Methods and Extended Data Fig. 1 explain the fabrication procedure in detail. Figure 1e shows a scanning electron microscope (SEM) image of the device after the metallization step with sealed channels. Because of the narrow incisions in the epilayer, the contacts do not require substantial oversizing. The microchannels are in direct contact with the active area of the chip, thus providing excellent thermal coupling between the hotspot and the cooling channel (Fig. 1f). Through micrometre-sized openings in the epilayer, 125- μm -deep and 20- μm -wide channels were created in the silicon substrate (Fig. 1g, h).

A series of devices was fabricated with SPMCs with equal width and spacing of 100 μm , 50 μm and 25 μm , and a channel depth of 250 μm in GaN-on-Si power devices, functioning as reference heat sinks (Fig. 2a) for evaluating the performance of the co-designed electronic-microfluidic mMMC devices. Three mMMC chips with 2, 4 and 10 inlet and outlet manifold channels and identical 20 \times 125 μm microchannels were fabricated, referred to as the 2 \times -, 4 \times - and 10 \times -manifold chips (Fig. 2b). Figure 2c shows a picture of the mMMC device with the 10 \times -manifold, including a schematic (Fig. 2d) to illustrate the flow path with coolant impinging directly onto the bottom of the GaN epilayer.

Thermo-hydraulic evaluation

A thermo-hydraulic analysis, using de-ionized water as a coolant, was performed on the cooling structures (Fig. 2a, b) to assess the cooling performance by measuring the thermal resistance, pressure drop and the resulting cooling coefficient of performance (COP), which indicates the energy efficiency of the heat sink. Figure 3a shows the total thermal resistance (R_{total}) between the surface temperature rise and the inlet temperature for the evaluated structures. By reducing the SPMC channel dimensions from 100 μm to 25 μm at identical flow rates, R_{total} reduces, which can be attributed to the increased surface area for heat transfer. However, the 4 \times - and 10 \times -manifold heat sinks show an additional substantial reduction in R_{total} compared to the 25- μm SPMC, approaching the limit of single-phase water-cooling (defined by its heat capacity). R_{total} was separated into three components: the contribution due to the heating of the water based on its heat capacity (R_{heat}), the contribution due to convective heat transfer in the microchannels (R_{conv}), and the contribution due to conduction (R_{cond}). The full data reduction procedure to obtain these values is explained in the Methods and in Extended Data Fig. 3. A breakdown of R_{total} is shown in Fig. 3b, revealing a strong relation between R_{conv} and microchannel size, where smaller channels reduce R_{conv} . A large decrease in R_{conv} was achieved with the 10 \times -manifold, resulting in an 85% and 76% reduction compared to the 50- μm and 100- μm -wide SPMCs, respectively. In combination with a very low R_{cond} for the co-designed manifolds, at a flow rate of 1.0 ml s^{-1} , a thermal resistance of 0.43 K W^{-1} was achieved. The 10 \times -manifold design thus allows heat fluxes up to 1,723 W cm^{-2} for a maximum temperature rise of 60 K, which is more than twice that of a 25- μm -wide SPMC.

Narrow channels, however, require a higher pressure to achieve equal flow rate (Fig. 3c). For a flow rate of 0.5 ml s^{-1} , SPMC widths of 100 μm , 50 μm and 25 μm require pressures of 160 mbar, 260 mbar

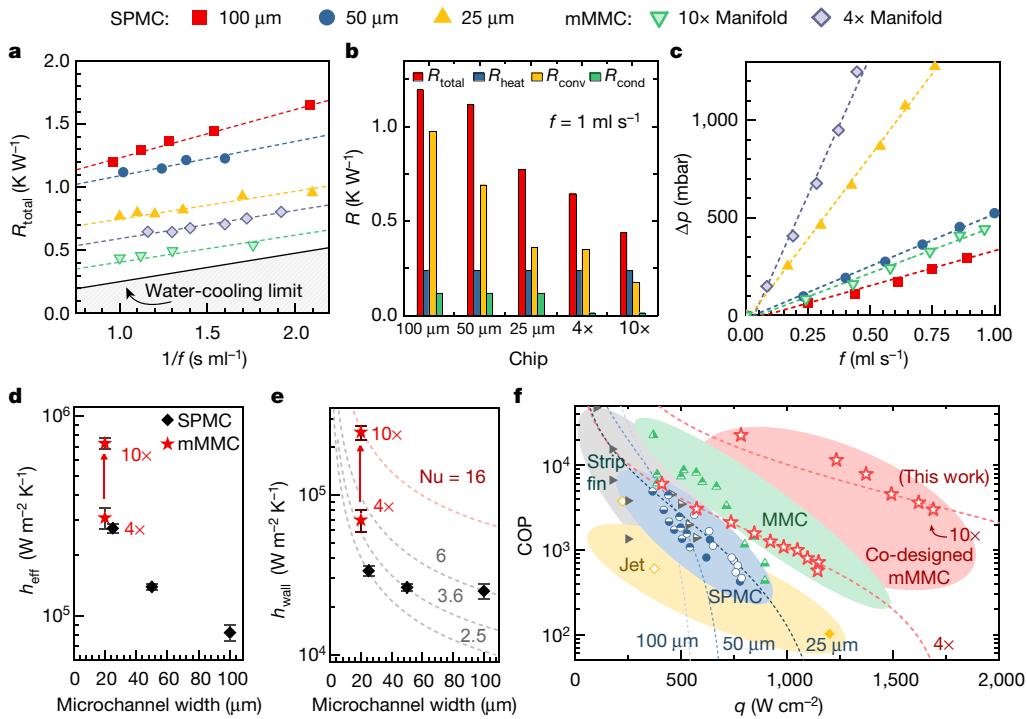


Fig. 3 | Thermo-hydraulic evaluation of the cooling strategies. **a**, Total thermal resistance R_{total} between the surface temperature and the inlet temperature of the coolant. The black line indicates the lower limit of thermal resistance for single-phase water cooling, determined by its heat capacity. **b**, Breakdown of the contributions of R_{total} into R_{heat} , R_{conv} and R_{cond} , for all devices evaluated. **c**, Pressure drop Δp versus flow rate f for the considered microchannel structures. The 4x- and 10x-manifold had 20-μm-wide channels. **d**, Effective (base-area averaged) heat-transfer coefficient h_{eff} for straight (SPMC) and manifold (mMMC) structures. Error bars indicate the standard deviation in the heat-transfer coefficient due to averaging of R_{conv} over the measured range of flow rates. **e**, Wall-averaged heat-transfer coefficient h_{wall} for straight and

manifold microchannels. A 4.4-fold increase in Nusselt number was observed between the 4x- and 10x-manifold. **f**, Benchmark of the experimentally demonstrated COP versus the maximum heat flux q for a temperature rise of 60 K. Shown are the SPMC (blue), the MMC (green), the impinging jet (yellow), the strip fin (grey) and the mMMC (red). More extensive benchmarking with simulation and analytical results, full references and further classification is provided in Extended Data Fig. 6 and Extended Data Table 2. A large improvement in COP for a given heat flux is achieved with our proposed mMMC structures (red). Dashed lines are models for COP versus heat flux, under the assumption of a constant heat-transfer coefficient and a linear pressure-flowrate relation, fitted through the experimental data.

and 810 mbar, respectively. The manifold structure substantially lowers the pressure drop by reducing the length of the flow path through the microchannel. When splitting the flow into smaller sections with the 10x-manifold, the pressure drop reduced to just 210 mbar. This highlights the benefit of the MMC structure: a lower thermal resistance than SPMCs can be obtained at a reduced pumping power consumption. However, although the manifold structure can reduce the pressure drop, the additional contractions and turns of the fluid can hinder this reduction. For example, 20-μm-wide microchannels in a 4x-manifold require a higher pressure of 1,300 mbar compared to the 25-μm-wide SPMC, which in part can also be attributed to the higher fluid velocity given that the mMMC channels (125 μm) are not as deep as in the SPMC (250 μm). These findings demonstrate the need for a carefully optimized geometry of the microchannel and manifold.

Figure 3d shows a clear trend for SPMCs of increased effective base-area-averaged heat-transfer coefficient (h_{eff}) for smaller microchannels. This is due to the combined effect of the increased surface area and local heat-transfer coefficient in the fully developed laminar-flow regime. The co-designed 4x-mMMC structures matches this trend with $h_{\text{eff}} = 3.1 \times 10^5 \text{ W m}^{-2} \text{ K}^{-1}$, but a large deviation from this pattern is observed when the effective length through which the coolant flows in the microchannel is reduced. For the 10x-manifold, h_{eff} more than doubles to $7.3 \times 10^5 \text{ W m}^{-2} \text{ K}^{-1}$, a rise that can be attributed to the high Nusselt number owing to the developing flow in the MMC structure^{27,45}. This effect becomes more pronounced when considering the wall-area-averaged heat-transfer coefficient (h_{wall}) (Fig. 3e), which eliminates the contribution of the increased surface area from

the heat-transfer coefficient, as well as accounts for the limited fin efficiency of the channels. Over a threefold increase in h_{wall} is observed between 25-μm-wide straight microchannels and the 10x-manifold heat sinks, up to $2.4 \times 10^5 \text{ W m}^{-2} \text{ K}^{-1}$. This value corresponds to a very high Nusselt number of 16, generally only achieved in larger-scale systems, or in more complex two-phase cooling systems, highlighting the superior thermal performance of this structure.

The combination of improved heat transfer and reduced pressure drop leads to much lower pumping power requirements. The cooling COP is defined as the ratio of extracted power to the pumping power required to provide such a level of cooling, while maintaining a maximum surface temperature rise of 60 K. Higher heat fluxes require higher flow rates, reducing the COP owing to the larger pumping power required. Figure 3f benchmarks the evaluated devices, along with other technologies found in the literature. For SPMC, channel widths of 100 μm, 50 μm and 25 μm show a consecutively higher COP for higher heat fluxes, with a COP in the range between 10^2 and 10^4 and heat fluxes between 350 W cm^{-2} and 800 W cm^{-2} . The 10x-manifold device vastly outperforms these SPMCs. At an identical COP of 5.0×10^3 , the 10x-manifold can sustain heat fluxes up to 1.7 kW cm^{-2} at 1.0 ml s^{-1} , compared to 400 W cm^{-2} , 450 W cm^{-2} and 550 W cm^{-2} for the 100-μm, 50-μm and 25-μm SPMCs, respectively. Furthermore, at a heat flux of 780 W cm^{-2} , the 10x-manifold provides a 50-fold increase in COP with respect to 25-μm SPMCs. Compared to MMC heat sinks presented in the literature, the proposed mMMC device outperforms the current state of the art, and demonstrates a large potential for energy-efficient cooling by having a thermal-centred approach in the device design.

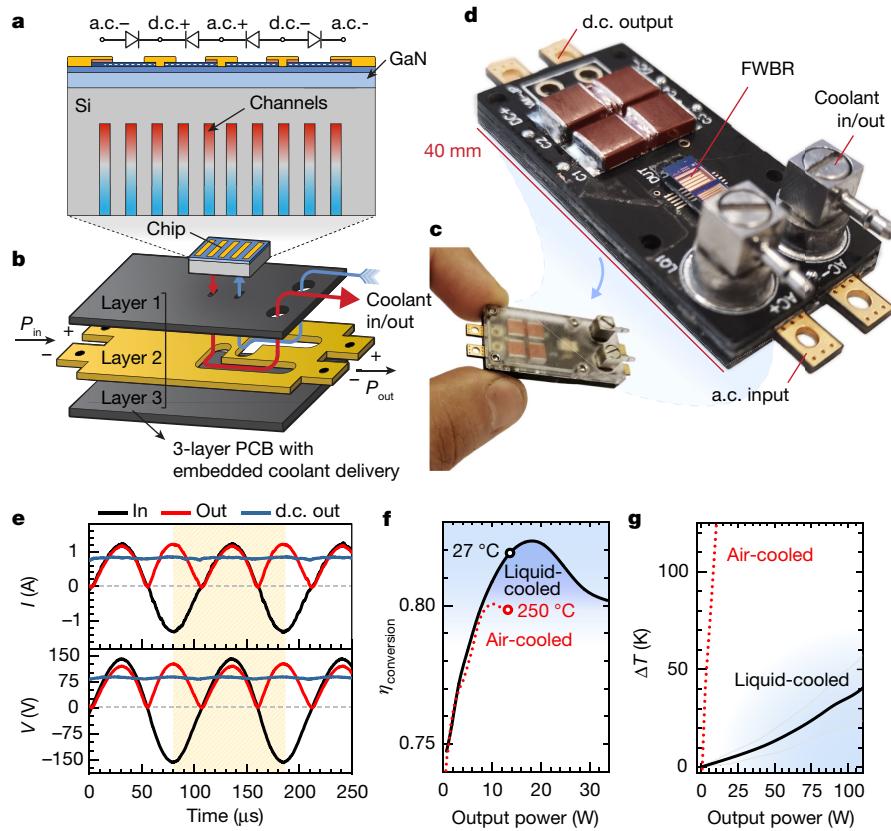


Fig. 4 | a.c.-d.c. converter with embedded liquid cooled GaN power integrated circuit.

a, Schematic illustration of the super-compact liquid-cooled power integrated circuit based on four GaN power Schottky barrier diodes integrated in a single chip in a full-bridge configuration.

b, A PCB-embedded coolant delivery was developed to feed the coolant to the device. The PCB consists of three layers, where the middle layer contains a fluid distribution channel. **c**, Photograph (taken by R.v.E.) of the full 120-W a.c.-d.c. converter with coolant delivery to the liquid-cooled power integrated circuit.

d, Converter without encapsulation, revealing the monolithically integrated full-wave bridge rectifier (FWBR) integrated circuit. **e**, Rectification waveforms

of the converter, 150-V a.c. input (black) and output before (red) and after (blue) filtering using output capacitors. **f**, Efficiency versus output power for the air-cooled and liquid-cooled a.c.-d.c. converter. At identical output power, the liquid-cooled converter exhibits substantially higher efficiency owing to the elimination of self-heating degradation. **g**, Temperature rise versus output power, showing a much higher temperature rise at equal output power for the air-cooled device compared to the embedded liquid cooling, which causes a large self-heating degradation. The black line shows the mean surface-temperature rise and the highlighted area shows the range between the minimum and maximum temperatures over the device's surface.

Power integrated circuit with embedded cooling

The lateral nature of AlGaN/GaN electronics enables the monolithic integration of multiple power devices onto a single substrate. This opens up opportunities for power electronics, whereby an entire converter can be integrated on a small chip, with large potential for energy, cost and space savings. However, the resulting high heat fluxes limit the maximum output power of the chip. To demonstrate the potential of embedded cooling in a semiconductor device, we monolithically integrated a full-bridge rectifier onto a single GaN-on-Si die. Rectification was provided using four high-performance tri-anode Schottky barrier diodes with a breakdown voltage of 1.2 kV and high-frequency capability up to 5 MHz (ref. ⁴⁶). 50-μm-wide cooling channels were integrated on the silicon substrate (Fig. 4a). To fully benefit from the compactness of high-performance microchannel cooling, a three-layer PCB with embedded coolant delivery channels was developed and used to guide the coolant to the device (Fig. 4b). The full fabrication of this monolithically integrated power device and the PCB is described in the Methods and shown in Extended Data Fig. 8. The device was finally fluidically connected to the PCB using laser-cut liquid- and solvent-resistant double-sided adhesive, providing a leak-proof connection. This method is low-cost and easy-to-prototype, and translates well to conventional solder bonding. Figure 4c, d shows the converter implemented, with a very compact form factor, rectifying an a.c. signal

with peak voltage and current of 150 V and 1.2 A, respectively (Fig. 4e). Integrated liquid cooling led to a small temperature rise of 0.34 K per watt of output power. For a maximum temperature rise of 60 K, this single die can thus produce an output power of 176 W at a flow rate of only 0.8 ml s⁻¹. Furthermore, the reduced operating temperature led to an increased conversion efficiency (Fig. 4f) by eliminating self-heating degradation from the electrical performance. The a.c.-d.c. converter was experimentally evaluated up to 120 W of output power, while the temperature rise stayed below 50 K (Fig. 4g). Considering the small converter volume (4.8 cm³), this corresponds to a high power density of 25 kW dm⁻³. Moreover, since all cooling occurs within its footprint, multiple devices can be densely packed onto the same PCB to increase the output power. This is a clear benefit over conventional heat sinks relying on heat spreading to large areas. These results show that the proposed high-performance cooling approach can enable the realization of high-power (kilowatt range) converters of the size of USB sticks in the foreseeable future.

Discussion and outlook

We present an approach for co-designing microfluidics and electronics for energy-efficient cooling, and demonstrate it on GaN-on-Si power devices by turning the passive silicon substrate from a low-cost carrier into a high-performance heat sink. COP values above 10,000 for heat

fluxes surpassing 1 kW cm^{-2} could be obtained by focusing on cooling in an early stage of the device design. As a practical implication, the average added-energy expenditure of more than 30% for cooling in data centres could potentially drop below 0.01% by adopting this design approach. The entire mMMC cooling structure can be monolithically integrated within the substrate, requiring only conventional fabrication procedures, thus making this economically viable. To realize this concept, solutions for the packaging and interconnects are required. The PCB-based fluid delivery presented provides an example of a way to use these co-designed chips, based on components familiar to the electronics designer. This means that, in order to provide maximum energy savings, cooling should be an integral step in the entire electronic design chain, from the device to the PCB design, and not merely an afterthought. If these practicalities can be addressed, we anticipate that the co-design of microfluidic and electronics will be appropriate for energy-efficient thermally-aware electronics design. This may aid in solving critical challenges in electronics applications, as well as enabling future integrated power converters on a chip to support the electrification of our society in a sustainable manner.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at <https://doi.org/10.1038/s41586-020-2666-1>.

1. Haensch, W. et al. Silicon CMOS devices beyond scaling. *IBM J. Res. Develop.* **50**, 339–361 (2006).
2. Kanduri, A. et al. A perspective on dark silicon. In *The Dark Side of Silicon: Energy Efficient Computing in the Dark Silicon Era* 3–20 (Springer, 2017).
3. Hardavellas, N., Ferdinand, M., Falsafi, B. & Ailamaki, A. Toward dark silicon in servers. *IEEE Micro* **31**, 6–15 (2011).
4. Nowak, E. J. Maintaining the benefits of CMOS scaling when scaling bogs down. *IBM J. Res. Develop.* **46**, 169–180 (2002).
5. Garimella, S. V. et al. Thermal challenges in next-generation electronic systems. *IEEE Trans. Compon. Packag. Technol.* **31**, 801–815 (2008).
6. Ohashi, H. Recent power devices trend. *J. Inst. Electr. Eng. Jpn* **122**, 168–171 (2002).
7. Digitalization And Energy 103–122 (International Energy Agency, 2017).
8. Shehabi, A. et al. United States Data Center Energy Usage Report LBNL-1005775 <https://www.osti.gov/biblio/1372902> (US DOE, Office of Scientific and Technical Information, 2016).
9. Jones, N. How to stop data centres from gobbling up the world's electricity. *Nature* **561**, 163–166 (2018).
10. Agostini, B. et al. State of the art of high heat flux cooling technologies. *Heat Transf. Eng.* **28**, 258–281 (2007).
11. Chu, R. C., Simons, R. E., Ellsworth, M. J., Schmidt, R. R. & Cozzolino, V. Review of cooling technologies for computer products. In *IEEE Transactions on Device and Materials Reliability* Vol. 4, 568–585 (IEEE, 2004).
12. 2015 Residential Energy Consumption Survey (RECS) <https://www.eia.gov/consumption/residential/data/2015/> (US Energy Information Administration, 2015).
13. DeOreo, W. B., Mayer, P., Dziegielewski, B. & Kiefer, J. Residential End Uses of Water Version 2 <https://www.waterrf.org/resource/residential-end-uses-water-version-2> (Water Research Foundation, 2016).
14. Annual Estimates of the Resident Population for Incorporated Places of 50,000 or More, Ranked by July 1, 2018 Population: April 1, 2010 to July 1, 2018 <https://www.census.gov/data/tables/time-series/demo/popest/2010s-total-cities-and-towns.html> (United States Census Bureau, 2019).
15. All-Island Generation Capacity Statement 2018–2027 http://www.soni.ltd.uk/media/documents/Generation_Capacity_Statement_2018.pdf (EirGrid Group, 2018).
16. Amano, H. et al. The 2018 GaN power electronics roadmap. *J. Phys. D* **51**, 163001 (2018).
17. Ohashi, H. et al. Power electronics innovation with next generation advanced power devices. *IEICE Trans. Commun.* **E87-B**, 3422–3429 (2004).
18. Wei, T. et al. High-efficiency polymer-based direct multi-jet impingement cooling solution for high-power devices. *IEEE Trans. Power Electron.* **34**, 6601–6612 (2019).
19. Tuckerman, D. B. & Pease, R. F. W. High-performance heat sinking for VLSI. *IEEE Electron Device Lett.* **2**, 126–129 (1981).
20. Mundinger, D. et al. Demonstration of high-performance silicon microchannel heat exchangers for laser diode array cooling. *Appl. Phys. Lett.* **53**, 1030–1032 (1988).
21. Phillips, R. J. Microchannel heat sinks. *Lincoln Lab. J.* **1**, 31–48 (1988).
22. Harpole, G. M. & Eninger, J. E. Micro-channel heat exchanger optimization. In *1991 Proc. Seventh IEEE Semiconductor Thermal Measurement and Management Symp.* 59–63 (IEEE, 1991).
23. Copeland, D., Behnia, M. & Nakayama, W. Manifold microchannel heat sinks: isothermal analysis. *IEEE Trans. Compon. Packag. Manuf. Technol.* **20**, 96–102 (1997).
24. Copeland, D., Takahira, H., Nakayama, W. & Pak, B. C. Manifold microchannel heat sinks: theory and experiment. In *Advances in Electronic Packaging Proc. Int. Intersociety Electronic Packaging Conference (INTERPACK '95)* Vol. 10-2, 829–835, https://library.epfl.ch/beast?record=ebi01_prod001476708 (American Society of Mechanical Engineers, Electrical and Electronics Packaging Division, 1995).
25. Copeland, D. Manifold microchannel heat sinks: numerical analysis. In *Cooling and Thermal Design of Electronic Systems 1995 ASME International Mechanical Engineering Cong. Exp.* Vol. 16, 111–116, https://library.epfl.ch/beast?record=ebi01_prod001583961 (American Society of Mechanical Engineers, Electrical and Electronics Packaging Division, 1995).
26. Copeland, D., Behnia, M. & Nakayama, W. Manifold microchannel heat sinks: conjugate and extended models. *Int. J. Microelectron. Packag. Mater. Technol.* **1**, 139–152 (1998).
27. Mandel, R., Shooshtari, A. & Ohadi, M. A 2.5-D' modeling approach for single-phase flow and heat transfer in manifold microchannels. *Int. J. Heat Mass Transf.* **126**, 317–330 (2018).
28. Ng, E. Y. K. & Poh, S. T. Investigative study of manifold microchannel heat sinks for electronic cooling design. *J. Electron. Manuf.* **9**, 155–166 (1999).
29. Ryu, J. H., Choi, D. H. & Kim, S. J. Three-dimensional numerical optimization of a manifold microchannel heat sink. *Int. J. Heat Mass Transf.* **46**, 1553–1562 (2003).
30. Sarangi, S., Bodla, K. K., Garimella, S. V. & Murthy, J. Y. Manifold microchannel heat sink design using optimization under uncertainty. *Int. J. Heat Mass Transf.* **69**, 92–105 (2014).
31. Cetegen, E., Dessiatoun, S. & Ohadi, M. Heat transfer analysis of force fed evaporation on microgrooved surfaces. In *Proc. 6th Int. Conf. on Nanochannels, Microchannels, and Minichannels (ICNMM2008)* Part A, 657–660, <https://asmedigitalcollection.asme.org/ICNMM/proceedings-abstract/ICNMM2008/48345/657/335936> (2008).
32. Kermani, E., Dessiatoun, S., Shooshtari, A. & Ohadi, M. M. Experimental investigation of heat transfer performance of a manifold microchannel heat sink for cooling of concentrated solar cells. In *Proc. Electronic Components and Technology Conf.* 453–459, <https://ieeexplore.ieee.org/document/5074053> (IEEE, 2009).
33. Drummond, K. P. et al. A hierarchical manifold microchannel heat sink array for high-heat-flux two-phase cooling of electronics. *Int. J. Heat Mass Transf.* **117**, 319–330 (2018).
34. Back, D. et al. Design, fabrication, and characterization of a compact hierarchical manifold microchannel heat sink array for two-phase cooling. *IEEE Trans. Compon. Packag. Manuf. Technol.* **9**, 1291–1300 (2019).
35. Escher, W., Brunschwiler, T., Michel, B. & Poulikakos, D. Experimental investigation of an ultrathin manifold microchannel heat sink for liquid-cooled chips. *J. Heat Transfer* **132**, 081402 (2010).
36. Schlotting, G. et al. Lid-integral cold-plate topology: integration, performance, and reliability. *J. Electron. Packag.* **138**, 010906 (2016).
37. Robinson, A. J., Kempers, R., Colenbrander, J., Bushnell, N. & Chen, R. A single phase hybrid micro heat sink using impinging micro-jet arrays and microchannels. *Appl. Therm. Eng.* **136**, 408–418 (2018).
38. Everhart, L. et al. Manifold microchannel cooler for direct backside liquid cooling of SiC power devices. In *ASME 5th Int. Conf. on Nanochannels, Microchannels, and Minichannels* 285–292 (ASME, 2007).
39. Gambin, V. et al. Impingement cooled embedded diamond multiphysics co-design. In *2016 15th IEEE Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM) 1518–1529* (IEEE, 2016).
40. Drummond, K. P. et al. Evaporative intrachip hotspot cooling with a hierarchical manifold microchannel heat sink array. In *2016 15th IEEE Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM) 307–315* (IEEE, 2016).
41. Shekhar Sharma, C. et al. Energy efficient hotspot-targeted embedded liquid cooling of electronics. *Appl. Energy* **138**, 414–422 (2015).
42. Samalav, V. K. Convective heat transfer in microchannels. *J. Electron. Mater.* **18**, 611–617 (1989).
43. Weisberg, A., Bau, H. H. & Zemel, J. N. Analysis of microchannels for integrated cooling. *Int. J. Heat Mass Transf.* **35**, 2465–2474 (1992).
44. Ryu, J. H., Choi, D. H. & Kim, S. J. Numerical optimization of the thermal performance of a microchannel heat sink. *Int. J. Heat Mass Transf.* **45**, 2823–2827 (2002).
45. Shah, R. K. & London, A. L. *Laminar Flow Forced Convection In Ducts : A Source Book For Compact Heat Exchanger Analytical Data* (Academic Press, 1978).
46. Neta, L., Kampitsis, G., Ma, J. & Matioli, E. Fast-switching tri-anode Schottky barrier diodes for monolithically integrated GaN-on-Si power circuits. *IEEE Electron Device Lett.* **41**, 99–102 (2019).

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Methods

Device fabrication process

The fabrication process of the co-designed microfluidic-electronic device is shown in Extended Data Fig. 1. Fabrication started with an AlGaN/GaN-on-silicon wafer with, from top to bottom: 2.9-nm-thick GaN cap layer, 20-nm-thick AlGaN barrier, 420-nm-thick GaN channel, 4.2- μm -thick buffer layer, on a 400- μm -thick silicon layer. First, a mesa was etched to define the active area of the chip, followed by a 1- μm -thick plasma-enhanced chemical vapour deposition of SiO₂ as an etching mask to obtain sharp sidewalls after GaN etching. Photoresist was lithographically patterned on top of the SiO₂ layer, to define and open a staggered pattern of slits in the SiO₂ mask with inductively coupled plasma etching using C₄F₈ chemistry. The staggered pattern, with 30- μm -long slits spaced 2 μm apart, prevented the epilayer from turning into a fragile cantilever after performing an undercut in the silicon substrate. Instead, the 2 μm spacing between each slit kept the epilayer together, resulting in good mechanical integrity of the epilayer during the fabrication process. The photoresist was stripped using an O₂ plasma and the exposed GaN slits were consecutively etched using Cl₂+Ar chemistry until the silicon substrate was reached, which was confirmed using end-point detection. The chips were then dipped into 40% KOH at 60 °C for 5 min to remove any remaining AlN-based material from the buffer^{47,48}. The Bosch process was used to etch the silicon slits approximately 115 μm deep, resulting in high-aspect-ratio slits. The microchannels in silicon were widened using an isotropic XeF₂ gas etch, which provided selectivity over GaN⁴⁹. XeF₂ gas etching was performed in a pulsed manner: the sample was exposed to XeF₂ at a controlled pressure (1.33 mbar) for 30 s, followed by evacuation of the etching chamber. This process was repeated for 45 cycles until the desired channel width was obtained. In situ optical etching tracking through the transparent GaN membrane was performed using a camera directly mounted on the etching chamber, as shown in Extended Data Fig. 1. This method enabled us to obtain the desired channel width accurately, and to ensure that all slits were coalesced into continuous channels underneath the epilayer. In this way, 20- μm wide microchannels were etched through the narrow openings in the epilayer. Next, the SiO₂ hard mask was stripped using 50% HF for 10 min, and the surface was further cleaned from all organic residues using piranha treatment. A Ti/Al/Ti/Ni/Au Ohmic contact stack was deposited using electron-beam evaporation and photolithographically patterned by lift-off, followed by an annealing step at 850 °C. The inlet and outlet channels were etched into the back side of the chip using the Bosch process, until the channels from both sides coalesced, which was confirmed by optical microscopy. The slits in the GaN epilayer were then sealed by electroplating approximately 7 μm of copper on top of the Ohmic contacts. For the electroplating process, a uniform seed layer of chromium-copper (20 nm/70 nm) was deposited on top of the device after the contact metallization step using electron-beam evaporation, where chromium served as an adhesion layer and copper as the seed layer. Next, 10 μm of photoresist was patterned to define the area to be electroplated. Electrical contact was made with the chip, which functions as the cathode, using an electrically conductive adhesive that was applied over all edges of the chip. First, the chip was briefly dipped in H₂SO₄ to remove any surface oxidation. Then, electroplating was performed using a galvanostat at 1 A for 7 min in a solution containing CuSO₄, H₂SO₄ and Cl⁻, as well as an addition of Intervia 8510 (Dow), while using a CuP anode. As the galvanically deposited copper film grows conformally and isotropically, the incisions in the GaN layer seal as the copper layer bridges the gap and coalesces on top of the cavity. After electroplating, the photoresist was stripped, and the seed layer was etched by performing a short copper wet-etch ((NH₄)₂S₂O₈ + H₂SO₄), followed by a chromium etch that is selective over copper (KMnO₄ + Na₃PO₄). Finally, the individual dies were separated using a dicing saw. The Supplementary Video

illustrates the flow path of the coolant through this mMMC heat sink structure.

Experimental setup for evaluation of cooling performance

An open-loop single-phase liquid cooling setup, schematically shown in Extended Data Fig. 2a was built underneath an infrared camera in order to perform liquid cooling experiments, as can be seen in Extended Data Fig. 2b. A reservoir of de-ionized water was pressurized with compressed air using a pressure controller (Elveflow OB1MK3), causing it to flow towards the test section manifold machined out of polyetheretherketone (PEEK) (Extended Data Fig. 2c). PEEK was chosen because of its low thermal conductivity, preventing the heat flux from leaking out of the system by conduction, as well as because of its high glass-transition temperature of 143 °C (ref.⁵⁰). The flow rate of the coolant was measured using a thermal mass flow sensor (Sensirion SLQ-QT500). Chips were mounted on laser-cut poly(methyl methacrylate) (PMMA) carriers with double-sided adhesive and connected to the test section using laser-cut silicone gaskets. A closed seal was obtained on these gaskets using four screws that push down on the PMMA carriers. In this way, no force needs to be applied directly on the chips, preventing the chips from breaking during mounting. Two pressure sensors (Elveflow MPS) were used to measure the pressure at the inlet and outlet of the chip, and the inlet and outlet fluid temperatures are measured using a type-K thermocouple (Thermocoax), integrated just before the inlet and just after the outlet of the chip. The thermocouples were calibrated using a thermostatic bath (Lauda RP855). The chips were connected to a power supply (TTI QPX1200), which simultaneously applies a voltage and measures the current over the device under test (DUT). Electrical connection with the device under test was made using six high-current-rated spring-loaded pins, connected to a custom-made PCB with a hole in the centre to allow infrared measurements. The temperature rise on the surface of the chip was measured using a FLIR SC3000 infrared camera. A LabVIEW automation program was developed to automate the data acquisition. The program waits for the liquid outlet temperature to stabilize, then sends a trigger signal to the video card of the personal computer connected to the infrared camera to record 20 snapshots, and increases the power dissipated on the chip until a critical surface temperature was reached. The surface of the chip was painted black using spray paint to increase emissivity. To further improve the accuracy of the infrared thermography, a pixel-by-pixel emissivity calibration was performed by flowing water at a controlled temperature using the thermostatic bath following the method described in ref.⁵¹. Infrared emission was measured at each temperature and a fit between temperature and infrared emission was established for each pixel of the photodetector. Finally, a MATLAB script was developed to automate the post-processing of the infrared data, which gave the mean surface temperature rise and the maximum surface temperature rise. The latter was defined as the mean value of the 20 pixels with the highest temperature readings, to be less susceptible to noise.

Pressure test

Before evaluating the cooling performance, pressure tests were performed by increasing the system pressure up to 4 bar (above atmospheric) on each chip. This procedure was intended as a burst test, but no failure was observed up to the maximum pressure capability of the experimental facility. It should be noted that typical epitaxial growth of AlGaN/GaN on a silicon substrate using metal–organic chemical vapour deposition is performed at temperatures around 1,000 °C. Owing to the mismatch in coefficient of thermal expansion, the resulting stress in the epilayer is typically on the order of 0.3 GPa, whereas the critical cracking stress lies around 1.1 GPa (ref.⁵²). Although the additional pressure inside the channels during liquid flow does contribute to the total stress in the epilayer, 1 bar (typical operation) is equivalent to only 0.1 MPa. This stress is more than three orders of magnitude smaller than the typical residual stress in the epilayer, and is therefore not expected

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to cause failure. This finding agrees with our observations, as well as with other works in the literature^{53,54}.

Data reduction

The cooling performance of all chips was analysed for power dissipations up to 75 W and flow rates of 0.1–1.1 ml s⁻¹. Extended Data Fig. 3 shows an overview of the data reduction procedure for the 10×-manifold chip to obtain the relevant values in Fig. 3. The maximum surface temperature ($\Delta T_{\text{surface}}$) rise was calculated by subtracting the coolant inlet temperature from the maximum infrared-measured surface temperature (Extended Data Fig. 3a). The liquid temperature rise (ΔT_{liquid}) was calculated by subtracting the inlet water temperature from the water outlet temperature, measured by thermocouple (Extended Data Fig. 3b). The wall temperature (ΔT_{wall}) was calculated by subtracting the mean water temperature between the inlet and outlet from the average surface temperature rise, and performing a correction for one-dimensional conduction through the epilayer, thermal boundary resistance and silicon in case of the straight channels (Extended Data Fig. 3c). A thermal boundary resistance between the GaN and silicon substrate of 1.0×10^{-7} W⁻¹ m² K was assumed^{55–57}. The effective applied power was calculated using an energy balance ($P = fpc_p \Delta T_{\text{liquid}}$), where ρ and c_p are the density and heat capacity of water, respectively. For all flow rates, the total thermal resistance (R_{total}), the caloric thermal resistance (R_{heat}) and convective thermal resistance (R_{conv}) were determined through a linear fit of the surface temperature rise (Extended Data Fig. 3a), coolant temperature rise (Extended Data Fig. 3b) and wall temperature rise (Extended Data Fig. 3c) versus dissipated power, respectively. Thus, every point in Extended Data Fig. 3d was derived from a wide range of measurements to ensure high accuracy. This figure was plotted against the inverse flow rate to highlight the linear relationship between R_{heat} and f^{-1} . As can be seen, most of the variation of R_{total} with flow rate can be accounted to R_{heat} , whereas R_{conv} shows little dependence on the flow rate. COP was calculated by dividing the maximum heat flux for a ΔT_{max} of 60° temperature rise by the required pumping power (P_{pump}) to achieve this level of cooling⁵⁸ ($\text{COP} = \Delta T_{\text{max}} / P_{\text{pump}} R_{\text{total}}$), where pumping power was calculated as the product of flow rate and pressure drop ($P_{\text{pump}} = f \Delta p$). The effective base-area-averaged heat transfer coefficient was calculated using $h_{\text{eff}} = (R_{\text{conv}} A_{\text{device}})^{-1}$, where A_{die} represents the footprint area of the active area of the device, containing both the electric device and the cooling structure. The average local heat transfer coefficient (h_{wall}) was determined by taking the fin efficiency (η) into account, which was calculated using $\eta = 1$ as a starting point for iteratively solving^{59,60}

$$\eta = \frac{\tanh\left(z \sqrt{\frac{2h_{\text{wall}}}{k_{\text{Si}} w_{\text{wall}}}}\right)}{z \sqrt{\frac{2h_{\text{wall}}}{k_{\text{Si}} w_{\text{wall}}}}}.$$

Here, z represents the channel depth, w_{wall} is the channel wall width and k_{Si} is the thermal conductivity of the silicon substrate, which was chosen to be 150 W m⁻¹ K⁻¹. Finally, based on h_{wall} , the average Nusselt number (Nu) was calculated for each measurement condition using $\text{Nu} = h_{\text{wall}} D_h / k_{\text{water}}$, where D_h is the hydraulic diameter of the channel ($D_h = (2w_c z) / (w_c + z)$) and k_{water} is the thermal conductivity of water at the mean measured temperature. Extended Data Fig. 5 shows a complete overview of the remaining datasets for temperature rise and thermal resistance of the 25 μm/50 μm/100 μm-SPMC and 4×-manifold MMC, and the full overview of the design parameters and derived values is presented in Extended Data Table 1. Extended Data Fig. 3e shows the Nusselt number and fin efficiency over the measured range of flow speeds, and Extended Data Fig. 3f shows both the effective base-area-averaged and average local heat transfer coefficients. In thermally developing laminar internal flow, the observed average Nusselt number is expected to increase with flow rate, owing to the increased entrance length. At higher flow rates, a longer entrance length will result in a higher heat

transfer coefficient. This general trend is observed in Extended Data Fig. 4d. For the 10×-manifold, this effect saturates, probably owing to the short length of the channels, which in combination with a potential shift in coolant distribution over the chip at higher Reynolds number, causes the Nusselt number to peak. A complete overview of the fin efficiencies and Nusselt numbers for all devices can be found in Extended Data Fig. 4c, d. Extended Data Fig. 5 shows the additional thermo-hydraulic analysis on all evaluated devices used for deriving their cooling performance. Extended Data Table 1 summarizes all dimensions and cooling performance of the chips. The performance of the mMMC chips, as well as the SPMC chips evaluated in this work, were benchmarked against a wide range of works in the literature that use water as a coolant (Extended Data Fig. 6). The cooling approaches were classified as SPMC^(19,61), pin-fins^(61,62), strip-fins^(61,63,64), MMC^(29,35,65–68), impinging jet^(37,61,69–71), and mMMC (this work). A distinction was made between techniques where the water is in direct contact with the die and the die contains cooling structures (embedded cooling), approaches where the water is in direct with the die, but the die itself does not contain cooling structures (bare-die cooling), and indirect cooling, which requires an additional thermal interface between the heat sink and the chip. All the data used in the benchmarking study are available in the Supplementary Table.

Impact of hydrostatic pressure on electrical performance

Owing to the piezoelectric properties of GaN, changes in pressure and the resulting strain in the epilayer may affect the electrical performance of the device^{53,72}. To investigate these phenomena, the outlet of the test section in Extended Data Fig. 2 was plugged. The hydrostatic pressure applied to the test section was swept from 0 mbar to 1,590 mbar and back. At each step in pressure, a cyclic current–voltage measurement was performed, together with the measurement of the water temperature in the test section. After the water reached the ambient temperature of 22 °C, the next measurement was performed. This was done to prevent any drift in temperature during the 3-h-long measurement, which might affect the resistance of the chip. The 14 current–voltage characteristics (Extended Data Fig. 7a) show no clear impact on device performance. Next, R was derived from the current–voltage curves using a linear fit at each pressure condition. The observed variation in R remained within 1.5% of its initial value at atmospheric pressure (Extended Data Fig. 7b). These results show that the effect of the pressure range considered here on the electrical properties of the devices is negligible for the purpose of this work. The small impact of this effect on electrical performance could be attributed to the fact that the micro-channels are positioned below the pads, and covered with metal. Any change in carrier density in this region of the chip due to strain would not noticeably affect the device performance, as most of the contribution to the device's resistance occurs in the area between the pads.

a.c.–d.c. converter fabrication

Tri-anode Schottky barrier diode full-wave bridge rectifiers were fabricated on an AlGaN/GaN-on-silicon wafer with, from top to bottom: a 2.9-nm-thick GaN cap layer, a 20-nm-thick AlGaN barrier, a 420-nm-thick GaN channel and a 4.2-μm-thick buffer layer on a 400-μm-thick silicon substrate. The tri-anode/tri-gate regions were first defined using electron-beam lithography with a width and spacing of 200 nm, followed by a 200-nm-deep inductively coupled plasma etch following the process previously described in ref.⁴⁶. These dimensions have been shown to result in high breakdown voltage and excellent on-state performance⁷³. After Ohmic metal deposition for the cathode contacts, 20-nm-thick SiO₂ was deposited by atomic layer deposition as the tri-gate dielectric, and then selectively removed in the tri-anode region. A Ni/Au metal stack was deposited onto the tri-gate/tri-anode region to form the Schottky contact, as well as on the cathode. Extended Data Fig. 8d shows a SEM image of four scaled-up tri-gate Schottky barrier diodes forming the full-wave bridge rectifier. The close-up SEM image

shows the Schottky barrier diode structure. The channel length was 16.5 μm , corresponding to 1.2 kV of breakdown voltage⁴⁶. Next, the wafer was temporarily bonded to a carrier wafer before microchannels were etched in the back side using deep reactive ion etching to a depth of approximately 500 μm . After detaching the substrate from the carrier wafer and dicing, the individual liquid-cooled full-wave bridge rectifier was attached to a three-layer PCB using water-resistant adhesive with embedded coolant delivery channels. The top layer of the PCB provides the electric circuit connections and the middle layer contains the coolant delivery channels (Extended Data Fig. 8a). The individual layers of the PCB were easily connected using laser-cut adhesive (Extended Data Fig. 8b). Pressure-sensitive double-sided adhesive was used from AR-Global (ARseal 90880), with water- and solvent-resistant properties as well as a high-temperature operation range (up to 120 °C). A rectangular piece with inlet and outlet holes was laser-cut using a CO₂ laser. The double-sided adhesive was placed on the PCB, aligning the inlet and outlet holes of the adhesive with the PCB. Next, the chip was attached to adhesive on the PCB to create a seal. This approach emphasizes the ability to assemble a prototype without the need of expensive machines. Alternatively, since the PCB contains a gold-plated metalized landing pad, conventional large-scale industrial processes can be used as well, such as (eutectic) solder bonding between a metallization layer on the backside of the chip and the PCB. Extended Data Fig. 8c shows the final assembled converter.

a.c.–d.c. converter evaluation

The cooling performance of the a.c.–d.c. converter was investigated by connecting all four Schottky barrier diodes in parallel, such that a uniform known d.c. power dissipation could be applied to the chip. For flow rates varying between 0.08 ml s⁻¹ and 0.8 ml s⁻¹, the surface temperature rise was monitored increasing power dissipation up to 25 W (Extended Data Fig. 9b). The flow-rate-dependent thermal resistance was derived from the slope of surface temperature versus power (Extended Data Fig. 9c). For each flow rate, the pressure drop between the inlet and outlet was measured, and the corresponding pumping power was calculated (Extended Data Fig. 9d). Over the entire range of measured flow rates, the total pumping power stayed below 62 mW, which can be easily supplied by miniaturized piezoelectric micropumps to achieve a high system-level power density. To study the power-conversion performance of the a.c.–d.c. converter, the device was connected to a full-bridge inverter with LC filter to supply a 100-kHz a.c. input, up to 200 V peak to peak. The d.c. output of the converter was connected to a load of 50 Ω , and the flow rate was fixed at 0.8 ml s⁻¹. Extended Data Fig. 9a shows the input a.c. and output d.c. waveforms of the converter at 70 W of transferred power. Surface temperature was monitored using an infrared camera, while power was increased until a critical surface temperature rise of 60 K was observed. Following this approach, up to 120 W of output power could be delivered using this compact power converter.

Data availability

All the data needed to evaluate the conclusions in the paper are present in the paper, in the Extended Data and in the Supplementary Information.

47. Mileham, J. R. et al. Wet chemical etching of AlN. *Appl. Phys. Lett.* **67**, 1119 (1995).
48. Guo, W. et al. KOH based selective wet chemical etching of AlN, Al_xG_{1-x}N, and GaN crystals: a way towards substrate removal in deep ultraviolet-light emitting diode. *Appl. Phys. Lett.* **106**, 082110 (2015).
49. Vicknesh, S., Tripathy, S., Lin, V. K. X., Wang, L. S. & Chua, S. J. Fabrication of deeply undercut GaN-based microdisk structures on silicon platforms. *Appl. Phys. Lett.* **90**, 071906 (2007).
50. van der Vegt, A. K. & Govaert, L. E. *Polymeren: Van Keten Tot Kunstof* (VSSD, 2003).
51. Szczukiewicz, S., Borhani, N. & Thome, J. R. Fine-resolution two-phase flow heat transfer coefficient measurements of refrigerants in multi-microchannel evaporators. *Int. J. Heat Mass Transf.* **67**, 913–929 (2013).
52. Raghavan, S. & Redwing, J. M. Growth stresses and cracking in GaN films on (111) Si grown by metal-organic chemical-vapor deposition. I. AlN buffer layers. *J. Appl. Phys.* **98**, 023514 (2005).
53. Chapin, C. A., Miller, R. A., Dowling, K. M., Chen, R. & Senesky, D. G. InAlN/GaN high electron mobility micro-pressure sensors for high-temperature environments. *Sens. Actuat. A* **263**, 216–223 (2017).
54. Tan, X. et al. High performance AlGaN/GaN pressure sensor with a Wheatstone bridge circuit. *Microelectron. Eng.* **219**, 111143 (2020).
55. Sarua, A. et al. Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices. *IEEE Trans. Electron Dev.* **54**, 3152–3158 (2007).
56. Turin, V. O. & Balandin, A. A. Performance degradation of GaN field-effect transistors due to thermal boundary resistance at GaN/substrate interface. *Electron. Lett.* **40**, 81–83 (2004).
57. Kuzník, J. et al. Transient thermal characterization of AlGaN/GaN HEMTs grown on silicon. *IEEE Trans. Electron Dev.* **52**, 1698–1705 (2005).
58. Steinke, M. E. & Kandlikar, S. G. Single-phase liquid heat transfer in plain and enhanced microchannels. In *Proc. 4th Int. Conf. on Nanochannels, Microchannels and Minichannels (ICNMM2006)* <https://asmemedicalcollection.asme.org/ICNMM/proceedings-abstract/ICNMM2006/47608/943/323023> (ASME, 2006).
59. Tosun, I. *Modeling in Transport Phenomena* (Elsevier, 2007).
60. Hesselgreaves, J. E., Law, R. & Reay, D. A. *Compact Heat Exchangers* 2nd edn Vol. 1, Ch. 7, 275–360 (Butterworth-Heinemann, 2016).
61. Ndaa, S., Peles, Y. & Jensen, M. K. Multi-objective thermal design optimization and comparative analysis of electronics cooling technologies. *Int. J. Heat Mass Transf.* **52**, 4317–4326 (2009).
62. Brunschwiler, T. et al. Interlayer cooling potential in vertically integrated packages. In *Microsystem Technologies* Vol. 15, 57–74 (Springer, 2009).
63. Kandlikar, S. G. & Upadhye, H. R. Extending the heat flux limit with enhanced microchannels in direct single phase cooling of computer chips. In *21st Ann. IEEE Symp. on Semiconductor Thermal Measurement and Management 8–15* (IEEE, 2005).
64. Colgan, E. G. et al. A practical implementation of silicon microchannel coolers for high power chips. In *21st Ann. IEEE Symp. on Semiconductor Thermal Measurement and Management 1–7* (IEEE, 2005).
65. Jung, K. W. et al. Embedded cooling with 3D manifold for vehicle power electronics application: single-phase thermal-fluid performance. *Int. J. Heat Mass Transf.* **130**, 1108–1119 (2019).
66. Ohadi, M., Choo, K., Dessiatoun, S. & Cetegen, E. *Next Generation Microchannel Heat Exchangers* 1–111 (Springer, 2013).
67. Han, Y., Lau, B. L., Tang, G., Zhang, X. & Rhee, D. M. W. Si-based hybrid microcooler with multiple drainage microtrenches for high heat flux cooling. *IEEE Trans. Compon. Packag. Manuf. Technol.* **7**, 50–57 (2017).
68. Han, Y., Lau, B. L., Zhang, X., Leong, Y. C. & Choo, K. F. Thermal management of hotspots with a microjet-based hybrid heat sink for GaN-on-Si devices. *IEEE Trans. Compon. Packag. Manuf. Technol.* **4**, 1441–1450 (2014).
69. Driti, J., Hahn, J., Cadotte, R., McNulty, M. & Luppia, D. Embedded cooling of high heat flux electronics utilizing distributed microfluidic impingement jets. In *ASME 2015 Int. Tech. Conf. Exhib. on Packaging and Integration of Electronic and Photonic Microsystems (InterPACK 2015)/ASME 2015 13th Int. Conf. on Nanochannels, Microchannels, and Minichannels* Vol. 3, T10A014, https://library.epfl.ch/beast?record=ebi01_prod010609314 (ASME, 2015).
70. Natarajan, G. & Bezama, R. J. Microjet cooler with distributed returns. *Heat Transf. Eng.* **28**, 779–787 (2007).
71. Wei, T. et al. High efficiency direct liquid jet impingement cooling of high power devices using a 3D-shaped polymer cooler. In *Technical Digest International Electron Devices Meeting (IEDM) 32.5.1–32.5.4* <https://ieeexplore.ieee.org/document/8268487> (IEEE, 2018).
72. Dzuba, J. et al. AlGaN/GaN diaphragm-based pressure sensor with direct high performance piezoelectric transduction mechanism. *Appl. Phys. Lett.* **107**, 122102 (2015).
73. Ma, J., Santoruvo, G., Tandon, P. & Matioli, E. Enhanced electrical performance and heat dissipation in AlGaN/GaN Schottky barrier diodes using hybrid tri-anode structure. *IEEE Trans. Electron Devices* **63**, 3614–3619 (2016).

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Author contributions R.v.E. and E.M. conceived the project. R.v.E., R.S. and L.N. developed and optimized device fabrication processes. R.v.E. and L.N. fabricated the devices. R.v.E. designed and developed the experimental setup to study cooling performance. G.K. designed the circuits for evaluating the fabricated devices. R.v.E. and G.K. designed and performed the experiments. R.v.E. analysed the data. E.M. supervised the project. R.v.E. and E.M. wrote the manuscript with input from all authors.

Competing interests The authors declare no competing interests.

Additional information

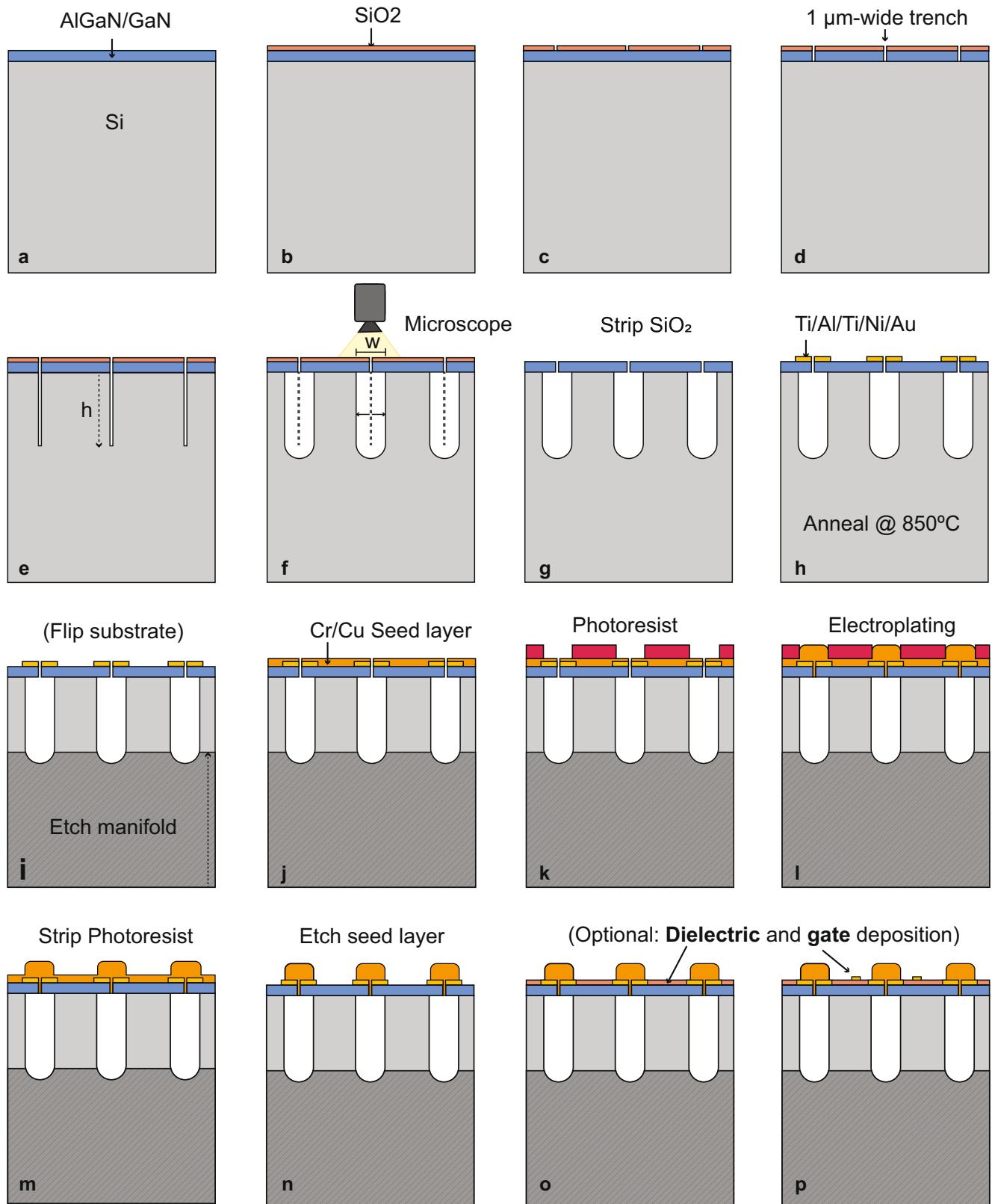
Supplementary information is available for this paper at <https://doi.org/10.1038/s41586-020-2666-1>.

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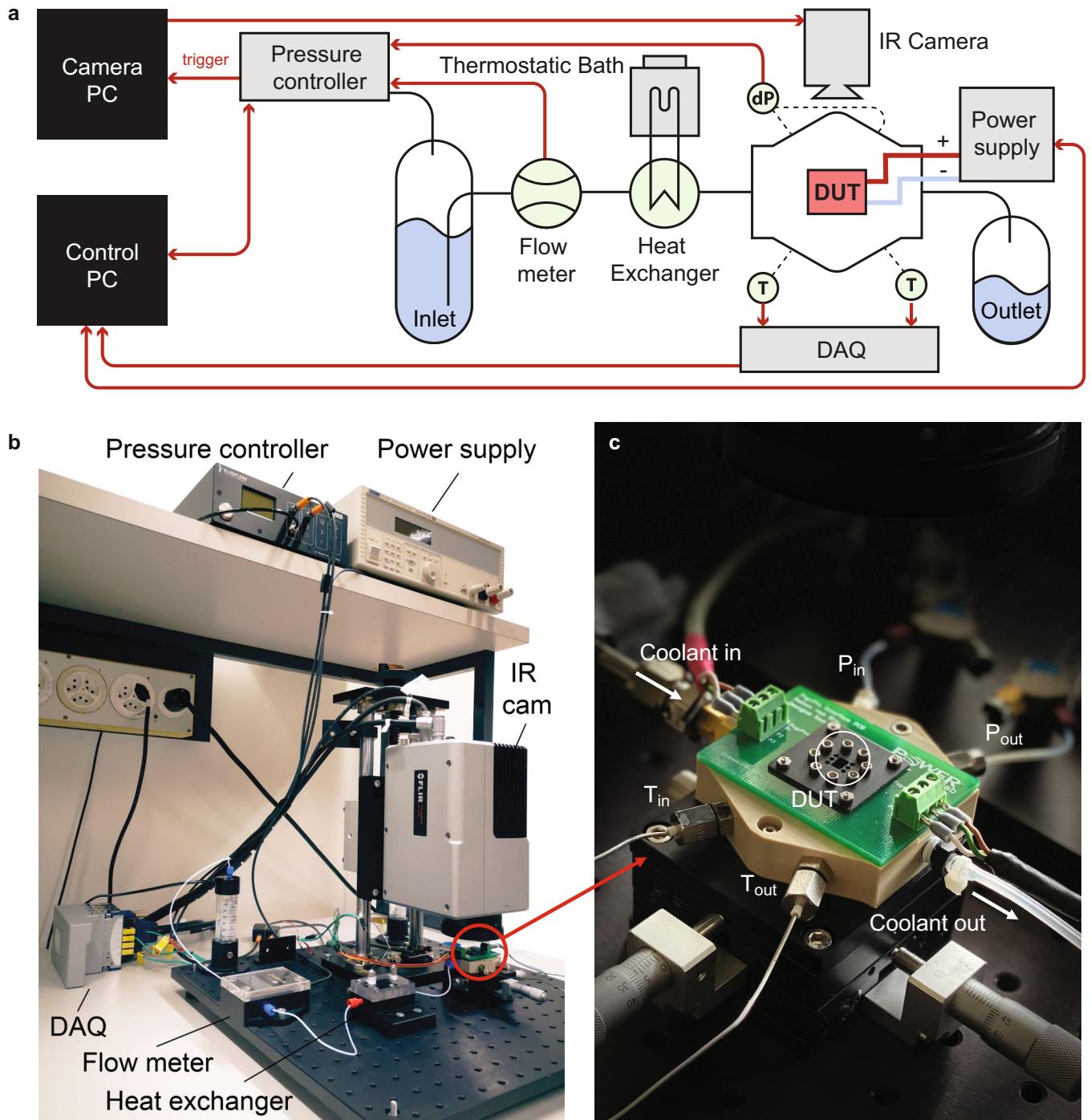
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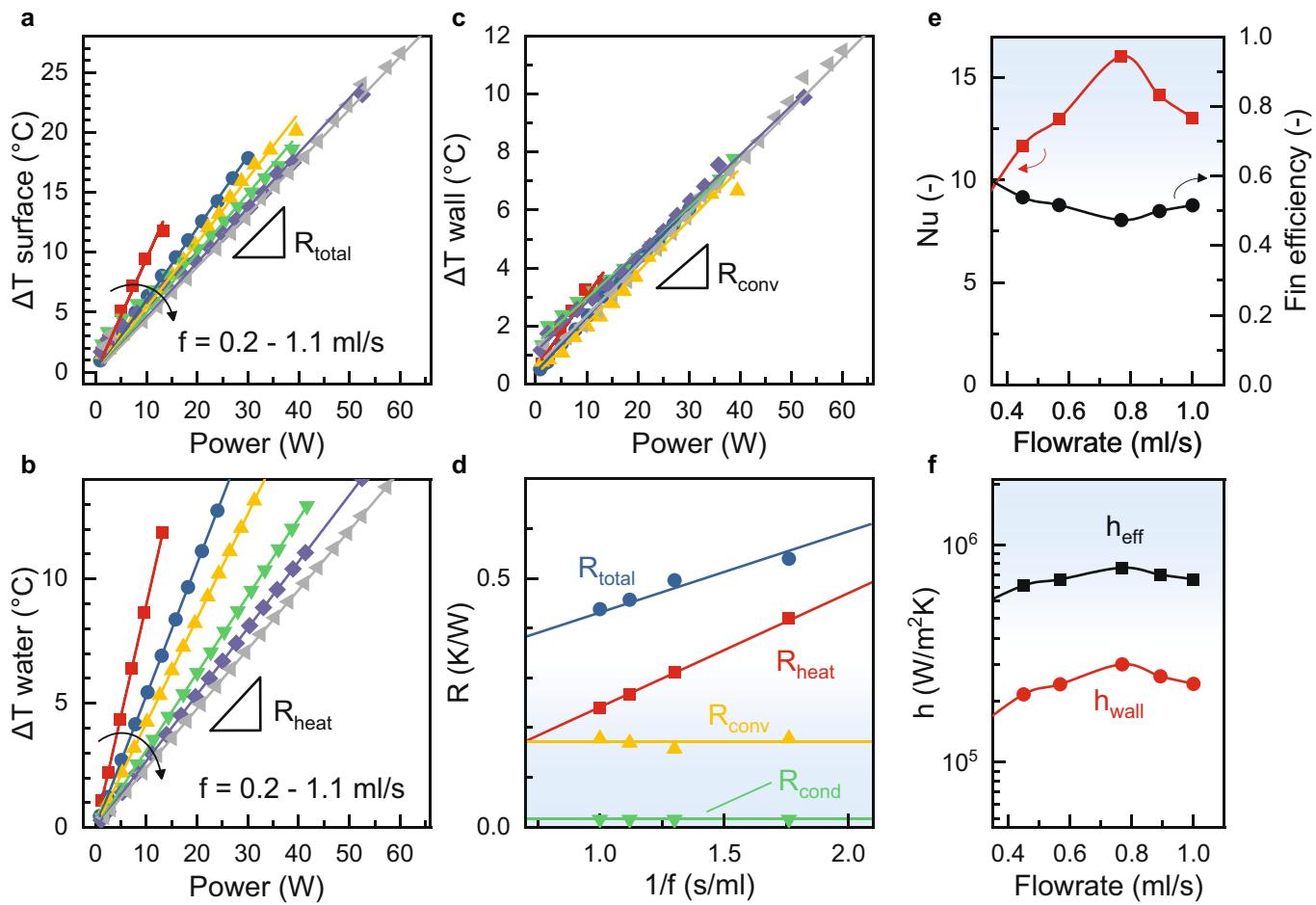
Extended Data Fig. 1 | Fabrication process of the co-designed microfluidic-electric device. **a**, AlGaN/GaN epilayer on a silicon substrate. **b**, SiO₂ hard-mask deposition. **c**, Hard mask patterning and opening. **d**, Epilayer etching until the substrate is reached. **e**, Anisotropic deep (to depth h) etching of the silicon substrate through the epilayer opening. **f**, Isotropic gas etching through the epilayer opening to widen the slits under the epilayer. An in situ optical etching tracking was put in place to control the width w of the channels. **g**, Hard-mask removal. **h**, Ohmic contact deposition and annealing, and seed

layer deposition for electroplating and patterning the electroplating mask. **i**, Manifold channel etching from the back of the substrate. **j**, Cr/Cu seed layer deposition for electroplating. **k**, Lithography step to define electroplating openings. **l**, Electroplating to seal the epilayer openings. **m**, Photoresist removal. **n**, Wet etch to remove Cr/Cu seed layer. **o**, Finish device fabrication with optional dielectric deposition. **p**, Finish device fabrication with optional gate metal deposition.



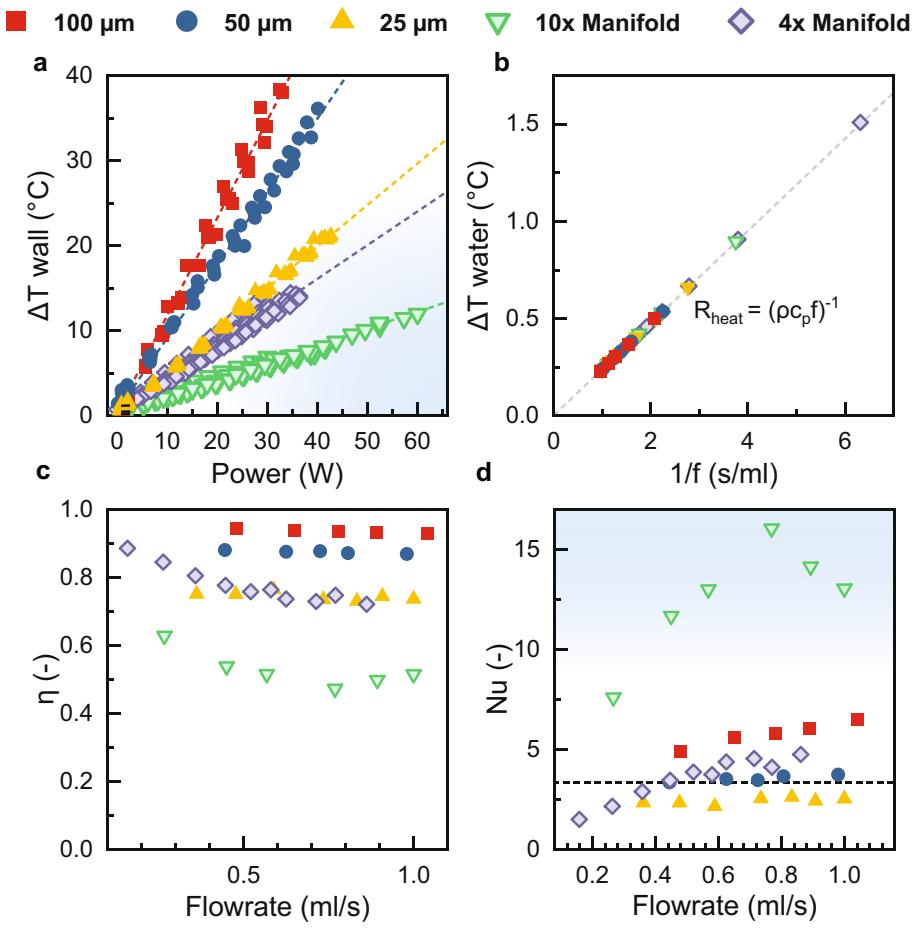
Extended Data Fig. 2 | Experimental setup for evaluating the thermo-hydraulic performance. **a**, Schematic overview of the measurement setup. An inlet reservoir of coolant is pressurized using a pressure controller, whereas the temperature is controlled using a thermostatic bath. Liquid flow through a flow meter into the test section, containing the chip (DUT). The temperature of the chip is monitored using

an infrared (IR) camera, and coolant temperature is monitored using thermocouples (T) and transferred to the personal computer (PC) using a data acquisition box (DAQ). Pressure drop over the chip (dP) is measured at the inlet and outlet port of the chip. **b**, Picture of the experimental setup for characterizing the thermal performance. **c**, Close-up picture of the test section.



Extended Data Fig. 3 | Example data reduction of thermal characterization experiments for the 10 \times -manifold chip. **a**, Peak surface temperature rise above the inlet temperature, measured using infrared thermography at varying power dissipation. The slope of the linear fit through the data points gives the total thermal resistance (R_{total}). **b**, Water temperature rise, measured between the inlet and outlet of the chip. The slope of the linear fit through the data points gives the contribution of the total thermal resistance due to the

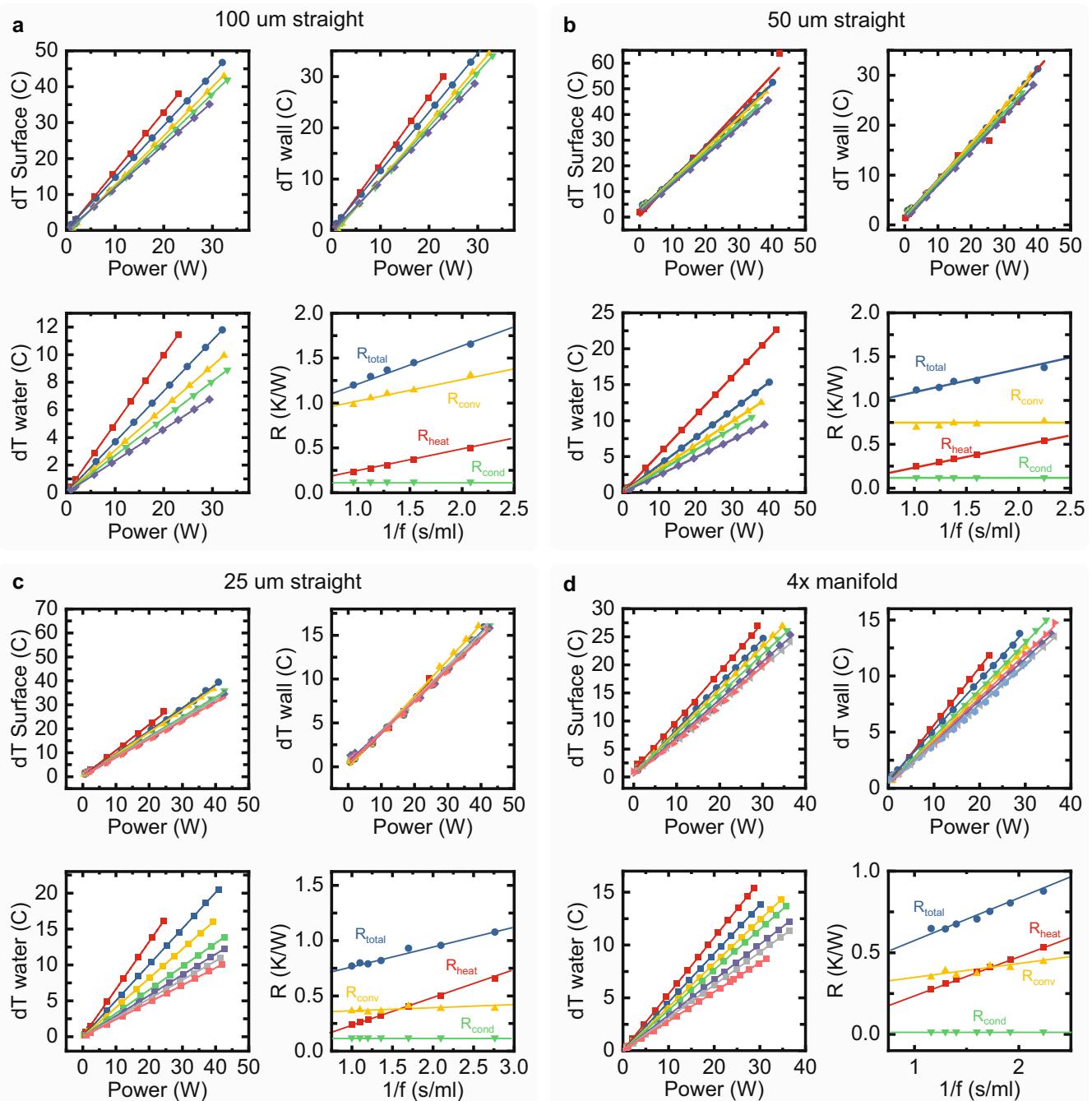
temperature rise of the water (R_{heat}). **c**, Wall temperature rise. The slope through these data points gives the convective thermal resistance. **d**, Total, caloric, convective and conductive thermal resistance versus the inverse flow rate. **e**, Nusselt number and fin efficiency. **f**, Effective base-area averaged heat transfer coefficient (h_{eff}) and wall-area averaged heat transfer coefficient (h_{wall}), taking the surface area of the microchannels as well as the fin efficiency into account.



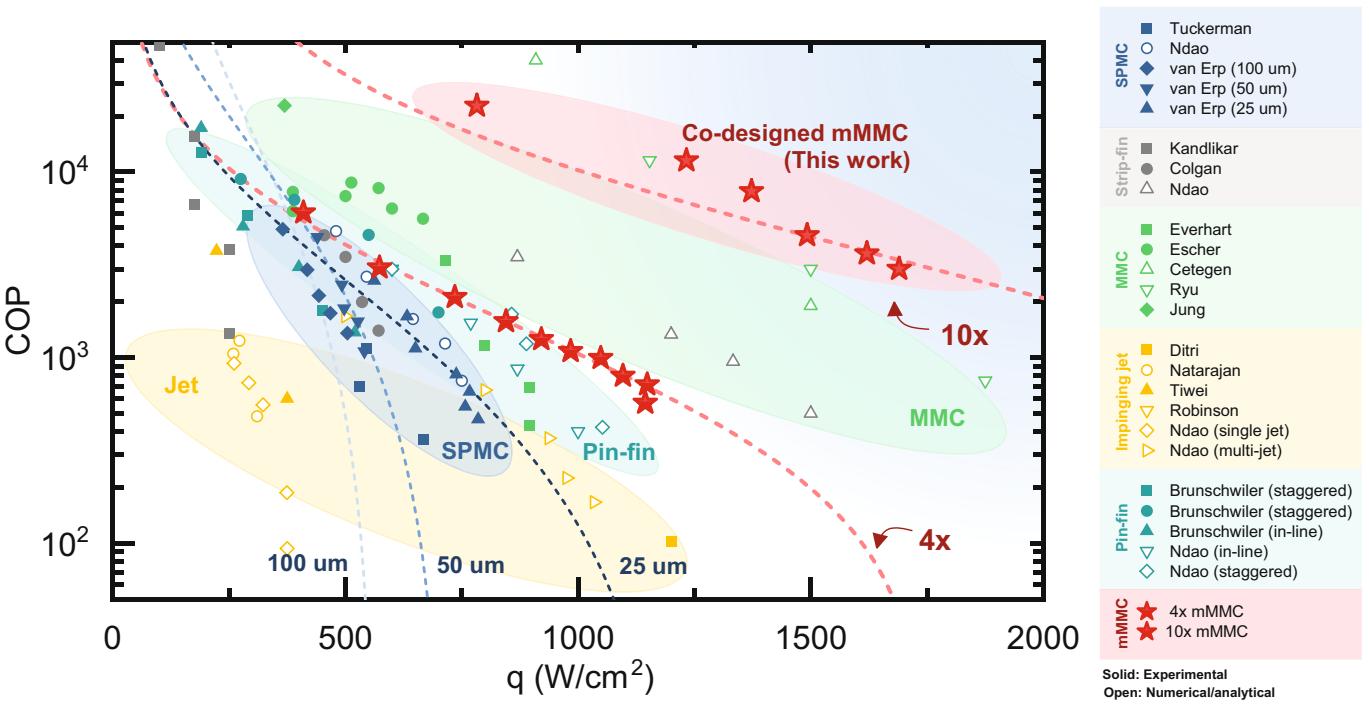
Extended Data Fig. 4 | Overview of derived values of the thermo-hydraulic analysis. **a**, Wall temperature for all devices. Each device shows a distinct slope in wall temperature rise versus power dissipation. **b**, Caloric thermal resistance

for all evaluated flow rates, showing a clear $(\rho c_p f)^{-1}$ relationship over all devices. **c**, Fin efficiency over a range flow rates. **d**, Nusselt number versus inverse flow rate. The dashed line indicates that $\text{Nu} = 3.66$ for fully developed internal flow.

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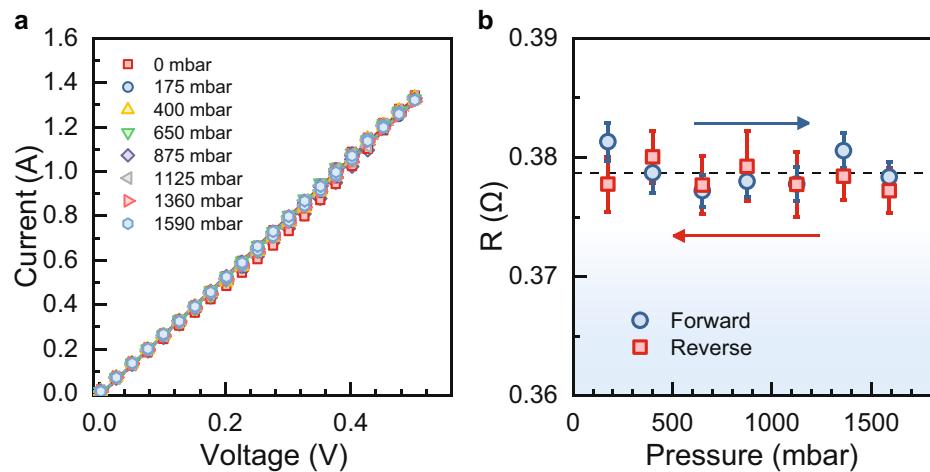
Extended Data Fig. 5 | Additional thermo-hydraulic data. Surface temperature rise dT , wall temperature rise, water temperature rise and thermal resistance R for: **a**, 100 μm -wide SPMC; **b**, 50 μm -wide SPMC straight microchannels; **c**, 25 μm -wide SPMC straight microchannels; and **d**, 4 \times -manifold.



Extended Data Fig. 6 | Extensive benchmarking plot of micro-structured cooling approaches in the literature using water as a working fluid. COP versus heat flux for a maximum surface temperature rise of 60 K. Solid markers indicate experimental results and open markers indicate numerical or

analytical calculations. The results in this work are indicated by red stars. Dashed lines correspond to predictions based on a constant heat transfer. References^{19,29,35,38,61–66,68–71} to all datasets used can be found in Extended Data Table 2, and all the data used are available in the Supplementary Table.

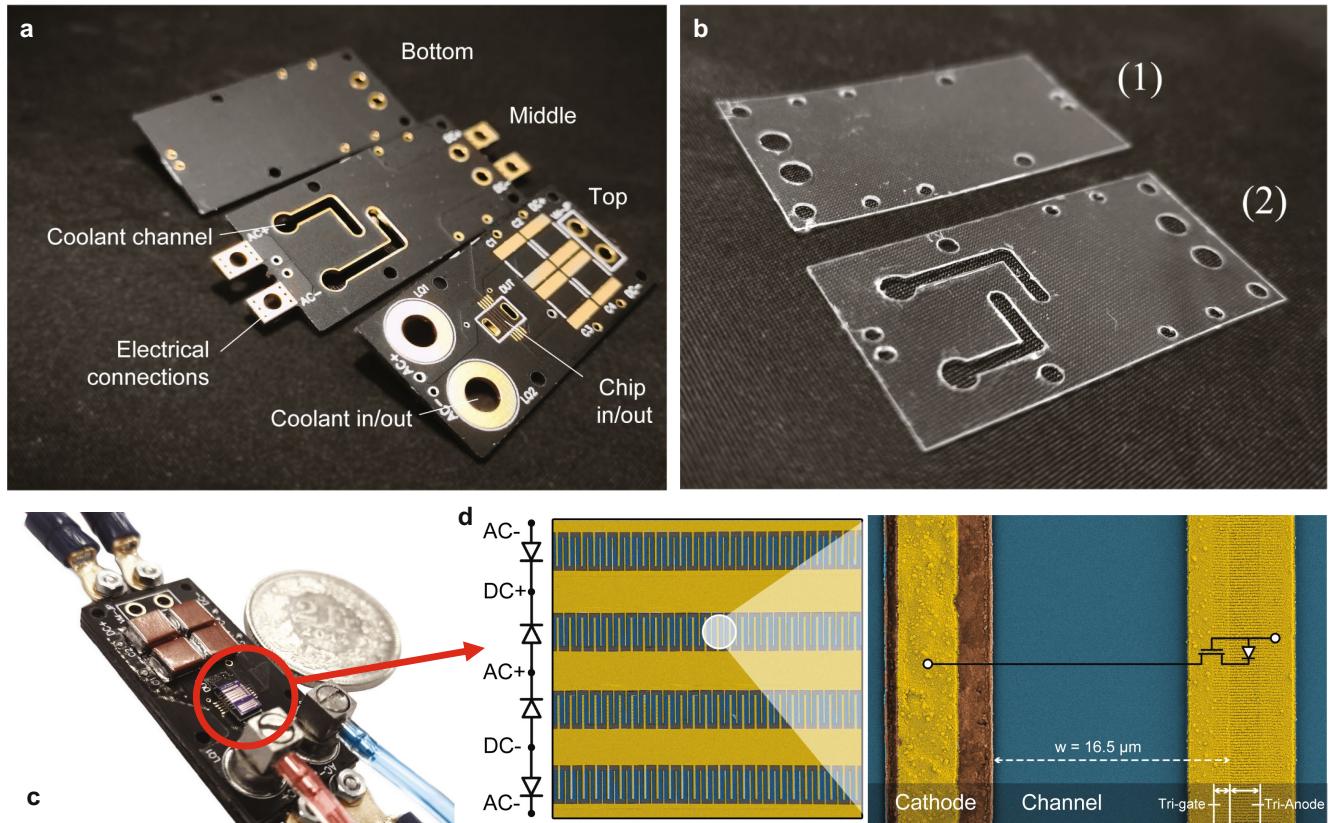
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Extended Data Fig. 7 | Impact of pressure on electrical performance.

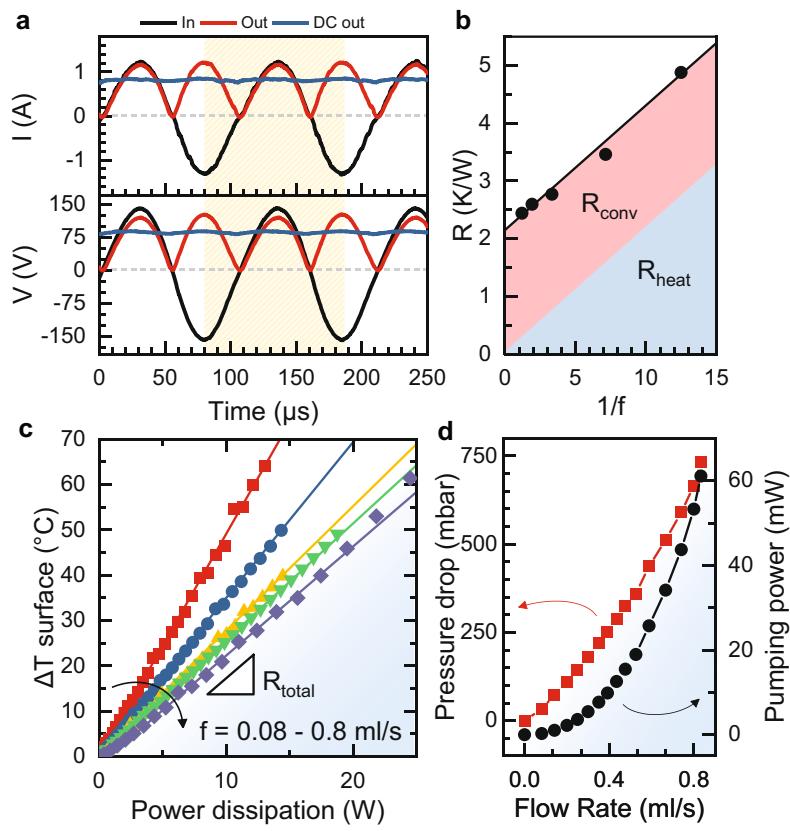
a, Current–voltage characteristics at hydrostatic pressure between 0 mbar and 1,590 mbar. **b**, Normalized change in electrical resistance versus pressure during a sweep in pressure up to 1,600 mbar and back. Each resistance value

was extracted using a linear fit ($R^2 > 0.997$) through a cyclic current–voltage measurement from 0 V to 0.5 V and back. Error bars indicate standard error of the fit over each set of 46 data points per condition.



Extended Data Fig. 8 | Structure of the integrated full-bridge rectifier with embedded cooling. **a**, Three PCBs that provide coolant delivery to the chip. **b**, Laser-cut adhesives used to bond the layers together. **c**, Converter after

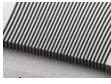
assembly, with electrical and fluidic connections. **d**, SEM image of the four-diode structure. The inset shows the polarity of each device and a close-up of the structure of the tri-anode Schottky barrier diode.



Extended Data Fig. 9 | Operation of the a.c.-d.c. converter with embedded cooling. **a**, Input and output waveforms of 150 V/1.2 A peak-to-peak rectification at 100 kHz. **b**, Surface temperature rise versus power dissipation

for varying flow-rates. **c**, Thermal resistance versus inverse flow rate of the full converter. Pressure drop and pumping power versus flow rate. **d**, Pressure drop and pumping power versus flow rate.

Extended Data Table 1 | Table of all design parameters and measured values per chip

Parameter	Unit	SPMC			mMMC		
							
Manifold channels	N_m	[$-$]	-	-	-	4	10
Channel Width	w_c	[μm]	100	50	25	20	20
Channel Depth	z	[μm]	250	250	250	125	125
Hydraulic diameter	D_h	[μm]	142	83	45	34	34
Device/cooling area	A_d	[cm^2]	0.099	0.099	0.099	0.081	0.081
Wetted area	A_{wet}	[cm^2]	0.348	0.598	1.09	0.476	0.476
Average convective thermal resistance	R_{conv}	[K/W]	1.1	0.73	0.37	0.41	0.17
Conductive thermal resistance	R'_{cond}	[K/W]	1.2×10^{-2}	1.2×10^{-2}	1.2×10^{-2}	1.5×10^{-3}	1.5×10^{-3}
Average effective heat transfer coefficient	h_{eff}	[W/m^2K]	8.2×10^4	1.4×10^5	2.7×10^5	3.1×10^5	7.3×10^5
Average local heat transfer coefficient	h_{wall}	[W/m^2K]	2.5×10^4	2.6×10^4	3.3×10^4	6.9×10^4	2.4×10^5
Average fin efficiency	η	[$-$]	0.94	0.87	0.74	0.76	0.50
Maximum Nusselt number	Nu	[$-$]	6.5	3.7	2.6	4.7	16
Hydraulic resistance	r_h	[$mbar-s/m$]	358	535	1692	2191	479

R is thermal resistance in $K W^{-1}$, and R' is surface-area-normalized thermal resistance in $cm^2 K W^{-1}$.

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Extended Data Table 2 | Selected references for the benchmarking study in Extended Data Fig. 6

Ref.	Authors	Year	Approach*	Geometry	Application	Work
This work	van Erp	2020	Embedded	mMMC	Power electronics	Experimental
[19]	Tuckerman & Pease	1981	Embedded	SPMC	Logic	Experimental
[61]	Ndao et al.	2009	-	SPMC	General	Optimization
[61]	Ndao et al.	2009	-	In-line pin fin	General	Optimization
[61]	Ndao et al.	2009	-	Staggered pin fin	General	Optimization
[61]	Ndao et al.	2009	-	Offset strip fin	General	Optimization
[61]	Ndao et al.	2009	-	Single Jet	General	Optimization
[61]	Ndao et al.	2009	-	Multi-Jet	General	Optimization
[38]	Everhart et al.	2007	Bare die	MMC bare die cooling	Power diode	Experimental
[35]	Escher et al.	2010	Embedded	MMC	Logic	Experimental
[64]	Colgan et al.	2005	Embedded or indirect	Offset strip fin	Logic	Experimental
[69]	Ditri et al.	2015	Bare die	Multi-jet	Bare die cooling	Numerical & experimental
[68]	Han et al.	2014	Indirect (Chip included)	Hybrid Jet/MMC	RF power amplifier	Numerical
[63]	Kandlikar & Upadhye	2005	-	Offset strip fin	General	Experimental
[70]	Natarajan & Bezama	2007	Direct	Multi-jet	Logic	Numerical
[71]	Wei et al.	2018	Bare die	Multi-jet	Logic	Experiment
[62]	Brunschwiler et al.	2009	Embedded	Pin-Fin Staggered	3D integration	Experimental
[62]	Brunschwiler et al.	2009	Embedded	Distorted Pin-Fin staggered	3D integration	Experimental
[62]	Brunschwiler et al.	2009	Embedded	In-line pin fin	3D integration	Experimental
[29]	Ryu et al.	2003	-	MMC	General	Numerical
[66]	Ohadi et al.	2013	Indirect (Chip not included)	MMC	General	Numerical
[65]	Jung et al.	2019	Direct	MMC	Vehicle power electronics	Experimental

Data are from refs. ^{19,29,35,38,61–66,68–71}. *‘Embedded’ means that the liquid is in direct contact with the die, and the cooling structure is embedded inside the die. ‘Bare die’ means that the liquid is in direct contact with the die, but no cooling structures are embedded inside the die. ‘Indirect’ means that the liquid is not in direct contact with the die, and no cooling structures are embedded inside the die. An additional interface between the chip and the cooling device is required. RF, radio frequency.