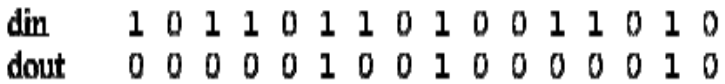
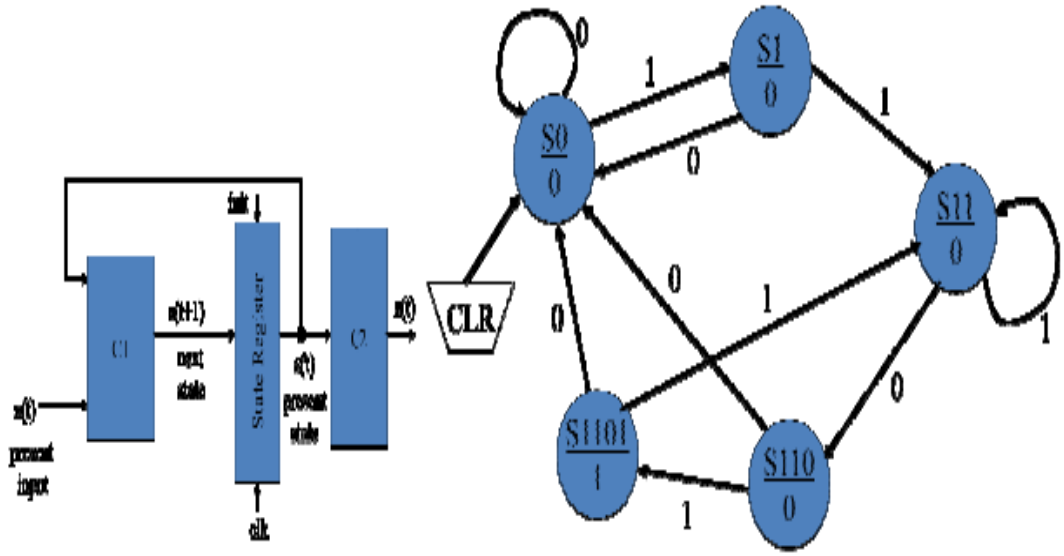
Objective: Write a program for behavior model 1101 Sequence Detector.

Theory

The 1101 sequence detector is a digital circuit that detects the presence of the binary sequence "1101" in an input stream of bits. It can be designed using either a Moore machine or a Mealy machine, and can allow for overlapping sequences or not. The key aspects include Moore machines (non-overlapping and overlapping), which output only when the full sequence is detected, and Mealy machines (non-overlapping and overlapping), which output based on both the current state and input. The choice between these designs depends on the specific requirements of the application, and the state diagrams, state tables, and logic equations for implementation are provided in the search results.





Source Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity SEQDET_020313 is
    Port ( clk : in  STD_LOGIC;
           clr : in  STD_LOGIC;
           din : in  STD_LOGIC;
           dout : out  STD_LOGIC);
end SEQDET_020313;

architecture Behavioral of SEQDET_020313 is
  type state_type is (S0, S1, S11, S110, S1101);
   signal present_state, next_state: state_type;
     begin
                synch: process (clk, clr)
                begin
                    if clr='1' then present_state <= S0;
                    elsif clk'event and clk='1' then
                                present_state <= next_state;
                    end if;
                end process;
                combl: process (present_state, din)
                begin
                 case present_state is
                   when S0 =>
                      if din='1' then
                                next_state <= S1;
                      else
                                next_state <= S0;
                      end if;
                   when S1=>
                      if din='1' then
                                next_state <= S11;
                      else
                                next_state <= S0;
                      end if;
                   when S11 =>
                      if din='0' then
                                next_state <= S110;
                      else
                                next_state <= S11;
                      end if;
                   when S110 =>
                      if din='1' then
                                next_state <= S1101;
                      else
                                next_state <= S0;
                      end if;
                   when S1101=>
                      if din='0' then
                                next_state <= S0;
                      else
                                next_state <=S11;
                      end if;
                   when others=>
                                 null;
                 end case;
                end process;
                comb2: process (present_state)
                 begin
                   if present_state = S1101 then
                                dout <= '1';
                   else
                                dout <= '0';
                   end if;
                end process;
end Behavioral;
```

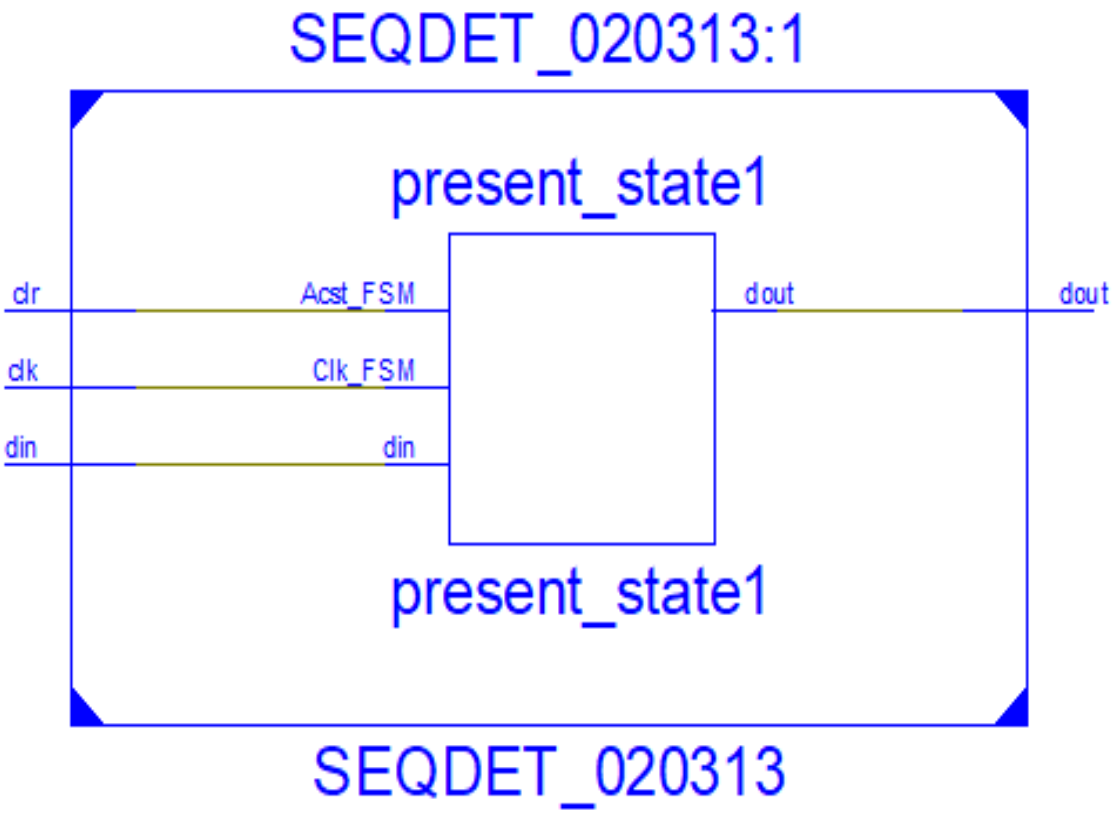


Fig 1 RTL diagram for Sequence Detector

Precaution:

Make sure that there are no syntax and Semantic errors.

Conclusion:

Hence, in this lab VHDL codes of behavior model of 1101 Sequence Detector were simulated and synthesized.