Objective: Write a program for structural model Full Adder Circuit.

Theory

The structural model of a Full Adder circuit depicts its composition using basic logic gates to perform binary addition. It processes three inputs (A, B, and C) to produce Sum and Carry-out outputs. The model typically employs two XOR gates for Sum calculation, along with AND and OR gates for Carry-out determination. This arrangement allows efficient processing of current bits and previous carries. The Full Adder's modular design enables cascading for multi-bit arithmetic operations, making it a fundamental building block in digital systems. This gate-level representation provides a clear understanding of the Full Adder's operation and serves as a blueprint for practical implementation in various digital circuits.

Source Code:

```
31  library IEEE;
32  use IEEE.STD_LOGIC_1164.ALL;
33  entity FA_020313 is
34      Port ( FA : in  STD_LOGIC;
35             FB : in  STD_LOGIC;
36             FSUM : out  STD_LOGIC;
37             FCARRY : out  STD_LOGIC;
38             FC : in  STD_LOGIC);
39  end FA_020313;
40
41  architecture structure of FA_020313 is
42  component HA is
43  port (A: in STD_LOGIC;
44        B: in STD_LOGIC;
45        S: out STD_LOGIC;
46        C: out STD_LOGIC);
47        end component;
48
49  component OR_Gate is
50  port(X: in STD_LOGIC;
51        Y: in STD_LOGIC;
52        Z: out STD_LOGIC
53        );
54        end component;
55
56  signal U,V,W: STD_LOGIC;
57  begin
58  U1 : HA port map(A=>FA,B=>FB,S=>U,C=>V);
59  U2 : HA port map(A=>U, B=>FC, S=>FSUM, C=>W);
60  U3 : OR_Gate port map(X=>V,Y=>W,Z=>FCARRY);
61  end structure;
```

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity HA is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           S : out  STD_LOGIC;
           C : out  STD_LOGIC);
end HA;

architecture Behavioral of HA is

begin
S <= A XOR B;
C <= A AND B;
end Behavioral;
```

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity OR_Gate is
    Port ( X : in  STD_LOGIC;
           Y : in  STD_LOGIC;
           Z : out  STD_LOGIC);
end OR_Gate;

architecture Behavioral of OR_Gate is

begin
Z <= X OR Y;

end Behavioral;
```

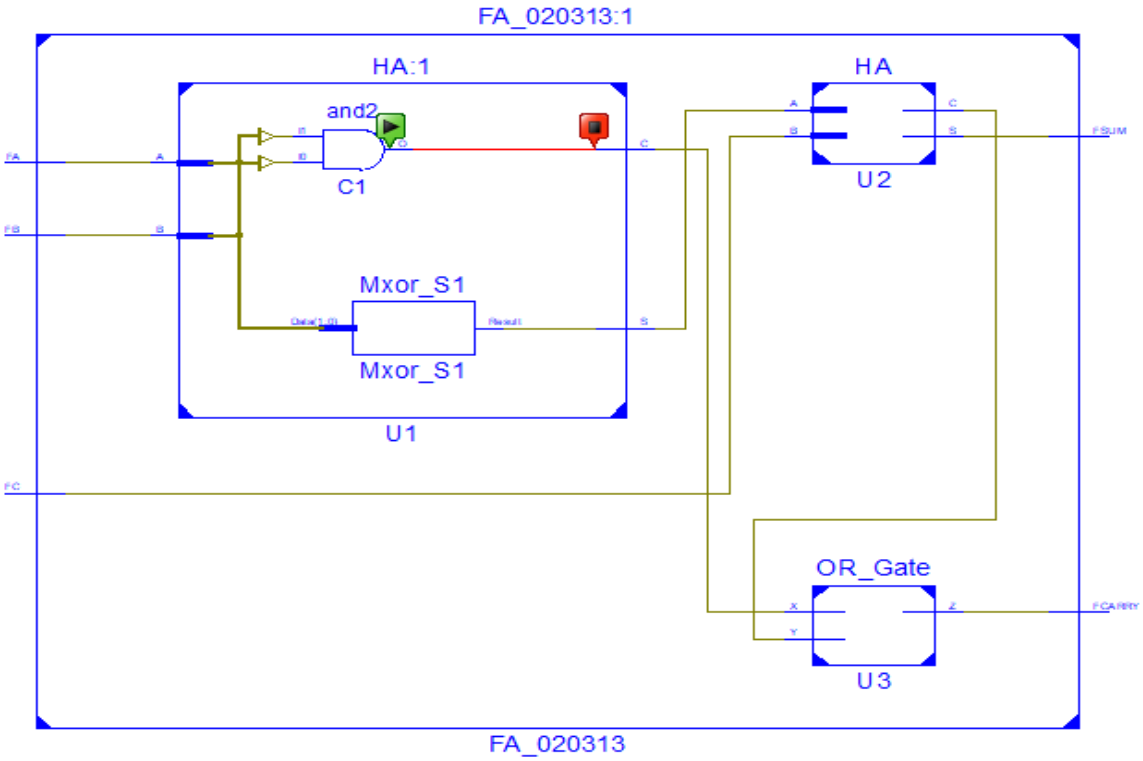

Fig 1 RTL diagram for Full Adder using Structural Modeling

Precaution:

Make sure that there are no syntax and Semantic errors.

Conclusion:

Hence, in this lab VHDL codes of structural model of Full Adder Circuit were simulated and synthesized.