ECE 4140/6240 Lab

VLSI Lab

Lab Material

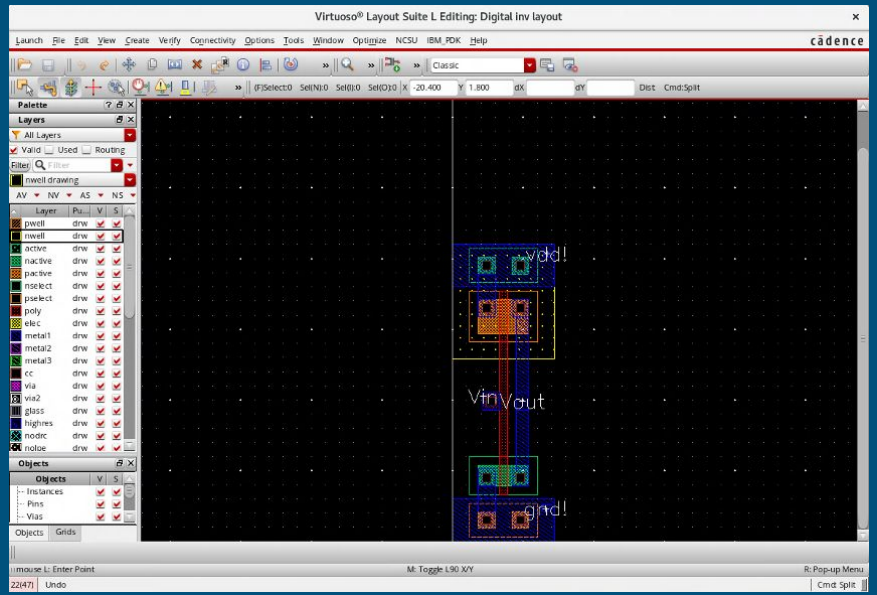
- We will be using the ECE course website provided, **blogs.gwu.edu/ece4140/**
  - password: 41406240RF

Today’s Objective

- Follow Lab #3

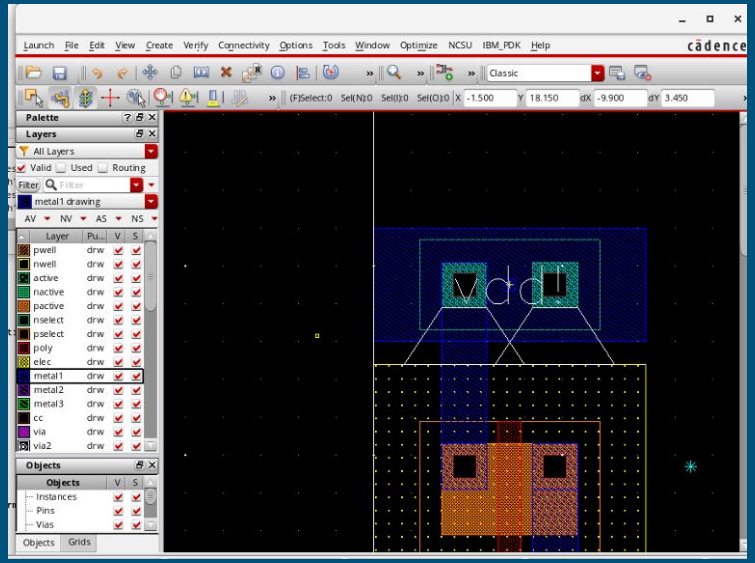
Layouts

- Manually laying down system, smaller scale than transistor level
- Allows for custom sizing of each component of transistor



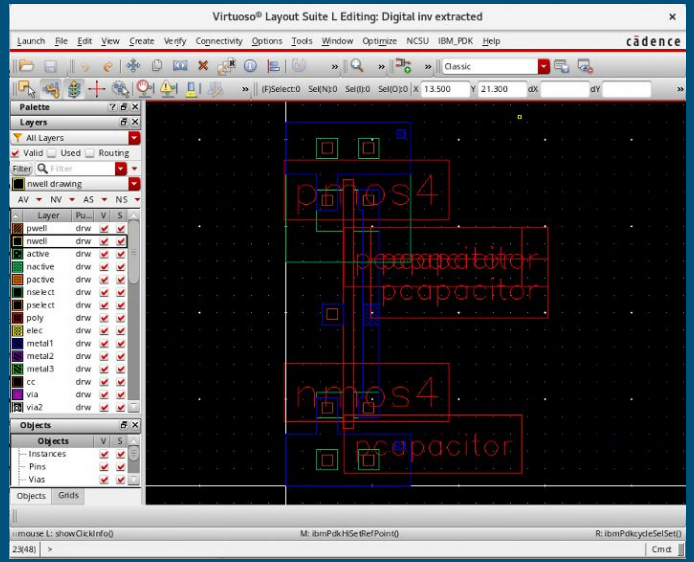
DRC

- DRC: Design Rule Check
- Runs a test to determine if design has followed all specifications of AMI C5N



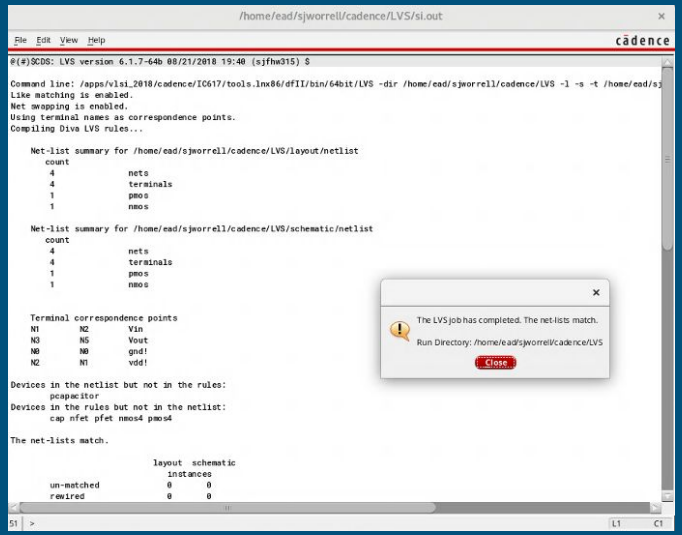
Extracted View

- Produces a view where the transistors, capacitors, etc. have been created
- Parameters for components are shown



LVS

- LVS: Layout vs. Schematic
- Runs a test to determine if the layout you have created perfectly matches the nets of the schematic



Things to watch out for

- Step 5: The picture of the measurements on the right is incorrect; disregard
- Step 9: Make sure to use the width 1.5um
- Step 10: Make sure your N-Well extends **over** the Vdd rail to the edge (the blue part)
- Lab Manual doesn't tell you to DRC until the end; consider doing it earlier to catch any issues
- If your pin names disappear (usually happens when closing and reopening the layout), open the pin menu again and they should appear
- **Pin names must match the schematic pin names, case sensitive**
- When running LVS, if it doesn't work, try having both schematic and extracted views open at the same time
- Backannoate does not work for this lab

Screenshots to include

- Overall completed layout
- “DRC Errors: 0” Window
- Extracted block layout
- Extracted parasitic layout
- LVS Match Window (“The net-lists match” text specifically)