ECE 4140/6240 – Importing PAD-Frame into Cadence
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Updated history: 12/10/21: Jerry Wu
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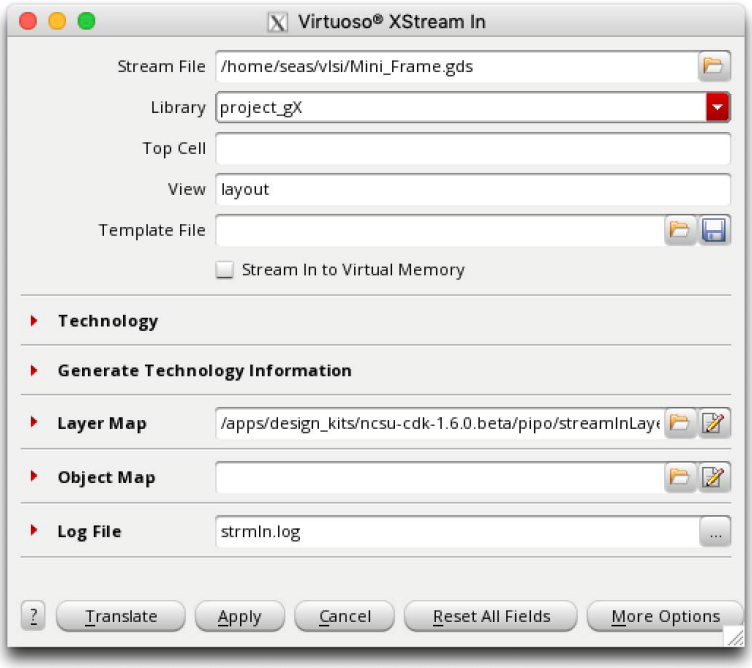
Background

The padframe structure will be discussed in the class. This tutorial will discuss how import the PAD frame and how to test your design with it.

Part 1: Import Procedure

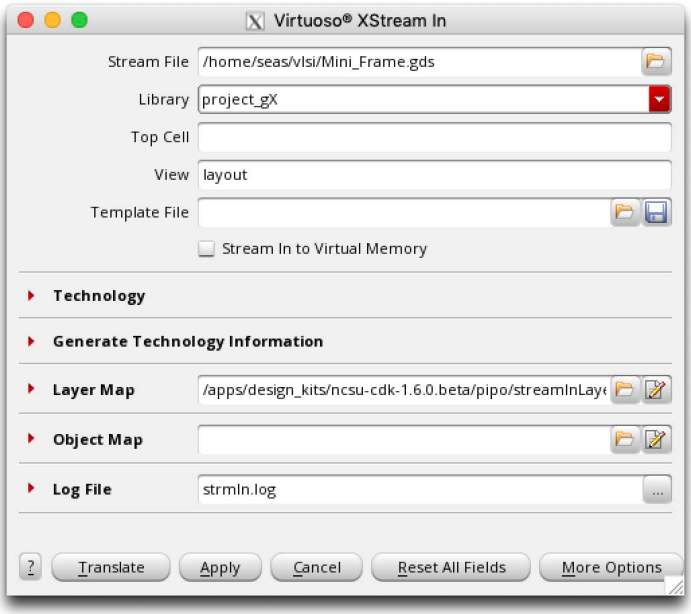
***Note**: Only 1 team member per group should follow the import procedure*

1. Start Cadence
2. From the CIW, choose: File->import->Stream
3. Fill in the window as follows (change project_gX to your group's project library name)



4. For the Stream File, browse to the following directory & file:

   /home/seas/vlsi/Mini_Frame.gds

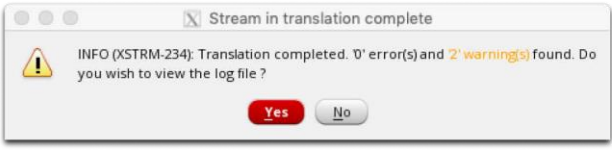


5. For layer Map, browse to the following directory & file:

   /apps/design_kits/ncsu-cdk-1.6.0.beta/pipo/streamInLayermap

Click Apply

6. You will see the stream in translation complete, ignore the warnings and click Yes, and close the strmln.log window.

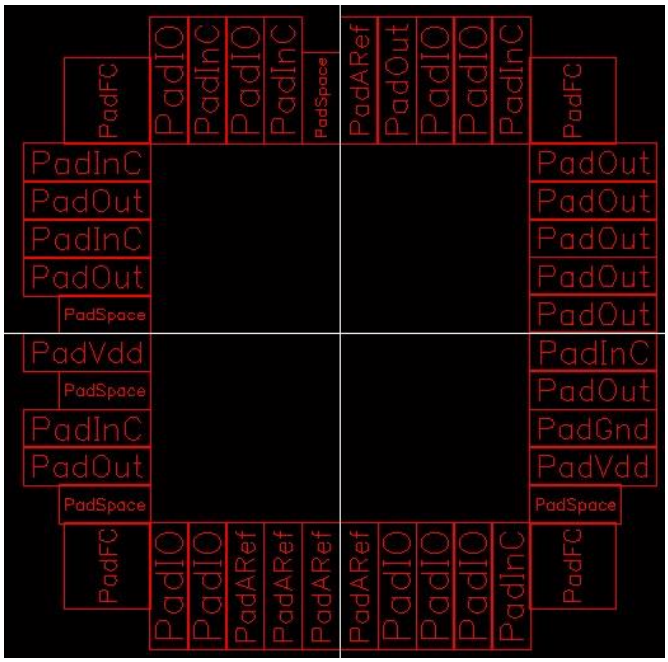


The translation process will yield 15 errors and 1 Warning. This # is okay, but no more. If you have more than 15 errors and 1 warning, look at the CIW to determine what went wrong before continuing.

7. After it has completed the import, click on the Library Manager, and open:

   Project_gX->Mini_Frame

8. Press <shift> f and you should see the following:


PadFC
PadIO
PadInC
PadIO
PadInC
PadSpace
PadARef
PadOut
PadIO
PadIO
PadInC
PadFC
PadInC
PadOut
PadInC
PadOut
PadSpace
PadOut
PadOut
PadOut
PadOut
PadVdd
PadSpace
PadInC
PadOut
PadSpace
PadInC
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PadGnd
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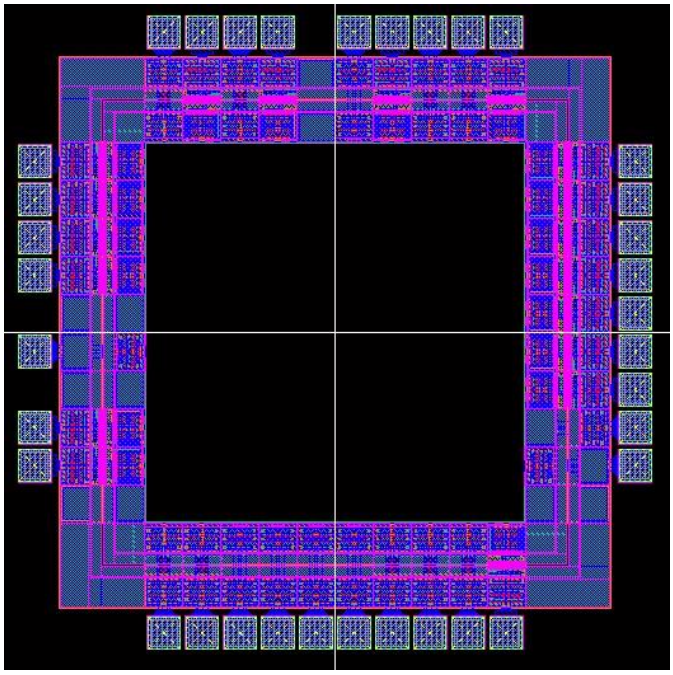
PadInC
PadFC

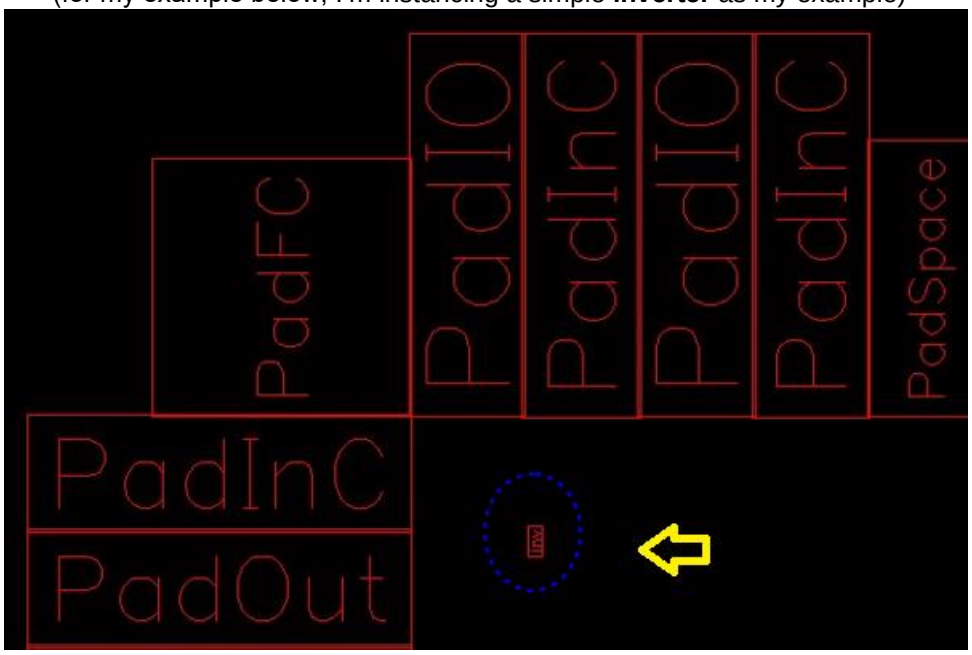


Part 2: PAD Connection and PIN placement procedure

This procedure should only be followed AFTER your final design is complete

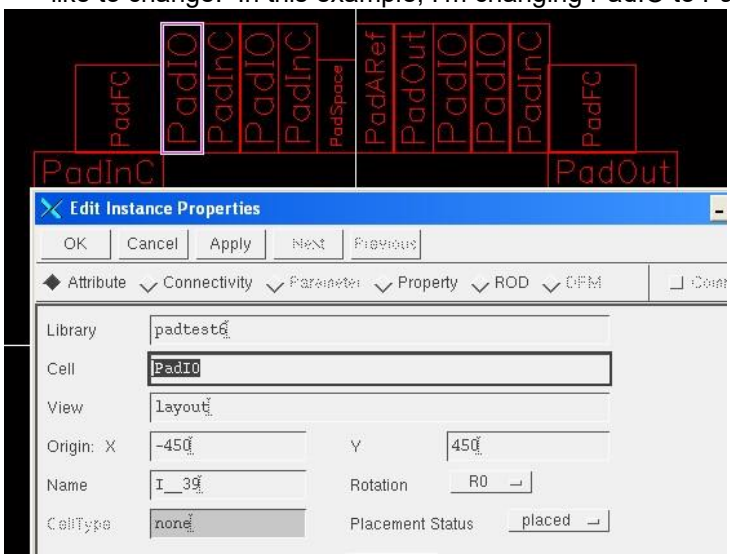
1. Open up the cell: project_gX -> Mini_Frame

2. Instance your FINAL design in the center of the PAD Frame
   (for my example below, I'm instancing a simple **inverter** as my example)

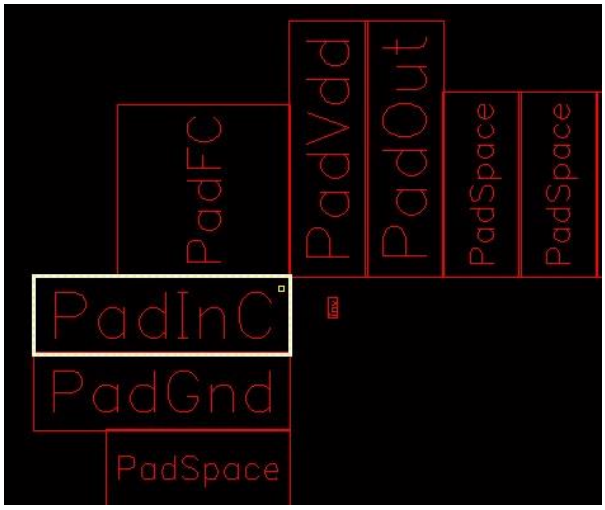


3. There are several different types of PADS, you will need to change their order to meet your project's needs
   a. PADINC is an input PAD
   b. PADOUT is an output PAD
   c. PADVDD is the VDD PAD
   d. PADVDD is the VDD PAD
   e. PADGND is the GND PAD
   f. PADSPACE is a "SPACER" pad for unneeded input pins

4. To change a PAD to a different type, click on the PAD, press "**q**" and type the name of the PAD you'd like to change. In this example, I'm changing PadIO to PadVdd

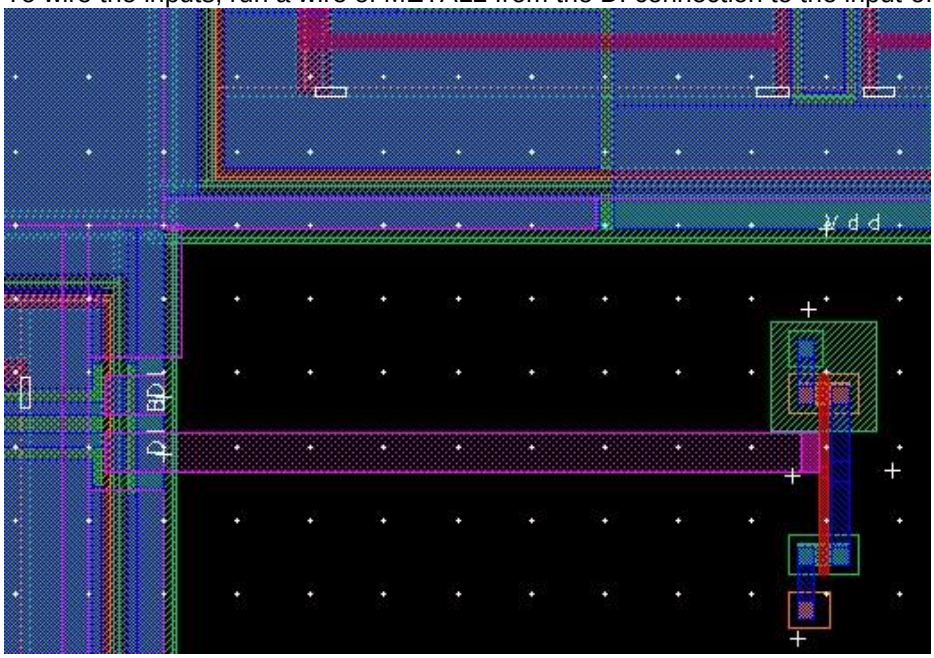


5. In this example (for the inverter), we will need a PADINC, PADOUT, PADVDD, and PADGND, in your project, you'll need to determine where to put PadInC, PadOut, and PadVdd depending on your design.

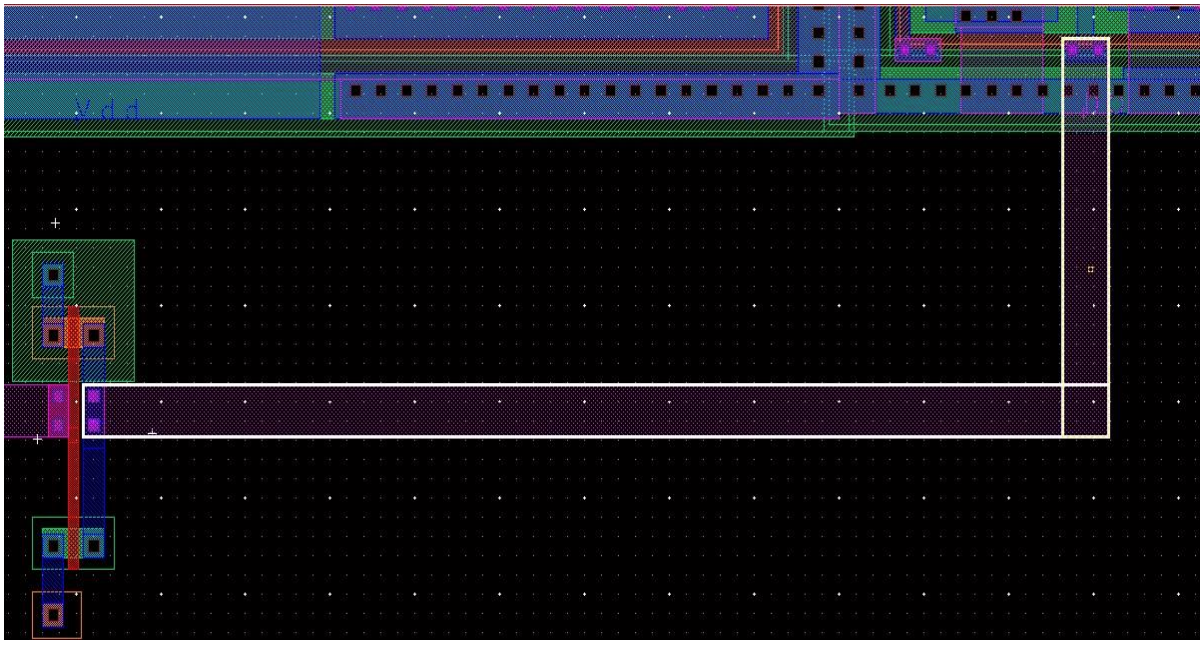


6. Zoom in on the **PADINC** (the side that faces your design), you will notice two strips of metal 2
   One is marked: **DI** (means DATA IN)
   One is marked: **BDI** (means DATA IN BAR – the inverted input)

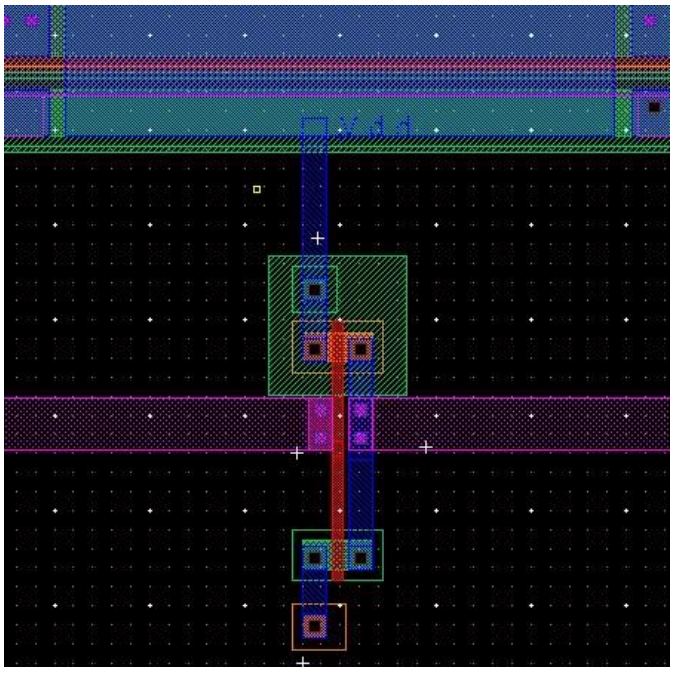
7. To wire the inputs, run a wire of METAL2 from the DI connection to the input of your design:



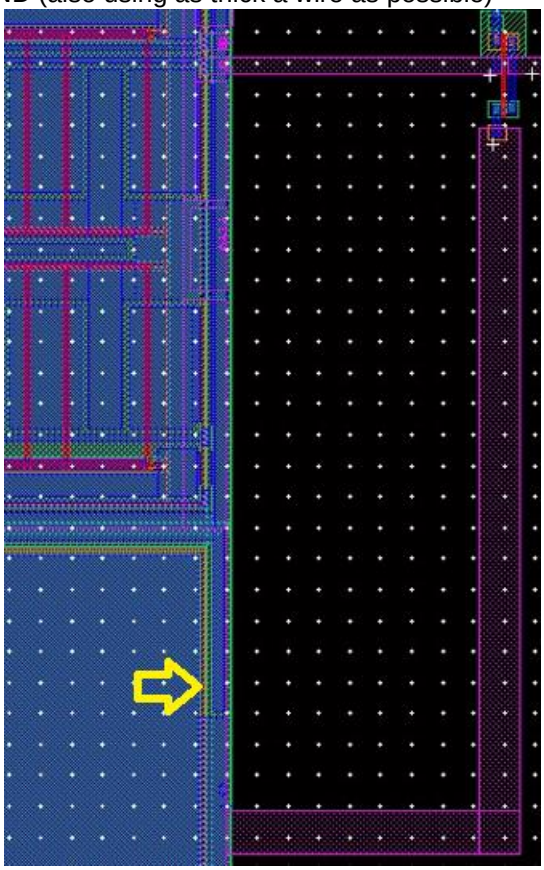
8. To wire the outputs, run a wire of METAL 2 from your output the **DO** connection on a PADOUT



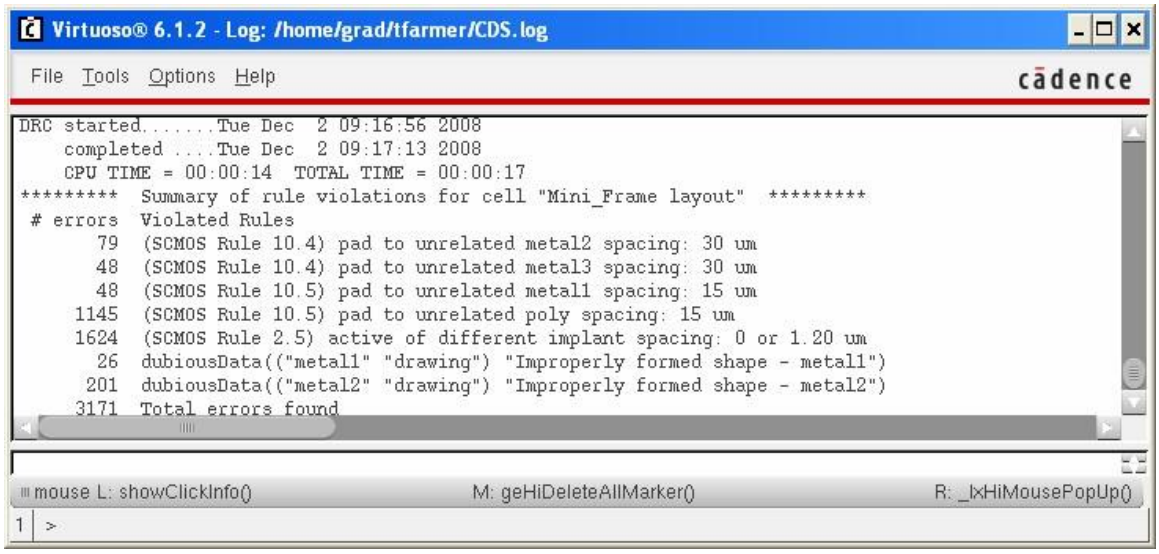
9. Wire VDD (use as thick a wire as possible!)



10. Wire GND (also using as thick a wire as possible)

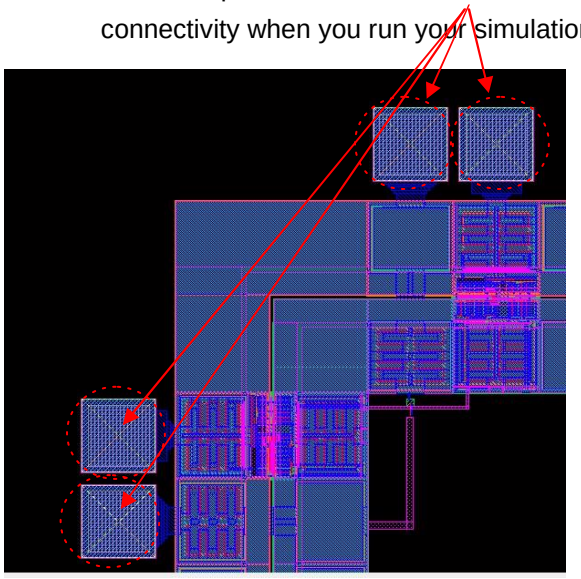


11. The DRC's from the PAD-FRAME are allowed by MOSIS, but your design, and all wires leading to and from it, MUST be DRC free for MOSIS to accept your design for fabrication.

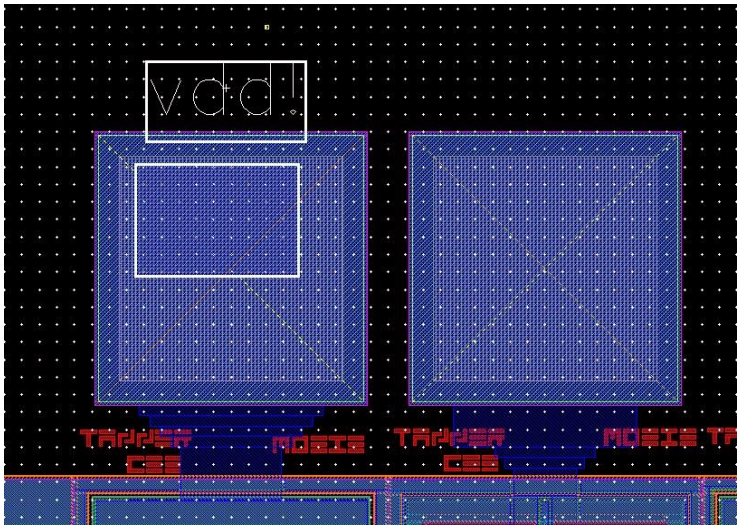


12. The next step is to place PINS on the PADS themselves.

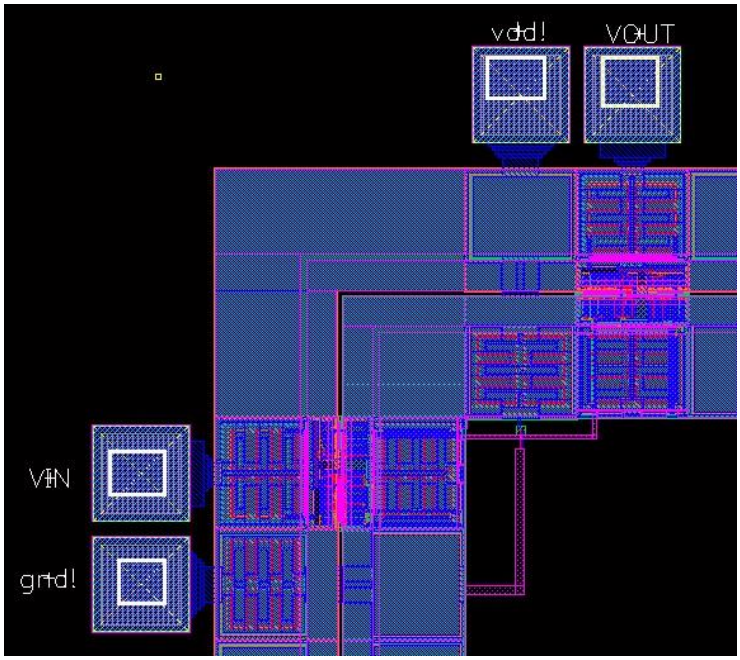
    - You must place PINS, on the **outer most** portion of the PADS. This will ensure electrical connectivity when you run your simulation on the extracted view of the design



13. Place a ***vdd!*** **JUMPER** pin, and a ***gnd!*** **JUMPER** pin. The PADS are metal1, choose metal1 when creating your **JUMPER** pin



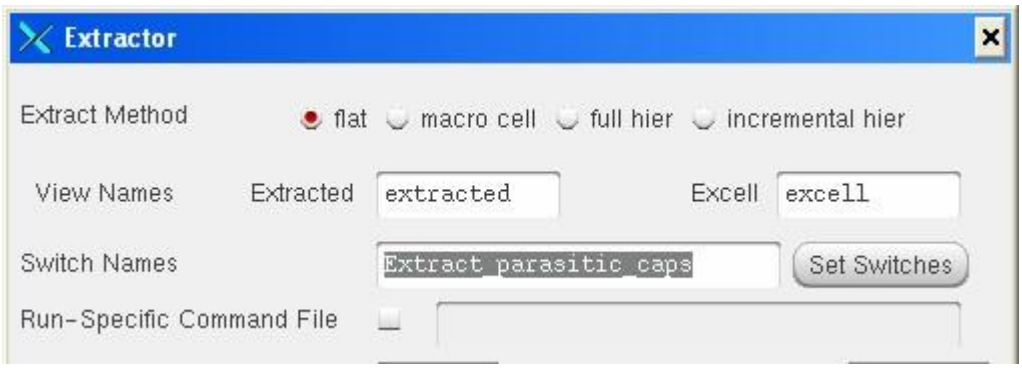
14. Place INPUT and OUTPUT pins that correspond to the PIN names you've used in your design. Once complete, you should have something similar to the following example:



- For a CLK, you would use a pin of type: Input, and a PAD of type PadInC.
- There was no CLK pin for the example above as it was just an inverter.

Part 3: Simulating your chip including the PAD-FRAME Parasitics

1. After you've finished connecting the PAD-FRAME to your design, run the extraction tool to generate an exacted view. Be sure to remember to set the switch: Extract Parasitic Caps

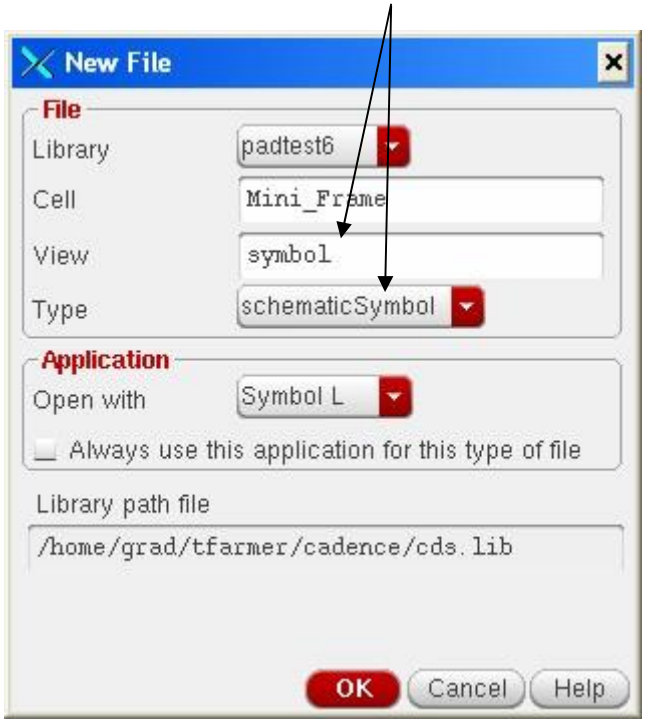


Ensure that there are 0 errors after the extraction is complete (see the CIW window)

2. Close the layout and extracted views

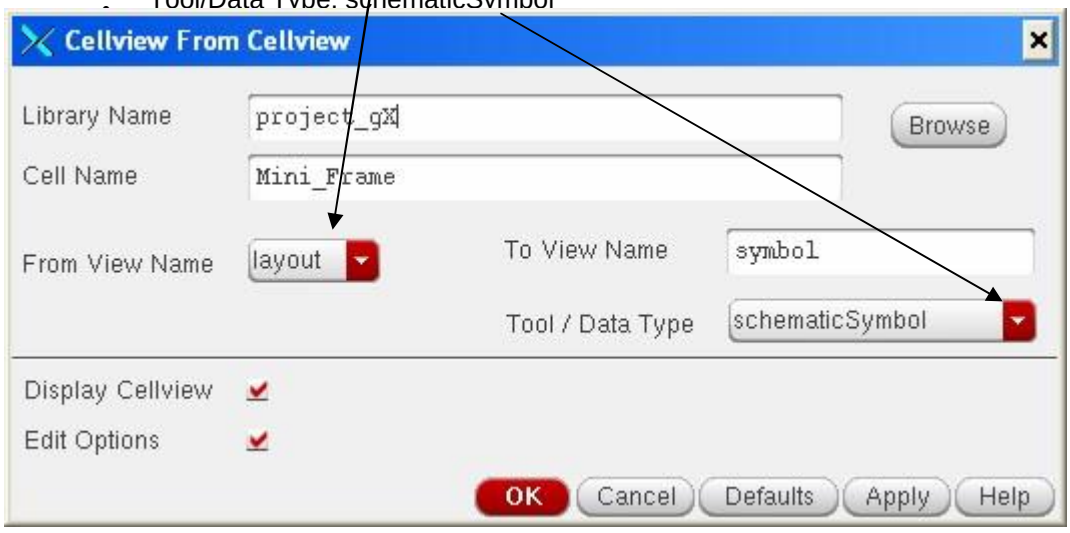
3. From the Library Manager, click on the MiniFrame cell in your project library
(in my example, my library is "padtest6" your library will be project_gX)

4. Create a cell with View: **SYMBOL**



5. Once the symbol editor opens from the menu, choose: Create->Cellview->From Cellview

- Update the window as follows
- From View Name: LAYOUT
- Tool/Data Type: schematicSymbol

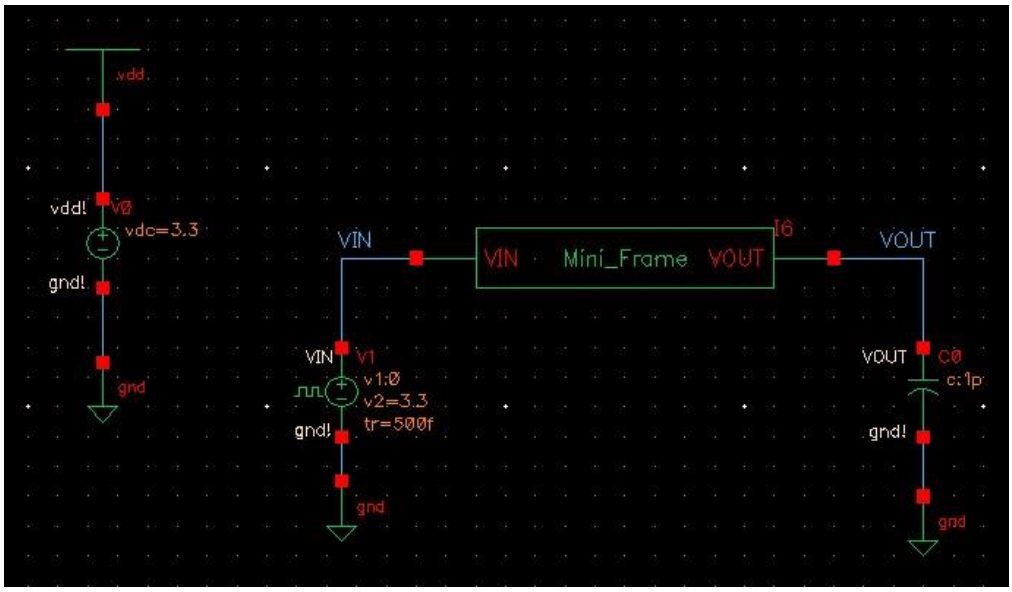


- Choose: REPLACE when this box comes up:

- In the example of the Inverter below, I have only a VIN and VOUT set of pins, you will have nearly 40 pins!

- Once complete, save the symbol and exit the symbol editor

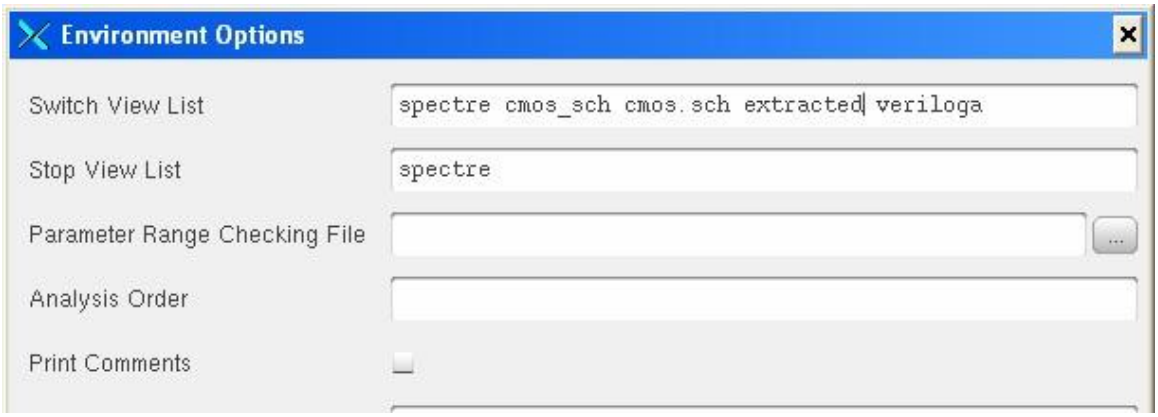
6. Instance your new symbol in your existing project test bench. In this example, I have a simple input pulse, in your simulations, you will probably have a verilog driver for your design. If you are using verilog, don't forget to update your "config" view



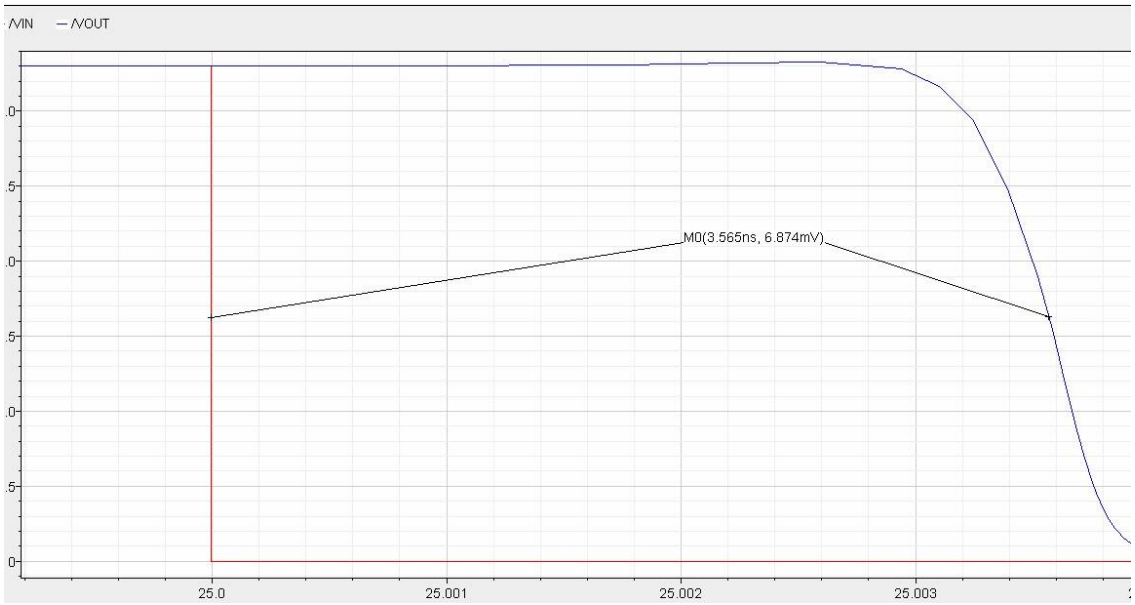
7. Launch the simulator. Load any saved state you may have for your simulation

8. From the simulator menu, choose: Simulation->Environment

9. Remove “schematic” from the Switch View List, and replace it with “Extracted”, then press OK



10. Run the simulation. You will now see a much larger propagation delay. It may require you to increase your CLK period to account for the propagation delay that the PAD-FRAME has introduced.


/VIN
/VOUT
M0(3.565ns, 6.874mV)
25.0
25.001
25.002
25.003