



ECE 4140/6240 Lab



VLSI Lab



Lab Material

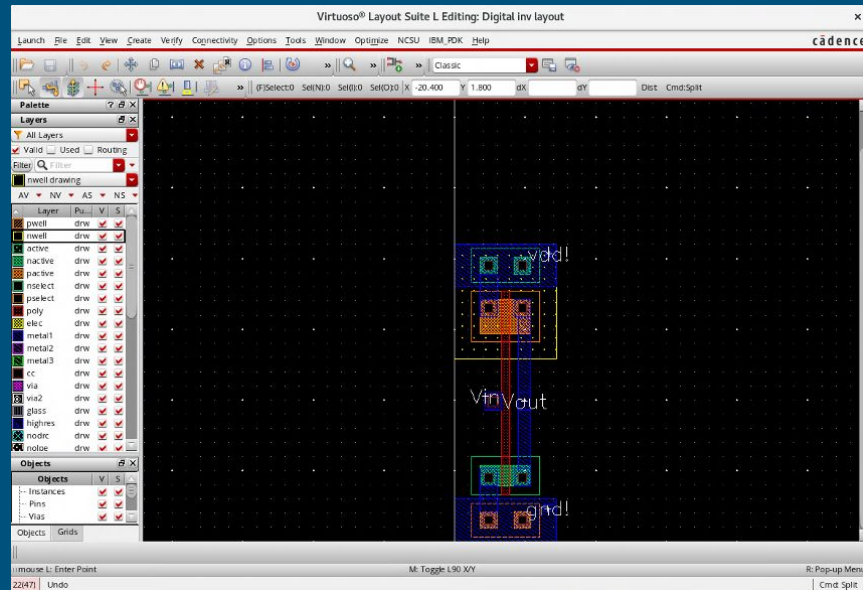
- We will be using the ECE course website provided, blogs.gwu.edu/ece4140/
 - password: 41406240RF

Today's Objective

- Follow Lab #3

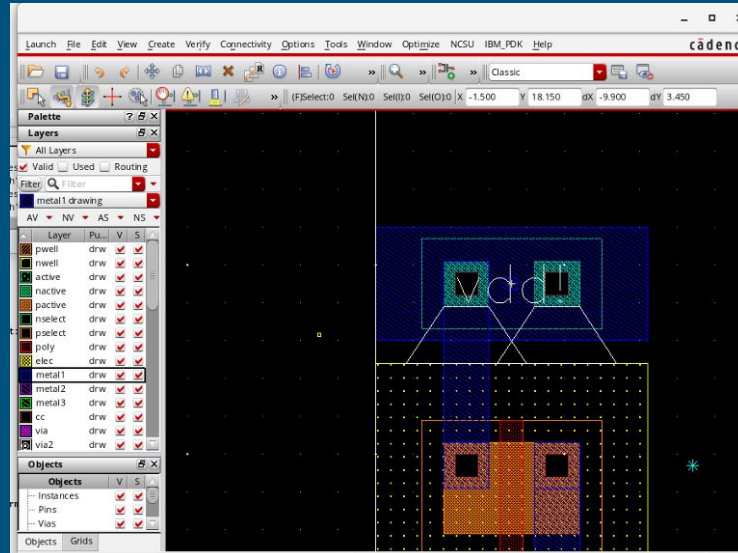
Layouts

- Manually laying down system, smaller scale than transistor level
- Allows for custom sizing of each component of transistor



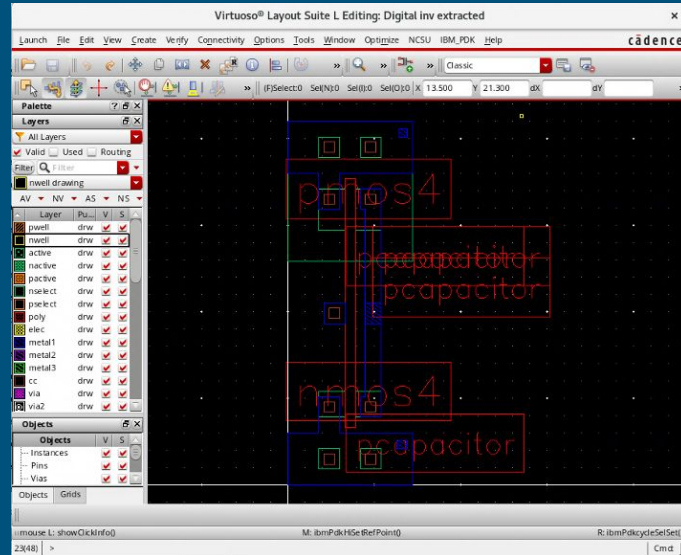
DRC

- DRC: Design Rule Check
- Runs a test to determine if design has followed all specifications of AMI C5N



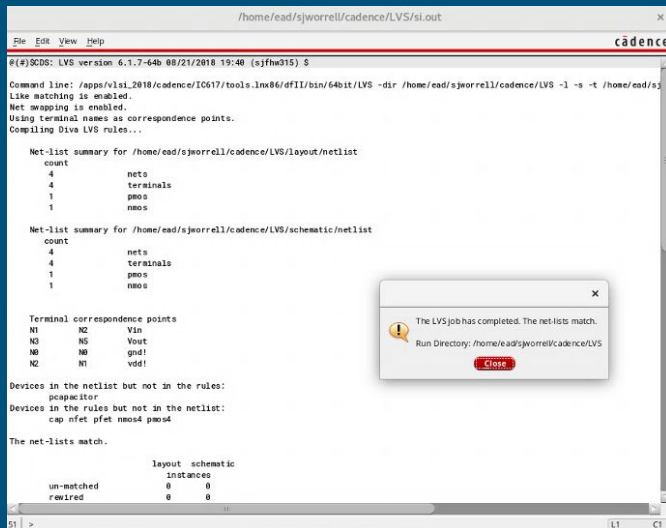
Extracted View

- Produces a view where the transistors, capacitors, etc. have been created
- Parameters for components are shown



LVS

- LVS: Layout vs. Schematic
- Runs a test to determine if the layout you have created perfectly matches the nets of the schematic



The screenshot shows the Cadence LVS tool window with the following text:

```
File Edit View Help
P(4)SCDS: LVS version 6.1.7-64b 88/21/2018 19:40 [sjfh315] $

Command line: /apps/vlsi_2018/cadence/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir /home/eas/sjworrell/cadence/LVS -l -s -t /home/eas/sjworrell/cadence/LVS
Like matching is enabled.
Net sweeping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/eas/sjworrell/cadence/LVS/layout/netlist
count
4      nets
4      terminals
1      pmos
1      nmos

Net-list summary for /home/eas/sjworrell/cadence/LVS/schematic/netlist
count
4      nets
4      terminals
1      pmos
1      nmos

Terminal correspondence points
N1      N2      Vin
N2      N3      Vout
N0      N0      gnd!
N2      N1      vdd!

Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos1 pmos1

The net-lists match.

              layout schematic
              instances
un-matched      0      0
required        0      0
```

A small dialog box is overlaid on the right side of the window, containing the message: "The LVS job has completed. The net-lists match. Run Directory: /home/eas/sjworrell/cadence/LVS" with a "Close" button.

Things to watch out for

- Step 5: The picture of the measurements on the right is incorrect; disregard
- Step 9: Make sure to use the width **1.5um**
- Step 10: Make sure your N-Well extends **over** the Vdd rail to the edge (the blue part)
- Lab Manual doesn't tell you to DRC until the end; consider doing it earlier to catch any issues
- If your pin names disappear (usually happens when closing and reopening the layout), open the pin menu again and they should appear
- **Pin names must match the schematic pin names, case sensitive**
- When running LVS, if it doesn't work, try having both schematic and extracted views open at the same time
- **Backannoate does not work for this lab**

Screenshots to include

- Overall completed layout
- “DRC Errors: 0” Window
- Extracted block layout
- Extracted parasitic layout
- LVS Match Window (“The net-lists match” text specifically)