CSE/EEE120
Final Exam

Name:_____**ASU ID:**_____

You have 1 hour and 50 minutes to complete and turn in this quiz (allow approximately 30 minutes for the multiple choice questions). Please read questions carefully and provide the answers in the form requested. SHOW YOUR WORK. Good luck!

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1. Given the truth table for function ***f***, answer the questions below (4 points each, 40 points total):

Line #	a	b	c	f
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

(a) Write function ***f*** in the canonical SOP and POS forms.

$$f = a'b'c + a'bc + ab'c' + ab'c + abc' + abc$$

$$f = (a+b+c)\cdot(a+b'+c)$$

(b) Write function ***f*** in short-hand (numerical) notation *(both SOP and POS forms).*

$$f = \Sigma m(1,3,4,5,6,7)$$

$$f = \Pi M(0,2)$$

(c) Reduce function ***f*** to a minimal form using whatever method you prefer.

a b	c = 0	c = 1
0 0	0	1
0 1	0	1
1 1	1	1
1 0	1	1

$f = a + c$

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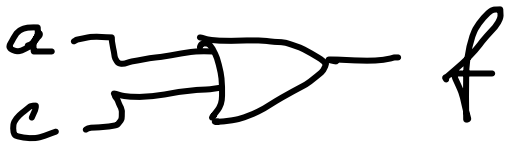
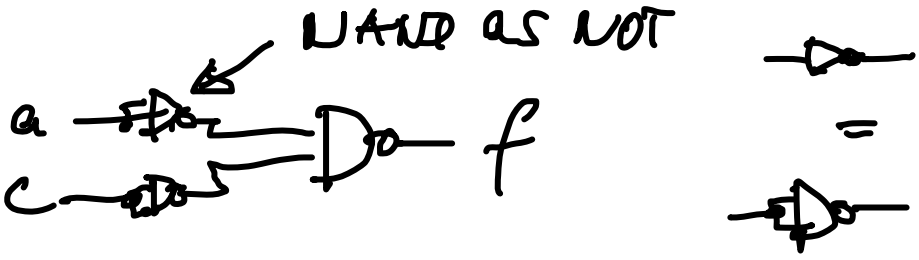
(d) Draw the logic circuit for the minimal form of function ***f*** obtained from part (c) using AND/OR/NOT gates. Make sure to label <u>all</u> wires correctly, including the interior wires. Assume only <u>uncomplemented</u> variables are available.



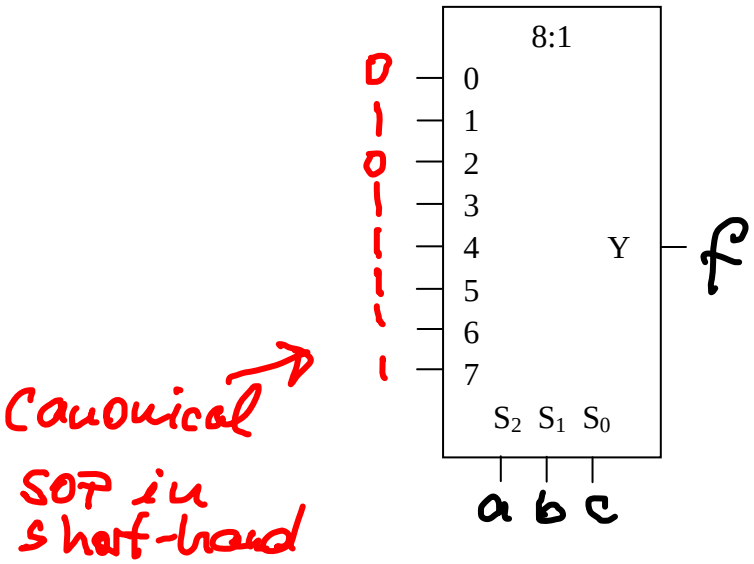
(e) Implement ***f*** using <u>only</u> NAND gates. Only uncomplemented inputs are available.



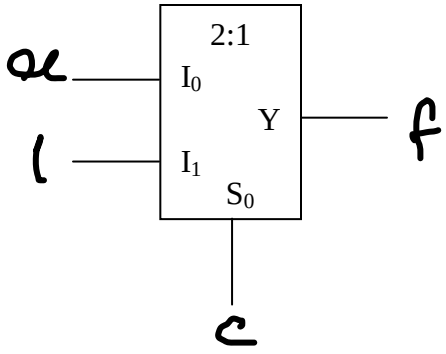
$f = a + c = (a' \cdot c')'$

NAND with inverted inputs

(f) Implement ***f*** using <u>only</u> an 8:1 MUX.



(g) Implement ***f*** using <u>only</u> a 2:1 MUX, using no additional logic gates.



$Y = \bar{I_0} \cdot \bar{S_0} + I_1 \cdot S_0$

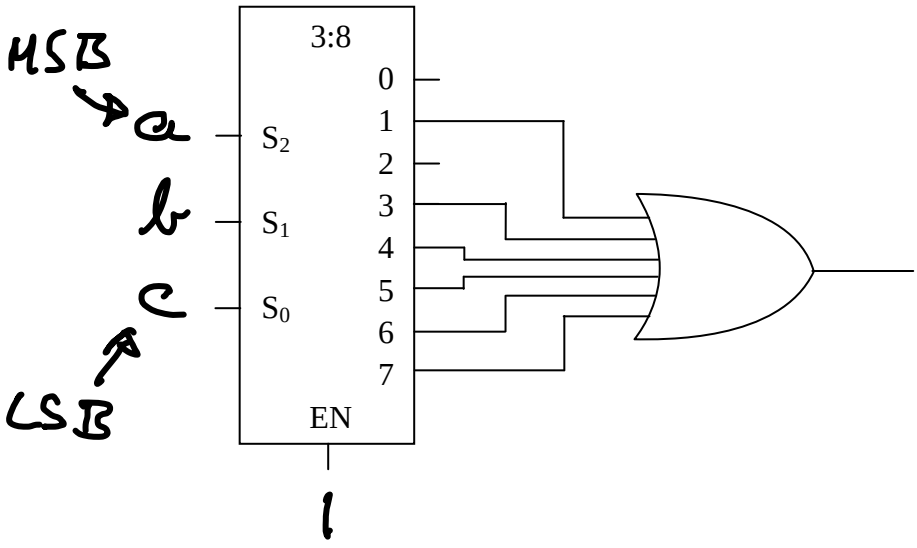
$= a + c$

$= I_0 \cdot \bar{c} + I_1 \cdot c$

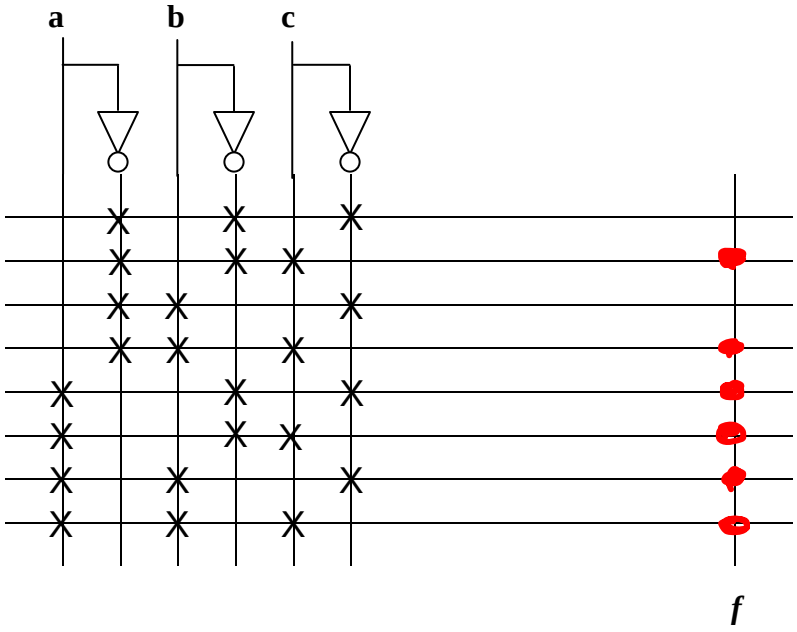
$= a \cdot \bar{c} + c$

$= a + c$

(h) Implement ***f*** using a 3:8 decoder and whatever logic gates you need.



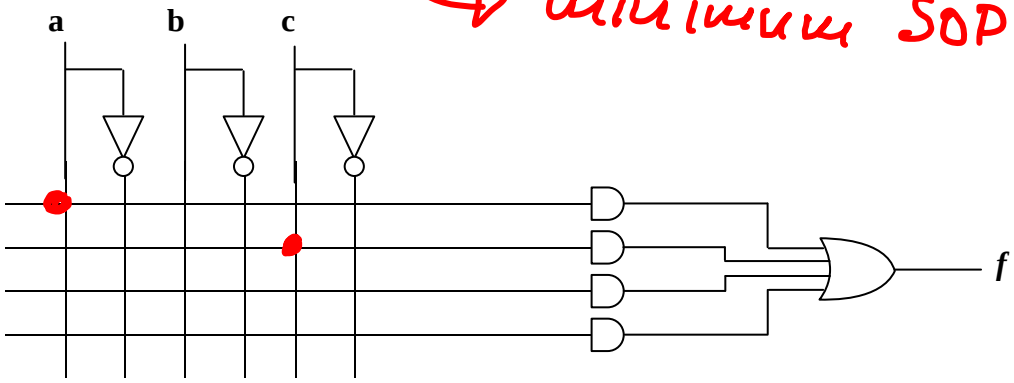
(i) Using the diagram provided, make the appropriate links to implement function ***f*** in a 3 - input, 1-output PROM.



Canonical SOP in short-hand

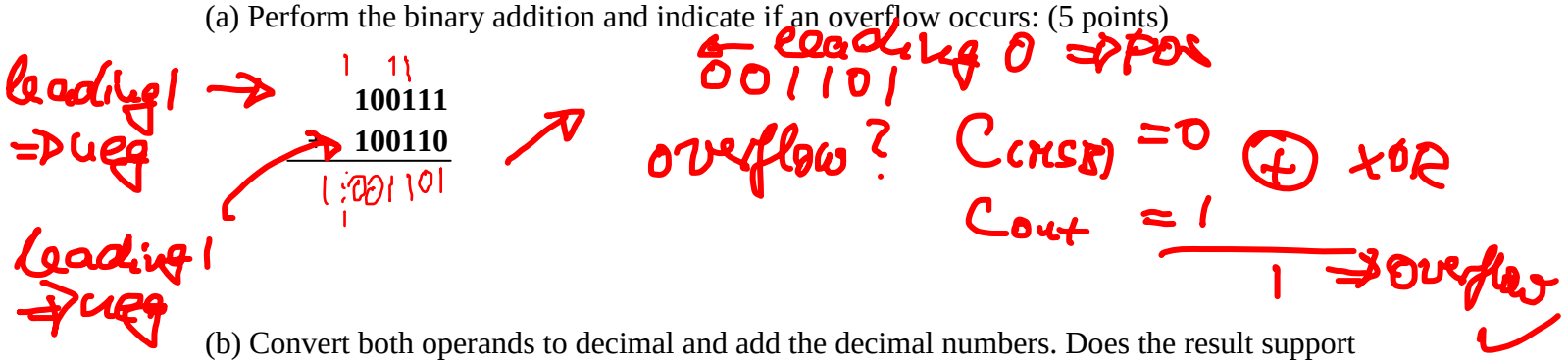
(j) Using the diagram provided, make the appropriate links to implement function ***f*** in a 3-input, 1-output PAL.

minimum SOP from part (c)

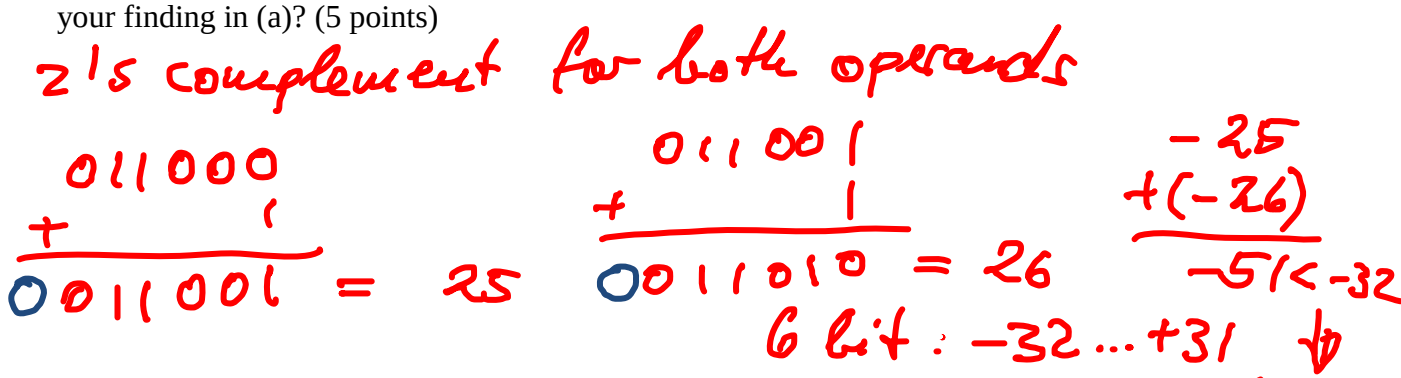


2. Assume that we have to add two 6-bit numbers in 2's complement form.

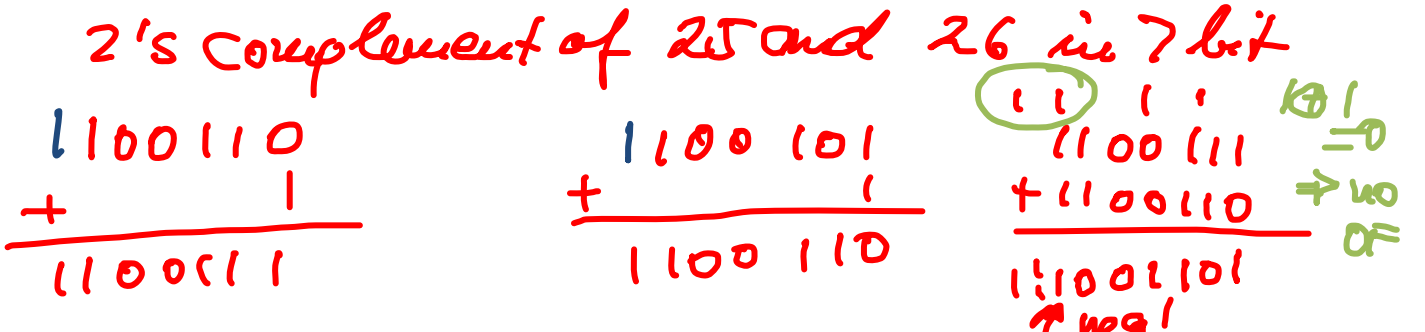
(a) Perform the binary addition and indicate if an overflow occurs: (5 points)



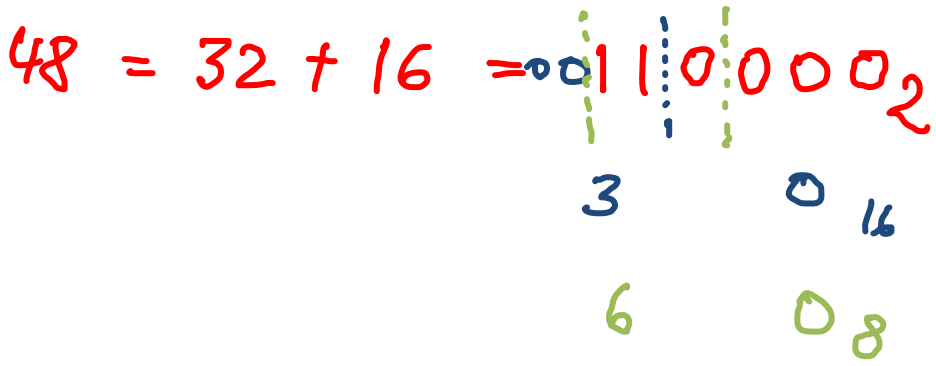
(b) Convert both operands to decimal and add the decimal numbers. Does the result support your finding in (a)? (5 points)



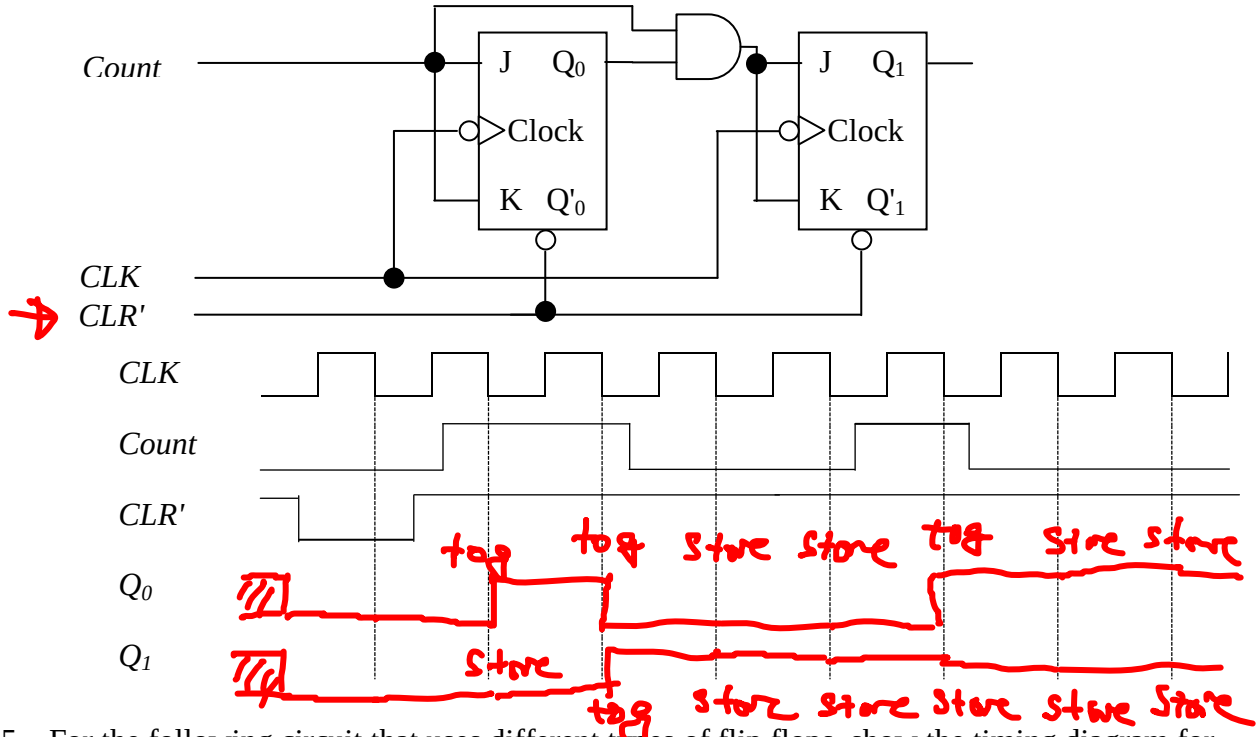
(c) Convert both operands to positive binary numbers using 2's complement arithmetic. Then, convert them to 7-bit numbers by adding a zero on the left side (MSb). Convert them again to negative numbers and perform the binary addition just as in (a). Does the overflow still occur? (5 points)



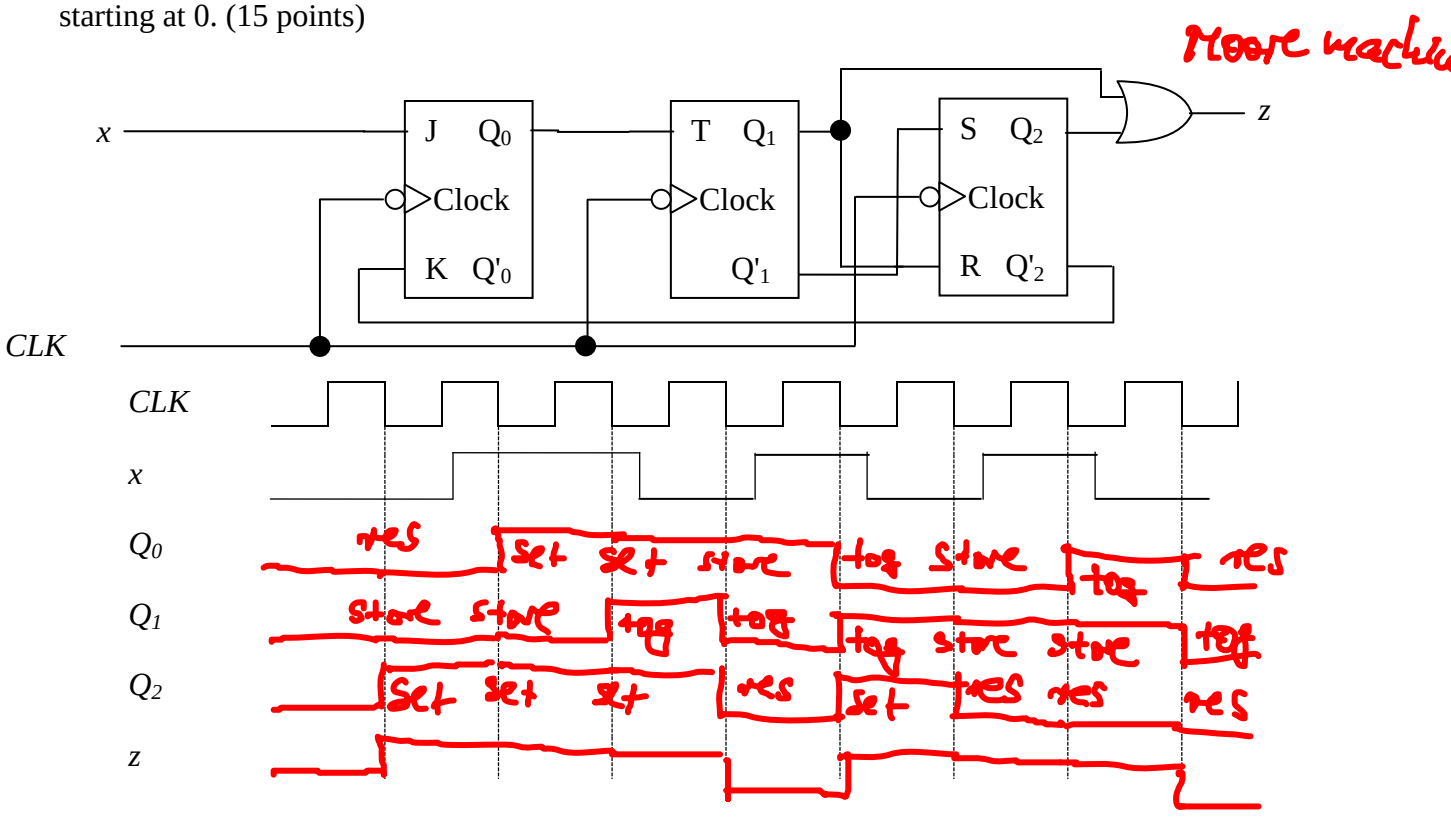
3. Write the decimal number 48 in (a) binary form, (b) hexadecimal form, and (c) octal (base-8) form. (4/3/3 points each, 10 points total)



4. For the following circuit that uses two *JK* flip flops with an active low clear (reset), show the timing diagram for Q_0 and Q_1. The flip flop is negative-edge triggered, just like the one used in the hardware labs. (10 points).



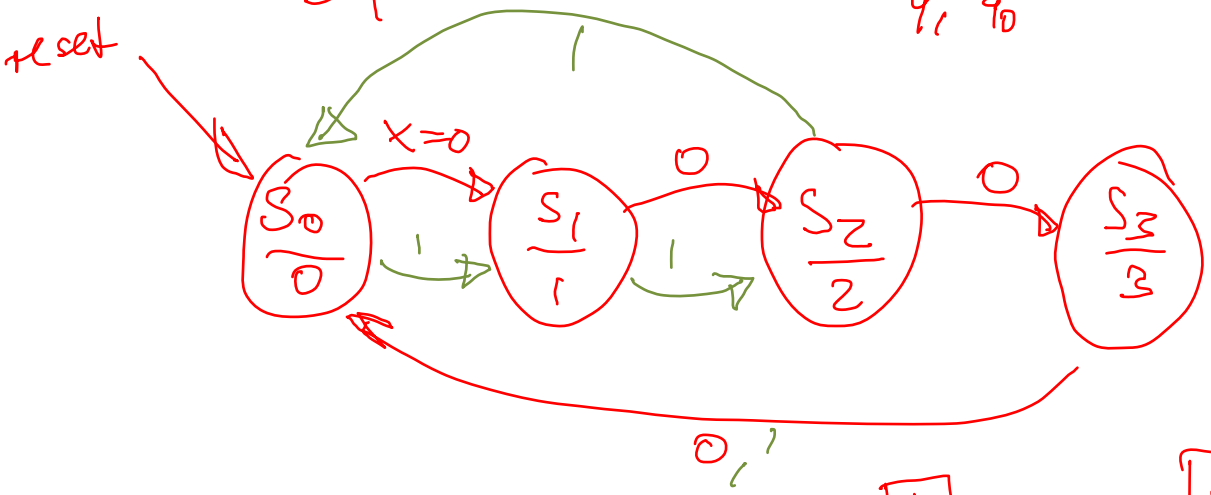
5. For the following circuit that uses different types of flip flops, show the timing diagram for the output z. The flip flops are negative-edge triggered. Assume that all flip flops are initially starting at 0. (15 points)



6. Design a **synchronous counter** that counts 0, 1, 2, 3, 0, 1, ... (divide-by-4 counter) when an input x = 0, and counts 0, 1, 2, 0, 1, ... when x = 1 (divide-by-3 counter) using **(a) *D* flip-flops and (b) *JK* flip-flops**.

   Note: You need to show the state definition table, the state transition diagram, the state transition table, the K-maps for the respective logic functions and the schematic of the implementation using flip-flops and logic gates in (a) as well as the K-maps for the logic functions and the schematic in (b). (5 points each, 35 points total)

State	Def	Bin
S_0	count = 0	0 0
S_1	1	0 1
S_2	2	1 0
S_3	3	1 1
		q_1 q_0



x	q_1	q_0	q_1^+	q_0^+
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0

D_1

x q_1 \ q_0	0	1
0 0	0	1
0 1	1	0
1 1	0	0
1 0	0	1

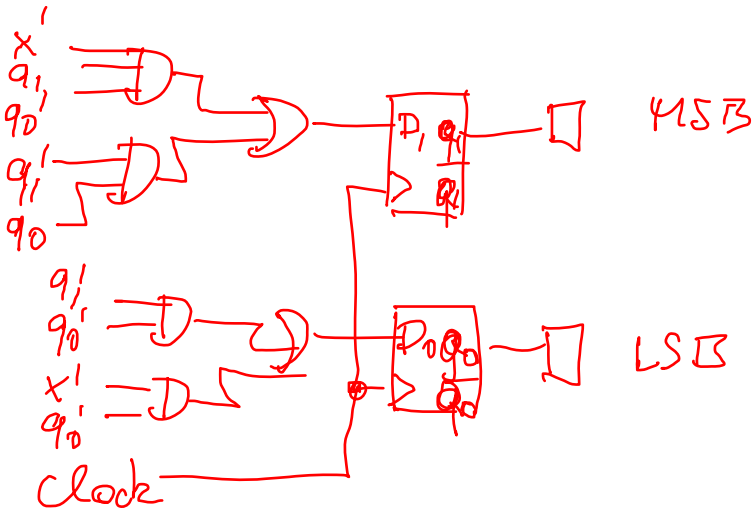
$D_1 = x' q_1 q_0' + q_1' q_0$

D_0

x q_1 \ q_0	0	1
0 0	1	0
0 1	1	0
1 1	0	0
1 0	1	0

$D_0 = q_1' q_0' + x' q_0'$

$J_1 = q_0$ $K_1 = x + q_0$ $J_0 = q_1' + x'$ $K_0 = 1$



7. Is the following circuit a Moore or a Mealy machine? Explain your answer! (5 points)