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Regular paper

Embedded Switched boost multilevel inverter forPV-fed single-phase grid

In the field of photovoltaic (PV) based energy utilization, grid-connected PV has achieved growing importance in recent times. Relating to that, this paper aims to analyze and design a symmetrical high-gain multilevel inverter (MLI) using an embedded type z-source inverter with a modular H-bridge. The developed inverter is used for connecting the PV system to a single-phase power grid. With the optimal shoot-through duty cycle, selected from a brief comparison of base inverters, the characteristic equations of the developed MLI are derived and its suitability in a single-phase grid-connected PV system is studied. The simulation study of the proposed inverter using MATLAB/Simulink is carried out with the multicarrier pulse width modulation (MC-PWM) and connected to the grid with a phase-locked loop (PLL) for the synchronization of the grid outputs with those of the inverter. The results are then verified and the outputs are presented.

Keywords: Power grid; Switching converters; DC-AC power converters; Power conditioning; System performance.

1. Introduction

Thestudies based on renewable energy generation are considered imperative as the energy demandhas been rising regularly. A major portion of the study involves Photovoltaic (PV/solar) energy-based generation and utilization [1]. While considering the utilization of the PV (or any renewable energy source), the integration of such renewable systems with the utility grid is considered to be of great benefit and the same is attracting much attention in many developing countries, especially for utilizing the excess power from any domestic/industrial PV systems. In these cases, a single-phase grid-connected system is a fitting solution for lowpower rated PV systems [2],[3]. As such connecting a PV system with any kind of application requires a power conditioner (PC) to regulate the power flow against the effects of partial shading. Many previous works have established that the effect of partial shading, irrespective of the array configuration is mainly observed in PV current [4]. This leads to a current difference between the shaded and unshaded panels, which may damage the panels and collectively affect the output PV power.

Hence, to lessen the damage due to the considerable current difference through the PV modules, a simple series-parallel type array with fewer series-connected and more parallel-connected modules isconsidereda cost-effective solution. The variation of the current outputs under different radiation are shown in fig.1, for better understanding. As a result, this PV array setup supplies lower PV voltage (V_{pv}) and higher current (I_{pv}) to meet the required power rating (P_{pv}).Relating to this, this work focuses on developing a high again inverter, to boost and feed the PV voltage to the single-phase grid.

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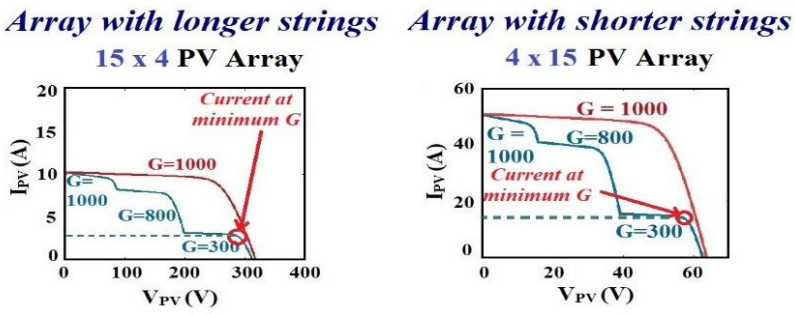


(a) (b)

Fig.1 PV array of 2 kW with (a) longer series string and (b) shorterseries string

Lately, owing to continuous research, many new types of inverters that achieve both boosting and converting, have been studied and added to the existing reservoir of literature. The focus has been on reducing the size and the cost of the PC as the power rating of the overall system is increased [5],[6].As such in many high-power industries, multilevel inverters (MLIs) are employed for applications that require high power from low/medium power sources, since high power sources could affect the reliability of the machine. They provide a promising edge over the conventional three-level inverter by giving better output waveforms with enhanced efficiency and easy control. Yet the studies and implementation of MLIs are limited to certain applications and their usage in grid-connected systems is still in the developing stage. From the basic types of MLI, many modifications are being studied to make multilevel inverters more feasible for domestic applications. One such type is the cascaded H-bridge MLI (CHb-MLI) consisting of series-connected power conversion cells (an H-bridge inverter) each of which is powered from separate sources; it has gained more attention in this area of research as it is more suited to renewable energy-connected grid systems, particularly where hybrid renewable resources are used [7],[8].

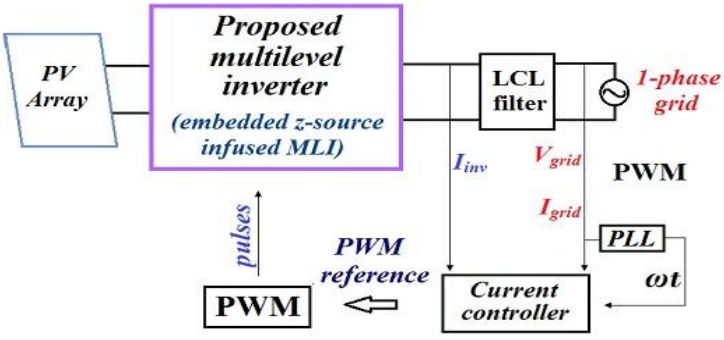


Fig.2 Overall block diagram

Though many new MLIs are being proposed, the study on using existing inverters to achieve a more reliable cascaded type MLI is still limited. Relating to this, this work will focus on obtaining a cascaded type MLI using a high gain, three-level inverter. The suitability of the proposed five-level inverter for grid application will be studied using simulation and the results will be discussed. The overall work reported in this paper is presented in the form of a block diagram in Fig. 2. Thus, the embedded switched boost

inverter will replace the power conversion cells in CHb-MLI; the MLI will be designed to feed a single-phase grid with the help of a suitable PV grid synchronization system.

2. Analysis of theProposed MLI

In the following sections, the basic analysis of the existing embedded switched boost (E-SBI) inverter topology combining the features of both embedded z-source and switched boost inverter is discussed (section 2.1). The proposed MLI using ESL-SBI is discussed and its characteristic equations are derived in sections 2.2 and 2.3 respectively, followed by the multicarrier PWM method used for pulse generation in section 2.4. Section 2.5 makes a brief comparison of the proposed MLI with other MLIs to have a better understanding of its advantage over the existing ones.

2.1 Embedded Switched-inductor Switch Boost Inverter (ESL-SBI)

Being the center of many power converters,the main purpose of introducing Z-source inverters (ZSI) was to combine the converters into one using the concept of shoot-through (ST) making it highly reliable. Having ZSI as a base, many inverters have been studied in the literature, one of which is the switched boost inverter [9] that best combines the properties of the boost converter and ZSI, using higher active and lesser passive elements concerning its parent inverter. The inverter has an extra switch for the boosting network known as the shoot-through switch which is powered only during the shoot-through period.

To enhance its performance, the feature of EZSI is added to it by placing the source within the boosting network to provide continuous input current that is lacking in the latter, apart from employing lesser passive elements [10], presented in Fig.3. To further amplify the gain of the inverter, a switched-inductor (SL) replaces the inductor within the boosting network, while the shoot-through duty cycle (D_S) remains the central boost factor. The working is classified into 2 modes; one is the ST mode which is also the boost mode whereas the other is the standard inverter mode of operation as shown in Fig. 3.

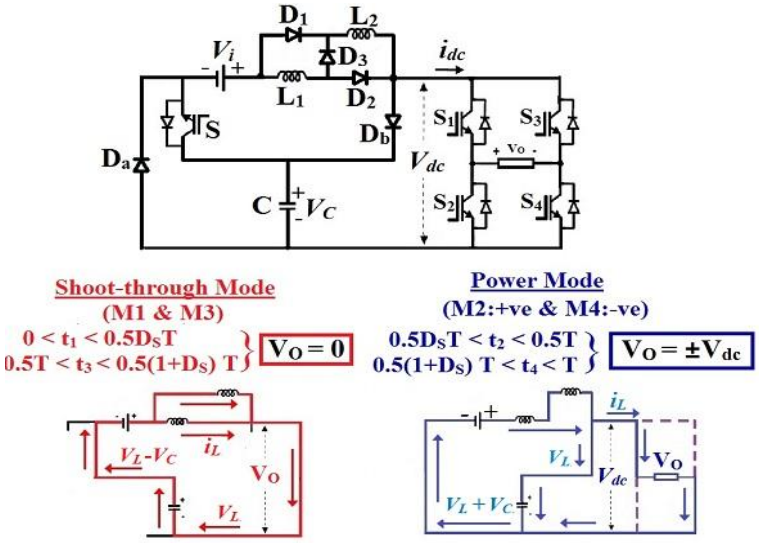
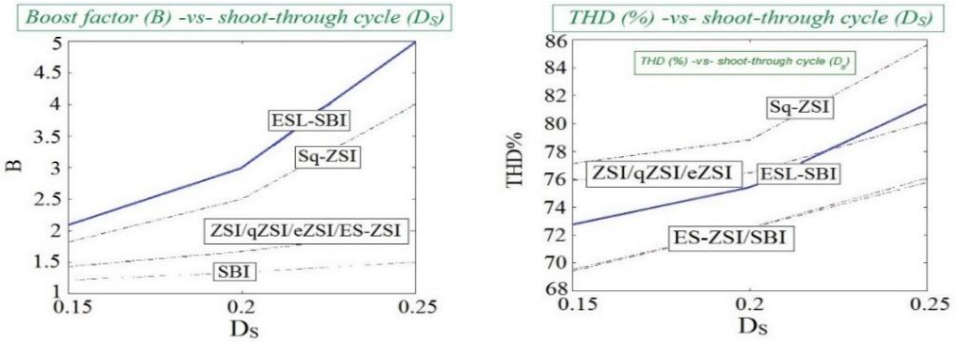


Fig.3 Embedded switched inductor switched boost inverter (ESL-SBI) with its modes



(a) (b)

Fig.4(a) Gain (B) –*vs*- D_S, and (b) THD –*vs*- D_S

As illustrated, during ST, the switch S is on, with $V_C > V_i$making D_a and D_b reversed, so the inductor (L) charges via the capacitor (C) through the closed ST switch with the inverter bridge being shorted. During the inverter's positive and negative cycle, the ST switch is in off condition and the inverter behaves like a current source charging the capacitor. The output equation is given as (1).

$$V_O = \frac{(1+D_S)}{(1-3D_S)} V_i \tag{1}$$

The inverter (ESL-SBI) is compared with the other basic type inverters to study and verify its performance based on parameters: gain and THD (total harmonic distortion) of the output without a filter circuit [11],[12]. The graphical depiction of the comparison of the boost factor and the resulting THD (in %) with $D_S$is given in Fig.4.

From the graph, it can be viewed that ESL-SBI has a good gain when compared with the other basic topologies and a better THD compared with most of the topologies. It can also be inferred that though the gain of the inverter increases with D_S, it also increases the harmonic content of the output. Hence to get an optimal working condition, a D_S value of 0.2 is chosen for the inverter in the following sections. Considering for a high gain application, the optimal number and the size of the components to achieve high gain and thereby minimize the overall loss from the system, the inverter ESL-SBI despite having the same THD margin, is considered to have better working in real-time applications with less effect on the overall system.

2.2 Embedded Switch Boost Multilevel Inverter (ESB-MLI)

For PV interface applications, a multilevel inverter is considered more compatible and promising for: *(i)* the generation of higher voltage using lower rated devices, *(ii)* increased stepped output improves the harmonic profile, *(iii)* its basic application suited to hybrid resource systems such as a PV array or fuel cell with DC-DC converter, wind turbine fed generators with suitable rectifiers, etc., [13],[14]. Amongst its types, the usage of low passive components for the same output levels and optimized circuit layout for compact packing makes cascaded h-bridge multilevel inverter (CHb-MLI) a positive option in such applications. In this work, two separate ESL-SBI are cascaded using a single h-bridge and

two auxiliary switches (S_5-S_6) [15], to obtain a five-level embedded switched boost multilevel inverter (ESB-MLI), as shown in Fig.5.

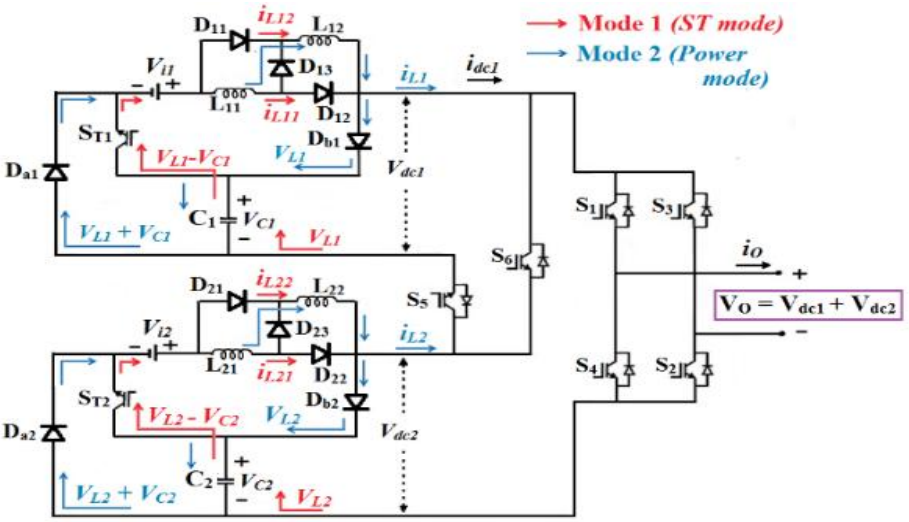


Fig. 5 Embedded switched boost multilevel inverter (ESB-MLI)

The MLI consists of two separate (symmetrical) sources;its topological operation is similar to a basic CHb-MLI to obtain the stepped output (illustrated in table I where S_{T1} and S_{T2} represent the shoot-through switches, S_1-S_4 are the inverter switches, and S_5-S_6 are auxiliary switches), where the boosting networks provide the power to the inverterconnected over a common load, for their operation.

Table 1: Switching Sequence for the developed MLI

(Vo)	**Auxiliary Switches (S_5-S_6)**	**Shoot-through Switches (S_{T1}- S_{T2})**	**Inverter (S_1-S_4)**
0	S_6	$S_{T1} + S_{T2}$	-
$+V_{dc}$	S_6	S_{T2}	$S_1 + S_2$
$+2V_{dc}$	S_5	-	$S_1 + S_2$
$+V_{dc}$	S_6	S_{T2}	$S_1 + S_2$
0	S_6	$S_{T1} + S_{T2}$	-
$-V_{dc}$	S_6	S_{T1}	$S_3 + S_4$
$-2V_{dc}$	S_5	-	$S_3 + S_4$
$-V_{dc}$	S_6	S_{T1}	$S_3 + S_4$

2.3 Modeling of Parameters

From the base inverter E-SBI, the performance equation of ESB-MLI can be derived. For any CHb-MLI, the output is the summation of the individual inverter peak output voltages, given in (2). The following equations are attained from the ST and inverter modes of the multilevel inverter of symmetrical structure where L_{11}=L_{12}= L_1, L_{22} = L_{21} = L_2. From

mode 1 (shoot-through), the inverter is shorted and hence can be considered two separated inverters (3) and (4).

$$V_O = \pm V_{dc} = V_{O1} + V_{O2}$$

(2)

$$V_{L_{11}} = V_{L_{12}} = V_{in_1} + V_{C_1} = V_{L_1} \quad (3)$$

$$V_{L_{21}} = V_{L_{22}} = V_{in_2} + V_{C_2} = V_{L_2} \quad (4)$$

We can also get $i_{in_1} = i_{C_1} = -2I_{L_1}$ and $i_{in_2} = i_{C_2} = -2I_{L_2}$ therefore the dc-link current and the output voltage are given as (5) and (6),

$$i_{dc_1} = 2I_{L_1}; i_{dc_2} = 2I_{L_2} \quad (5)$$

$$V_O = 0 \quad (6)$$

From mode 2 of the MLI, the voltage law yields the following equation $V_{L_{11}} + V_{L_{12}} = 2V_{L_1} = V_{in_1} - V_{C_1}$, from which we get the following equation,

$$V_{L_1} = \frac{V_{in_1} - V_{C_1}}{2}; V_{L_2} = \frac{V_{in_2} - V_{C_2}}{2} \quad (7)$$

From (7), we can get the peak voltage of the MLI as (8),

$$\pm V_{po} = V_{C_1} + V_{C_2} \quad (8)$$

With the inductor currents being the same as the input current (i_{in}), applying the current law will yield the following i_C (Capacitor current) in (9) where n=1, 2…,

$$i_{C_n} = i_{p_n} - i_{in_n} \quad (9)$$

2.3.1 Voltage Gain (B)

The inductor voltage balance law for a circuit state that the summation of the inductor voltage over a given timeperiod is zero,

$$\int_0^T V_L \, dt = 0 \quad (10)$$

Considering the inverter-1 of the MLI, we can derive the capacitor voltage of the inverter by substituting (3) and (7) in (10) whence the capacitor voltage for both inverters can be written as (11),

$$V_{C_n} = V_{in_n} \frac{\left(1 + D_S\right)}{\left(1 - 3D_S\right)} \quad (11)$$

From the above equation, by substituting the values in (8) the peak output voltage of the MLI is given as (12), where B is the gain/boost factor of the proposed MLI.

$$V_O = \pm V_{po} = \left(V_{in_1} + V_{in_2} \right) \frac{(1 - D_S)}{\left(1 - 3D_S\right)} = \left(V_{in_1} + V_{in_2} \right) B \tag{12}$$

2.3.2 Capacitor through Ripple Voltage $\left(\Delta v_{C_n} \right)$

The capacitor current equation and the capacitor current from the individual cascaded inverters are equated to derive the capacitor voltage ripple as given in (13) below.

$$i_{C_n} = -2I_{L_n} \tag{13}$$

Equating the capacitor currents, we get (14), which on integration yields the absolute capacitor voltage, as given in (15),

$$-2I_{L_n} = C_n \frac{dv_{c_n}}{dt} \tag{14}$$

$$\left| \Delta v_{c_n} \right| = \frac{I_{L_n}}{C_n} D_S T \tag{15}$$

Considering the capacitor current balance law, the inductor current of E-SBI is $i_{C_n} = \mathrm{I}_{\mathrm{L}_n} - i_{dc}$. The values of i_{dc_1} , andare computed from (11) and (13), i.e., Hence, on applying the law and simplifying, the inductor current can be obtained as,

$$I_{L_n} = \frac{(1 - D_S)(1 + D_S)}{R\left(1 - 3D_S\right)^2} V_{in_n} \tag{16}$$

Substituting (16) in (15),

$$\left| \Delta v_{c_n} \right| = \frac{D_S \left(1 - D_S\right)\left(1 + D_S\right)}{RC_n f \left(1 - 3D_S\right)^2} \tag{17}$$

Where *f* is the switching frequency of the proposed MLI. It can be observed that the ripple value of V_C is inversely proportional to *f* and C (capacitance value).Now to find the approximate capacitor value, xc% (allowable voltage ripple) is defined as (18),

$$x_c\% = \frac{\Delta v_{c_n}}{V_C} \times 100 \tag{18}$$

Applying (17) and (11) in the above equation, the capacitor value for the required ripple level is obtained as (19).

$$C_n = \frac{D_S \left(1 - D_S\right) \times 100}{Rf \left(1 - 3D_S\right) x_c\%} \tag{19}$$

2.3.3 Inductor through Ripple current (Δi_{L_n})

The inductor current ripple can be obtained from (3), (4), and the inductor voltage equation $v_{L_n} = L_n \frac{di_{L_n}}{dt}$. Taking n=1, 2…of the individual inverters, we get (20) on equating the inductor voltage equations,

$$L_n \frac{di_L}{dt} = V_{in_n} + V_{C_n} \tag{20}$$

The following set of equations is achieved by applying integration on (20); and by substituting it in (10), the absolute inductor current is given as in (22).

$$\int di_{L_n} = \frac{\left(V_{in_n} + V_{C_n}\right) D_S T}{2L_n} \tag{21}$$

$$\left|\Delta i_{L_n}\right| = \frac{D_S\left(1-D_S\right)V_{in_n}}{L_n f\left(1-3D_S\right)} \tag{22}$$

Similar to $|\Delta v_c|$, the ripple value of the inductor current is also inversely proportional to*f*and L (inductor value).

To find the approximate inductor value ofx_L% (allowable current ripple) given by the expression $\frac{\Delta i_{L_n}}{I_L} \times 100$. Substituting from (22) and (16), we can get the inductor value for defined/allowable ripple levels as given in (23) and (24).

$$x_L\,\% = \frac{RD_S\left(1-3D_S\right)}{L_n f\left(1+D_S\right)} \times 100 \tag{23}$$

$$L_n = \frac{RD_S\left(1-3D_S\right)\times 100}{f\left(1+D_S\right)x_L\,\%} \tag{24}$$

With the above-derived design equations, the proposed MLI can be designed for the standard level ripple and also according to our requirement and tested in MATLAB simulation software.

2.4 MC-PWM for Proposed MLI

For an MLI, multicarrier PWM is the most effective control method to generate switching pulses where a set of carriers based on the number of levels, interact with the modulating signal to obtain the respective pulses for the inverter switches. It is categorized as level-shifted and phase-shifted PWM, of which the former has easier control than the latter and hence generally preferred. In this work, inverted sine carrier PWM (ISC PWM) is utilized to generate the pulses. ISC PWM is proven to enhance the fundamental V_O even at

a low modulation index with reduced switching losses[16].

$$V_{st} = V_{car}\left(1 - D_S\right) \tag{25}$$

In this case, a unipolar inverter sine carrier is generated to get the controlled pulse, whereas the shoot-through signal is obtained by comparing a line indexwith two carrierswhose values are chosen based on the D_S requirement given in (25).

2.5 Performance Comparison with Other Multilevel Topologies

The basic idea for preferring an MLI is to feed equipment or machinery of a high-powerrating from a medium or low power voltage source. In this section, a basic comparative analysis of the multilevel inverters with the proposed MLI for the same input is carried out as shown in table II below (where L-inductors, C- capacitors, D-diodes, and S-switches). Since the proposed MLI is obtained from cascading a three-level inverter, it is compared with the other z-source type cascaded MLI for a common input $V_{in} = 50V$ [17]-[19].

Table 2:Multilevel Topological Comparison

MLIs	V_O (M=1)	Passive components (L+C)	Active components (S+D)
CHb-MLI	100	-	8+8
ZSI-MLI	150	4+4	6+8
qZSI-MLI	160	4+4	8+10
Conventional ESB-MLI	300	4+2	10+18
Modular ESB-MLI	300	4+2	8 +16

From the table, it can be inferred that ESB-MLI is the most suited multilevel inverter for connecting low/medium powered sources with a grid (1-phase/3-phase). ESB-MLI uses lesser passive and more active elements to achieve the high gain output, for the same number of the source but lower values of the components.

3. Closed-Loop for GridSynchronization

To reduce the current harmonics injected into the grid within the standardized limit, a high value of filter inductance shall be needed. Yet for the application involving residential power generation of some kW/MW, where price, size, and system dynamics are considered key factors, such filters are drawbacks. The most common solution to this is to use T (LCL) filter for grid-tie inverter systems [20].

While implementing a grid-connected system, synchronization of the grid and the inverter outputs is considered a prime stage to overcome the power quality-related problems that shall be caused by some unpredicted disturbances. One of the most commonly used methods is the current controller method involvinga d-q rotating frame where the direct-axis (d-axis) is brought in alignment with the grid voltage. Where a DC-link controller is used to generate the reference value for the active current (I_{d_ref}) to control the active power.

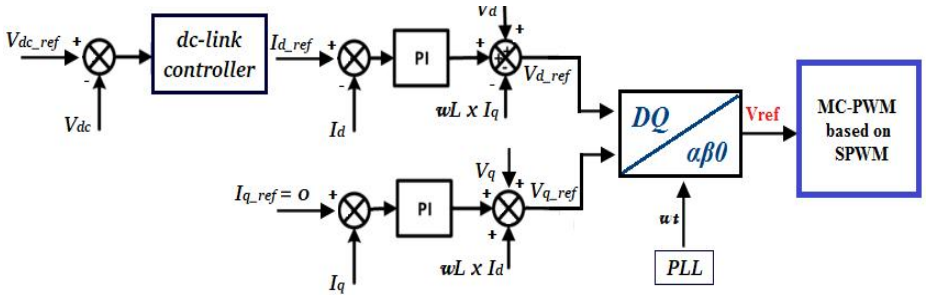


Fig. 6 DQ current controller loop with dc-link control

Also known as the Voltage Oriented Control, where the current reference for the direct-axis (I_{d_ref}) controls the active power while for the quadrature-axis (I_{q_ref}), the current reference is set to zero to reduce the overall reactive power [21]. Fig.6 shows the d-q control system used in this work. Since both the grid-side and inverter-side parameters are transformed in d-q components resulting in dc values, PI controllers are used forreducing the steady-state error to zero between the references and the actual current of I_d and I_q.

4. Simulation of the work

With the information presented above the proposed topology is simulated in MATLAB in this section. The inverter is connected with the grid through a filter network, to trim down the unwanted frequency harmonics present in the output.

A T-type filteris used as explicated in the literature to keep the THD within a low range, thereby providing a better output to the grid. The simulation is conducted for 2 kW grid power with $V_{in.} = V_{in.}$ (input voltage) of 50-60V, f_S = 25kHz (switching frequency) for component values L_1 = L_2 = 1.5 mH (inductors), C = 47 µF (capacitor) with filter components (C_f = 10 µF, $L_{f_{1,2}}$ = 5mH).

A D_S of 0.2 is considered to run the simulation, to get a common ground between low THD and a better boost factor for the PD multicarrier modulation. The overall synchronization control method for the proposed MLI in a single-phase grid-connected PV system is shown in Fig. 7 with a closed-loop circuit consisting of a PLL block and the d-q current controller. The outputs of the proposed MLI are given in Fig. 8.

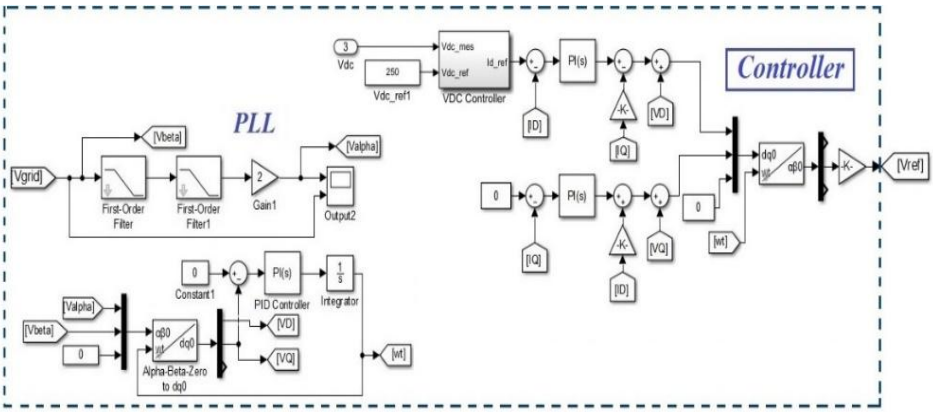


Fig. 7 Synchronization control for grid connected ESL-SB MLI

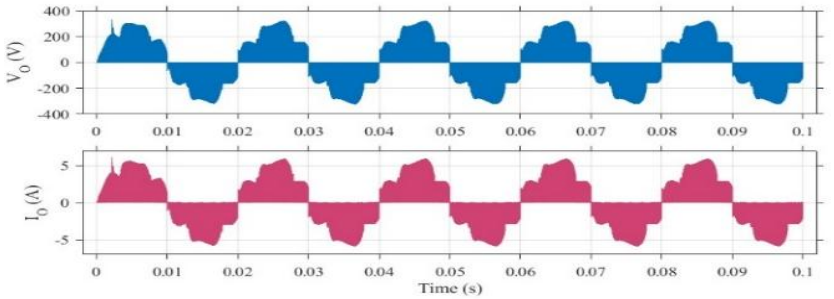


Fig. 8 Output from the inverter

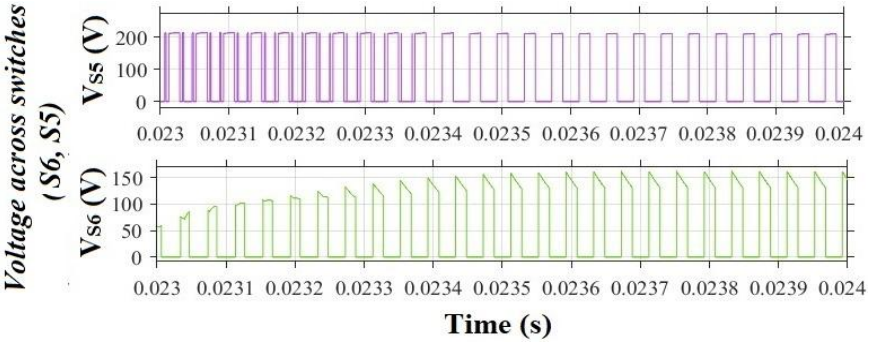


Fig.9Voltage across auxiliary switches

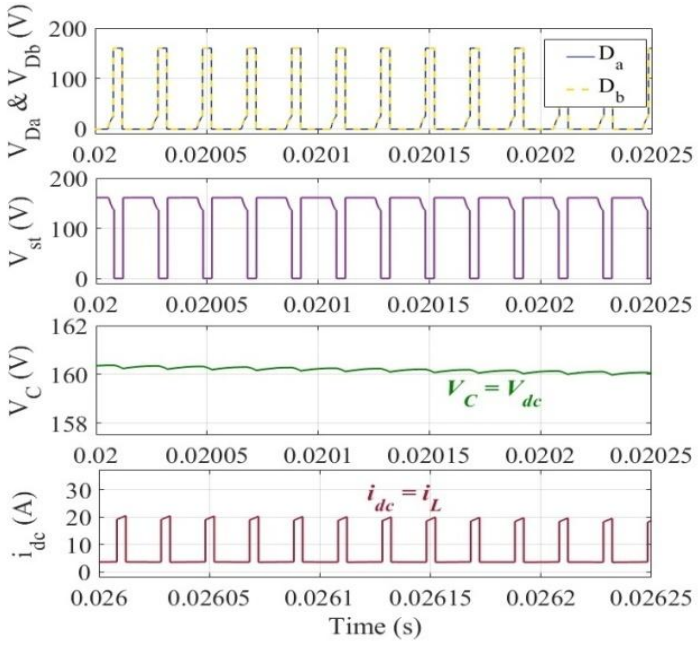
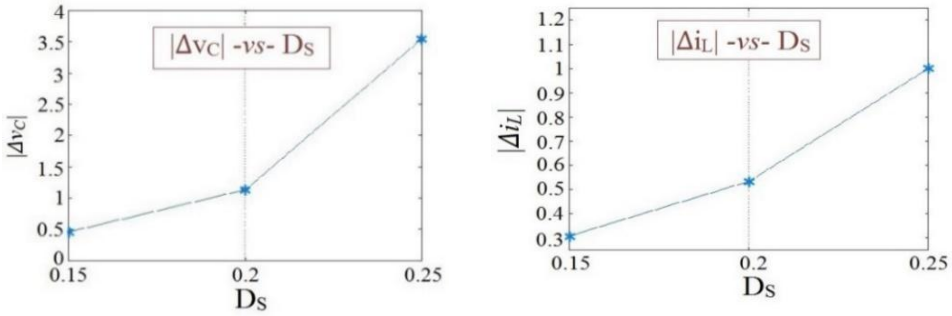


Fig.10 Voltage and current through the components

The voltage across the auxiliary switches connecting the h-bridge, the inverter components (diodes ‘a’ and ‘b’, ST switch, capacitor), the current across the inductor are shown in Fig. 9 and Fig. 10, and the variations of $|\Delta v_C|$ andto D_S are shown in Fig. 11(a)

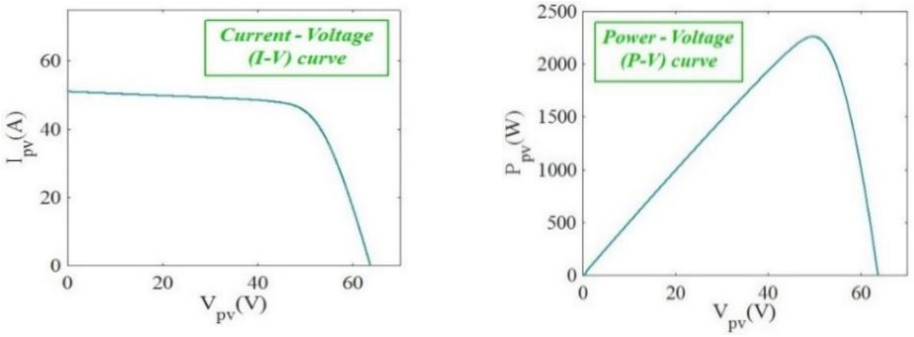
&Fig.11(b) below.



(a) (b)

Fig. 11 (a) $|\Delta v_C|$ -*vs*- D_S, and (b) $\Delta i_L|$ -*vs*- D_S

A one-diode-based PV array is designed and connected to the proposed MLI, with each module being rated 37W [22]. To feed a single-phase grid, 4 series modules, and 15 parallel modules are connected to achieve the required rating; Fig. 12(a) & Fig. 12(b) show the PV and IV characteristics of the PV Array.



(a) (b)

Fig. 12 (a) I_{PV}-*vs*- V_{PV} and (b) P_{PV}-*vs*- V_{PV}

The multilevel output voltage from the proposed MLI and the synchronized grid outputs with the inverter current under different voltage conditions are shown in Fig. 13.

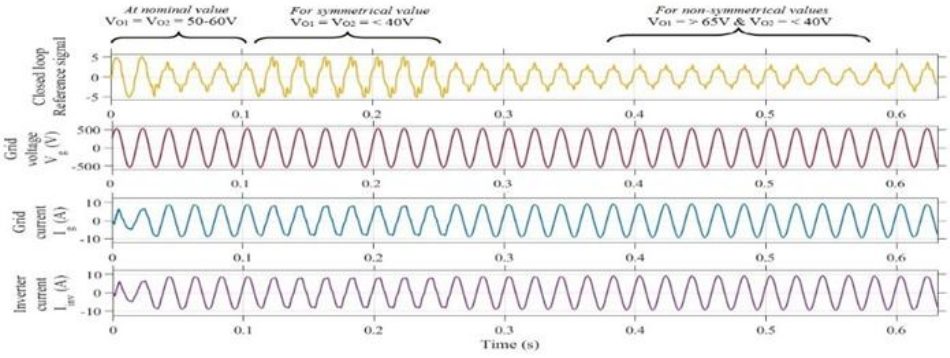


Fig. 13 Output values of grid synchronized with inverter values

From the above figure, it can be viewed that even at different input voltages (resulting due to partial shading), the reference from the d-q method alters accordingly to sustain their synchronization between the grid and the inverter currents. The grid values are also in phase with each other.

5. Hardware

To further study the reliability of the proposed MLI, an experimental setup has been developed based on the simulation parameters, as shown in Fig. 14. The MLI prototype has been designed using power MOSFETs (IRF740) and diodes (MUR1570G) and power from a DC source with V_{in} ≈50V to feed a single-phase load.With the help of Xilinx, the FPGA processor provides controlled signals to the respective switches via a driver circuit. The resultant output voltage and current waveforms from the inverter are shown in Fig. 15(a) and the input and dc-link voltage are shown in Fig. 15(b).

The current through the switched-inductor cell (I_L) of the MLI, ispresented in Fig. 16. Fig. 17 (a) and Fig. 17 (b)gives the voltage across the ST switch and auxiliary diodes (Da and Db) while Fig. 18 is the harmonic values of the output.

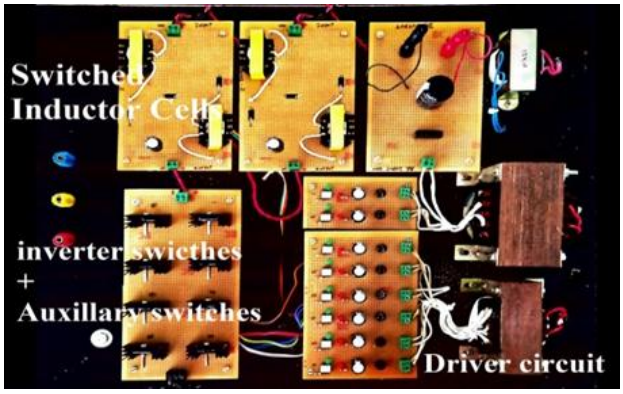
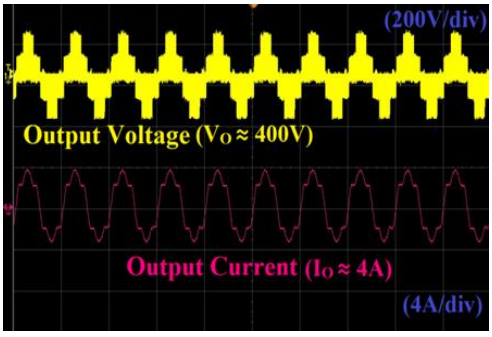


Fig. 14 Hardware set-up of proposed MLI



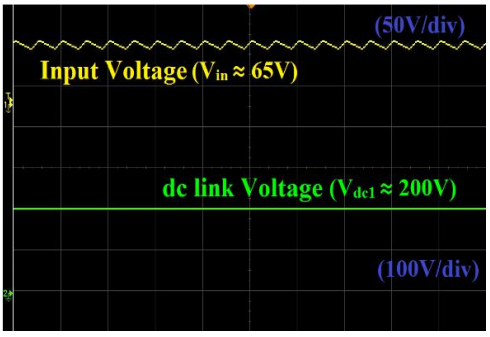


Fig. 15 (a)The output waveforms of the proposed MLI, and (b) V_{in} and V_{dc}

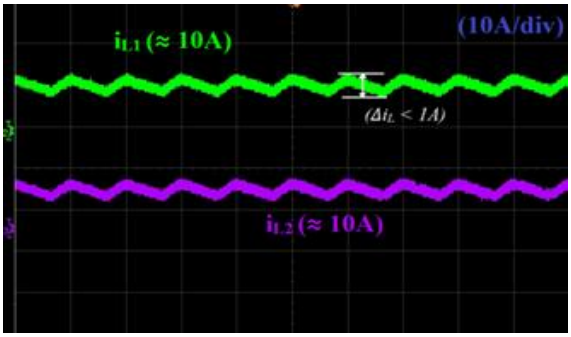


Fig. 16 I_L (I_{L1}= I_{L2}) from the SL cell

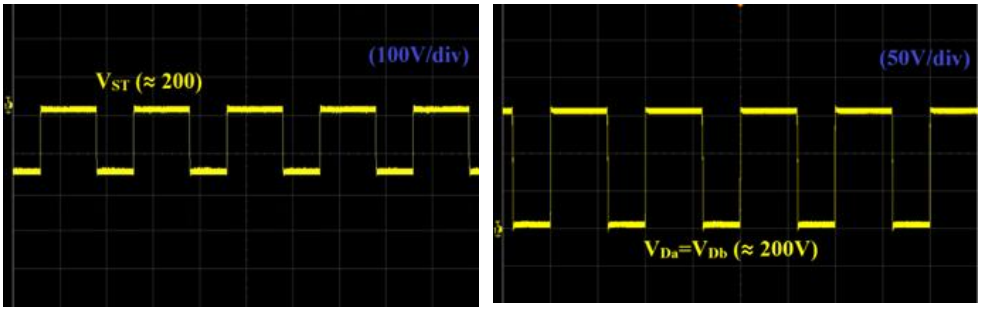


Fig. 17 (a) V_{ST}, and (b) V_{Da} and V_{Db}

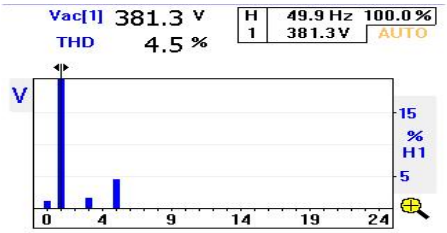


Fig. 18 Harmonics of V_O

It can be observed that the output voltage is around 3 times the input for a given D_S (ST duty cycle), which is concurring with the results from the simulation. It can be viewed that the real time values are slightly lower than the simulated values, attributing it to the component losses. Still the measured output voltage harmonic is found to be inside the acceptable limit.

6. Conclusion

In this paper, the suitability of using a multilevel inverter for interfacing a PV module to a single-phase grid has been discussed. Having an inherent structure that is suitable for use in distributed power systems; cascaded MLI (CMLI) has gained more recognition for producing an output of lower harmonic content and EMI thereby reducing the filter requirements. Relating to that, this work has proposed a new cascaded type MLI (CMLI) for a single-phase grid powered from a PV module.

The inverter equations of the proposed MLI have been derived with the help of the equation of the base topology.The proposed PV fed MLI controlled by phase-disposed

multicarrier PWM has been simulated and the results have been displayed. From the results, it could be inferred that the proposed inverter even with a basic modulation method is capable of producing high output voltage with better output waveform thereby reducing THD. Hence it can be used for an application that requires high-powered output from low-powered sources. Further, simulations have been carried out with suitable topological changes to connect the MLI to a 2 kW grid while the entire set-up has been synchronized using a d-q current control loop and the outputs are presented. Based on the results, a prototype of the proposed MLI was developed and tested under open-loop conditions. The results have showcased the reliability and suitability of the proposed MLI in a single-phase grid-connected PV system.

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References

[1] M. S. Nazir, A. N. Abdalla, H. M. Sohail, Y. F. Tang, G. I. Rashed, and W. Chen, "Optimal planning and investment of Multi-renewable power generation and energy storage system capacity", *Journal of Electrical Systems*, 17(2), pp. 171-181, 2021.

[2] A. Nouaiti, A. Mesbahi, A. Saad, M. Khafallah, and M. Reddak, "Realization of a Single-Phase Multilevel Inverter for Grid-Connected Photovoltaic System", *Engineering, Technology & Applied Science Research,* 8(5), pp.3344–3349, 2018.

[3] S. Mehta, and V. Puri, "A review of different multi-level inverter topologies for grid integration of solar photovoltaic system", *Renewable Energy Focus*, vol. 43, pp.263-276, 2022.

[4] Okan Bingöl, and Burçin Özkaya, "Analysis and comparison of different PV array configurations under partial shading conditions," Solar Energy, vol. 160, pp. 336-343, 2018.

[5] A. Thummalagunta, N. R. Patne, and N. Kodandaram, "Analysis and Control of Switched Quasi-Impedance-Source-Inverter With Superior Boosting Ability for Renewable Energy Applications*", IEEE Transactions on Industry Applications*, 58 (3), pp.3783-3793, 2022.

[6] T. Li, and Q. Cheng, "A comparative study of Z-source inverter and enhanced topologies", *CES Transactions on Electrical Machines and Systems*, 2(3), pp.284-288, 2018.

[7] S. Ahmad, S. H. Johari, A. Ahmad, and M. F. M. A. Halim, "Grid-connected multilevel inverters for PV application", *2015 IEEE Conference on Energy Conversion (CANCON)*, pp.181-186, 2015.

[8] A. Sinha, M. Das, and K. Jana, "Control of asymmetrical cascaded multilevel inverter for a grid-connected photovoltaic system", *IET Renewable Power Generation*, 13(9), pp.1456-1465, 2019.

[9] A. Ravindranath, S. K. Mishra, and A. Joshi, "Analysis and PWM control of Switched Boost Inverter", IEEE Trans. Industrial Electronics, 60(12), pp. 5593–5602, Dec. 2013.

[10] E. Babaei, E.ShokatiAsl, M. H.Babayi, and Sara Laali, "Developed Embedded Switched-Z-Source Inverter", *IET Power Electronics*, 9(9), pp. 1828 1841, 2016.

[11] T. Divya, and, R. Ramaprabha, "Comparative Topological Study of Embedded Based Switched Boost Inverter", *Advances in Parallel Computing*(IOS press E-books), 37, pp.37 – 44, 2020.

[12] J. Yuan, Y. Yang, and F. Blaabjerg, "A Switched Quasi-Z-Source Inverter with Continuous Input Currents", *Energies*, 13(6), pp.1-6, 2019.

[13] B. Ahmed, K. A. Aganah, M. Ndoye, M. A. Arif, C. Luciano and G. V. Murphy, "Single-phase cascaded multilevel inverter topology for distributed DC sources", *IEEE 8th Annual Ubiquitous Computing, Electronics and Mobile Communication Conference (UEMCON)*, *October*, pp.514-519, 2017.

[14] A. R. Adly, H. Y. Abdul-Hamid, A. Elhussiny, M. S. Zaky, E.E. El-Kholy, "A Brief Review of the Conventional and Multilevel Inverters Topologies", *2023 IEEE Conference on Power Electronics and Renewable Energy (CPERE)*, *February,* pp.1-8, 2023.

[15] S. Kota, V. P. Muddineni, A. K. Dadiboina, and G. Venna, "Simulation and analysis of novel cascaded z source inverter," International Journal of Advances in Engineering & Technology, 5(2), pp. 207-215, 2013.

[16] R. Seyezhai, and B. L. Mathur, "Performance evaluation of inverted sine PWM technique for an asymmetric cascaded multilevel inverter",*Journal of Theoretical and Applied Information Technology,* 9(2), pp. 91-98, 2009.

[17] N. Pragallapati, and S.K.J. Ranade, "Cascaded H-Bridge MLI based Grid Connected Cell Level Battery Energy Storage System", *International Conference on Power, Control and Computing Technologies (ICPC2T), January*, pp.359-362, 2020.

[18] K. Vijayalakshmi, and C. Balamurugan, "Z–Source Multilevel Inverter Based On Embedded Controller", *Proc. Indonesian Journal of Electrical Engineering and Computer Science,* 6(1), pp.1-8, 2017.

[19] D. Umarani, and R. Seyezhai, "Modeling and Control of Quasi Z-source Cascaded H-bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems", *Energy Procedia*, 90, pp.250-259, 2016.

[20] M. Pastor, and J. Dudrik, "Design and control of LCL filter with active damping for grid-connected inverter", International Conference on Electrical Drives and Power Electronics (EDPE), September, pp.465-469, 2015.

[21] B. Li, S. Huang, X. Chen and Y. Xiang, "A simplified DQ-frame current controller for single-phase grid-connected inverters with LCL filters", *20th International Conference on Electrical Machines and Systems (ICEMS)*, *August,* pp.1-5, 2017.

[22] N. Pandiarajan, and, R. Muthu, "Mathematical modeling of a photovoltaic module with Simulink", *1st International Conference on Electrical Energy Systems, January,* pp.258-263, IEEE, 2011.