

Embedded Switched Z-Source Multilevel Inverter for Grid Interfaced Photovoltaic Systems

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Abstract—The modeling and the implementation of the embedded switched z-source type cascaded multilevel inverter for photovoltaic (PV) interfaced applications have been presented. With the ability to draw continuous current with an inherent filtering capability, the embedded switched z-source type inverter provides a single-stage conversion with a high output gain which makes it suitable for PV arrays with a low voltage rating. By applying a modular cascading method with a reduced number of H-bridge the multilevel inverter (MLI) is designed for a series-parallel connected PV array. It is controlled using the basic multicarrier PWM technique and synchronized with the grid. With the derived design equations for each mode, its stability has been analyzed and compared for different duty cycles. The developed MLI connected with a PV array has been simulated with the idea of reducing the impact of partial shading by using shorter series of strings, providing a high gain conversion with lower stress across the components. A prototype of the MLI has been tested to give a power rating of 2 kW and the results from both the simulation and the hardware have been discussed.

Index Terms—bridge circuits, DC-AC power converters, power grid, pulse width modulation, solar energy.

I. INTRODUCTION

With the escalating power demands thanks to the technological advancements in recent years, the significance of photovoltaic (PV) systems has grown in all streams of engineering. One such application is the grid-connected PV system that is gaining popularity in tropical countries [1]. Yet domestically utilized grid-connected (Gc-PV) or building-integrated PV arrays (Bi-PV) are sensitive to partial shading, resulting in reduced energy yield from the PV. It has been observed from many works cited in the literature that series-connected PV panels are more sensitive to partial shading than parallel connections [2]. To simply mitigate this problem, shorter series-connected and more parallel-connected arrays are used. In such cases, the PV array supplies lower voltage (V_{pv}) and higher current (I_{pv}) to meet the required power rating (P_{pv}).

MLIs, especially the Cascaded type multilevel inverters (C-MLI) have started gaining attention to improve the quality of the output from the array [3-4]. The main reason for this growth is its ability to produce a stepped output with reducing harmonics, and to best handle during conduction of the same leg without affecting the inverter performance. And with the provision of using separate sources for the inverter, it is also more suitable for renewable sources. However, in MLI a DC-DC converter is required to boost

the input fed to the inverter that increases the cost and complexity of the circuit. From the discussed points, it can be understood that an inverter with high gain that provides a boosted output voltage with better power quality, is required [5].

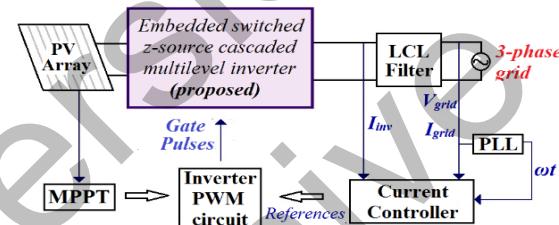


Figure 1. Overall block diagram

In regard to this, a five-level z-source type multilevel inverter for PV interfaced applications has been studied. Considering the features of different z-source inverters [6] and multilevel inverters, this work focuses on obtaining a high gain multilevel inverter using an embedded type z-source inverter. The parent inverter is a switched boost inverter [7] that combines the properties of a boost converter with an impedance network while using higher active elements than the latter. The impedance network is connected to a modular cascaded H-bridge inverter with the idea of reducing the switching components and thereby its switching loss when compared with the conventional C-MLI. The work discussed in this paper is represented in Fig. 1. By incorporating the advantages of cascaded H-bridge MLI to the embedded type switched ZSI; the proposed MLI can be a promising topology for all PV-related applications in near future.

II. DESCRIPTION OF THE WORK

When a PV panel is shaded, the panel's photocurrent reduces causing mismatches in the electrical characteristics of the panels [8]. This reduction depends on many factors such as array configuration, shade intensity, and so on; yet when series connected panels are shaded, it limits the panel string current which will lead to hotspots due to uneven distribution of the current. A substantial impact of partial shading on the array is based on the array interconnection (series-parallel connections) $m \times n$ panels, where series connected (m) panels are more susceptible to shading than the parallel connected (n) ones. Also, it has been presented in the literature that under partially shaded or any fault conditions, series-connected arrays are less robust when compared with the other connections such as series-parallel

(SP) or TCT connections [9-10].

While in a TCT (Total Cross Tied) configuration, the ties disconnect the shaded modules to avoid their effect on the unshaded modules, the complexity of examining and controlling the TCT connected PV arrays to obtain the best output is a major concern. Besides, there is difficulty during the expansion of the size of the array, and so SP connected PV arrays are preferred as both the control and the addition of the array is less complicated in comparison. Hence, when considering series-connected and SP-connected arrays, the latter is more robust during partial shading. For example, a 2

kW rated power can be considered which could be obtained from both Figs. 2(a) and 2(b) connections with 37W rated panel. The former has a long series of strings that provides higher output voltage (V_{pv}) and lower current (I_{pv}), while the latter has shorter series of connections and increased parallel strings providing a low V_{pv} and higher I_{pv} . Yet, since the effect of shading mainly affects the panel current, a PV array with high output current is expected to cause considerably less damage to devices. Hence, a shorter series-long parallel-connected array is considerable.

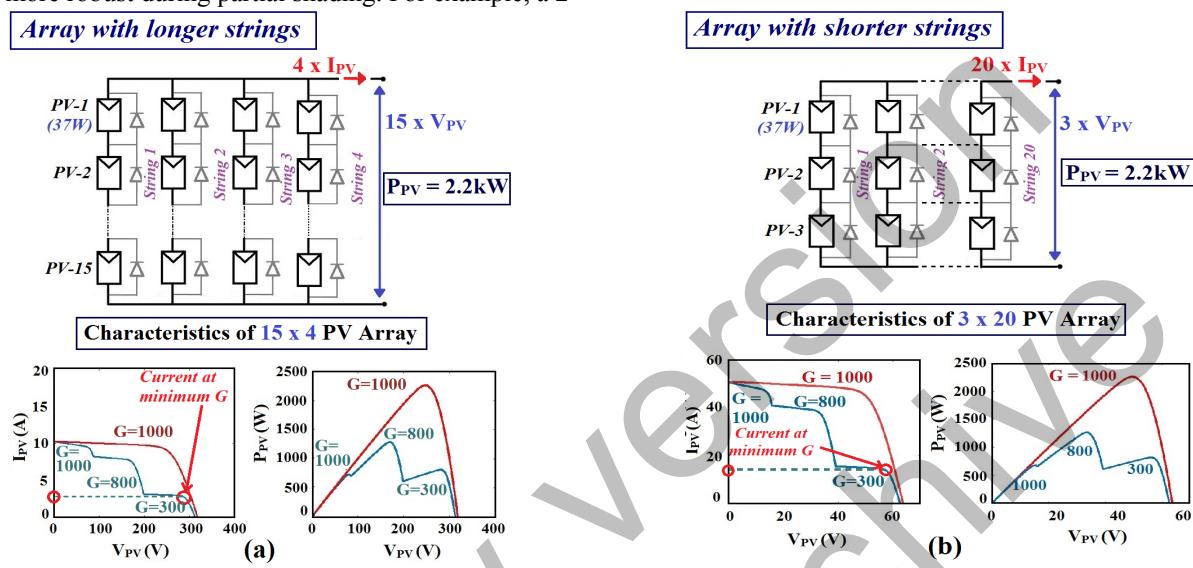


Figure 2. PV array of 2 kW with (a) longer series string and (b) longer parallel string

Hence, in view of the advantage of a short series string, this work proposes a high gain MLI to boost the varying output voltage of the PV array to meet the required voltage rating as in the case of Gc-PV or Bi-PV. This inverter replaces the two-stage inverter unit (Fig. 3(a)) that requires around 15 series panels per string with a single-stage multilevel inverter that requires only 3-4 series of panels per string (Fig. 3(b)) as shown below.

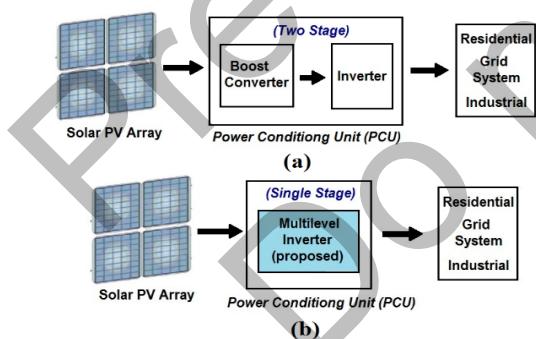


Figure 3. PV array connected with (a) double stage PCU and (b) single-stage PCU

Since the inverter to be developed is a cascaded type MLI, both the sources of the MLI are fed from a different array of different renewable sources, so that the effect of partial shading on the overall inverter can be further reduced; the size of the PV array can be further reduced based on the requirement.

III. MULTILEVEL INVERTER

The operation and the design of the proposed multilevel inverter (multilevel embedded switched-inductor z-source

inverter (mESL-ZSI)) have been discussed in the following sections.

To have a general understanding, a brief comparison of z-source type topologies has been discussed in section A, from which the stability analysis of the ESL-ZSI has been carried out in section B. The derivation of design equations of the MLI has been done in section C. To generate switching pulses for the MLI, two types of multicarrier PWM methods have been compared and their effect has been discussed in section D. The efficiency of the proposed MLI has been calculated for different duty-cycle by calculating the losses in section E.

A. Embedded switched-inductor z-source inverter (ESL-ZSI)

Through the years, the conventional z-source inverter (ZSI) has undergone varied topological changes due to the efforts made to reduce or eliminate its drawbacks while retaining its main advantage like buck-boost operation. Many new switched-capacitor/switched-inductor-based topologies have also been implemented to improve the conversion ratio.

This section focuses on comparing some existing z-source topologies to gain a better understanding of the ESL-ZSI. To reduce the overall size and the efficiency of the system and to avoid the effect of di/dt on the capacitor charging path, this work focuses on using a switched-inductor cell. Inverters with topological improvements in the existing ZSIs are selected and compared in terms of gain, voltage stress across the capacitors, and the number of passive elements which contribute to the overall loss of the system [11-15]

tabulated in Table I.

TABLE I. SWITCHING PATTERN

Name	Gain (M=1)	Capacitor voltage (V_c)	Passive component
Z-source inverter (ZSI) [6]	$\frac{1}{(1-2D_S)}$	$\frac{(1-D_S)V_i}{(1-2D_S)}$	$2L + 2C$
Quasi-ZSI (qZSI) [6]	$\frac{1}{(1-2D_S)}$	$V_{C1} = \frac{(1-D_S)}{(1-2D_S)} V_i$	$2L + 2C$
		$V_{C2} = \frac{D_S}{(1-2D_S)} V_i$	
Switched Boost inverter (SBI) [7]	$\frac{(1-D_S)}{(1-2D_S)}$	$\frac{(1-D_S)V_i}{(1-2D_S)}$	$1L + 1C$
Series ZSI (s-ZSI) [12]	$\frac{1}{(1-2D_S)}$	$\frac{D_S}{(1-2D_S)} V_i$	$2L + 3C$
Embedded ZSI (E-ZSI) [14]	$\frac{1}{(1-2D_S)}$	$\frac{2V_i}{(1-2D_S)}$	$2L + 2C$
Switched quasi ZSI with continuous input current (s-qZSI) [16]	$\frac{1}{(1-3D_S)}$	$V_{C1} = \frac{V_i}{(1-3D_S)}$	$2L+3C$
		$V_{C2} = V_{C3} = \frac{D_S V_i}{(1-3D_S)}$	
Embedded switched ZSI (ES-ZSI) [17]	$\frac{1}{(1-2D_S)}$	$\frac{V_i}{(1-2D_S)}$	$1L + 1C$
Embedded switched-inductor ZSI (ESL-ZSI) [17]	$\frac{(1+D_S)}{(1-3D_S)}$	$\frac{(1+D_S)V_i}{(1-3D_S)}$	$2L+1C$

Apart from the topological comparison, the following graph (Fig. 4) has been constructed by conducting a

simulation study on each topology (the common simulation concerning the shoot-through duty cycle (D_S)).

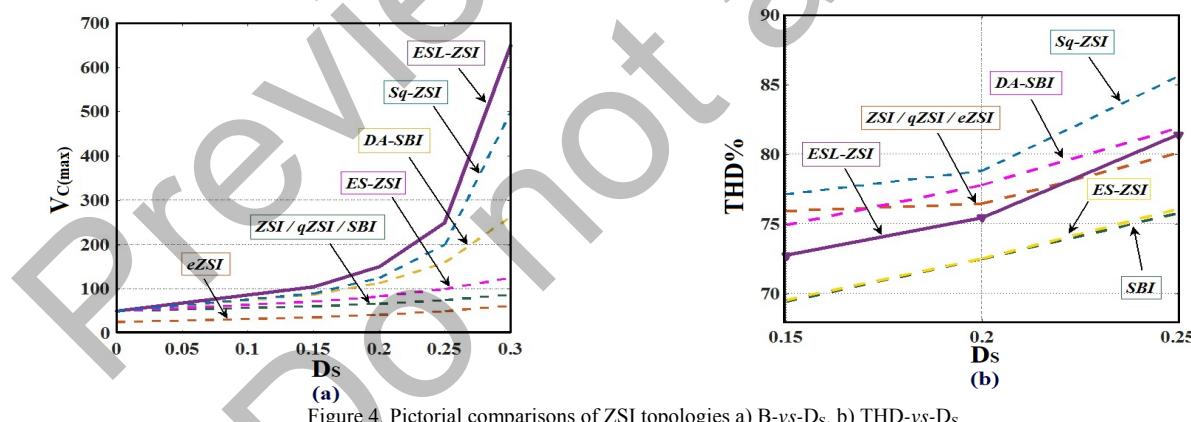
TABLE II. SWITCHING PATTERN

Component	Value
Input Voltage (V_{in1})	50 V
Switching frequency (f_s)	25 kHz
Modulation index (M)	0.8
Shoot-through duty cycle (D_S)	0.2
Inductors ($L_1=L_2=L$)	2.5 mH
Capacitor ($C_1=C_2=C_3=C$)	50 μ F

The comparison shows that by varying and restructuring existing topologies, the disadvantages of ZSI such as inrush current, voltage stress, etc. can be reduced. In this regard, it can be viewed that both S-qZSI [16] and ESL-ZSI [17] draw continuous input current and convert the input with higher gain, but since the number of passive components is higher in S-qZSI, ESL-ZSI is preferred for the PV applications that require high gain inversions.

B. Analysis of ESL-ZSI

The steady-state response of the inverter has been calculated with the help of the state-space averaging (SSA) technique, where the following assumptions have been considered: *a*) all the switches and the diodes are considered ideal, *b*) the series resistance for the components are considered to be negligible, *c*) the values of inductors are symmetrical ($L_1 = L_2 = L$) and *d*) capacitor voltage over the time period is considered a constant [18].

Figure 4. Pictorial comparisons of ZSI topologies a) B-vs-D_s, b) THD-vs-D_s

As mentioned earlier, [17] the two operating modes of ESL-ZSI follow the other conventional ZSI consisting of the shoot-through mode and power mode (negative and positive). Fig. 5 illustrates the equivalent circuits of the inverter during both modes. The inductor current (I_L) and the capacitor voltage (V_C) are the two-state variables considered in this modeling. The first mode is the shoot-through mode where the inductors are charged in parallel. (1) to (5) have been obtained by using Kirchhoff's voltage law (KVL) and current law (KCL) shown in Fig. 5 (a) – *Mode 1 (ST mode)*, parameters are given in Table II for reference, based on the effect of capacitor voltage and THD

(a) Mode 1 (Shoot-through mode) (b) Mode 2 (Power mode)

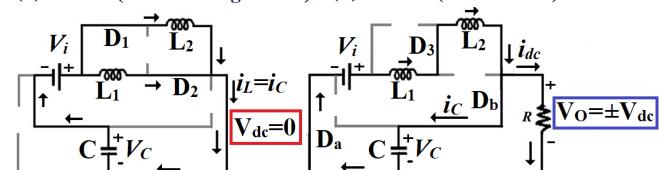


Figure 5. Operating modes of ESL-ZSI (a) ST (boost) mode and (b) power mode

$$V_i = V_L - V_C = 2L \frac{di_L}{dt} - V_C \quad (1)$$

$$\frac{di_L}{dt} = \frac{V_i}{2L} + \frac{V_C}{2L} \quad (2)$$

$$i_L = -\left(C \frac{dV_C}{dt}\right) \quad (3)$$

$$\frac{dV_C}{dt} = -\left(\frac{2i_L}{C}\right) \quad (4)$$

$$V_o = 0 \quad (5)$$

where, $di_L / dt = \dot{i}_L$ ($= \dot{i}_1$) and $dV_C / dt = \dot{V}_C$ ($= \dot{V}_2$).

The state-space (ss) equations for each mode can be written in the following matrix form as shown in (6) and (7) where X is one of the state variables, A is the average state matrix, B is the average input matrix, and U is the input variables forming the steady-state matrices. The ss equation for the mode 1 is written as (8).

$$\dot{X} = A_n X + B_n U \quad (6)$$

$$\dot{Y} = CX + DU \quad (7)$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2L} \\ -\frac{2}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} \quad (8)$$

Similarly, the ss equations and matrix for mode 2 (power mode) as shown in Fig. 5 (b), are given from (9) to (13).

$$V_i = V_L + V_C = 2L \frac{di_L}{dt} + V_C \quad (9)$$

$$\frac{di_L}{dt} = \frac{V_i}{2L} - \frac{V_C}{2L} \quad (10)$$

$$\frac{dV_C}{dt} = \frac{i_L}{C} - \frac{V_C}{RC} \quad (11)$$

$$V_o = \pm V_C \quad (12)$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L} \\ 1 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} [V_i] \quad (13)$$

Now by performing state-space averaging on (6), the following (14) has been arrived at; where d represents the duty cycle during the shoot-through mode ($= D_S$). Rewriting the equations in the matrices forms, we get averaged matrices A and B, given in (15). For many systems, the D is usually a null matrix, whereas output matrix C is given by (16).

$$\dot{\bar{X}} = A \bar{x} + B \bar{u} = [\bar{A}_1 d + \bar{A}_2 (1-d)] \bar{x} + [\bar{B}_1 d + \bar{B}_2 (1-d)] \bar{u} \quad (4)$$

$$A = \begin{bmatrix} 0 & \frac{d}{2L} \\ -\frac{2d}{C} & 0 \end{bmatrix} + \begin{bmatrix} 0 & -\frac{(1-d)}{2L} \\ \frac{1-d}{C} & -\frac{(1-d)}{RC} \end{bmatrix} = \begin{bmatrix} 0 & \frac{(2d-1)}{2L} \\ \frac{(1-3d)}{C} & -\frac{(1-d)}{RC} \end{bmatrix} \quad (15)$$

$$B = \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}; D = 0 \quad (16)$$

The derived matrices are used in (17) to get the transfer function for the steady-state model; the final simplified G(s) equation is represented in (19) below, for the values of L = 2.5 mH, C = 50 μF, R = 45 Ω the transfer function of ESL-ZSI in terms of d is given by (20).

$$G(S) = C(sI - A)^{-1} B + D \quad (17)$$

$$G(S) = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \left\{ s \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - \begin{bmatrix} 0 & \frac{(2d-1)}{2L} \\ \frac{(1-3d)}{C} & -\frac{(1-d)}{RC} \end{bmatrix} \right\}^{-1} \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} + 0 \quad (18)$$

$$G(S) = \frac{\left[\frac{(1-3d)}{2LC}\right]}{S^2 + \frac{S(1-d)}{RC} - \frac{(2d-1)(1-3d)}{2LC}} \quad (19)$$

$$G(S) = \frac{4000000 - 1200000d}{S^2 + 400S(1-d) + 4000000(2d-1)(1-3d)} \quad (20)$$

Now to perform the dynamic analysis of the model, *small-signal analysis* is carried out where small ac signals are added to the averaged values i.e., a corresponding ac signal is added with the state variables and input variables represented in (21).

$$\begin{bmatrix} \frac{d(i_L + \hat{i}_L)}{dt} \\ \frac{d(V_C + \hat{V}_C)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} [V_i] \quad (21)$$

The dc terms representing the steady-state model and also the product of ac terms are neglected for simplification and for focusing the analysis on their ac behavior only. The small-signal model for ESL-ZSI is given by (22) and (23),

$$\frac{d\hat{i}_L}{dt} = \frac{(2d-1)}{2L} \hat{V}_C + \frac{\hat{V}_i}{2L} + \frac{2\hat{V}_C}{2L} \hat{d} \quad (22)$$

$$\frac{d\hat{V}_C}{dt} = \frac{(1-3d)}{C} \hat{i}_L - \frac{(1-d)}{RC} \hat{V}_C - \frac{3\hat{i}_L}{C} \hat{d} + \frac{2\hat{V}_C}{RC} \hat{d} \quad (23)$$

The zero-pole plot for the steady-state analysis is given for different d values in Fig. 6; we can see that the system is stable since all the poles are on the left plane.

Pole - Zero Map

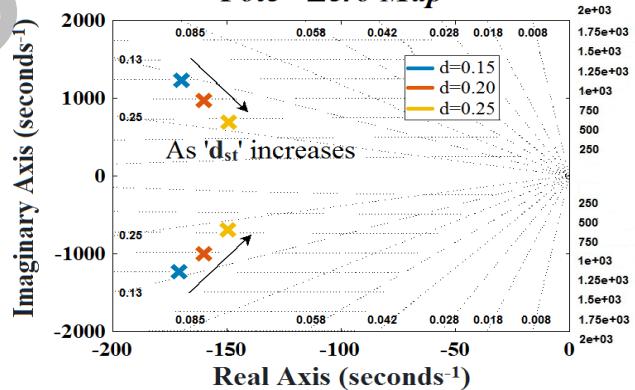


Figure 6. O-X plot for the derived transfer function

It can also be inferred that for given values, the poles of the system move towards the right as the shoot-through duty cycle has been increased. Hence, a nominal range of D_S has been chosen to carry out the simulation studies in the latter part of the paper.

C. Multilevel embedded switched-inductor z-source inverter (mESL-ZSI) with reduced H-bridge switches

A five-level (5-L) embedded switched-inductor z-source inverter (ESL-ZSI) is shown in Fig. 7, which is obtained by

cascading two ESL-ZSIs with switches S5 and S6 and connecting it to a single h-bridge inverter [19]. By switching the auxiliary switches (S5 and S6), the steeped output is obtained, unlike the conventional MLI where two h-bridge inverters are cascaded to get a five-level output. The impedance network of inductors and capacitors boosts the dc-link voltage by effectively using the shoot-through (ST) stage, and also since the source is placed within this network it draws continuous input current suitable for PV operations.

In general, the operating modes for each ESL-ZSI consist of shoot-through (boosting) mode and power (positive/negative) mode as shown in the above figure. At any time during its cycle, the topology is considered to be in these two modes to give the required voltage level. The switching pattern for the proposed system is similar to a basic cascaded MLI that gives a five-level stepped output thereby reducing the harmonic content of the output, specified in Table III.

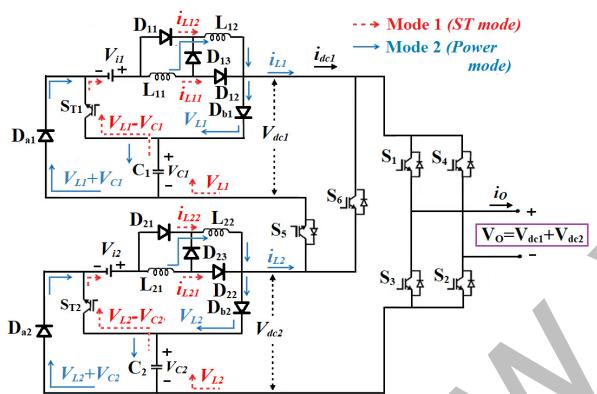


Figure 7. Schematic of the Five-level ESL-ZSI

TABLE III. SWITCHING SEQUENCE FOR MLI FOR 1 CYCLE

Output Voltage (VO)	Inverter 1 Switches	Auxiliary switches	Time period (TS)
0	ST*	S6	D _s /2
+V _{dc}	S1, S2	-	(1-D _s)/8
+2V _{dc}	S1, S2	S5	(1-D _s)/4
+V _{dc}	S1, S2	-	(1-D _s)/8
0	ST	S6	D _s /2
-V _{dc}	S3, S4	-	(1-D _s)/8
-2V _{dc}	S3, S4	S5	(1-D _s)/4
-V _{dc}	ST	-	(1-D _s)/8

ST* - shoot-through where all the switches of the H-bridge are on

With the basic knowledge of operations of ESL-ZSI the following performance equations for the proposed multilevel inverter have been derived for a symmetrical structure where L₁₁=L₁₂=L₁, L₂₁=L₂₂=L₂. During the ST mode, the inverter bridges are shorted and considered as two separate inverters represented in (24) to (27).

$$V_{L_{11}} = V_{L_{12}} = V_{i_1} + V_{C_1} = V_{L_1}; V_{L_{21}} = V_{L_{22}} = V_{i_2} + V_{C_2} = V_{L_2} \quad (24)$$

$$i_{C_1} = -2I_{L_1}; i_{C_2} = -2I_{L_2} \quad (25)$$

$$i_{dc_1} = 2I_{L_1}; i_{dc_2} = 2I_{L_2} \quad (26)$$

$$V_0 = 0 \quad (27)$$

Similarly, (28) and (30) are written to represent the MLI during the power mode,

$$i_{C_n} = I_L - i_{dc_n} \quad (28)$$

$$V_{L_1} = \frac{V_{i_1} - V_{C_1}}{2}; V_{L_2} = \frac{V_{i_2} - V_{C_2}}{2} \quad (29)$$

$$V_0 = \pm V_{peak_o} = V_{C_1} + V_{C_2} \quad (30)$$

From (28) to (30), the characteristic equation of the MLI can be obtained as follows: 1. The gain of the inverter is derived from solving the inductor voltage balance law equation (30). On solving this (31) and using them in (29), the gain equation has been derived as (32).

$$\int_0^{T_s} V_L dt = \int_0^{D_s T_s} (V_{i_1} + V_{C_1}) dt + \int_{D_s T_s}^T (V_{i_1} - V_{C_1}) dt = 0 \quad (31)$$

$$V_{C_n} = V_{dc_n(\max)} = V_{in} \left(\frac{1+D_s}{1-3D_s} \right) \quad (32)$$

$$V_0 = V_{C_1} + V_{C_2} = (V_{i_1} + V_{i_2}) \left(\frac{1+D_s}{1-3D_s} \right) = (V_{i_1} + V_{i_2}) B \quad (33)$$

where, $B = \left(\frac{1+D_s}{1-3D_s} \right)$ is the boost factor of the inverter.

Similarly, the average inductor current (I_{Ln}) and therefrom the equation for capacitor voltage ripple (ΔV_{C_n}) has been obtained with the help of the capacitor current balance law ($\int_0^{T_s} i_c dt = 0$). By means of (33) (capacitor current equation), (34) is obtained.

$$i_{C_n} = -2I_{L_n} = C_n \frac{dV_{C_n}}{dt} = 2C_n \frac{\Delta V_{C_n}}{D_s T_s} \quad (34)$$

$$|\Delta V_{C_n}| = \frac{I_{L_n}}{C_n} D_s T \quad (35)$$

Now, on substituting the values of i_{dc1} and i_c in (28), and simplifying we get (36). (37) has been derived by substituting inductor current in (35). The equation is used to calculate the value of the capacitor for a given ripple level (38), where $x\%$ (allowable voltage ripple) = $(\Delta V_{C_n} / V_C) \cdot 100$.

$$I_{L_n} = \frac{(1-D_s)(1+D_s)V_{i,n}}{R(1-3D_s)^2} \quad (36)$$

$$|\Delta V_{C_n}| = \frac{D_s(1-D_s)(1+D_s)V_{i,n}}{RC_n f(1-3D_s)^2} \quad (37)$$

$$C_n = \frac{D_s(1-D_s) \times 100}{Rf(1-3D_s)x\%} \quad (38)$$

The ripple for inductor current is derived from the basic inductor voltage law shown in the following (39) and (40).

$$L_n = \frac{di_{L_n}}{dt} = V_{i,n} + V_{C_n} \quad (39)$$

$$\int di_{L_n} = \left[\frac{V_{i,n}}{L_n} + \frac{V_{i,n}(1+D_s)}{(1-3D_s)L_n} \right] \frac{D_s T}{2} = \frac{D_s}{L_n f} \left(\frac{1-D_s}{1-3D_s} \right) V_{i,n} \quad (40)$$

The design equation for the inductor has been derived similarly to the capacitor with the help of $x\% = (\Delta i_{L_n} / i_L) \cdot 100$ (allowable current ripple), shown in (41),

$$L_n = \frac{RD_s(1-3D_s)x100}{f(1+D_s)x_L\%} \quad (41)$$

With the help of the above design equations, the proposed multilevel inverter will be modeled and implemented in the following sections. The control pulses for both the h-bridge and the shoot-through switches of the MLI are obtained using a basic sine multicarrier PWM, discussed in the next section.

D. Multicarrier PWM (mcPWM) for MLI

As the name suggests, this PWM method uses multiple carrier signals to generate effective control pulses for the h-bridge of the multilevel inverter. There are 3 types of multicarrier based on level-shift types [20]: *a*) Phase disposition with all carrier signals being identical, *b*) phase opposition disposition with signals above and below the zero lines carriers are displaced by 180° and *c*) A-phase disposition with each signal is in 180° difference. Additionally, the inverse-sine multicarrier PWM (Fig. 8) method is considered, where the level-shifted inverse sine carrier signals are compared to generate pulses for the switches [19]. Though all the methods give almost identical output by literature, it has been verified that both PD and inverse-sine methods result in lesser THD than POD and APOD. For simplicity, the phase disposition mcPWM method has been employed in this work.

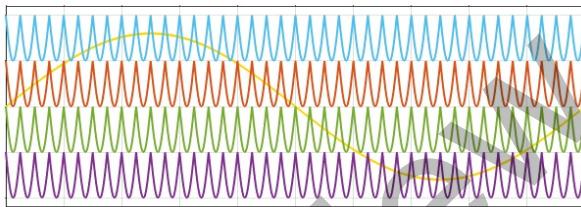


Figure 8. Inverse-sine mcPWM

$$V_{st} = V_{car}(1-D_S) \quad (42)$$

The pulses from the modulator should be a factor of both the mcPWM and the shoot-through duty cycle (D_S), for which a separate shoot-through index is used to obtain the pulse for the shoot-through switch and for computing the final pulse for the inverter bridge. The value of the ST index is chosen based on (42), where D_S is chosen based on the requirement.

E. Loss and Efficiency Calculation

The efficiency of the proposed multilevel inverter is calculated in this section. The efficiency of any converter is based on the total power loss of the converter which is given by (43).

$$\eta\% = \frac{P_o}{P_o + P_{Loss}} \cdot 100 \quad (43)$$

where P_o is the output power of the converter and P_{Loss} (P_{TL}) is the total power loss of the converter. To obtain the P_{TL} of the inverter, losses from each component need to be calculated as given in (44), concerning which few assumptions are made for the components [17]:

$$P_{TLoss} = P_{T,S} + P_{T,D} + P_{T,rC} + P_{T,rL} \quad (44)$$

Referring to the base topology, the total power loss from the switches ($P_{T,S}$) can be calculated from the conduction loss, turn-on loss, and turn-off loss of all the switches (S_1-S_4 , S_5 , S_6 , S_{T1} , and S_{T2}) as stated in (45). Assuming the

components are turned on symmetrically (Table III), the total power loss of both the inverter H-bridge and the shoot-through switches has been derived as (46).

$$P_{T,S} = \begin{cases} 4(P_{cd,S1} + P_{sw,S1}^{on} + P_{sw,S1}^{off}) + \\ P_{cd,S5} + P_{sw,S5}^{on} + P_{sw,S15}^{off} + \\ 3(P_{cd,ST} + P_{sw,ST}^{on} + P_{sw,SST}^{off}) \end{cases} \quad (45)$$

$$P_{T,S} = \begin{cases} 4 \left[I_L V_{F,S} D_S + I_L^2 r_S D_S + I_L V_{F,S} \frac{(1-D_S)}{2} + I_L^2 r_S \frac{(1-D_S)}{2} \right. \\ \left. + \frac{1}{6} B V_{in} I_L (t_{on} + t_{off}) f_S \right] \\ + \left[I_L V_{F,S} D_S + I_L^2 r_S D_S + I_L V_{F,S} \frac{(1-D_S)}{2} + I_L^2 r_S \frac{(1-D_S)}{2} \right. \\ \left. + \frac{1}{3} B V_{in} I_L (t_{on} + t_{off}) f_S \right] \\ + 3 \left[2 I_L V_{F,S} D_S + 2 I_L^2 r_S D_S \right] \\ \left. + \frac{2}{3} B V_{in} I_L (t_{on} + t_{off}) f_S \right] \end{cases} \quad (46)$$

Similarly, the power loss associated with diodes, capacitors, and inductors can be stated from (47) to (50), where t_b is from the reverse recovery time ($t_{rr} = t_a + t_b$) which has been taken from the datasheet of the diode. The k in (44) is the number of inductors, to calculate the diode power losses in the SL cell.

$$P_{T,D} = 2 \left\{ P_{cd,Da} + P_{sw,Da}^{off} + P_{cd,DB} + P_{sw,DB}^{off} \right\} + \sum_{n=2}^{n=k} \left[\sum_{i=3}^{i=k} \left(P_{cd,D_{3n-1}} + P_{sw,D_{3n-1}}^{off} \right) \right] \quad (47)$$

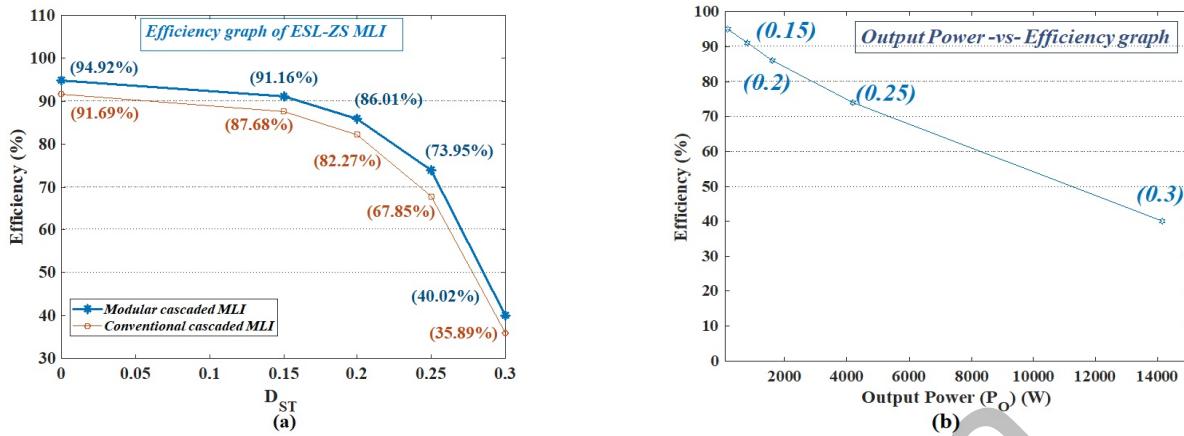
$$P_{D,tot} = 2 \left\{ \begin{array}{l} V_{F,D} I_L (1-D_S) \\ + r_D I_L^2 (1-D_S) + \\ \frac{2}{3} B V_{in} I_r t_b f_S + \\ V_{F,D} \left(I_L - \frac{B V_{in}}{R} \right) (1-D_S) \\ + r_D \left(I_L - \frac{B V_{in}}{R} \right)^2 (1-D_S) \\ + 2 \left[\frac{V_{F,D} I_L D_S +}{r_D I_L^2 D_S +} \right. \\ \left. \frac{(B+1) V_{in} I_r t_b f_S}{6} \right] \end{array} \right\} \quad (48)$$

$$P_{T,rC} = \frac{1}{T_S} \int_0^{T_S} r_C i_C^2 dt = r_C (nI_L)^2 D_S \quad (49)$$

$$+ r_C \left(I_L - \frac{B V_{in}}{R} \right)^2 (1-D_S)$$

$$P_{T,rL} = n r_L I_L^2 \quad (50)$$

Based on the formulas obtained, the efficiency of the proposed MLI is calculated by considering standard components parameters, $V_{F,S} = V_{F,D} = 1$ V, $r_S = 0.5$ Ω, $r_D = 0.1$ Ω, $t_{on} + t_{off} = 90$ nS, $t_b(t_d) = 20$ nS, $I_{rr} = 10$ μA, $R = 45$ Ω, $r_C = 0.2$ Ω, $r_L = 0.15$ Ω (taken from datasheets of IRF740 and MUR1560G) for $V_{in} = 50$ V with $f_S = 25$ kHz which is chosen from literature.

Figure 9. (a) Efficiency -vs- D_S , (b) Efficiency -vs- P_O

The efficiencies of both the conventional and the developed ESL-ZS multilevel inverter over different duty cycle are shown in a graphical format in Fig. 9(a). Also, the plot showing the effect of efficiency with increase in output power (P_O) is shown in Fig. 9(b). It may be noted that the efficiency of the converter decreases as the shoot-through duty cycle is increased; hence a duty cycle of 0.2 is considered an optimal value as increasing the duty cycle beyond that decreases the efficiency drastically below 70%.

IV. PV-GRID SYNCHRONISATION

A. Photovoltaic Model with MPPT

The multilevel inverter can be powered from a PV model, which will be modeled based on the characteristic equations of the one-diode model [20] (Fig. 10). The effect of series and shunt resistors (R_S & R_{Sh}) are usually neglected owing to their extreme values

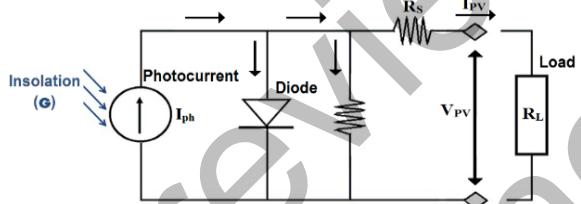


Figure 10. One-diode model of PV

The output current of the one-diode PV model is given by (51), where parameters are designed at standard conditions for a PV cell.

$$I_{pv} = \begin{cases} \left(N_p \times I_{ph} \right) - N_p \times I_o \left[\exp \left\{ \frac{q \times (V_{pv} + I_{pv} R_s)}{N_s A k} \right\} - 1 \right] \\ - \frac{V_{pv} + (I_{pv} R_s)}{R_{sh}} \end{cases} \quad (51)$$

To feed a 3-phase grid, a 4×15 PV array has been considered to power each phase of the proposed MLI to feed standard three-phase grid values. The model of the PV is referenced from the Solkar 36W_p PV module [21]. With the values provided, the above PV model has been designed for standard G and T values.

The PV module feeds out a maximum output voltage of 19V (V_{mpp}) and outputs current of 1.94A (I_{mpp}) under standard temperature and insolation ($T = 25^\circ\text{C} = T_{ref}$ and $\lambda = 1000 \text{ W/m}^2$) conditions. Yet, due to varying external conditions that lead to complexity between the temperature

and total resistance, the PV module produces non-linear output. Hence, an individual MPPT circuit is provided for the PV array per phase, which tracks and samples the PV output to calculate the fitting modulation index for the individual inverter [22]. In this work, the incremental conductance method has been used to assist the PV to reach maximum power at varying conditions in which the V_{PV} and I_{PV} have been sampled and their incremental difference has been used to enumerate the difference in power (dP/dV) [23]. The MATLAB coding for the incremental conductance technique has been taken from literature and executed using the MatLab function block [24].

B. Phase Lock for Synchronization with DQ Current Controller Method

The voltage or current signals used for synchronization might be not free of noise, harmonics, voltage sags, and swells, and phase angle jump or be corrupted by unbalanced operating conditions. To generate a reliable control strategy where a smooth transition between two modes of operation of a grid is achieved, a synchronization of the grid and the inverter output has been carried out [25].

A PLL has been installed for detecting the phase angle of an assumed input signal. A basic PLL mainly consists of a phase detector, loop filter, and a voltage-controlled oscillator (VCO) in a feedback loop. Many new PLL schematics have emerged as a variation of the basic structure such as single, enhanced, quadrature, synchronous reference frame, adaptive notch filtering, etc. The main problem in the grid system is to detect the difference in phase angle concerning the input signal and drive this value to zero with the support of a controller. In this work, a simple DQ frame current controller (Fig. 11) has been used to stabilize the power flow between the inverter and the grid [26]. The PI controller tracks and regulates the current that results in minimum to zero steady-state error in the system.

The terms DQ and $\alpha\beta$ in the figure refer to the variables in the DQ-frame and $\alpha\beta$ -frame. Here, the reactive current (I_q) reference is given zero since the system variables are dc; based on which the reference for the PWM modulator is calculated.

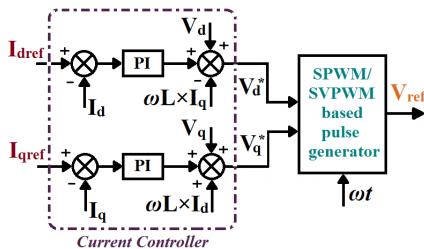


Figure 11. DQ-frame current controller

V. SIMULATION

In this section, the simulation of the overall circuit in MATLAB/Simulink software has been discussed based on the analysis and the design of the inverter discussed above. The parameter considered for the simulation is given in Table IV.

TABLE IV. COMPONENT FOR SIMULATION

Component	Value				
Input Voltage (V_{in1}/V_{in2})	45-75 V				
Input current (I_{in})	~29A				
Switching frequency (f_s)	25 kHz				
Modulation index (M)	0.8-0.9				
Shoot-through duty cycle (D_S)	0.2				
Boost factor (B)	3				
Inductors (L_1, L_2)	2.5 mH				
Capacitor (C)	50 μ F				
Inverter	<table border="1"> <tr> <td>Filter Capacitor (C_f)</td><td>1 μF</td></tr> <tr> <td>Filter Inductor (L_f)</td><td>1mH</td></tr> </table>	Filter Capacitor (C_f)	1 μ F	Filter Inductor (L_f)	1mH
Filter Capacitor (C_f)	1 μ F				
Filter Inductor (L_f)	1mH				
Grid	<table border="1"> <tr> <td>Filter Capacitor (C_f)</td><td>2 μF</td></tr> <tr> <td>Filter Inductor (L_{f1-1})</td><td>10mH</td></tr> </table>	Filter Capacitor (C_f)	2 μ F	Filter Inductor (L_{f1-1})	10mH
Filter Capacitor (C_f)	2 μ F				
Filter Inductor (L_{f1-1})	10mH				

The simulation circuit for the proposed multilevel inverter with DC input and load for one phase was carried out and per-phase values of the V_{dc} (dc-link voltage), V_o (Output voltage) and I_o (Output current), for different voltage levels are shown in Fig. 12. The voltages of $V_{ST1-ST2}$, V_{S5} , V_{S6} and V_{Da} , V_{Db} (D_a and D_b), i_{L1-L2} are presented in Fig. 13 and Fig. 14.

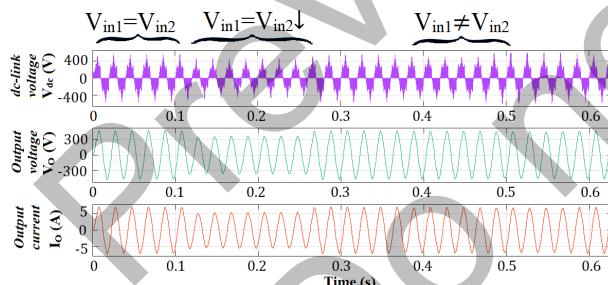


Figure 12. The per-phase dc-link and output values for varying input values

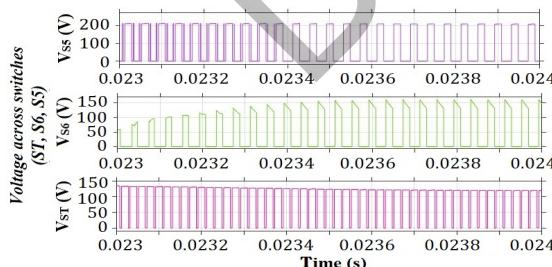


Figure 13. The voltage across ST switches for single phase

The overall simulation of the proposed work (represented in Fig. 1) with the controller circuits has been carried out. The grid is connected to the inverter through a filter circuit to trim and regulate the flow of power between them.

Having studied many new filter circuits in the literature, a basic LCL filter (T-filter) has been considered optimum for the PV-grid interface for this work. The design of the T-filter is considered [27], to provide a better output by reducing the THD.

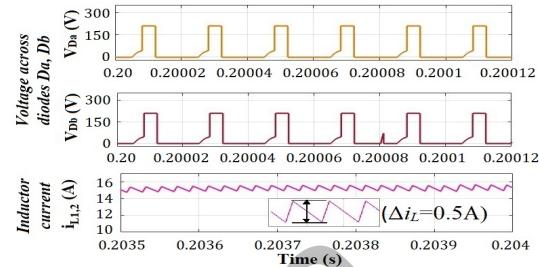


Figure 14. Voltage and current across diode and inductors respectively

The outputs from the PL blocks are represented in Figs. 15 and 16. The figures show the individual phase reference waveforms, and the changes in DQ current values to synchronize the grid.

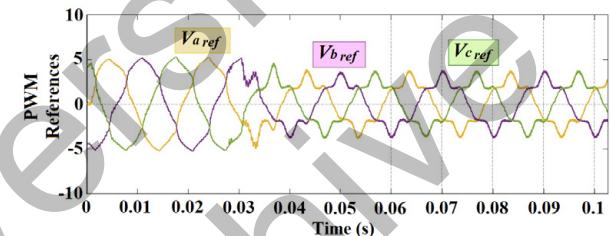


Figure 15. The reference waveform from the controller

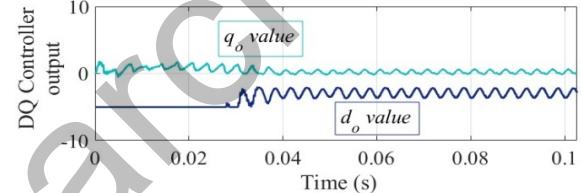


Figure 16. Change in controller DQ values

It can be observed from Fig. 17, that grid current is in synchronization with the inverter current, while the grid values are also in phase with each other. The effect of varying voltage (result partial shading) on the MLI and thereby on the grid outputs can be viewed in Fig. 18.

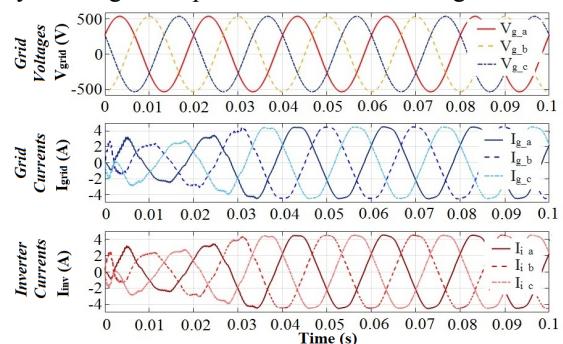


Figure 17. Outputs of the grid with inverter current

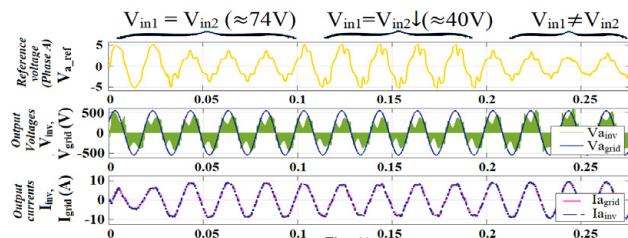
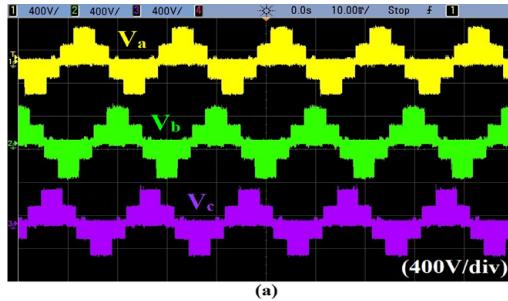


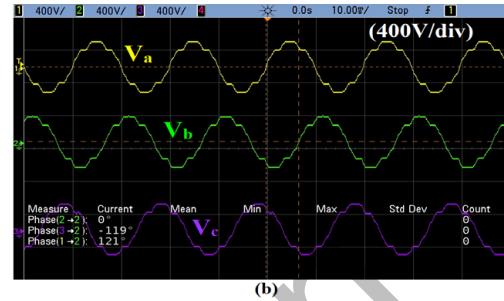
Figure 18. Effect of varying voltage on output grid values

VI. HARDWARE STUDY

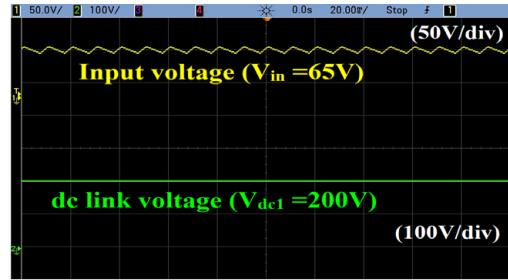
The hardware prototype of the three-phase five-level embedded switched-inductor z-source inverter has been fabricated and tested. The prototype has been powered by a



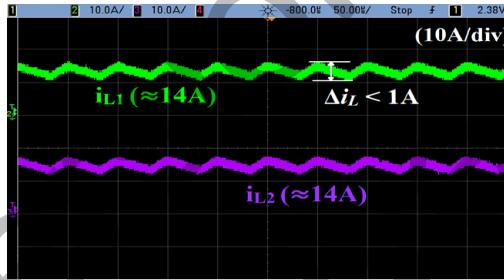
(a)

Figure 19. V_o for 3 phases a) without filter

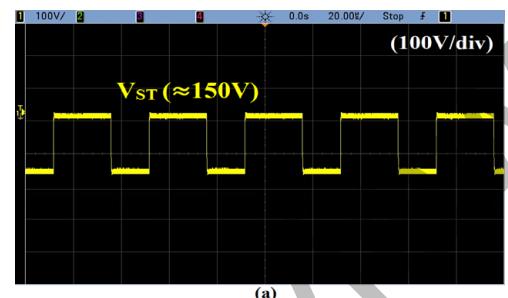
(b)



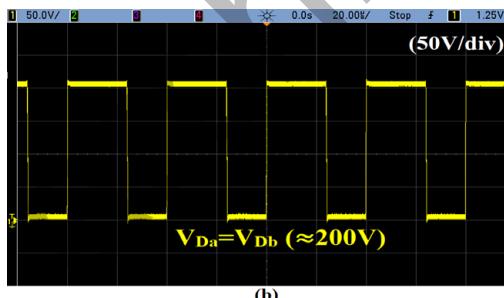
(a)

Figure 20. Per phase values (Phase-A): a) V_{in} and V_{dc} , b) i_{L1} and i_{L2} 

(b)



(a)

Figure 21. Voltages through Shoot-through switches V_{ST} ($V_{ST1}=V_{ST2}=V_{ST}$) and voltage across the diodes ($V_{Da}=V_{Db}$)

(b)

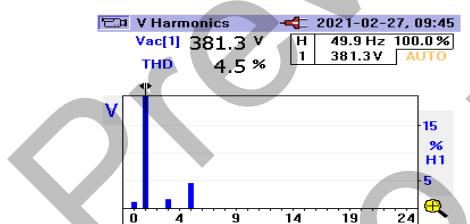
Figure 22. Harmonic analysis of V_o (Output voltage) and I_o (Output current)

Fig. 19 shows the output waveforms of the proposed MLI for 3 phases and the filtered waveform across the load with a respective phase shift. Mainly, it was observed that the input voltage has been boosted slightly more than 3 times (gain) for the given shoot-through of 20%.

In other words, the expected gain value has been attained for input less than 76V (i.e., simulated value) as shown in Fig. 20(a). Figs. 20(b) and Fig. 21 shows the inductor currents (i_{L1} , i_{L2}), the voltage across the shoot-through switches ($V_{ST1}=V_{ST2}=V_{ST}$), and the voltage across the diodes 'a' and 'b' for one phase (V_{Da} , V_{Db}), which are in agreement with the simulated results. The harmonic analysis of the output values across the load have been measured using a fluke meter, presented in Fig. 22.

DC source to feed a 3-phase load for a D_S ratio of 20% and modulation index of 90%. The PWM pulses for the proposed inverter have been programmed into the FPGA processor using Xilinx.

To carry out the simulation study of the proposed

VII. CONCLUSION

A multilevel cascaded topology using an embedded switched inductor Z-source inverter (mESL-ZSI) and modular h-bridge, for a PV interface application involving shorter series strings that produce low output voltage was discussed in this paper. To analyze the stability of its base inverter (ESL-ZSI), both its steady-state and dynamic equations were derived in theory and verified. Based on this, the multilevel topology was obtained by cascading two 3-level ESL-ZSI networks with a modular MLI that uses less switching components. This paper further discusses the modes of operation with which the topology's characteristic equations were derived.

multilevel inverter, the topology was executed in MATLAB using the values from the literature. When a basic multicarrier PWM method was employed, the simulation results showed that the inverter was able to produce a high gain output for an optimum D_S of 0.2 with low voltage stress across the ST switch. As the basic idea of the work was to implement the proposed MLI in PV interfaced applications, the inverter was simulated with a PV-grid interface for standard three-phase conditions. A PV array of 2kW rating with shorter series string and more parallel strings was connected per phase of the MLI connected to a 3-phase grid. The grid outputs were synchronized with that of the inverter by implementing a current controller with PLL. It was observed that even under non-symmetrical input conditions, the grid values were kept synchronized thereby providing a reliable supply to the grid. A hardware prototype of the proposed MLI was built to verify the result from the simulation study and to verify the results in real-time applications. The results obtained illustrated and proved that the proposed MLI produced high gain output with reduced voltage stress; hence, it was found to be suitable for PV array structure with short series connections to lessen the effect of partial shading, like a grid-connected PV system.

ACKNOWLEDGMENT

The authors would like to convey their gratitude to the Management of Sri Sivasubramaniya Nadar College of Engineering, Rajiv Gandhi Salai (OMR), Kalavakkam, Tamil Nadu, India, for providing all the necessary assistance to complete this work.

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