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Preface

Power system is undergoing tremendous developments such as integration of more and more renewable energy resources, advancements in power electronic interfaces, energy efficiency measures, control and introduction of more intelligence in the grid. This book constitutes selected high-quality papers presented in the Second International Conference on Power Engineering, Computing and CONtrol, PECCON 2019, during 12 to 14 December 2019.

The main theme of PECCON 2019 is "smart technology for smart grid". The conference provided a forum for practicing professionals, academicians, research scholars and students to exchange their innovative ideas, inferences and knowledge gathered through rigorous experiments. This book volume consists of 39 chapters and is organized into four parts—*Sustainable Energy Technologies*, *Power Electronics*, *Electric Vehicles* and *Allied Technologies*. This book will be useful to the researchers, academicians, students and professionals working in the field as well as R&D organizations in the domain of electrical power and energy infrastructure.

We, the editors of this book, are thankful to all the authors who have contributed to the paper submission. We also thank all the reviewers and technical committee members for providing their valuable comments on time and help towards the improvement of the quality of papers presented in the conference. We also thank members of the advisory board and session chairs for their valuable comments. Our special thanks to Series Editors, Lecture Notes in Electrical Engineering, Springer, for giving us the opportunity to publish this edited volume in the series.

Chennai, India K. Jamuna
Fisciano, Italy Pierluigi Siano

About the Editors

Dr. Pierluigi Siano (M'09–SM'14) received the M.Sc. degree in electronic engineering and the Ph.D. degree in information and electrical engineering from the University of Salerno, Salerno, Italy, in 2001 and 2006, respectively. He is a Professor and Scientific Director of the Smart Grids and Smart Cities Laboratory with the Department of Management & Innovation Systems, University of Salerno. His research activities are centered on demand response, on the integration of distributed energy resources in smart grids and on planning and management of power systems. He has co-authored more than 450 papers including more than 250 international journal papers that received more than 8400 citations with an H-index equal to 46. He received the award as 2019 Highly cited Researcher by ISI Web of Science Group. He has been the Chair of the IES TC on Smart Grids. He is Editor for the Power & Energy Society Section of IEEE Access, IEEE Transactions on Industrial Informatics, IEEE Transactions on Industrial Electronics, Open Journal of the IEEE IES and of IET Renewable Power Generation.

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Mathematical Modelling of Embedded Switched-Inductor Z-Source Inverter for Photovoltaic Energy Conversion

T. Divya and R. Ramaprabha

Abstract Z-source inverters provide single-stage power conversion for photovoltaic (PV) interface as it does the job of boosting and DC-AC conversion. The topology presented here is derived by fusing the switched-inductor cell (SL) in an embedded switched Z-source inverter which eliminates the problem of inverter leg short circuit (SC). Its output voltage varies over a wide range without any requirement of a time delay in turning on the power switches. This inverter generates high gain factor for the same structural elements in comparison with other topologies and is expected to give continuous input current, and hence, it is more suitable for PV and fuel cell interface. The mathematical model of ESI-ZSI along with PV array is presented in this chapter. The advantageousness of the ESI-ZSI inverter over few basic inverters will be presented by comparing the parameters of the similar existing topologies reported in the literature.

Keywords Z-source inverter · Modelling · PV module · Incremental conductance

1 Introduction

Energy conservation has been a central topic for many government schemes owing to the decrease in conventional energy resources with the rapid increase in energy demand. First preference is given to solar energy or in other words, photovoltaic (PV) energy, because of its abundance in nature, green, and inexhaustible [1, 2]. Existing PV panels have a lower and varying range of input voltage, and thus, the energy converted by photovoltaic panels, intended for any specific application, should be conditioned by a suitable inverter for further use. Also in many applications, the single-stage architecture is often preferred to realize PV interfaced applications due to its considerable reduction in power loss. Such conditions demand for a buck-boost type inverters, and one such inverter to convert and boost the PV voltage for required applications is presented in this paper with PV interfacing.

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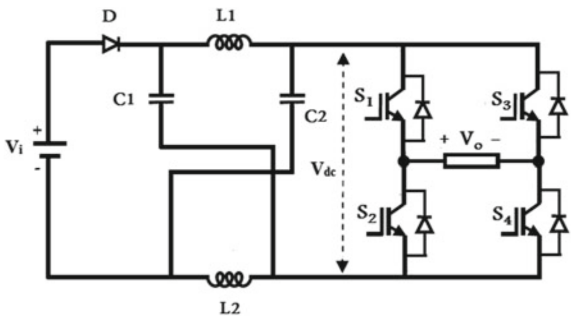


Fig. 1 Impedance source inverter

Conventional VSIs and CSIs experience similar problem such as (1) works only in either buck or boost mode, (2) high harmonics and electromagnetic inference (EMI), and (3) high voltage stress of input range [3–5]. New and combination of topologies have been developed to offer a better boost value for nominal duty ratio. Z-source inverter (ZSI) (Fig. 1.) was developed for extending the output range of inverter by providing both buck and boost operation. But a conventional ZSI also experiences several drawbacks; hence, modifications of existing and new topologies based on ZSI have been suggested, allowing an extended range of power conversion applications [6, 7].

Along the way, another novel power converter having the same functionality as ZSI was proposed, switched boost inverter (SBI) [8, 9]. This work focuses on few topological changes to an existing topology to increase its efficiency while retaining its main operational merits. Basically, an embedded Z-source (EZSI) is considered for its reduced capacitor voltage rating. Adding to this, the switched-boosting network replaces the inductive structures to provide a stable inverter structure. Along with the structure model, generalized modelling of a PV array with MPPT will be presented in this paper as an overall system.

2 Embedded Switched-Inductor ZSI

A new topology with a boosting network incorporated in an embedded switched boost inverter (ESBI) [10] is presented as in Fig. 3. The network consisting of three diodes and two inductors called the switched-inductor (SL) cell usually connects the source and the inverter network as shown in Fig. 2a, b which shows SL cell with $n \geq$ two diodes and inductors.

The operation of the modified inverter consists of three basic modes based on the operating conditions of the switches and diodes of the network similar to that of ESBI. The shoot-through in the ZSI is a major boosting factor of the topology. Hence, the duty cycle (D) of the inverter is considered to be above 0.5, and D_{St}—period of shoot-through is considered 0.2. The modes are briefly explained below.

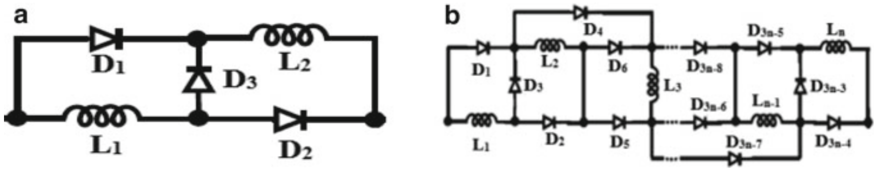


Fig. 2 **a** A switched-inductor network. **b** SL cell with $n \geq 2$

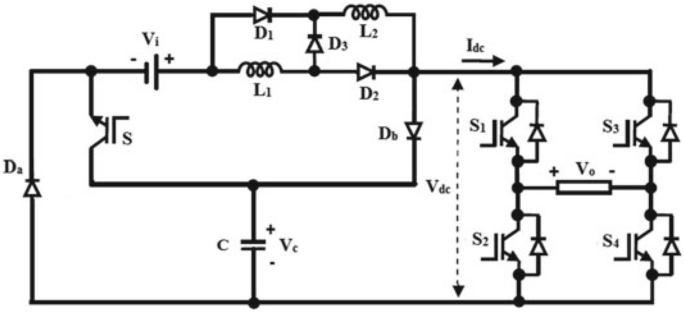


Fig. 3 A embedded switched-inductor ZSI (ES-ZSI)

For Mode-1 (M1), shoot-through stage, all switches (S_1–S_4) of the inverter plus switch (S) are turned on. The diodes are reversed, and thereby, capacitor's stored energy charges the inductor's stored energy.

The energy stored of the capacitor can be obtained as using KVL,

$$v_{Da} = v_{Db} = -V_C;\ i_c = -2I_L \tag{1}$$

$$v_{D3} = -V_C - V_i \tag{2}$$

The inductor voltage is

$$v_L = v_{L1} = v_{L2} = V_C + V_i \tag{3}$$

The inductor current increases by a slope of $\frac{V_c+V_i}{2\mathrm{L}}$. At mode 1, the two inductor currents supply i_{DC} to the inverter neglecting the ripple. For M1,

$$i_{dc} = 2I_L \text{ and } v_o = 0 \tag{4}$$

For Mode-2 (M2), except for S_1 and S_4, other switches are turned off for normal boosting stage. The capacitor's stored energy increases while the inductor's decrease since its voltage goes negative.

Since diode D_b is forward biased, the capacitor stored energy is given by KVL,

$$i_c = I_L - i_{dc};\ V_C = v_{dc} \tag{5}$$

The inductor-stored energy is decreased by a slope of $\frac{V_i - V_c}{2L}$, and Eq. (4) gives its equating parameters:

$$v_L = v_{D1} = v_{D2} = \frac{V_i - V_c}{2} \tag{6}$$

For M2, the maximum output

$$v_o = v_{dc,max} \tag{7}$$

For Mode-3 (M3), this is similar to M2 with S_2 and S_3 which are turned on while the rest are off. The output of the inverter is negative in this mode.

For M3, the minimum output

$$v_o = -v_{dc,max} \tag{8}$$

In Fig. 4, G_S–G_{S4} represent the switching signals of the switches S–S_4. The same topology can be improvised by linking n number of SL cells instead of one with just 2Ls and 3Ds.

The gate pulses G_S–G_{S4} are provided with a simple sine PWM method provided in [10, 11], where a sine wave envelope and a straight-line envelope are used for inverter switches and shoot-through switch in the circuit.

3 Modelling of the Performance Parameters

3.1 Overall Voltage Gain

Voltage gain factor is calculated by means of the inductor voltage balance law, characterized by Eq. (9) over T (the time period of the modified inverter).

$$\int_0^t V_L \mathrm{d}t = 0 \tag{9}$$

Substituting from Eq. (3), (6) in above equation, we get

$$\int_0^{D_{St}\mathrm{T}} (V_c + V_i)\mathrm{d}t + \int_{D_{St}\mathrm{T}}^{T} (\frac{V_i - V_c}{2})\mathrm{d}t \tag{10}$$

The average capacitor voltage can be obtained on simplifying Eq. (10),

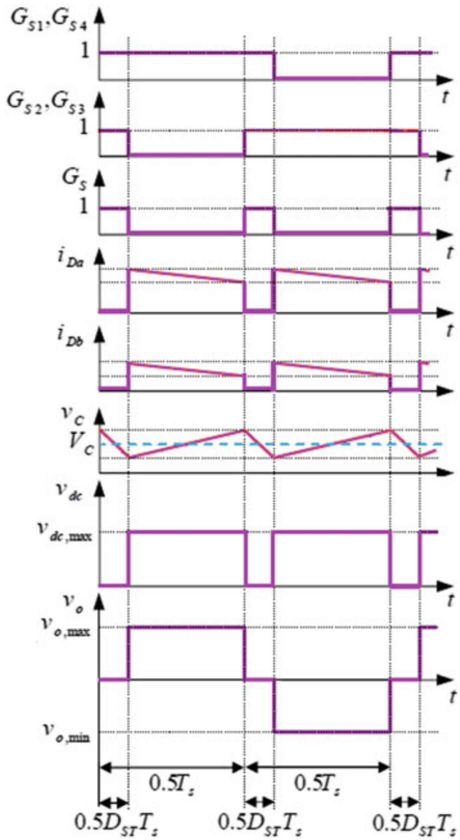


Fig. 4 Waveforms of ESI-ZSI

$$V_c = \frac{1 + D_{St}}{1 - 3D_{St}} V_{\mathrm{i}} \tag{11}$$

From Eq. (5),

$$v_{\mathrm{dc,max}} = V_c = \frac{1 + D_{St}}{1 - 3D_{St}} V_{\mathrm{i}} = B V_{\mathrm{i}} \tag{12}$$

where B is boosting factor, consequently the peak values of the load voltage are given as

$$v_{\mathrm{o,max}} = -v_{\mathrm{o,min}} = v_{\mathrm{dc,max}} = \frac{1 + D_{St}}{1 - 3D_{St}} V_{\mathrm{i}} \tag{13}$$

3.2 Current Ripple of Inductor

Inductor current ripple is derived from the inductor voltage $v_L = L\frac{di_L}{dt}$, and Eq. 3 is represented in Eq. 14,

$$\Delta i_L = \frac{V_c + V_i}{2L} D_{St} T \tag{14}$$

From Eqs. 11 and 14,

$$|\Delta i_L| = \frac{D_{St}(1 - D_{St})}{L f_s (1 - 3D_{St})} V_i \tag{15}$$

From Eq. 15, it can be computed that switching frequency, and the inductance is inversely proportional to the inductor current ripple.

3.3 Voltage Ripple of Capacitor

Capacitor voltage ripple is derived from the capacitor current $i_c = C\frac{dv_c}{dt}$, and Eq. 1 is represented in Eq. 16,

$$-2IL = 2C\frac{\Delta v_c}{D_{St} T} \tag{16}$$

This is rewritten as,

$$|\Delta v_c| = \frac{D_{St} I_L T}{C} \tag{17}$$

From Eqs. (1), (5), (14), and the capacitor current balance law,

$$-2I_L D_{St} T + (1 - D_{St})[I_L - \frac{(1 + D_{St})V_i}{R(1 - 3D_{St})}]T = 0 \tag{18}$$

The inductor current value can be obtained on simplifying the above equation.

$$I_L = \frac{(1 - D_{St})(1 + D_{St})V_i}{R(1 - 3D_{St})^2} \tag{19}$$

Substitute the value of Eq. 19 in Eq. 17

$$|\Delta v_c| = \frac{D_{St}(1 - D_{St})(1 + D_{St})V_i}{RCf_s(1 - 3D_{St})^2} \tag{20}$$

Similarly, from Eq. 20, it can be computed that capacitor voltage ripple is inversely proportional to the capacitance of the inverter.

4 Comparison of Performance Parameters

This section briefs the comparative analysis of the modified topology with basic inverter topologies in literature. The comparison will be based on gain factor (B), ripple of the inductor current ($|\Delta i_L|$) and ripple of the capacitor voltage ($|\Delta v_c|$). Figure 5 presents the circuit diagram of the embedded switched boost inverter [10].

Increased gain factor will be the primary aim of the topology, and its advantages and disadvantages will be obtained by comparing it with embedded switched boost inverter and ZSI (Fig. 5).

The derivations of these parameters have been studied with its working in [3, 10]. The related equations of the proposed inverter along with topologies to be compared obtained from the studies are given in Table 1 From the table, it can be observed that the D_{st} is the common factor for all the parameters in all these topologies.

The performance parameters are calculated theatrically using the above derivations. Tables 2 and 3 show the comparative performances of the inverter topologies based on the parameters calculated mathematically.

The calculations from the table yield that the given topology produces an increased gain factor in comparison with the basic topology for lesser number of passive elements. Table 4 also illustrates that increasing the shoot through duty cycle also

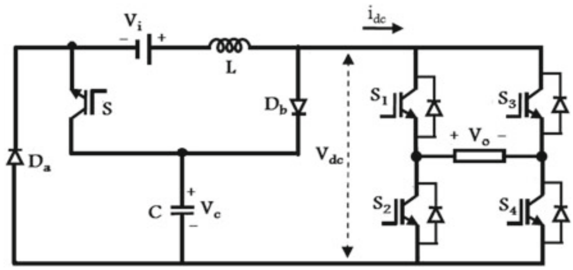


Fig. 5 Embedded switched boost inverter

Table 1 Comparison of parameters

Parameters	ZSI	ESBI	ESI-ZSI
B	$\frac{1}{1-2D_{St}}$	$\frac{1}{1-2D_{St}}$	$\frac{1+D_{St}}{1-3D_{St}}$
$\lvert\Delta i_L\rvert$	$\frac{(1-D_{St})V_i}{Lf_s(1-2D_{St})}$	$\frac{D_{St}(1-D_{St})V_i}{Lf_s(1-2D_{St})}$	$\frac{D_{St}(1-D_{St})V_i}{Lf_s(1-3D_{St})}$
$\lvert\Delta \boldsymbol{v}_{\mathbf{c}}\rvert$	$\frac{D_{St}(1-D_{St})V_i}{RCf_s(1-2D_{St})}$	$\frac{D_{St}(1-D_{St})V_i}{2RCf_s(1-2D_{St})^2}$	$\frac{D_{St}(1-D_{St})(1+D_{St})V_i}{RCf_s(1-3D_{St})^2}$
Passive elements ($L + C$)	$2 + 2$	$1 + 1$	$2 + 1$

Table 2 Comparison of gain factor

D_{st}	ZSI/ESBI	ESI-ZSI
0.15	1.43	2.09
0.2	1.67	3
0.25	2	5
0.3	2.5	13

Table 3 Comparison of inductor current ripple

D_{st}	ZSI	ESBI	ESI-ZSI
0.15	2.59	0.39	0.49
0.2	2.84	0.5	0.85
0.25	3.2	0.8	1.6
0.3	3.73	1.12	4.48

Table 4 Comparison of capacitor voltage ripple

D_{st}	ZSI	ESBI	ESI-ZSI
0.15	0.15	0.06	0.15
0.2	0.22	0.08	0.25
0.25	0.31	0.103	0.44
0.3	0.43	0.135	1.18

increases the ripples along with the gain factor; hence, the D_{st} is varied from (0.15–0.25)

5 Photovoltaic Model

5.1 Modelling of the Cell

The photovoltaic (PV) array provides the source for the designed inverter; the PV cell is modelled from the equation of one-diode model [11] (Fig. 6). The figures show the important elements of the PV model which will be designed based on the following equation.

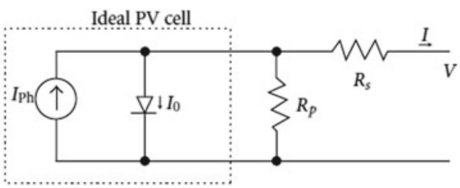


Fig. 6 One-diode model

where
$\mathbf{I_{ph}}$, photocurrent
$\mathbf{R_s}$, series resistance (*very small—neglected*)
$\mathbf{R_{sh}}$, shunt resistance (*very large—neglected*).

The I_{ph} equation for a one-diode model is given below, based on which the modelling of the PV cell will be explained.

$$I_{\text{ph}} = [I_{\text{scr}} + K_i(T_k - T_{\text{ref}})] * \frac{\lambda}{1000} \tag{21}$$

where
I_{ph}, current at 25 °C and 1000 W/m^2
I_{scr}, SC current at 25 °C and 1000 W/m^2 (2.55 A)
K_i, SC current/temperature coefficient (0.0017 A/k)
T_k, Actual temperature (in K)
T_{ref}, reference temperature (298 K)
λ, irradiation (1000 W/m^2)

Other important factors needed to model the PV cell are the reverse saturation current (I_{rs}) and saturation current (I_{O}), and the equation for the factors is be given by the equation below

$$I_{rs} = \frac{I_{\text{scr}}}{\left[\exp\left(\frac{qV_{\text{oc}}}{N_s kAT}\right) - 1\right]} \tag{22}$$

where
q, electron charge (1.6×10^{-19} C)
V_{oc}, open-circuit voltage (21.24 V)
N_{S}, no. of cells in series (36)
K, Boltzman constant (1.3805×10^{-23} J/K)
A, ideality factor (1.6)

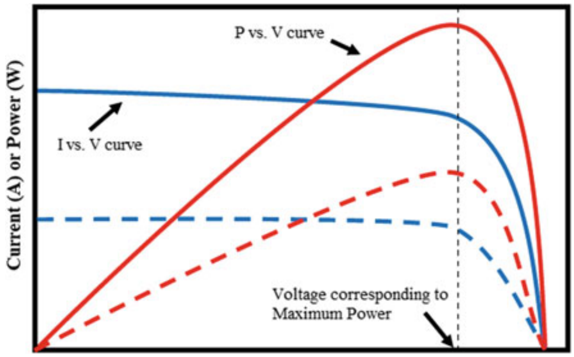
$$I_{\text{O}} = I_{\text{rs}}\left[\frac{T}{T_r}\right]^3 \exp\left[\frac{\text{q} * \text{E}_{\text{go}}}{\text{Ak}}\left\{\frac{1}{\text{T}_{\text{r}}} - \frac{1}{\text{T}}\right\}\right] \tag{23}$$

where
T, operating temperature (K)
E_{go}, band-gap energy (1.1 eV @ 25 °C)

From the above factors, the output current of the one-diode PV model is given by equation

$$I_{\text{PV}} = N_{\text{p}} * I_{\text{ph}} - N_{\text{p}} * I_{\text{O}}\left[\exp\left\{\frac{q * (V_{\text{PV}} + I_{\text{PV}} R_{\text{s}})}{N_{\text{S}} Ak}\right\} - 1\right] - \frac{V_{\text{PV}} + (I_{\text{PV}} R_{\text{S}})}{R_{\text{Sh}}} \tag{24}$$

Fig. 7 PV characteristics



For simplification, N_s is considered as 36, and N_p is considered to be 1 for simplification. Since we have considered the value of R_{sh} to be high, the above I_{PV} will change as follows,

$$I_{PV} = I_{ph} - I_O\left[\exp\left\{\frac{q * (V_{PV} + I_{PV}R_s)}{N_S A k}\right\} - 1\right] \tag{25}$$

The output voltage and current are measured to plot the characteristics of the designed PV; Fig. 7 shows the PV characteristics (I–V and P–V).

5.2 PV Sizing

The simulation is designed a source power of (110–120) W, and hence, a PV module with maximum output voltage of 16.54 V and output current of 2.25 A is considered. The model of the PV was referenced from the Solkar 36W_P PV module for which the data sheet is also given in [11]. As per our requirement, three PV modules are series connected to form the PV array with a maximum power point voltage of 49.6 V and power of 112 V (3 × 1 array). Figure 13 shows the series connected PV modules used in the work.

5.3 MPPT—Incremental Conductance (InC)

Maximum power point tracking is employed to track the maximum power point for the designed PV array. In this work, incremental conductance (InC) method is used for optimum usage of the PV array. The InC provides maximum power by tracking its incremental change in the PV array power using change in its current and voltage [12]. Figure 8 shows the flowchart for InC based on which a MATLAB code is written.

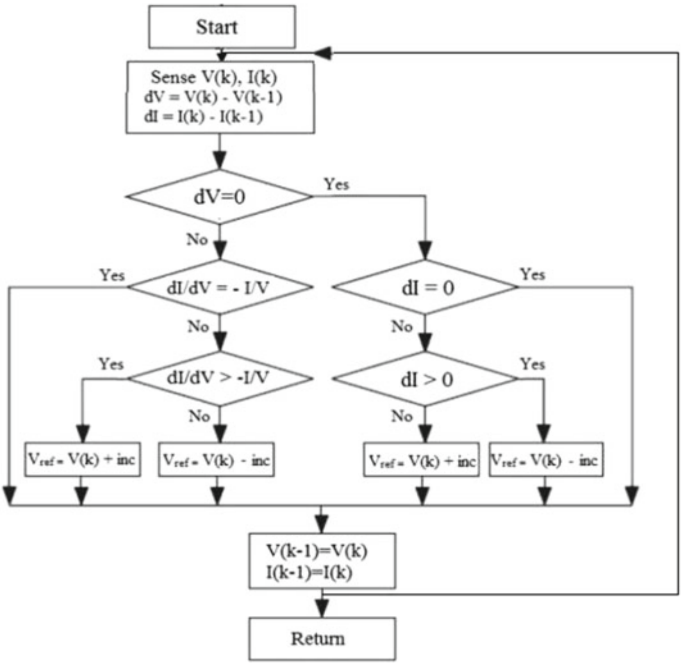


Fig. 8 InC flowchart

6 Simulation Results

6.1 PV Array

Based on the above equations, the following PV module is designed, and each parameter are designed into separate block (Figs. 9, 10, 11, 12, and 13).

6.2 ESI-ZSI Model

The simulation circuit of embedded switched-inductor ZSI supplied with the designed PV Array and MPP tracking is presented in Fig. 14. Since the output of the inverter may have unwanted frequency waves, a band pass (LC) filter is employed across load to remove the unwanted frequencies and provide an almost sinusoidal output suitable for applications. The component parameters for the simulation carried out are given below (Table 5).

From the simulation of proposed inverter using the above parameters, the output waveforms of the embedded switched-inductor ZSI are obtained as given in Fig. 16. The gating signals to be given to the switches are presented in Fig. 15.

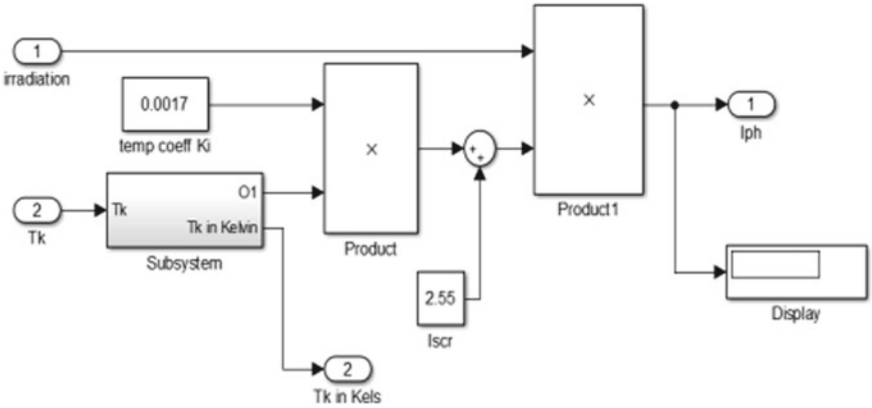


Fig. 9 I_{ph} block

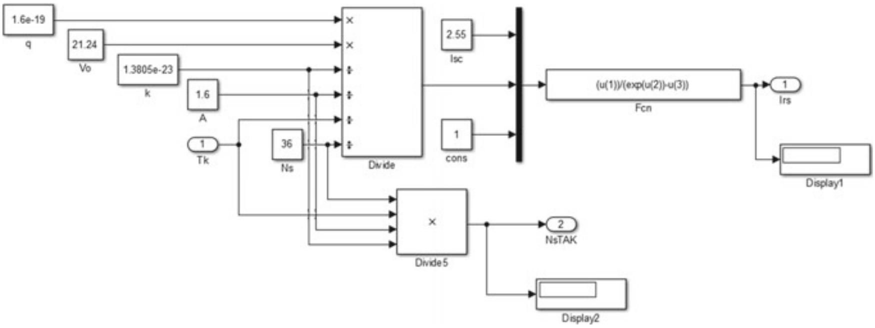


Fig. 10 I_{rs} block

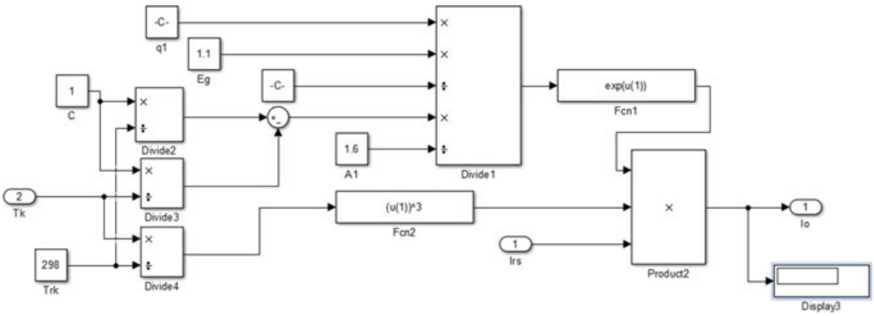


Fig. 11 I_{o} block

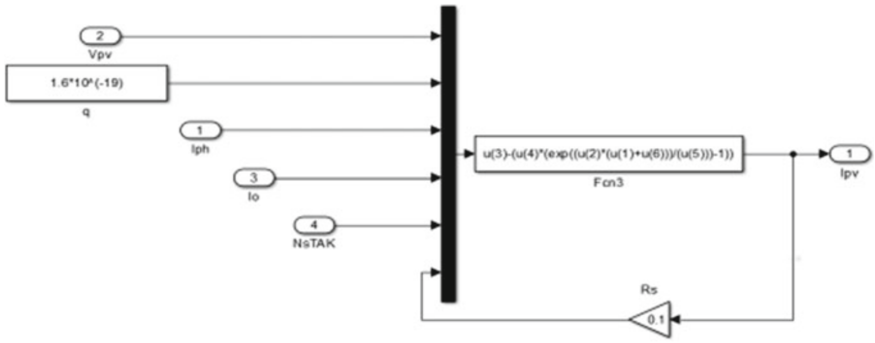
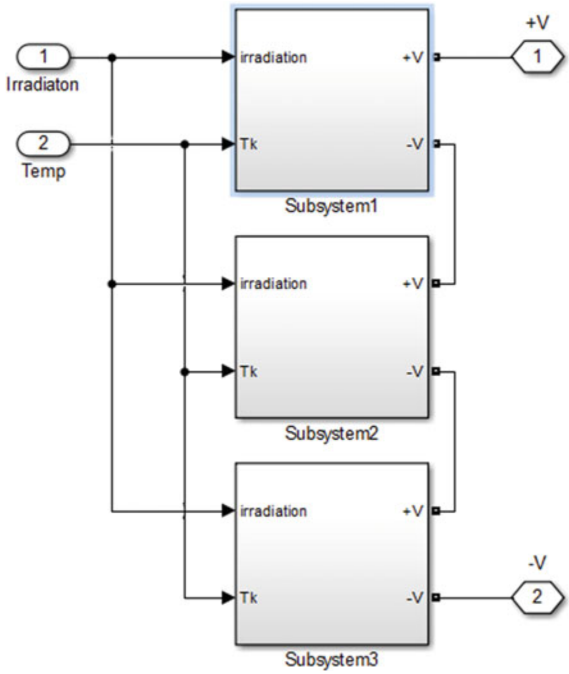


Fig. 12 I_{PV} block

Fig. 13 Series PV module



As discussed before, the embedded switched-inductor Z-source inverter operates at higher gain factor compared to its base topologies.

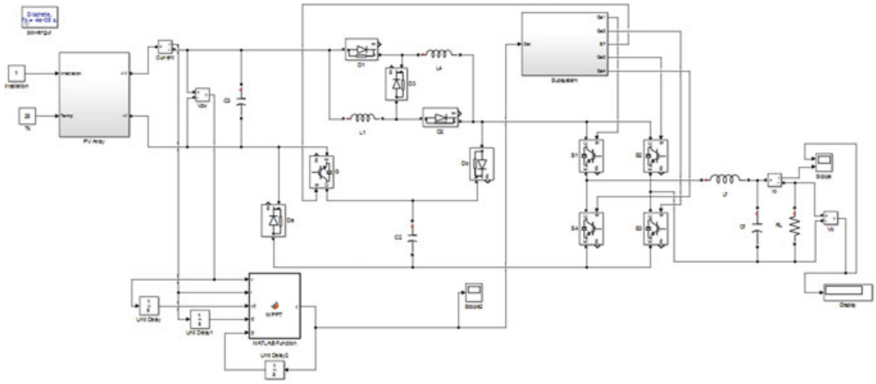


Fig. 14 Simulation circuit of ESI-ZSI with PV

Table 5 Simulation parameters

Components	ESI-ZSI
Input voltage (V_{in})	40–50 V
Switching frequency (f_s)	25 kHz
Inductors (L_1, L_2)	1.5 mH
Capacitor (C)	47 μF
Load (R)	55 Ω
Filter capacitor (C_f)	10 μF
Filter inductor (L_f)	1.2 mH

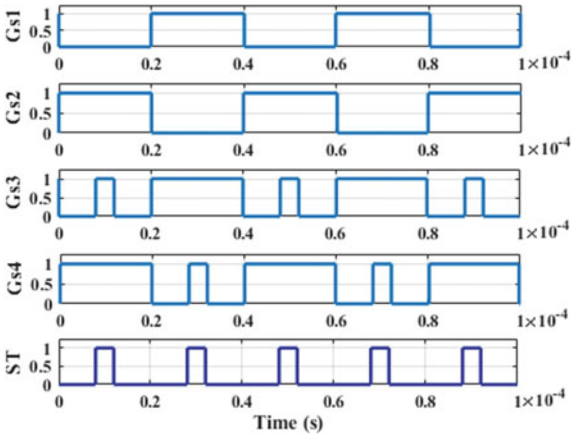


Fig. 15 Pulse for the switches

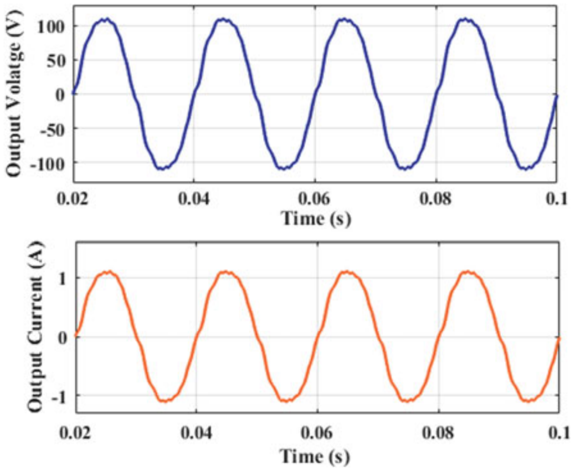


Fig. 16 Voltage and current waveform of ESI-ZSI

7 Inference

The basic parameters of ESI-ZS inverter were modelled with D_{st} as a common factor, and hence, D_{st} plays the main role in modelling an application-specific inverter circuit. Basic parameters were considered for comparison of the inverters among embedded switched-inductor ZSI, with embedded SBI and conventional ZSI which were made in terms of gain factor, current, and voltage ripple. From this comparison table, it is yielded that the designed symmetrical topology is found to be superior, providing a variable gain factor by varying D_{st} and with the number of SL cell connected. A suitable PV array was considered and designed for the verification of the simulation results. InC MPPT was also implemented with the PV array to provide the maximum power to the inverter. The results of the designed topology was simulated with a simple pulse-width modulated (PWM) generated pulses sourced from a PV array, and the results are provided. With this, the hardware verification of the topology will be carried out in future works.

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