A blue and white logo

Description automatically generated with medium confidence **San Francisco Bay University**

**EE577 Functional Verification with System Verilog**

**Homework #5**

**Due day: 8/6/2023**

**Instruction:**

1. **Push the answer sheets/source code to Github.**
2. **Please follow the code style rule like programs on handout.**
3. **Overdue homework submission cannot be accepted.**
4. **Takes academic honesty and integrity seriously (Zero Tolerance of Cheating & Plagiarism)**
5. Run the example verification programs in Counter and BitDiv1 & BitDiv2 folders, then show running results.

BitDiv1

*A screenshot of a computer program

Description automatically generated*

Design files window

A screenshot of a computer

Description automatically generated

Testbench window

A screenshot of a computer

Description automatically generated

Result

**BitDiv2**

A screenshot of a computer program

Description automatically generated

Design files window

A screenshot of a computer program

Description automatically generated

testbench window

A screenshot of a computer program

Description automatically generated

Result

**Arbiter**

**A screenshot of a computer program

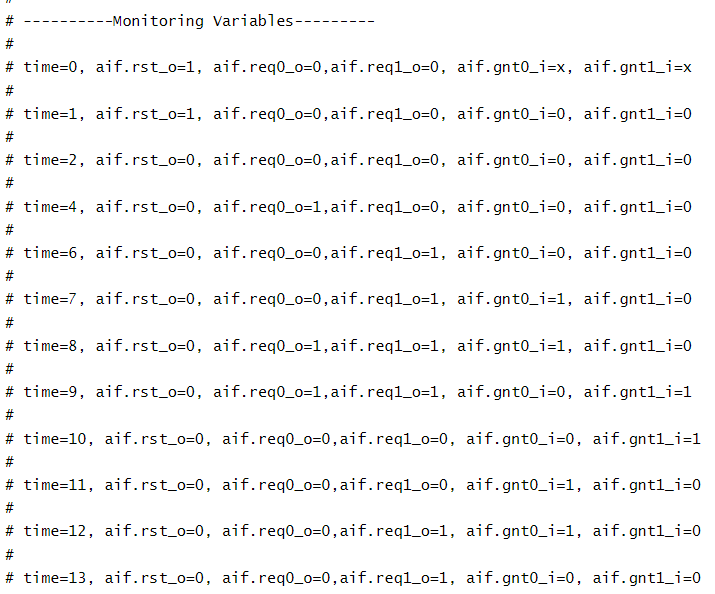
Description automatically generated**

Design window

A screenshot of a computer

Description automatically generated

testbench window



Result

**Counter**

A screen shot of a computer code

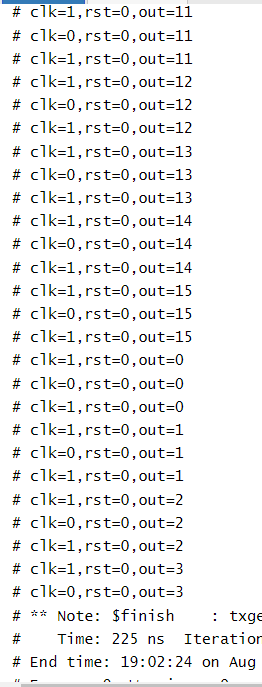
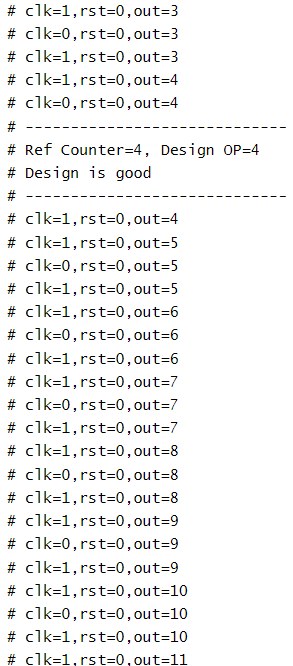
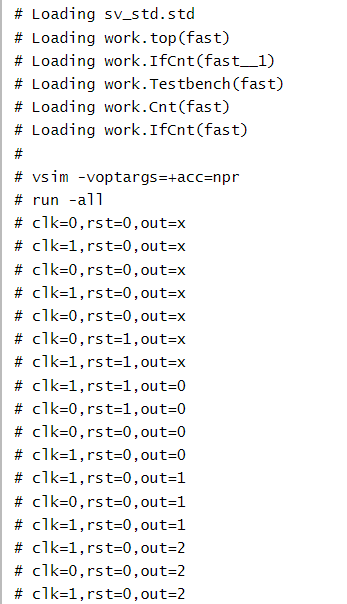
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Design window

A screenshot of a computer program

Description automatically generated

testbench window



Result