Assignment_6 Statistics
Memory Simulation with Cache
Computer Architecture Lab
CS311

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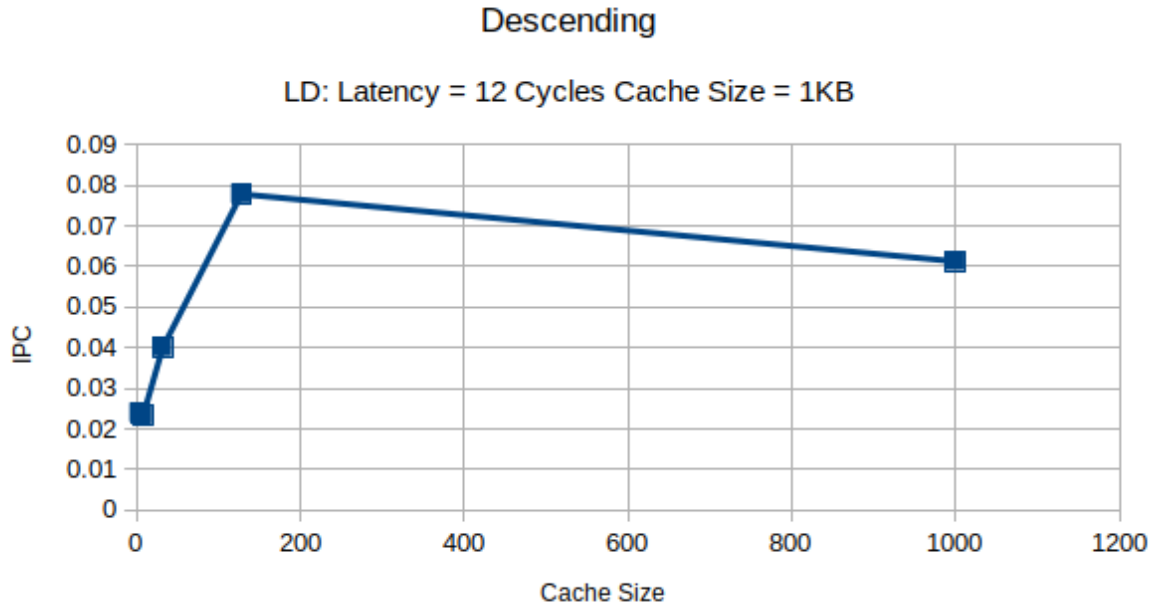
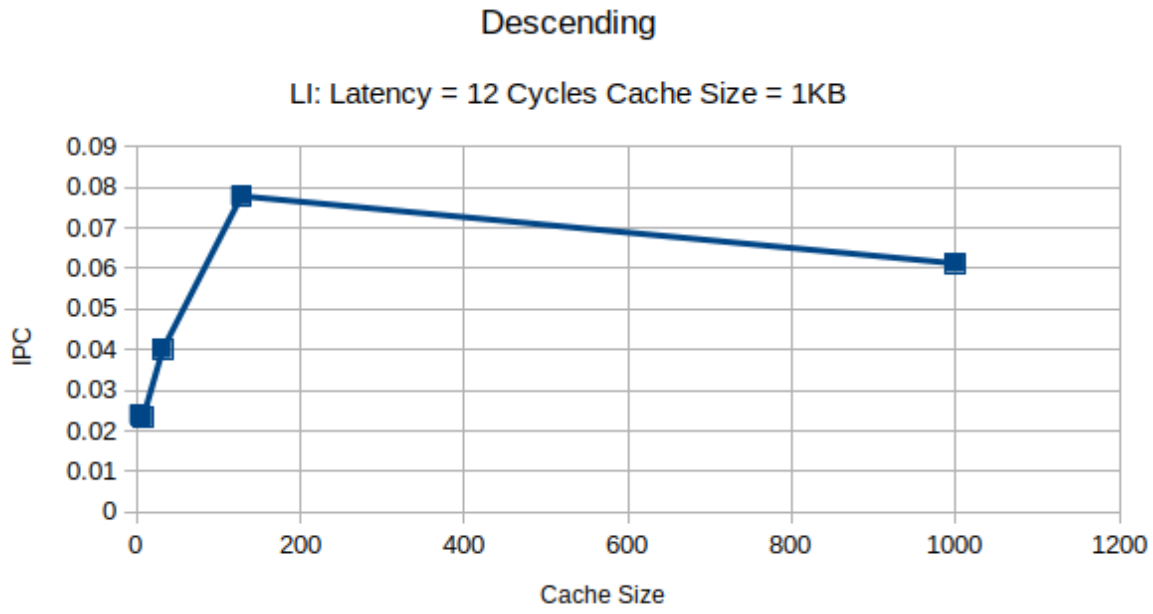
1 Problem Statement

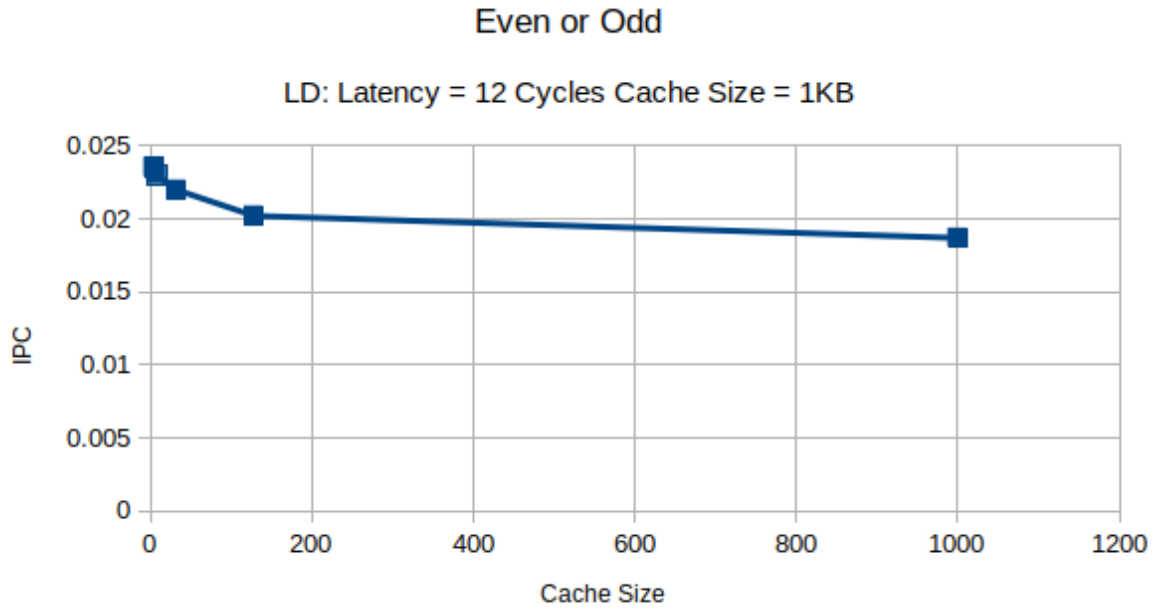
Add caches to the simulated memory system.

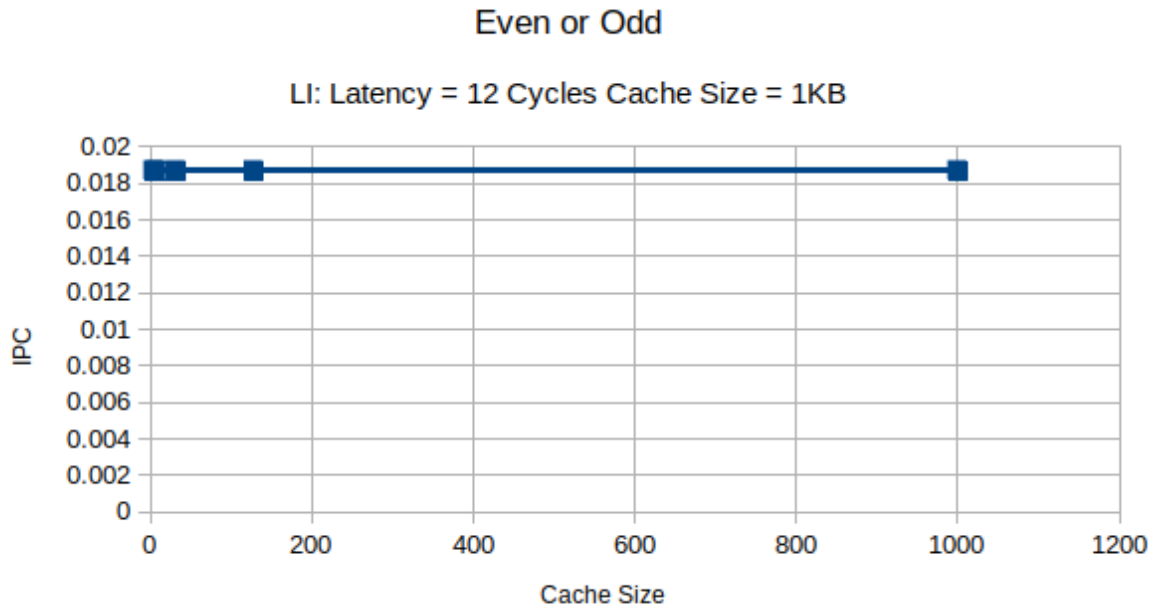
2 Statistics for files Submitted in Assignment 1

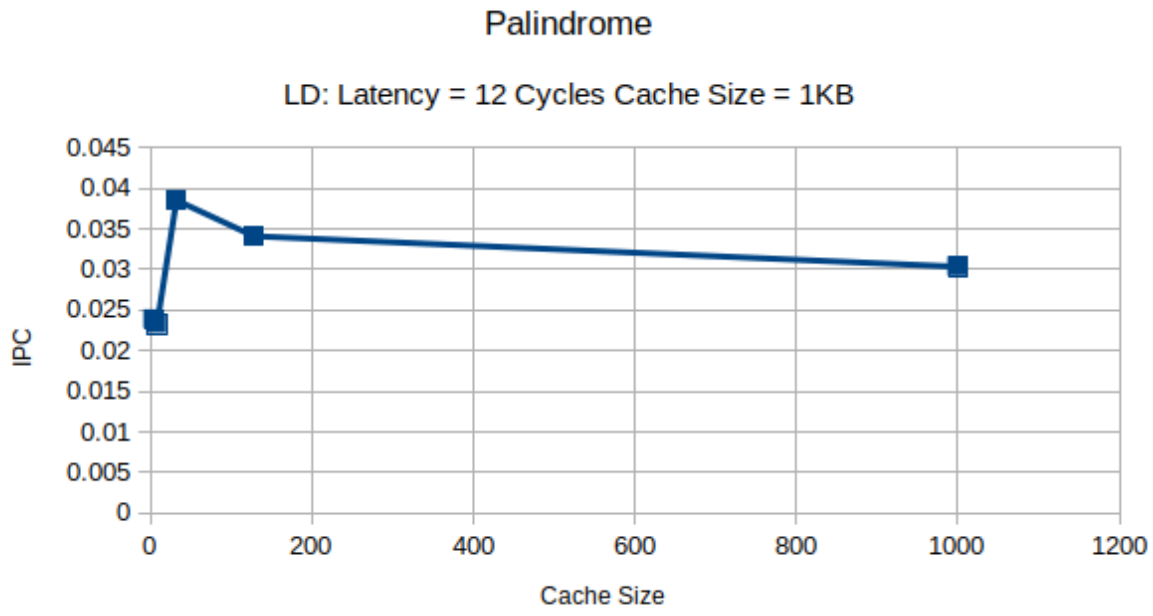
The graphs of IPC v/s Cache Size for different configurations of caches are pasted below.

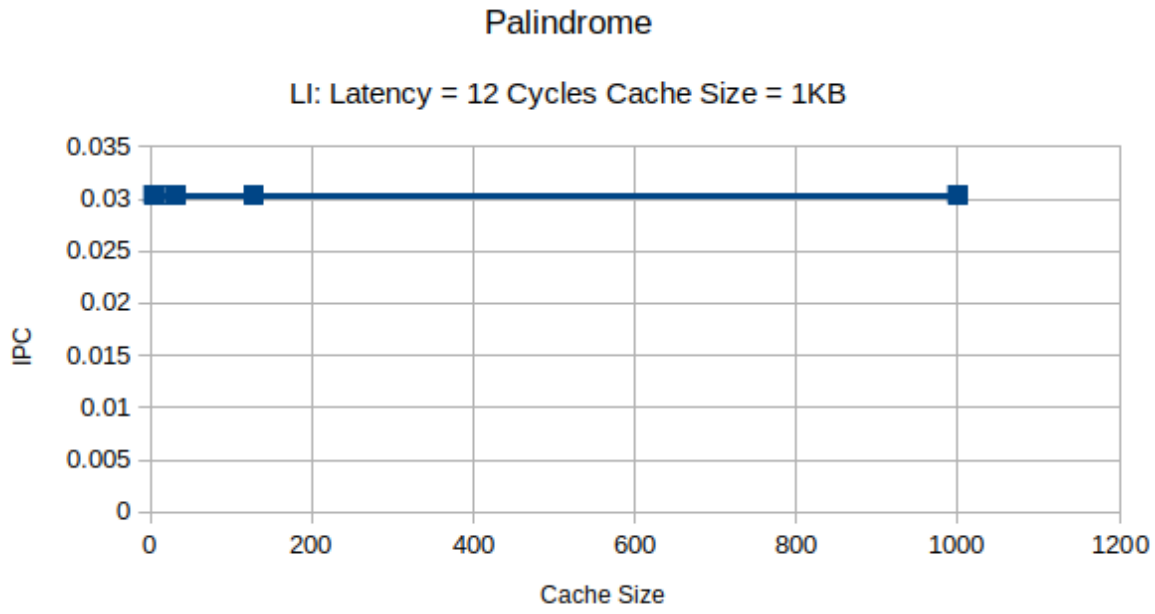


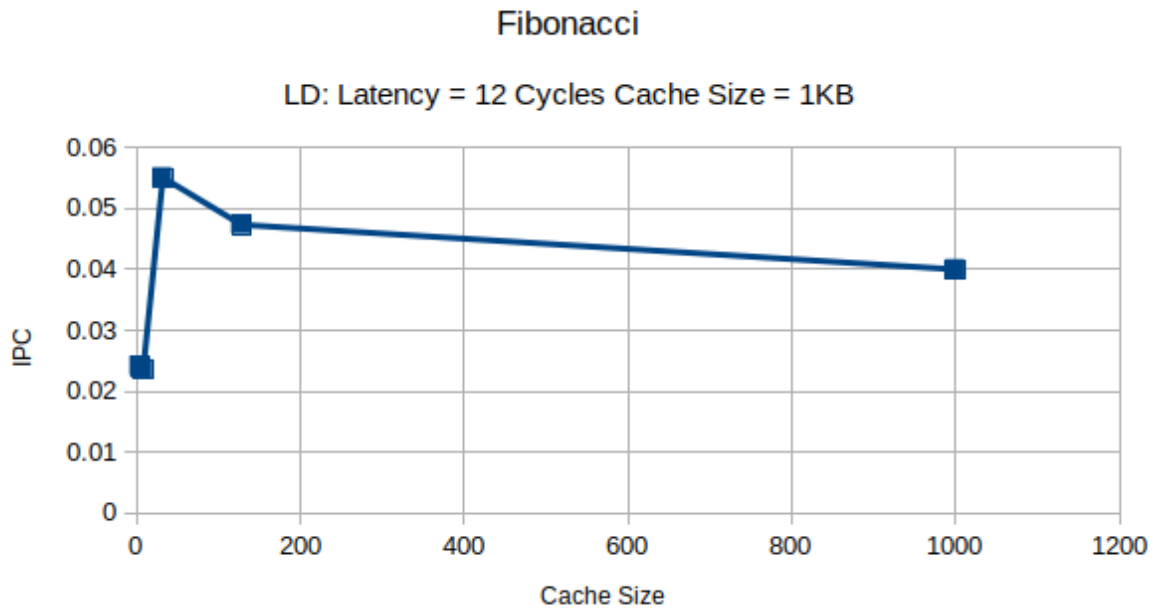

Descending
LI: Latency = 12 Cycles Cache Size = 1KB
IPC
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
200
400
600
800
1000
1200
Cache Size


Even or Odd
LD: Latency = 12 Cycles Cache Size = 1KB
IPC
0.025
0.02
0.015
0.01
0.005
0
0
200
400
600
800
1000
1200
Cache Size

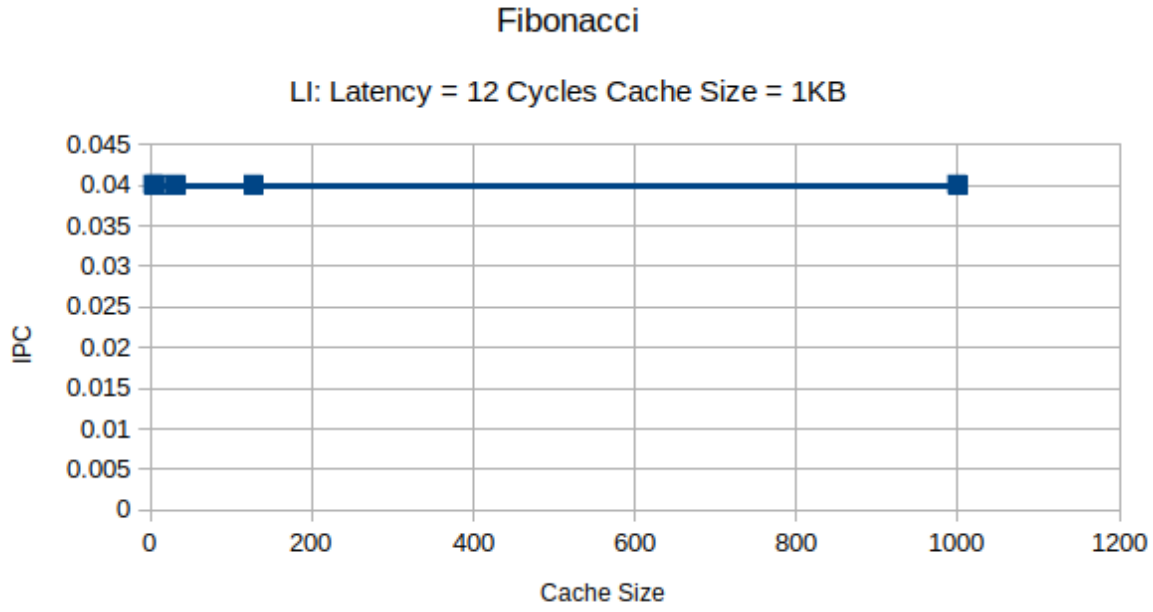

Even or Odd
LI: Latency = 12 Cycles Cache Size = 1KB
IPC
0.02
0.018
0.016
0.014
0.012
0.01
0.008
0.006
0.004
0.002
0
0
200
400
600
800
1000
1200
Cache Size


Palindrome
LD: Latency = 12 Cycles Cache Size = 1KB
IPC
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
0
200
400
600
800
1000
1200
Cache Size

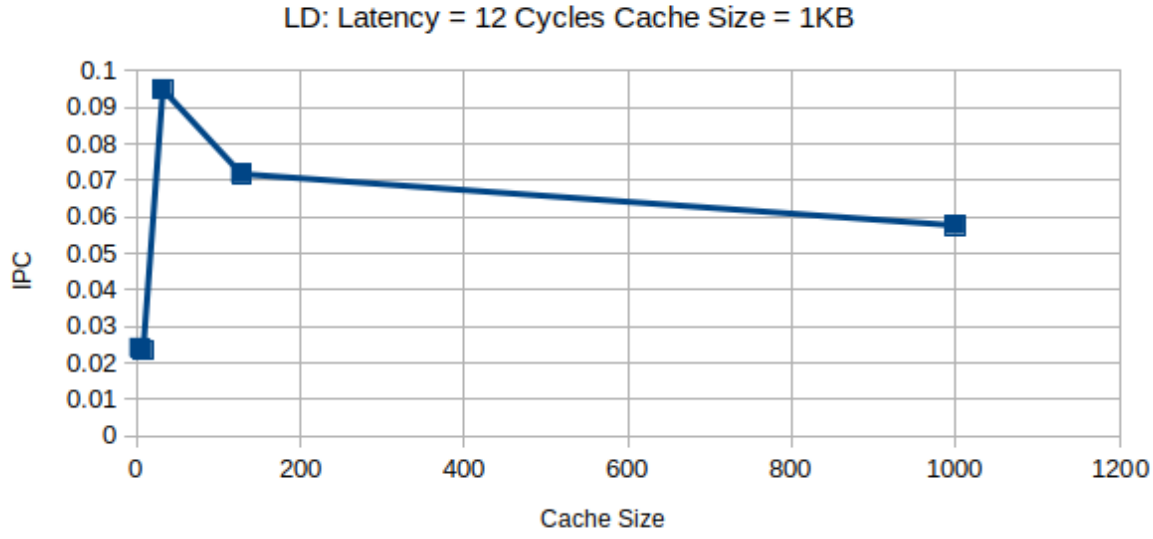

Palindrome
LI: Latency = 12 Cycles Cache Size = 1KB
IPC
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
0
200
400
600
800
1000
1200
Cache Size

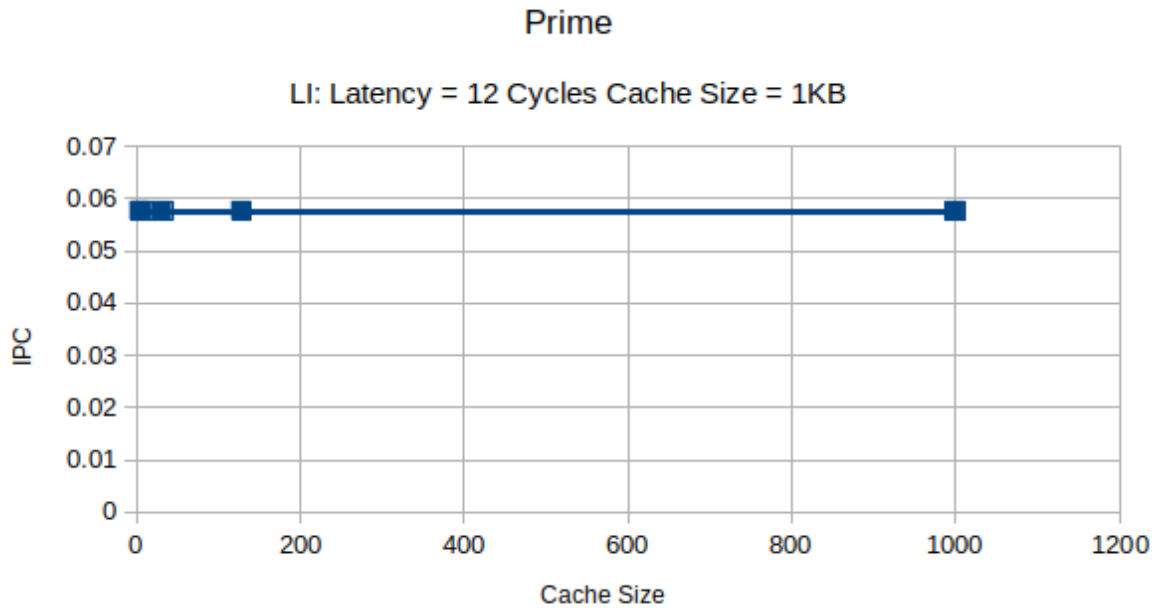

Fibonacci
LD: Latency = 12 Cycles Cache Size = 1KB
IPC
0.06
0.05
0.04
0.03
0.02
0.01
0
0
200
400
600
800
1000
1200
Cache Size

Fibonacci



Prime





2.1 Observation

The graphs plotted can be divided into two categories.

First: IPC increases (typically till 12 words) and then decreases. This type of graph is mostly seen for cases where cache for l1d is constant and we vary cache for l1i. The possible reason is because there are only the few instructions which are repeated in the loop again and again and hence these intructions are called directly from the cache after once called. IPC starts decreasing after few cycles because on increasing cache size latency is increasing while the hit rate is constant.

Second: IPC remains constant irrespective of the cache size. This type of graph is mostly seen for cases where cache for l1i is constant and we vary cache for l1d. This is because load and store operations are not repeated in entire program. Only for Decreasing program we can see the trend of first increasing and then decreasing because there are few repeating load and store operations.