

**Assignment\_3 Result**  
ToyRisc Simulator 1  
Computer Architecture Lab  
CS311  
Prof. Rajshekar K:

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Teammates: Devanshu Agarwal  
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Lab Date: 10/08/18  
Due Date: 04/09/18

## 1 Problem Statement

Develop a single cycle processor simulator for ToyRISC.

## 2 Statistics for files Submitted in Assignment 1

Program	Number of Instructions	Number of Cycles	Processor Speed
descending	250	1250	0.2
even-out	6	30	0.2
fibonacci	67	335	0.2
palindrome	22	110	0.2
prime	100	500	0.2