Assignment_4 Statistics **16002018, 160010006**
5-stage pipeline Teammates:Devanshu Agarwal
Computer Architecture Lab Lokesh Kumar
CS311 Lab Date: 31/08/18
Prof. Rajshekar K: Due Date: 14/09/18

1 Problem Statement

Upgrade the simulator to a pipelined core model.

2 Statistics for files Submitted in Assignment 1

The statistics for the single cycle processor are given in Table 1 and for the pipeline processor with data and control interlocks are given in Table 2

Table 1: Statistics for Single Cycle Processor

Program	Number of Instructions	Number of Cycles	Processor Speed
descending	250	1250	0.2
even-out	6	30	0.2
fibonacci	67	335	0.2
palindrome	22	110	0.2
prime	100	500	0.2

Table 2: Statistics for Pipeline Processor

Program	Number of Cycles	Number of OF Stage Stall	Number of times instruction on wrong branch
descending	560	203	51
even-out	22	9	1
fibonacci	148	60	8
palindrome	48	14	5
prime	24	7	1

On comparing these two tables we can clearly see that the number of cycles for the pipeline processor are lesser then the single cycle processor. Further we can see that as the ratio of number of instructions and number of of stage stall increases the number of cycles decreases drastically for the pipeline processors and same holds for the ratio of number of instructions with number of times wrong instruction entered the branch.