Assignment_5 Statistics **16002018, 160010006**
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CS311 Lab Date: 28/9/18
Prof. Rajshekar K: Due Date: 12/10/18

1 Problem Statement

Upgraade the simulator to Discrete Event Simulator.

2 Statistics for files Submitted in Assignment 1

The statistics for discrete event simulator is given in Table 1

Table 1: Statistics for assignment 5

Program	Number of Cycles Taken	Number of Dynamic Instructions	Instructions Per Cycle
Descending	10271	250	0.02434
Even or Odd	249	6	0.02409
Fibonacci	2710	67	0.02473
Prime	4054	100	0.02466
Palindrome	901	22	0.02441

The comparison of number of cycles taken for single cycle processor, pipeline processor, pipeline processor with latencies is given is Table 2.

Table 2: Comparision between all three models

Program	Single Cycle Processor	Pipeline Processor	Pipeline Processor with Latencies
Descending	1250	560	10271
Even or Odd	30	22	249
Fibonacci	335	148	2710
Prime	500	24	4054
Palindrome	110	48	901

The comparison shows us that on modelling latencies the number of cycles increases many folds from that of single cycle processor and simple pipeline processor.
Cycles in programs like descending and fibonacci increases ten fold becuase of many load and store operations respectively. Cycles in prime number also increases ten folds as compared to previous statistics, possible reason can be because of many division operations in the program. Instructions per cycle for all the instructions are coming almost same because of high latencies. Main memory latency is 40. Because of this high latency almost every instruction got executed by every stage before instruction fetch could fetch the next instruction from main memory.