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Introduction

The final report, the ELE 404 Amplifier Design Project, is presented on this document. Calculations for components were done manually and then the design was made accordingly. The design was made using MultiSim, it was also used to test the circuit and check requirements. The calculations and assumptions that were made are in the appendix.

Objectives

The objective of this design project was to design, analyze, simulate, and test a single-supply, multistage, inverting or non-inverting, transistor amplifier with a set of requirements. The requirements are as followed:

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: no larger than $\mathbf{10}\ \boldsymbol{mA}$;
- No-load voltage gain (at 1 kHz): $|\boldsymbol{Avo}| = \mathbf{50}$ ($\pm\ \mathbf{10}\%$);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with RL = 1 $k\Omega$): no smaller than $\mathbf{90}\%$ of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 $k\Omega$): no smaller than 4 V peak
- to peak;
- Input resistance (at 1 kHz): no smaller than $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz ($-\mathbf{3}\boldsymbol{dB}$ response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than $\mathbf{220}\ \boldsymbol{k\Omega}$ from the E24 series;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit

Circuit Under Test

The Circuit below was designed for the project.

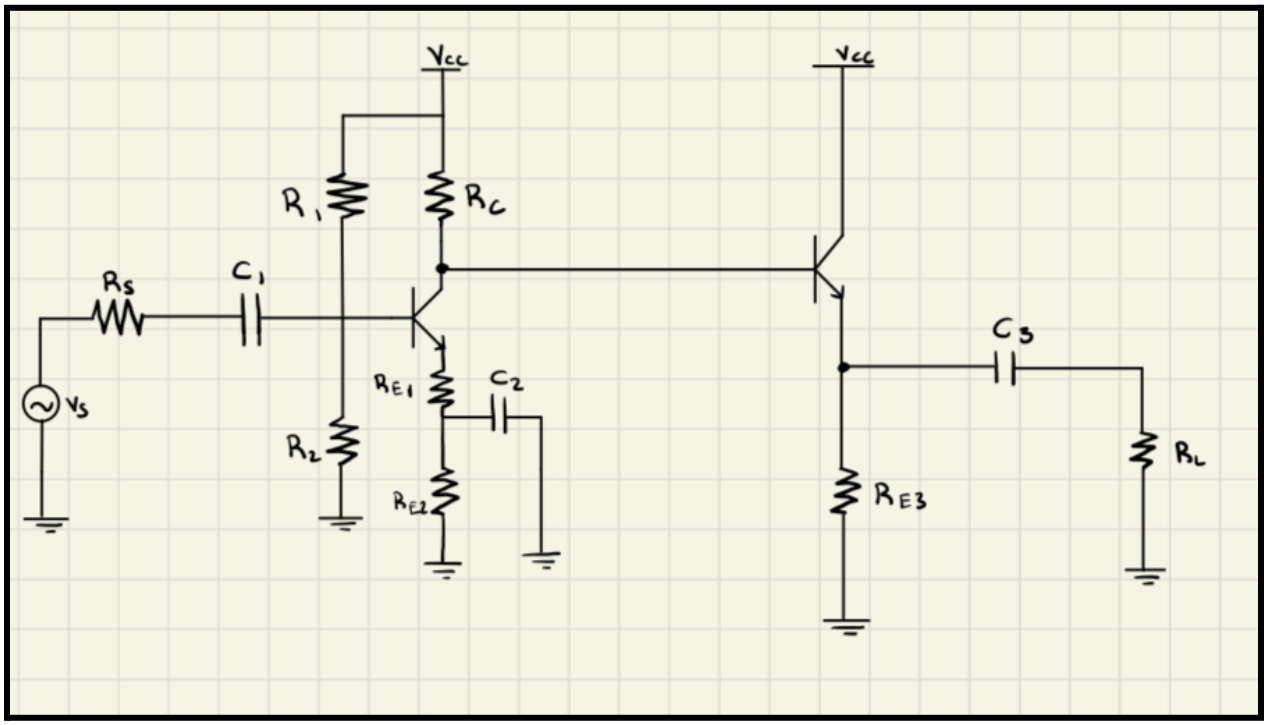


Figure 1. Hand drawn design of circuit which models a two-stage amplifier

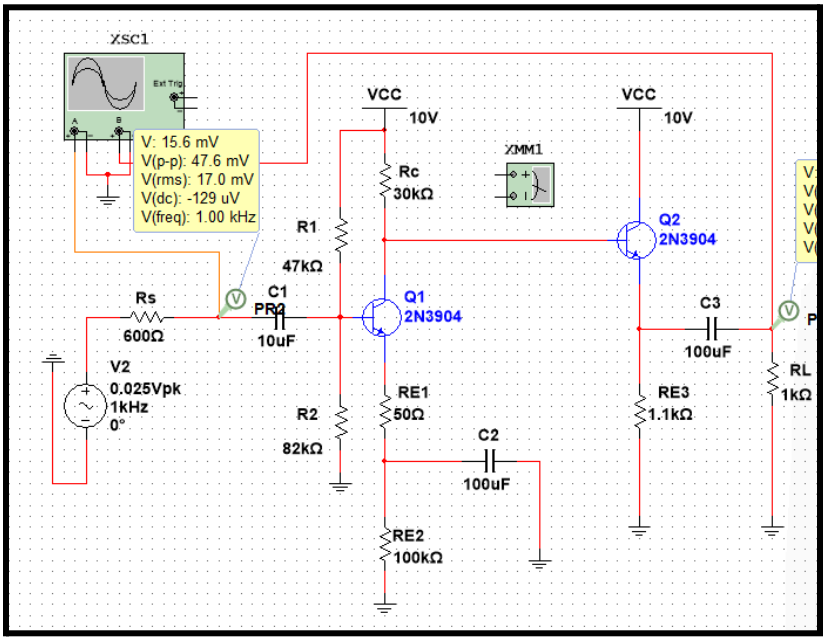


Figure 2. Two-Stage amplifier circuit designed in MultiSim

Circuit Description

A 2-stage amplifier was selected in order to meet the requirement of the project. This included having a gain of 50 while maintaining $R_{in} \geq 20k\Omega$. This design includes a CE (common emitter) stage and a CC (common collector) stage. I first set the first stage gain to be 50 and the final stage gain to be 1. When you multiply the two stages it will lead to having an overall gain of 50. I first started my calculations by making an assumption for R_C. This assumption was 30kΩ. Then I found an IC which helped in getting a value for g_m which was 1.73mS. I then used g_m to find R_{E1} which ended up being 21.97Ω. After that I used a simple equation of $R_{E1} + R_{E2}$ to find out what it was. That value became 85.5kΩ. Then I subtracted 85.5kΩ with 21.97Ω to find out what R_{E2} is which became 85.5kΩ. Then I used the R_i requirements to solve for R1 and R2. These following resistor values ended up being 46.13kΩ and 82.37Ω respectively. These values for resistors differ on the actual MultiSim design as they were rounded to the nearest expected value that was given as a requirement. The capacitors on the circuit allows AC signals to pass through but blocks off any DC signals. Through all these calculations and designs the requirements were met on the final design.

Experimental Results

C1	C2	C3
10μF	100μF	100μF

Table 1. Capacitor Values

R1	R2
$47k\Omega$	$82k\Omega$

Table 2. Resistor Values

RE1	RE2	RE3	RC
50Ω	$100k\Omega$	$1.1k\Omega$	$30k\Omega$

Table 3. Emitter and Collector Resistor Values

I_c	β	V_{cc}	g_m
0.0667 mA	150	10 V	1.73mS

Table 4. Useful Values from Stage 1

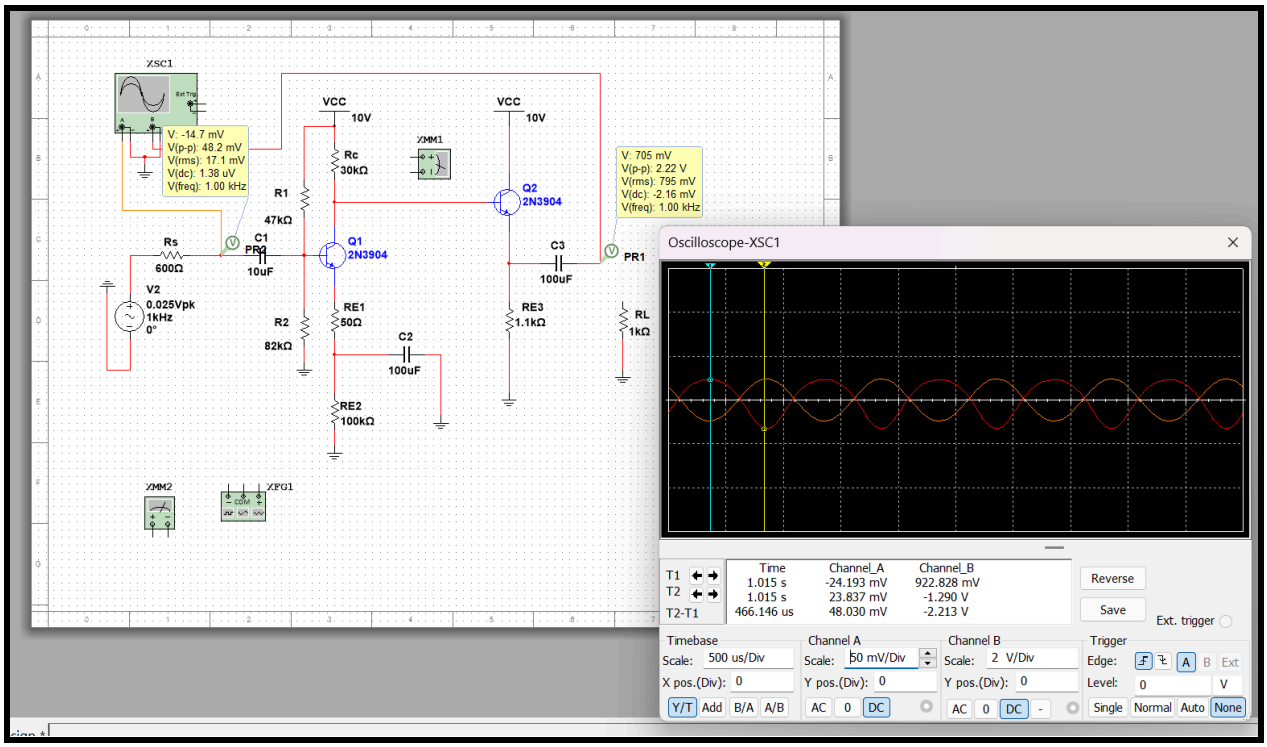


Figure E1. MultiSim and waveform of input and output voltages ($R_L = \infty$)

$V_{I,p\text{-}p}$ (mV)	$V_{o,p\text{-}p}$ (V)	A_{vo} (V/V)
48.030	2.213	46.075

Table E1. V_I, V_o, A_V (no load voltage gain)

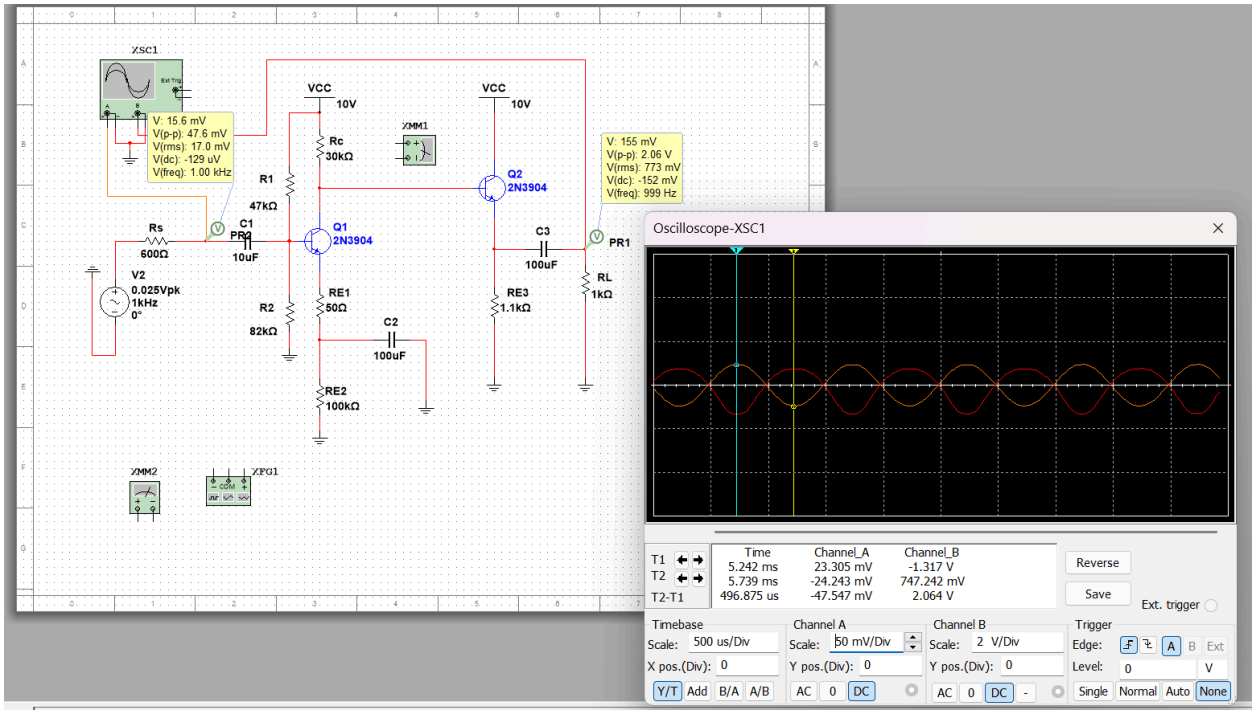


Figure E2. MultiSim and waveform of input and output voltages (R_L = 1kΩ)

$V_{I,p\text{-}p}$ (mV)	$V_{o,p\text{-}p}$ (V)	A_{vo} (V/V)
47.547	2.064	43.410

Table E2. V_I, V_o, A_V (with load voltage gain)

$$Input\ Resistance = R1//R2//Ri = \frac{1}{\frac{1}{47}+\frac{1}{82}+\frac{1}{61.8}} \approx 20.14k\Omega > 20k\Omega$$

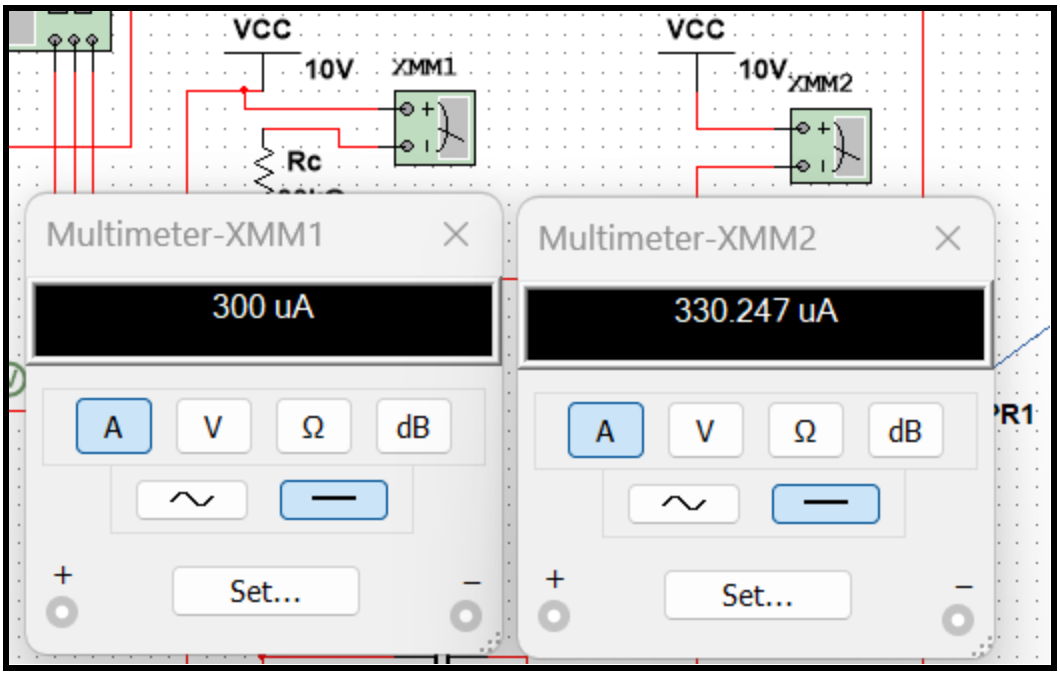


Figure 3. MultiSim simulation shows the Quiescent Current < 10mA

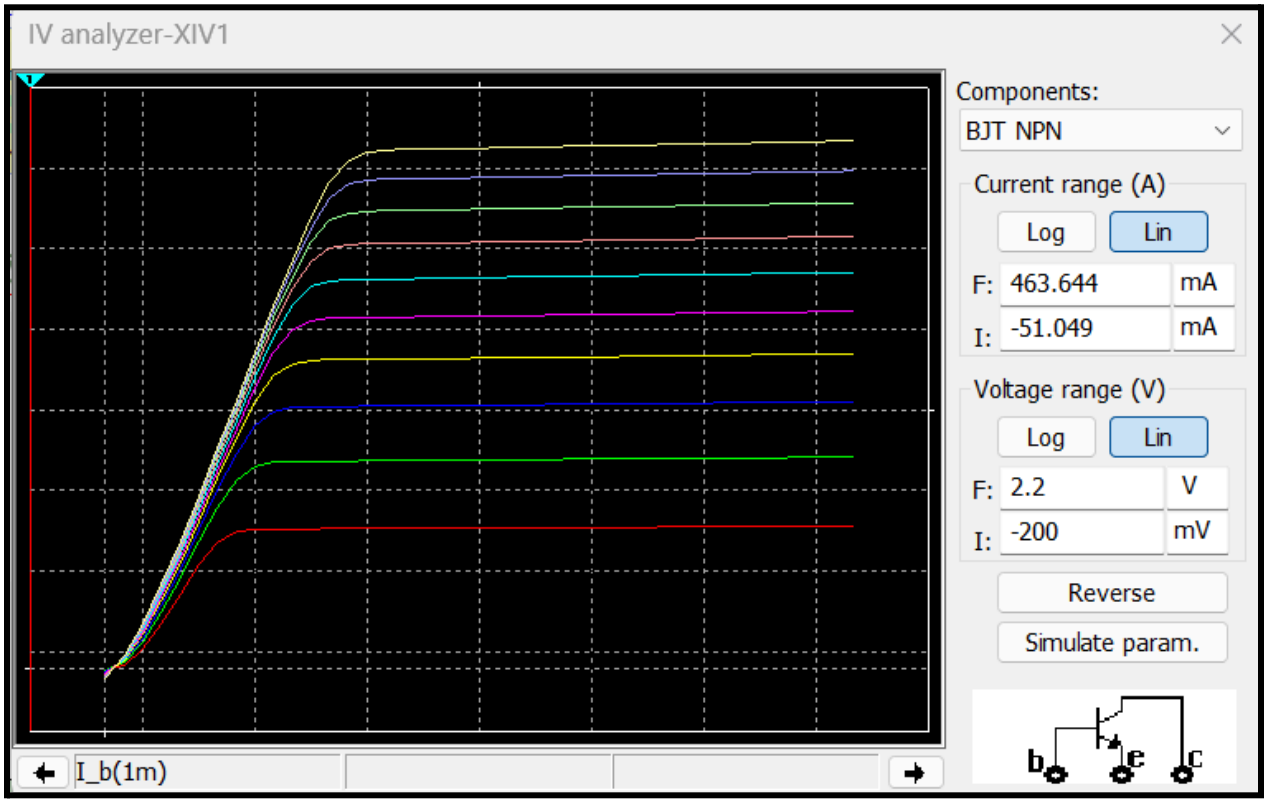


Figure 4. Transistor 1 characteristics graph (CE Amplifier)

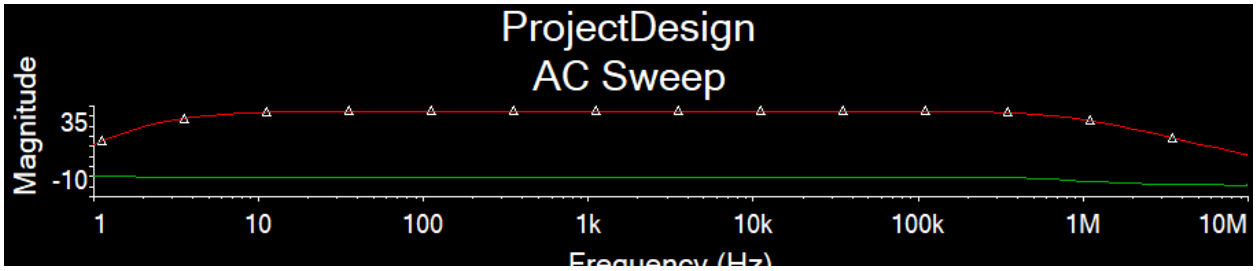


Figure 5. Frequency Response Graph

Conclusion

Overall the design project was conducted well and majority of the specifications were achieved. The design was a CE-CC amplifier and the gain was within the range. The frequency response graph is seen above. The resistors and capacitors that are used have been selected from the requirements. Overall the project design was a success.

Appendix

Assumptions $= \frac{1}{2}(V_{cc} + V_E + 0.3) \Rightarrow V_C = 6.2V$

- $\beta = 150$
- $R_o = 30k\Omega$
- For biasing current stability Set V_E to $3V_{BE}$

  $V_E = (3)(0.7) = 2.1V$
- For a good output voltage swing & and to ensure BJT does not enter saturation mode we do the following:

  $V_C = \frac{1}{2}(V_{cc} + V_E + 0.3V)$

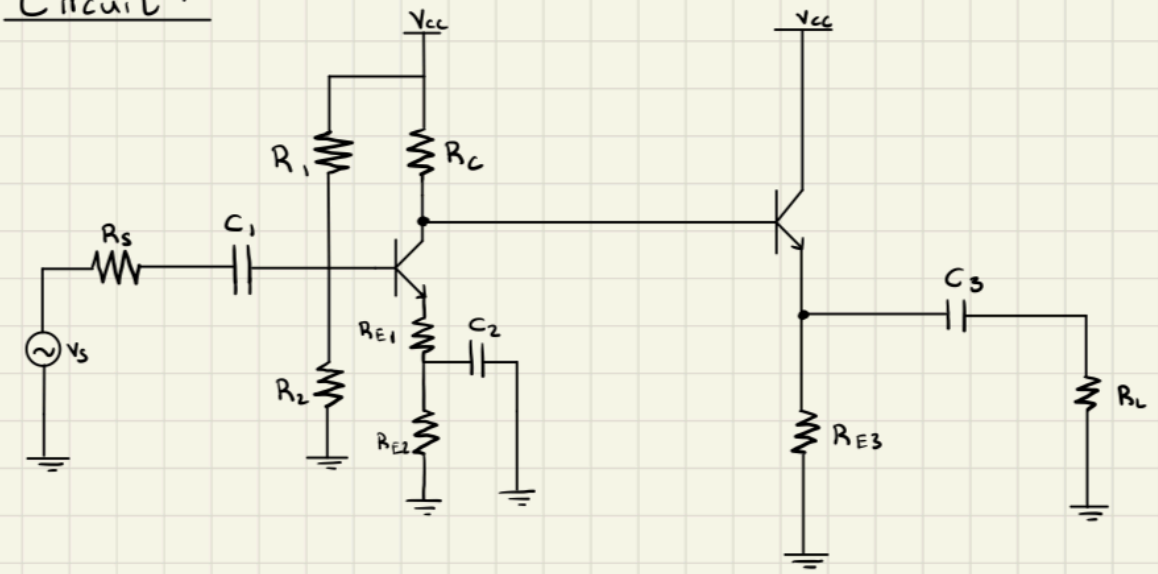
  $8 = \frac{1}{2}(10 + V_E + 0.3V)$

  $16 = 10.3 + V_E$

  $V_E = 5.7V$

- For CE amp, $R_o = R_c$: $R_c = 30k\Omega$

Circuit:



Calculations

Determining g_m

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$I_C = \frac{10V - 8V}{30k\Omega} \Rightarrow I_C \approx I_E \Rightarrow I_E = 0.0667mA$$

$$I_C = 6.67 \times 10^{-5} A$$

$$I_C = 0.0667 mA$$

$$g_m = 26(0.667)$$

$$g_m = 1.73_m S$$

Known that $I_E = 0.0667_{mA}$ and $V_E = 5.7V$

$$R_{E1} + R_{E2} = \frac{V_E}{I_E} = \frac{5.7V}{6.67 \times 10^{-5} A} = 85.51k\Omega$$

$$R_{E1} + R_{E2} = 85.5k\Omega$$

Using gain requirment

$$|A_{V0}| = \left| \frac{-g_m R_C}{1 + g_m R_{E1}} \right| = 50$$

$$50 = \frac{(1.73\ mS)(30k\Omega)}{1 + (1.73\ mS)R_{E1}}$$

$$50(1 + (1.73mS)R_{E1} = (1.73\ mS)(30k\Omega)$$

$$1 + (1.73\ mS)R_{E1} = \frac{(1.73\ mS)(30k\Omega)}{50}$$

$$(1.73mS)R_{E1} = \frac{(1.73\ mS)(30k\Omega)}{50} - 1$$

$$R_{E1} = \frac{(30k\Omega)}{50} - \frac{1}{1.73 \times 10^{-3} S}$$

$$R_{E1} = 21.97\Omega$$

From $R_{E1} + R_{E2}$

$$R_{E2} = 85.5k\Omega - 21.97$$

$$R_{E2} = 85.5k\Omega$$

Use R_i requirement to find R_1 and R_2

$$R_i \geq 20k\Omega$$

$$(R_1 // R_2 // R_i') \geq 20k\Omega$$

$$\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_i'} \geq \frac{1}{20}$$

$$R_1 // R_2 \geq \left(\frac{1}{20} - \frac{1}{61.8}\right)^{-1}$$

$$R_1 // R_2 \geq 29.57\ k\Omega$$

$$R_1 // R_2 = 29.57\ k\Omega$$

$$\frac{R_1 \cdot R_2}{R_1 + R_2} = 29.57 \quad (1)$$

$$r_e = \frac{26}{0.0667} = 389.81\Omega$$

$$R_i' = \beta(r_e + R_{E1}) = 150(389.81 + 21.97) = 61761\Omega = 61.81k\Omega$$

$$V_B = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$6.4 = 10 \cdot \frac{R_2}{R_1 + R_2}$$

$$(2) \quad \frac{R_1 + R_2}{R_2} = 1.56$$

Solve ① and ②

① $\frac{R_1 \cdot R_2}{R_1 + R_2} = 29.57$ ② $\frac{R_1 + R_2}{R_2} = 1.56$

$\frac{R_1}{R_2} + 1 = 1.56$

$\frac{R_1}{R_2} = 1.56 - 1$

$R_1 = (0.56) R_2$

② Sub into ①

$\frac{(0.56)R_2 \cdot R_2}{(0.56)R_2 + R_2} = 29.57$

$\frac{0.56 R_2^2}{0.56 R_2 + R_2} = 29.57$

$\frac{0.56 R_2^2}{(0.56+1) R_2} = 29.57$

$\frac{0.56 R_2}{1.56} = 29.57$

$R_2 = 82.37 \text{ k}\Omega$

Sub R_2 into ②

$\frac{R_1 + 70.12}{70.12} = 1.56$

$R_1 + 82.37 = (1.56)(82.37)$

$R_1 = 128.50 - 82.37$

$R_1 = 46.13 \text{ k}\Omega$