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DHARMSINH DESAI UNIVERSITY, NADIAD

FUCULTY OF Technology

ONLINE SESSIONAL EXAMINATION

B. Tech (CE) Sem 5th

SUBJECT: MICROPROCESSOR FUNDAMENTAL

& PROCERAMMINCE

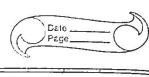
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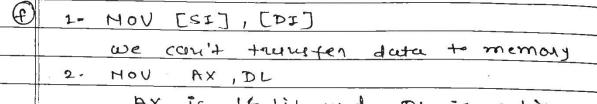


3.1 HOW does some compute 20 bit Physical (a) addness ? 20 bit is calculated by segment and offset cicleness. PA = segment address x 10H + offset @ myseimum size of extres segment is Possible 21c = 65,535 bytes (64 Kb) because offset size is 16 bit. Thenefore the more size is 216 memory location minimum size of segment is 16 because minimum value of segment is 16 memony location (c) - add sess is specified by cpy and can only be directed from the CPU towards other devices and not the nevence. The duty bus is meaut for the trunsfer of dute. In mn moc pin is high mn this mn used in single Process system To demultiple seing The Pin no=30 ot 8085 is used it is called ALE pin (Address Latch enuble).





(F) AAD is used to convert ASCII value to . P unpacked BCD value. The AAD is only useful when it precedes a DIV Instruction that divides the adjusted value in Ax Register **(£)** 1- MOV [SI], [DI]

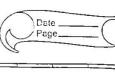


Ax is 16 bit und DL is & bit so the openund size is not mutch.



Parogrummuble periphenal interface (PPI) (c) Ic - 82BS - It is used to munage autometically hundshake operation It can be programmed to a sieceive an signal from a phesipheral and also send an int signal and send the ACK signal buck to PheniPhenal at proper time. IC-8255's Pumpose is priogrammable Ilo device which may be used with micolopholessons. - These use 24 Ilo pins which may be judividually programmed in 9 different groups of 12. 8255 is high pentonmable and industry standard configuration that's why it is compatible with 8086____ It is used in 3 mujors modes of openation. 8255 can be configured in two modes = 1. BSR mode (Bit set Reset) 2. Ilo Modes In Ito mode three modes available. Mode 01 Mode 1, Mode 2 -





- Modes are configured by control was - BSR (Bit set Reset) Mode: If bit 7 of control word is a logic then 8255 will be configured us BSR mode. In this mode we can set on Reset the Pius. D7 D6 D5 D4 D2 D1 DO D3 SIR × BI+ select X × 6 set -1 BSR Sc+ = 0 Reset -C mode Bit 0 Bit 1 Bitz Bit3 Bit 4 Bit 5 Bita Bit I

There are mainly 3 working modes. Hode 0 - Basic Ilo

Mode 1 - strobed Ilo Mode 2 - bidinectional Ilo





There is 3 Part A, Part B and Part c

Posit Mode 0 Hode 1 Mode 2

A V V X

Basic Ilo: will control signal from

Lit and sies:

hasal shak (strobed) Ilo: It will ack up

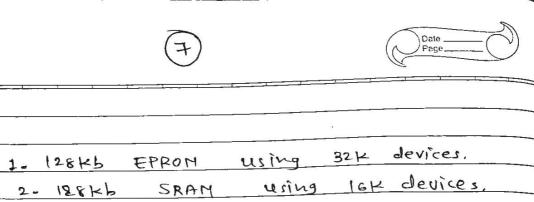
and 8285 that it is possible to transfer

data so some data will not be lost.

bidinectional Ilo: It is same as strobed

Ilo but It will work on both in

and out bidinectional



2- 128Kb SRAM using IGK devices. In EPROIY grequised size is 128kb and chip size is 3212b so, the nequined chips $n_1 = 128 = 4$ chips. 032 · Number of sets, 4 = 4 = 2 no of bunks

· size of set = 2 * 32 = 64 Kb

Se+ 2

set 1

(b)

for EPROM

7 F0000h

> E0000h

so, we can said the ending address

is stants from FFFFFh.

Stanting

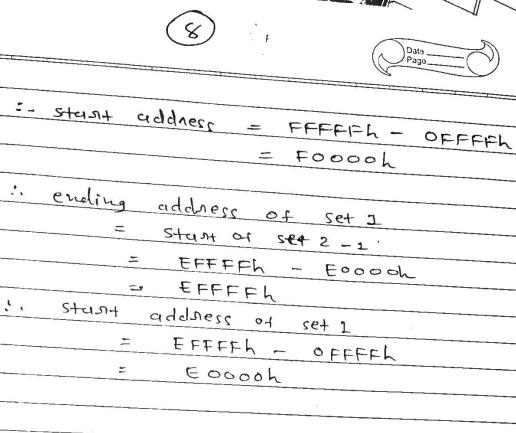
address

Ending

addrea

EFFFFh

FFFFFh

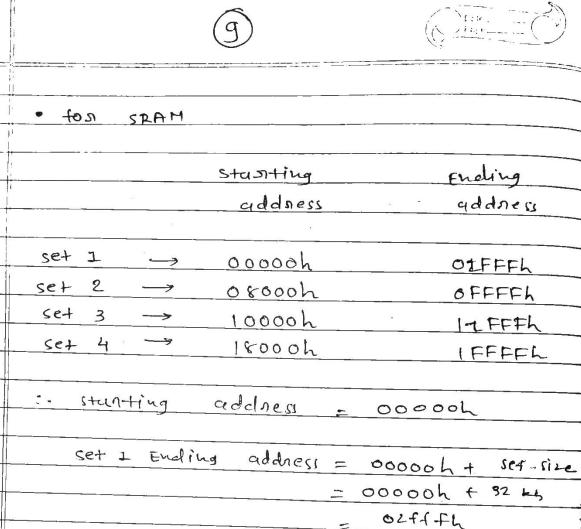


In SRAM prequired size is 128 Kb

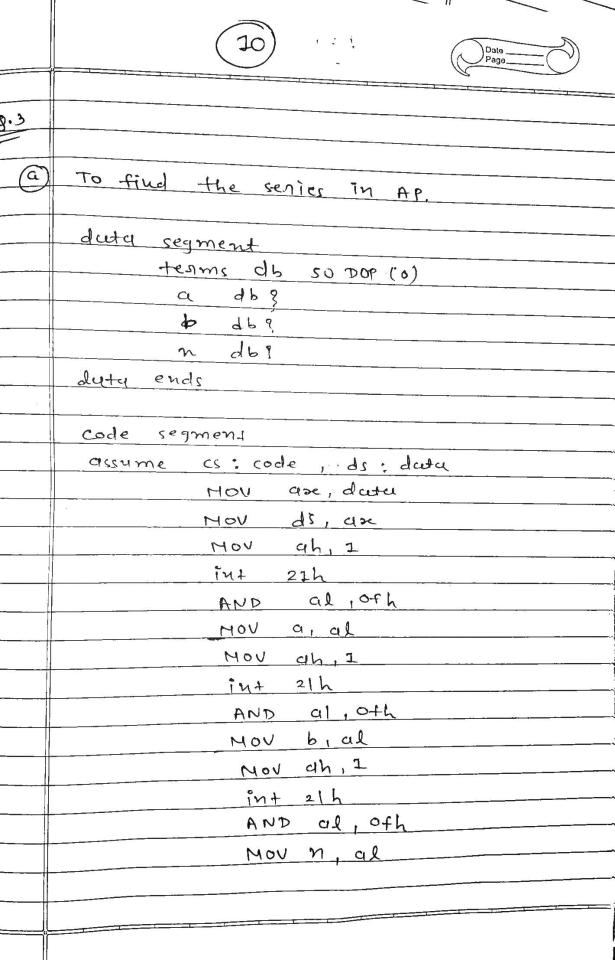
and chip size is lok. :- The required chips m2 = 128 = 8

-- Number of sets = 8 = 4 no. of banks

:. size of sets, = 2 * 16___ = 6' 32 Kb



= 00000h + 32 kg = 02f1fh



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lea sI, terms	
MOU [SI], a	
MOV cl, ozh	
Continue: Mov al, cl dec al MUL b add al, cl MOV [SI], al inc SI cmp n, cl; Inz continue	
int ogh code ends	
end.	
X — END OF ANSWER	SHEFTX