

# Optimize RISCV32I Design Using OpenROAD Project

**Objective:** Optimize the riscv32i design for Power, Performance (i.e. frequency), or design area using openRoad tool suites using 7 nm library.

Design link: <https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts/tree/master/flow/designs/src/riscv32i>

## Introduction:

An outline of steps used to build a chip using OpenROAD is shown below:

- Initialize floorplan - define the chip size and cell rows
- Place pins (for designs without pads )
- Place macro cells (RAMs, embedded macros)
- Insert substrate tap cells.
- Insert power distribution network.
- Macro Placement of macro cells
- Global placement of standard cells
- Repair max slew, max capacitance, and max fanout violations and long wires
- Clock tree synthesis
- Optimize setup/hold timing.
- Insert fill cells.
- Global routing (route guides for detailed routing)
- Antenna repair
- Detailed routing
- Parasitic extraction
- Static timing analysis
- OpenROAD uses the OpenDB database and OpenSTA for static timing analysis.

## Design Information:

<b>Design name</b>	Simple RISCV 32I core
<b>Top module</b>	riscv_top
<b>Constraint information:</b>	clk_period 1600
<b>Config.mk file information</b>	<pre>export DESIGN_NICKNAME = riscv32i export DESIGN_NAME = riscv_top export PLATFORM = asap7</pre>

### **How I started OpenROAD project:**

1. Ran make for all targets written in Makefile from Netlist to GDS using make command.
2. Steps followed to run make for all targets in make file:
  - a. Design set: DESIGN\_CONFIG=../designs/asap7/riscv32i/config.mk
  - b. cd OpenROAD-flow-scripts/flow/
  - c. make
  - d. observed logs, and results directories
  - e. opened to view floorplan using make gui\_floorplan.
  - f. opened to view placement using make gui\_place.
  - g. opened to view cts using make gui\_cts
  - h. opened to view routing using make gui\_route.
  - i. opened to view final design using make gui\_final
  - j. Observed parameters in final and 6\_report.log file (internal power, switching power, total power, report\_design\_area, critical path slack).
3. Steps to optimize the design are following:
  - a. cd design/asap/riscv32i/
  - b. modified parameters like clk\_period in constraint.sdc.
  - c. modified parameters like core area and die area, core utilization, export arguments for synthesis, floorplan, placement, routing, and CTS steps.
  - d. Observed the updated log files in logs directory and compare parameter with old logs.

**Also, you will find a summary of my holistic understanding after the conclusion of experiments of page #37**

\*\*\*\*\* Different scenarios\*\*\*\*\*

Total number of experiments performed = 25

Total number of good working experiments = 19

Total number of failed experiments = 6

I have fully documented total number of good/working experiments and total number of failed experiments at the end of this document to make it easy.

**For easy experiments reference you will find the 2 set of tables on page #40 (second last page)**

## Experiment #1

No change in OpenROAD files: ran make without any changes clk\_period 1600

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.00e-03    5.29e-05    1.92e-07    1.06e-03    11.4%
Combinational   7.05e-03    6.95e-04    5.17e-04    8.26e-03    88.6%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          8.05e-03    7.48e-04    5.17e-04    9.32e-03    100.0%
               86.4%        8.0%        5.5%
=====

```

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-----
6.5733
-----
finish slack div critical path delay
-----
0.386089
=====
```

**Design Area Report**

```
=====
finish report_design_area
-----
Design area 2503 u^2 23% utilization.
=====
```

## Experiment #2

Changed clk\_period 1300

Power Report in 6\_report.log:

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.24e-03    6.51e-05    1.92e-07    1.30e-03    11.5%
Combinational   8.67e-03    8.58e-04    5.17e-04    1.00e-02    88.5%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          9.91e-03    9.23e-04    5.17e-04    1.13e-02   100.0%
               87.3%        8.1%        4.6%
=====
```

Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
-77.0796
-----
finish slack div critical path delay
-----
-5.150992
=====
```

Design Area Report in 6\_report.log:

```
=====
finish report_design_area
-----
Design area 2522 u^2 23% utilization.
=====
```

## Experiment #3

Changed clk\_period 1580

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.02e-03    5.37e-05    1.92e-07    1.07e-03    11.4%
Combinational   7.13e-03    6.98e-04    5.17e-04    8.34e-03    88.6%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          8.15e-03    7.52e-04    5.17e-04    9.42e-03   100.0%
               86.5%        8.0%       5.5%
-----
```

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-72.6782
-----
finish slack div critical path delay
-4.100691
-----
```

**Design Area Report in 6\_report.log:**

```
=====
finish report_design_area
-----
Design area 2507 u^2 23% utilization.
-----
```

## Experiment #4

Changed clk\_period 1000

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.61e-03    8.49e-05    1.92e-07    1.69e-03    11.6%
Combinational   1.13e-02    1.12e-03    5.17e-04    1.29e-02    88.4%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          1.29e-02    1.21e-03    5.17e-04    1.46e-02    100.0%
          88.2%        8.3%        3.5%
=====
```

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-----
-292.4064
=====
```

**Design Area Report in 6\_report.log:**

```
=====
finish report_design_area
-----
Design area 2517 u^2 23% utilization.
=====
```

## Experiment #5

Changed clk\_period 1100

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.46e-03    7.68e-05    1.92e-07    1.54e-03    11.6%
Combinational   1.02e-02    1.01e-03    5.17e-04    1.18e-02    88.4%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          1.17e-02    1.09e-03    5.17e-04    1.33e-02    100.0%
               87.9%        8.2%       3.9%
=====
```

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-----
-242.1651
=====

```

**Design Area Report in 6\_report.log:**

```
=====
finish report_design_area
-----
Design area 2515 u^2 23% utilization.
=====
```

## Experiment #6

Changed clk\_period 1535

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.05e-03    5.52e-05    1.92e-07    1.10e-03   11.4%
Combinational   7.34e-03    7.24e-04    5.17e-04    8.58e-03   88.6%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00   0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00   0.0%
-----
Total          8.39e-03    7.79e-04    5.17e-04    9.69e-03   100.0%
               86.6%        8.0%       5.3%
=====
```

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-----
-1684.0197
=====
```

**Design Area Report in 6\_report.log:**

```
=====
finish report_design_area
-----
Design area 2539 u^2 23% utilization.
=====
```

## Experiment #7

Clk\_period 1500

### Changes in Makefile:

```
export GPL_TIMING_DRIVEN = 1  
export GPL_ROUTABILITY_DRIVEN = 1  
export DPO_MAX_DISPLACEMENT = 5 1
```

### Changes in config.mk file

```
export MACRO_PLACE_HALO = 1 1  
export PDN_TCL = designs/asap7/mock-array-big/pdn.tcl  
export MACRO_EXTENSION = 2  
export ENABLE_DPO = 1
```

### Power Report in 6\_report.log:

```
=====  
finish report_power  
-----  


| Group         | Internal Power    | Switching Power  | Leakage Power    | Total Power (Watts) |        |
|---------------|-------------------|------------------|------------------|---------------------|--------|
| Sequential    | 1.07e-03          | 5.62e-05         | 1.92e-07         | 1.13e-03            | 11.4%  |
| Combinational | 7.51e-03          | 7.27e-04         | 5.17e-04         | 8.76e-03            | 88.6%  |
| Macro         | 0.00e+00          | 0.00e+00         | 0.00e+00         | 0.00e+00            | 0.0%   |
| Pad           | 0.00e+00          | 0.00e+00         | 0.00e+00         | 0.00e+00            | 0.0%   |
| Total         | 8.59e-03<br>86.9% | 7.83e-04<br>7.9% | 5.17e-04<br>5.2% | 9.89e-03            | 100.0% |

  
=====
```

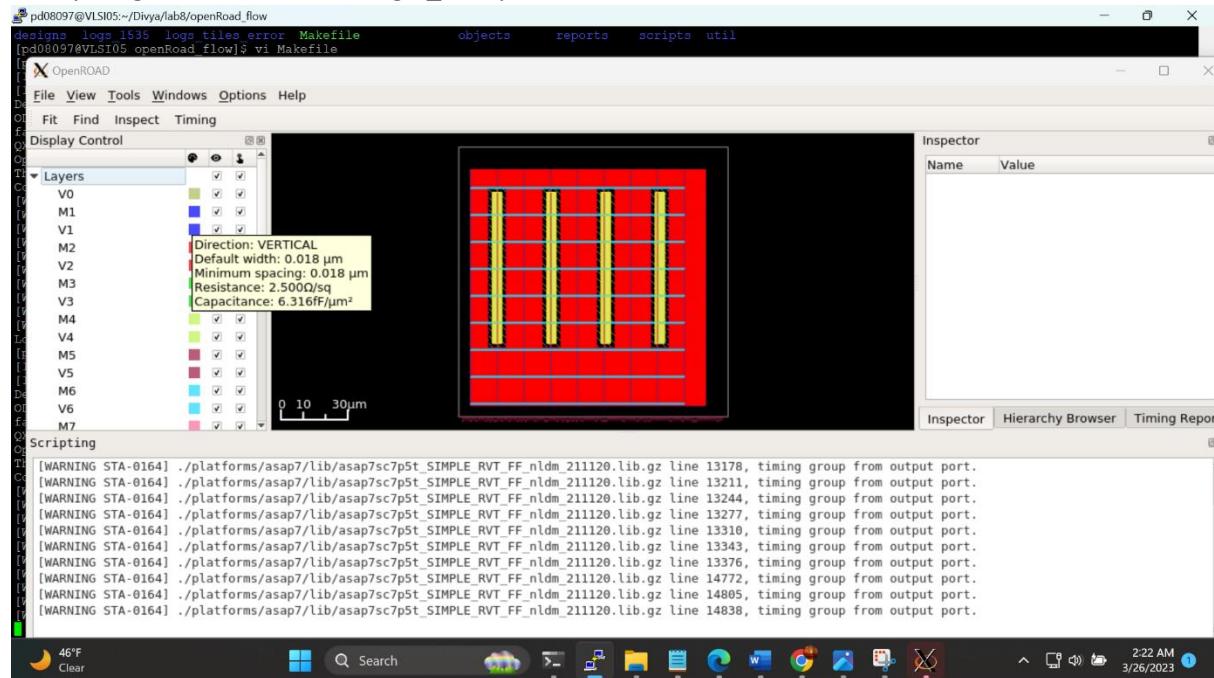
### Timing Report in 6\_report.log:

```
=====  
finish report_design_area  
-----  
Design area 2439 u^2 22% utilization.  
=====
```

### Design Area Report in 6\_report.log:

```
=====  
finish critical path slack  
-----  
7.0769  
=====
```

## Floorplan gui: Command: make gui\_floorplan



## Experiment #8

### Changed Files:

**constraint.sdc**

Clk\_period 1508

### Changes in Makefile:

```
export GPL_TIMING_DRIVEN = 1
```

```
export GPL_ROUTABILITY_DRIVEN = 1
```

```
export DPO_MAX_DISPLACEMENT = 5 1
```

### Changes in config.mk file

```
export MACRO_PLACE_HALO = 1 1
```

```
export PDN_TCL = designs/asap7/mock-array-big/pdn.tcl
```

```
export MACRO_EXTENSION = 2
```

```
export ENABLE_DPO = 1
```

### Power Report in 6\_report.log:

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	1.07e-03	5.60e-05	1.92e-07	1.12e-03	11.4%
Combinational	7.47e-03	7.24e-04	5.17e-04	8.71e-03	88.6%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	8.54e-03	7.80e-04	5.17e-04	9.84e-03	100.0%
	86.8%	7.9%	5.3%		

### Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
29.6565
```

### Design Area Report in 6\_report.log:

```
=====
finish report_design_area
-----
Design area 2437 u^2 22% utilization.
```

## Experiment #9

### Changed Files:

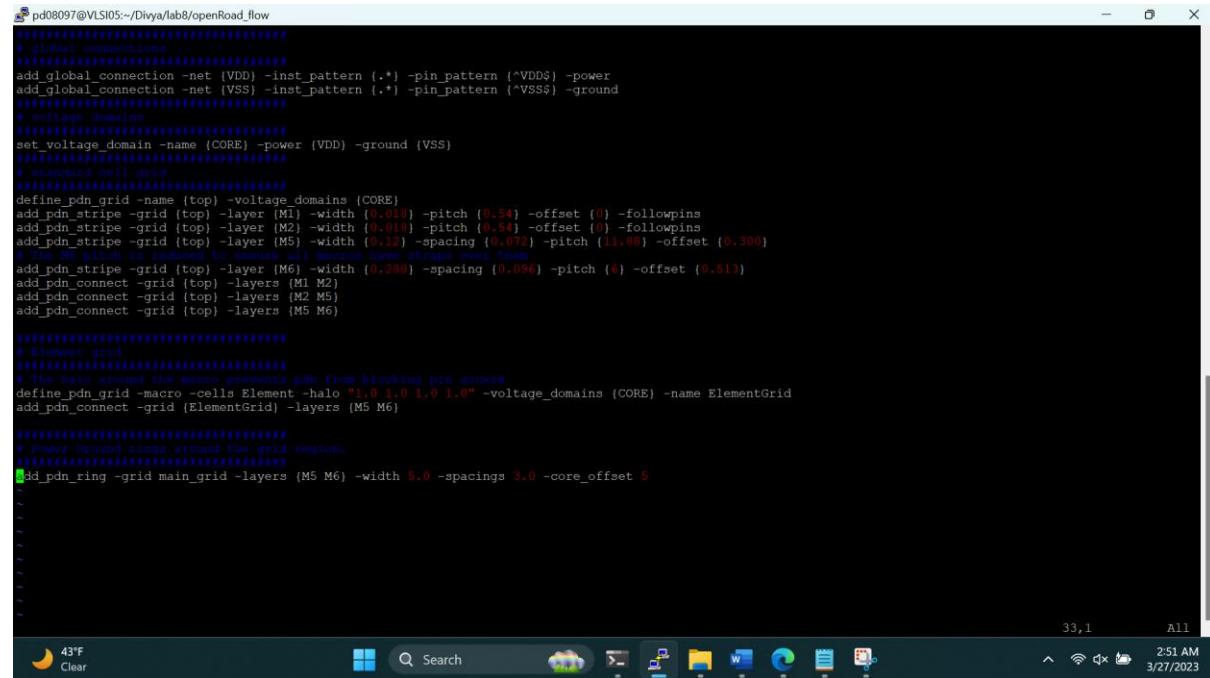
constraint.sdc

Clk\_period 1508

Cd ./designs/asap7/mock-array-big/pdn.tcl

Added pad rings by below command in pdn.tcl script:

```
add_pdn_ring -grid main_grid -layers {M5 M6} -width 5.0 -spacings 3.0 -core_offset 5
```



```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
# Global connections
add_global_connection -net {VDD} -inst_pattern {*} -pin_pattern {"VDD$} -power
add_global_connection -net {VSS} -inst_pattern {*} -pin_pattern {"VSS$} -ground

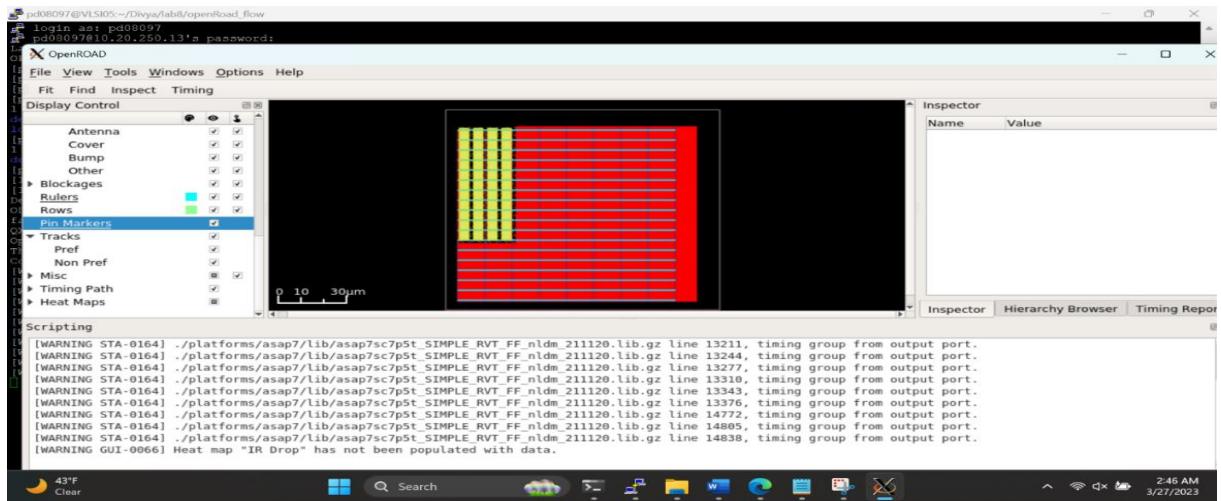
# Set voltage domain
set_voltage_domain -name {CORE} -power {VDD} -ground {VSS}

# Define PDN grid
define_pdn_grid -name {top} -voltage_domains {CORE}
add_pdn_stripe -grid {top} -layer {M1} -width {0.018} -pitch {0.54} -offset {} -followpins
add_pdn_stripe -grid {top} -layer {M2} -width {0.018} -pitch {0.54} -offset {} -followpins
add_pdn_stripe -grid {top} -layer {M5} -width {0.18} -spacing {0.012} -pitch {1.00} -offset {0.300}
add_pdn_stripe -grid {top} -layer {M6} -width {0.200} -spacing {0.096} -pitch {0} -offset {0.513}
add_pdn_connect -grid {top} -layers {M1 M2}
add_pdn_connect -grid {top} -layers {M2 M5}
add_pdn_connect -grid {top} -layers {M5 M6}

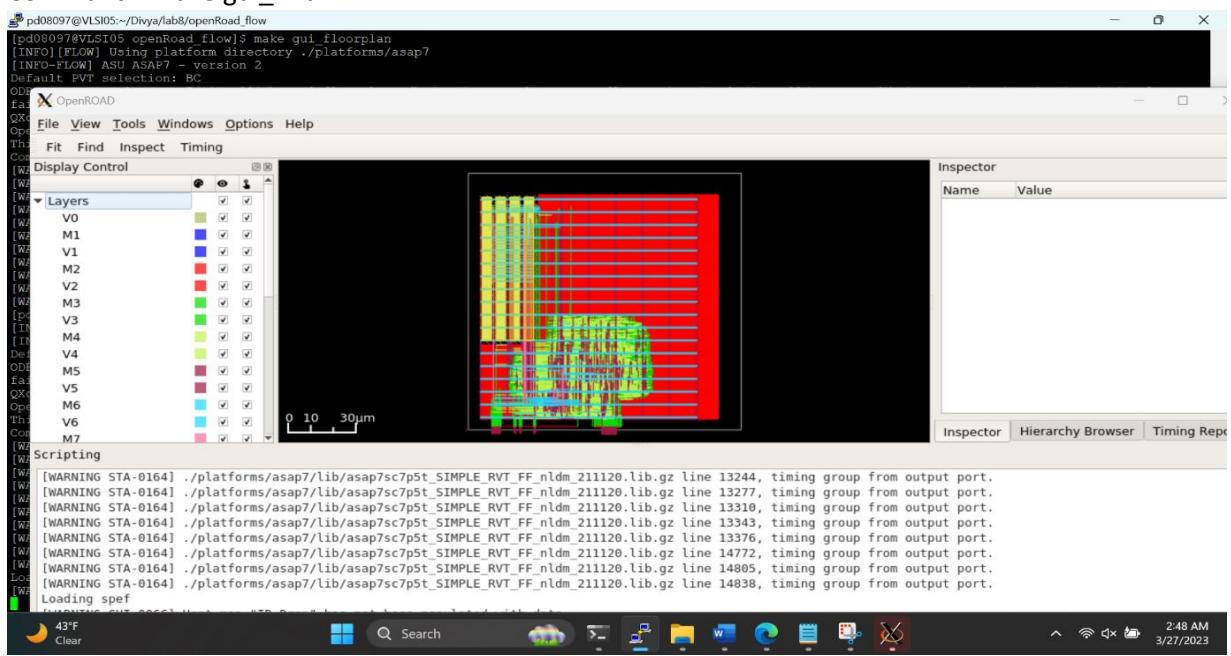
# Element grid
# This adds around the macro connection pin from blocking pin issues
define_pdn_grid -macro -cells Element -halo "1.0 1.0 1.0 1.0" -voltage_domains {CORE} -name ElementGrid
add_pdn_connect -grid {ElementGrid} -layers {M5 M6}

# Power/Ground rings around the grid regions.
add_pdn_ring -grid main_grid -layers {M5 M6} -width 5.0 -spacings 3.0 -core_offset 5
```

**Below is updated floorplan:** Command: make gui\_floorplan



Command : make gui\_final



## Command: make gui\_final zoom view

```
[pd08097@VLSI05:~/Divya/lab8/openRoad flow]
[pd08097@VLSI05 openRoad flow]$ make gui floorplan
[INFO] [FLOW] Using platform directory ./platforms/asap7
[INFO-FLOW] ASU ASAP7 - version 2
Default PVT selection: BC
ODE
fa X OpenROAD
QX File View Tools Windows Options Help
Th Fit Find Inspect Timing
Con Display Control
[W] Layers
[W] V0
[W] M1
[W] V1
[W] M2
[W] V2
[W] M3
[V] M4
[V] M5
[V] V5
[V] M6
[V] M7
[V] V7
[V] M8
[V] V8
[V] M9
[W] Scripting
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.

Inspector
Name Value
Type Inst
Name riscv/dp/rft/_11096_
Module riscv/dp/rft
Master AO21x1_ASAP7_75t_R
Descri... Combinational
Placem... PLACED
Source ... NONE
Dont T... False
Orienta... R0
X 52.812 μm
Y 39.150 μm
▼ ITerms 6 items
A1 riscv/dp/rft2[5]
A2 riscv/dp/rft/_05886_
B riscv/dp/rft/_05895_
VDD VDD
[...]
```

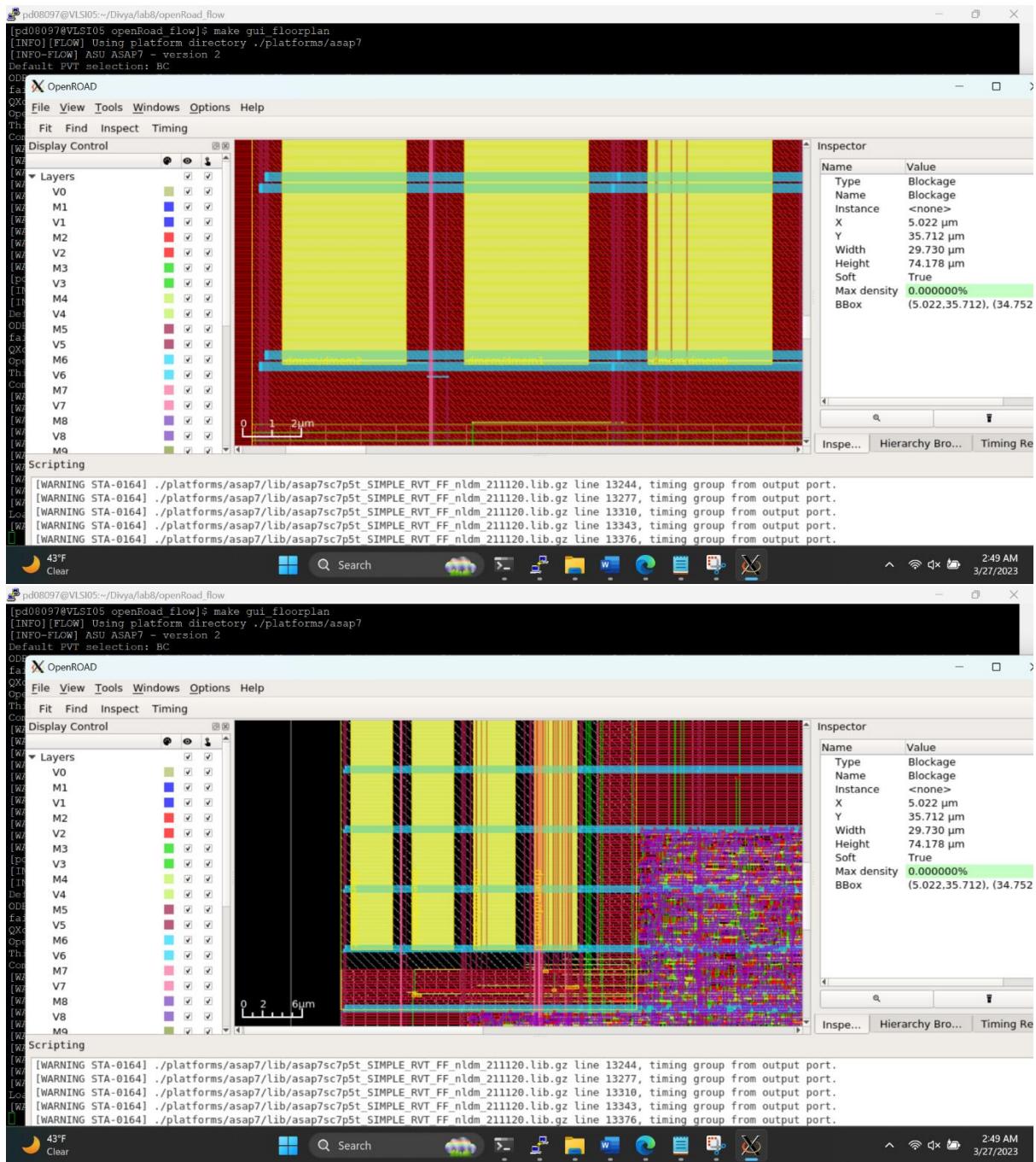
43°F Clear 2:48 AM 3/27/2023

```
[pd08097@VLSI05:~/Divya/lab8/openRoad flow]
[pd08097@VLSI05 openRoad flow]$ make gui floorplan
[INFO] [FLOW] Using platform directory ./platforms/asap7
[INFO-FLOW] ASU ASAP7 - version 2
Default PVT selection: BC
ODE
fa X OpenROAD
QX File View Tools Windows Options Help
Th Fit Find Inspect Timing
Con Display Control
[W] Layers
[W] V0
[W] M1
[W] V1
[W] M2
[W] V2
[W] M3
[V] M4
[V] M5
[V] V5
[V] M6
[V] M7
[V] V7
[V] M8
[V] V8
[V] M9
[W] Scripting
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.
[W] [WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.

Inspector
Name Value
Type Net
Name VSS
Signal type GROUND
Source type NONE
Wire type ROUTED
Special True
Dont Touch False
ITerms 49545 items
BTerms 0 items
Buffer tree VSS
BBox (5.022,5.121), (109.998

[...]
```

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## Experiment #10

Clock period: 1508

Added below changes in Makefile to enable arguments for global placements settings.

```
export GPL_TIMING_DRIVEN = 1  
export GPL_SKIP_INITIAL_PLACE = 0  
export GPL_INCREMENTAL = 1  
export GPL_TIMING_DRIVEN_NET_WEIGHT_MAX = 1  
export GPL_TIMING_DRIVEN_NETS_PERCENTAGE = 1  
export GPL_INITIAL_PLACE_MAX_ITER = 1  
export GPL_ROUTABILITY_DRIVEN = 1  
  
export ENABLE_DPO = 1  
export DPO_MAX_DISPLACEMENT ?= 5 1
```

Modified Global placement.tcl script

```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
export MAX_UNGROUP_SIZE ?= 0
endif
# Enables Re-synthesis for area reclaim
export RESYNTH_AREA_RECOVER = 0
export RESYNTH_TIMING_RECOVER ?= 0
export ABC_AREA ?= 0

# Global setting for Synthesis
export SYNTN_ARGS ?= -flatten

# Global setting for Floorplan
export PLACE_PINS_ARGS

export FLOW VARIANT ?= base

export GPL_TIMING_DRIVEN = 1
export GPL_SKIP_INITIAL_PLACE = 0
export GPL_INCREMENTAL = 1
export GPL_TIMING_DRIVEN_NET_WEIGHT_MAX = 1
export GPL_TIMING_DRIVEN_NETS_PERCENTAGE = 1
export GPL_INITIAL_PLACE_MAX_ITER = 1
export GPL_ROUTABILITY_DRIVEN = 1

export ENABLE_DPO = 1
export DPO_MAX_DISPLACEMENT ?= 5 1

# Setup working directories
export DESIGN_NICKNAME ?= $(DESIGN_NAME)

export DESIGN_DIR = $(dir $(DESIGN_CONFIG))
export LOG_DIR = $(WORK_HOME)/logs/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)
export OBJECTS_DIR = $(WORK_HOME)/objects/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)
export REPORTS_DIR = $(WORK_HOME)/reports/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)
export RESULTS_DIR = $(WORK_HOME)/results/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)

ifdef BLOCKS
$[info [INFO][FLOW] Invoked hierarchical flow.)
$[foreach block,$(BLOCKS),$[info Block $block needs to be hardened.)]
endif
Makefile      122,1    11% scripts/global_place.tcl      23,5    66%
```

61°F Sunny 4:01 PM 3/27/2023

```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
export MAX_UNGROUP_SIZE ?= 0
endif
# Enables Re-synthesis for area reclaim
export RESYNTH_AREA_RECOVER = 0
export RESYNTH_TIMING_RECOVER ?= 0
export ABC_AREA ?= 0

# Global setting for Synthesis
export SYNTN_ARGS ?= -flatten

# Global setting for Floorplan
export PLACE_PINS_ARGS

export FLOW VARIANT ?= base

export GPL_TIMING_DRIVEN = 1
export GPL_SKIP_INITIAL_PLACE = 0
export GPL_INCREMENTAL = 1
export GPL_TIMING_DRIVEN_NET_WEIGHT_MAX = 1
export GPL_TIMING_DRIVEN_NETS_PERCENTAGE = 1
export GPL_INITIAL_PLACE_MAX_ITER = 1
export GPL_ROUTABILITY_DRIVEN = 1

export ENABLE_DPO = 1
export DPO_MAX_DISPLACEMENT ?= 5 1

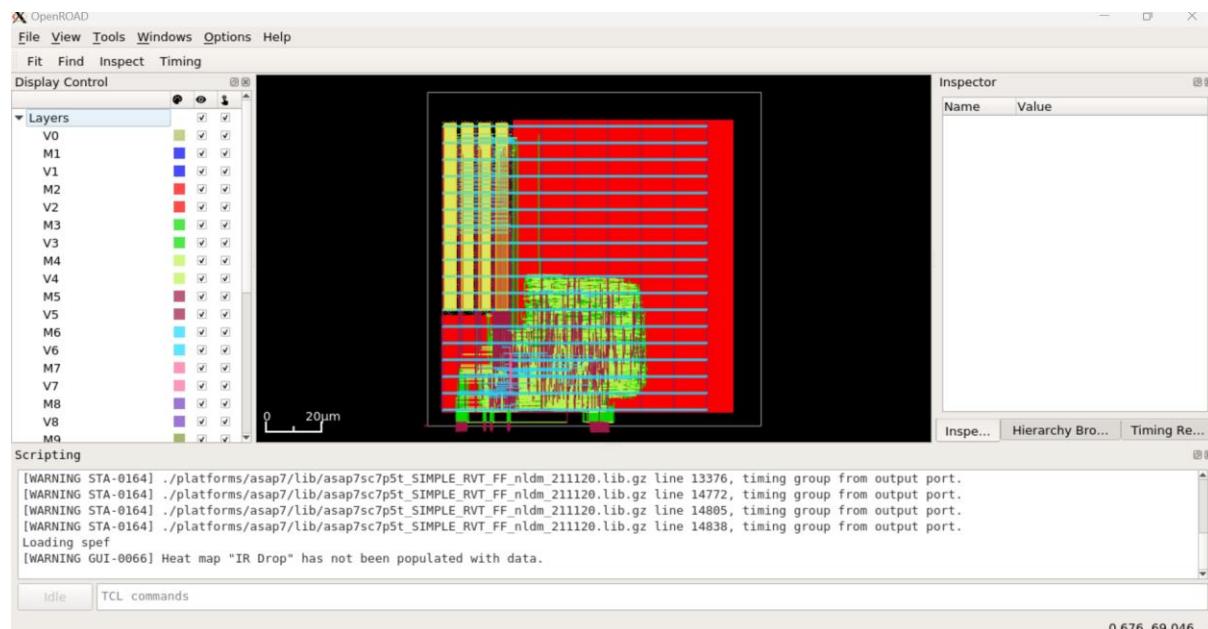
# Setup working directories
export DESIGN_NICKNAME ?= $(DESIGN_NAME)

export DESIGN_DIR = $(dir $(DESIGN_CONFIG))
export LOG_DIR = $(WORK_HOME)/logs/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)
export OBJECTS_DIR = $(WORK_HOME)/objects/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)
export REPORTS_DIR = $(WORK_HOME)/reports/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)
export RESULTS_DIR = $(WORK_HOME)/results/$(PLATFORM)/$(DESIGN_NICKNAME)/$(FLOW_VARIANT)

ifdef BLOCKS
$[info [INFO][FLOW] Invoked hierarchical flow.)
$[foreach block,$(BLOCKS),$[info Block $block needs to be hardened.)]
endif
Makefile      122,1    11% scripts/global_place.tcl      23,5    66%
```

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## RISCV32 final gui: make gui\_final



# Experiment #11

## Changed Core Are and Die Area

```
export DIE_AREA = 0 0 110 110
```

```
export CORE_AREA = 5 5 100 100
```

```
clk_period 1508
```

### Power Report in 6\_report.log:

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	1.07e-03	5.65e-05	1.92e-07	1.12e-03	11.4%
Combinational	7.47e-03	7.25e-04	5.17e-04	8.72e-03	88.6%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	8.54e-03	7.82e-04	5.17e-04	9.84e-03	100.0%
	86.8%	7.9%	5.3%		

### Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
38.5209
```

### Design Area Report in 6\_report.log:

```
=====
finish report_design_area
-----
Design area 2431 u^2 27% utilization.
```

### Errors/Warning:

```
[WARNING GUI-0076] failed to get the current screen resources
[WARNING QXcbConnection: XCB error: 170 (Unknown), sequence: 170, resource id: 90, major code: 146 (Unknown), minor code: 20
Elapsed time: 1:01.22[h]:min:sec. CPU time: user 48.67 sys 1.58 (82%). Peak memory: 1425952KB.
cp results/asap7/riscv32i/base/5_route.sdc results/asap7/riscv32i/base/6_final.sdc
sed 'OR_DEFAULT/d' platforms/asap7/lef/asap7_tech_lx_201209.lef > objects/asap7/riscv32i/base/klayout_tech.lef
sed 's,<lef-files>.*</lef-files>,<lef-files>/home/pd08097/Divya/lab8/openRoad_flow/objects/asap7/riscv32i/base/klayout_tech.lef</lef-files><lef-files>/home/pd08097/Divya/lab8/openRoad_flow/platforms/asap7/lef/asap7sc7p5t_28_R_lx_220121a.lef</lef-files><lef-files>/home/pd08097/Divya/lab8/openRoad_flow/platforms/asap7/lef/fakeram_256x32.lef</lef-files>,q
platforms/asap7/kLayout/asap7.lyt > objects/asap7/riscv32i/base/klayout.lyt
(/usr/bin/time -f "%E[h]:%M:min:sec. CPU time: user %U sys %S (%P). Peak memory: %MRB." stdbuf -oL /usr/bin/klayout -zz -rd design_name=riscv_top
\'
-rd in_def=results/asap7/riscv32i/base/6_final.def \
-rd in_file="./platforms/asap7/gds/asap7sc7p5t_28_R_220121a.gds" \
-rd config_file= \
-rd seal_file="" \
-rd out_file=results/asap7/riscv32i/base/6_1_merged.gds \
-rd tech_file=/objects/asap7/riscv32i/base/klayout.lyt \
-rd layer_map= \
-r -r ./util/def2stream.py) 2>&1 | tee ./logs/asap7/riscv32i/base/6_1_merge.log
[INFO] Reporting cells prior to loading DEF ...
[INFO] Reading DEF ...
[INFO] Clearing cells...
[INFO] Merging GDS files...
[INFO] Copying toplevel cell 'riscv_top'
[WARNING: no fill config file specified
[INFO] Checking for missing cell from GDS/OAS...
[INFO] Found GDS ALLOW_EMPTY variable.
[WARNING] LEF Cell 'fakeram_256x32' ignored. Matches GDS_ALLOW_EMPTY.
[INFO] Checking for orphan cell in the final layout...
[INFO] Writing out GDS/OAS 'results/asap7/riscv32i/base/6_1_merged.gds'
Elapsed time: 0:03.77[h]:min:sec. CPU time: user 3.48 sys 0.29 (99%). Peak memory: 344612KB.
cp results/asap7/riscv32i/base/6_1_merged.gds results/asap7/riscv32i/base/6_final.gds
Log Elapsed seconds
```

# Experiment #12

## Changed Core Are and Die Area

```
export DIE_AREA = 0 0 110 110
```

```
export CORE_AREA = 5 5 98 98
```

**Commented Pin-Place export command:**

```
#export PLACE_PINS_ARGS = -exclude left:* -exclude right:* -exclude top:*
```

**Power Report in 6\_report.log:**

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	1.07e-03	5.66e-05	1.92e-07	1.12e-03	11.4%
Combinational	7.47e-03	7.24e-04	5.17e-04	8.71e-03	88.6%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	8.53e-03	7.81e-04	5.17e-04	9.83e-03	100.0%
	86.8%	7.9%	5.3%		

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-----
3.9549
```

**Design Area Report in 6\_report.log:**

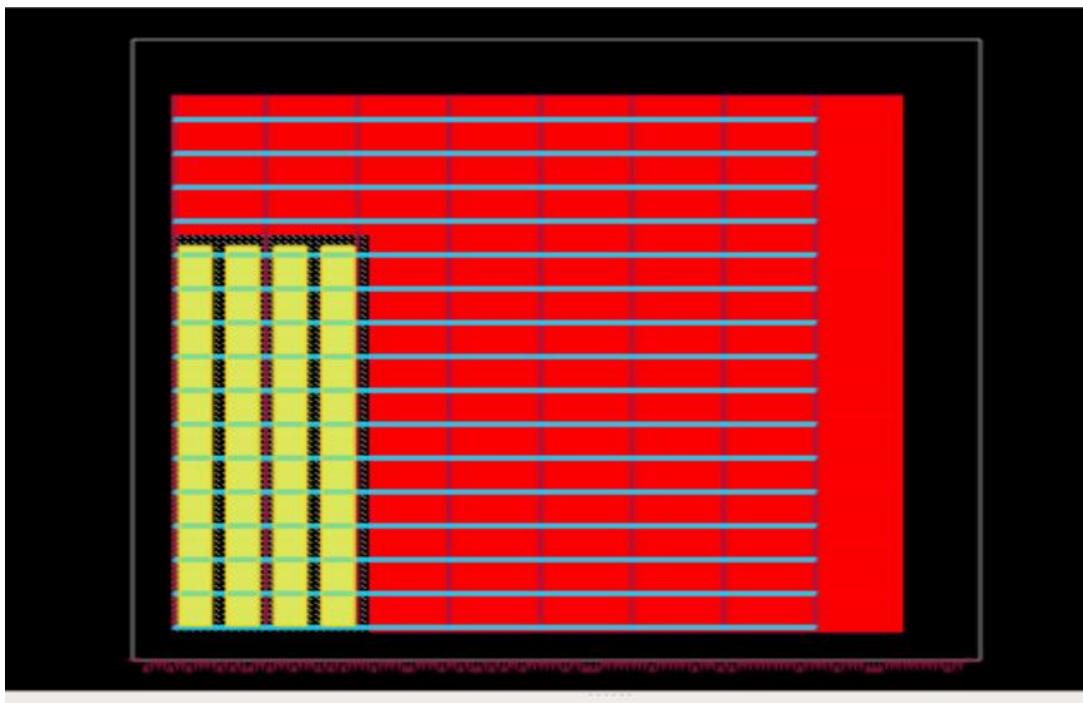
```
=====
finish report_design_area
-----
Design area 2428 u^2 28% utilization.
```

**Errors/Warning:**

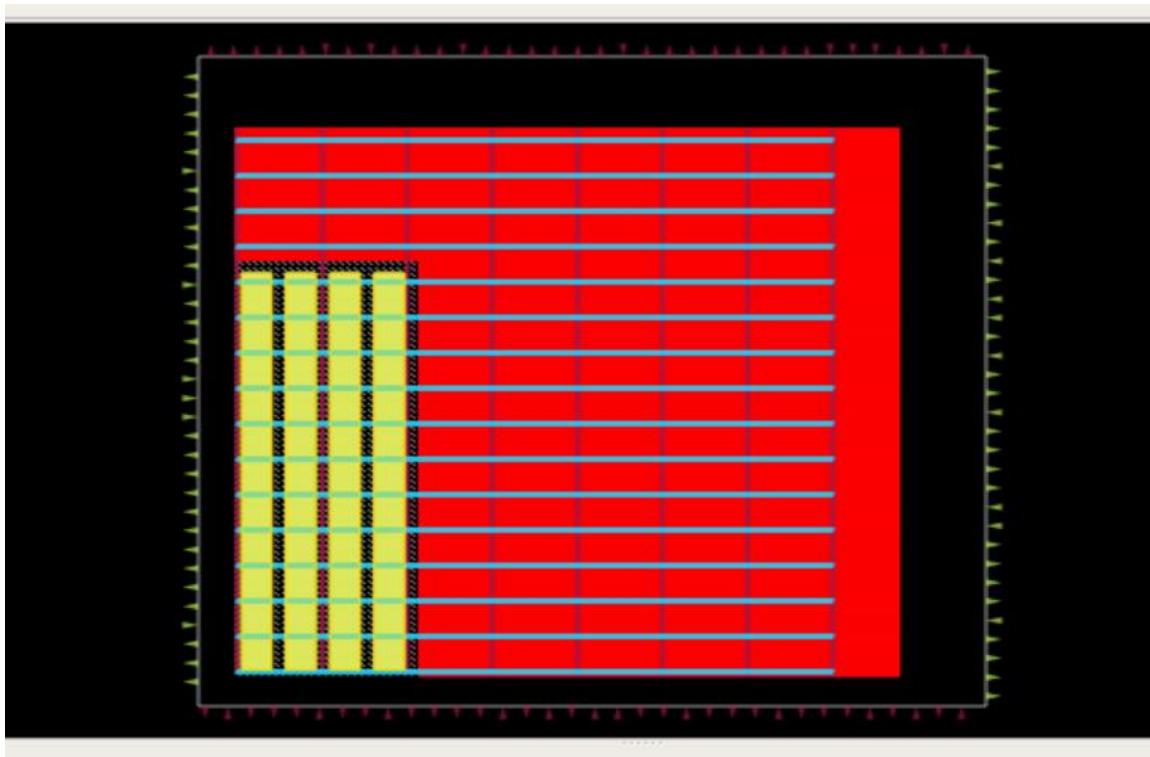
```
[WARNING GUI-0076] failed to get the current screen resources
[WARNING GUI-0076] XkbConnection XCB error: 170 Unknown sequence: 170, resource id: 90, major code: 146 (Unknown), minor code: 20
Elapsed time: 0:03.87min:sec CPU time: user 0.34 sys 0.32 (100%). Peak memory: 1418952KB.
cp results/asap7/riscv32i/base/5_route.sdc results/asap7/riscv32i/base/6_final.sdc
sed 'OR_DEFAULTD' platform/asap7/lef/asap7_tech_1x_201209.lef > objects/asap7/riscv32i/base/klayout_tech.lef
sed 's,<lef-files>,*</lef-files>,<lef-files>/home/pd08097/Divya/lab8/openRoad_flow/objects/asap7/riscv32i/base/klayout_tech.lef</lef-files><lef-files>/home/pd08097/Divya/lab8/openRoad_flow/platform/asap7/lef/asap7sc7p5t_28_R_ix_220121a.lef</lef-files><lef-files>/home/pd08097/Divya/lab8/openRoad_flow/platform/asap7/lef/fakeram7_256x32.lef</lef-files>,*' platforms/asap7/RLayout/asap7.lyt > objects/asap7/riscv32i/base/klayout.lyt
/usr/bin/time -l Elapsed time: 0:03.87min:sec CPU time: user 0.34 sys 0.32 (100%). Peak memory: %MRB.' stdbuf -o L /usr/bin/klayout -zz -rd design_name=riscv_top
`-
-rd in def=results/asap7/riscv32i/base/6_final.def \
-rd in files=".platforms/asap7/gds/asap7sc7p5t_28_R_220121a.gds " \
-rd config_file= \
-rd seal_file="" \
-rd top_level_file=results/asap7/riscv32i/base/6_1_merged.gds \
-rd tech_file=objects/asap7/riscv32i/base/klayout.lyt \
-rd layer_map= \
-r ./util/def2strem.py 2>&1 | tee ./logs/asap7/riscv32i/base/6_1_merge.log
[INFO] Reporting cells prior to loading DEF ...
[INFO] Reading DEF ...
[INFO] Creating cells...
[INFO] Merging GDS/OAS files...
./platforms/asap7/gds/asap7sc7p5t_28_R_220121a.gds
[INFO] Copying toplevel cell 'riscv_top'
WARNING: no fill config file specified
[INFO] Checking for missing cells from GDS/OAS...
[INFO] Found 0 GDS and 0 OAS Variables
[WARNING] LEF Cell 'fakeram7_256x32' ignored. Matches GDS_ALLOW_EMPTY.
[INFO] Checking for orphan cell in the final layout...
[INFO] No orphan cells
[INFO] Writing out GDS/OAS 'results/asap7/riscv32i/base/6_1_merged.gds'
Elapsed time: 0:03.87min:sec CPU time: user 0.34 sys 0.32 (100%). Peak memory: 343044KB.
cp results/asap7/riscv32i/base/6_1_merged.gds results/asap7/riscv32i/base/6_final.gds
```

Floorplan Comparison in Experiment 11 and Experiment 12:

**Floorplan in Experiment #11**



**Floorplan in Experiment #12**



## Experiment #13

Added in Makefile: export PLACE\_DENSITY\_LB\_ADDON = 0.20

export ENABLE\_DPO = 1 (Enabled Detailed placement Optimization)

Power Report in 6\_report.log:

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	1.06e-03	5.65e-05	1.58e-07	1.11e-03	11.9%
Combinational	7.30e-03	4.49e-04	5.17e-04	8.27e-03	88.1%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	8.36e-03	5.05e-04	5.17e-04	9.38e-03	100.0%
	89.1%	5.4%	5.5%		

Timing Report in 6\_report.log:

finish critical path delay
1307.1575
finish critical path slack
12.3425

Design Area Report in 6\_report.log:

finish report_design_area
Design area 2387 u^2 22% utilization.

## Experiment #14

Changed set cluster\_size 35 in cts.tcl

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.06e-03    5.65e-05    1.58e-07    1.12e-03   11.9%
Combinational   7.29e-03    4.45e-04    5.17e-04    8.25e-03   88.1%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00   0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00   0.0%
-----
Total          8.35e-03    5.01e-04    5.17e-04    9.37e-03   100.0%
               89.1%        5.3%        5.5%
```

**Timing Report in 6\_report.log:**

```
=====
finish slack div critical path delay
-----
-0.861621
```

.

**Design Area Report in 6\_report.log:**

```
=====
finish report_design_area
-----
Design area 2386 u^2 22% utilization.
```

## Experiment #15

Changed set cluster\_size 26 in cts.tcl

Power Report in 6\_report.log:

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.05e-03    5.65e-05    1.58e-07    1.11e-03   11.8%
Combinational   7.31e-03    4.52e-04    5.17e-04    8.28e-03   88.2%
Macro           0.00e+00    0.00e+00    0.00e+00    0.00e+00   0.0%
Pad             0.00e+00    0.00e+00    0.00e+00    0.00e+00   0.0%
-----
Total           8.36e-03    5.08e-04    5.17e-04    9.39e-03   100.0%
          89.1%        5.4%        5.5%
```

Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
8.8917
```

Design Area Report in 6\_report.log:

```
=====
finish report_design_area
-----
Design area 2387 u^2 22% utilization.
```

# Experiment #16

## Modified Io\_placement.tcl

```
make_io_sites -horizontal_site IOSITE -vertical_site IOSITE -corner_site IOSITE -offset 15
```

```
place_pad -master PADCELL_SIG_V -row IO_EAST -location 110 "IO_EAST_SIDE"  
place_pad -master PADCELL_SIG_V -row IO_WEST -location 110 "IO_WEST_SIDE"  
place_pad -master PADCELL_SIG_H -row IO_NORTH -location 110 "IO_NORTH_SIDE"  
place_pad -master PADCELL_SIG_H -row IO_SOUTH -location 110 "IO_SOUTH_SIDE"
```

```
source $::env(SCRIPTS_DIR)/load.tcl  
load_design 3_1_place_gp_skip_io.odb 2_floorplan.sdc "Starting io placement"  
  
if {[info exists ::env(FLOORPLAN_DEF)]} {  
    puts "Skipping IO placement as DEF file was used to initialize floorplan."  
#    place_pad -row IO_SOUTH -location 280.0 {u_clk.u_in}  
} else {  
    if {[info exists ::env(IO_CONSTRAINTS)]} {  
        source $::env(IO_CONSTRAINTS)  
    }  
    place_pins -hor_layer $::env(IO_PLACER_H) \  
        -ver_layer $::env(IO_PLACER_V) \  
        {*}$::env(PLACE_PINS_ARGS)  
# place_pad -row IO_SOUTH -location 280.0 {u_clk.u_in}  
#make_io_sites -horizontal_site IOSITE -vertical_site IOSITE -corner_site IOSITE -offset 15  
  
place_pad -master PADCELL_SIG_V -row IO_EAST -location 110 "IO_EAST_SIDE"  
place_pad -master PADCELL_SIG_V -row IO_WEST -location 110 "IO_WEST_SIDE"  
place_pad -master PADCELL_SIG_H -row IO_NORTH -location 110 "IO_NORTH_SIDE"  
place_pad -master PADCELL_SIG_H -row IO_SOUTH -location 110 "IO_SOUTH_SIDE"  
}  
  
if {![$info exists save_checkpoint] || $save_checkpoint} {  
    write_db $::env(RESULTS_DIR)/3_2_place_iop.odb  
}  
~  
~
```

## Errors/Warnings:

```
Has top down IO Constraints. Skip global placement without IOs  
Elapsed time: 0:02.24[h:]min:sec. CPU time: user 2.09 sys 0.14 (99%). Peak memory: 167860KB.  
/usr/bin/time -f %E[h:]min:sec. CPU time: user %U sys %S (%P). Peak memory: %MKB.' /usr/openroad/OpenROAD-flow-scripts/tools/install/OpenROAD  
/bin/openroad -exit -no_init ./scripts/io_placement.tcl -metrics ./logs/asap7/riscv32i/base/3_2_place_iop.json 2>&1 | tee ./logs/asap7/riscv32i/base/3_2_pl  
ace_iop.log  
OpenROAD v2.0-6995-g5c85b36  
This program is licensed under the BSD-3 license. See the LICENSE file for details.  
Components of this program may be licensed under more restrictive licenses which must be honored.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13178, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13211, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14772, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14805, timing group from output port.  
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14838, timing group from output port.  
Found 4 macro blocks.  
Using lu default distance from corners.  
Using 2 tracks default min distance between IO pins.  
[INFO PPL-0010] Tentative 0 to set up sections.  
[INFO PPL-0001] Number of slots 4920  
[INFO PPL-0002] Number of I/O 135  
[INFO PPL-0003] Number of I/O w/sink 135  
[INFO PPL-0004] Number of I/O w/o sink 1  
[INFO PPL-0005] Slots per section 200  
[INFO PPL-0006] Slots increase factor 0.01  
[INFO PPL-0008] Successfully assigned pins to sections.  
[INFO PPL-0012] I/O nets HWL: 10135.87 um.  
Error: io_placement.tcl: 21 invalid command name "place_pad"  
Elapsed time: 0:02.20[h:]min:sec. CPU time: user 2.05 sys 0.15 (100%). Peak memory: 175040KB.  
make: *** [results/asap7/riscv32i/base/3_2_place_iop.odb] Error 1
```

## Experiment #17

### Modified input delay in constraint.sdc

Power Report in 6\_report.log:

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	1.05e-03	5.65e-05	1.58e-07	1.11e-03	11.8%
Combinational	7.31e-03	4.50e-04	5.17e-04	8.28e-03	88.2%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	8.36e-03 89.1%	5.07e-04 5.4%	5.17e-04 5.5%	9.39e-03	100.0%

Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
9.0941
=====
```

Design Area Report in 6\_report.log:

```
=====
finish report_design_area
-----
Design area 2387 u^2 22% utilization.
```

## Experiment #18

Modified input delay in constraint by multiple of 0.10 ns

Startpoint: riscv/dp/rf/\_13595\_ (rising edge-triggered flip-flop clocked by clk)

Endpoint: dmem/dmem0 (rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: min : Slack -4.94

```
current_design riscv_top

set clk_name clk
set clk_port_name clk
set clk_period 1508
set clk_io_pct 0.125
set clk_io_pctt 0.10

set clk_port [get_ports $clk_port_name]

create_clock -name $clk_name -period $clk_period $clk_port

set non_clock_inputs [lsearch -inline -all -not -exact [all_inputs] $clk_port]
set_input_delay [expr $clk_period * $clk_io_pctt] -clock $clk_name $non_clock_inputs
set_output_delay [expr $clk_period * $clk_io_pct] -clock $clk_name [all_outputs]
```

Power Report in 6\_report.log:

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.05e-03        5.66e-05        1.58e-07        1.11e-03    11.8%
Combinational   7.31e-03        4.50e-04        5.17e-04        8.28e-03    88.2%
Macro           0.00e+00        0.00e+00        0.00e+00        0.00e+00    0.0%
Pad             0.00e+00        0.00e+00        0.00e+00        0.00e+00    0.0%
-----
Total           8.36e-03        5.07e-04        5.17e-04        9.39e-03    100.0%
          89.1%                5.4%            5.5%
```

Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
21.1206
```

Design Area Report in 6\_report.log:

```
=====
finish report_design_area
-----
Design area 2390 u^2 22% utilization.
```

## Experiment #19

Modified clk period 1510ns and input delay in constraint by multiple of 0.2 ns

Power Report in 6\_report.log:

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.05e-03    5.66e-05    1.58e-07    1.11e-03    11.8%
Combinational   7.31e-03    4.52e-04    5.17e-04    8.28e-03    88.2%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          8.36e-03    5.09e-04    5.17e-04    9.39e-03    100.0%
               89.1%        5.4%        5.5%
-----
finish report_design_area
```

Timing Report in 6\_report.log:

```
=====
finish critical path slack
-----
12.5940
```

Design Area Report in 6\_report.log:

```
=====
finish critical path slack
-----
12.5940
```

## Experiment #20

Modified clk period 1508ns and input delay in constraint by multiple of 0.10 ns

Power Report in 6\_report.log:

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	1.05e-03	5.72e-05	1.58e-07	1.11e-03	11.8%
Combinational	7.31e-03	4.52e-04	5.17e-04	8.28e-03	88.2%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	8.36e-03	5.10e-04	5.17e-04	9.39e-03	100.0%
	89.1%	5.4%	5.5%		

Timing Report in 6\_report.log:

finish critical path slack
-945.7178

Design Area Report in 6\_report.log:

finish report_design_area
Design area 2395 u^2 22% utilization.

Constraint.sdc

```
current_design riscv_top

set clk_name clk
set clk_port_name clk
set clk_period 1508
set clk_io_pct 0.125
set clk_io_pctt 0.00

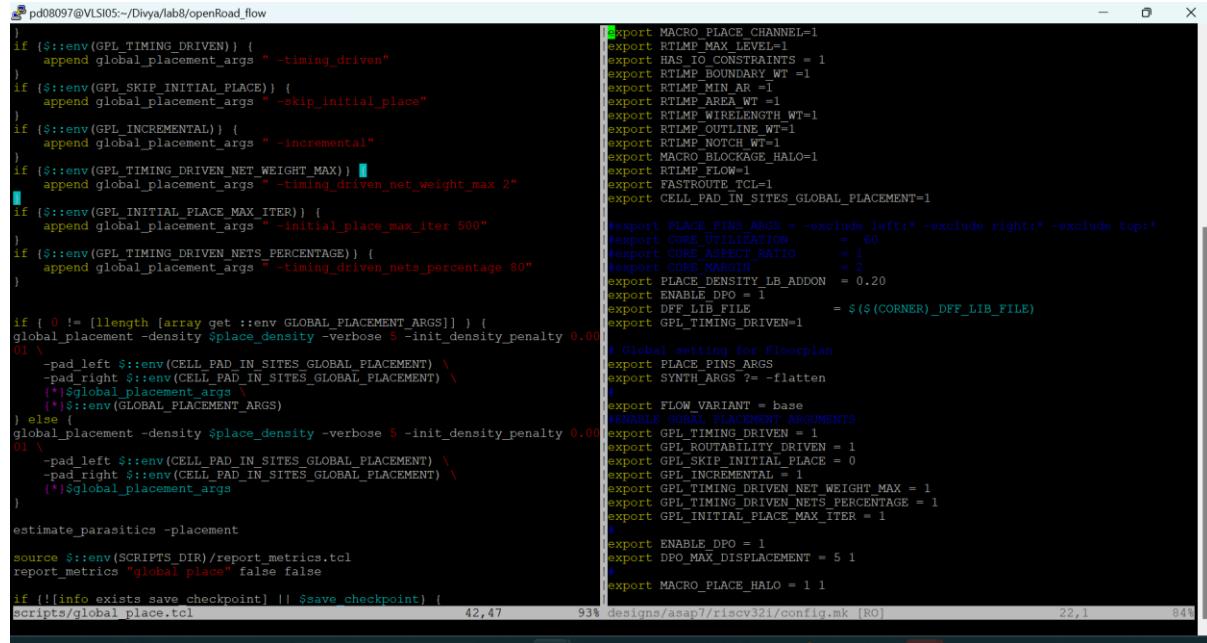
set clk_port [get_ports $clk_port_name]

create_clock -name $clk_name -period $clk_period $clk_port

set non_clock_inputs [lsearch -inline -all -not -exact [all_inputs] $clk_port]
set_input_delay [expr $clk_period * $clk_io_pctt] -clock $clk_name $non_clock_inputs
set_output_delay [expr $clk_period * $clk_io_pct] -clock $clk_name [all_outputs]
~
```

# Experiment #21

## Modified global\_place.tcl file and constraint.sdc



```
pd08097@VLSI05:~/Divy/lab8/openRoad_flow
$ ./global_place.tcl
export MACRO_PLACE_CHANNEL=1
export RTLMP_MAX_LEVEL=1
export HAS_IO_CONSTRAINTS = 1
export RTLMP_BOUNDARY_WT =1
export RTLMP_MIN_AR =1
export RTLMP_AREA_WT =1
export RTLMP_WIRELENGTH_WT=1
export RTLMP_OUTLINE_WT=1
export RTLMP_NOTCH_WT=1
export MACRO_BLOCKAGE_HALO=1
export RTLMP_FLOW=1
export FASTROUTE_TCL=1
export CELL_PAD_IN_SITES_GLOBAL_PLACEMENT=1

export PLACE_PINS_ARGS = -exclude left: -exclude right: -exclude top:
export CORE_UTILIZATION = 60
export CORE_ASPECT_RATIO = 1
export CORE_MARGIN = 2
export PLACE_DENSITY_LB_ADDON = 0.20
export ENABLE_DPO = 1
export DFF_LIB_FILE = $(CORNER)_DFF_LIB_FILE
export GPL_TIMING_DRIVEN=1

# Global setting for Floorplan
export PLACE_PINS_ARGS
export SYNTH_ARGS ?= -flatten

export FLOW_VARIANT = base
ENABLE_GLOBAL_PLACEMENT_ARGUMENTS
export GPL_TIMING_DRIVEN = 1
export GPL_ROUTABILITY_DRIVEN = 1
export GPL_SKIPPING_INITIAL_PLACE = 0
export GPL_INCREMENTAL = 1
export GPL_TIMING_DRIVEN_NET_WEIGHT_MAX = 1
export GPL_TIMING_DRIVEN_NETS_PERCENTAGE = 1
export GPL_INITIAL_PLACE_MAX_ITER = 1

export ENABLE_DPO = 1
export DPO_MAX_DISPLACEMENT = 5 1
export MACRO_PLACE_HALO = 1 1

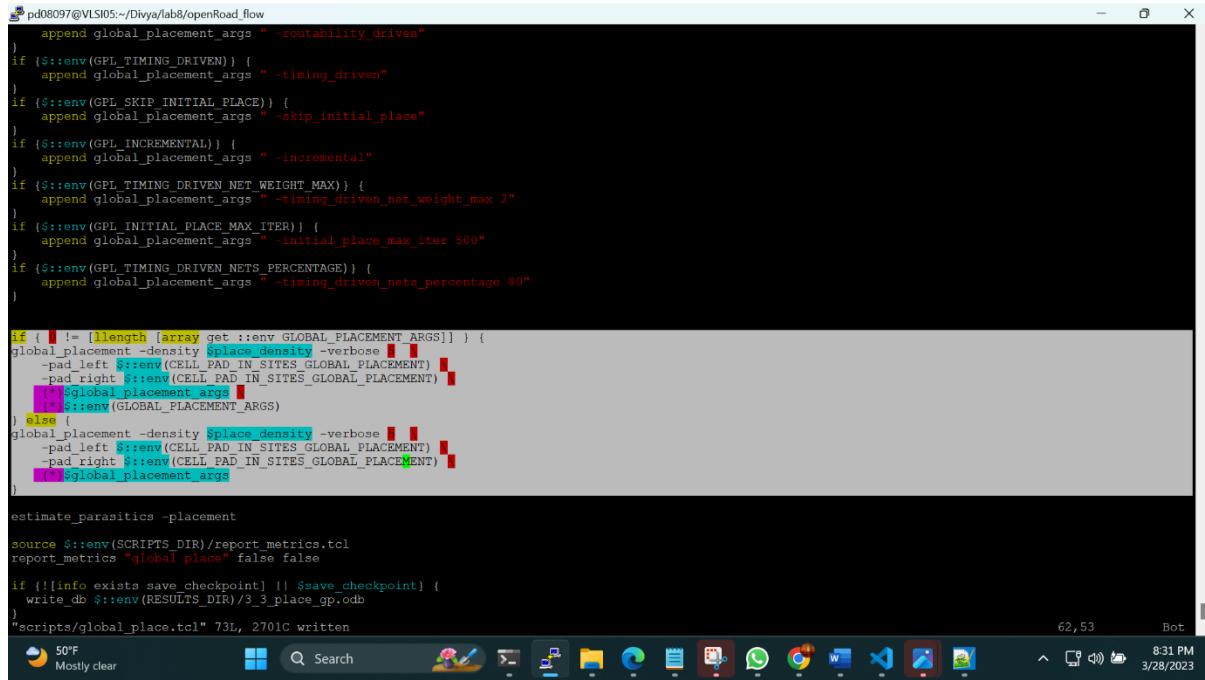
scripts/global.place.tcl      42,47      93% designs/asap7/riscv32i/config.mk [RO]      22,1      84%
```

## Error:

```
Using lu default distance from corners.
Using 2 tracks default min distance between IO pins.
[INFO PPL-0007] Random pin placement.
Elapsed time: 0:02.26[h]:min:sec. CPU time: user 2.08 sys 0.17 (99%). Peak memory: 171832KB.
(/usr/bin/time -f '%Elapsed time: %E[h]:%min:%sec. CPU time: %U sys %S (%P). Peak memory: %MKB.' /usr/openroad/OpenROAD-flow-scripts/tools/install/OpenROAD
/bin/openroad -exit -no_init ./scripts/tdma_place.tcl -metrics ./logs/asap7/riscv32i/base/2_3_tdma.json) 2>&1 | tee ./logs/asap7/riscv32i/base/2_3_tdma_place.log
OpenROAD v2.0-6895-g5c85b36
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13178, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13211, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 14772, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 14805, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14838, timing group from output port.
RTLMP flow enabled. Skipping tdmas place.
Elapsed time: 0:02.21[h]:min:sec. CPU time: user 2.05 sys 0.15 (100%). Peak memory: 171052KB.
(/usr/bin/time -f '%Elapsed time: %E[h]:%min:%sec. CPU time: %U sys %S (%P). Peak memory: %MKB.' /usr/openroad/OpenROAD-flow-scripts/tools/install/OpenROAD
/bin/openroad -exit -no_init ./scripts/macros_place.tcl -metrics ./logs/asap7/riscv32i/base/2_4_mplace.json) 2>&1 | tee ./logs/asap7/riscv32i/base/2_4_mplace.log
OpenROAD v2.0-6895-g5c85b36
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13178, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13211, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 14772, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t SIMPLE_RVT_FF_nldm_211120.lib.gz line 14805, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14838, timing group from output port.
Error: macro_place.tcl, 128 missing function argument at @_ in expression "max(1, @_)"
Elapsed time: 0:02.17[h]:min:sec. CPU time: user 2.02 sys 0.15 (100%). Peak memory: 170860KB.
make: *** [results/asap7/riscv32i/base/2_4_floorplan_macro.odb] Error 1
[pd08097@VLSI05 openRoad_flow]$
```

## Experiment #22

Modified global\_place.tcl file below again

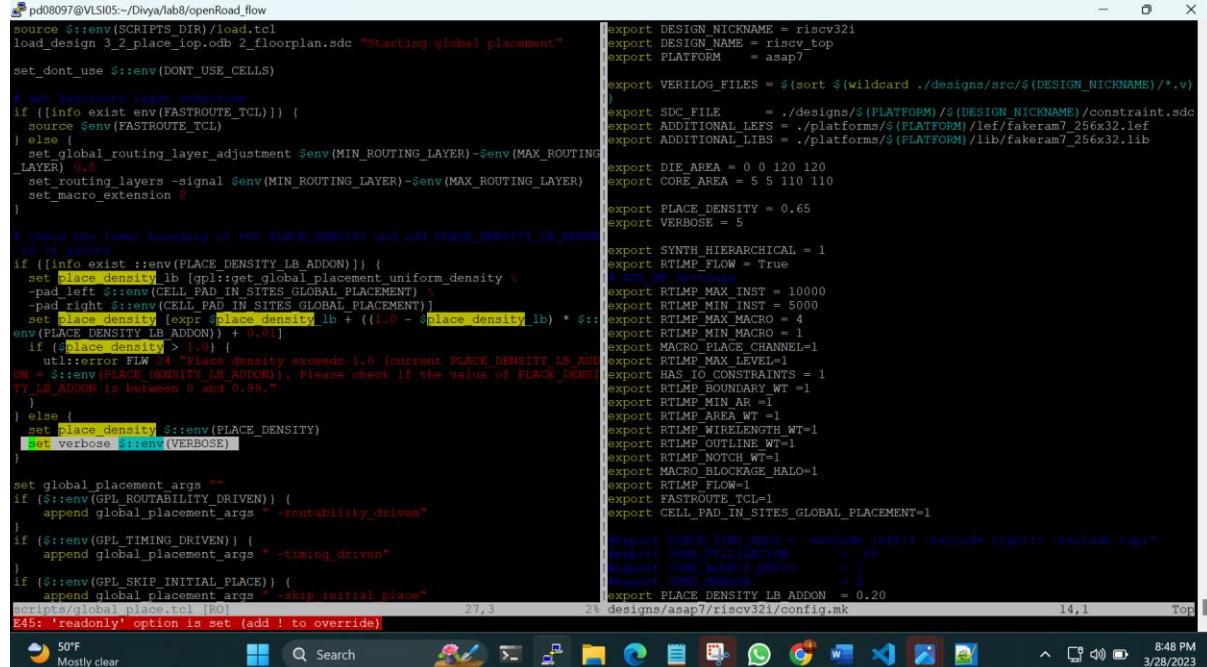


```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
    append global_placement_args "-routability_driven"
}
if ($::env(GPL_TIMING_DRIVEN)) {
    append global_placement_args "-timing_driven"
}
if ($::env(GPL_SKIP_INITIAL_PLACE)) {
    append global_placement_args "-skip_initial_place"
}
if ($::env(GPL_INCREMENTAL)) {
    append global_placement_args "-incremental"
}
if ($::env(GPL_TIMING_DRIVEN_NET_WEIGHT_MAX)) {
    append global_placement_args "-timing_driven_net_weight_max 2"
}
if ($::env(GPL_INITIAL_PLACE_MAX_ITER)) {
    append global_placement_args "-initial_place_max_iter 500"
}
if ($::env(GPL_TIMING_DRIVEN_NETS_PERCENTAGE)) {
    append global_placement_args "-timing_driven_nets_percentage 80"
}

if {[llength [array get ::env GLOBAL_PLACEMENT_ARGS]] } {
    global_placement -density $place_density -verbose
    -pad left $::env(CELL_PAD_IN_SITES_GLOBAL_PLACEMENT)
    -pad right $::env(CELL_PAD_IN_SITES_GLOBAL_PLACEMENT)
    {*}$global_placement_args
} else {
    global_placement -density $place_density -verbose
    -pad left $::env(CELL_PAD_IN_SITES_GLOBAL_PLACEMENT)
    -pad right $::env(CELL_PAD_IN_SITES_GLOBAL_PLACEMENT)
    {*}$global_placement_args
}
estimate_parasitics -placement
source $::env(SCRIPTS_DIR)/report_metrics.tcl
report_metrics "global place" false false
if {[![info exists save_checkpoint] || $save_checkpoint]} {
    write_db $::env(RESULTS_DIR)/3_place_gp.odb
}
"scripts/global_place.tcl" 73L, 2701C written
      50°F Mostly clear          62,53   Bot  8:31 PM  3/28/2023
```

## Experiment #23

Another Modification added verbose argument variable in config.mk for global\_placement command:



```

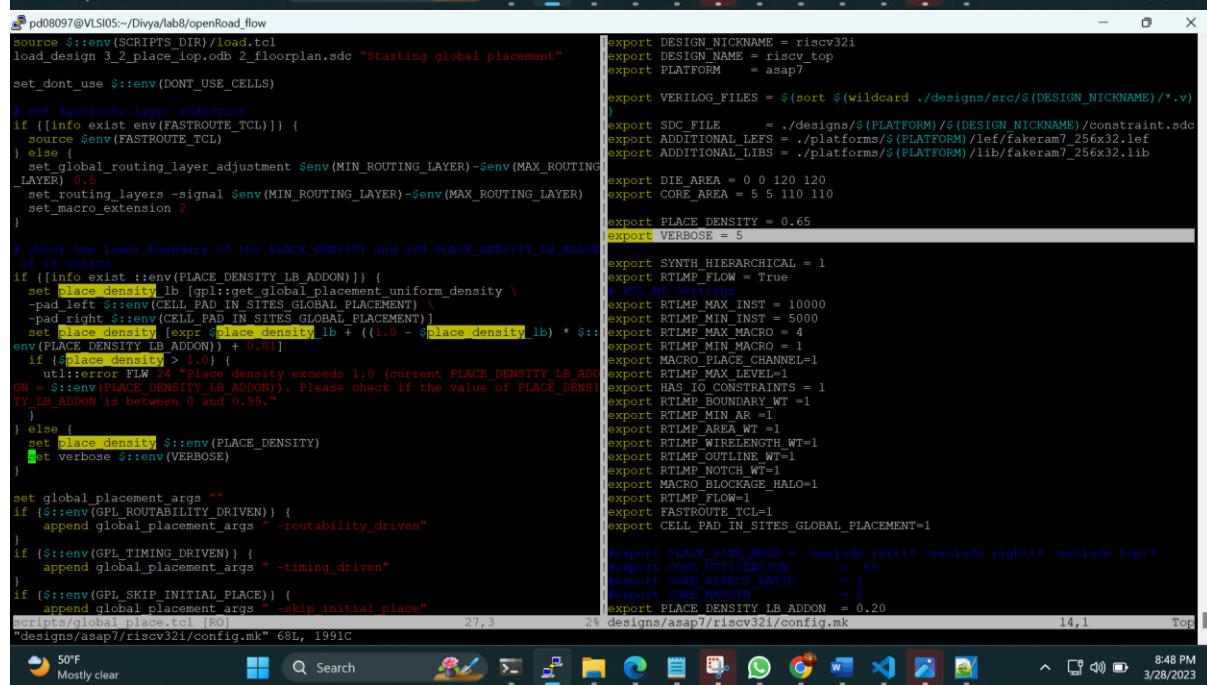
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
source $::env(SCRIPTS_DIR)/load.tcl
load_design 3_2_place_iop.odb 2_floorplan.sdc "Starting global placement"
set _dont_use $::env(DONT_USE_CELLS)

# set fastroute layer reduction
if {[info exist env(FASTRROUTE_TCL)]} {
    source $env(FASTRROUTE_TCL)
} else {
    set_global_routing_layer_adjustment $env(MIN_ROUTING_LAYER)-$env(MAX_ROUTING_LAYER) 0.5
    set_routing_layers -signal $env(MIN_ROUTING_LAYER)-$env(MAX_ROUTING_LAYER)
    set_macro_extension 2
}

# check the lower boundary of the PLACE_DENSITY and add PLACE_DENSITY_LB_ADDON
# if it exists
if {[info exist ::env(PLACE_DENSITY_LB_ADDON)]} {
    set place_density_lb [expr ${::env(PLACE_DENSITY)} * ${::env(PLACE_DENSITY_LB_ADDON)}]
    set place_density [expr $place_density_lb + ((1.0 - $place_density_lb) * ${::env(PLACE_DENSITY_LB_ADDON)} + 0.01)]
    if {$place_density > 1.0} {
        util::error FLW 74 "place density exceeds 1.0 (current PLACE_DENSITY LB ADDON = ${::env(PLACE_DENSITY_LB_ADDON)}). Please check if the value of PLACE_DENSITY_LB_ADDON is between 0 and 0.99."
    } else {
        set place_density $::env(PLACE_DENSITY)
        set verbose $::env(VERBOSE)
    }
}

set_global_placement_args ""
if ${::env(GPL_ROUTEABILITY_DRIVEN)} {
    append_global_placement_args "-routeability_driven"
}
if ${::env(GPL_TIMING_DRIVEN)} {
    append_global_placement_args "-timing_driven"
}
if ${::env(GPL_SKIP_INITIAL_PLACE)} {
    append_global_placement_args "-skip_initial_place"
}
scripts/global_place.tcl [RO]
E45: 'readonly' option is set (add ! to override)

```



```

pd08097@VLSI05:~/Divya/lab8/openRoad_flow
source $::env(SCRIPTS_DIR)/load.tcl
load_design 3_2_place_iop.odb 2_floorplan.sdc "Starting global placement"
set _dont_use $::env(DONT_USE_CELLS)

# set fastroute layer reduction
if {[info exist env(FASTRROUTE_TCL)]} {
    source $env(FASTRROUTE_TCL)
} else {
    set_global_routing_layer_adjustment $env(MIN_ROUTING_LAYER)-$env(MAX_ROUTING_LAYER) 0.5
    set_routing_layers -signal $env(MIN_ROUTING_LAYER)-$env(MAX_ROUTING_LAYER)
    set_macro_extension 2
}

# check the lower boundary of the PLACE_DENSITY and add PLACE_DENSITY_LB_ADDON
# if it exists
if {[info exist ::env(PLACE_DENSITY_LB_ADDON)]} {
    set place_density_lb [expr ${::env(PLACE_DENSITY)} * ${::env(PLACE_DENSITY_LB_ADDON)}]
    set place_density [expr $place_density_lb + ((1.0 - $place_density_lb) * ${::env(PLACE_DENSITY_LB_ADDON)} + 0.01)]
    if {$place_density > 1.0} {
        util::error FLW 74 "place density exceeds 1.0 (current PLACE_DENSITY LB ADDON = ${::env(PLACE_DENSITY_LB_ADDON)}). Please check if the value of PLACE_DENSITY_LB_ADDON is between 0 and 0.99."
    } else {
        set place_density $::env(PLACE_DENSITY)
        set verbose $::env(VERBOSE)
    }
}

set_global_placement_args ""
if ${::env(GPL_ROUTEABILITY_DRIVEN)} {
    append_global_placement_args "-routeability_driven"
}
if ${::env(GPL_TIMING_DRIVEN)} {
    append_global_placement_args "-timing_driven"
}
if ${::env(GPL_SKIP_INITIAL_PLACE)} {
    append_global_placement_args "-skip_initial_place"
}
scripts/global_place.tcl [RO]
"designs/asap7/riscv32i/config.mk" 68L, 1991C

```

## Error :

```
OpenROAD v2.0-6895-g5c85b36
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13178, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13211, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14772, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14805, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14838, timing group from output port.
RTLMF flow enabled. Skipping tdmz place.
Elapsed time: 0:02.23[h]:min:sec. CPU time: user 2.07 sys 0.16 (9%). Peak memory: 171028KB.
(/usr/bin/time -f '%E[h]:min:sec. CPU time: user %U sys %S (%). Peak memory: %MKB.' /usr/openroad/OpenROAD-flow-scripts/tools/install/OpenROAD
/bin/openroad -exit -no_init ./scripts/macro_place.tcl -metrics ./logs/asap7/riscv32i/base/2_4_mplace.json) 2>&1 | tee ./logs/asap7/riscv32i/base/2_4_mplace
.log
OpenROAD v2.0-6895-g5c85b36
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13178, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13211, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13244, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13277, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13310, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13343, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 13376, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14772, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14805, timing group from output port.
[WARNING STA-0164] ./platforms/asap7/lib/asap7sc7p5t_SIMPLE_RVT_FF_nldm_211120.lib.gz line 14838, timing group from output port.
Error: macro_place.tcl: 128 missing function argument at `_@_
in expression "max(1, @_@)"
Elapsed time: 0:02.19[h]:min:sec. CPU time: user 2.03 sys 0.16 (100%). Peak memory: 170852KB.
make: *** [results/asap7/riscv32i/base/2_4_floorplan_macro.odb] Error 1
[pd08097@VLSI05 openRoad_flow]$
```

## Experiment #24

**Commented global placement flags and argument which are added in experiment 23.**

**Power Report in 6\_report.log:**

```
=====
finish report_power
-----
Group           Internal Power   Switching Power   Leakage Power   Total Power (Watts)
-----
Sequential      1.05e-03    5.64e-05    1.58e-07    1.11e-03    11.8%
Combinational   7.31e-03    4.51e-04    5.17e-04    8.28e-03    88.2%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          8.36e-03    5.08e-04    5.17e-04    9.39e-03    100.0%
     89.1%        5.4%        5.5%
```

**Timing Report in 6\_report.log:**

```
=====
finish critical path slack
-----
-37.3019
```

**Design Area Report in 6\_report.log:**

```
=====
finish report_design_area
-----
Design area 2396 u^2 22% utilization.
```

# Experiment #25

## Changed PLACE\_DENSITY =0.75

```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
export DESIGN NICKNAME = riscv32i
export DESIGN NAME = riscv_top
export PLATFORM = asap7
export VERILOG FILES = $(sort $(_wildcard ./designs/src/S(DESIGN NICKNAME)/*.v))
export SDC FILE = ./designs/$(_wildcard ./designs/$(_wildcard ./designs/src/S(DESIGN NICKNAME)/constraint.sdc)
export ADDITIONAL LEFS = ./platforms/$(_wildcard ./platforms/fakeram7_256x32.lef
export ADDITIONAL LIBS = ./platforms/$(_wildcard ./platforms/lib/fakeram7_256x32.lib
export DIE AREA = 0 0 120 120
export CORE AREA = 5 5 100 100
export PLACE DENSITY = 0.75
#export VERBOSE = 5
export SYNTH HIERARCHICAL = 1
export RTLMF FLOW = True
# RTLMF Settings
export RTLMF MAX INST = 10000
export RTLMF MIN INST = 5000
export RTLMF MAX MACRO = 4
export RTLMF MIN MACRO = 1
export MACRO PLACE CHANNEL=1
export RTLMF MAX LEVEL=1
export HAS IO CONSTRAINTS = 1
export RTLMF BOUNDARY WT =1
export RTLMF MIN AR =1
export RTLMF AREA WT =1
export RTLMF WIRE LENGTH WT=1
export RTLMF OUTLINE WT=1
export RTLMF NOTCH WT=1
export MACRO BLOCKAGE HALO=1
export RTLMF FLOW=1
#export FASTROUTE_TCL=1
#export CELL_PAD_IN_SITES_GLOBAL_PLACEMENT=1
#export PLACE PINS ARG = -exclude left: -exclude right: -exclude top:
#export CORE UTILIZATION = 60
#export CORE ASPECT RATIO =
#export CORE MARGIN =
#export PLACE DENSITY LB ADDON = 0.20
export ENABLE DPO = 1
export DFF LIB FILE = $( $(CORNER)_DFF_LIB_FILE )
13,1 Top
49°F Rain 10:31 PM 3/28/2023
```

## Changed Number of Tracks 6 in add\_routing\_blk.tcl

```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
# Create Routing Blockages around Macros for GF12
# Created by Minsoo Kim (mkl226@engr.ucsd.edu)
set db [:;ord::get_db]
set block [$db getChip] getBlock]
set tech [$db getTech]
set layer_M2 [stech findLayer M2]
set layer_M3 [stech findLayer M3]
set layer_C4 [stech findLayer C4]
set numTrack 6
set allInsts [$block getInsts]
set cnt 0
foreach inst $allInsts {
    set master [$inst getMaster]
    set name [$master getName]
    set loc_llx [lindex [$inst getLocation] 0]
    set loc_lly [lindex [$inst getLocation] 1]
    if {[string match "*gf12* $name"] || [string match "IN12LP* $name"]} {
        set w [$master getWidth]
        set h [$master getHeight]
        set llx_Mx [expr $loc_llx - (128*$numTrack)]
        set lly_Mx [expr $loc_lly - (128*$numTrack)]
        set urx_Mx [expr $loc_llx + $w + (128*$numTrack)]
        set ury_Mx [expr $loc_lly + $h + (128*$numTrack)]
        set llx_Cx $loc_llx
        set lly_Cx [expr $loc_lly - (160*$numTrack)]
        set urx_Cx [expr $loc_llx + $w]
        set ury_Cx [expr $loc_lly + $h + (160*$numTrack)]
        set obs_M2 [odb:dbObstruction_create $block $layer_M2 $llx_Mx $lly_Mx $urx_Mx $ury_Mx]
        set obs_M3 [odb:dbObstruction_create $block $layer_M3 $llx_Mx $lly_Mx $urx_Mx $ury_Mx]
        set obs_C4 [odb:dbObstruction_create $block $layer_C4 $llx_Cx $lly_Cx $urx_Cx $ury_Cx]
    }
    incr cnt
}
"scripts/add_routing_blk.tcl" 49L, 1515C
1,1 Top
49°F Rain 10:19 PM 3/28/2023
```

## Error: Macro Tiling Error

```
pd08097@VLSI05:~/Divya/lab8/openRoad_flow
```

```
Print Physical Hierarchy Tree after splitting std cell and macros in leaf clusters
```

```
root (0) num_macro : 4 num_std_cell : 8992 macro_area : 1100.752 std_cell_area : 1074.3816
+---L0 (1) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---L1 (2) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---L2 (3) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---T0 (4) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---T1 (5) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---T2 (6) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---R0 (7) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---R1 (8) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---R2 (9) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---B0 (10) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---B1 (11) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---B2 (12) num_macro : 0 num_std_cell : 0 macro_area : 0.0 std_cell_area : 0.0
+---boot||dmem||pcmux (13) num_macro : 0 num_std_cell : 96 macro_area : 0.0 std_cell_area : 9.09792
+---riscv (16) num_macro : 0 num_std_cell : 8894 macro_area : 0.0 std_cell_area : 1065.1378
+---(root)_glue_logic (17) num_macro : 0 num_std_cell : 2 macro_area : 0.0 std_cell_area : 0.1458
+---dmem/dmem0||dmem/dmem1||dmem/dmem2||dmem/dmem3 (18) num_macro : 4 num_std_cell : 0 macro_area : 1100.752 std_cell_area : 0.0
Determine shaping function for clusters -- Macro Tilings.

[ERROR MPL-0004] This no valid tilings for hard macro cluser: dmem/dmem0||dmem/dmem1||dmem/dmem2||dmem/dmem3
Error: macro_place.tcl, 128 MPL-0004
Elapsed time: 0:03.64 [h]:min:sec. CPU time: user 7.79 sys 0.16 (218%). Peak memory: 189456KB.
make: *** [results/asap7/riscv32i/base/2_4_floorplan_macro.odb] Error 1
[pd08097@VLSI05 openRoad_flow]$ vi
```



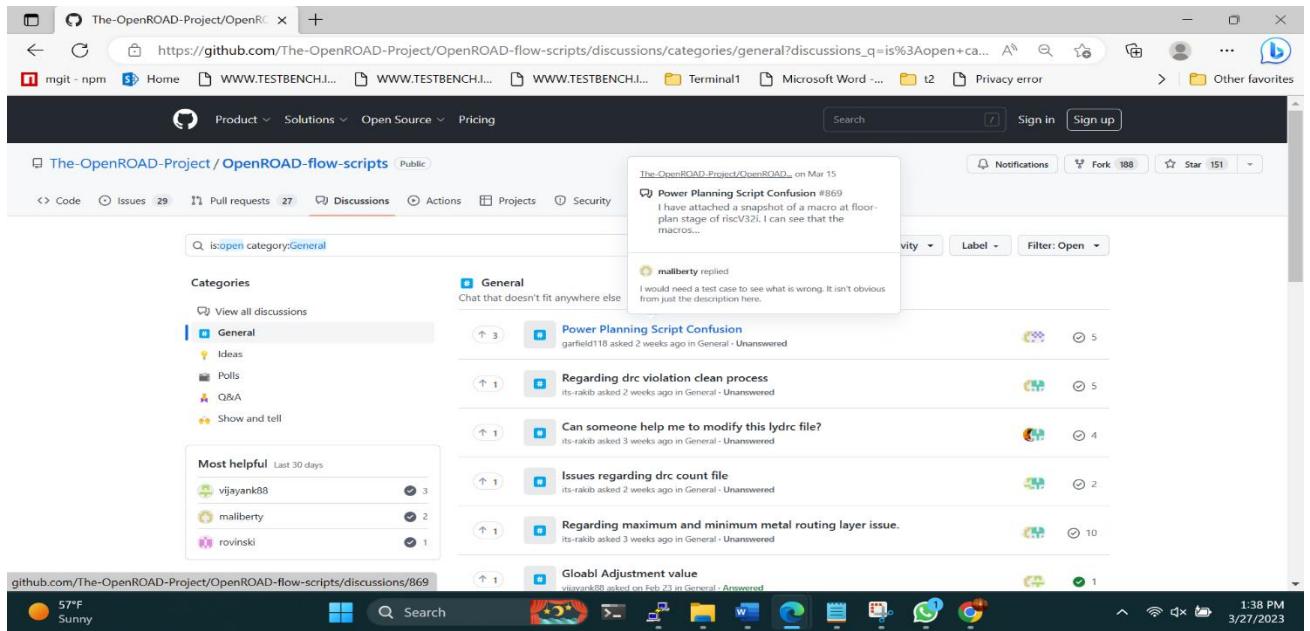
## **MY HOLISTIC UNDERSTANDING FROM THE EXPERIMENTS PERFORMED**

**My Experiment Learnings, and Experience to optimize the riscv32i design.**

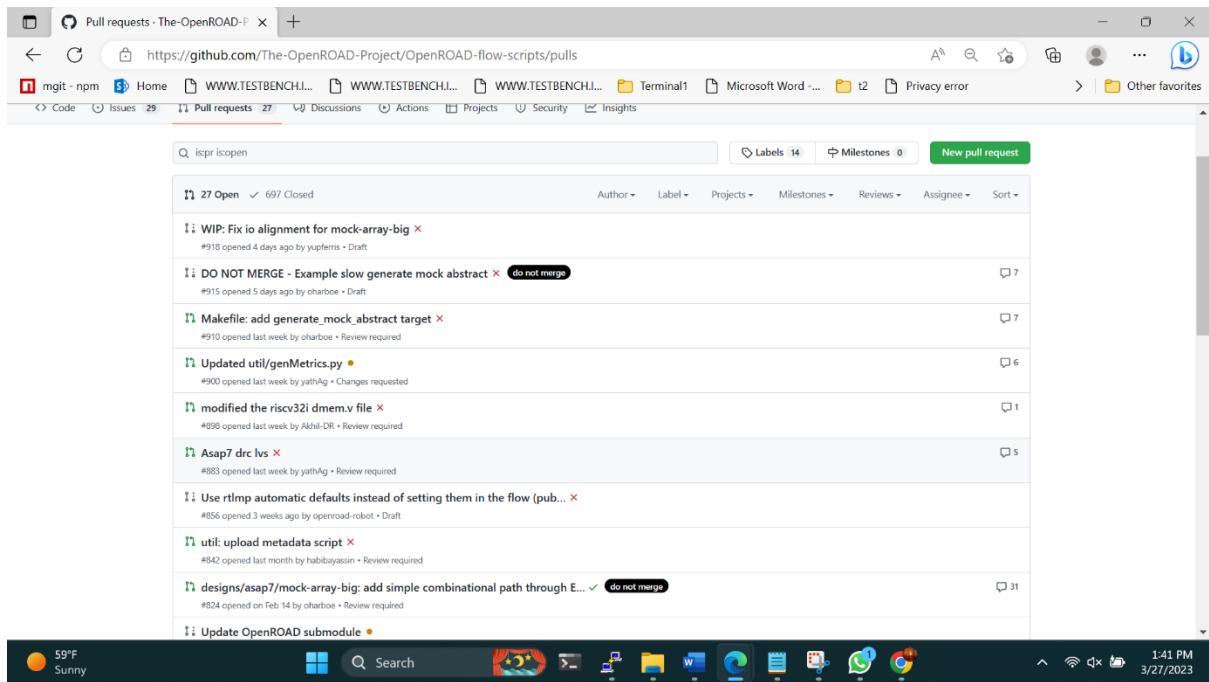
1. Understood the
  - OpenROAD flow scripts,
  - Makefile,
  - directory structure,
  - design constraint and
  - config file.
2. Understood the OpenROAD tcl script commands.
3. Understood OpenROAD github page, issues and discussions.

**My Challenges during the Experiment are following.**

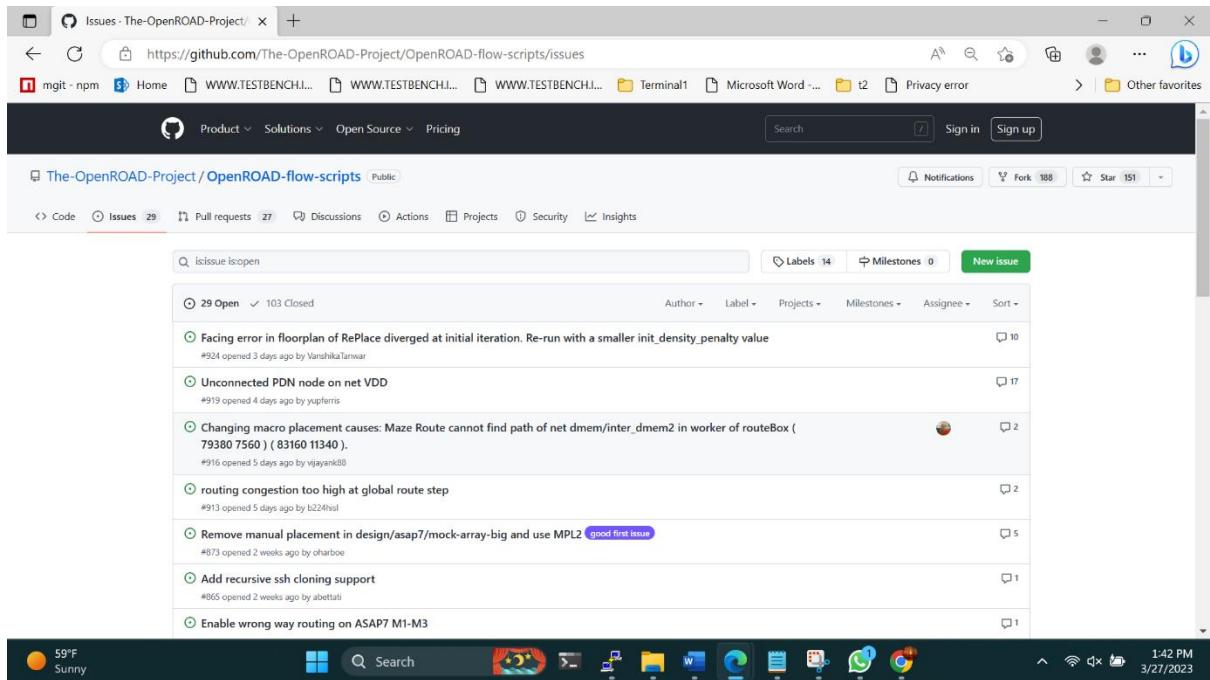
1. Can't see the IO pad rings in gui mode of OpenROAD.
2. Challenging while comparing timing reports of all steps.
3. No man command like synopsys tool to look the description of commands. I try to look into github page in src folder for individual command and description.
4. Make run after clean all is challenging it takes so long to see the small change.
5. Challenging to fix the tool error.
6. Challenging to make changes of core utilization.
7. Challenging to find the location of macros for manual macro placement.
8. Challenging to fix or unfixed the macro placement.
9. Challenging to optimize using global and detail placement step iteration step.
10. Challenging to understand the difference between PLACE\_DENSITY and CORE\_UTILIZATION variables.



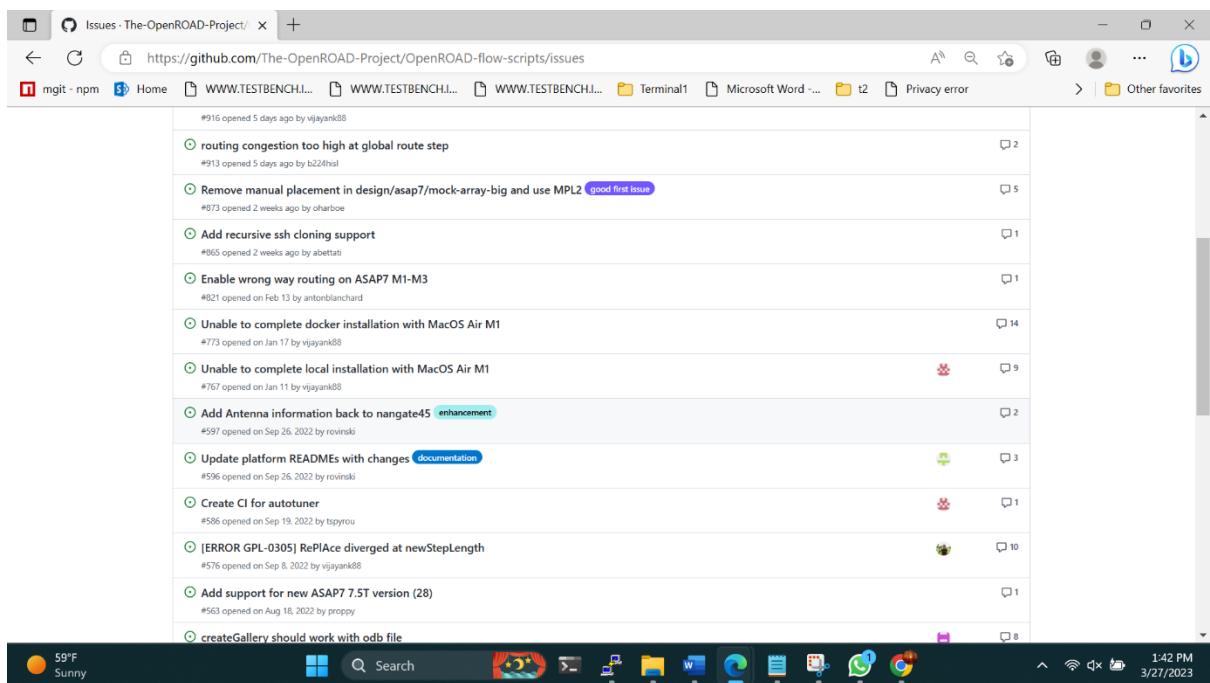
**FIGURE 1: OpenROAD Github Discussion Page.**



**FIGURE 2: OpenROAD Github Pull request Page.**



**FIGURE 3: OpenROAD Github Issues Page.**



**FIGURE 4: OpenROAD Github Issues Page. (Contd.)**

## SNAPSHOT OF GOOD WORKING GEXPERIMENTS

Experiment #	CLK_PERIOD	TOTAL POWER	DESIGN AREA & UTILIZATION	FINISH CRITICAL PATH SLACK
1	1600	9.32e-03	2503 23%	6.57
2	1300	1.13e-02	2522 23%	-77.07
3	1580	9.42e-03	2507 23%	-72.67
4	1000	1.46e-02	2517 23%	-292.40
5	1100	1.33e-02	2515 23%	-242.16
6	1535	9.69e-03	2539 23%	-1684.07
7	1500	9.89e-03	2439 22%	7.07
8	1508	9.84e-03	2437 22%	29.6565
9	1508	9.84e-03	2437 22%	29.6565
10	1508	9.84e-03	2448 22%	26.30
11	1508	9.84e-03	2431 27%	38.52
12	1508 (config.mk)	9.83e-03	2428 28%	3.95
13	1508 (config.mk)	9.38e-03	2387 22%	12.34
14	1508 (cts.tcl)	9.37e-03	2386 22%	-0.861621
15	1508 (cts.tcl)	9.39e-03	2387 22%	8.8917
17	1508	9.39e-03	2387 22%	9.09
18	1508	9.39e-03	2390 22%	21.12
19	1510	9.39e-03	2387 22%	12.59

## SNAPSHOT OF FAILED GEXPERIMENTS

Experiment #	Modification Details Constraint /Config Parameter/tcl script files/ Makefile (clk_period: 1508)	TOTAL POWER	DESIGN AREA & UTILIZATION	FINISH CRITICAL PATH SLACK
16	Constraint clk_period: 1508 (io_placement.tcl)	Make run Failed		
20	Constraint clk_period: 1508 Input delay: 0.09*clk_period Output delay: 0.125*clk_period	9.39e-03	2395 22%	-945.7178
21	Constraint.sdc and global_place.tcl: Global Placement variable arguments defined updated	Make run Failed		
22	Constraint.sdc and global_place.tcl: Added verbose flag in global placement command	Make run Failed		
23	Global Placement variable arguments defined	Make run Failed		
24	Comment Placement variables defined in exp 23.	9.39e-03	2396 22%	-37.30
25	PLACE_DENSITY =0.75 Number of Tracks 6 in add_routing_blk.tcl	Make run Failed		

