DIVYA DARSHAN VR

9092109353 | divyadarshanvr09@gmail.com | Divyadarshanvr | Divyadadarshanvr09 | Portfolio

PROFESSIONAL SUMMARY

Pre-final year ECE student passionate about VLSI and semiconductor design, skilled in Verilog, digital design, and FPGA prototyping, and actively learning ASIC flow and VLSI tools.

EDUCATION

College Of Engineering Guindy,
Anna University – Chennai, Tamil Nadu 2023- Present
Bachelor of Engineering in Electronics and Communication Engineering
CGPA: 8.50 / 10
Relevant Coursework & Knowledge: Digital Electronics, Solid-State Devices, Computer Architecture, Embedded Systems, CMOS, Basics of STA

SKILLS AND INTERESTS

TECHNICAL SKILLS:

- **Programming & HDL:** C, C++, Python, Assembly (8085,8086,8051 & RiscV), Verilog HDL
- **Hardware & Platforms:** FPGA Prototyping, ESP32, Arduino
- **Design Skills:** PCB Design
- **Protocols:** UART, I2C, SPI

TOOLS: Xilinx Vivado, Yosys, Magic, Qflow, OpenSTA, OpenLane, Easy EDA, Arduino IDE, LT Spice, MatLab, Linux, GitHub, GNU Radio, Cisco packet tracer, CST Antenna Design.

PROJECTS

Branch Predictor Enhancement for Shakti C-Class Core | May 2025 – August 2025 |
CEG Fabless x Shakti Processor Team (IITM) x Vyoma Systems (IITM)

- We **Implemented** a Tournament Branch Predictor and **revamped** the existing Bimodal Predictor in the **Shakti C-Class RISC-V core** using **Bluespec SystemVerilog (BSV)** to enhance prediction performance.
- **Integrated** global and local history mechanisms, achieving a **prediction accuracy of 90.36%** and **MPKI of 15.93**, closely matching the optimized **bimodal predictor (90.45%, 15.77 MPKI)** while improving design modularity and scalability.

8-Bit Accumulator Based Processor | Jan 2025 – Sept 2025 |
CEG Fabless Initiative (Alumni-Student Forum):

- We **Designed and implemented** an **8-bit Accumulator-Based Processor** using **Verilog**, integrating a modular **ALU**, **Control Unit**, and **Register File** for basic instruction execution.
- **Completed full ASIC flow** and **successfully submitted** the design to the **TinyTapeout foundry (eFabless)** using the **Sky130 PDK**, achieving **74.23% area utilization**, ensuring efficient layout and timing closure.

ONGOING PROJECT

INDIA RISC-V SoC CHIP TAPEOUT | By VLSI System Design & IIT Gandhinagar |Sept 2025 – Present |

- **I'm a part of a 20-week RISC-V SoC Tapeout Program**, gaining hands-on experience with **Synopsys EDA tools** and **SCL 180nm PDK**.
- **Covered synthesis, STA**, and labs related to it. Currently focused on **Floorplanning** and **PnR** and documentation is maintained in Github.

INTERNSHIP EXPERIENCE

RISC –V Design Intern | May 2025 – August 2025
CEG Fabless, Anna University | In collaboration with Vyoma Systems and Shakti Processor Group, IIT Madras

- Completed 4-week intensive training covering RISC-V privileged and unprivileged specifications, CSR operations, debugging, cocotb-based verification, and Shakti C-Class architecture.
- Contributed to a 4-week project phase, applying RISC-V knowledge to implement Tournament Branch predictor for shakti's C-Class.

IOT DEVELOPER INTERN | July 2024 – August 2024 |
Centre for Entrepreneurship Development, Anna University, Chennai

- Developed a smart IV bag monitoring system using IoT technologies to track fluid levels and alert medical staff in real time**.**

ACHIEVEMENTS AND CERTIFICATIONS

- CMOS Digital VLSI Design | NPTEL | IIT Kharagpur | **Silver Medal** and ranked in the **Top 5%** of course participants. |
- Winner of Robo Soccer Event in "RESONANCE'25' an Intra College Event. |
- 4x Times **State Level Champion** in 110mts Hurdles | 2022-2024
- Silver Medalist in **South zone Junior National** Athletic Championship | Guntur, AP| 2022

LEADERSHIP AND EXPERIENCE

IEEE – ELECTRON DEVICES SOCIETY CEG, *SECRETARY* *2025- Present*
Assisted in organizing events and workshops for students

ECEA – ORGANIZING SECRETARY *2025- Present*
Head of Non-Technical Domain and responsible for conducting events.

ECEA – JOINT SECRETARY *2024- 2025*
Assisted in conducting Non-Technical event for students.