VIT UNIVERSITY
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VELLORE ▪ CHENNAI
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SCHOOL OF ELECTRICAL ENGINEERING

LAB MANUAL / RECORD

On

EEE 4028

VLSI DESIGN

LABORATORY

(Fall Semester -2017-18)

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Register Number: **15BEE0174**

LAB SLOT: L23+L24

This work is submitted in partial fulfilment of the requirement of the award of the degree of Bachelor of Technology in EEE.

Internal Examiner

External Examiner

Objectives:

- To provide students with the background needed to design, develop, and test digital arithmetic circuits using IEEE standard Verilog HDL.
- To provide an understanding complex arithmetic circuit design principle and its architecture design.

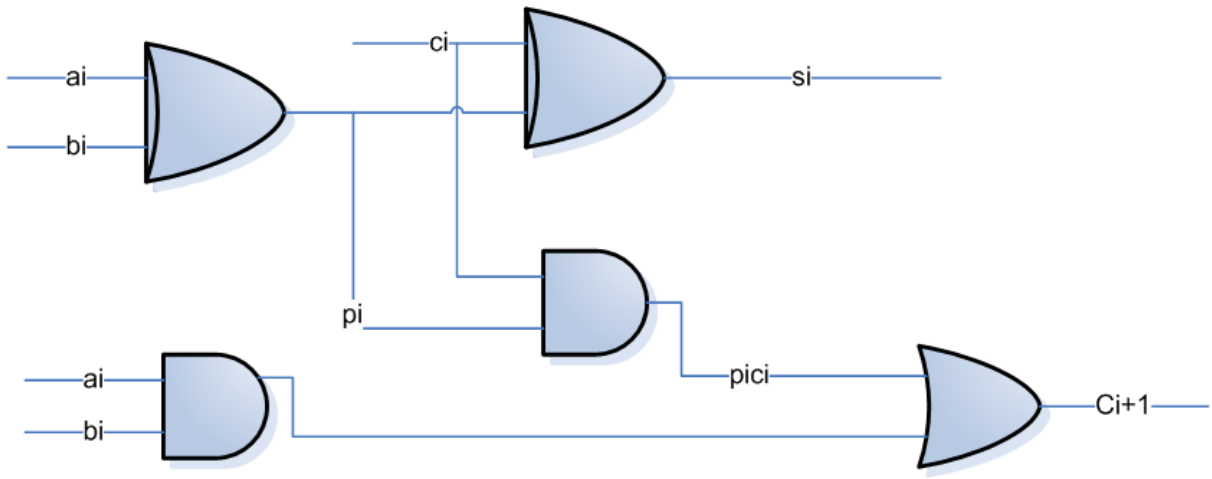
Outcomes:

- After completion of this course the students will be familiar with design and implementation of Digital Arithmetic building blocks using Verilog HDL and Xilinx FPGA Design Flow.

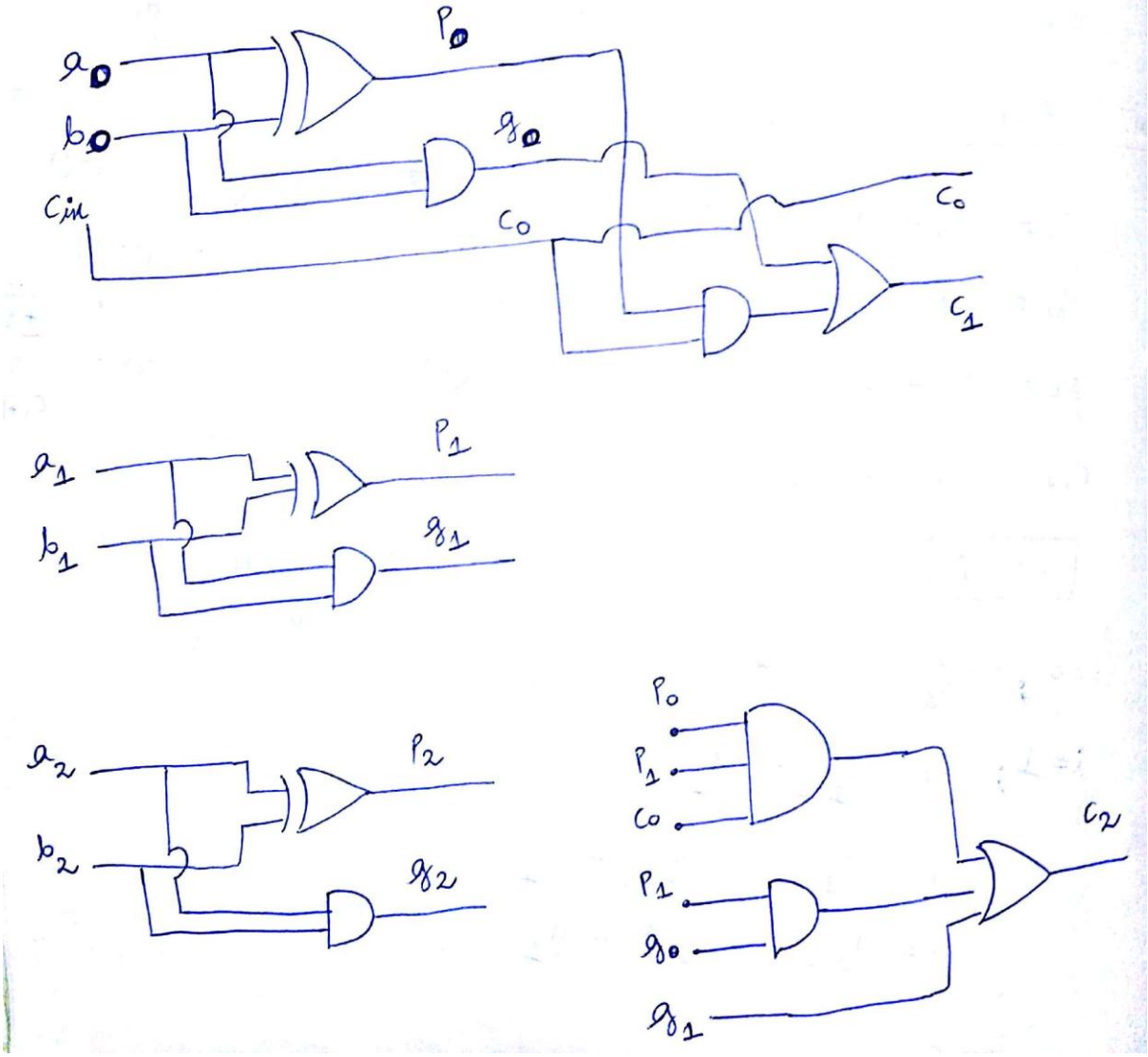
EXPT 2: 4-BIT CARRY LOOK AHEAD ADDER

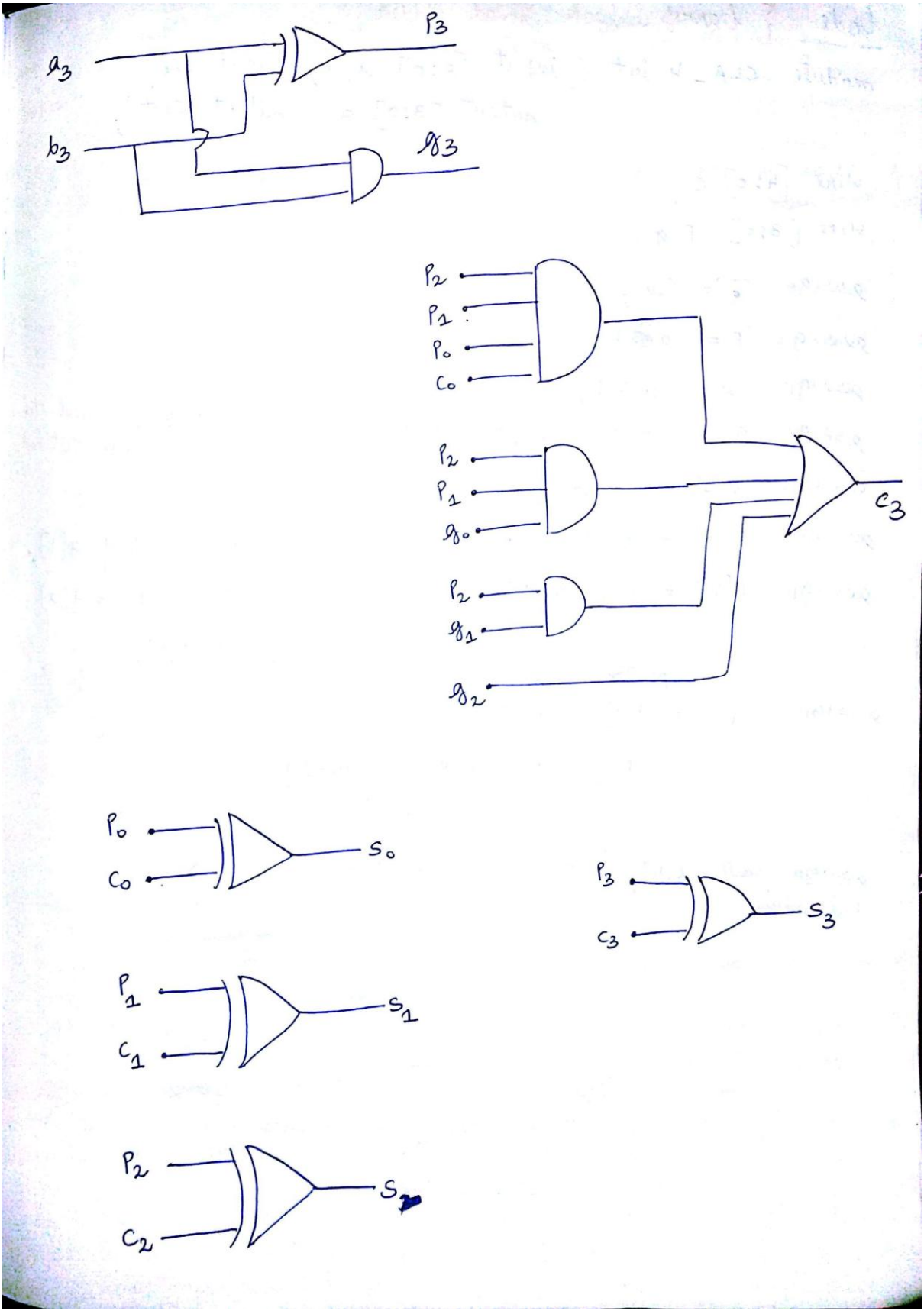
Objective: To design, implement and test a 4-bit CARRY LOOK AHEAD ADDER circuit.

Circuit Diagram:



Logic Gate Diagram:




a_3
b_3
P_3
g_3
P_2
P_1
P_0
C_0
P_2
P_1
g_0
P_2
g_1
g_2
C_3
P_0
C_0
S_0
P_1
C_1
S_1
P_2
C_2
S_2
P_3
C_3
S_3

DESIGN CODE:

```
module CLA(
   input [3:0] a,
   input [3:0] b,
   input cin,
   output [3:0] s,
   output cout
   );

wire [4:0] c;
wire [3:0] p,g;
assign c[0]=cin;
assign p= a^b;
assign g= a&b;
assign s= p^c[3:0];
assign c[1] = (p[0]&c[0])|g[0];
assign c[2] = (p[1]&p[0]&c[0])|(p[1]&g[0])|g[1];
assign c[3] = (p[1]&p[0]&p[2]&c[0])|(p[1]&p[2]&g[0])|(p[2]&g[1])|g[2];
assign c[4] = (p[3]&p[1]&p[2]&p[0]&c[0])|(p[1]&p[2]&p[3]&g[0])|(p[2]&p[3]&g[1])|(p[3]&g[2]|g[3]);
assign cout = c[4];
endmodule
```

TEST BENCH CODE:

```
module CLA_4bit;
	// Inputs
	reg [3:0] a;
	reg [3:0] b;
	reg cin;
	// Outputs
	wire [3:0] s;
	wire cout;
	reg [4:0] check;
	CLA uut (
		.a(a),
		.b(b),
		.cin(cin),
		.s(s),
		.cout(cout)
	);
		// Initialize Inputs
		initial repeat(20) begin
		a=$random;
		b=$random;
		cin=$random;
		check = a+b+cin;
		// Wait 100 ns for global reset to finish
		#10 $display($time,"%d+%d+%d=%d(%d)",a,b,cin,{cout,s},check);
	 end
    endmodule
```

RESULT:

Successfully designed, implemented and tested CARRY LOOK AHEAD ADDER circuit using Xilinx ISE tool.

Device utilization summary:

Selected Device: 3s500efg320-4

Number of Slices: 4 out of 4656 0%

Number of 4 input LUTs: 8 out of 9312 0%

Number of IOs: 14

Number of bonded IOBs: 14 out of 232 6%

Partition Resource Summary:

No Partitions were found in this design

Timing Summary:

Speed Grade: -4

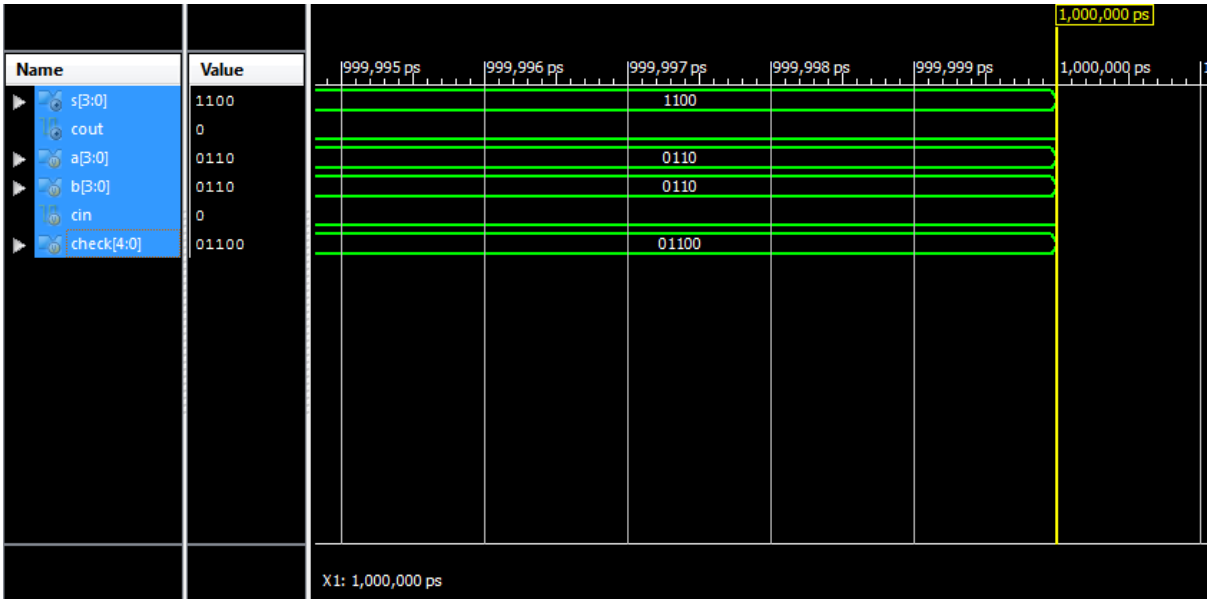
Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.838ns

OUTPUT:



10 4+ 1+1= 6(6)
20 3+13+1=17(17)
30 5+ 2+1= 8(8)
4013+ 6+1=20(20)
5013+12+1=26(26)
60 6+ 5+0=11(11)
70 5+ 7+0=12(12)
8015+ 2+0=17(17)
90 8+ 5+0=13(13)
10013+13+1=27(27)
110 3+10+0=13(13)
120 0+10+1=11(11)
130 6+ 3+1=10(10)
140 3+11+1=15(15)
150 2+14+1=17(17)
16015+ 3+0=18(18)
17010+12+0=22(22)
18010+ 1+0=11(11)
190 8+ 9+1=18(18)
200 6+ 6+0=12(12)

Lab Work: Carry Look Ahead Adder

3/8/17. Verilog Test Fixture (Exp-2)

```
module CLA_4bit;

reg [3:0] a;
reg [3:0] b;

wire [3:0] s;
wire cout;
reg [4:0] check;

CLA uut (
        .a(a)
        .b(b)
        .cin(cin)
        .s(s)
        .cout(cout)
);

initial repeat(20) begin
 a = $random;
 b = $random;
cin = $random;
check = a+b+cin;
#10 $display($time, "%d + %d + %d = %d(%d)",
                a, b, cin, {cout,s}, check);

end
endmodule
```

3/8/17