Power-optimized NORA Multiplexer using charge recycling

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Abstract. In the realm of digital circuitry, efficient power usage stands as a critical factor ensuring both operational efficiency and minimized energy consumption. Within digital circuits, the multiplexer, a fundamental component, facilitates the selection of a specific input signal from several options based on control signals. The focus on energy efficiency has led to considerable interest in multiplexer design, with the CMOS logic style gaining prominence due to its inherent benefits, including low static power dissipation, robustness against voltage fluctuations, and efficient layout.

Over recent decades, researchers have been dedicated to enhancing CMOS multiplexer performance through innovative designs and optimization methodologies. This paper specifically delves into a power-optimized CMOS multiplexer design that leverages charge recycling principles. The primary aim of charge recycling is to curtail power consumption by reutilizing stored charge within the multiplexer's internal nodes during its operational cycles. By employing a power-clock generator utilizing a stepwise charging mechanism, this approach efficiently recycles and redistributes charge within the multiplexer. The adoption of minimum-sized transistors, utilizing TSMC 180nm CMOS technology in our design, further bolsters power optimization. To gauge efficiency, our study conducts a comparative analysis between the power-optimized CMOS multiplexer design and the standard NORA dynamic design, evaluating their respective performance merits.

KEYWORDS

Charge recycling, Power Optimization, Dynamic Circuit, Multiplexer.

INTRODUCTION

Multiplexers, often denoted as "MUX," stand as fundamental digital circuits indispensable in electronics and computer systems [1]. Their pivotal role lies in data routing and selection, enabling the conveyance of numerous input signals through a solitary output line. Such versatility renders them integral in diverse domains, encompassing telecommunications [2], computer memory systems, and data processing units [3]. Structurally, a multiplexer comprises multiple input lines (n inputs), one or more select lines (control inputs), and a sole output line. The quantity of input lines correlates with 2^n, where 'n' denotes the number of select lines, dictating the transmission of data from the chosen input line to the output.

A multiplexer circuit can be designed using multiple design methodologies such as pass transistor logic, static CMOS logic, ratioed CMOS logic, and dynamic CMOS logic. Each one of these design styles has its circuit designs. However, static CMOS logic and dynamic CMOS logic have replaced the remaining design methodologies due to simple design and low power consumption as compared to the remaining methodologies [4]. The choice between static CMOS and dynamic CMOS depends on various factors, including power consumption requirements, speed

considerations, area constraints, noise immunity needs, and the specific application's demands. Designers select the appropriate CMOS type based on these factors to achieve the best trade-offs between performance, power consumption, and area efficiency for a given integrated circuit design. Dynamic CMOS designs are used extensively in applications that require higher speed and higher density, such as high-speed digital signal processing, memory designs (especially DRAM), and applications where area efficiency is more crucial than static power consumption.
In Multiplexer design, A dynamic circuit offers high speed, reduced size, and the ability to expand without affecting the overall design. Hence making it the ideal design style for these circuits.
The paper is organized as follows. In Section II, the principles of the NORA Multiplexer design are examined while in Section III, the new recycling technique is introduced and the operation of the circuit is analyzed. Finally, in Section IV, simulation results on two case studies are presented and in Section V the conclusions are drawn.

NORA MULTIPLEXER DESIGN

NORA logic, a design technique for multiplexers in dynamic CMOS circuits, avoids race conditions and works well in circuits with multiple stages (pipelined circuits)[5]. In this design style, NORA logic is structured using cascaded networks of nMOS and pMOS dynamic logic that conclude on latches, as depicted in Fig.1. The operation of the circuit involves two phases: precharge and evaluation, governed by clock signals clock(phi) and its complement clock_bar(phi'). In the precharge phase, the clock signal (phi) is at a low state (0), causing capacitor C1 to charge to a high voltage (VDD) and capacitor C2 to discharge to a low voltage (0). At the positive cycle of the clock, the pre-charging PMOS (M_{P1}) and predischarging NMOS (M_{P2}) get turned off and the state of the capacitor C1 is determined by the logical function of the n circuit, while the state of capacitor C2 is determined by its inverse.

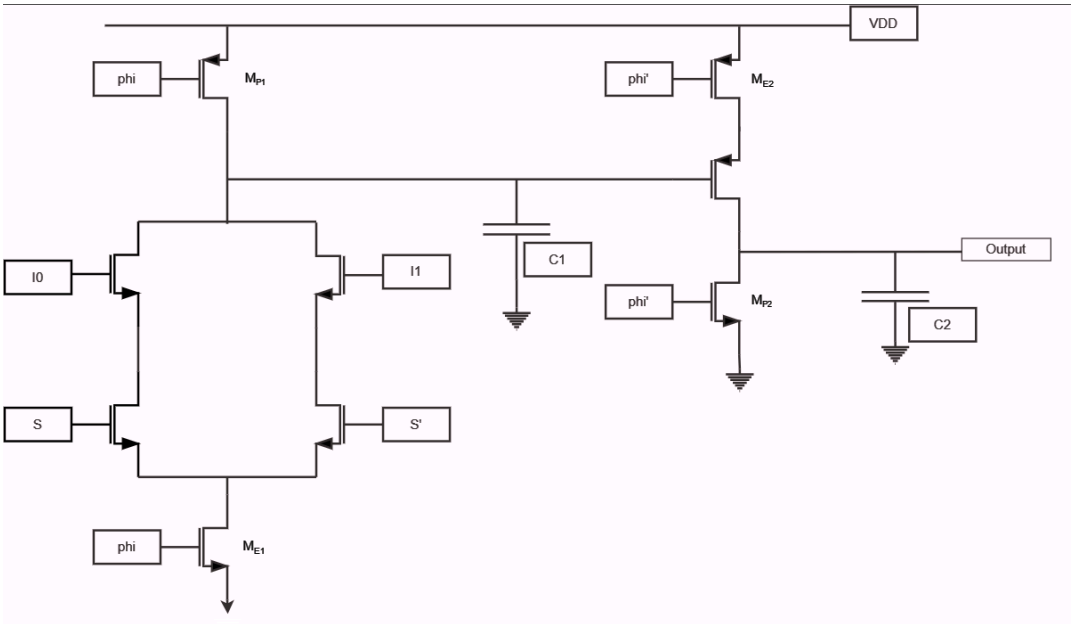

Fig 1 - NORA CMOS Multiplexer

Throughout a cycle, the circuit exhibits zero static power dissipation owing to the minimal leakage current in the 180nm technology [6]. However, the total power dissipation primarily stems from dynamic power dissipation.

In this circuit, the aggregate power dissipation can be computed by accounting for the power dissipation during a precharge and the subsequent ecycle valuation cycle. The energy linked to this power dissipation (E) is expressed as follows:

$$E = Ep + En = C_1 V_{DD}^2 + C_2 V_{DD}^2$$

As seen from the above equation, in each precharge phase, the capacitors C1 and C2 may have to make a low to high and high to low transitions respectively. This constant charging and discharging during the precharge phase contributes significantly to the energy dissipation in the device. Towards that end, a solution needs to be arrived upon to redistribute the excess energy within the capacitors before a precharge phase to reduce the charging/discharging voltage to further reduce the energy dissipation.

CHARGE RECYCLING TECHNIQUE

The design of charge recycling (illustrated in Fig 2) integrates a conditional switch that operates selectively, activating after each evaluation phase and before each subsequent precharge phase. Introducing an additional phase between evaluation and precharge phases (as depicted in Fig 3), known as the "recycle phase," allows for variable durations, potentially ranging from zero to any desired time interval [7]. To enable this functionality, an additional clock signal (PHI_M) and its complement (PHI_MB) are utilized, as shown in Fig 3. PHI_M shares the same period as PHI_M but exhibits a higher duty cycle, as indicated. The extension of PHI_M's duty cycle corresponds to the duration of the recycle phase. During a recycling phase following an active evaluation phase, the switch remains in the "on" state exclusively.

Following an active evaluation phase, the output of the first gate discharges to ground through its nMOS network, while the output of the second gate charges through its pMOS network. Consequently, upon activation of the SW switch, controlled charge sharing occurs between these outputs. Charges migrate from the second gate's output (operating at a high potential and slated for discharge in the subsequent precharge phase) to the first gate's output (operating at a lower potential and to be charged in the following precharge phase). This process allows a portion of the charge used during an active evaluation phase to be recycled and utilized in the subsequent precharge phase, potentially leading to energy savings in circuit operation [8].

To delve further, after an active evaluation phase, only C2 retains a charge equivalent to VDD, representing the total charge stored in the circuit output nodes. Allowing the necessary duration for a complete recycle phase, which equalizes the voltages on both output nodes to Veq through charge sharing, the charges on C1 and C2 become Q1 and Q2, respectively. This is mathematically defined by the following equations [8]:

$$C_2 V_{DD} = Q_1 + Q_2$$

$$Q_1 = C_1 V_p$$

$$Q_2 = C_2 V_p$$

and consequently,

$$V_{eq} = \frac{C_2 V_{DD}}{C_1 + C_2}$$

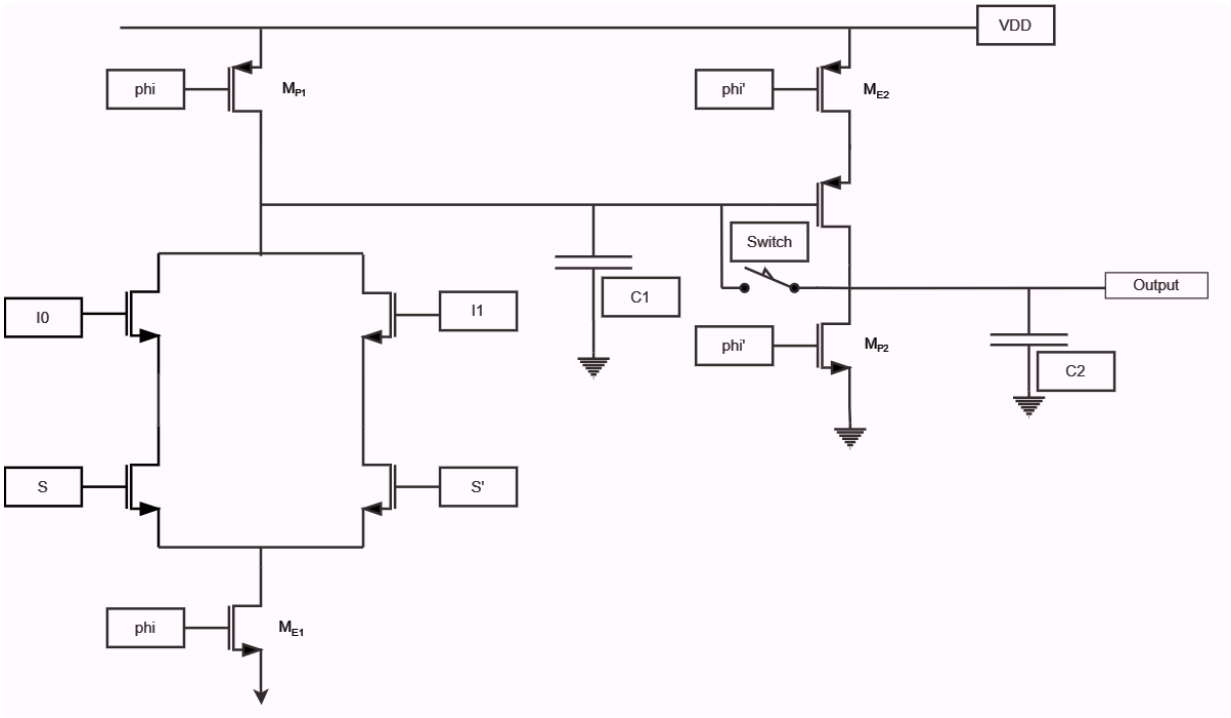

Fig 2 - NORA CMOS Multiplexer with Switch

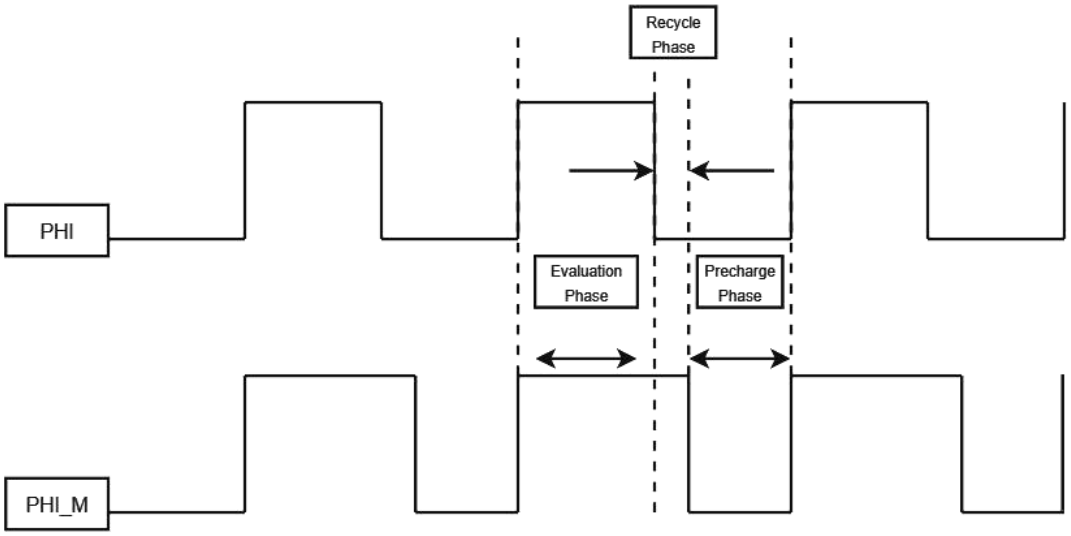

Fig 3 - Waveform for modified clocks

Subsequently, during the following precharge phase, the output of the first gate will transition from Gnd to VDD, and simultaneously, the output of the second gate will shift from VDD to Gnd [8]. The energy dissipation (E) by the first gate within a clock cycle involving an active evaluation phase comprises the energy utilized to switch a bit, discharging its output from VDD to Gnd during the evaluation phase, along with the energy required to recharge the node from Gnd to VDD during the subsequent precharge phase, formulated as [8]

$$E_n^i = \frac{C_1 V_{DD}^2}{2} + \frac{V_{DD}}{2}\int_{V_{eq}}^{V_{DD}} C_1 V_{DD}.dv = \frac{2C_1^2+C_1C_2}{2(C_1+C_2)}V_{DD}^2$$

$$E_p^i = \frac{C_2 V_{DD}^2}{2} + \frac{V_{DD}}{2}\int_{0}^{V_{DD}} C_p.dv = \frac{2C_2^2+C_1C_2}{2(C_1+C_2)}V_{DD}^2$$

$$E_{total}^i = E_P^i + E_n^i = \frac{C_p^2+C_x^2+C_pC_x}{2(C_p+C_x)}V_{DD}^2$$

Energy Density Factor ***α***

$$\alpha = \frac{E - E_{total}^i}{E} = \frac{C_P.C_x}{(C_P+C_x)^2}\text{,,,,,,,,}$$

To serve this purpose, a recycling switch denoted as SW, consisting of a diode-connected transistor (M5) in conjunction with a pass transistor (M6), is employed, as illustrated in Figure 4. The diode-connected transistor regulates the direction of charge flow, allowing charge transfer exclusively from the charged output node of the second gate to the discharged output node of the first gate [7]. Additionally, the pass transistor responds to the complementary clock signal, PHI_MB, ensuring that charge transfer occurs after the active evaluation phase, rather than during it. In cases where a recycling phase is introduced between the evaluation and precharge phases in the circuit's operation, the modified clock signals, PHI_M and its complementary signal PHI_MB, are utilized to control transistors M1 and M4, respectively, based on the signal waveforms delineated in Figure 3.

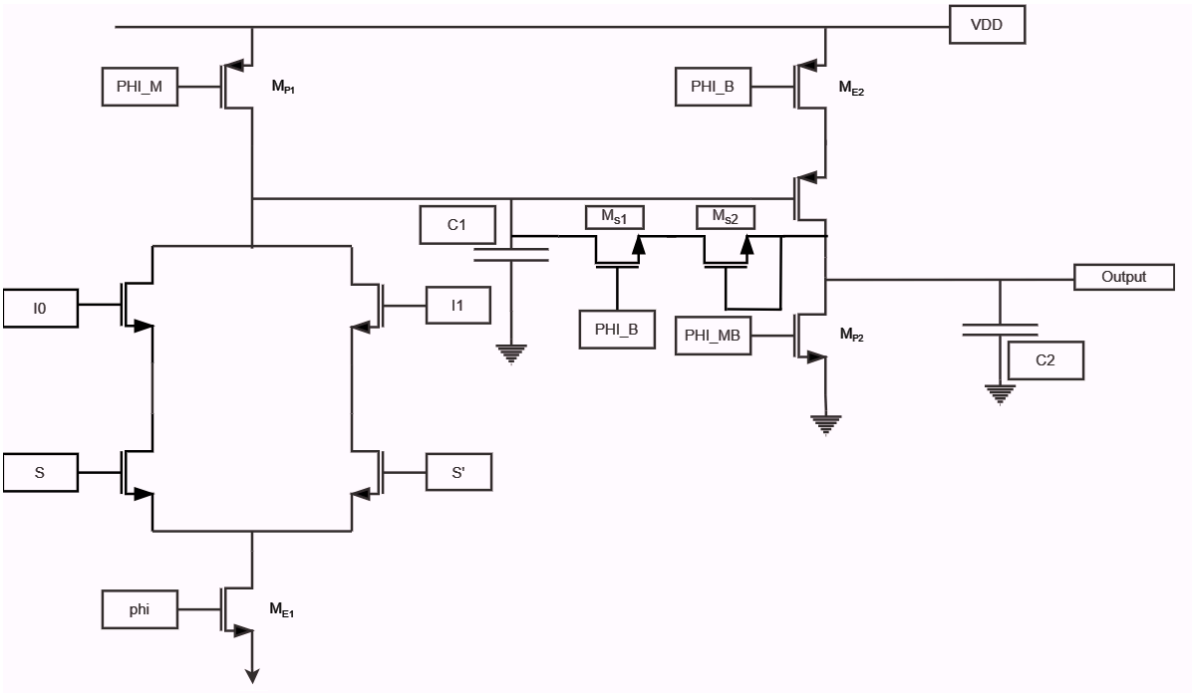

Fig 4 - NORA CMOS Multiplexer with diode connected switch

SIMULATION

The LTSpice simulations for the 2X1[8] and 4X1 charge-recycled NORA multiplexer circuits have been presented in the given segment. The circuits were implemented using 180 nm CMOS technology parameters. A supply voltage of 1 V was chosen, and considering a Vswing of 1 V, Vdd - Vswing is equal to 0 V. Additionally, the load capacitance (CL) was set to 1 nF.

2X1 Multiplexer

2X1 multiplexer circuit with charge recycling is simulated on LTspice (Figure 5) and has the following signals-

1.) sel- selection voltage, maximum voltage- 1V
2.) Clk- Clock signal, maximum voltage- 1V, time period- 2ms
3.) Clkm- recycle clock signal, maximum voltage- 1V, time period-2ms
4.) I0- Select line 0, maximum voltage- 1V
5.) I1- Select line 1, maximum voltage- 1V
6.) Out- output voltage

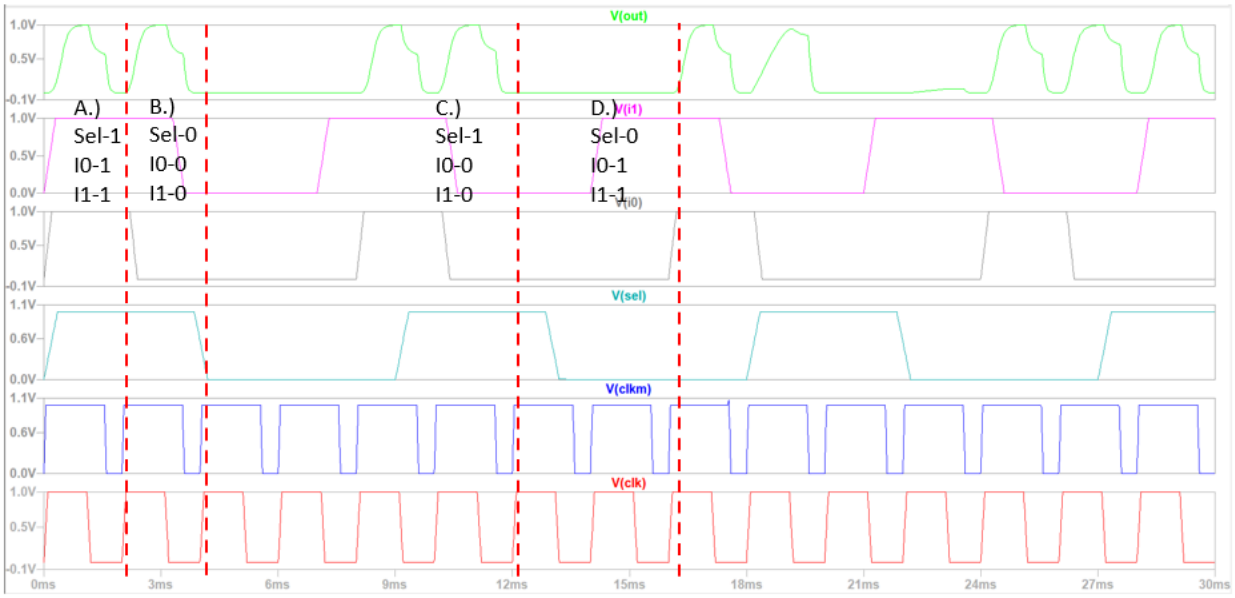

Fig 5 - 2X1 Mux with charge recycling

The circuit has been functionally verified using the different input case patterns and matched with their desired output.

4X1 Multiplexer

4X1 multiplexer circuit with charge recycling is simulated on LTspice (Figure 6) and has the following signals-

1.) Sel0- selection voltage 1, maximum voltage- 1V

2.) Sel1- selection voltage 2, maximum voltage- 1V
3.) Clk- Clock signal, maximum voltage- 1V, time-period- 2ms
4.) Clkm- recycle clock signal, maximum voltage-1V, time-period-2ms
5.) I0- select line 1, maximum voltage- 1V
6.) I1- select line 2, maximum voltage- 1V
7.) I2- select line 3, maximum voltage- 1V
8.) I3- select line 4, maximum voltage- 1V

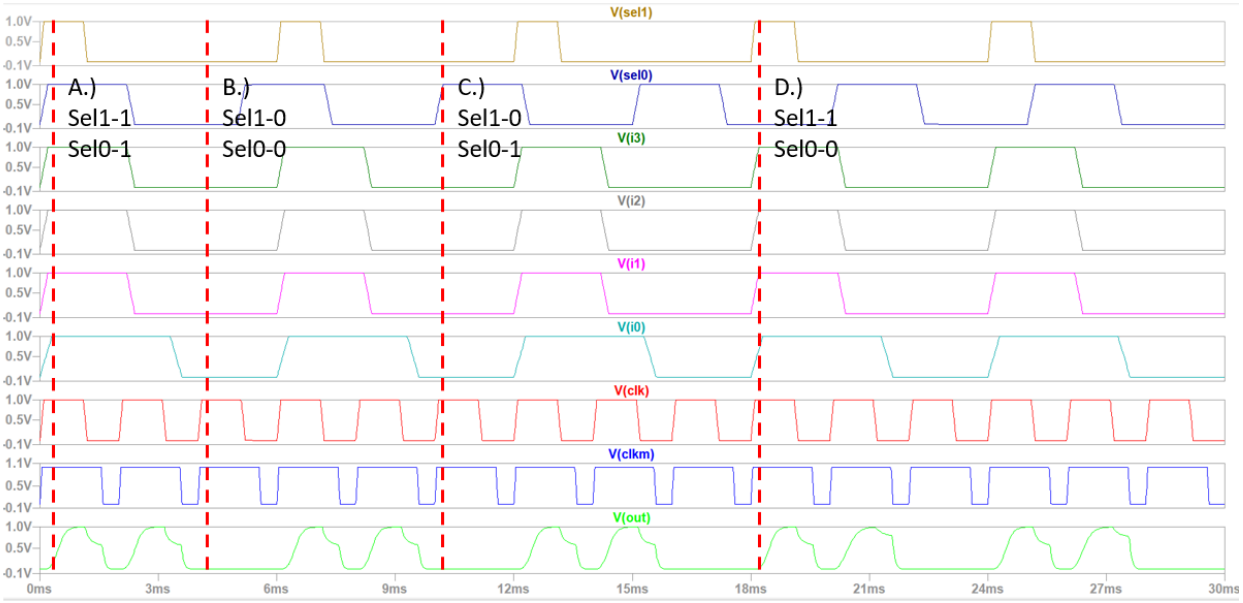

Fig 6 - 4X1 mux with charge recycling

The circuit has been functionally verified using the different input case patterns and matched with their desired output.

PERFORMANCE ANALYSIS

We designed multiple 2X1 and 4X1 multiplexer circuits using both NORA CMOS [9] and NORA CMOS with charge recycling design styles in LTspice, utilizing 180nm CMOS technology. To ensure a comprehensive comparison of circuit performance, we also implemented Domino dynamic logic. In our simulations, we maintained Vswing at 1V, VDD at 1V, and CL at 1nF. The obtained data, including Delay, Power, and the count of transistors, are organized in Table 2 for analysis.

Table 1 - Parameter comparison for various designs

Digital block	Delay(ps)	Power (uW)	No. of Transistors
2X1 Mux (Domino)	330.2	1.842	15
2X1 Mux (NORA)	249.1	0.997	13
2X1 Mux (charge recycling)	270.03	0.790	17
4X1 Mux (Domino)	443.7	2.578	25
4X1 Mux (NORA)	358	1.692	23
4X1 Mux (charge recycling)	364	1.250	27

Our comparison analysis showcases that NORA with charge recycling design style has a drastic improvement over its other dynamic counterparts such as Dynamic Domino logic and NORA. NORA with charge recycling design style demonstrates significant enhancements in power dissipation and delay, with improvements of up to 45.78% and 20.7% respectively compared to Domino dynamic CMOS and NORA logic styles. Additionally, in terms of power-delay product (PDP), it showcases remarkable gains of 63.33% and 30.42% over the same comparison.

CONCLUSION

In conclusion, this study presents a novel low-power design methodology tailored for the NORA Multiplexer circuit. Through the integration of a charge recycling methodology, a unidirectional charge transfer topology, and a novel clocking technique, our proposed technique enables the effective recycling of charge across operational phases. This strategic reuse not only minimizes the energy demand for circuit operation but also contributes to a sustainable and energy-efficient design paradigm.

Moreover, the introduced clocking scheme proves to be highly effective in eliminating short-circuit currents, further enhancing the overall reliability of the NORA Multiplexer circuit. Through comprehensive simulation results conducted on a circuit implemented with 0.18-m CMOS technology, we have substantiated the efficacy of our approach. The findings reveal minimal delay penalties, highlighting the practical viability of our design strategy.

In essence, this research marks a significant stride towards achieving low-power, energy-efficient circuits, addressing the growing need for sustainable electronic systems. The observed decrease in the energy-delay product highlights the practical viability and considerable potential of our proposed methodology for advancing the current state-of-the-art in circuit design. As we navigate towards a future characterized by increasing energy constraints, our

innovative approach holds promise for contributing to the development of greener and more sustainable electronic technologies.

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