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ORIGINAL RESEARCH

A novel single-ended 9T SRAM cell with write assist and decoupled read path for efficient low-voltage applications

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Abstract In this work, a novel single ended single port Write Assist Read decoupled (WARD) 9T SRAM bitcell is proposed to enhance improved write latency. The design incorporates a low threshold (V_{TH}) write access transistor and leverages virtual ground (VGND) assist for low voltage operation at 32 nm CMOS technology node. It demonstrates notable improvements in write delay over conventional SRAM bitcells. At V_{DD} = 0.6 V, the WARD 9T cell offers reduced write'1' delay and write'0' delay. Additionally, WARD 9T cell demonstrates a substantial reduction in read delay and bitline leakage attributed to the stacked configuration for n-type transistors.

Keywords Low power · SNM · Variation tolerant · 9T cell

1 Introduction

In light of technological advancements, the proliferation of smart devices, and the widespread adoption of internet of things (IoT) across various industries, there is a burgeoning need for energy efficient architectures. Particularly in applications like wireless sensing networks (WSN) [1], where sensors continuously monitor environmental activities and transmit data wirelessly, energy consumption becomes a critical concern, necessitating extended battery life. To address this, there has been a considerable focus on the design of low-power static random access memory (SRAM) circuits [2, 3].

Over the past few decades, scaling down complementary metal oxide semiconductor (CMOS) devices has been a prevalent strategy to enhance performance in terms of speed, power consumption, memory density, and noise margins. However, this approach, while effective in reducing power, has introduced challenges such as undesired leakage current, variability issues, and increased susceptibility to intra and inter-die process variations. This has led to mismatches in transistor's threshold voltage between adjacent transistors in a bitcell, resulting in asymmetrical characteristics. Several key parameters require attention to enhance the SRAM cell's performance, including power consumption reduction, low leakage, improved stability, and resolution of read-write conflicts. One method to address power consumption is the reduction of the supply voltage. However, supply voltage scaling directly impacts dynamic power consumption quadratically and leakage power exponentially. This approach, while reducing power, adversely affects circuit performance by increasing sensitivity to process variations and significantly degrading noise margins. The combined effects of supply voltage scaling and augmented process variation have substantially increased the risk of memory failure and exponentially elevated read/write delays [4, 5]. Operational delays escalate with the downscaling of the supply voltage, limiting the speed of the SRAM cell. In the deep subthreshold regime, subthreshold leakage has emerged as a significant issue in embedded cache. To mitigate this,

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transistor stacking presents a viable solution, raising a transistor's threshold voltage to suppress leakage current. The strategic use of high threshold transistors in non-critical paths further reduces subthreshold leakage.

These aforementioned applications necessitate speedy operation and low latency. To address these requirements, a single ended single port topology based half select free read decoupled (WARD) nine transistor SRAM cell is proposed in this paper that showcases shortened write delay by incorporating a low V_{TH} n-type transistor as write access transistor and transmission gate in the feedback connection between inverter pair. Additionally, this cell yields read SNM free operation by dissociating read current discharging path from memory core of the bitcell. The proposed cell exhibits considerably low dynamic swing to the single ended structure of the cell.

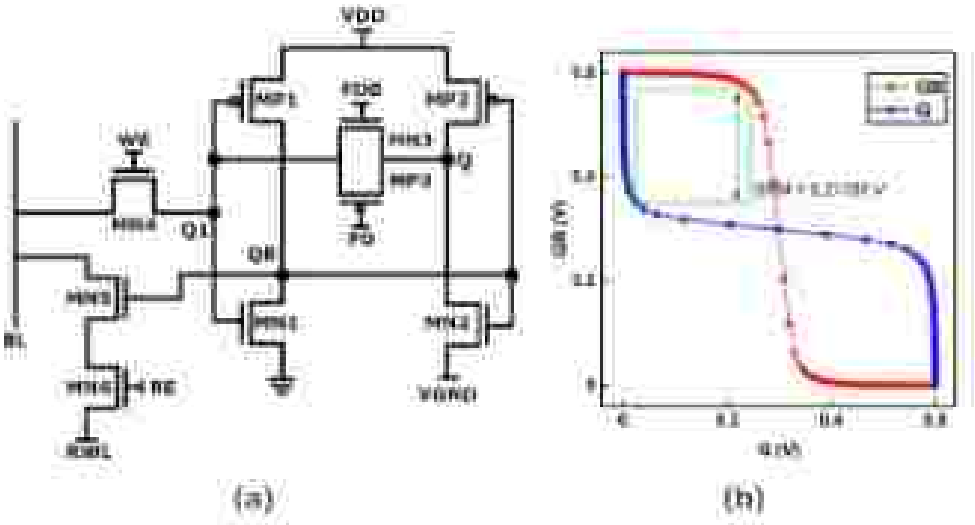
The rest of the paper is structured into the following sections. The proposed WARD 9T SRAM cell architecture is introduced in Section 2. A comparative evaluation for read and write delay performance metrics for the cells is demonstrated in section 3. The static and dynamic power usage analysis is outlined in section 4. The performance and results of the studied SRAM cells are presented and analysed in Section 5. The study concludes with key takeaways in Section 6.

2 Proposed write assist read decoupled 9T SRAM cell

The schematic diagram of proposed nine transistor (9T) Write Assist Read Decoupled (WARD) SRAM bitcell is shown in Fig 1. The core of WARD bit cell includes MN1-MN2 NMOS and MP1-MP2 PMOS transistors, forming an inverter pair latch to store 1-bit information. The cell registers read SNM free operation by dissociating the read path, comprised of MN5-MN6 transistors, from the inverter pair latch. Thus, the proposed WARD 9T SRAM cell is highly stable during read operation. The gate of transistor MN5 is shorted to internal output node 'QB' whereas operation of transistor MN6 is governed by the read enable (RE) signal and its source is shorted to read wordline (RWL) signal. The stacked configuration of these n-type transistors has greatly alleviate the bitline leakage. The write path for the proposed WARD bitcell includes MN4 access transistor, controlled by write enable (WE) signal. A transmission gate MP3-MN3, controlled by the feedback disabled (FD) and FDB signals respectively, is employed in between the feedback path of the inverter pair, thereby enhancing the write '1' performance of the bitcell. Additionally, a (low V_{TH}) transistor MN4 is employed in the write path resulting in a faster write '1' onto cross coupled inverters. A VGND signal is employed at the source of MN2 transistor, set to V_{DD} to ease write '1' operation and grounded otherwise. The proposed design achieves a noticeable reduction in dynamic power consumption. The cell works in different modes based on the configuration of different control signals outlined in Table 1.

2.1 Hold operation

An SRAM cell goes into an energy-saving mode in the hold mode, carefully storing its data without actively performing read or write operations. When the access transistors are inactive, the internal core of memory is disconnected from the bitlines preventing unintended interference. Hold static noise margin (HSNM) gauges the ability to retain cached data during hold mode. SNM values are extracted using the method defined in [16]. Fig. 1b sketches the hold butterfly curve for the proposed 9T cell. This analysis is imperative since memory operates in hold state for the bulk of time. The HSNM values for proposed 9T cell, at different operating voltage, is depicted in Table 2.



(a) (b)

Fig. 1 a Schematic Diagram for Proposed Write Assist Read Decoupled (WARD) 9T SRAM Cell b Butterfly curve of WARD 9T cell

Table 1 Control signals of Proposed 9T cell

	BL	RWL	RE	FD	FDB	WE	WGND
Hold	GND	GND	GND	GND	V_{DD}	GND	GND
Read	Precharged	GND	V_{DD}	GND	V_{DD}	GND	GND
Write'0'	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND
Write'1'	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}

Table 2 Various performance metrics comparison for Proposed 9T cell at different V_{DD}

	0.4 V	0.5 V	0.6 V	0.7 V	0.8 V
HSNM (V)	0.122	0.174	0.217	0.256	0.275
RSNM (V)	0.132	0.174	0.211	0.256	0.275
Write Margin (V)	0.303	0.253	0.380	0.356	0.403
Write'1' delay (ns)	36.25	6.933	3.170	1.619	0.934
Write'0' delay (ns)	7.132	1.341	0.703	0.374	0.466
Read delay (ns)	6.360	2.218	1.251	0.913	0.718
Read Power (pW)	0.629	2.486	6.669	13.52	22.77
Write'1' Power (pW)	0.031	0.244	0.779	1.834	4.266
Write'0' Power (pW)	0.342	1.061	4.234	8.808	14.86
Leakage Power (nW)	6.710	11.25	18.38	29.26	46.42

2.2 Read operation

During the read process, the initial step involves precharging the bitline (BL) to V_{DD}. Subsequently, RE is asserted and RWL is grounded to establish a path for the bitline discharging current. Transistor MN5 is gated to node 'QB' which makes the bitline discharge conditionally via MN5–MN6 transistors based on the data value cached in the inverter latch. If cached data in the bitcell is "1" (Q="1", QB="0"), then bitline retains its pre-charged voltage.

Read Stability is the cell's ability to prevent the cached data being modified during read process and the same is gauged via read static noise margin (RSNM). The proposed cell design incorporates a dedicated read buffer for reading operations to eliminate read upset problem. Thus read stability is not compromised in this design and read SNM is as good as hold SNM. To assess the reliability of proposed 9T cell in an SRAM array, a range of bitline capacitance values ranging from 10 to 1000f, mirroring different array sizes, is taken into account. The study probes its influence on read delay within the SRAM array as shown in Fig. 2c as depicted in [7]. This extensive analysis sheds light into how varying bitline capacitance influences bitcell behavior and performance across different operating conditions.

2.3 Write operation

During write operation, the desired data is written onto the bitline and data is generated at node 'Q' and 'QB' corresponds to logic state on bitline (BL). When BL is set to logic '1'/'0', it generates logic '1'/'0' at node Q and logic '0'/'1' at node 'QB'. A low V_{TH} device is strategically utilized for the write access transistor (WAT). This device jacks up the driving strength of WAT resulting in speedy write '1'/'0' and improved write performance. Fig. 2a presents distribution curves that showcases the write '1' delay of the 9TP cell under two different scenarios: 1. With write assist techniques: This configuration involves utilizing techniques designed to expedite the write '1' operation. 2. Without write assist techniques: This case operates without

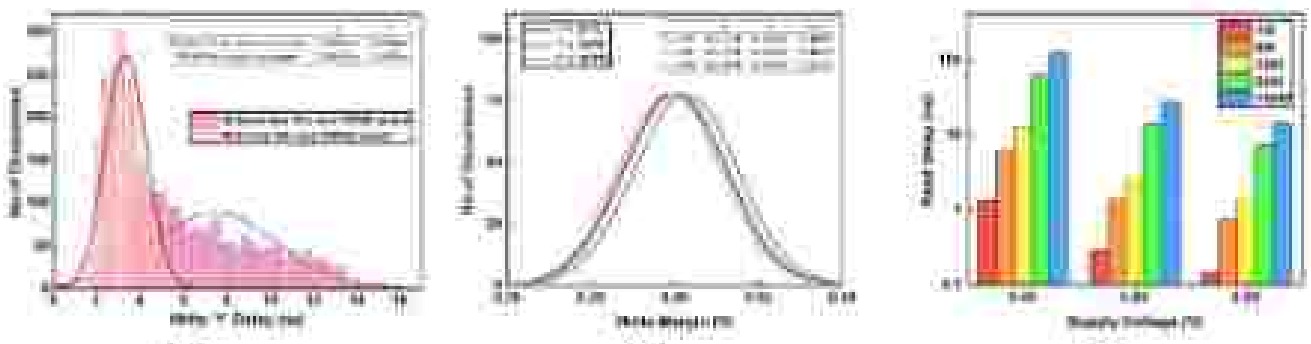


Fig. 2 a Write'1' Delay Distribution Curves for proposed 9T cell under two different scenarios b WM Distribution Graph for the proposed 9T Cell at different temperatures c Read Delay as a function of Bitline Capacitance

the above-mentioned write assist techniques, establishing a reference point for comparison.

In contrast to the traditional write static noise margin (WSNM) method, Write Margin (WM) offer a feasible substitute as it effectively assess the stability without necessitating direct access to internal data storage nodes. The WM, in this study, is calculated using the method defined in [8]. The worst case WM is considered for carrying out WM analysis of proposed 9T cell at different V_{TH} in Table 2.

This study further explores how the write margin (WM) of proposed SRAM architecture is affected by process variations. In this work, device's V_{TH} is deviated 40 mV from its nominal value to investigate the bitcell's reliability for 2k data points. Fig. 2d demonstrates the WM distribution curves of proposed 9T cell across diverse temperature range.

3 Read/write delay

Write delay or Write access time (T_{WA}), a critical metric in SRAM performance, refers to the duration required to successfully inscribe a new data value into the bitcell. It's typically measured as the time period that elapses between the Wordline (WL) signal activation and the point when the relevant data node crosses a designated voltage threshold. This threshold varies based on whether '1' or '0' being written. For write '1' operation, the '0' storing node must charge to 90% of V_{DD} and for write '0' operation, the '1' storing node must discharge to 10% of V_{DD}, as indicated in [9]. The write'1' (T_{WA}'1') and write'0' delay (T_{WA}'0') values for the proposed 9T cell under different operating voltage is depicted in Table 2. An SRAM cell's speed during the read operation can be assessed using the read delay (T_{RA}) measure. For single-ended read operations, T_{RA} stands as the time interval between the wordline's activation and the moment when bitline discharges to half of initial precharged value, as indicated in [9]. The read delay (T_{RA}) for the proposed 9T cell under different operating voltage is depicted in Table 2.

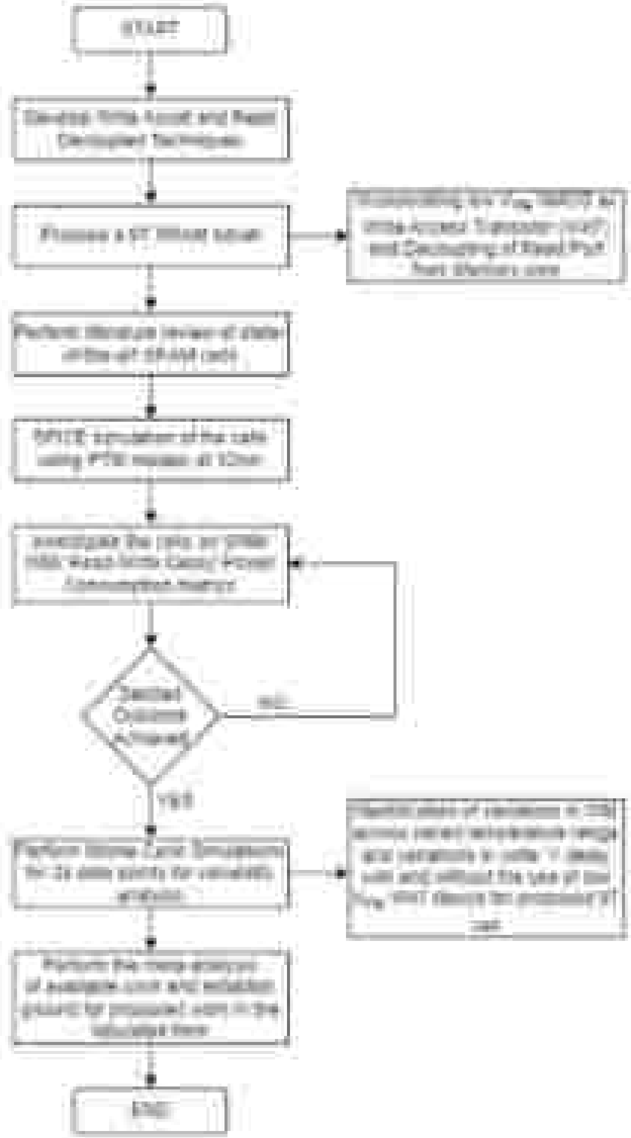


Fig. 3 The proposed design flow for 9T SRAM circuit design and the methodology presented for its performance analysis against state-of-the-art SRAM cells

4 Dynamic/static power consumption

Dynamic power dissipation, encompassing both dynamic read power and dynamic write power, constitutes a significant portion of the overall power dissipation, primarily attributed to the charging/discharging of large capacitances associated with bitlines and control signals. The widely acknowledged strategy for mitigating dynamic power is the reduction in supply voltage, as it leads to a quadratic reduction in dynamic power ($P_{dynamic}$). Considering that most SRAM bitcells in an array are inactive for extended periods of time, static power leakage power is an important parameter [10]. Mathematically, leakage power is expressed as the product of V_{DD} and leakage current. Dynamic read power (P_{read}), dynamic write '1' power (P_{write1}), dynamic write '0' power (P_{write0}) and leakage power ($P_{leakage}$) for proposed cell is depicted in Table 2 across different operating voltages.

5 Cell performance and consumption

In this segment, the performance of the newly proposed 9T cell is assessed and estimated via spice simulations at 32 nm technology node using Predictive Technology Model [11]. Fig.3 illustrates the design process encompassing the design of the proposed 9T cell, which integrates write assist and

Table 3 Comparison of various studied SRAM cells with proposed cell based on different design metrics at V_{DD} = 0.6 V

	WARD 9T cell	7T cell [12]	8T cell [13]	9T HWA [14]	9T SB [9]	9T TRD [15]	10T cell [16]	11T cell [17]
HSNM (V)	0.2174	0.133	0.229	0.2173	0.226	0.125	0.175	0.216
RSNM (V)	0.2174	0.133	0.229	0.2173	0.226	0.125	0.085	0.216
WM (V)	0.300	0.300	0.106	0.301	0.296	0.300	0.234	0.300
T_{WA} '1' (ns)	3.170	6.717	0.634	10.06	7.689	1.374	9.812	1.151
T_{WA} '0' (ns)	0.703	0.886	0.340	1.170	0.891	1.092	1.100	1.190
T_{RA} (ns)	1.351	0.592	2.097	1.349	11.43	1.347	1.188	2.995
P_{read} (µW)	6.669	13.22	4.294	6.677	0.826	6.677	7.579	4.295
P_{write1} (µW)	1.986	1.180	7.366	0.866	1.027	7.699	0.831	3.283
P_{write0} (µW)	4.734	4.206	4.765	3.191	4.204	3.466	3.414	3.222
$P_{leakage}$ (nW)	18.38	17.86	27.31	17.07	11.81	17.03	14.54	23.05

read decoupled techniques. The methodology employed in conducting the performance analysis of the proposed architecture is also depicted, comparing it against state-of-the-art SRAM bitcells. To gauge the effectiveness of the proposed cell, a thorough comparison is conducted against pre-existing SRAM bitcell topologies as shown in Table 3. To assure fair and relevant comparison, sizing (aspect ratio) of all the n-type and p-type transistors in both pre-existing cells and the proposed cell is presumed to be 64/32 and 80/32 respectively while for the transmission gate, both the transistors are sized at 32/32 with a bitline capacitance of 50fF. All the cells are simulated at an operating voltage of 0.6 V and 27 °C room temperature.

It is evident from the Table 3 that among all the cells incorporating single ended write structure, 9TP cell has least write '0' delay and third best write '1' delay after 9T TRD and 11T cell due to the utilization of transmission gate in the write path and negative bitline scheme respectively. Among all the cells studied, only 7T and 10T cell has better read delay performance than 9TP cell but this improvement comes at a cost of increased bitline leakage and degraded read SNM respectively. The 9TP cell consumes highest write '0' power after 8T cell, attributed to the lower write '0' delay as $P_{dynamic}$ and delay shares inverse relationship with each other.

6 Conclusion and future scope

In this study, a highly stable and robust Write Assist Read Decoupled (WARD) 9T SRAM cell has been introduced in this work. The architecture of the cell designed for a 32 nm technology node. The read disturbance is eliminated by the proposed design due to the use of a dissociated read path. Furthermore, the write '1' issue in the proposed single-ended design is removed with the aid of a feedback-cutting transmission gate, a low threshold write access transistor and VGND write-assist technique. The 9TP SRAM showed notable enhancements in RSNM (HSNM) and write '0' delay, surpassing other 9T cells discussed in this study. The suggested 9T cell demonstrates a significant enhancement in read/write speed. The cell introduced here could benefit from further analysis such as the impact of single event upsets (SEUs), flipping of cell's state due to ionized particles striking a sensitive node, on the cell's performance against harsh space radiations and other issues like half select disturbances for memory array architecture design.

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Data availability My manuscript has no associated data.

Code availability Not Applicable.

Declarations

Conflict of interest Not Applicable.

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