Design of Optimized One Bit Arithmetic Logic Unit in QCA - Quantum-Dot Cellular Automata

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Abstract. One way to get around the limitations of CMOS technology is to switch to quantum dot cellular automata (QCA). An ALU (Arithmetic Logic Unit) serves as the basic component in every computer system. This study presents the development of an improved one-bit ALU tailored for QCA. The AND, ADD, OR and XOR operations are included in the suggested ALU framework. The suggested topology makes use of a low complexity 2:1 MUX, an incredibly effective two input XOR gate, along with an efficient full adder. QCADesigner simulates the suggested ALU structure, and the simulation's outcome is assessed. Evaluation findings show that the recommended design outperforms the other options in terms of energy dissipation, dimensions, complexity, and number of cells.

INTRODUCTION

Low fault tolerance, limited design flexibility, and high cost are some of the limitations of CMOS designs, which result in low dependability and high failure rates. CMOS designs are replaced with designs based on novel nanoscale technology, such as QCA which stands for quantum dot cellular automata [1]. One choice for possible future remedies is QCA [2] which is capable of solving the aforementioned issues [3]. QCA has a small footprint, low power consumption, rapid operation speed, and high density. [4]. There is an electron in two of the four dots positioned at the opposite corners of a QCA cell. Electron pairs are used in coulomb repulsion, which serves as the foundation for the polarization process [5].

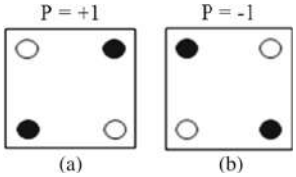


FIGURE 1. The two distinct polarizations in a QCA cell: a) positive and b) negative.

As seen in Figure 1a and b, respectively, two different polarizations (p) of the QCA cells are possible: p = +1 (logic high) and p = −1 (logic low) [6, 7]. As illustrated in Figs. 2a and 2b, respectively, sequentially connecting same polarization 90° cells or different polarization 45° cells combine to create a QCA wire [8, 9, 10]. As seen in Figs. 3a and b respectively, the inverter gate and 3-input majority gate, are the two QCA foundational gates. [5]. If the input of the inverter gate changes to logic low, the outcome switches to logic high, and vice versa. If one of any inputs in the majority gate changes to negative (P=-1) that is logic 0, the output will be an AND of other 2 inputs; if it changes

to positive (P=+1) that is logic 1, the output will be an OR of the other 2 inputs [5]. Figs. 4a and b display more inverter gate configurations.

Within QCA, there are three fundamental kinds of wire crossings: coplanar crossings, multilayer crossings, and crossings with distinct clock zones. As seen in Figure 5a, coplanar crossing [5] involves two wires in QCA, one at a 45° angle and the other at a 90° angle. As seen in Figure 5b, multi-layer crossing [11] involves three tiers of two 90° wires crossing each other. Two QCA wires cross each other when they cross with different clock zones [12], as seen in Figure 5c, with a difference of two clock zones. Clocking is the method of timing in QCA. In a QCA circuit, an adiabatic clocking mechanism is utilized. This clocking system comprises four distinct clocking zones labeled as 0, 1, 2, and 3. Each clock zone encompasses four phases: Hold, Release, Switch, and Relax, as illustrated in Figure 6. [13].

The fundamental building block of all computers is the ALU. ALU includes a variety of arithmetic and logical operations, including AND, OR, XOR, XNOR, decrement, addition, subtraction, increment, and so on [14]. Select lines are available for a range of operations in the ALU, one of the combinational and multiple operation structures [15, 16]. This paper presents the design of an enhanced ALU for a single bit in QCA. The recommended QCA-based ALU structure consists of AND, ADD, XOR, and OR operations. This design makes use of the full adder, XOR, and improved MUX 2:1 structure.

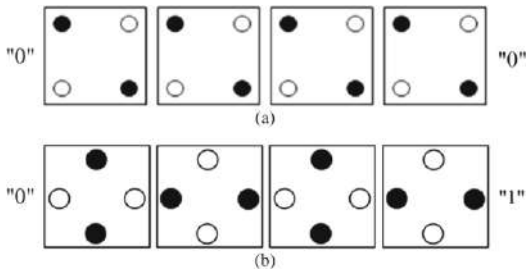


FIGURE 2. QCA wire with a) 90° cells; b) 45° cells [17]

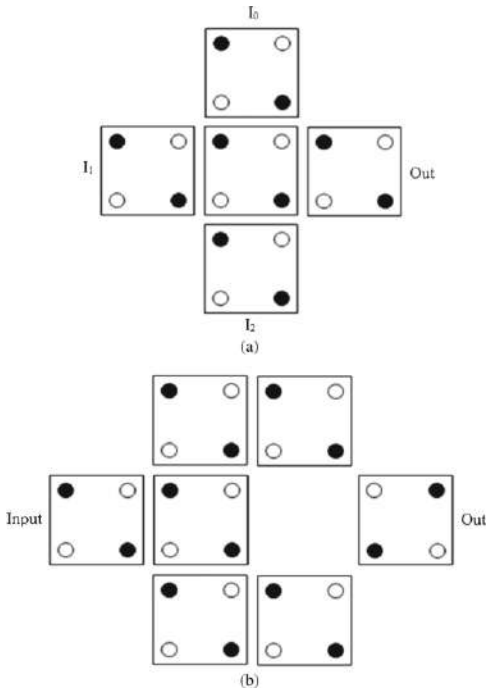


FIGURE 3. a) 3- input Majority gate; b) Inverter gate:

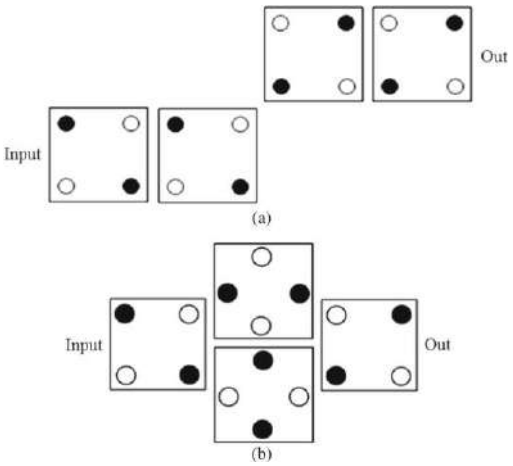


FIGURE 4. More inverter gates in QCA are a) employing diagonal 90° cells; b) employing 45° and 90° cells.

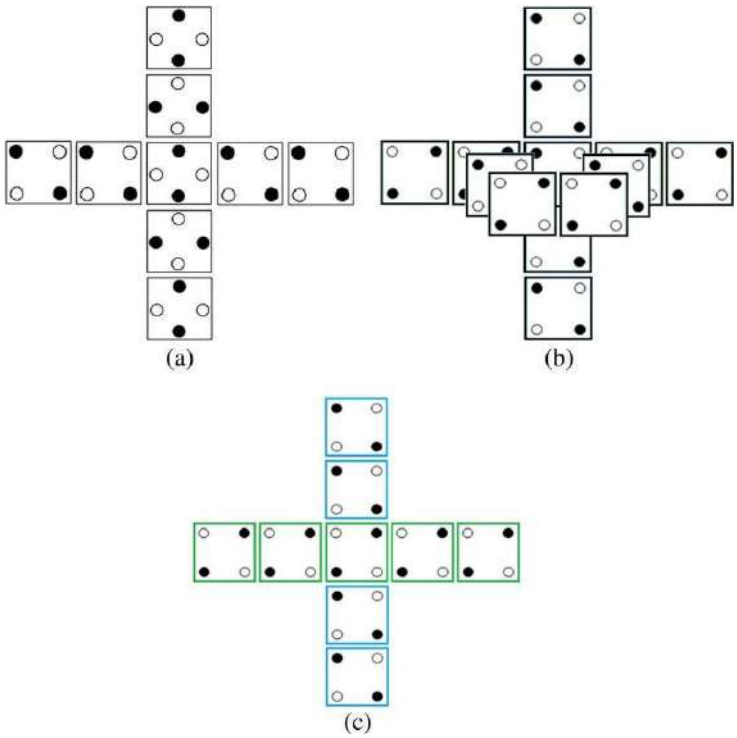


FIGURE 5. a) Co-planar wire crossing; b) Multi-layer wire crossing; c) Wire crossing over different clock zones

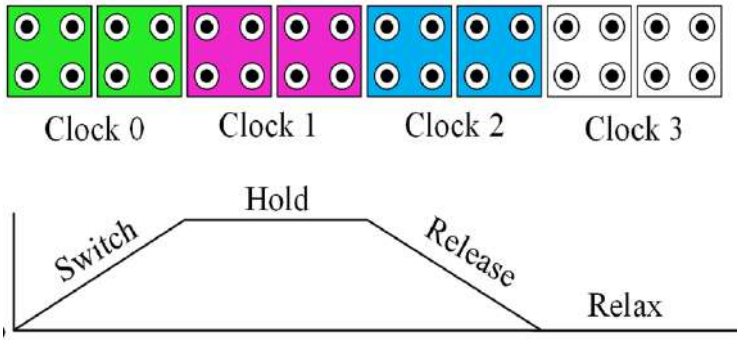


FIGURE 6. Clocking zones in QCA [13]

METHODOLOGY

Design and Simulation of Modules

This study presents an improved single-bit ALU design in QCA. Operations AND, ADD, OR, and XOR are included in the proposed ALU. This design makes use of the enhanced XOR, Full adder, and MUX 2:1 structures. Rather than relying on any Boolean calculations, the MUX 2:1 and XOR utilize an inherent property of QCA cells. Figure 7 [12] displays the QCA configuration of 2:1 MUX utilized in the proposed design. Compared to previous designs, the MUX 2:1's construction is straightforward and incredibly effective. It has 13 cells, 2 clock zone delay, 0.01 μm2 occupied area, and no cross wiring. F = AS' + BS is what mux 2:1 outputs. Input A is output of mux 2:1 if S = 0, while input B is output of MUX 2:1 if, S=1. Three mux of 2:1 configuration are used by the suggested ALU design to create a 4:1 MUX.

FIGURE 7. a) QCA layout of MUX 2:1; b) Waveform of MUX 2:1 [12]

The suggested ALU is designed using an ultra-efficient 2-input XOR gate [18]. Figure 8 shows the XOR gate's QCA configuration. The gate features 13 cells, 2 clock zones delay and occupied an area of 0.01 μm2. An XOR gate has the following output: A ⊕ B = OUT = AB' + A'B. The XOR yields 0 as a result, if both inputs are the same, that is, "00" or "11", otherwise yields 1 as a result.

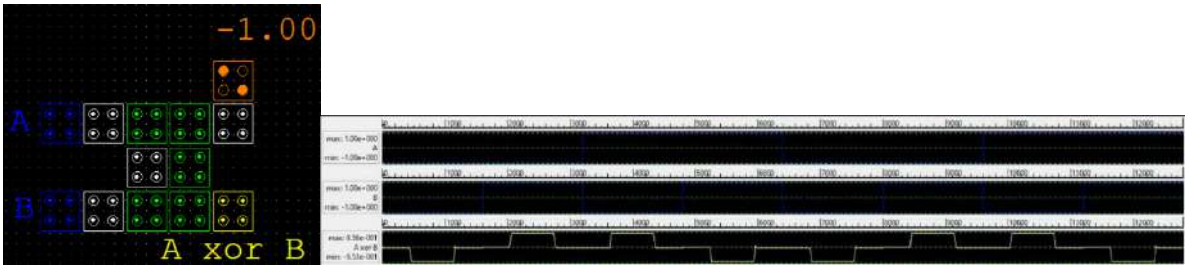


FIGURE 8. a) Two-input XOR gate in QCA [18]; b) Waveform of XOR Gate

The suggested ALU uses a Full adder with ultra-high speed, little delay, and low complexity [18]. Fig. 9 displays the whole adder's QCA configuration. This Full adder utilizes 16 cells, occupied an area of 0.02 μm2, and 2 clock zones delay. Only 90° cells are used in this construction. The following equations yield the entire adder:

$$SUM = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in}$$

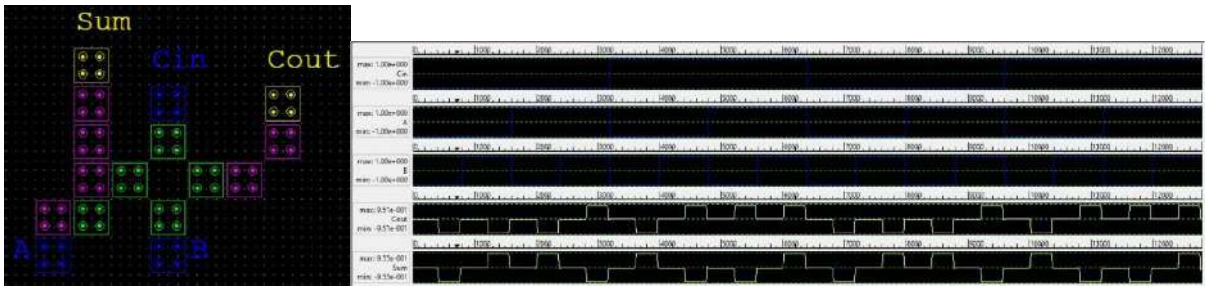


FIGURE 9. a) Full Adder design in QCA [18]; b) Waveform of Full Adder

Proposed Design of ALU

This study presents an improved single-bit ALU design in QCA. Operations AND, OR, XOR, and ADD are included in the proposed ALU. In this layout, the enhanced frameworks of XOR, Full adder, and MUX 2:1 are employed. Instead of depending on Boolean expressions and basic gates, the MUX 2:1, Full Adder, and XOR leverage a trait intrinsic to QCA cells. Fig. 7 [12] displays the MUX 2:1 QCA configuration that is employed in the suggested ALU.

Fig. 10a displays the ALU's QCA design. There is no need for a 45° wire in this configuration because input A travels via input B with a two-clock zone delay. We utilized crossings that distinct several clock zones.

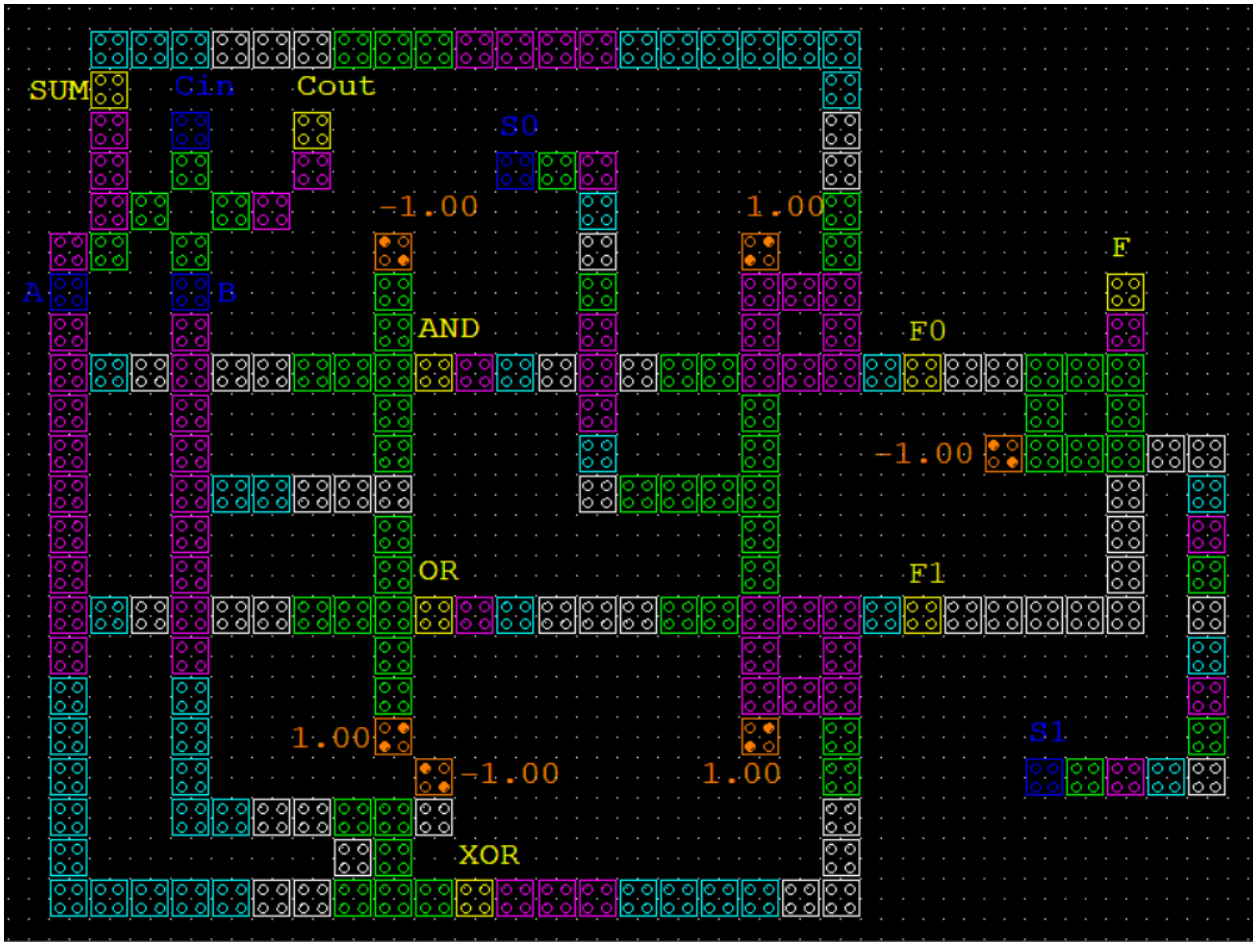
Based on the following equations, the suggested structure functions:

$$F0 = SUM.S0 + AND.S0'$$
$$F1 = OR.S0' + XOR.S0$$
$$F = F0.S1' + F1.S1$$

F0 is the outcome of upper 2:1 MUX for AND instruction and ADD instruction. F1 is the outcome of lower 2:1 MUX for OR instruction and XOR instruction. For both F0 and F1, F is the result of 2:1 MUX.

TABLE 1. Instruction Set of proposed ALU

Select Lines		Instruction	Result
S1	**S0**		
0	0	AND	F = A . B
0	1	SUM	F = Sum = $A \oplus B \oplus C_{in}$ $C_{out} = A.B + B.C_{in} + C_{in}.A$
1	0	OR	F = A + B
1	1	XOR	$F = A \oplus B$



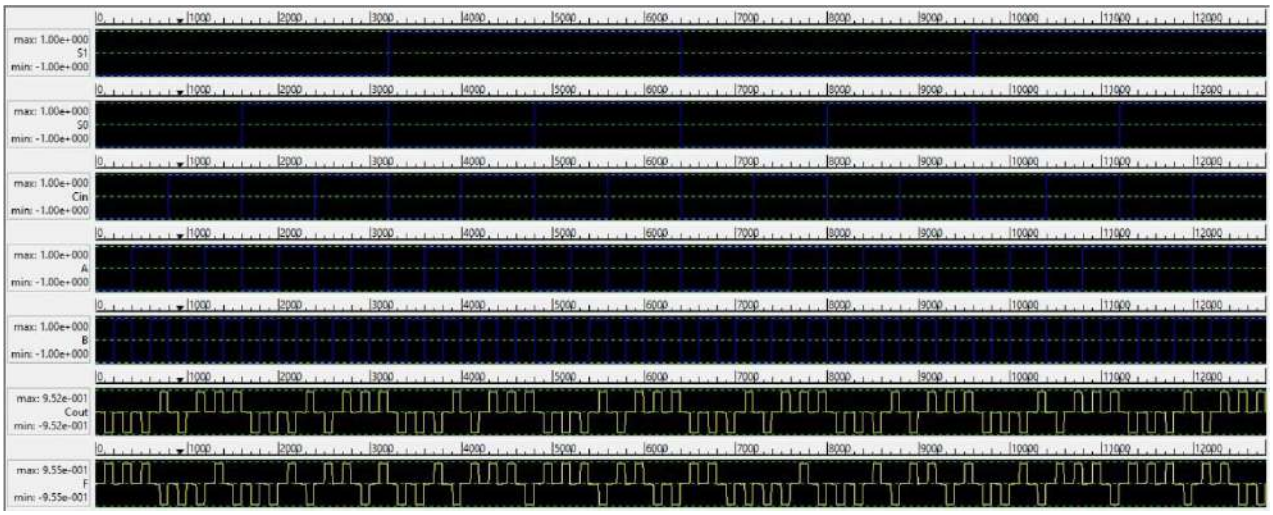


FIGURE 10. a) Proposed ALU's QCA Layout; b) Waveform of outputs from ALU

RESULTS AND DISCUSSION

Simulation Results and Comparisons

QCA Designer is used to simulate the proposed design. The Coherence Vector simulation engine was utilized in version 2.0.3 [19]. Table 2 shows the parameters used in the simulation. Figure 10b displays the simulation results for the suggested single-bit ALU. The proposed structure does the following four basic operations: AND, OR, XOR, and ADD. It features three input lines (A, B, and Cin), two select lines (S0 and S1), and one output line (F). This outcome demonstrates that, under many scenarios, the anticipated output is indeed produced.

The output of starting time that is generated before expected output F is unimportant. This ALU contains 220 cells, occupied area 0.26 μm2, cross wiring with clock zone delay and three clock cycle delay. This design uses cross-wiring of 90° cells with multiple clock zones. When compared to earlier designs, the suggested one is significantly more efficient in terms of occupied space, energy dissipation and the amount of cells used.

To assess the effectiveness of the suggested design, it is compared with earlier versions [10, 14, 15, 19-24]. Table 2 defines the simulation parameters used. Table 3 displays the evaluation's findings. Table 3 suggests that in comparison to the previous architectures, the recommended design of ALU is better in terms of size, number of cells, and simpler design.

TABLE 2. Simulation Engine Parameters

Simulation Engine Parameters	Delay (Clock Cycles)
Cell Dimensions	18 nm × 18 nm
Diameter of Dot	5 nm
Time Step	1.00e-016
Simulation Duration	7.00e-011
Clock Low	3.80e-023
Clock High	9.80e-022
Clock Shift	0.00e+000
Clock Amplitude Factor	2.000
Relative Permittivity	12.900
Radius of Effect	65.000 nm
Layer Separation	11.500

TABLE 3. One-bit ALU structures' assessment outcomes

Design (One Bit ALU)	Area	Number of Cells	Delay (Clock Cycles)	Cross Wiring
[14]	2.34	1075	2	Coplanar
[15]	0.39	1376	5	Multilayer
[20]	0.92	494	3	Coplanar
[23]	0.85	391	3	Multilayer
[24]	2.28	1190	6	Coplanar
[21]	1.68	918	9	Coplanar
[19]	3.04	1096	15	Coplanar
[22]	0.78	430	3	Multilayer
[10]	0.29	257	2	Coplanar
Proposed	0.26	220	3	Coplanar

Analysis of Energy Dissipation

In the QCA circuit design, QCA-E, a modeling tool [25-27] was utilized to determine energy dissipation of the cells. The two energies—that is, the total and average energy loss—were assessed using the technique. The analysis was conducted using T = 1K, the default operating temperature selected for the energy dissipation research of the proposed design. The energy dissipated by the current circuitry and the suggested design are displayed in the table.

TABLE 4. Energy Dissipation Values for Existing Design [10] vs Proposed Design

Type of Energy Dissipation (in meV)	T = 1K	
	Existing design [22]	Proposed Design
Per Cycle Average	$6.81 \times 10{-}3$ eV ± $5.72 \times 10{-}4$ eV	$5.58 \times 10{-}3$ eV ± $4.61 \times 10{-}4$ eV
Total	$7.50 \times 10{-}2$ eV ± $6.29 \times 10{-}3$ eV	$6.13 \times 10{-}2$ eV ± $5.07 \times 10{-}3$ eV

It uses the approach described in [27] to approximate the dissipated energy of the circuits created in QCA. Ebath_total, gives the entire energy dissipated as a whole value. This can be roughly expressed as the sum of all "bath" of energy (Ebath) added by each design cell for every clock cycle. The energy exchanged between the clock and each of the circuit's constituent cells, which are spaced apart by one clock cycle, is multiplied by two to calculate Eclk. The total energy dissipated by the proposed 1-bit ALU is $6.13 \times 10{-}2$ eV, with error of around ±$5.07 \times 10{-}3$ eV. For Each cycle, the circuit's average energy dissipation for each cycle turns out to be $5.58 \times 10{-}3$ eV with an Error of ±$4.61 \times 10{-}4$ eV.

CONCLUSION

The paper proposes an improved single-bit ALU structure in QCA. AND, OR, XOR, and ADD are the four basic operations carried out by the proposed structure. A two-bit ALU and other features can be implemented with ease by adding modular extensions to the suggested structure. Version 2.0.3 of QCADesigner simulates the suggested structure. The simulation's output demonstrates how the suggested ALU outperforms the earlier solutions in terms of size and cell count using simpler design architecture.

Our design achieved a 14.39% reduction in the amount of cells within a condensed area (10.344% smaller). This translates to an impressive 18.061% decrease in average power dissipation per cycle and an 18.267% reduction in total power dissipation, at the cost of an additional clock cycle from existing design [10].

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