A design technique for energy reduction in dynamic DCVSL logic

Anshul Iyer
Department of Electronics and Communication
Delhi Technological University
Delhi, India
anshuliyer_ec20b12_07@dtu.ac.in

Harsh Sinha
Department of Electronics and Communication
Delhi Technological University
Delhi, India
harshsinha_ec20b12_59@dtu.ac.in

Ishaan Singh
Department of Electronics and Communication
Delhi Technological University
Delhi, India
ishaansingh_ec20b12_66@dtu.ac.in

Neeta Pandey
Department of Electronics and Communication
Delhi Technological University
Delhi, India
neetapandey@dce.ac.in

***Abstract* — In the domain of digital circuitry, optimizing power consumption is paramount for enhancing operational efficiency and minimizing energy usage. This paper introduces a novel design approach aimed at significantly reducing energy consumption in Dynamic Differential Cascode Voltage Switch Logic (Dy-DCVSL) circuits, widely employed in low-power CMOS design. While Dy-DCVSL offers inherent advantages over traditional CMOS logic, further enhancements are essential for modern portable and battery-powered devices. The proposed technique leverages charge recycling, a method that recovers and reuses charge within the logic gates themselves. By implementing this approach, the dynamic power consumption associated with charging and discharging internal capacitances during operation is effectively mitigated. The paper provides detailed insights into the design implementation of the charge recycling mechanism within Dy-DCVSL gates and comprehensively analyzes its impact on power dissipation.**

Keywords*— *CMOS technology, Dynamic circuit design, Charge Recyling, Power Delay Product

I. Introduction

The escalating demand for portable, battery-operated systems accentuates the critical significance of implementing low-power design methodologies in microelectronics. Digital CMOS circuits manifest three primary sources of power consumption: short-circuit current arising from the direct path between power supplies, dynamic current stemming from circuit switching activity, and leakage current attributed to device-level leakage. Tackling these power consumption challenges has been the subject of extensive research [1-3], resulting in a plethora of methodologies documented in the literature.

This paper introduces a novel low-power design technique tailored specifically for Dynamic Cascode Voltage Switch Logic (Dy-DCVSL) [5]. The approach revolves around the concept of charge recycling, which seeks to minimize dynamic energy dissipation by repurposing charges stored at internal circuit nodes during one clock cycle for use in the subsequent cycle. This innovative technique is facilitated by a recycle-switching topology enabling unidirectional charge transfer between circuit nodes. Importantly, the implementation of this topology yields a secondary benefit: the elimination of short-circuit current.

The paper is structured as follows to comprehensively elucidate the proposed methodology and its ramifications. Section II provides an in-depth exposition of the principles underlying Dy-DCVSL circuit design, offering insights into its theoretical underpinnings. In Section III, the charge-recycling approach is introduced and a thorough analysis of the operational dynamics of the proposed modification is conducted. Furthermore, Section IV showcases simulation results from carefully selected case studies, offering empirical validation of the approach's efficacy. Finally, in Section V, drawing on key insights from the preceding sections, conclusions are drawn.

II. Dy-DCVSL circuit design

A. *Dynamic Differential Cascode Voltage Switch Logic (Dy-DCVSL)*

Dy-DCVSL is an advanced logic design combining CMOS and ratioed pseudo-NMOS logic for compact, high-speed circuits [1,6]. It offers various configurations with specific advantages [5].

B. *Basic Dy-DCVSL Gate*

A Dy-DCVSL gate (Fig 1 in [5]) uses a clock (CLK) to control precharge and evaluation phases [6]. During precharge (CLK low), both outputs (OUT, OUTB) are precharged high (VDD) by transistors M1, M4 (NMOS only). Evaluation (CLK high) activates logic evaluation. Depending on the input, one output goes low via transistors M2, M3 (cross-coupled for faster switching) with help from M5, M6.

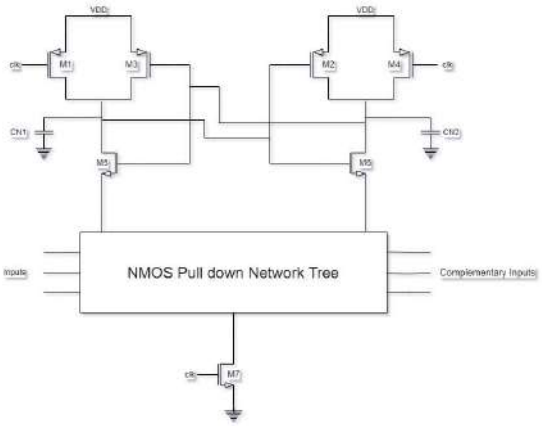

Fig. 1 N-Dy-DCVSL cell

C. *Dy-DCVSL Pipeline*

Cascading Dy-DCVSL units creates a pipeline for higher efficiency (Fig 2). An inverted clock (CLK_B) and a p-Dy-DCVSL unit are used. Transistors M8, M11 pre-discharge capacitors CP1, CP2 during the low CLK phase, while M1, M4 pre-charge CN1, CN2.

In the evaluation phase (high CLK), each unit performs its function. Capacitors (CN1, CN2, CP1, CP2) store outputs.

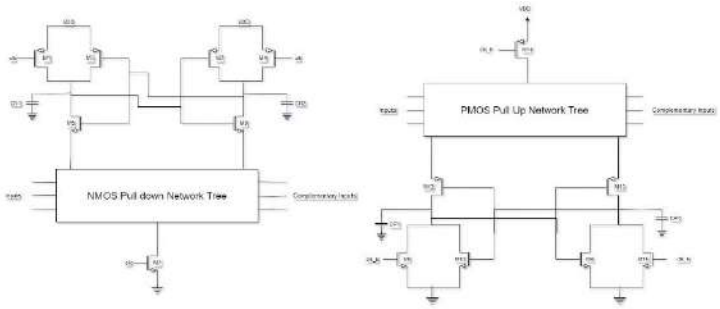

Fig. 2 Cascading Dy-DCVSL cells

D. *Energy Dissipation*

The total dynamic energy (Etot) dissipated during a clock cycle depends on the capacitances (Cn, Cp) of these capacitors and the energy dissipated by each gate (Ep, En).

Half this energy dissipates each phase. If the evaluation paths are inactive, there's no energy dissipation.

The goal is to reduce energy dissipation by reusing charges during active evaluation phases (references maintained).

III. Proposed dynamic DCVSL with charge recycling

A. *Charge Recycling Mechanism*

The charge recycling mechanism, as depicted in Figure 3, employs conditional switches SW1 and SW2, which activate after each evaluation phase and before each subsequent precharge phase. Figure 4 introduces a "recycle phase" between the evaluation and precharge phases, facilitated by an additional clock signal (CLK_M) and its complement (CLK_M_B) [7].

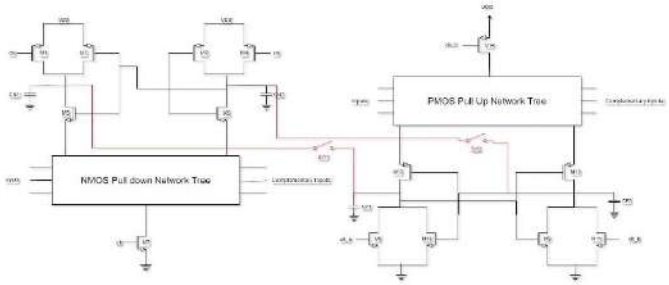

Fig. 3 Dy-DCVSL switches with conditional switches

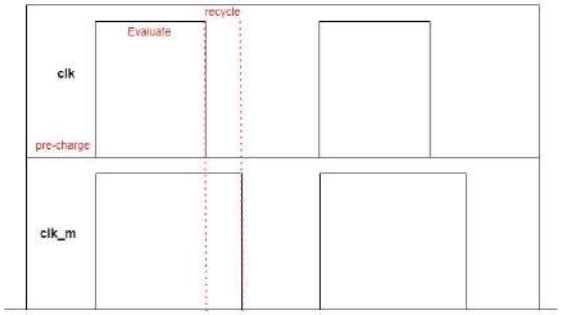

Fig. 4 Clocking Scheme

B. Output State Alteration

After an evaluation phase, the outputs of the first gate (n-Dy-DCVSL) change based on the implemented logic, affecting either discharge or maintenance of high states for CN1 or CN2. The outputs of the second gate change through its pMOS network, resulting in either charging or maintenance of low states for CP1 or CP2. Switches SW1 and SW2 facilitate controlled charge sharing between these outputs.

C. Charge Migration and Energy Savings

During a recycle phase following an evaluation phase, the switches remain in the "on" state exclusively. Charges migrate from the second gate's outputs, set for discharge, to the first gate's output, destined for charging in the subsequent precharge phase, aiding in energy savings.

D. Charge Equalization and Equations

After an active evaluation phase, only Cp retains a charge equivalent to VDD, representing the total charge stored. During a complete recycle phase, voltages on both output nodes equalize to Veq through charge sharing. The charges on Cp and Cn become Qp and Qn, respectively [8].

$$C_p V_{DD} = Q_p + Q_n$$
$$Q_p = C_p V_P$$
$$Q_n = C_n V_P$$

and consequently,

$$V_{eq} = \frac{C_n V_{DD}}{C_p + C_n}$$

E. Precharge Phase and Energy Dissipation

During the subsequent precharge phase, the first gate's output transitions from ground to VDD, while the second gate's output shifts from VDD to ground. The energy dissipated by the first gate in a clock cycle involving an active evaluation phase comprises two components, as described by equations [8].

$$E_n^i = \frac{C_n V_{DD}^2}{2} + \frac{V_{DD}}{2} \int_{V_{eq}}^{V_{DD}} C_n V_{DD}.dv = \frac{2C_n^2 + C_n C_p}{2(C_n + C_p)} V_{DD}^2$$

$$E_p^i = \frac{C_p V_{DD}^2}{2} + \frac{V_{DD}}{2} \int_{0}^{V_{DD}} C_p.dv = \frac{2C_p^2 + C_n C_p}{2(C_n + C_p)} V_{DD}^2$$

$$E_{total}^i = E_p^i + E_n^i = \frac{C_p^2 + C_p C_n + C_n^2}{2(C_p + C_n)} V_{DD}^2$$

Energy Density Factor $\boldsymbol{\alpha}$

$$\alpha = \frac{E - E_{total}^i}{E} = \frac{C_p . C_n}{(C_p + C_n)^2}$$

F. Control and Regulation

Recycling switches SW1 and SW2, comprising diode-connected transistors in conjunction with pass transistors, regulate charge flow direction, as illustrated in Figure 5. The pass transistor responds to CLK_M_B, ensuring charge transfer occurs after the active evaluation phase. Modified clock signals, CLK_M and CLK_M_B, control transistors based on signal waveforms delineated in Figure 4.

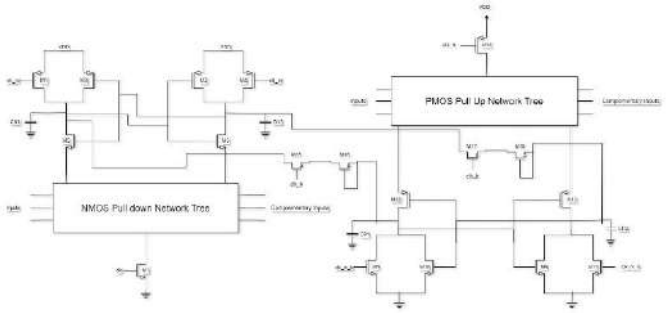

Fig. 5 Charge Recycling with Diode connected loads and pass transistors

IV. Results

The LTSpice simulations for 3 input AND/NAND and OR/NOR DVCSL circuits with charge recycling have been presented in the given segment. The circuits were implemented using 180 nm CMOS technology parameters. A supply voltage of 1 V was chosen, and considering a Vswing of 1 V, Vdd - Vswing is equal to 0 V. Additionally, the load capacitance (CL) was set to 10 fF. The values of calculated performance indexes have been compared with literature in table 1.

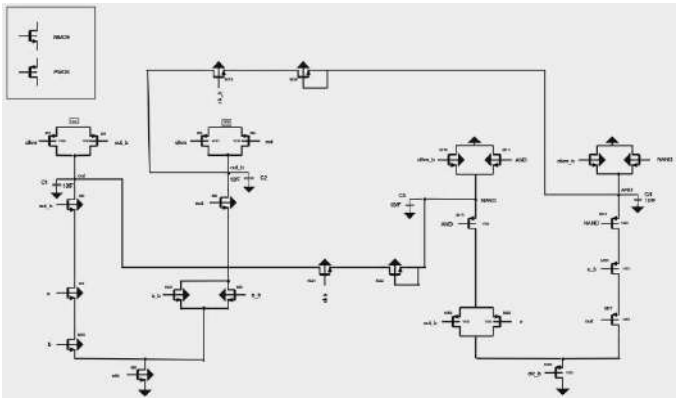

Fig. 6 3-input AND/NAND circuit

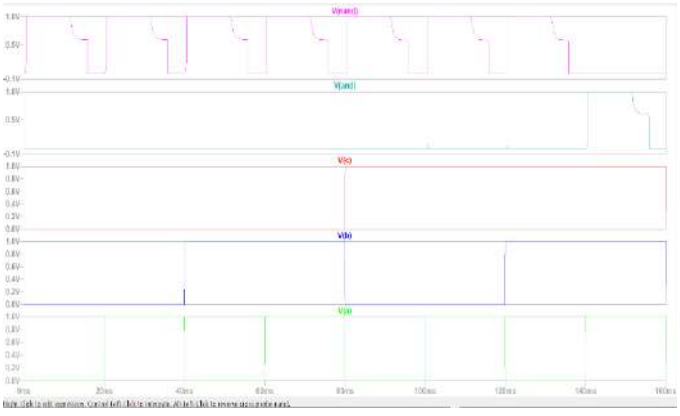

Fig. 7 Output waveform for 3 input AND/NAND circuit

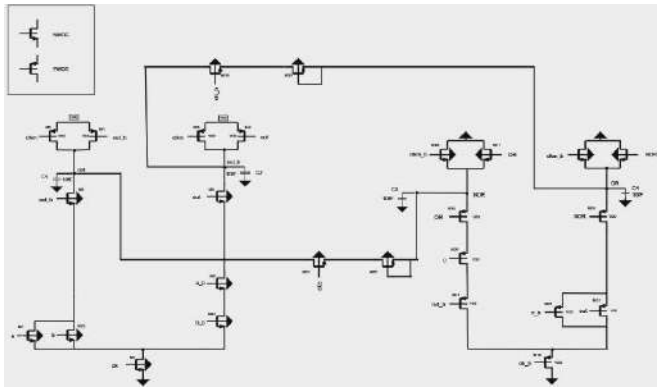

Fig. 8 3-input OR/NOR circuit

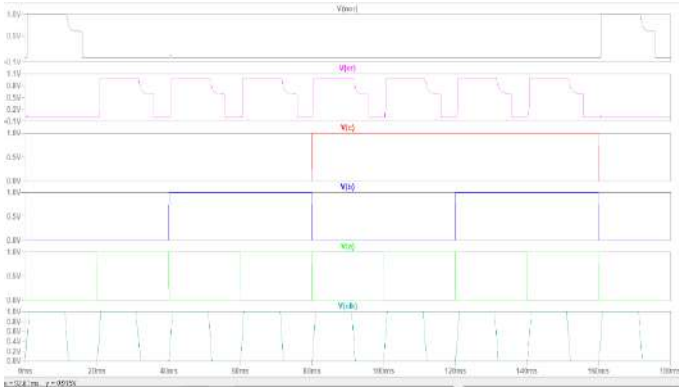

Fig. 9 Output waveform of 3-input OR/NOR circuit

Table1. Comparison of different transforms with literature

digital block	delay (ns)	power (nw)	no. of transistors
3 input and/nand (dy-dcvsl)	11.86	95.24	22
3 input and/nand (charge recycling)	22.49	23.75	26
3 input or/nor (dy-dcvsl)	8.07	83.32	22
3 input or/nor (charge recycling)	19.24	20.51	26

The comparative analysis demonstrates a significant enhancement in performance for Dy-DCVSL circuits incorporating charge recycling, as opposed to their counterparts without this feature. Specifically, we observed a substantial 41.31 percent reduction in the Power-Delay Product (PDP), albeit accompanied by an increase in transistor count.

V. Conclusion

This study pioneers a methodology tailored for Dynamic Differential Cascode Voltage Switch Logic (Dy-DCVSL), focusing on minimizing power consumption. By integrating charge recycling, a unidirectional charge transfer structure, and an innovative clocking scheme, our approach enables efficient charge reuse across operational phases, reducing energy requirements and promoting sustainability.

Moreover, our novel clocking scheme effectively mitigates short-circuit currents, enhancing Dy-DCVSL circuit reliability. Through extensive simulations on a 180nm CMOS platform, we validated our methodology, demonstrating minimal delays and practical feasibility.

REFERENCES

[1] 1995. Minimizing power consumption in digital CMOS circuits. Proceedings of the IEEE, 83(4), pp.498-523.

[2] Weste, N.H. and Eshraghian, K., 1985. Principles of CMOS VLSI design: a systems perspective. Addison-Wesley Longman Publishing Co., Inc..

[3] Veendrick, H.J., 1984. Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits. IEEE Journal of Solid-State Circuits, 19(4), pp.468-473.

[4] Chu, Kan & Pulfrey, David. (1987). A comparison of CMOS circuit techniques: Differential Cascode Voltage Switch logic versus conventional logic. Solid-State Circuits, IEEE Journal of. SC-22. 528 - 532. 10.1109/JSSC.1987.1052767.

[5] Heller, L., Griffin, W., Davis, J. and Thoma, N., 1984, February. Cascode voltage switch logic: A differential CMOS logic family. In 1984 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Vol. 27, pp. 16-17). IEEE.

[6] Bajpai, P., Pandey, N., Gupta, K., Bagga, S. and Panda, J., 2017. On improving the performance of dynamic DCVSL circuits. Journal of Electrical and Computer Engineering, 2017.

[7] Tsiatouhas, Yiorgos, et al. "A low power NORA circuit design technique based on charge recycling." 10th IEEE International Conference on Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003. Vol. 1. IEEE, 2003.

[8] Limniotis, Konstantinos & Tsiatouhas, Yiorgos & Haniotakis, Themistoklis & Arapoyanni, A.. (2007). A design technique for energy reduction in NORA CMOS logic. Circuits and Systems I: Regular Papers, IEEE Transactions on. 53. 2647 - 2655. 10.1109/TCSI.2006.885690.