Analysis of Different Comparator Architectures of Successive Approximation Register ADC

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Abstract. This paper presents a comparison of different comparator architectures employed in Successive Approximation Register Analog-to-Digital Converters (SAR ADCs). It thoroughly examines and evaluates a spectrum of comparator designs, encompassing traditional architectures, double-tail comparator variations, and Elzakker comparator variations. All versions of comparator blocks were designed and prototyped in the 45 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology. This paper focuses on essential parameters such as power dissipation and propagation delay with varying supply voltage, aiming to highlight performance characteristics and trade-offs among different designs. In terms of static and dynamic power consumption, energy dissipation, and time delay, the Modified Elzakker Comparator emerges as a compelling choice, particularly suitable for applications prioritizing energy efficiency. Conversely, for applications emphasizing high-speed operation, the Modified Double Tail Comparator proves to be a standout performer.

Keywords: Comparator, Analog-to-digital converter (ADC), Successive Approximation Register (SAR), dynamic clocked comparator, Double Tail Comparator, Elzakker Comparator, performance analysis

1 Introduction

In today's digital age, the analog world persists alongside digital processing. Bridging these realms requires analog-to-digital conversion, especially for interactions between the digital and physical worlds. This conversion is crucial in various fields such as wireless communication, data storage, sensor applications, biomedical research and healthcare practices [10]. Given the pivotal role of this conversion, communication system designers must meticulously craft the design of ADCs. Comparator circuits are essential in shaping analog-to-digital converter (ADC) architectures, influencing their speed, precision, and energy efficiency. ADCs with low power consumption and high-speed capabilities are particularly suitable for integration into portable electronic devices[14].

In the realm of Analog-to-Digital Converters (ADCs), various types have emerged, each with distinct advantages and disadvantages catering to specific

applications. Successive Approximation Register (SAR) ADCs, in particular, have garnered significant attention due to their suitability for high-speed and low-power applications [7, 13]. SAR ADCs operate by iteratively approximating the input voltage with a digital code, rendering them inherently fast and efficient. Their simplicity in architecture and ability to achieve high resolution make SAR ADCs favorable for applications where speed and precision are paramount. However, these advantages are counterbalanced by their susceptibility to noise and complexity in scaling to higher resolutions. Other types of ADCs, such as Delta-Sigma and Flash, offer unique attributes such as enhanced resolution and speed, respectively. Delta-Sigma ADCs excel in achieving high resolutions, especially in low-frequency applications, but are often slower compared to SAR ADCs [5]. On the other hand, Flash ADCs are renowned for their speed but can be power-hungry and complex, limiting their use in certain low-power applications [4]. This paper investigates the optimal comparator design (theoretically) by underscoring the performance characteristics and trade-offs between varions designs through a comprehensive analysis of the different comparator blocks used in SAR ADCs.

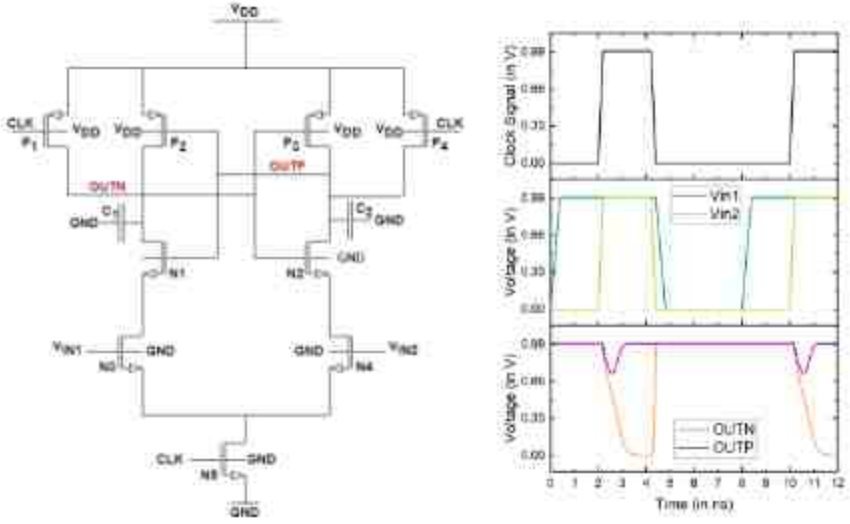
In 1992, T. Kobayashi et al. introduced an efficient ARM latch comparator utilizing 0.7μm CMOS technology, consisting of five NMOS and four PMOS transistors [9]. It finds applications in memory bit-line detection, A/D conversion, and wireline reception, serving as a robust latch with high sensitivity. Dynamic pre-amplifiers have gained popularity for their energy efficiency, prompting the exploration of modified comparator architectures to enhance performance parameters. A double-tail latch-type architecture was later introduced, incorporating two-tail transistors to improve common-mode rejection and reduce offset voltages, beneficial for low-voltage operations [11]. However, optimizing energy consumption for a given signal-to-noise ratio (SNR) remained challenging. The Modified Double Tail Comparator addressed this by adding two control transistors to the first stage, significantly reducing delay time while maintaining low power and fast operation [2]. Further evolution led to modifications by Elzakkar to achieve enhanced gain and reduced comparator noise and offset. This design achieved energy savings by reducing pre-charge energy and resulted in a 50 percent reduction in energy consumption [6]. Inspired by Elzakkar's work, Harijot Singh Bindra proposed a novel comparator design in 2018, featuring dynamic biasing and a tail capacitor to reduce energy consumption and delay [3].

The subsequent sections of this paper are organized as follows: Section 2 presents the working and schematic diagrams of conventional comparator architectures. Section 3 discusses the Double-Tail Comparator, while Section 4 delves into the Modified Double-Tail Comparator. In Section 5, the Elzakker comparator is examined, and Section 6 explores the Modified Elzakker. A performance comparison of these state-of-the-art architectures is provided in Section 7, followed by the Conclusion and Future Scope in Section 8.

2 Conventional Comparator

In the conventional comparator architecture, as shown in Fig. 1(a), in the absence of an active clock signal, the cross-coupled CMOS pre-charges OUTN and OUTP to the supply voltage (V_{DD}), leading to the deactivation of PMOS transistors P2 and P3 and the activation of NMOS transistors N1 and N2 [8].

A pulsating clock signal is subsequently applied to the circuit. The inputs to be compared are introduced at N3 and N4, with N5 establishing a connection between these NMOS and the ground. P2, N1, P3, and N2 collectively form a cross-coupled CMOS structure.



((a)) ((b))

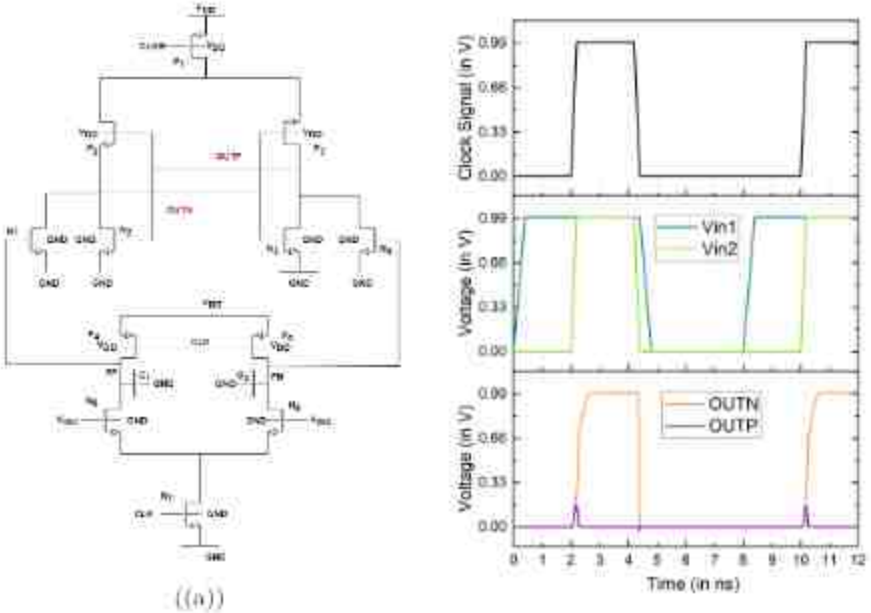
Fig. 1: Conventional Comparator (a) Schematic Diagram (b) Transient Analysis for V_{DD} = 1 V.

Upon the transition of the clock signal to a high logic state, P1 and P4 are turned off, while N5 is turned on. Initially, NMOS transistors N1 and N2 are activated, causing their source terminals to be charged to V_{DD} through OUTN and OUTP. In the scenario where Vin1>Vin2, OUTN discharges more rapidly than OUTP. Consequently, OUTN triggers the activation of P3, forcing OUTP to reach the V_{DD} level. As a result, the OUTN node assumes a logic low state, while the OUTP node attains a logic high state at the V_{DD} level [12]. This has been validated through the transient analysis depicted in Fig. 1(b).

3 Double Tail Comparator

In the double-tail comparator architecture, as shown in Fig. 2(a), the incorporation of two tail transistors (P1 and N7) is pivotal[11]. The inputs for comparison, designated as Vin1 and Vin2, are directed to N5 and N6 transistors. A pulsating clock signal is systematically applied to N7, serving as the timing reference for the circuit, while an inverse clock signal (ClkB) is concurrently applied to the complementary tail transistor (P1).

During a logic-low state of the clock, both tail transistors are deactivated. The clock signal activates transistors P4 and P5, resulting in the charging of nodes Fn and Fp to the supply voltage (V_{DD}). This action, in turn, activates N1 and N4 transistors. Subsequently, these transistors, when activated, pull down the output nodes, OUTN and OUTP, to the ground level. Simultaneously, P2 and P3 transistors are turned on.



((a)) ((b))

Fig. 2: Double Tail Comparator (a) Schematic Diagram (b) Transient Analysis for $V_{DD} = 1$ V.

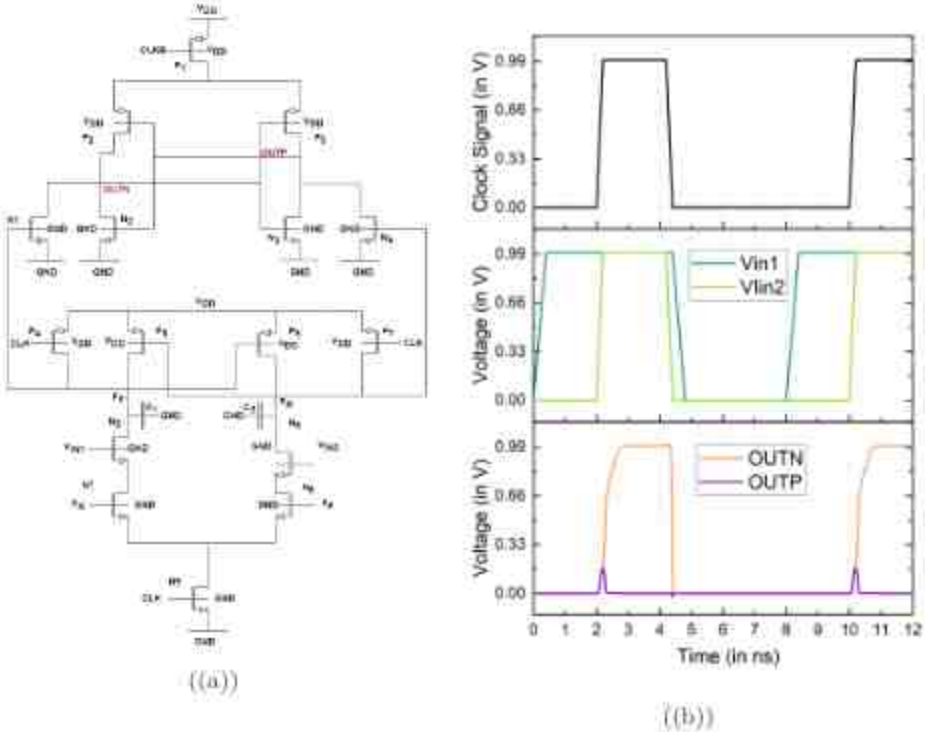
Upon transition to a high logic level of the clock, P4 and P5 are deactivated, and the tail transistors (P1 and N7) are activated [8]. This initiates the charging process of OUTN and OUTP. Both output nodes, OUTN and OUTP, possess

two discharging paths (OUTN through N1 and N2, while OUTP through N3 and N4).

In cases where Vin1>Vin2, Fp undergoes faster discharge than Fn. Consequently, N1 is switched off more rapidly, eliminating one discharging path for OUTN, while OUTP still retains two discharging paths. Consequently, OUTP reaches the ground state first. Upon achieving a ground state, P2 is activated, redirecting the charging of OUTN to V_{DD} instead of ground. Consequently, the OUTP node assumes a logic low state, while the OUTN node charges to the V_{DD} level [1]. The same is validated through the transient analysis depicted in Fig. 2(b).

4 Modified Double Tail Comparator

In the modified double-tail architecture, as shown in Fig. 3(a), the input and clock signal configurations mirror those of the conventional double-tail architecture. Consequently, during the initial phase, the operation aligns, with Fn



((a)) ((b))

Fig. 3: Modified Double Tail Comparator (a) Schematic Diagram (b) Transient Analysis for $V_{DD} = 1$ V.

and Fp nodes charged to V_{DD} while OUTN and OUTP are pulled down to the ground. Upon activation of the clock and simultaneous switching on of both tail transistors, OUTN and OUTP undergo charging to V_{DD} (facilitated by P2 and P3). Simultaneously, as P4 and P7 are turned off, the discharging process commences for Fp and Fn nodes.

When Vin1>Vin2, Fp experiences a significantly faster discharge rate than Fn. Consequently, N7 and P6 are activated, while N8 and P5 are deactivated. The activation of N7 establishes a low-resistance path, expediting the discharge of Fp. Simultaneously, by deactivating P5, Fp is permitted to discharge completely. This reduction in response time leads to decreased delay but increased power dissipation, distinguishing the modified architecture through the inclusion of the transistors P5, P6, N7, and N8.

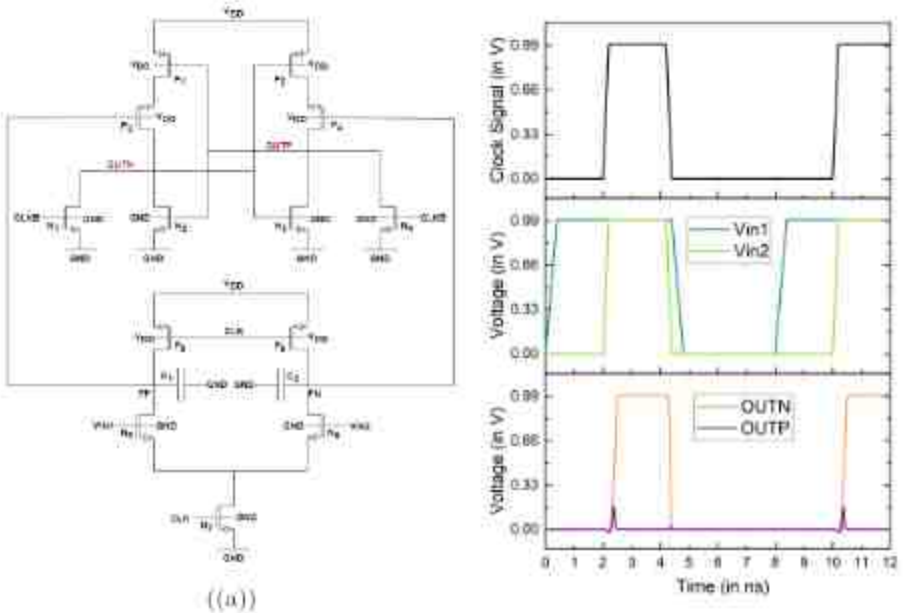
Following the discharge of Fp, N1 deactivates, diminishing the discharging paths for OUTN relative to OUTP. As a result, OUTP promptly pulls down to the ground, activating P2. This transistor, in turn, pulls up OUTN to V_{DD} before it reaches the ground. Consequently, OUTN achieves a V_{DD} level, while OUTP attains a logic low level. This has been validated through the transient analysis depicted in Fig. 3(b). This mechanism contributes to the operational characteristics that define the distinctive features of the modified double-tail architecture [2].

5 Elzakker Comparator

In the context of the elzakker architecture, as depicted in Fig. 4(a), the pulsating clock signal is applied to transistors P5 and P6, while the inverse of the clock signal is directed to transistors N1 and N4. The input signals Vin1 and Vin2, subject to comparison, are introduced to transistors N5 and N6 [6].

In the absence of an active clock signal, P5 and P6 are activated, leading to the charging of nodes Fp and Fn to V_{DD}. Simultaneously, this action precharges capacitors C1 and C2. The charged state of nodes Fp and Fn results in the deactivation of transistors P3 and P4. Concomitantly, transistors N1 and N4 are turned on by the inverse clock signal at their gate terminals, pulling down OUTN and OUTP to the ground. This, in turn, activates transistors P1 and P2.

Upon the clock assuming a logic high level, P5, P6, N1, and N4 are deactivated. Consequently, capacitors C1 and C2, along with nodes Fp and Fn, initiate the discharge process. When Vin1 surpasses Vin2, C1 and Fp discharge more rapidly than Fn. This leads to the activation of transistor P3 before P4. Upon P3 activation, OUTN is pulled up to V_{DD}, facilitated by the presence of P1. Once OUTN reaches V_{DD}, P2 deactivates before OUTP can attain V_{DD}, resulting in OUTN achieving a V_{DD} level while OUTP attains a logic low level. This has been validated through the transient analysis depicted in Fig. 4(b). This mechanism underscores the operational dynamics inherent in the elzakker architecture.



((a)) ((b))

Fig. 4: Elzakker Comparator (a) Schematic Diagram (b) Transient Analysis for $V_{DD} = 1$ V.

6 Modified Elzakker Comparator

In the modified Elzakker circuit, as shown in Fig. 5(a), a single enhancement has been implemented by introducing an NMOS transistor labeled M8, which operates with an inverted clock signal at its gate, along with the incorporation of a 20F capacitor named C3 [3]. The primary advantage of this modification lies in preventing unnecessary charging.

When Vin1 exceeds Vin2, akin to the conventional Elzakker circuit, Fp and C1 discharge more rapidly. However, instead of fully discharging the capacitor to zero, the charge is distributed between C1 and the newly added C3. This leads to a reduction in delay when the capacitor undergoes recharging in the subsequent clock cycle. This has been validated through the transient analysis depicted in Fig. 5(b). Furthermore, the presence of transistor N8 plays a crucial role in conserving both static and dynamic power, distinguishing it from the original Elzakker circuit. This straightforward adjustment proves effective in minimizing charging inefficiencies and optimizing power utilization.

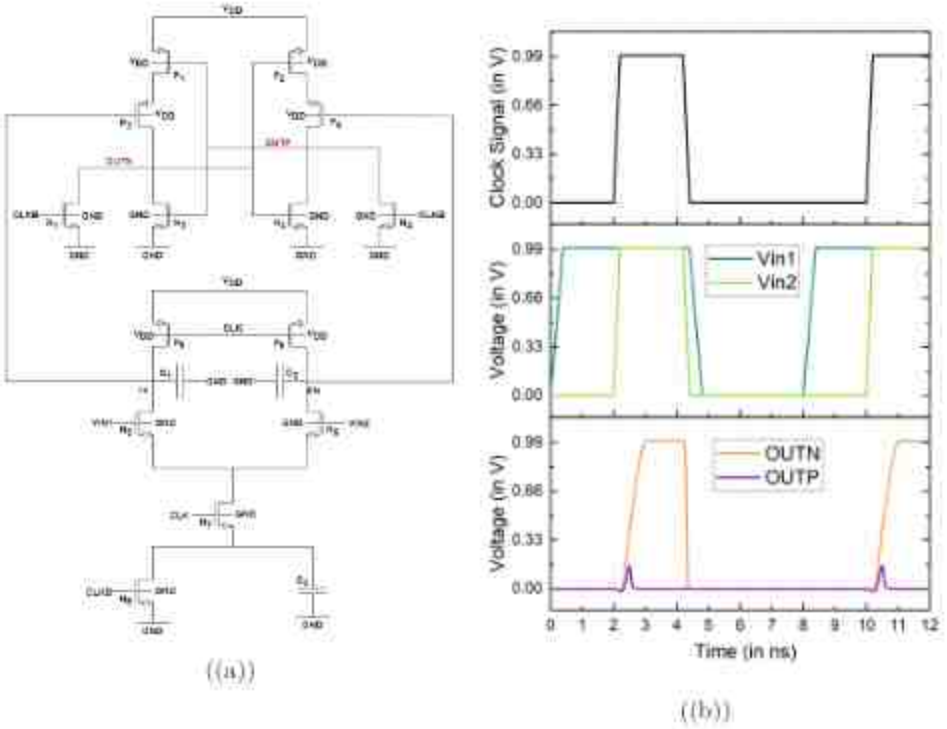


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Fig. 5: Modified Elzakker Comparator (a) Schematic Diagram (b) Transient Analysis for $V_{DD} = 1$ V.

7 Performance Analysis

In this comprehensive analysis, the performance metrics of five architectures of the comparator block of Successive Approximation Register Analog-to-Digital Converter (SAR ADC): Conventional Comparator, Double Tail Comparator, Modified Double Tail Comparator, Elzakker Comparator, and Modified Elzakker Comparator are systematically evaluated and compared in Table 1. Implemented on a 45 nm CMOS technology node, the architectures are scrutinized across various critical parameters like power dissipation and propagation delay using LTSpice software with a temperature of 27 ^{0}C.

The Modified Elzakker Comparator achieves the lowest static power dissipation at 34.891 nW, representing a 37.4% decrease compared to the Conventional Comparator. The Double Tail Comparator demonstrates the highest dynamic power dissipation at 42.1675 μW, showcasing a 119% increase compared to the Modified Elzakker Comparator, which records the lowest dynamic power dissipation. The Modified Elzakker Comparator outperforms others with a total energy

dissipation of 19.54 fJ, exhibiting a 65.4% and 65.8% reduction compared to the Conventional and Double Tail Comparators, respectively.

Table 1: Performance metrics of the State-of-the-Art Architectures of SAR ADC at temperature = 27 °C

Parameters	Conventional	Double Tail	M. Double Tail	Elzakker	M. Elzakker
CMOS Technology (nm)	45	45	45	45	45
Supply Voltage (V)	1	1	1	1	1
Static Power (nW)	27.932	35.436	62.07	41.577	34.891
Dynamic Power (μW)	16.0845	42.1675	29.237	46.5705	11.49595
Total Energy (fJ)	23.191	56.601	47.397	46.244	19.54
Time Delay (ps)	284.959	109.23	125.365	167.693	237.091
Min. Op. Voltage (V)	0.8	0.4	0.4	0.7	0.8
Max. Freq. (GHz)	0.303	1.538	1.315	1	0.769

The Double Tail Comparator exhibits the lowest time delay at 109.23 ps, showcasing a 61.7% reduction compared to the Conventional Comparator. The Modified Elzakker Comparator, with a time delay of 237.091 ps, reflects a 17.0% increase compared to the Double Tail Comparator. Both the Double Tail and Modified Double Tail Comparators operate at 0.4 V, showcasing a 50% reduction compared to the 0.8 V minimum operating voltage of the Conventional and Modified Elzakker Comparators. The Modified Double Tail Comparator demonstrates the highest maximum sampling frequency at 1.538 GHz, representing a 407% increase compared to the Conventional Comparator. The Modified Elzakker Comparator, with a maximum sampling frequency of 769 MHz, showcases a 59.6% reduction compared to the Modified Double Tail Comparator.

The Total Energy Dissipation (in femtojoules, fJ) for five comparator architectures increases with V_{DD}, showcasing a direct correlation as shown in Fig. 6(a). Notably, the Modified Elzakker Comparator consistently demonstrates superior efficiency, ranging from 10.01 fJ at 0.8V to 31.723 fJ at 1.2V, positioning it as a more power-efficient choice across the voltage spectrum. Fig. 6(b) illustrates the time delay (in picoseconds, ps) of five comparator architectures at various power supply voltages (V_{DD}). A technical analysis reveals an inverse relationship between V_{DD} and time delay, where an increase in V_{DD} results in decreased delay. The Double Tail and Modified Double Tail show lower time delays (84.2096 ps and 95.4026 ps, respectively, at 1.2V), suggesting a comparatively faster response. The static power dissipation (in nanowatts, nW) across different power supply voltages (V_{DD}) reveals a consistent increase in static power dissipation with rising V_{DD} according to Fig. 6(c). At lower (V_{DD} levels, the Modified Elzakkar Comparator exhibits lower static power (14.667 nW at 0.8V) compared to others; however, as V_{DD} further increases, the conventional

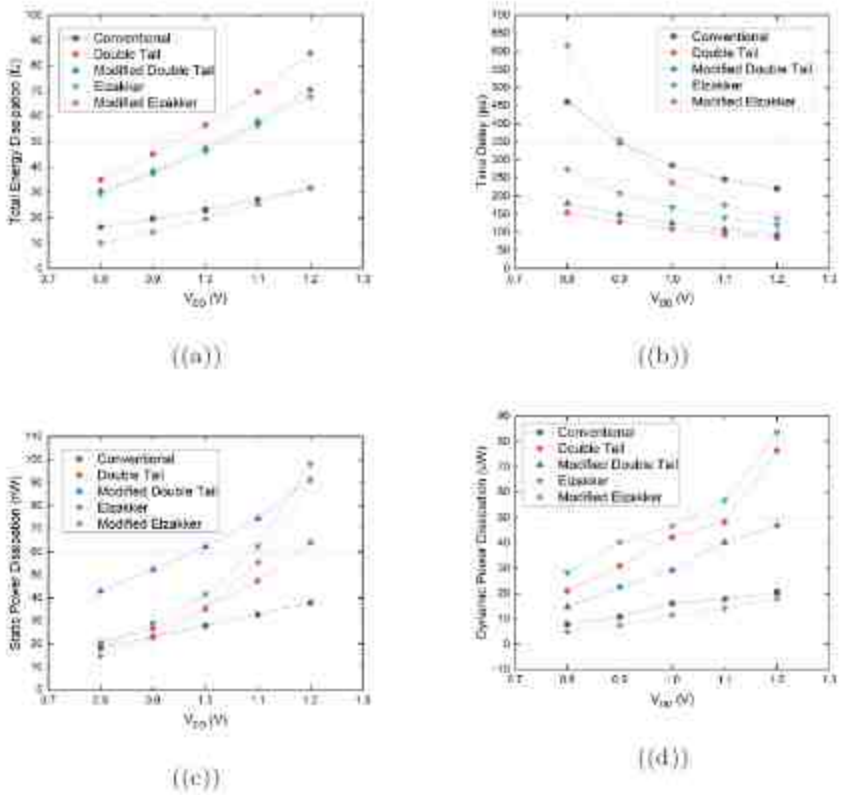

Fig. 6: Parametric comparison of different comparator architectures across different supply voltages (V_{DD}) (a) Total Energy Dissipation (b) Time Delay (c) Static Power Dissipation (d) Dynamic Power Dissipation.

comparator starts to display the lowest static power (37.784 nW at 1.2V). Fig. 6(d) depicts that as V_{DD} increases, dynamic power dissipation generally rises. The Modified Elzakker Comparator consistently outperforms others, with the lowest power consumption across all voltages, ranging from 4.9533 μW at 0.8 V to 18.146 μW at 1.2 V. In contrast, the conventional comparator starts at 7.7697 μW and reaches 20.9455 μW at the same voltage levels, demonstrating a steady increase in power consumption with higher V_{DD}.

8 Conclusion and Future Scope

The selection of the appropriate Successive Approximation Register Analog-to-Digital Converter (SAR ADC) comparator architecture is crucial and depends on the specific demands of the target application. In this comparative analysis across various parameters in the context of 45 nm CMOS technology, it becomes

evident that different SAR ADC architectures exhibit distinct strengths and weaknesses.

Given considerations of static and dynamic power consumption, energy dissipation, and time delay, the Modified Elzakker Comparator emerges as a compelling choice for energy-efficient applications. Its distinctive design elements contribute to significant reductions in both static and dynamic power, making it an ideal solution for scenarios with stringent power constraints. Conversely, the Modified Double Tail Comparator excels in high-speed operations due to its efficient comparison process, making it suitable for applications requiring rapid data conversion.

The study's potential limitations involve its narrow focus on specific comparator architectures and technology nodes, possibly overlooking alternative designs and newer processes. Simplified metrics may overlook important performance aspects, and the study's scope may not encompass all application scenarios. Practical implementation factors could impact real-world performance differently than anticipated. Future research directions include exploring advanced process technologies, integrating comparators into SoC designs, optimizing for low-power and high-speed applications, and investigating mixed-signal integration and reliability enhancement, potentially uncovering novel architectures to enhance analog-to-digital conversion efficiency.

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