An Enhancement Mode Double T- Gate Field Plate GaN HEMT for power electronics application

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***Abstract*— In this report, we have proposed and investigated p-GaN HEMT for improved performance. The proposed device utilises a double T-field plate at the gate electrode of the proposed device to reduce electric field near the drain edge of the gate. The reduction in electric field enhances the breakdown voltage (BV) of the proposed device which is suitable for high power electronics application. The simulation findings were validated by calibrating the device models with experimental results. Also, the study includes a comparative analysis exhibiting superior DC characteristics, such as enhanced on-current, maximum drain current, high BV, low gate leakage current and elevated transconductance in contrast to conventional T-Field plate HEMTs. Moreover, the fabrication process for our device has been outlined, accompanied by optimization efforts aimed to achieving peak performance, particularly focusing on BV. Additionally, a comparative analysis with existing state-of-the-art devices has been conducted to evaluate the superiority of our device.**

Keywords—HEMT, Field plate, Electric field, Breakdown voltage, Gate leakage

I. Introduction

HEMTs were developed to meet the increasing need for fast switching, high power, and low-noise performance [1][2]. GaN based HEMTs are commonly used as high-power, high-frequency devices due to their excellent characteristics, such as high BV, on-current, and fast switching [3]. The primary objectives in power device research center around attaining elevated BVs.

Several studies have been also reported to enhance the HEMT's performance. The AlGaN/GaN HEMT, designed for high-power applications and featuring a field plate, has been investigated for its performance characteristics. Chitransh et al. [4] presented a peak drain current of 3 A/mm. In addition, the introduction of parasitic capacitances due to SiN_x passivation and sensitivity to gate bias are reported. However, both affecting device accuracy and practical application. Kabemura et al. [5] explored the breakdown characteristics in field-plate AlGaN/GaN HEMT with a high-k passivation layer, comparing results with SiN passivation. The findings indicate improved BV with short field plates and high-k layers, suggesting potential applications in power switches. However, challenges in evaluating fringing capacitance in high-k dielectric applications are highlighted. Fletcher et al. [6] proposed a discrete field plate technique to enhance the BV and RF performance of AlGaN/GaN HEMTs. They have achieved a BV of 330 V and a cut-off frequency of 20 GHz. Although their finding not validated with experimental results.

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Chander et al. [7] reported a T field plate to enhance the BV. Using of T field plate gate structure, the peak electric field is decreased at gate edge by spreading the electric field on drain/source side. As a result, increased BV obtained of 950 V. Despite that potential impact on parasitic capacitances and device thermal performance was not presented in their work.

To address these drawbacks, a novel Double T-Field plate HEMT (DT-FPHEMT) has been proposed and investigated to improve the overall performance of the device. In the proposed device, a double T-field plate has been introduced to improve the gate leakage current which enhances BV of the proposed device. Also, the proposed device achieves improvement in on-current, maximum drain current, and high transconductance (g_m) as compared to the conventional T-Field plate HEMT [7]. During the calibration process of device models, experimental results were used to confirm the precision of simulation outcomes. The process flow has been proposed to make the Double T-field-HEMT, Furthermore, a comparison has been presented between the proposed DT-FPHEMT and reported devices, considering various performance metrics.

II. Device, Simulation and Calibration

Fig. 1(a) displays the structure of conventional T-field plate HEMTs, while Fig. 1(b) illustrates the proposed Double T-field plate configuration. Two T-field plates have been incorporated in the proposed device at the gate region. Table 1 presents the parameters of the proposed device. The proposed DT-FPHEMT device employs the layers including a 3.4 µm field plate length with thickness of 100 nm, source to field plate length of 2 µm, drain to field plate length 3 µm. SiN passivation layer length in left side 3 µm and right side 4 µm. The Al content for the AlGaN barrier layer is fixed at 0.2 whereas the Mg doping of the p-GaN layer is $3 \times 10^{17} cm^{-3}$.

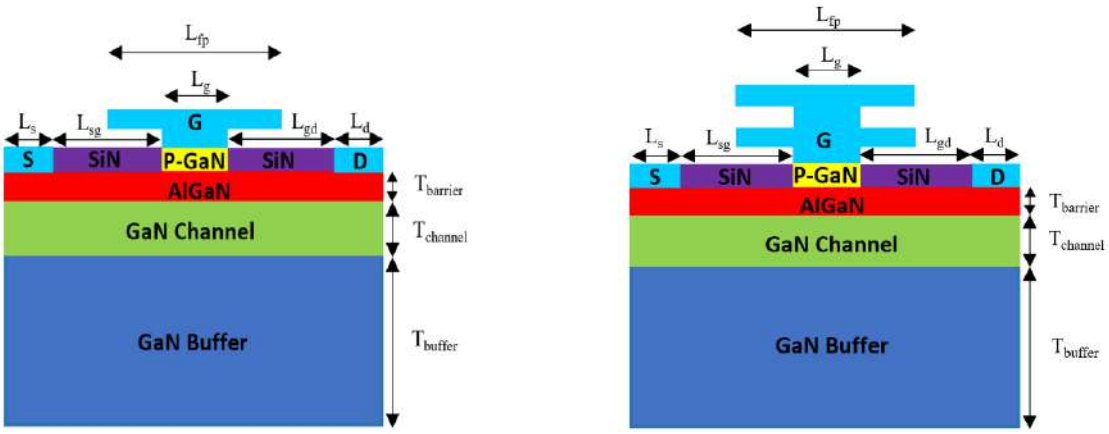

Fig. 1. The structure of (a) Conventional T-Field plate HEMT and (b) The Proposed DT-Field Plate HEMT

Table 1
The parameters of the DT-Field Plate HEMT.

Parameters	Unit	Value	Description
L_s	µm	1	Source electrode length
L_d	µm	1	Drain electrode length
L_g	µm	1.4	Gate electrode length
L_{GaN}	µm	2	GaN channel length
L_{sg}	µm	3	Gate to source distance
L_{gd}	µm	4	Gate to drain distance
$T_{p\text{-}GaN}$	nm	110	p-GaN layer thickness
$T_{barrier}$	nm	15	AlGaN barrier thickness
T_{SiN}	nm	300	SiN Passivation thickness
T_{GaN}	nm	85	GaN channel layer thickness
T_{GaN}	µm	2	GaN buffer layer thickness

SILVACO tool is utilized for calibrating and of the simulating devices. Calibration is crucial for verifying the accuracy and relevance of the simulation methods and models utilized to analyze the device. As a result, the simulation methods and models are to calibrate the experimental data.

The conventional p-GaN HEMT has been calibrated by taking into account the structural parameters, which include a p-GaN layer of 110 nm thickness, a $Al_{0.26}Ga_{0.74}N$ barrier layer of 15 nm, a GaN channel layer of 85 nm, and a $Al_{0.25}Ga_{0.75}N$ buffer layer of 2µm [8] Fig. 2 illustrates the transfer characteristics of p-GaN HEMT through a comparison of experimental and simulated data. The graphical representation demonstrates a high level of accuracy in the fitting between the simulated results and the experimental data. This alignment serves as confirmation of the reliability and precision of the simulation models employed in the analysis.

In the simulation, various models are employed to capture the behavior of the p-GaN HEMT accurately. The SRH model is used to account carrier generation and recombination, while the GaN polarization model considers the impact of polarization effects. The Fermi–Dirac model is employed for Fermi statistics, and both high-field and low-field mobility models are incorporated for mobility considerations. Additionally, the impact ionization model, specifically the Toyabe model, is applied to capture nonlocal impact ionization effects. The carrier transport in the channel is represented using the drift-diffusion transport model, which is grounded in Boltzmann transport theory. Models such as Gansat, a nitride mobility model and Albrecht for saturation velocity, are also integrated into the simulations to provide a comprehensive understanding of the device characteristics.

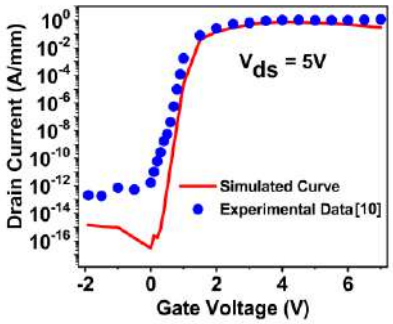

Fig. 2. Calibration of the transfer characteristics for conventional p-GaN HEMT

III. Proposed Fabrication Steps of the DT-FP HEMT

The proposed device can be manufactured through a CMOS-compatible process flow, as illustrated in the accompanying Fig. 3(a)-Fig. 3(e). The GaN channel layer and the AlGaN barrier layer are grown over the GaN buffer through MOCVD as depicted in the Fig. 3(b). The epitaxial structure of the p-GaN HEMT with a GaN buffer is cultivated using metal-organic chemical vapor deposition (MOCVD), as indicated in

the Fig. 3(c) [8][9]. The SiN passivation layer is deposited using PECVD, as shown in Fig. 3(d). Following this, the process involves selectively etching a p-GaN layer using plasma, followed by the deposition of ohmic contacts using electron beam evaporation and shaping the Double T structure, as illustrated in Figure Fig. 3(e).

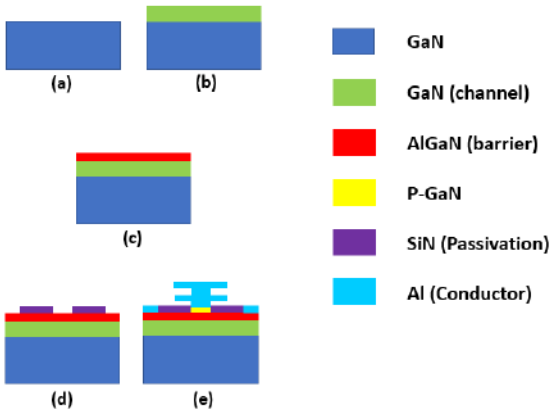

Fig. 3. Fabrication steps for the proposed DT-FPHEMT (a) Starting as buffer (b) Growth of channel layer (c) Growth of barrier layer (d) plasma-enhanced chemical vapor deposition of SiN. (e) Plasma etching of p-GaN layer and attaching conductor using electron beam

IV. Results and Discussion

In this section, we have examined the DC characteristics of both the conventional T-FPHEMT and the proposed DT-FPHEMT like on-current, maximum drain current, transconductance, gate leakage, and BV. Also, we have conducted optimization for the proposed device by adjusting the field plate length to attain the best possible performance.

4.1. Comparison of the DC characteristics of conventional T-FPHEMT and the proposed DT-FPHEMT

Due to the presence of T-field plate gate, the electric field is reduced in channel, because field plate distributes the electric field over the channel layer [7]. The introduction of an additional T field plate further decreases electric field as depicted in the Fig. 4. Hence, the electric field in the channel is lower for DT-FPHEMT compared to T-FPHEMT.

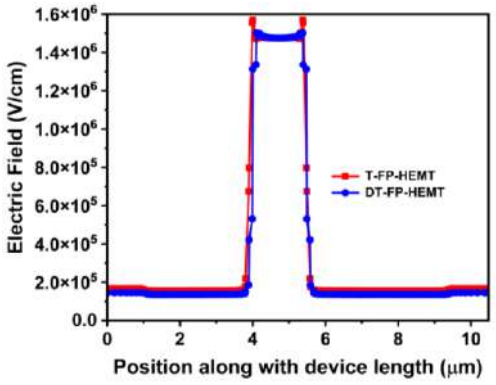

Fig. 4. Electric field distribution over channel of T-FPHEMT and DT-FPHEMT

Fig.5(a) and Fig.5(b) depicts the I_d-V_d and I_d-V_g characteristics, respectively, for the proposed and conventional device. The I_d-V_d characteristics, reveals that the DT-FPHEMT device achieves a maximum drain current ($I_{ds,max}$) at 0.0461 A/mm, in contrast to the T-FPHEMT's 0.0375 A/mm at constant gate-source voltage (Vgs) of 8V. The I_d-V_g characteristics shows the improved drain current for the DT-FPHEMT as compared to the conventional device. The enhancement of drain current is due to a decrease in the electric field within the channel area is primarily attributed to two factors improved carrier mobility and enhanced stability of the two-dimensional electron gas (2-DEG). The Low electric field result in reduced scattering of charge carriers, particularly electrons, enabling them to traverse the channel more efficiently, thus enhancing carrier mobility. In Addition, a more stable and denser 2-DEG, facilitated by the lower electric fields, ensures a consistent supply of electrons for conduction, further enhancing the drain current.

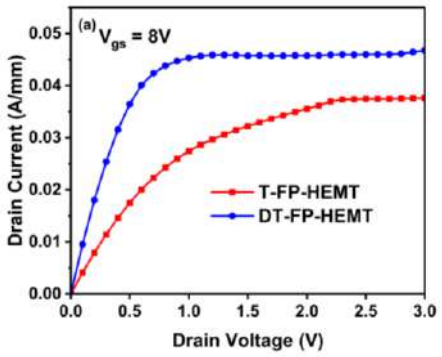

Fig. 5 (a). Output characteristics of T-FPHEMT and DT-FPHEMT

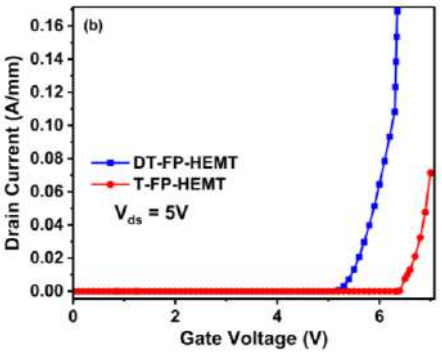

Fig. 5 (b). Transfer Characteristics of T-FPHEMT and DT-FPHEMT

Fig. 6 presents the transconductance (g_m) for both T-FPHEMT and the proposed DT-FPHEMT. The increase in g_m with a reduction in electric field in the channel area of AlGaN/GaN HEMT is primarily influenced by improved carrier mobility. As the electric field decreases, carriers experience less scattering, leading to enhanced mobility. This enhanced mobility results in a more efficient transfer of charge carriers in the channel, contributing to higher g_m. As the drain current rises due to less gate electric field, the g_m consistently

shows an upward trend [10]. Consequently, it is evident that the g_m of DT-FPHEMT surpasses that of T-FPHEMT. Specifically, the g_m value for DT-FPHEMT is 613 mS/mm, while T-FPHEMT records a value of 378 mS/mm.

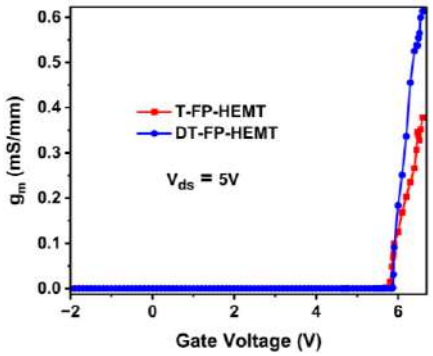

Fig. 6. The g_m of T-FPHEMT and DT-FPHEMT

Fig. 7 presents the gate leakage for the both T-FPHEMT and the proposed DT-FPHEMT. The reduction in gate leakage in AlGaN/GaN HEMTs due to a lower electric field in the channel area is related to the impact of electric field on carrier transport and tunneling phenomena. Gate leakage in a transistor is often associated with carriers tunneling through the gate dielectric. When the electric field in the channel area is reduced, carriers experience less energy, making it less likely for them to tunnel through the gate dielectric. Lowering the electric field diminishes the probability of carriers gaining enough energy to overcome the potential barrier of the gate dielectric, thereby reducing gate leakage. In summary, less electric field in the channel area lowers the energy of carriers, decreasing the likelihood of tunneling through the gate dielectric and resulting in reduced gate leakage in AlGaN/GaN HEMTs. This is an important consideration for optimizing the performance and reliability of such devices. To suppress gate leakage current, the electric field surrounding the channel remains minimized due to the incorporation of a double field plate. As depicted in Fig. 7 the, DT-FPHEMT exhibits reduced gate leakage current compared to T-FPHEMT at a constant drain to source voltage of 13 V.

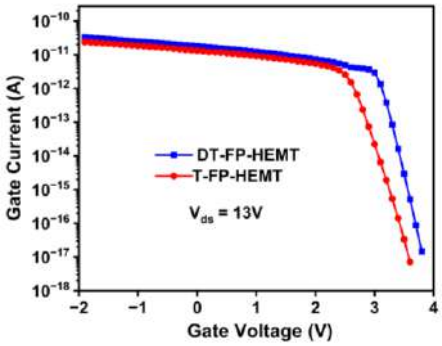

Fig. 7. Gate leakage current of T-FPHEMT and DT-FPHEMT

Fig. 8 presents the BV for the both T-FPHEMT and DT-FPHEMT. The BV in proposed device increases with a decrease in electric field in the channel area due to the interplay of two factors. Firstly, lower electric fields lead to enhanced carrier mobility, reducing the likelihood of carrier impact ionization and breakdown. Secondly, the formation of a 2-DEG gas at the AlGaN/GaN interface benefits from a more stable and dense electron population when the electric field is minimized. This effect of improved carrier mobility and a robust 2-DEG contributes to the overall increase in BV in the channel area of the device. This diminished electric field contributes to the higher BV observed in DT-FPHEMT, reaching 1700V, in contrast to the BV of 1400V for T-FPHEMT shown in Fig. 8 [7].

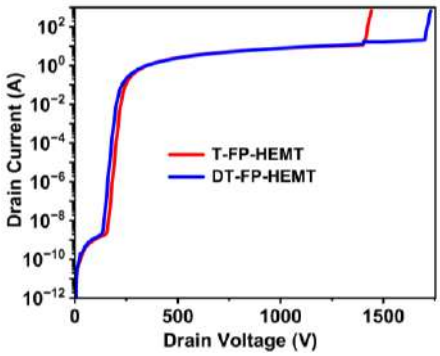

Fig. 8. BV of T-FPHEMT and DT-FPHEMT

4.2. Optimization of the device design parameters

Our study primarily focuses on assessing the power-handling capabilities and the BV of the proposed device. To enhance the BV, we optimized the length of the field plate [11]. Consequently, the BV of the DT-FPHEMT was measured with varying field plate lengths (2.6µm, 3µm, 3.4µm).

A maximum BV of 1700V was attained with a length of the double T-field plate set at 3.4µm. This enhanced BV is ascribed to the longer field plate, which demonstrates a reduced electric field strength in the gate channel compared to a shorter field plate, as depicted in Fig. 8. The BVs of the DT-FPHEMT with various Length field plate (L_{FP}) values are depicted in the corresponding Fig. 9. Table 2 shows the values of BV at different values of L_{FP}.

Table 2

The BV values corresponding to different (L_{FP}) are as follows:

L_{FP} (µm)	BV (V)
2.6	1500
3	1550
3.4	1700

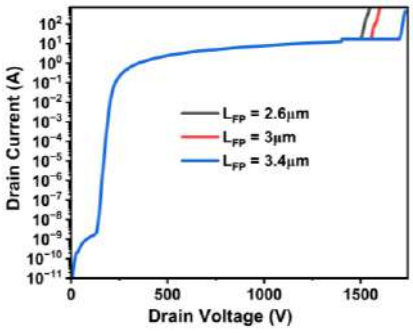

Fig. 9. Optimized BV of the DT-FPHEMT with different L_{FP}

Table 3 The comparison of the proposed DT-FPHEMT and the reported devices with respect to the overall performance.

Parameters	**Ref.** [6]	**Ref.** [12]	**Ref.** [13]	**T-FPHEMT**	**DT-FPHEMT**
BV (V)	330	98	562	1400	1700
$I_{d\ s,max}$ (A/mm)	-	1.6	0.8575	0.0375	0.0461
g_m (mS/mm)	275	400	305.6	378	613

Table 3 presents a comparison of the DC performance between our proposed structure and existing devices. This comparison highlights the enhancements in BV, drain current, and transconductance observed in our proposed device in comparison to previously reported devices.

V. Conclusion

In conclusion, the investigation presented a novel Double T-Field Plate HEMT (DT-FPHEMT) with notable improvements in key performances metrics such as BV, drain current and transconductance. The proposed DT-FPHEMT exhibits a remarkable improvement of 21% in the BV, 23% in the drain current and 62% in the transconductance (g_m). By focusing on optimizing the field plate length, we have further elevated the performance metrics, resulting in a notable achievement of a maximum BV of 1700 V at 3.4 µm. Consequently, the findings reported in this paper suggest the that the proposed DT-FPHEMT device has a potential for applications in power electronics.

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