New 14T Hybrid Full Adder: Minimizing Power and Maximizing Speed

Anurag Chauhan[1a], Chetan Batra[1b], Harish Tripathi[1c], and Himanshu Kumar[1d]
Department of ECE, Delhi Technological University, Delhi, India[1]
anuragchauhan@dtu.ac.in[1a]
chetanbat2001@gmail.com[1b]
harishtripathi_ec20b17_14@dtu.ac.in[1c]
hkkumar261@gmail.com[1d]

Abstract – Adder is a critical component of many digital systems and circuits, such as DSP processors, ALUs, and ASICs, that execute different various arithmetic operations. As the technologies scale down, the threshold voltage decreases, leading in increased power dissipation. This research introduces a 14T hybrid full adder and compares it with number of full adders with respect to power usage, signal latency, and power delay product (PDP). Both the existing circuits and the proposed design are built and tested under identical conditions, utilizing 90nm technology on Cadence Virtuoso. The comparison reveals that the proposed full adder improves the latency and PDP by 11.49% to 44.77% and 0.48% to 66.56%, respectively, hence making it appropriate for usage in speedy operations.

Keywords – Cadence Virtuoso, Full Adder, Less PDP, Low Delay

1 INTRODUCTION

In VLSI circuit designing it is the full adder that covers the majority of logical operations and with the advancement in circuit designing it becomes important to integrate a large number of functionalities in a small area [1]. Nowadays researchers are focusing on lowering the number of transistors beginning from the most basic standard CMOS circuit which has 28 Transistors. So far, several logic families have been investigated, including CMOS, pass-transistor-logic (PTL), transmission gate logic, and so on. Each design has its advantages and limitations, and all these architectures aim to enhance the different metrics of performance such as power usage, latency, PDP, and transistor count. There exists a conflict between power and signal latency; lowering the voltage results in less power but increases delay in the circuit. The equation (1) is used to theoretically calculate the static power loss [2]

$$P_s = I_C * V_{dd} \qquad (1)$$

Where I_c = Leakage Current, V_{dd} = Supply Voltage

CMOS-based full adders use a combination of pull-up and pull-down networks. The designs are very robust when it comes to noise and scalability [3]. It has some disadvantages also such as high input Capacitance. The second way to implement a full adder relies on PTL, it is one of the promising technologies as it reduces the number of transistors however it has to deal with the issue of voltage decline. To overcome these issues hybrid full adders are used, they are implemented using one or more than one logic family. With the help of three inputs (A, B, and Cin) a full adder produces 2 outputs (Sum and Cout). The truth-table for an adder is illustrated in table 1.

Table 1. Truth Table for Full Adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The primary objective of this paper is to design a 14T full adder using a hybrid approach which is implemented on Cadence Virtuoso using 90nm technology. This paper presents a comparative analysis of the presented design and the existing designs at the same conditions and it aims to minimize power consumption and increase circuit speed. The rising demand for high-speed and low-power arithmetic units in recent digital systems such as ALUs, DSP processors, and ASICs is the motivating factor for this work. As the technology nodes scale down the necessity for creating an efficient full adder that can work in low power and low delay also increases. The goal of this study is to enhance the performance parameters for the proposed design but it does not consider the issue of transistor count or area and in this study, no attempts are made to

reduce the number of transistors as compared to some existing circuits. Additionally, to verify the robustness of the circuit more testing across different environments is required [19].

2 RELATED WORKS

In the literature, various designs for full adders have been proposed using various methodologies. These designs differ in the number of transistors they use, their design pattern for creating internal nodes, and logic design methods techniques they employ. Changing some parameters may enhance the performance of few parameters while it might make others worsened. For comparing the performance, various 1-bit full adder's circuits are taken.

***Mahmood Rafiee**:*

Mahmood Rafiee full adder circuit, as depicted in fig. 1, consumes 23 transistors. The circuit utilizes a hybrid approach, dividing the circuit into three modules. Here, the first module consists of generating XOR (at the source of N4), XNOR (at the source of N5), and an AND gate (at the Drain of N2). The AND gate is producing the output A'B. The second module generates the Cout signal using six transistors (P4, P5, N7, N8, N9 and N10) and diverse input connections. It generates the Cout signal with a unique structure [15]. The sum logic is implemented by the third module, which consumes cascaded XOR/XNOR and a 2:1 MUX implemented using transmission gates. The circuit computes the sum by considering Cin as modules-2's selector, which connects the XOR and XNOR signals.

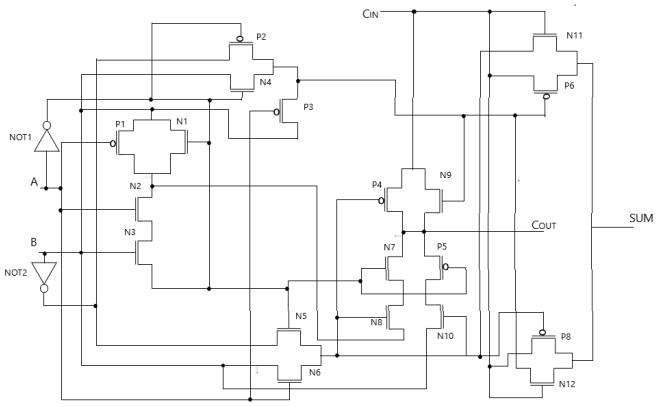


Fig. 1: Mahmood Rafiee Full Adder.

Mehedi Hassan

The full adder proposed by Mehedi Hasan, as shown in fig. 2, uses 4 modules for sum and carry generation. Two modules each generated carry and sum. The AND-OR outputs are produced by the initial module while the second employs a 2:1 MUX with transmission gates to have output carry either the AND or OR signal generated by Module-I based on the Cin signal (fig 2. (a)). The sum is generated using two XOR modules, that are constructed using transmission gates and pass transistors (fig. 2(b)) [16].

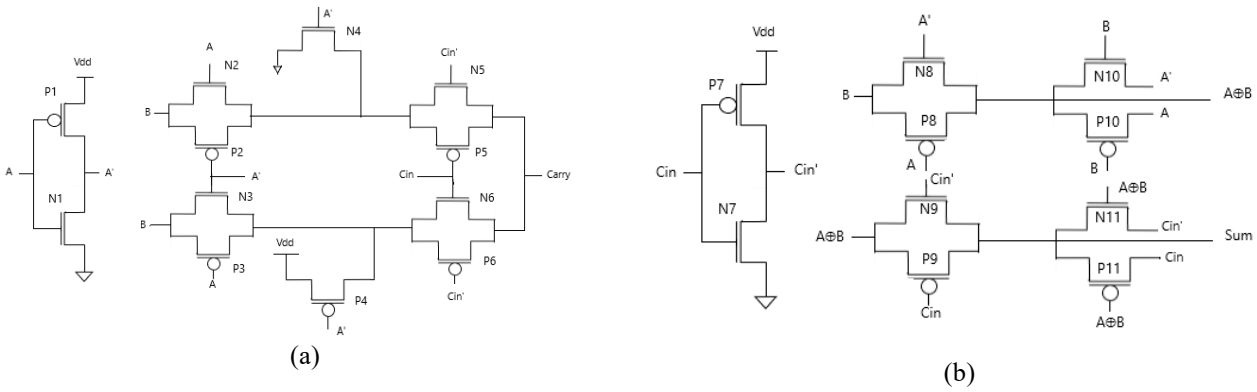


Fig. 2: Mehedi Hassan Full Adder. (a) Carry (Cout) Generation Circuit, (b) Sum Generation Circuit

Mark Vesterbacka model:

The full adder in fig. 3 uses three transmission gates in addition to a cross-coupled 6T XOR and XNOR circuit [4]. It works on the principle of complementary cross- coupled NMOS and a cross-coupled PMOS structure, the 6T XOR and XNOR design is utilized. The circuit's key feature is its feedback loops which reduce the threshold voltage loss.

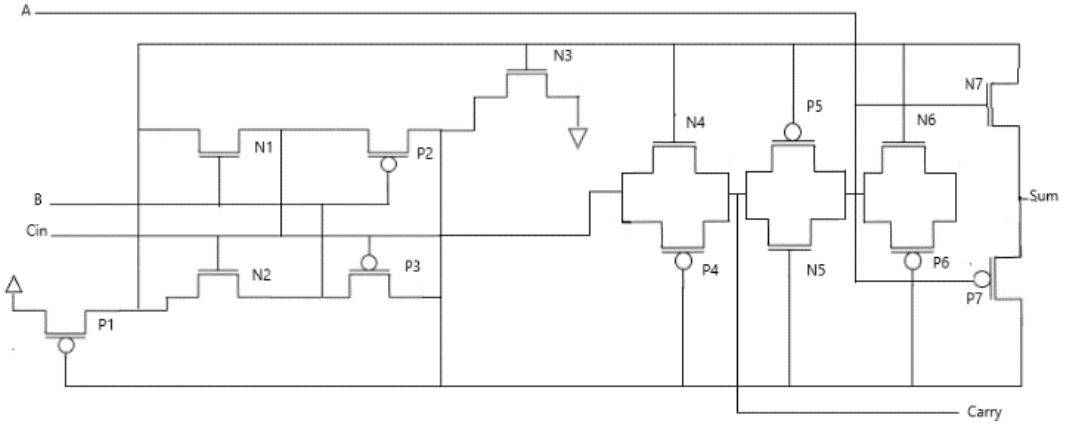


Fig.3: Mark Vesterbacka *Full* Adder.

***Abu-Shama model*:**

This full adder circuit depicted in fig. 4 [5] uses a new approach for XOR function. The new 4T XOR gate [11] generates the half sum, while the second half of the circuit uses transmission gate theory [11] to generate sum and carry out.

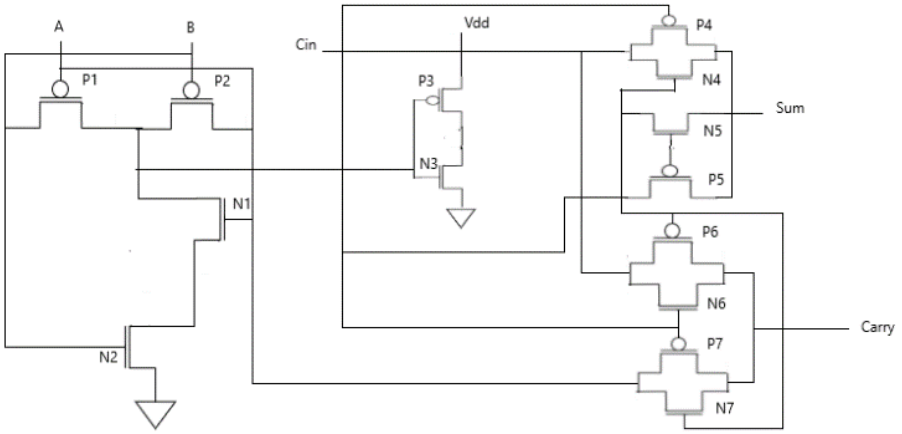


Fig. 4: Abu-Shama Full Adder.

Shahmini* Subramaniam *model:

With the help of six NMOS and four inverters a full adder circuit is constructed whose schematic is shown in fig. 5 [6]. High reliability and reduced load capacitance which in turn lowers the power usage and access time, is the advantage of this design. When all the inputs are set to high (or 1), it increases the access time which contributes to the disadvantage of this circuit.

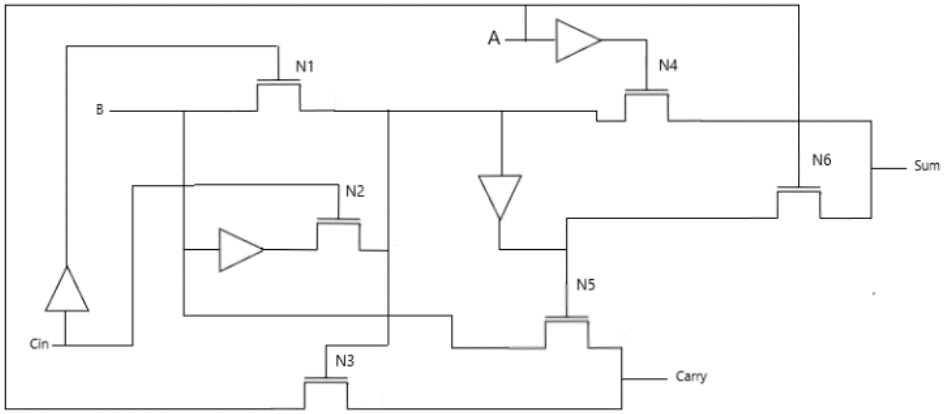


Fig. 5: Shamini Subramaniam Full Adder.

S.Narendra Model

This circuit uses 4T XOR design which fig.10 depicts. The circuit for the design is visible in fig. 6 [7]. The equation of sum is obtained by two transmission gates with inputs XNOR (XOR passed through a CMOS inverter), XNOR and B whereas the carry is implemented by using the 4T XOR circuit with inputs as Cin and XOR so obtained.

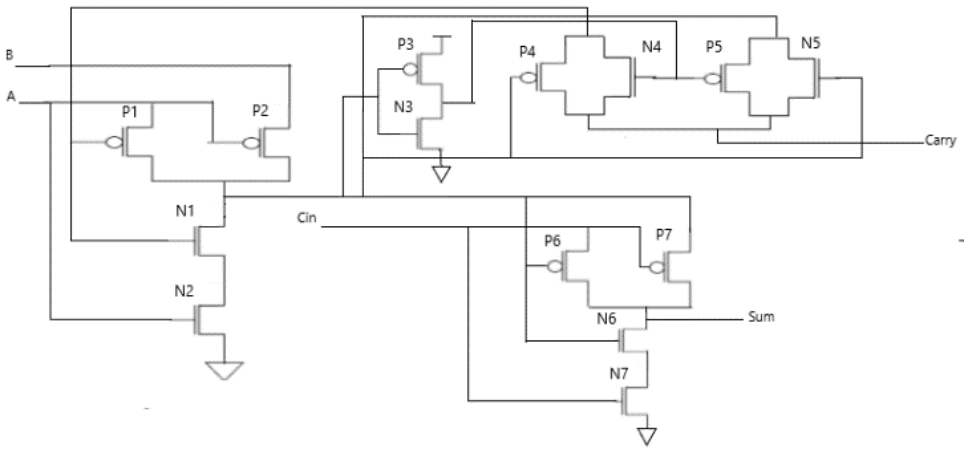


Fig. 6: S. Narendra Full Adder.

Paras Model

The entire full adder (fig. 7) circuit is constructed using twelve transistors [17]. The XOR/XNOR circuit is constructed using three PMOS (P1-P3) and three NMOS (N1-N3), a total of six transistors are used. The gate terminal of the P1 is responsible for generating XOR signal and the gate terminal of the N1 is responsible for generating XNOR signal. Two pass transistors namely P4 and N4 acts as pass gates generating the sum when provided input as Cin. Depending upon the circuit arrangement, the output can be same as input signal or complementary. The carry-out signal is generated using two transmission gates.

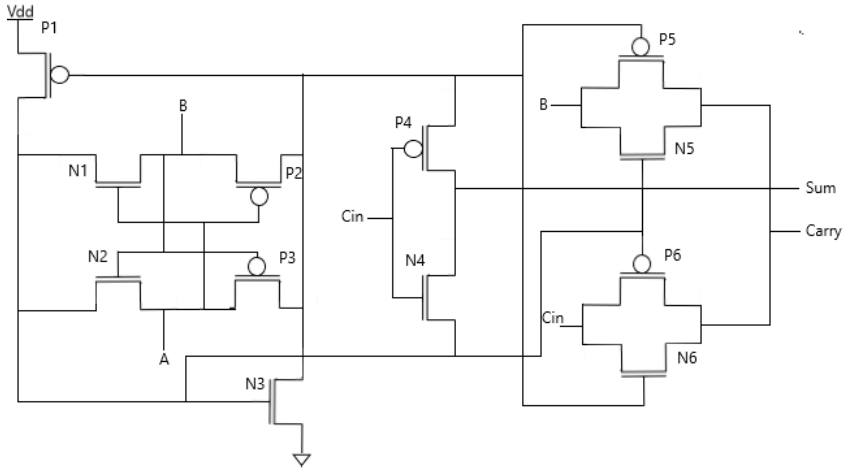


Fig. 7: Paras Full Adder.

Akshay Bhaskar Model

Ten transistors are used in the construction of this complete full adder [18], fig. 8 displays the schematic of the full adder. Two 4T XOR gates are used (P1, P2, N1, N2 and P3, N3, P4, N4) followed by a multiplexer (P5 and N5). The second XOR circuit generates a sum of the full adder and the multiplexer is responsible for producing carry (Cout).

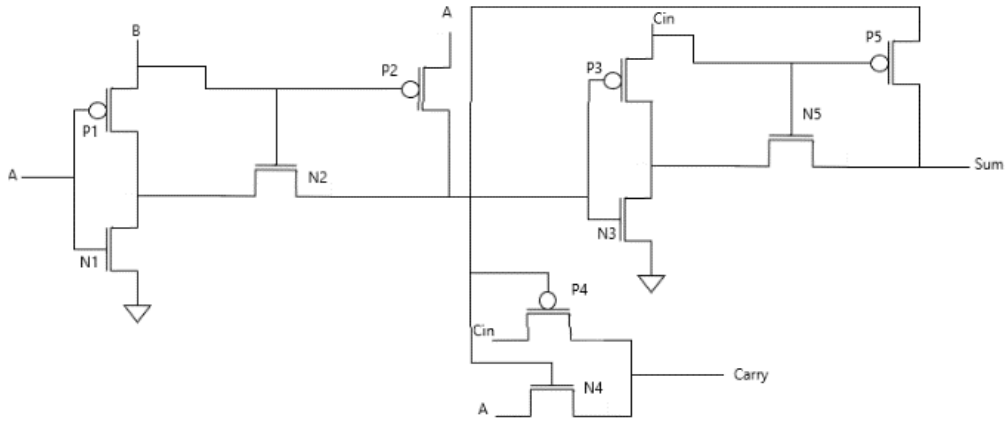
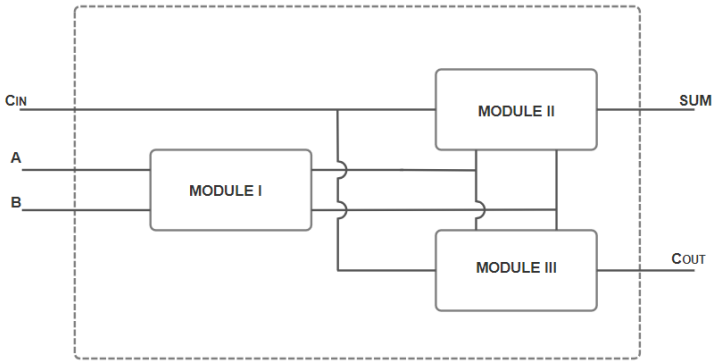


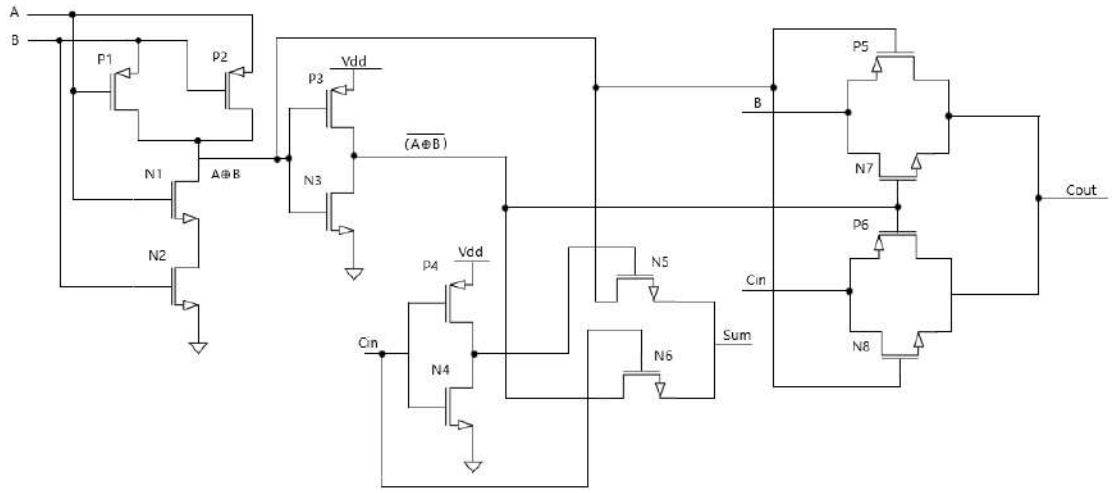
Fig. 8: Akshay Bhaskar Full Adder.

3 PROPOSED DESIGN

The proposed design has three modules. Module I is in charge of producing XOR and XNOR outputs, for sum and carry modules II and III are used respectively. The block diagram for the suggested design is depicted in fig. 9(a).



(a)



(b)

Fig 9. (a) Proposed design's block diagram. (b) Schematic for proposed design.

Since each module has a unique benefit, they are cascaded so that when combined they perform like a conventional adder [4] [8]-[9]. Every module is built in such a way so that it optimizes the adder circuit's overall performance, including lowering the latency, area, power usage, and PDP [10].

3.1 XOR/XNOR Signal Generation – Module-I

With the help of 6 MOSFETS, (P1, P2, P3 and N1, N2, N3) Module-I generates XOR and XNOR signal, which is shown in fig. 9(a). The XOR output is produced using 4 MOSFETS (P1, P2, N1 and N2), and this XOR Signal is passed through a CMOS Inverter (P3 and N3) to generate XNOR Signal [11].

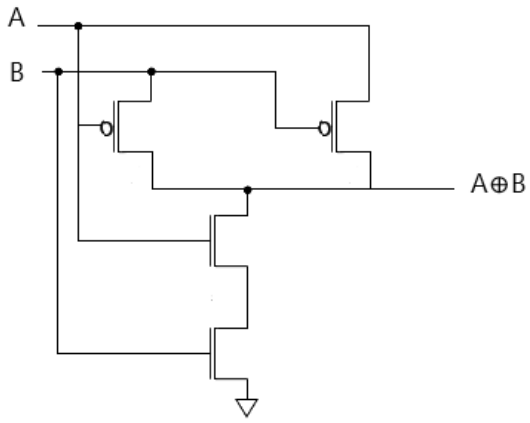


Fig. 10: XOR XNOR Circuit.

3.2 2:1 Multiplexer Logic using Pass Transistor Logic with nMOSFET for Sum Signal Generation – Module-II

The sum module is generated in Module-II of fig. 9(a), using four MOSFETs, (P4, and N4, N5, N6). The resultant Boolean expression for the sum is shown in equation (2).

$$S\ (Sum) = (C_{in} \cdot (A \oplus B)' + C_{in}' \cdot (A \oplus B)) \qquad (2)$$

The CMOS inverter is used initially to have complement of Cin (P4 and N4). N5 and N6's nMOSFETS gates are connected to XNOS and XOR signals produced by Module-I, respectively. When the Cin is high (or logic "1") the output is linked to XOR signal and to XNOR when Cin signal is logic "0".

The MOFETS in Pass Transistor Logic are used as a switch rather than amplifier, which makes static power dissipation very low and hence lead to lower power consumption by it over digital circuits [12]. Pass Transistor logic is good for making small circuits as it needs fewer gates as compared to other types of logic. However, it possesses some drawbacks

too. The Pass Transistor Logic with nMOSFET suffer from threshold voltage drop when passing a logic "1". This drop can lead issues with signal swings or level restoration at the gate output [13].

3.3 Carry-out Signal Generation Circuit using Transmission Gate Logic – Module-III

In order to generate carry signal (Cout), the third module contains two transmission gates (one with P5 and N7 and the other with P6 and N8) [14]. The Boolean expression of Cout Signal is shown in equation (3):

$$C\ (Cout) = C_{in}' \cdot (A \oplus B) + B \cdot (A \oplus B)') \qquad (3)$$

4 PERFORMANCE ANALYSIS AND RESULTS

The existing designs and the presented design are built using Cadence Virtuoso at 90nm technology. We have considered the same environment for all the circuits. A buffer is employed at each input and output terminal which is made by using two inverters in series. The supply voltage (Vdd) is set to 0.9V for analysis of circuits. At terminals A, B, and C, we provided square wave pulses of 100MHz, 50MHz, and 25MHz frequencies, respectively. Power consumption, delay, and PDP are the parameters used for performance analysis and the presented circuit is compared to all the previous circuits. Three major components of total power are dynamic power ($P_{dynamic)}$ (also known as switching power),), short-circuit power (P_{sc}), and static power (P_{static}) (or leakage power) [17]. The expression for power consumption is shown in equation (4).

$$P_{total} = P_{static} + P_{dynamic} + P_{sc} \qquad (4)$$

When the device is inactive, the leakage current flows through the transistors causing the static power. Node capacitance switching causes dynamic power or switching power loss. When the short-circuit current flows from the supply voltage(Vdd) to the ground, it causes the short-circuit power loss. Fig. 11 displays the output waveform of the presented circuit, which Table 1 verifies. We calculated the propagation delay, which occurs when the input reaches half of Vdd and the output crosses a defined threshold for each transition from "0" to "1" and from "1" to "0". Table 2 depicts the delay in propagation for all the input signals (A, B, and C) with respect to the SUM signal. Table 2 clearly demonstrates that for most circuit designs, signal A has the maximum propagation delay, while signal C has the minimum propagation delay. For signals A and B, the proposed circuit has the lowest delay with respect to sum, making it an efficient design for high-speed computing applications, while the C signal shows the lowest delay for Rafiee [15]. Table 3 shows the propagation delay of input signals with respect to the carry signal. The trend is very similar to Table 2, where for most of the designs, signal A shows the maximum delay and signal C shows the minimum delay. Table 3 clearly demonstrates that the proposed design outperforms existing designs in terms of delay. The comparison displays that the proposed design exhibits a lower delay compared to most other designs across all inputs A, B, and C. Following Narendra [17], the proposed circuit provides the minimum delay for signal A compared to other designs. Similarly signal B exhibits a lower delay compared to other designs. However, the Hasan's [16] delay for input C is better than the proposed design. However, when compared to signals A and B, the Hasan design [16] may be effective for specific tasks involving input C, but it may not be suitable for other inputs. Table 4 compares the different full adders depending on transistor count, power consumption, delay, and PDP. Includes, design ranges in transistor count from 10 to 23, with proposed design using 14 transistors. According to table 4, the power consumption of designs varies from 4.984 µW (Shamini [6]) to 15.98 µW (Hasan [16]), with proposed design requiring 7.87 µW, indicating it is relatively power efficient. For final delay, the highest delay for both sum and carrying signals with respect to inputs A, B, and C is considered and have taken this maximum delay for the calculation. When considering delay, the proposed design demonstrate the lowest delay of 205.17 ps, while the largest delay is 371.5 ps (Rafiee [15]) and hence making it suitable for high-speed applications. This low delay can be beneficial for high-speed applications. The efficiency of a design in terms of energy can be determined with the help of PDP, also highlighted in table 4, calculated by multiplying total power and maximum delay after considering all paths. It helps us understanding the compromise between power and latency. The PDP value as shown in the table 4, ranges from 1614.687 aJ (Proposed) to 4829.156 aJ (Hasan), with proposed design having lowest PDP, showcasing an optimal balance between power consumption and operational speed. Fig. 12 (a), (b), and (c) shows the comparison of the power, latency, and PDP (from table 4), in a graphical way, of the suggested design with the existing designs, respectively. The effeciency in both speed and energy consumption makes the proposed design ideal for incorporation into high-peerformance, energy-sensitive applications, such as portable devices, battery powered systems, and advanced computing architecturs that require both rapid data processing and power effeciency.

At various voltages, spanning from 0.6V to 1.8V, the power of the proposed circuit is calculated (Table 5) and plotted (fig. 13). Table 5 displays the power consumption value of the presented full adder at various voltages, ranging from 0.6V to 1.8V. The plot of power consumption versus supply voltage is shown in fig. 13. The curve fitting tool (on MATLAB) is

used to obtain the equation of the fifth-degree polynomial (eq. 5), which depcits the mathematical relationship between power consumption and supply voltages in the suggested design.

$$P(x) = a*x^5 + b*x^4 + c*x^3 + d*x^2 + e*x^1 + f \qquad (5)$$

In this equation (5), P(x) denotes the power consumption at voltage V, with constant coeffecient values a = -16.0547 e-6, b = 190.4309 e-6 , c = -343.5239 e-6, d = 301.6786 e-6, e = -138.1071 e-6, and f = 25.6975 e-6. Using this equation (5), we can calculate the power consumption values at any voltage between 0.6V and 1.8V for our proposed design. The power consumption shows a clear trend, as the working voltage increases from 0.6V to 1.8V, power usage increases exponentially (eq. 5) from 0.653µW to 446.8µW. At lower voltages (0.6V to 1.0V), the design consums very little ower, make it ideal for energy saving applications including battery-powered devices and portable devices. However, as voltage exceeds 1.0V, power consumption increases drastically, demonstarting that while the design may accommodate higher performance requirements, it does so at a significant power cost. This makes the suggested architecture adaptable, allowing it to be addapted to specific applications, such as maximizing energy effeciency for extended life or achieving high performance for intensecomputing activities. Thus, the design's capacity to operate effeciently at both low and high voltages demonstartes its adaptbility and potential for widespread application in a variety of technological disciplines.

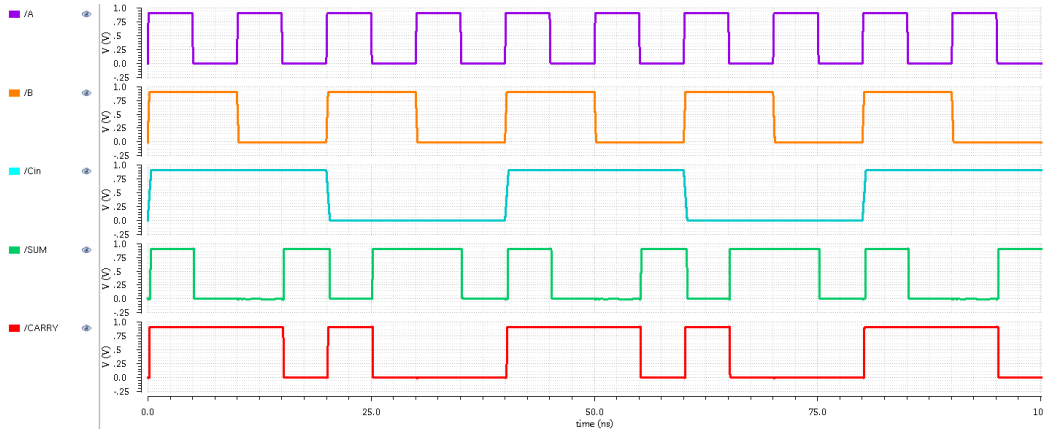


Fig. 11: Output Waveform of presented 14T adder.

Table 2: Sum Delay for input A, B, and C(in ps).

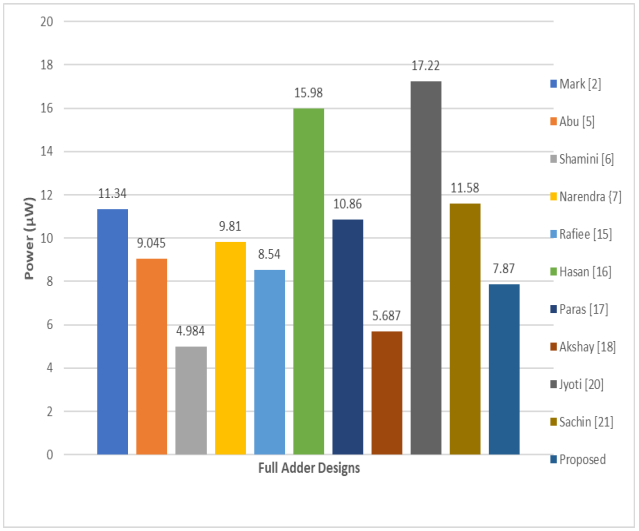
Design	A	B	C	Ref.
Rafiee	273.33	223.3	123.35	[15]
Hasan	302.2	252.2	152.2	[16]
Jyoti	207.535	213.55	113.45	[20]
Sachin	250.4	200.4	100.4	[21]
Mark	293.52	293.85	143.50	[4]
Abu	274.45	254.422	124.425	[5]
Shamini	278.355	228.357	128.35	[6]
Narendra	231.8	226.25	126.45	[7]
Paras	315.5	249.6	221.1	[17]
Akshay	271.95	226.355	126.335	[18]
Proposed	196.805	205.17	123.5	

Table 3: Carry Delay for input A, B, and C(in ps).

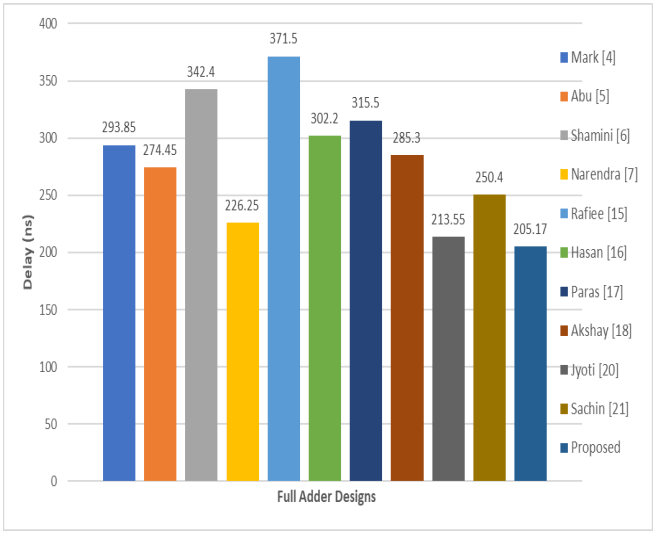
Design	A	B	C	Ref.
Rafiee	308.3	371.5	271.5	[15]
Hasan	150.995	100.04	11.15	[16]
Jyoti	179.6	137.8	37.8	[20]
Sachin	142.5	55.1	55	[21]
Mark	162.505	65.81	41.47	[4]
Abu	153.77	43.1	56.9	[5]
Shamini	268.01	342.4	242.4	[6]
Narendra	117.6	112.9	12.9	[7]
Paras	167.85	66.9	33.1	[17]
Akshay	285.295	235.295	135.295	[18]
Proposed	151	70.47	34.81	

Table 4: Full adder simulation results at supply voltage of 0.9V.

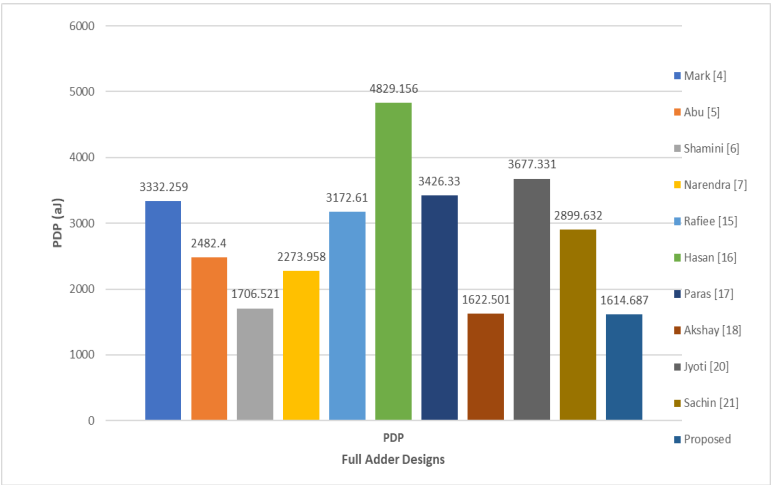
Design	Transistor Count	Power (µW)	Delay (ps)	PDP (aJ)	Ref.
Rafiee	23	8.54	371.5	3172.61	[15]
Hasan	22	15.98	302.2	4829.156	[16]
Jyoti	20	17.22	213.55	3677.331	[20]
Sachin	18	11.58	250.60	2899.632	[21]
Mark	14	11.34	293.85	3332.259	[4]
Abu	14	9.045	274.45	2482.400	[5]
Shamini	14	4.984	342.4	1706.521	[6]
Narendra	14	9.81	231.8	2273.958	[7]
Paras	12	10.86	315.5	3426.33	[17]
Akshay	10	5.687	285.3	1622.501	[18]
Proposed	14	7.87	205.17	1614.687	



(a)



(b)



(c)

Fig. 12: Comparison of different 14T adder cells (a) Power Consumption, (b) Delay, (c) PDP

Table 5 : Simulation values of power consumption for the proposed circuit at different supply voltages.

Voltage(V)	0.6	0.8	1.0	1.2	1.4	1.6	1.8
Power (µW)	0.653	5.23	19.9	56	126	249.7	446.8

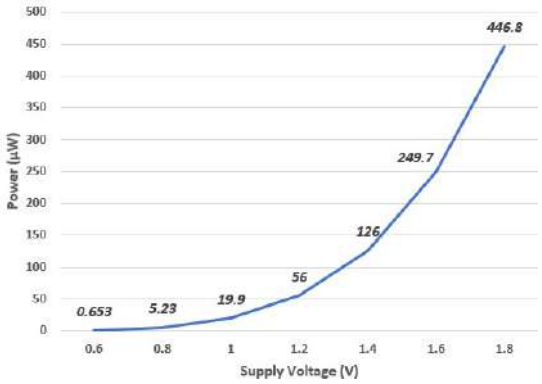


Fig. 13: Plot of Power Consumption versus various voltages for proposed circuit.

5 CONCLUSION AND FUTURE SCOPE

This research introduced a 14T 1-bit hybrid full adder circuit with better results. Using Cadence Virtuoso, the performance of our design is compared with that of existing circuits. As per the results, the presented design exhibits improved performance regarding power, delay, and PDP when operated in a single cell. The introduced circuit improves the latency and PDP by 11.49% to 44.77 % and 0.48% to 66.56%, respectively above prior circuits. The suggested 14T full adder is ideal for applications that require efficiency and speed. The proposed design can enhance performance and energy efficiency in ALUs, due to its low power consumption and quick operation. This adder can be useful in DSP applications as it meets the demand for fast and efficient arithmetic operations.

Future work could involve designing whole adder circuits with varied widths and technologies. Additional studies could focus on extending the suggested design larger bit-width adder, such as 8-bit or 16-bit version, solving issues like increased connection complexities while retaining performance metrics. Integrating the suggested full adder with other arithmetic unit such as multipliers and dividers may result in creation of a comprehensive low-power, high-speed ALUs. Additionally, suggested full adder design can be used in a variety of other low-power applications.

REFERENECES

[1] B. Basheer and R. Merin varkey, "Review on Various Full Adder Circuits," *2019 3rd International Conference on Computing Methodologies and Communication (ICCMC)*, Erode, India, 2019, pp. 877-880.

[2] A. K. Yadav, B. P. Shrivatava and A. K. Dadoriya, "Low power high speed 1-bit full adder circuit design at 45nm CMOS technology," *2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE)*, Bhopal, India, 2017, pp. 427-432.

[3] R. Charan *et al*., "Review of Performance Analysis of Some Basic Full Adder Circuits," *2023 International Conference on Advanced & Global Engineering Challenges (AGEC)*, Surampalem, Kakinada, India, 2023, pp. 102-106.

[4] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage-swing nodes," *1999 IEEE Workshop on Signal Processing Systems. SiPS 99. Design and Implementation (Cat. No.99TH8461)*, Taipei, Taiwan, 1999.

[5] E. Abu-Shama and M. Bayoumi, "A new cell for low power adders," *1996 IEEE International Symposium on Circuits and Systems. Circuits and Systems Connecting the World. ISCAS 96*, Atlanta, GA, USA, 1996.

[6] S. Subramaniam, T. W. X. Wilson, A. K. Singh and G. R. Murthy, "A proposed reliable and power efficient 14T full adder circuit design," *TENCON 2017 - 2017 IEEE Region 10 Conference*, Penang, Malaysia, 2017.

[7] S.Narendra, A.Maheswara Reddy, S.Saleem and K.M.Haneef. "14 Transistor Full Adder Circuit using 4 Transistor Xor Gate and Transmission Gate." (2018).

[8] Kanojia, Ayush & Agrawal, Sachin & Lorenzo, Rohit. (2023). Comprehensive Analysis of a Power-Efficient 1-Bit Hybrid Full Adder Cell. Wireless Personal Communications.

[9] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar and A. Dandapat, "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit," in IEEE Transactions on Very Large-Scale Integration (VLSI) *Systems*, vol. 23, no. 10, pp. 2001-2008, Oct. 2015.

[10] Manjunath K M, Abdul Lateef Haroon P S, A. Pagi and Ulaganathan J, "Analysis of various full-adder circuits in cadence," *2015 International Conference on Emerging Research in Electronics, Computer Science and Technology (ICERECT)*, Mandya, India, 2015, pp. 90-97.

[11] Jyh-Ming Wang, Sung-Chuan Fang and Wu-Shiung Feng, "New efficient designs for XOR and XNOR functions on the transistor level," in *IEEE Journal of Solid-State Circuits*, vol. 29, no. 7, pp. 780-786, July 1994,

[12] D. RadhaKrishnan “Low-voltage low-power CMOS full adder,” IEEE Proc.-Circuits Devices Syst., vol. 148, no. 1, pp. 19-24, Feb. 2001.

[13] Mingyan Zhang, Jiangmin Gu and Chip-Hong Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," *2003 IEEE International Symposium on Circuits and Systems (ISCAS)*, Bangkok, Thailand, 2003, pp. V-V.

[14] C. -K. Tung, Y. -C. Hung, S. -H. Shieh and G. -S. Huang, "A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded System," *2007 IEEE Design and Diagnostics of Electronic Circuits and Systems*, Krakow, Poland, 2007, pp. 1-4.

[15] M. Rafiee, N. Shiri and A. Sadeghi, "High-Performance 1-Bit Full Adder With Excellent Driving Capability for Multistage Structures," in *IEEE Embedded Systems Letters*, vol. 14, no. 1, pp. 47-50, March 2022.

[16] M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman and S. Islam, "Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 8, pp. 1464-1468, Aug. 2020.

[17] Paras, R. Lorenzo, A. Singh and A. Kaur, "Optimizing the 12T Hybrid 1-Bit Full Adder Circuit for Low Energy Applications," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp. 1-5.

[18] A. Bhaskar, R. Dheeraj, S. Saravanan and K. J. Naidu, "A low power and high speed 10 transistor full adder using multi threshold technique," *2016 11th International Conference on Industrial and Information Systems (ICIIS)*, Roorkee, 2016, pp. 371-374.

[19] Hasan, M., Siddique, A.H., Mondol, A.H. et al. Comprehensive study of 1-Bit full adder cells: review, performance comparison and scalability analysis. SN Appl. Sci. 3, 644 (2021).

[20]. Kandpal, J., Tomar, A. Design and implementation of high-performance 20-T hybrid full adder circuit. Analog IntegrCirc Sig Process 119, 97–110 (2024).

[21]. Kanojia, A., Agrawal, S. & Lorenzo, R. Comprehensive Analysis of a Power-Efficient 1-Bit Hybrid Full Adder Cell. Wireless Pers Commun 129, 1097–1111 (2023).