Design of 8T DTMOS Schmitt Trigger SRAM Cell For Various Low Energy Applications

Neeta Pandey[1*], Aditya Singh Mann[2] and Abhay Setia[2]

[1] Department of Electronics and Communication Engineering, Delhi Technological University, New Delhi, India
[2] Department of Electronics and Communication Engineering, Delhi Technological University, New Delhi, India

[*]E-mail: neetapandey@dce.ac.in

Abstract. Internet of things (IoT) based systems require power-efficient circuits to raise the battery lifeline. This study presents a single-ended 8T SRAM cell. The core of the proposed 8T SRAM cell is composed of a Schmitt-Trigger circuit which a dynamic body bias technique is applied to a standard CMOS inverter through a feedback mechanism, whereby the threshold voltages of two MOSFETs can be changed, thus changing the switching voltage. Read operation of the proposed cell is conducted using the shared footer per word transistor. The write path is cut-off during the read operation, improving RSNM. A transmission gate placed in the cell core is used to cut the feedback path during write operation. To prove superiority of the proposed cell it is compared with four state-of-the-art SRAM cells under identical conditions on Cadence Virtuoso using 45nm technology at VDD=0.8 V. The proposed circuit shows a 135.74 % improvement in terms of RSNM and a 44.04 % improvement in terms of peak-to-peak power compared to the 6T DTMOS Cell.

1. Introduction

In the realm of modern integrated circuits, Static Random Access Memory (SRAM) stands as a cornerstone, crucial for various computing systems and applications. Its significance is particularly pronounced in the Internet of Things (IoT) landscape, where power efficiency is paramount. As IoT devices proliferate, spanning sensors, actuators, and wearables, the demand for power-efficient memory solutions grows.

SRAM finds diverse applications in IoT, including data caching, buffering, and temporary storage of sensor readings. Designing SRAM cells tailored for IoT is crucial, considering factors like read stability. This paper presents a novel 8T SRAM cell design integrating a Schmitt-Trigger circuit with dynamic body biasing, aimed at reducing power consumption while ensuring reliable data storage and retrieval. Through comparative analysis, the proposed design demonstrates superior performance metrics compared to existing solutions, highlighting its potential to enhance energy efficiency and prolong battery life in IoT devices. Innovative memory design methodologies like this are instrumental in meeting the evolving demands of IoT systems, fostering seamless integration into the expanding IoT landscape.

Further, Dynamic Threshold Metal-Oxide-Semiconductor (DTMOS) is used in different applications including SRAM, to enhance performance and mitigate power consumption challenges. Its implementation in SRAM design offers several advantages that contribute to better efficiency and reliability. DTMOS technology presents a promising avenue for SRAM design, offering dynamic threshold voltage control that can minimize leakage currents during standby modes, performance, and robustness against variations. Its implementation in SRAM architecture aligns with the growing demand for energy-efficient and adaptable memory solutions across various computing and electronic applications.

In this paper, an 8T SRAM cell is put forward that uses a Schmitt-Trigger circuit wherein dynamic body bias technique is applied. The read operation of the proposed cell employs a shared footer per word transistor. A transmission gate placed in the cell core is used to cut the feedback path during write operation. The paper is arranged in six sections. Literature review is presented in Section II followed by description of performance parameters in Section III. The proposed cell is described in Section IV. The simulation results are presented in Section V and the paper concludes in Section VI.

2. Literature Review

In order to make innovative interventions more effective, we need to improve memory systems. To do this, different designs have been suggested, ranging from 6T to 18T SRAM cells. These designs include various ways of reading and writing data, like single-end or differential methods. Researchers have also looked into ways to use less power and make access faster, without sacrificing other important aspects of performance. The following section aims to summarize and analyze the research done in this area, to see what methods work best for improving memory systems.

Erfan Abbasian et al.[1] proposed a novel 7T Single Ended Schmitt Trigger based SRAM that uses DTMOS. In this cell the read decoupling technique is used to improve RSNM and to enhance WSNM, there is a feedback-cutting mechanism. It demonstrates extremely low T_{RA}. Raghav Shekhar et al.[4] proposed a 10T differential SRAM cell that uses 6T SRAM cell along with additional four transistors in the form of a vertically oriented inverter whose output is attached to the source of the NMOS of another inverter. This configuration prevents any inversion taking place during the read process by restoring the value. This cell provides large hold and read noise margins. Ravi Teja Yekula et al.[7] proposes a 13T SRAM [add technique] cell that has a shorter read access time than existing circuits and has applications for deep-space. It consists of a stacked NMOS structure consisting of three transistors which can perform a differential read operation without affecting the nodes of the SRAM cell. S. Cai et al.[8], the author's have proposed an 18T SRAM cell which is based on Muller C elements. The circuit has 4 storage nodes, namely, Q, QB, A and B. It is immune to Single Event Upset (SEU) and demonstrates high-reliability but a certain area overhead. Yinghuan Lv et al.[9] proposed a radiation hardened 8T structure, which utilizes the concept of cutting the inverter feedback, with the help of NMOS transistors attached to the path between the drain of the PMOS and the drain of the NMOS.It has large read current, low leakage current, and a large RSNM with some area sacrifice.

3. SRAM Cell Performance

One of the fundamental building blocks of memory architectures is the 6T SRAM cell, that provides high-speed and reliable data storage in electronic systems. Comprising six transistors arranged in a specific configuration, the 6T SRAM cell operates based on bistability principles, allowing it to retain data until power is provided to the system. A six-transistor (6T) SRAM bitcell serves fundamentally as a unit within the SRAM array as depicted in Fig 1 (a). The 6T SRAM bitcell comprises two access transistors (M1 and M2) and two back to back connected inverters (M3-M4, M5-M6) linked to each data storage node. The paired inverters create a latch that has binary information, storing the data's true and complementary versions. Figure 1(b) shows the DTMOS based counterpart of 6T SRAM bit cell.

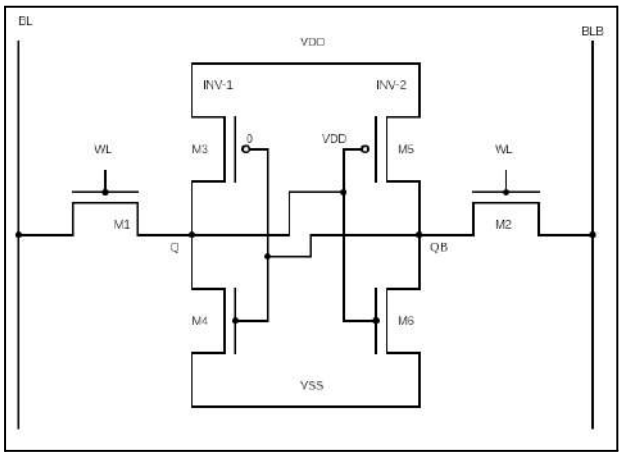

Figure 1(a). 6T SRAM Bitcell

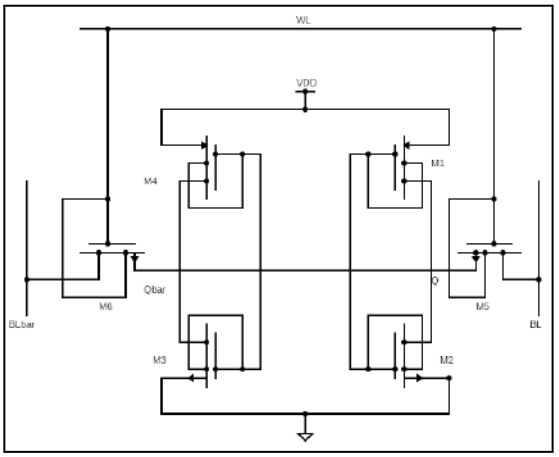

Figure 1(b). 6T SRAM Bitcell based on DTMOS

Noise margin, Read and Write access time; and Power are some of the important parameters to study the performance of an SRAM. These parameters are described in the following text:

Noise Margin:

The prime indicator in an SRAM bitcell used to gauge its stability during read cycles and in a hold state is the Static Noise Margin (SNM). It represents the maximum level of DC noise (VN) that the cross-coupled inverter pair can withstand while retaining the bitcell's data. Extracting the read SNM involves observing the read voltage transfer characteristics (VTC). From Fig 1(a), this measurement entails checking the voltage across the data storage node Q (or QB) while maintaining bias at VDD for both bitlines (BL, BLB) and the wordline (WL), while the node voltage at QB (or Q) is concurrently monitored. Read and write access times are crucial parameters in the operation of 6T SRAM, determining how quickly data can be retrieved from or written into the memory cell.

Read and Write Access Time:

The read access time(TRA) in a 6T SRAM cell refers to the duration required to access stored information from the memory cell. The read access time is affected by various factors such as Cell Size, Sense Amplifier Speed and Bitline Capacitance. During a read operation, the stored data is accessed by sensing the voltage difference between the bitlines. The write access time(TWA) refers to the duration necessary to write new data into the SRAM cell. Factors influencing write access time include Write Driver Speed, Precharge Time and Cell Size This process involves modifying the cell's state to store new information.

Power:

Power is measured while performing the DC operating point analysis, that is, it is measured when we are sweeping the node QB and the bitlines and the worldline are set to VDD. The power is obtained using the inbuilt analysis feature of Virtuoso. Several parameters, including power dissipation, are optimized to achieve better efficiency in SRAM designs.

4. Proposed 8T DTMOS Cell

The proposed cell employs the cascaded inverter based DTMOS Schmitt Trigger [10].The schematic of the proposed circuit is given in Fig. 2. In the circuit NM1-PM0 and PM1-NM0 form two inverters, such that the transistors' body of one is connected to the output of the other. An inbuilt body bias is provided through the dynamic threshold configuration which forms the basis of our feedback mechanism. The proposed bitcell uses a single bitline(BL) to form read and write operations. A feedback cutting transmission gate has been placed inside the cell core which is controlled by the WWL and WWLB signals. The following subsection explains the working of the proposed cell.

Read Operation:

The read operation is helped by the read assist transistors and provides a discharging path by utilising the opposite nature of the WWLB signal. The write path is cutoff by pulling down the WWL signal. The read assist transistors NM4 and NM5, gated by the node QB and WWLB signal respectively and help in the discharging process. The NM5 read assist transistor is shared per word.

Write Operation:

The write operation is initiated by the pulling up the WWL signal, which cuts the feedback mechanism and establishes the write path; now the circuit behaves as two cascaded inverters. In order to write '1' at storage node 'Q', the BL is set to VDD which drives the circuit to its complement value.

Hold Operation:

During the hold operation the WWL is pulled down in order to establish the feedback path and the bitline is pre-charged to VDD and the inverters form a cross-coupled pair.

5. Simulation

The simulation has been carried out using the Cadence Analog Design environment, in order to verify the read, write and hold operations with a supply voltage of 0.8 V. The circuit has been tested for a timespan of 45 ns in which from 0 to 15 ns, a value is written into the node 'Q' to initiate charge reversal. From 15 to 30 ns, we are holding the value, and from 30 to 45 ns we are reading the storage node. The key timing signals here are WWL and WWLB which initiate the operations by cutting and establishing the feedback path during various stages.

The noise margin has been obtained by keeping in mind the complementary nature of various signals, as during the read operation we do not want to activate the write path, in Fig. 4, we have provided the butterfly curve obtained for SNM. The Write SNM is calculated by obtaining the Write and Read VTCs and plotting the smallest square possible between the two curves. The power has been obtained using the inbuilt peak-to-peak power feature of Virtuoso using the calculator.

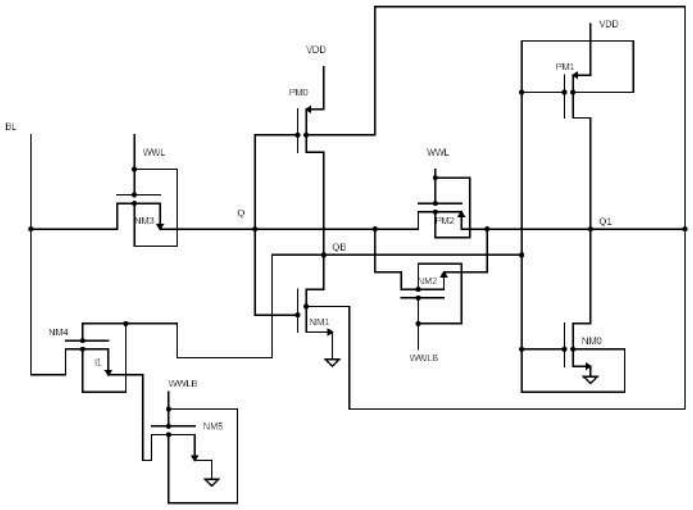

Figure 2. 8T DTMOS (Proposed)

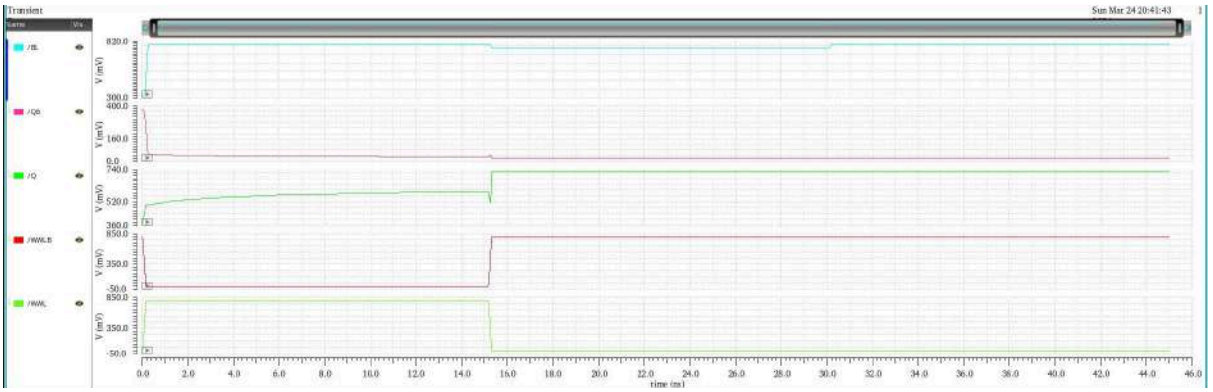

Figure 3. Read and Write Timing Diagram of Proposed 8T DTMOS SRAM Bitcell

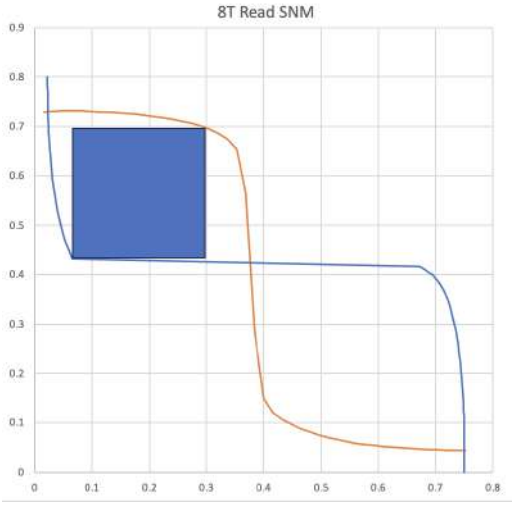

Figure 4. Read SNM of Proposed 8T DTMOS SRAM Bitcell

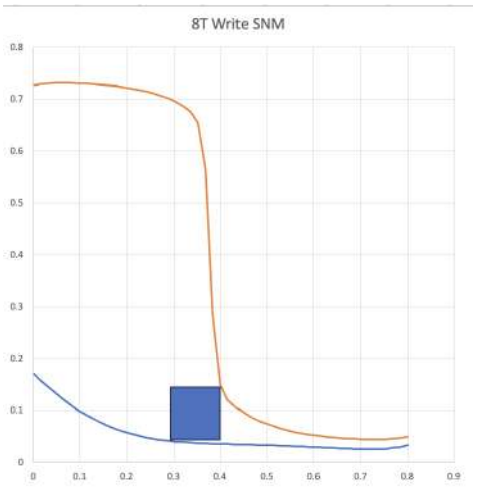

Figure 5. Write SNM of Proposed 8T DTMOS SRAM Bitcell

Table 1. Parameter Comparison for Various Designs

Parameters	DTMOS 6T	Schmitt Trigger 7T	RHD 8T	RHD 10T	8T DTMOS (Proposed)
Read SNM (V)	0.09771	0.210504	0.09951	0.13544	0.23035
Write SNM (V)	0.09961	-	0.16035	0.05327	0.09570
T_{RA} (ps)	50	60.678	71.7	85	76.1
T_{WA} (ps)	327.68	207.1831	144.19	192.22	84
Power(peak-to-peak) (μW)	72.2	129	90.4	61.6	40.4

6. Conclusion

In this study, we proposed a novel 8T DTMOS SRAM Cell, which employs the Schmitt Trigger topology. The proposed shows the best RSNM among all the bitcells studied and also demonstrates a good TRA and TWA. It improves upon the existing topologies by employing the transmission gate technique and does away with the read decoupling technique. The key variable that we wanted to optimize was power and a major reduction has been observed after performing peak-to-peak power analysis. The power has reduced from 72.2 uW in the 6T DTMOS SRAM Cell to 40.4 uW in the proposed SRAM cell, marking a 44.04 % reduction. Thus, in comparison to the circuits study the proposed circuits stands out with regard to Power and Read SNM in the context of 45nm technology.The proposed circuit is first in terms of RSNM, TWA and peak-to-peak power and third in terms of TRA. Since we have successfully managed to reduce the power consumption of SRAM bitcell which makes it suitable for IoT applications in which energy efficient bitcells are necessary to raise the battery lifetime.

References

[1] Abbasian, E., & Gholipour, M. (2021b). Design of a Schmitt-Trigger-Based 7T SRAM cell for variation resilient Low-Energy consumption and reliable internet of things applications. AEU - International Journal of Electronics and Communications, 138, 153899. https://doi.org/10.1016/j.aeue.2021.153899

[2] Panchal, A., Sharma, P., Gupta, A., Neema, V., Tiwari, N., & Sindal, R. (2023). Improved reliability single loop single feed 7T SRAM cell for biomedical applications. Memories - Materials Devices Circuits and Systems, 4, 100057. https://doi.org/10.1016/j.memori.2023.100057

[3] Roy, C., & Islam, A. (2021). Design of low power, variation tolerant single bitline 9T SRAM cell in 16-nm technology in subthreshold region. Microelectronics Reliability, 120, 114126. https://doi.org/10.1016/j.microrel.2021.114126

[4] Shekhar, R., & Kumar, C. I. (2022). Design of highly reliable radiation hardened 10T SRAM cell for low voltage applications. Integration, 87, 176–181. https://doi.org/10.1016/j.vlsi.2022.07.004

[5] Mittal, Sparsh & Verma, Gaurav & Kaushik, Brajesh Kumar & Khanday, Farooq. (2021). A Survey of SRAM-based In-Memory Computing Techniques and Applications. Journal of Systems Architecture. 119. 10.1016/j.sysarc.2021.102276.

[6] Sugii, N. (2015). Low-power-consumption fully depleted silicon-on-insulator technology. Microelectronic Engineering, 132, 226–235. https://doi.org/10.1016/j.mee.2014.08.004

[7] Teja Yekula R., Pandey M. & Islam A., "A Highly Reliable Radiation Tolerant 13T SRAM Cell for Deep Space Applications," in Microelectronics reliability, vol. 1330, pp. 1–14, Jun. 2022. Publisher: Elsevier, DOI: https://doi.org/10.1016/j.microrel.2022.114527

[8] Cai, S., Wen, Y., Ouyang, J., Wang, W., Yu, F., & Li, B. (2023). A highly reliable and low-power cross-coupled 18T SRAM cell. Microelectronics Journal, 134, 105729. https://doi.org/10.1016/j.mejo.2023.105729

[9] Lv, Y., Wang, Q., Ge, H., Xie, T., & Chen, J. (2021). A highly reliable radiation hardened 8T SRAM cell design. Microelectronics Reliability, 125, 114376. https://doi.org/10.1016/j.microrel.2021.114376

[10] Zhang C, Srivastava A, Ajmera P. Low voltage CMOS Schmitt trigger circuits. Electron Lett 2003;39:1696–8.