

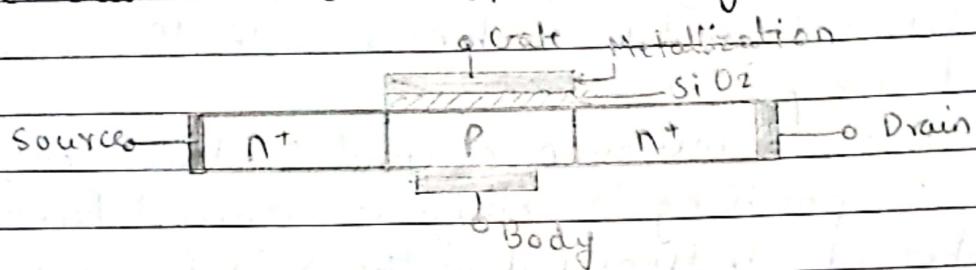
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Assignment No 1

Q.1 Explain with neat diagram the working of power MOSFET and IGBT. Draw steady state characteristics of it and explain same.

→ Power MOSFET :-

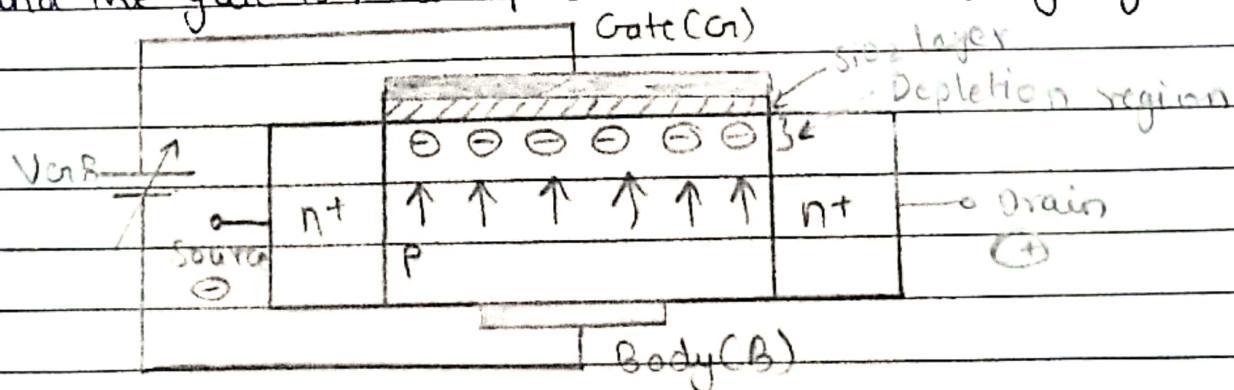
- The basic structure of the n-type is as shown below :



- Power MOSFET is a minority carrier device. The conduction takes place only due to electrons. Hence it is felt that the conduction cannot take place through a MOSFET from drain (n⁺) to source (n⁺) due to presence of p-layer (base layer) between them.
- But practically it is possible due to phenomenon called 'Inversion layer creation'.
- (C) - The operation of power MOSFETs can be divided into two steps :

① Formation of depletion region :

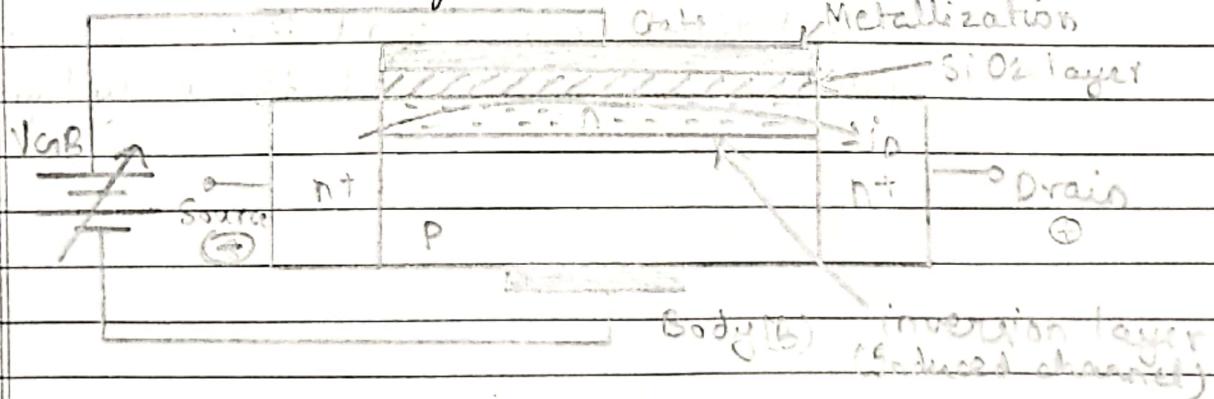
- The MOSFET is forward biased by connecting a positive voltage to its drain terminal w.r.t. its source terminal and the gate is made positive w.r.t. the body layer



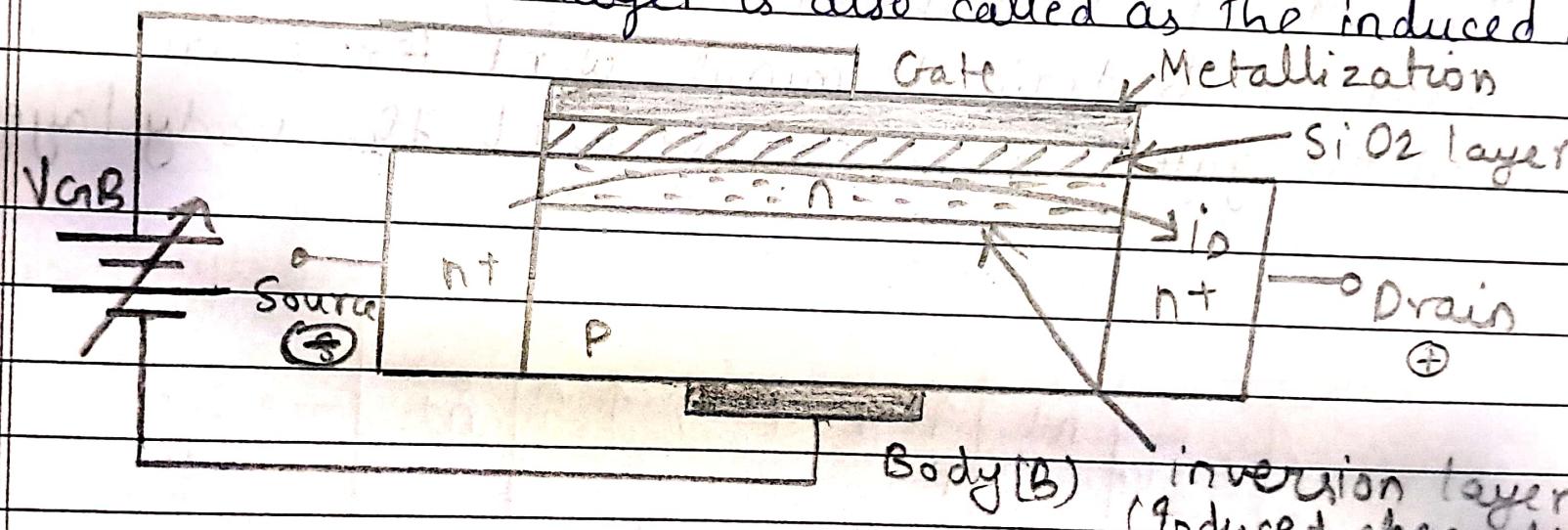
- The 'P' layer of fig consists of a large number of holes and few electrons. The holes are majority carriers.
- Hence they outnumber the electrons which are minority carriers, still the number of electrons present in the 'P' layer is sufficiently large.
- Due to positive voltage applied between gate and body as shown in fig, these electrons are attracted towards the gate and gather below the SiO_2 layer and produce depletion layer by combining with the holes that are present there.

(2) Creation of inversion channel (induced channel):-

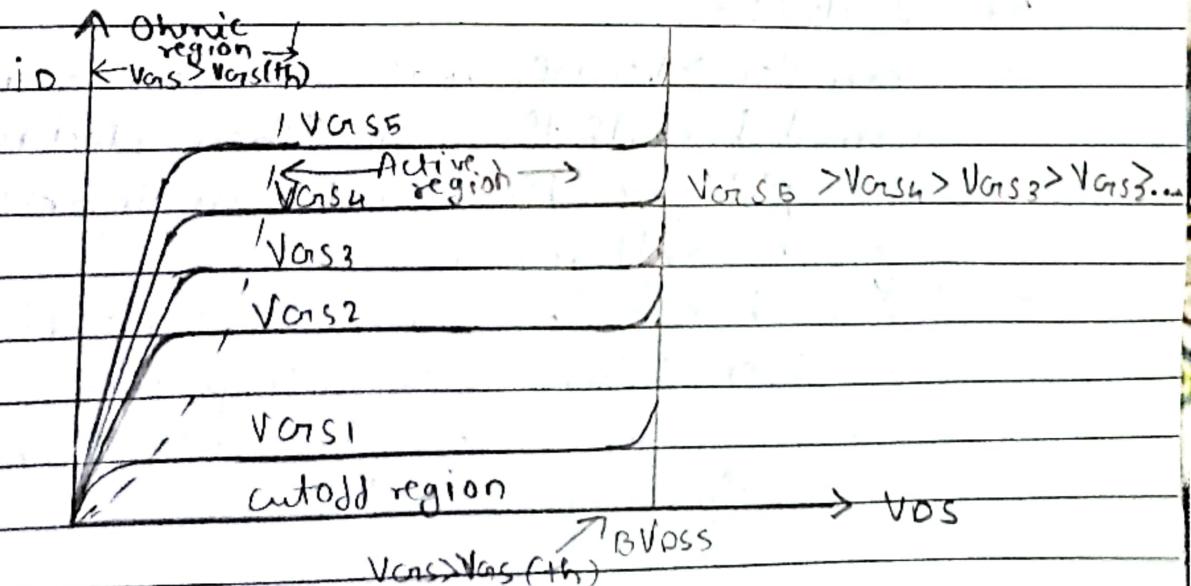
- If the positive gate voltage is increased further, the number of electrons below the SiO_2 layer will be greater than the number of holes.
- Thus the conductivity of the part of P-layer close to SiO_2 layer will change from +ve to -ve.
- That means an n-type of sub layer is formed between SiO_2 layer.
- This process is known as creation of the inversion layer, and the process of generation of an inversion layer due to the externally applied gate voltage is known as the "Field effect".
- The inversion layer is also called as the induced channel.



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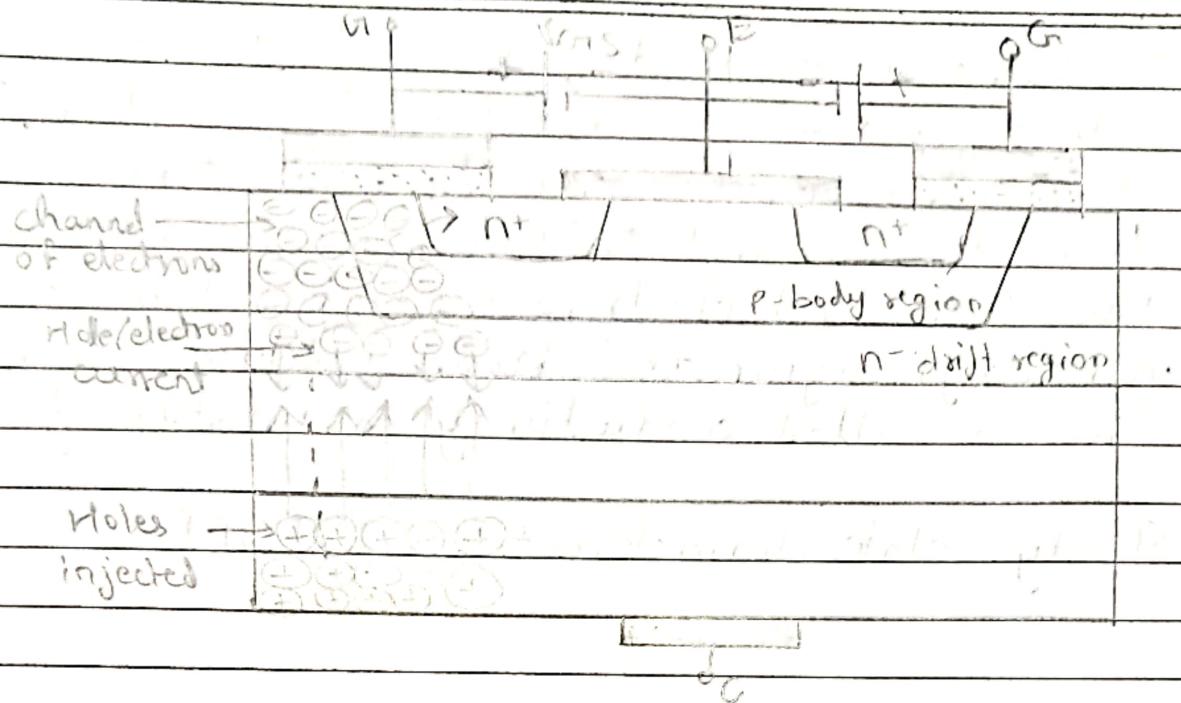
- This induced channel will connect the two n^+ layers on either sides of p-region
- In this way now the n-type channel gets created in the p-type body layer and conduction can take place through this layer
- The resistance of the induced channel is dependent on the magnitude of gate to base (body) voltage. Higher the gate voltage less is the resistance. The MOSFET acts as a variable resistor
- With increase in the gate to body voltage, the resistance will decrease, however it cannot decrease below a certain min value. If the max specified value of gate to voltage is exceeded then SiO_2 layer will break down
- Steady State characteristics of MOSFETs
- The drain current i_D is plotted w.r.t drain to source voltage V_{DS} .
- These characteristics are plotted for various values of gate source voltages (V_{GS})
- There are three regions in the characteristics: Ohmic, active and cutoff region.



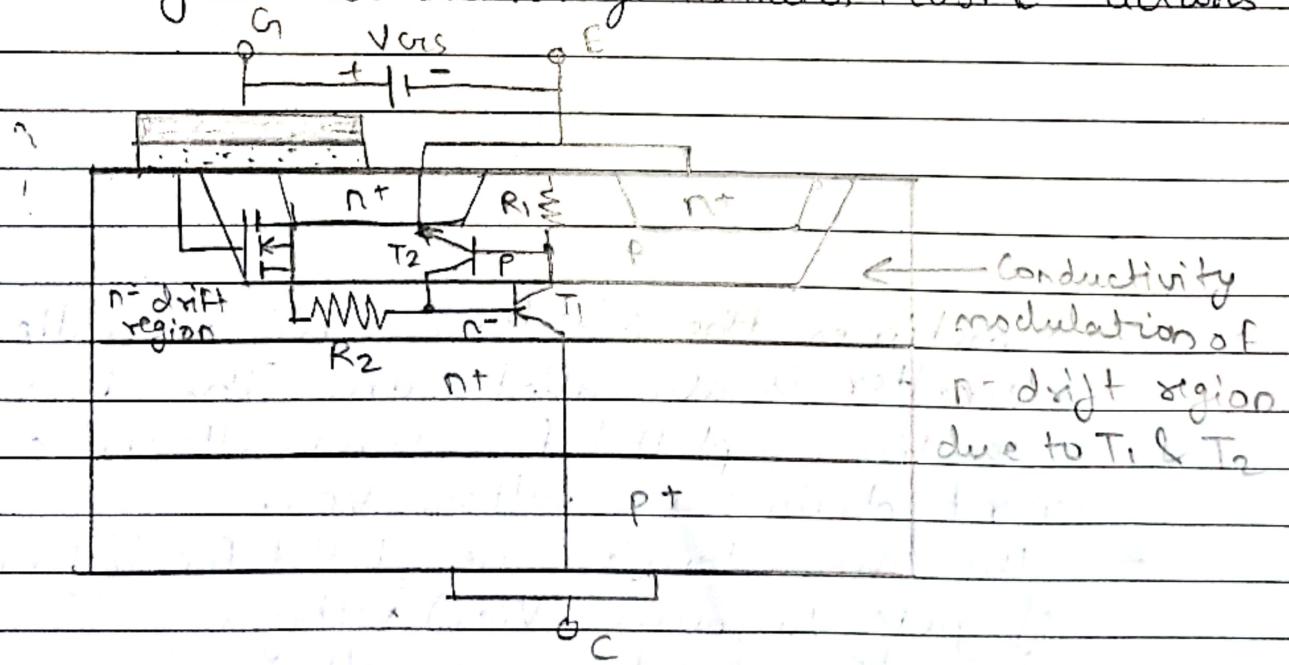
- In the cutoff region, the drain current is negligible and the MOSFET is said to be in 'OFF' state. The MOSFET is driven in cutoff region by applying $V_{GS} < V_{GS(th)}$. Here $V_{GS(th)}$ is the threshold gate source voltage. When gate to source voltage is less than threshold gate source voltage, MOSFET is off, i.e. in cutoff region.
- The MOSFET is driven into ohmic region when $V_{GS} \gg V_{GS(th)}$. In the ohmic region, the MOSFET conducts heavily. Hence it is said to be 'on' in the ohmic region. Thus, by applying heavy gate to source voltage, MOSFET can be turned on.
- In the power electronic applications, MOSFET is never operated in the active region. In active region, it acts as an amplifier. For switching applications, MOSFET is operated only in ohmic and cutoff regions.
- The BV_{DSS} is the drain to source breakdown voltage, when the gate is open circuited. The MOSFET is damaged if drain to source voltage is increased above BV_{DSS} .

IGBT:-

- When $V_{GS} > V_{GS(\text{threshold})}$, then the channel of electrons is formed beneath the gate. These electrons attract holes from p^+ layer. Hence, holes are injected from p^+ layer into n -drift region.
- Thus hole/electron current starts flowing from collector to emitter. When holes enter p -type body region, they attract more electrons from n^+ layer. This action is exactly similar to MOSFET.

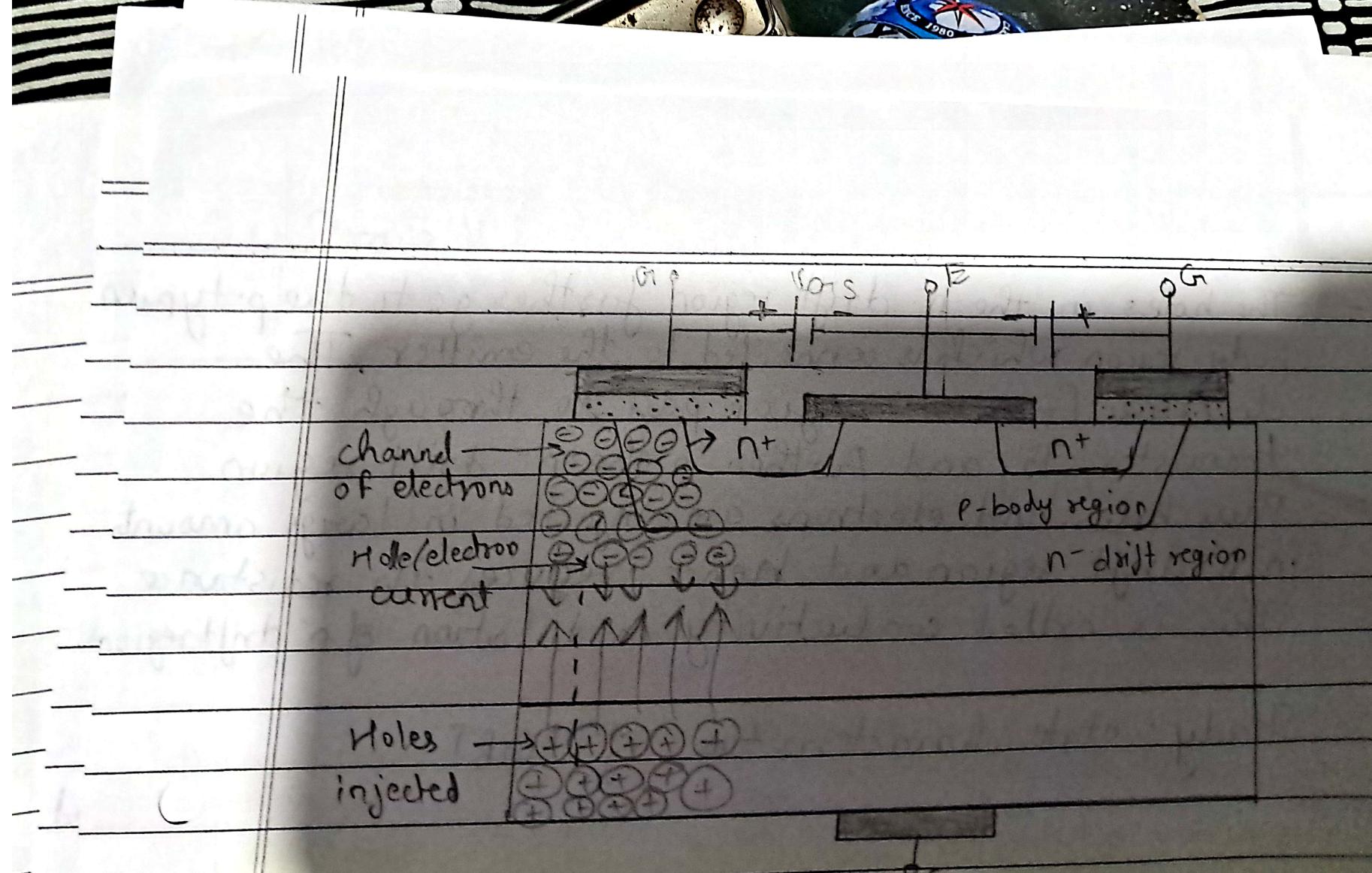


A positive gate to source voltage initiates MOSFET actions



Structure of IGBT

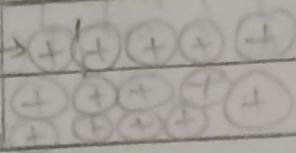
- The MOSFET is formed with input gate, emitter as source and n-drift region as drain. The two transistors T_1 & T_2 are formed. The holes injected by the p+ injecting layer go to the n-drift region. This n-drift region is base of T_1 and collector of T_2 .



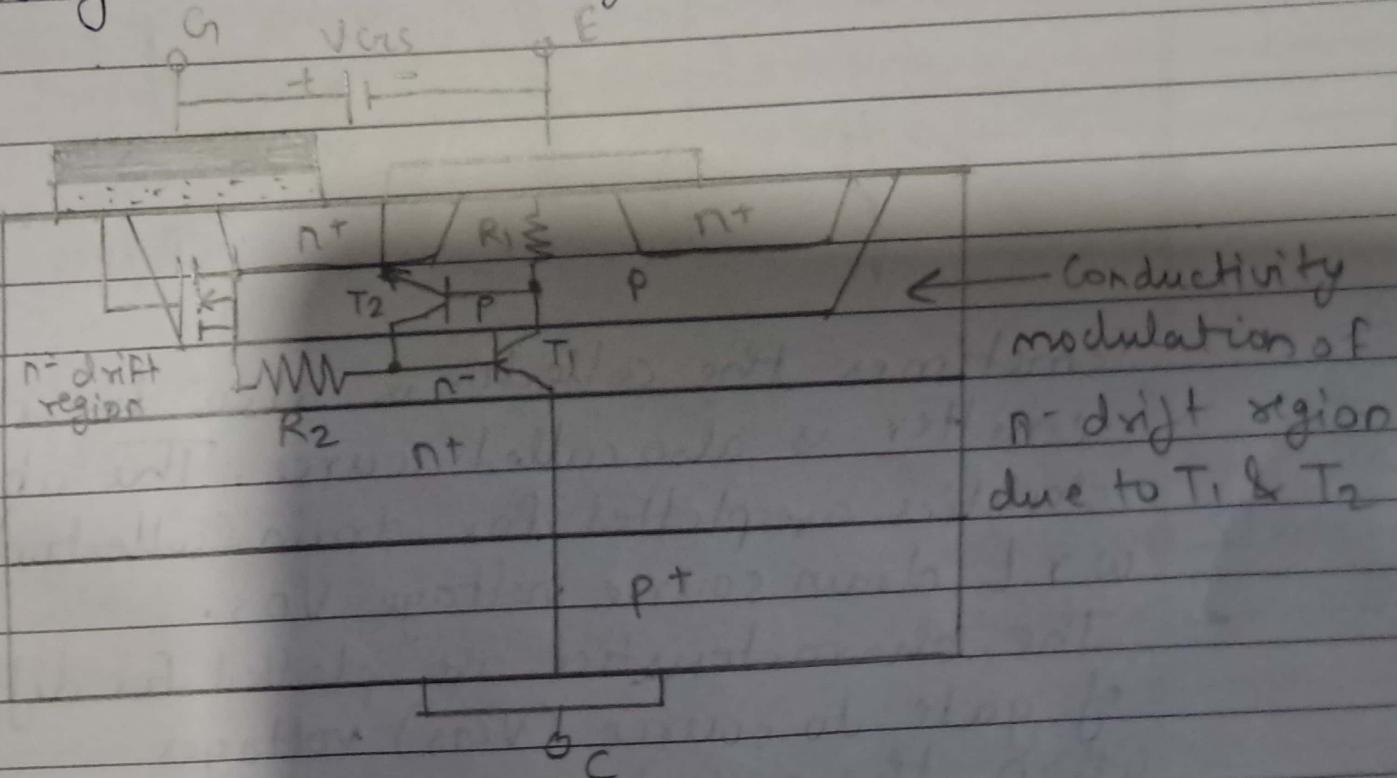
current

Holes

injected



A positive gate to source voltage initiates MOSFET actions



Structure of IGBT

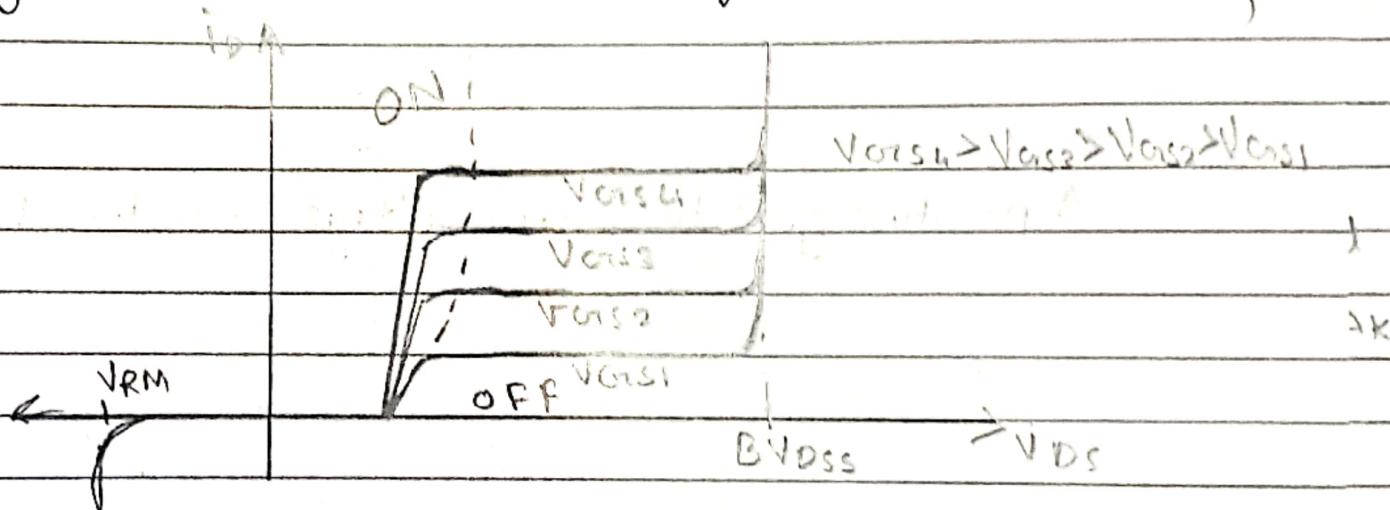
The MOSFET is formed with input gate, emitter as source



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The holes in the n⁻ drift region further go to the p-type body region which is connected to the emitter. The electrons from n⁺ region pass through the transistor T₂ and further in the n⁻ drift region. Thus holes and electrons are injected in large amounts in n⁻ drift region and hence reduces its resistance. This is called conductivity modulation of n⁻ drift region.

Steady state characteristics of IGBT



Sometimes the collector is also called drain and emitter is also called source. The above characteristics are plotted for drain (collector) current i_D w.r.t drain source voltage V_{DS}.

The characteristics are plotted for different values of gate to source (V_{GSS}) voltages.

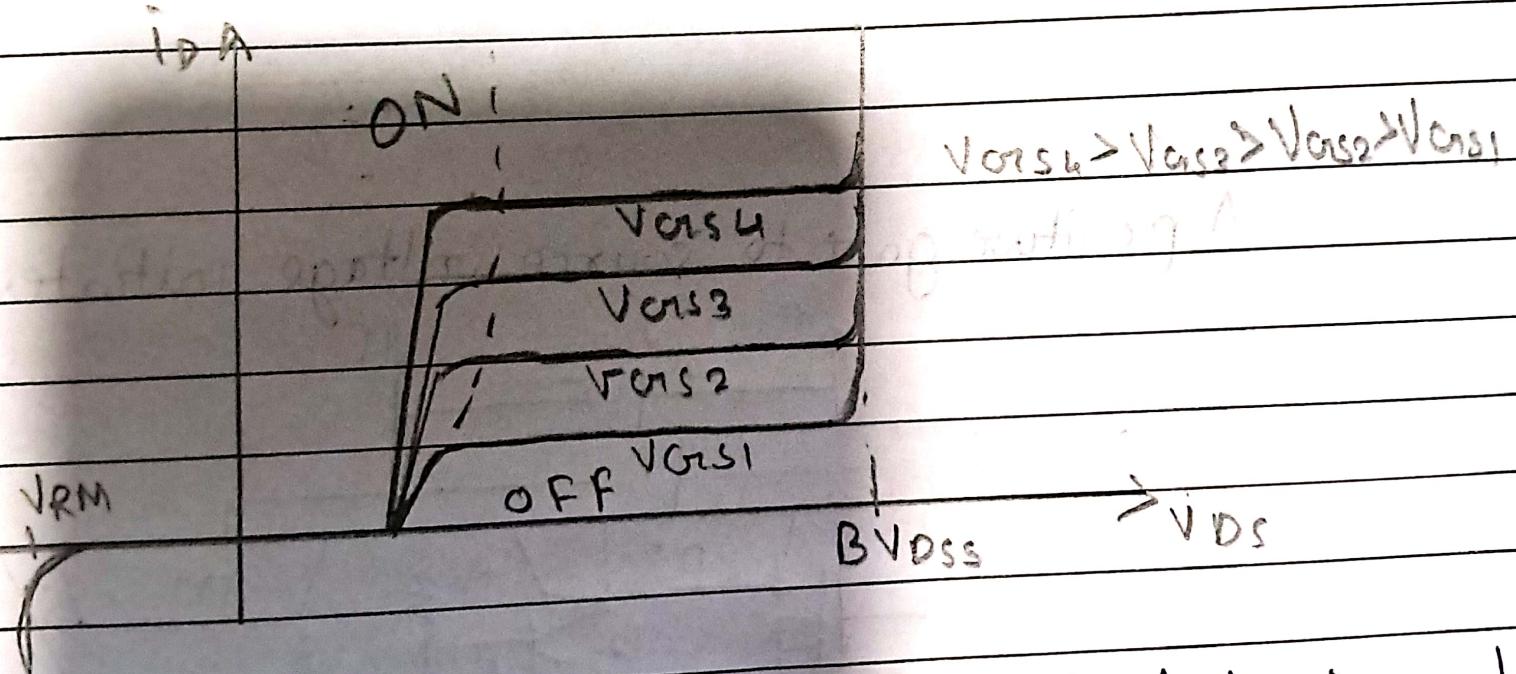
When the gate to source voltage is greater than the threshold voltage ($V_{GSS(TH)}$) the IGBT turns on.

The IGBT is off when $V_{GSS} < V_{GSS(TH)}$

The BV_{DSS} is the breakdown drain to source voltage when gate is open circuited. The IGBT is the popular device now-a-days. The IGBT has simplest drive circuit and it has low on-state losses.

is the n⁻ drift region further go to the p-type or which is connected to the emitter. The z from n⁺ region pass through the T₂ and further is the n⁻ drift region. Ies and electrons are injected in large amount ft region and hence reduces its resistance. called conductivity modulation of n⁻ drift region

state characteristics of TGBT

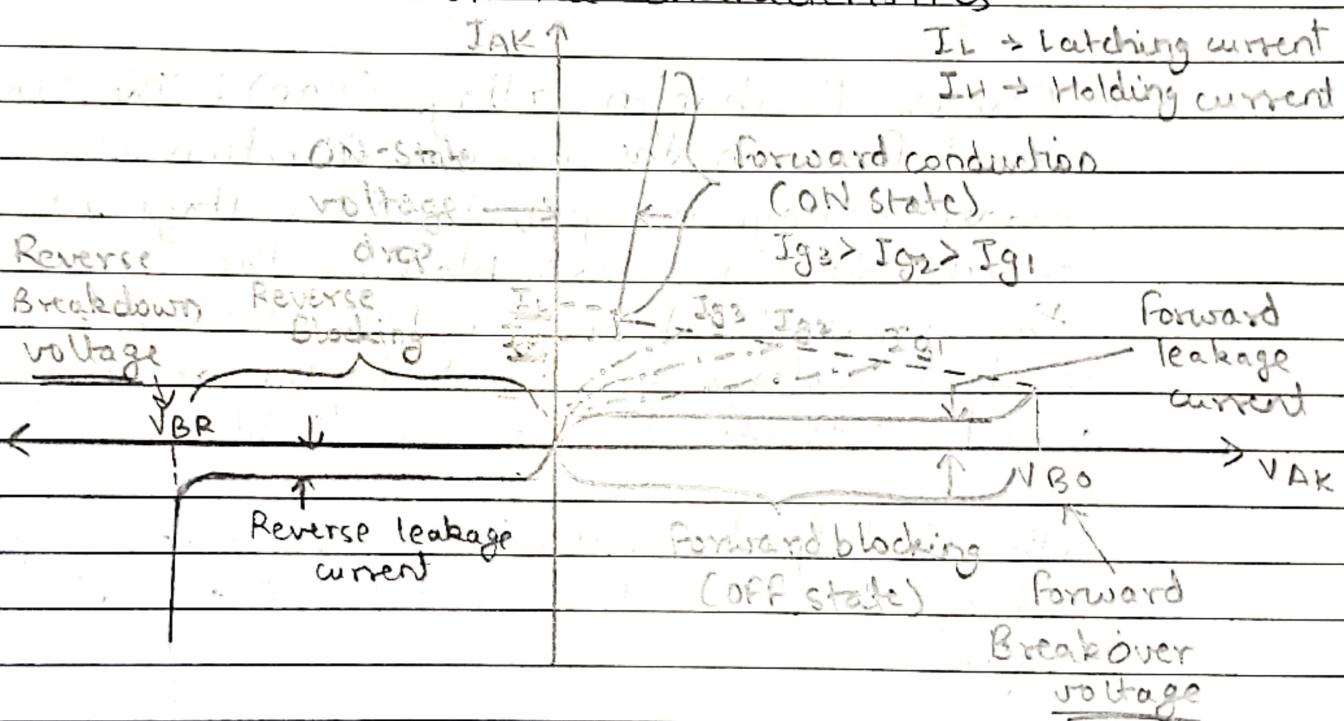


the collector is also ~~also~~ called drain and it is also called source. The above characteristics are plotted for drain (collector) current i_D vs drain source voltage V_{DS}.

characteristics are plotted for different values of source (V_S) voltages. The gate to source voltages is greater than the (V_G) the TGBT turns off.

Q.2 Draw V-I characteristics of SCR. Explain the parameters :
 1) Latching current
 2) Holding current
 3) V_{BO}
 4) V_{BR}

And show them on the characteristics

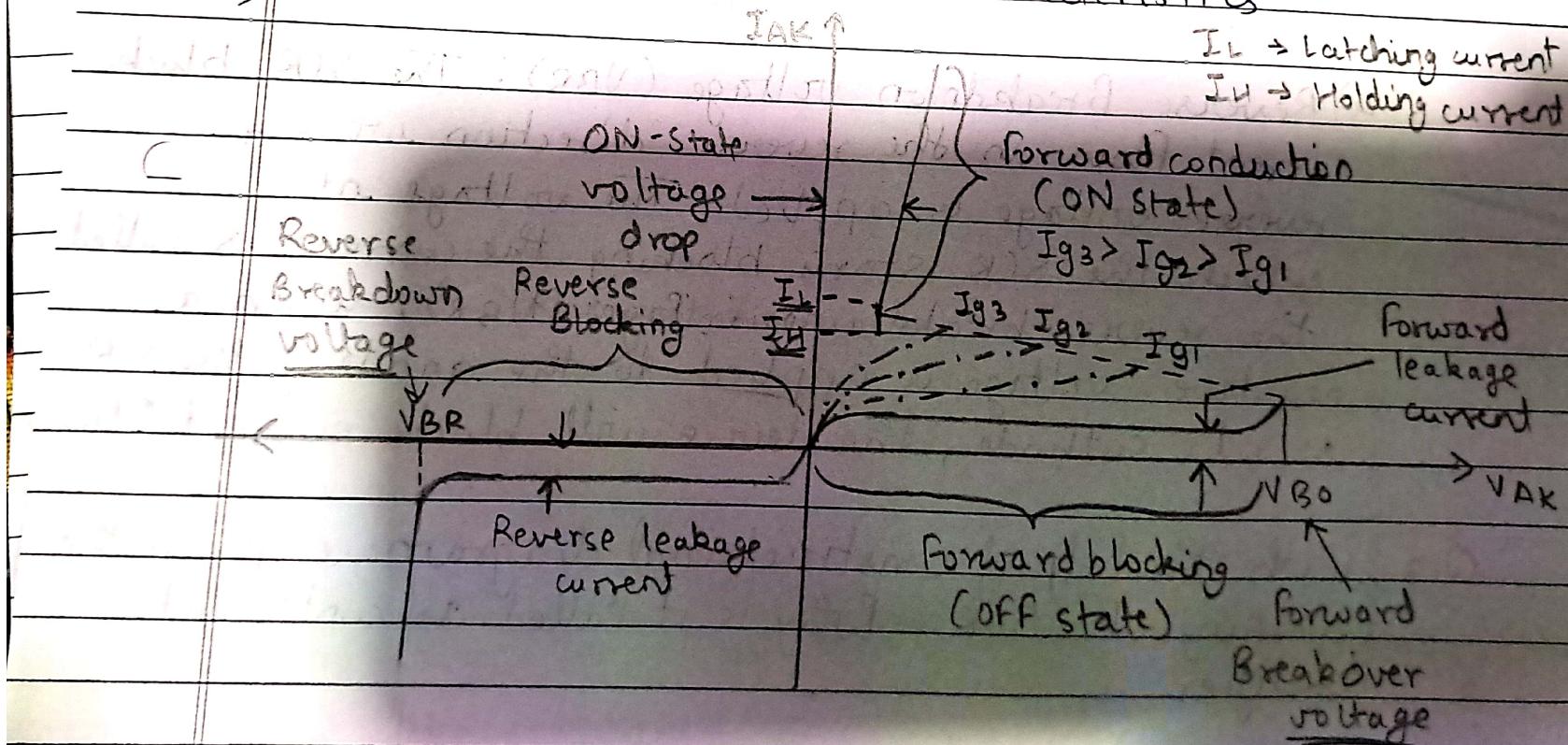


i) Latching current (I_L): It is minimum anode current that must flow through SCR to latch it into the on-state. The latching current is higher than the holding current. The latching current is important when SCR is being turned on.

2) Holding current (I_H): It represents the minimum current that can flow through SCR and still "hold" it in the on-state. The voltage associated with the holding current is termed as holding voltage V_H . If the forward anode current is reduced below holding current SCR will be turned off.

Q.2 Draw V-I characteristics of SCR. Explain the parameters :
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And show them on the characteristics



- i) Latching current(I_L): It is minimum anode current that must flow through SCR to latch it into the on-state

3) Forward breakover voltage (V_{BO}): This is the maximum forward voltage that can be applied between anode and cathode, without initiating forward conduction. This voltage is defined for a zero gate current. In short this is the maximum forward voltage across SCR in its off-state.

4) Reverse Breakdown voltage (V_{BR}): The SCR blocks current flow in the reverse direction when a reverse voltage is applied. The voltage at which the SCR starts blocking the current is called the reverse breakdown voltage (V_{BR}). When a negative voltage is applied to the anode of the SCR w.r.t cathode, the device will block current flow.

Q.3 With the help of constructional diagram; explain the working of SCR. Why is it called as controlled rectifier.

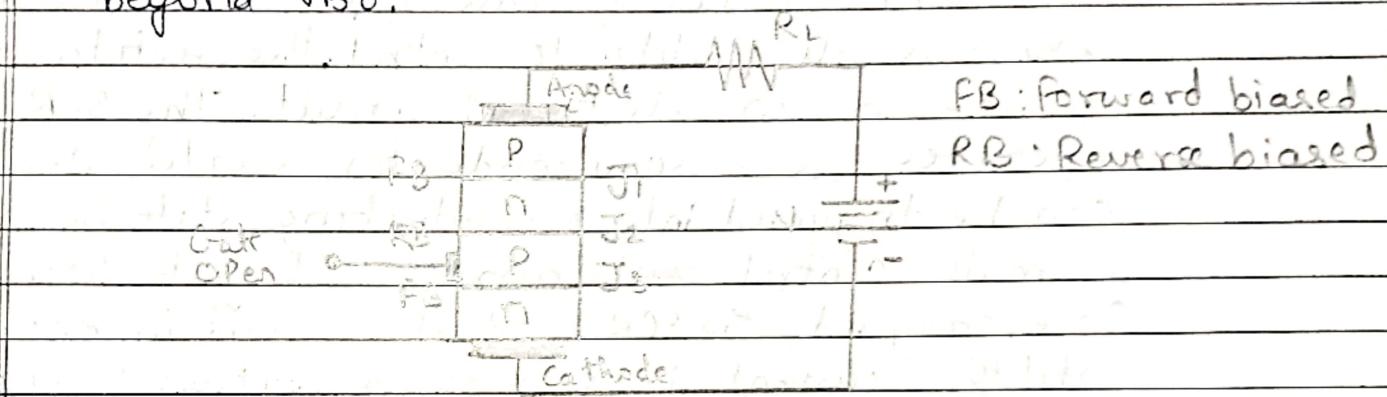
→ The working of SCR can be studied under two different operating conditions

① Operation without gate current:-

- The gate terminal of SCR is left open so that $I_G = 0$. SCR is forward biased by applying a positive voltage to anode w.r.t cathode.
- Out of three junctions, the junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased.
- Therefore current does not flow through the SCR. The entire applied voltage appears across the junction J_2 .
- As the anode to cathode voltage is increased, the

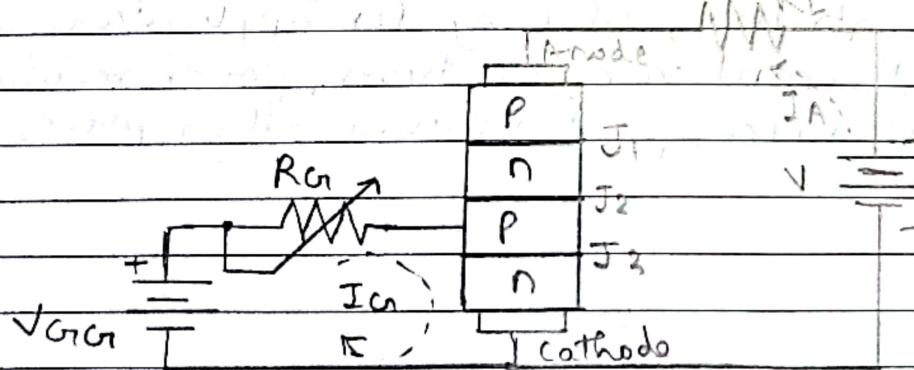
, the voltage across junction J_2 increases.

- At a certain voltage this junction will breakdown and SCR will start conducting. This voltage is called as forward breakover voltage (V_{BO}).
- Thus it is possible to turn on an SCR without any gate current by exceeding its V_{BO} forward voltage beyond V_{BO} .



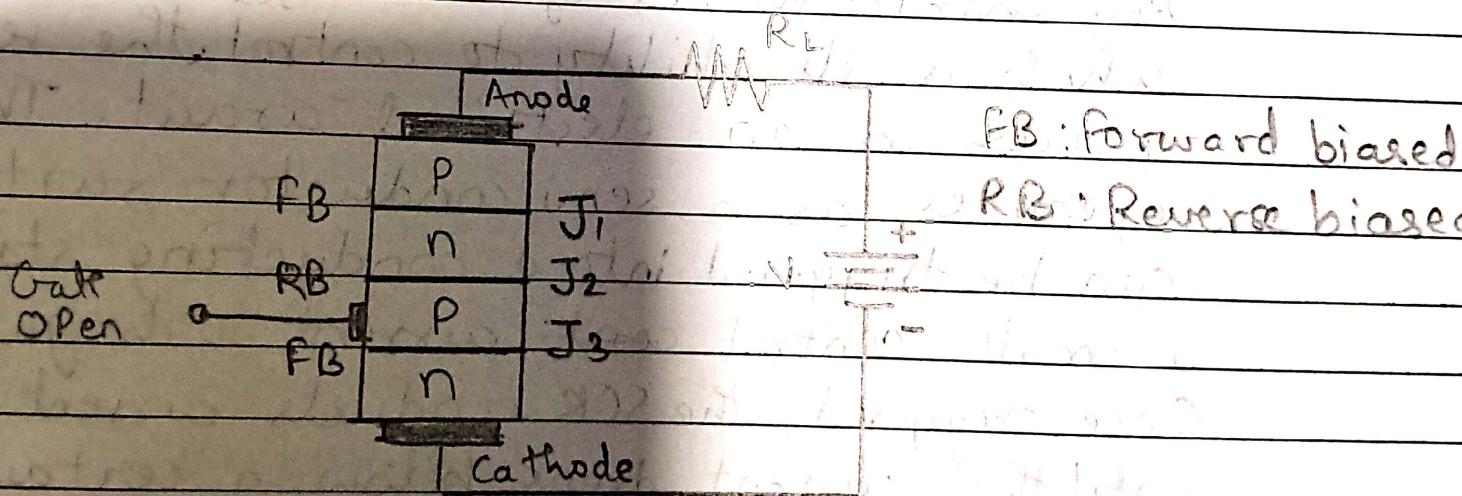
② Operation with Gate Current :-

- The following figure shows that SCR is forward biased as before and the gate cathode junction is also forward biased using an external power source.



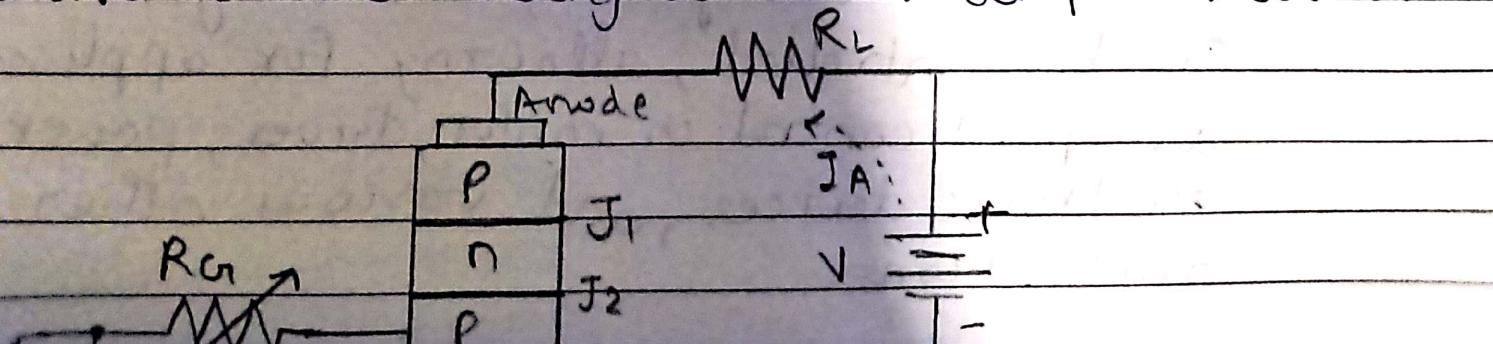
- The gate current I_{Gn} starts flowing which can be adjusted by the resistance R_G .
- As explained, the value of gate current will decide break over voltage of SCR.

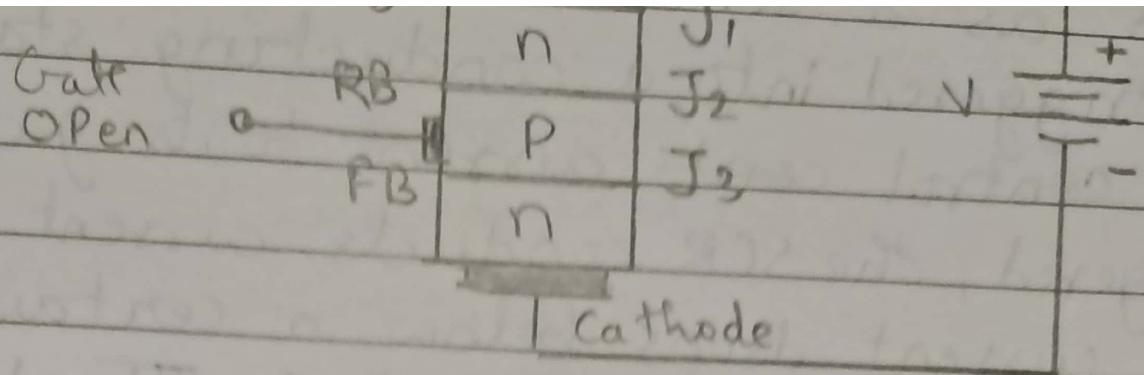
The voltage across junction J_2 increases. At a certain voltage this junction will breakdown and SCR will start conducting. This voltage is called forward breakdown voltage (V_{BO}). Thus it is possible to turn on an SCR without any gate current by exceeding its V_{BO} forward voltage beyond V_{BO} .



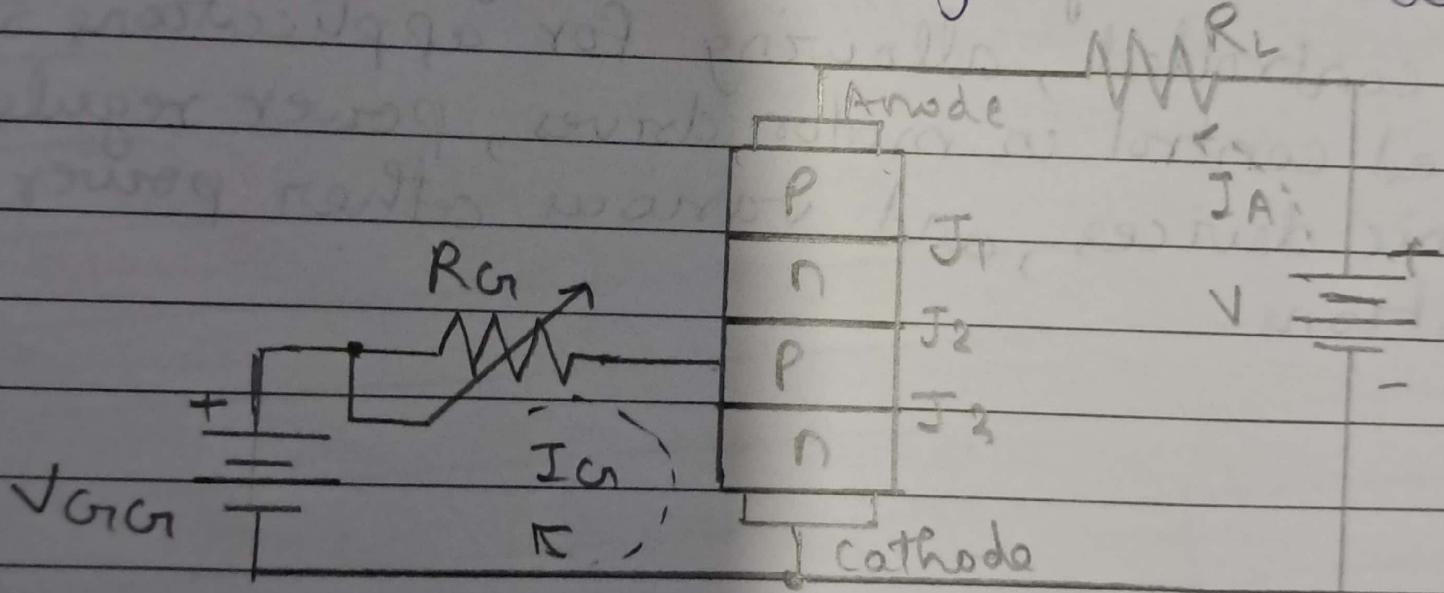
Operation with Gate Current :-

The following figure shows that SCR is forward biased before and the gate cathode junction is also forward biased using an external power source





② Operation with Gate Current :-
 The following figure shows that SCR is as before and the gate cathode junction forward biased using an external power source.



The gate current I_{G1} starts flowing which is limited by the resistance R_{G1} . As explained, the value of gate current determines the breakdown voltage of SCR.

- As I_{cr} increases, the break over voltage of an SCR will decrease i.e. SCR will turn on at lower and lower voltages.
- * The term SCR stands for Silicon Controlled Rectifier. The name "controlled rectifier" reflects the key characteristics of this semiconductor device, which is its ability to control the rectification process in an electrical circuit. The SCR operates as a semiconductor switch that can be triggered into a conducting state by applying a small control current to its gate terminal. Once triggered, the SCR conducts current in one direction until the current drops below a certain level or until a reverse voltage is applied. The term "controlled rectifier" is particularly relevant when the SCR is used in rectifier circuits, where it can control the conversion of AC to DC. By triggering the SCR at specific points in the AC waveform, the rectification process can be controlled, allowing for applications such as speed control in motor drives, power regulation in electronic devices, and various other power control applications.

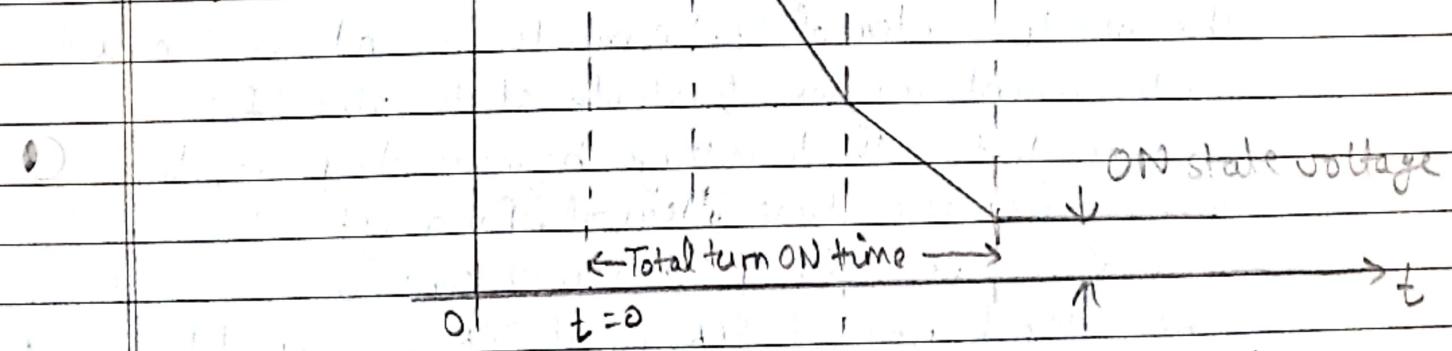
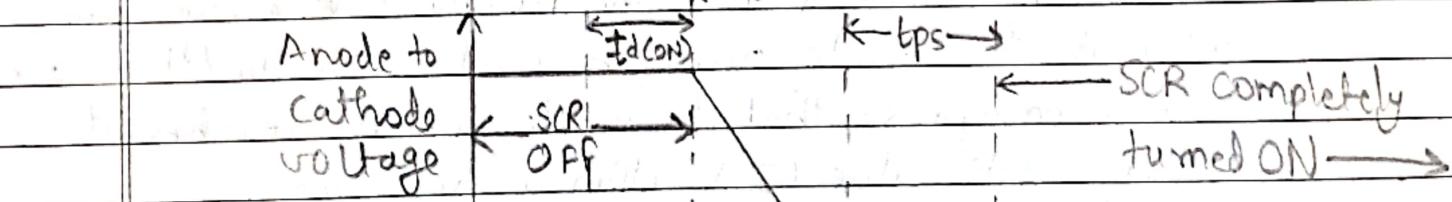
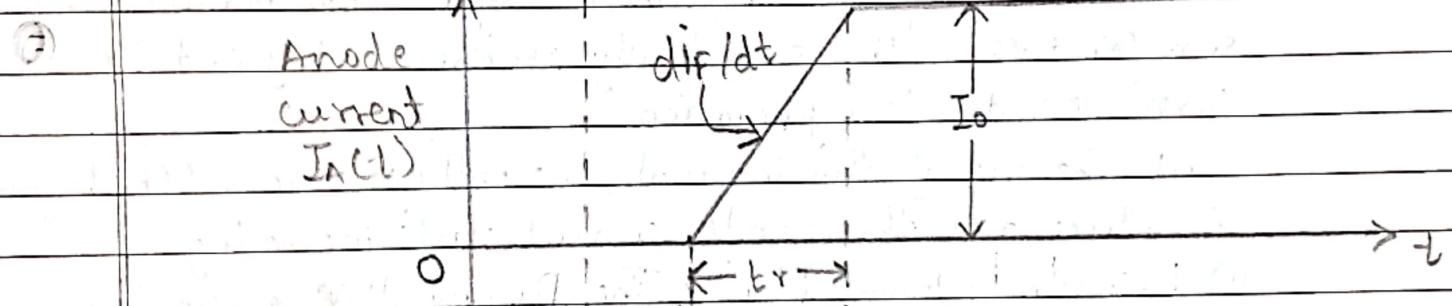
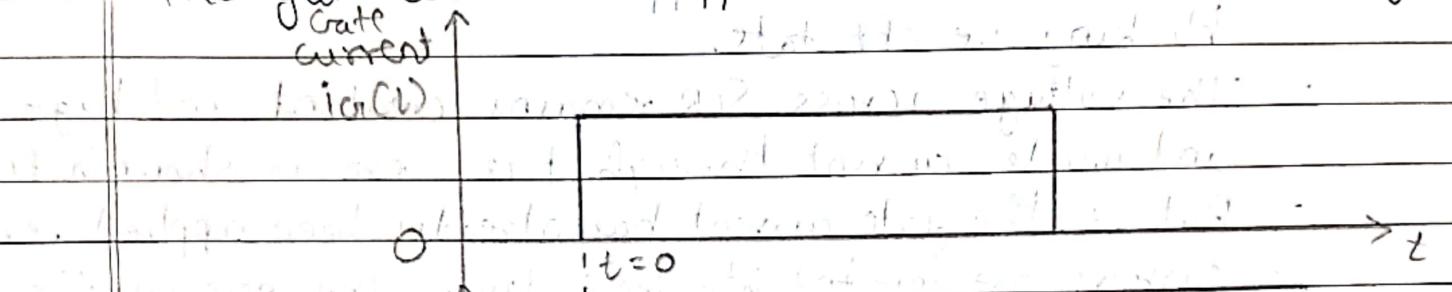
- As I_{on} increases, the break over voltage of SCR will decrease i.e. SCR will turn on at lower and lower voltages.
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Q.3 Draw and explain the switching characteristics of SCR. Write down equation for turn on and turn off time.

→ Switching characteristics of SCR is the time variation of voltage across its anode and cathode terminals and the current through it during its turn on and turn off process.

① Turn-On Characteristics of SCR:-

- SCR is turned on by applying a current pulse of specified magnitude and duration to the gate of the device.
- The gate current is applied at $t=0$ as shown in fig.



- The waveform for the anode current and anode to cathode voltage at the time of turn-on are as shown in Fig.
- The forward anode current increases at a constant rate dI/dt . The total time taken by SCR to turn on completely can be subdivided into three time intervals.

They are :

- 1) The turn-on delay time $t_{d(on)}$,
- 2) The rise time (t_r),
- & 3) The spreading time (t_{ps}).

$$\therefore t_{\text{on}} = t_{d(\text{CON})} + t_r + t_{\text{ps}}$$

i) Turn-on delay time $t_{d(\text{CON})}$: During the turn on delay time $t_{d(\text{CON})}$ the SCR appears to remain the forward blocking i.e off state.

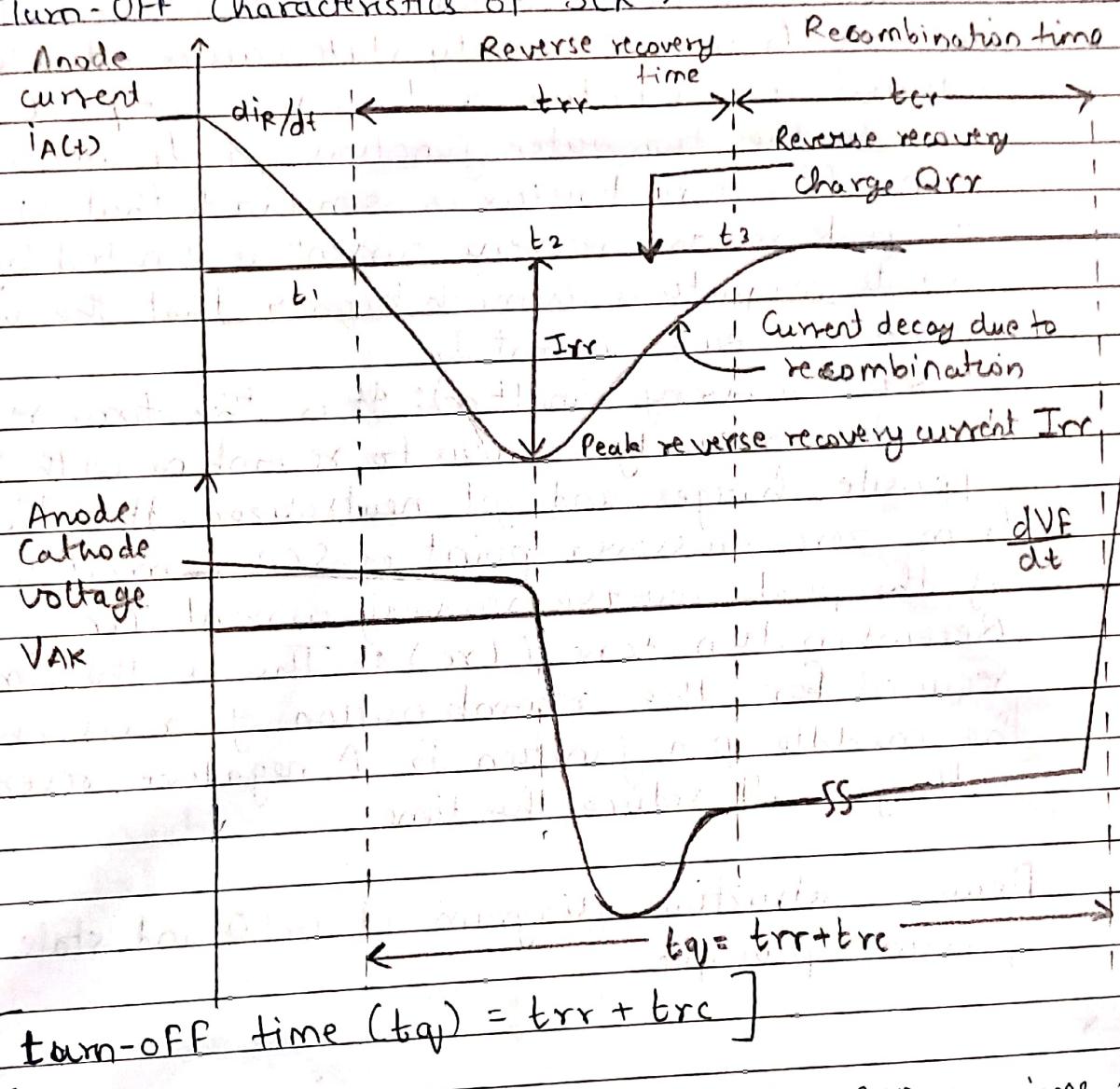
- The voltage across SCR remains constant and high, and anode current through it is zero as shown in fig
- But as the gate current has already been applied, excess carriers are injected into the p_2 layer. This increases the sum $(x_1 + x_2)$. This sum finally reaches unity and SCR turns on, due to regeneration
- At the end of this interval, the voltage across SCR begins to reduce and the anode current starts increasing

ii) Rise time interval (t_r): During this rise time interval the anode current rises at a rate dI/dt . This rate is large enough so that the anode current reaches its steady state value (I_s) within a short time

- The rise time interval (t_r) comes to an end as soon as the anode current reaches its steady state value (I_s)
- The anode to cathode voltage begins to drop rapidly during the rise time interval. Even after the rise time interval is over the plasma will continue to spread over the lateral area of SCR until SCR is completely shorted out by the large number of excess carriers

iii) Plasma spreading interval (t_{ps}): The time required for the plasma to spread from the region around the gate to the entire device cross section is the "Plasma Spreading Time (t_{ps})".

(2) Turn-OFF Characteristics of SCR :

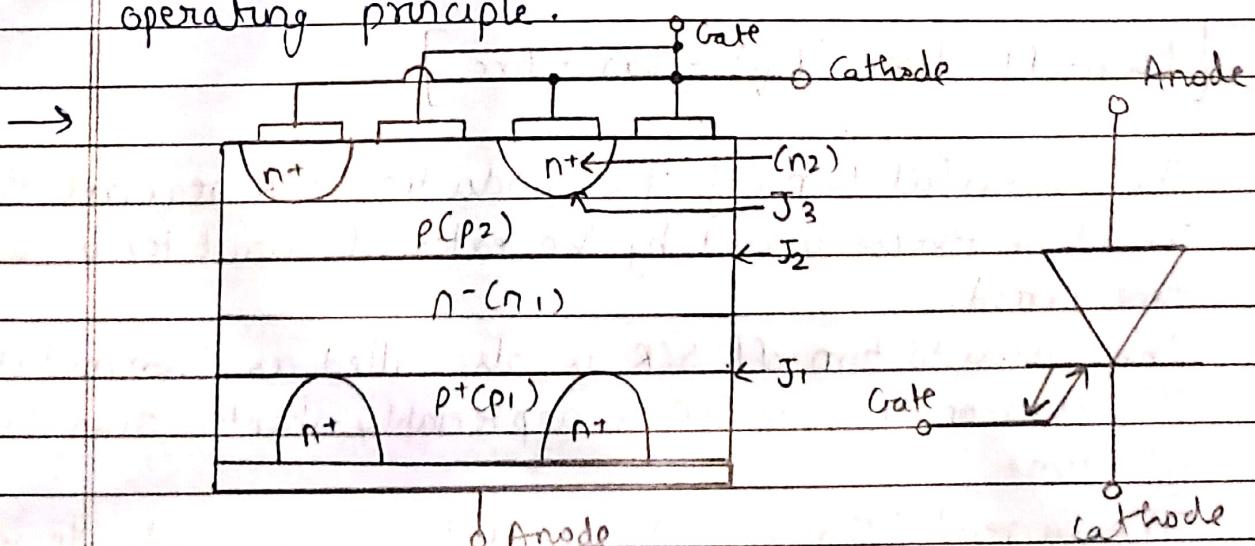


- The successful turn-off of a conducting SCR requires that it should be reverse biased by the external circuit for a minimum time period.
- The process to turn-off SCR is also called as "commutation".
- The turn-on time of SCR is appreciably shorter than the turn-off time.
- The current through the conducting SCR starts decreasing at $t=0$ at a fixed rate dI_A/dt . This rate of change of current is decided by the external circuit. As the current

decreases, the excess carrier in the four layers of SCR decrease from their steady state values, due to the internal recombination and carrier sweepout.

- Due to the two outer junctions j_1 , J_1 and J_3 , the turn-off characteristics is similar to that of a diode. The peak reverse recovery current is denoted by I_{rr} and its magnitude is much higher than the normal reverse blocking current I_r .
- Reverse recovery time (t_{rr}): It is the time required for the minority carriers to recombine with the opposite charges and get neutralized. It is the time from zero crossover point of SCR current to 25% of the peak reverse recovery current I_{rr} .
- Recombination time (t_{rc}): This is the time required for the recombination of excess charges in the middle p-n junction J_2 . A negative reverse voltage will reduce this time.

Q.5 Draw construction diagram of GTO and state its operating principle.



(a) Structure of GTO

(b) Circuit symbol of GTO

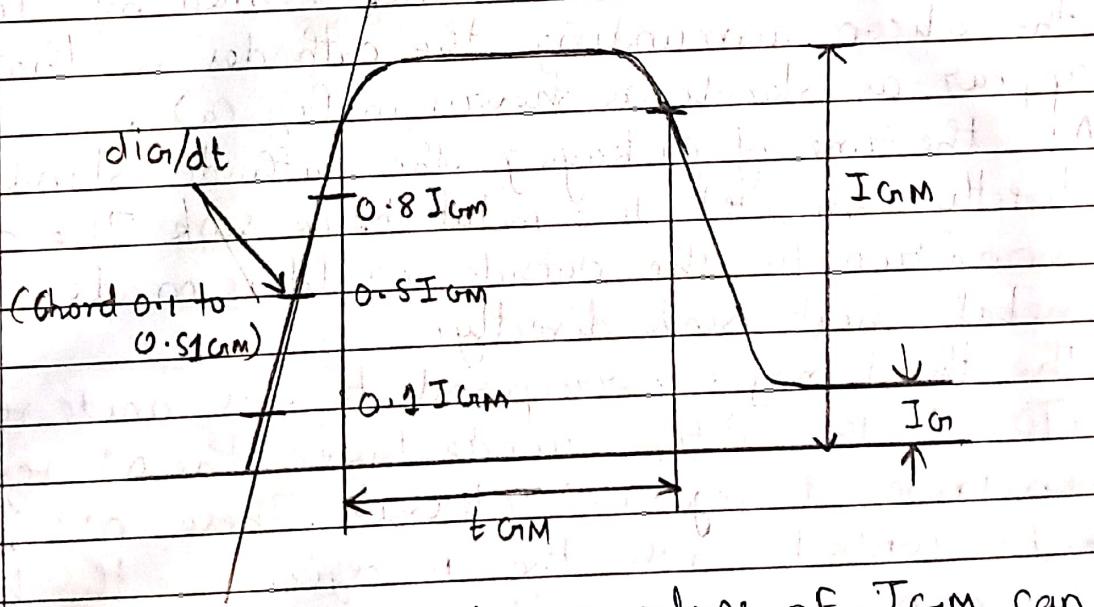
- The basic structure of GTO is basically a four layer structure similar to a conventional SCR as shown in Fig (a).
- Fig (b) shows the circuit symbol for the GTO, which is a three terminal device. Gate is control terminal.
- The two arrows marked on the gate terminal indicate that the gate current for GTO can be either positive or negative.
- The gate & cathode structures of GTO are highly interdigitated as compared to those in SCRs with various types of geometrical forms.
- The cathode areas are usually formed by etching away the silicon surrounding the cathodes so that they appear as islands as shown in Fig (a).
- At the time of packaging the cathode islands are directly connected to a metal heat sink. The cathode connection to the outside world is made with this metal heat sink directly.
- The third major corresponds to the anode region of GTO. In the P type anode layer the n⁺ regions penetrate at regular intervals. These 'n⁺' regions make contact with the n⁻ region i.e. the base layer n⁻. This results in the so called "Shorted Anode Structure" of GTO.
- **Operating Principle:** The turn on mechanism of GTO is exactly same as that of a conventional SCR. The dependence of GTO's breakover voltage on the magnitude of gate current is also same as that of SCR.
- In short, the working principle of GTO at the time on and in the on state is same as that of SCR.

- However, the operation at the time of turn-off is entirely different. In order to turn off a conducting CrTO, we have to apply a negative gate current pulse at the gate terminal.

Q6. Explain turn on, turn off mechanism in GTO.

→ Turn ON :

- A GTO has a highly interdigitized gate structure with no regenerative gate. Thus, it requires a large initial gate triggering pulse.

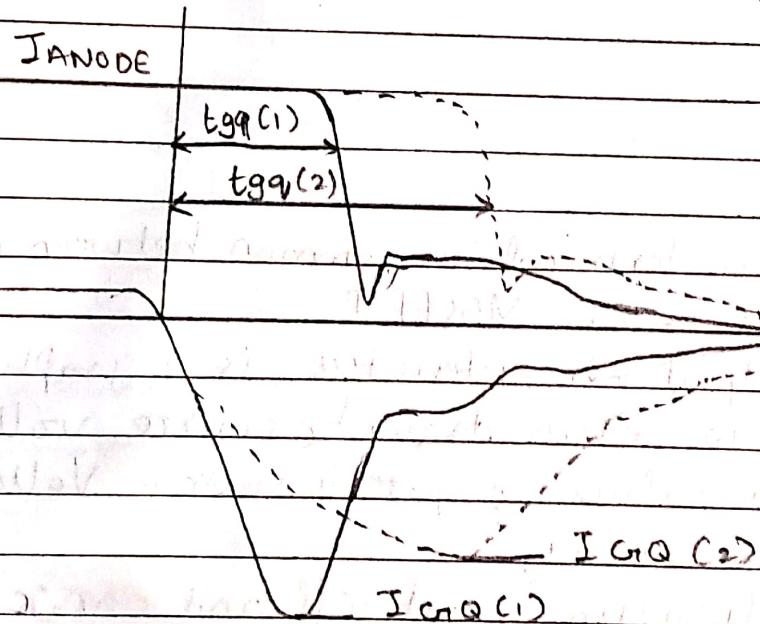


- Minimum and maximum values of I_{Gm} can be derived from the device data sheet. A value of $dig = dt$ positioned against turn-on time is given under the device characteristics found on the data sheet.
- The rate of rise of gate current $dig = dt$ will affect the device turn-on losses. The duration of the I_{Gm} pulse should not be less than half the minimum forward time given in data sheet ratings.

- A longer period will be required if the anode current dI/dt is low such that I_{anode} is maintained until a sufficient level of anode current is established.

Turn OFF :

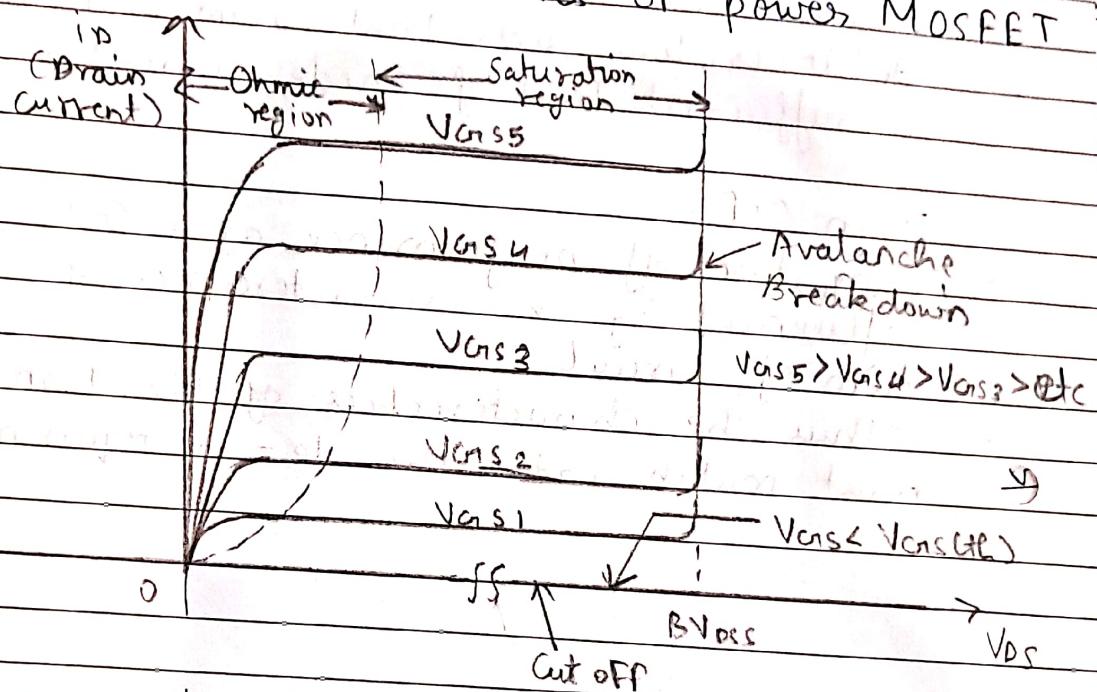
- The turn-off performance of a CrTO is greatly influenced by the characteristics of the gate turn-off circuit
- Thus the characteristics of the turn-off circuit must match with the de-ice requirements.



- Fig shows the typical anode and gate currents during the turn-off. The gate turn-off process involves the extraction of the gate charge, the gate avalanche period, and the anode current decay.
- The amount of charge extraction is a device parameter and its values is not affected significantly by the external circuit conditions.
- The initial peak turn-off current and turn-off time, which are important parameters of the turning-off process, depend on the external circuit components.

Q.7.

→ Explain J-V characteristics of power MOSFET

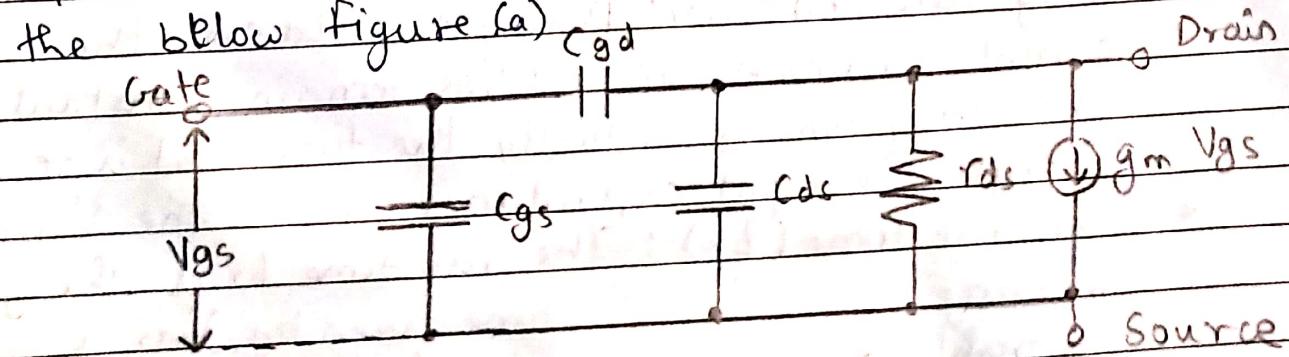


- The source terminal is common between the i/p & o/p of the mosfe MOSFET
- The output characteristics, is a graph of drain current in versus drain to source voltage V_{DS} for different values of gate to source Voltage V_{GS} as shown it fig.
- The saturation, cut-off and ohmic regions of the characteristics are also shown in fig.
- In the power electronic applications where the MOSFET is used as switch, the device must be operated in the cut-off and ohmic region when turned off and on respectively
- The operation in the saturation region should be avoided to reduce the power dissipation in the on-state
- The MOSFET is in the cut-off state when the gate source voltage V_{GS} is less than the threshold voltage $V_{G(S)th}$.

- The device must withstand to the applied voltage and to avoid the breakdown the drain to source breakdown voltage should be greater than the applied voltage
- The breakdown takes place due to the avalanche breakdown of the drain body junction.
- When a larger positive gate to source voltage is applied power MOSFET goes into the ohmic region where drain to source voltage $V_{DS(on)}$ is small
- In this region of operation the power dissipation can be kept reasonably low, by minimizing the on-state voltage
- In the saturation region the drain current is almost independent of the drain to source voltage V_{DS} . It is only dependent on the gate to source voltage V_{GS} .
- In the saturation region the gate voltage V_{GS} is greater than the threshold voltage $V_{GS(th)}$ and the drain current increases with increase in V_{GS} .

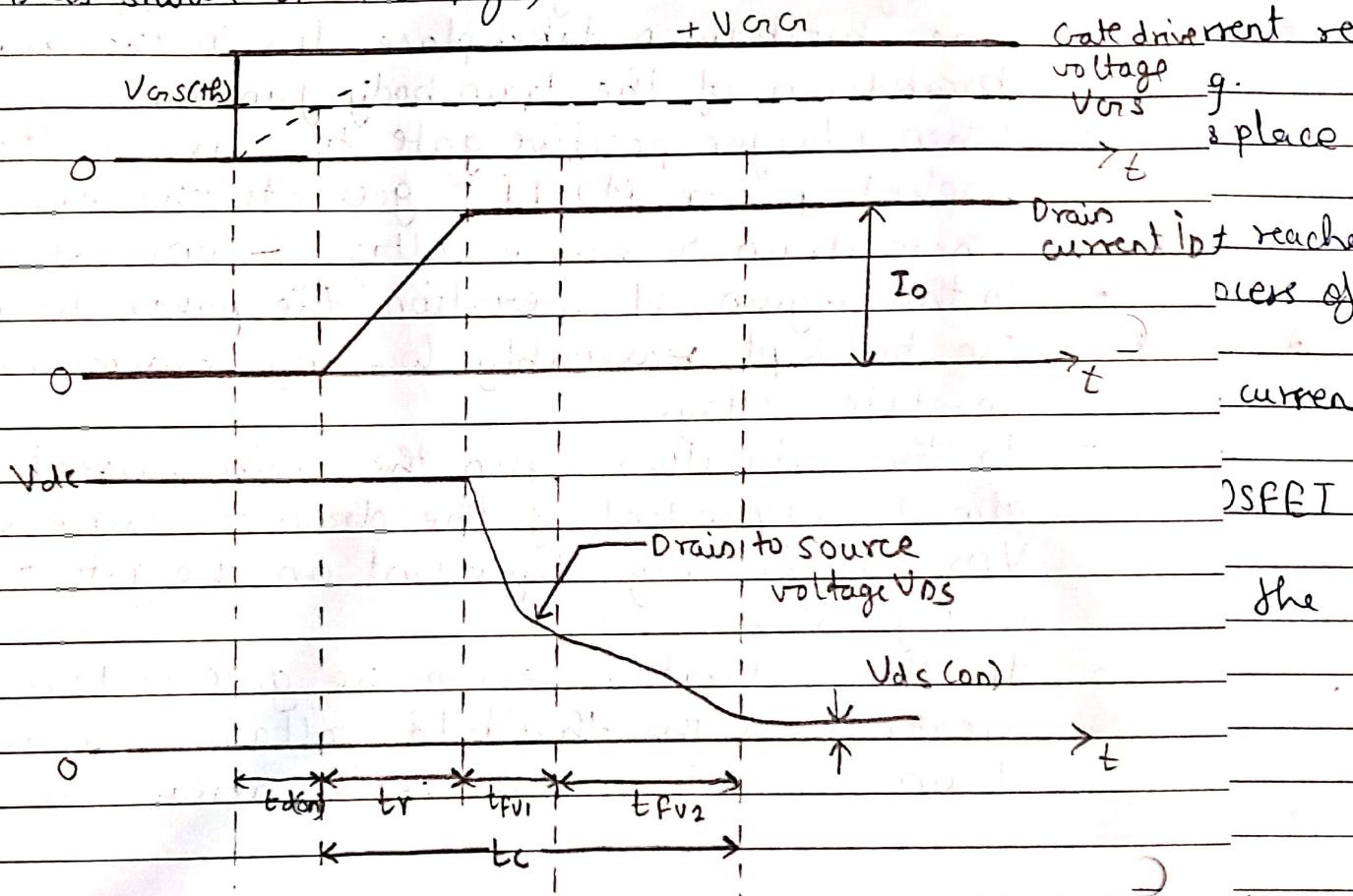
Q.8 Draw and explain the switching characteristics of FET, MOSFET

→ The switching mode of MOSFET is shown in the below figure (a)



* Turn on Characteristics :

- The turn on characteristic of power MOSFET is as shown in the Fig(b) below

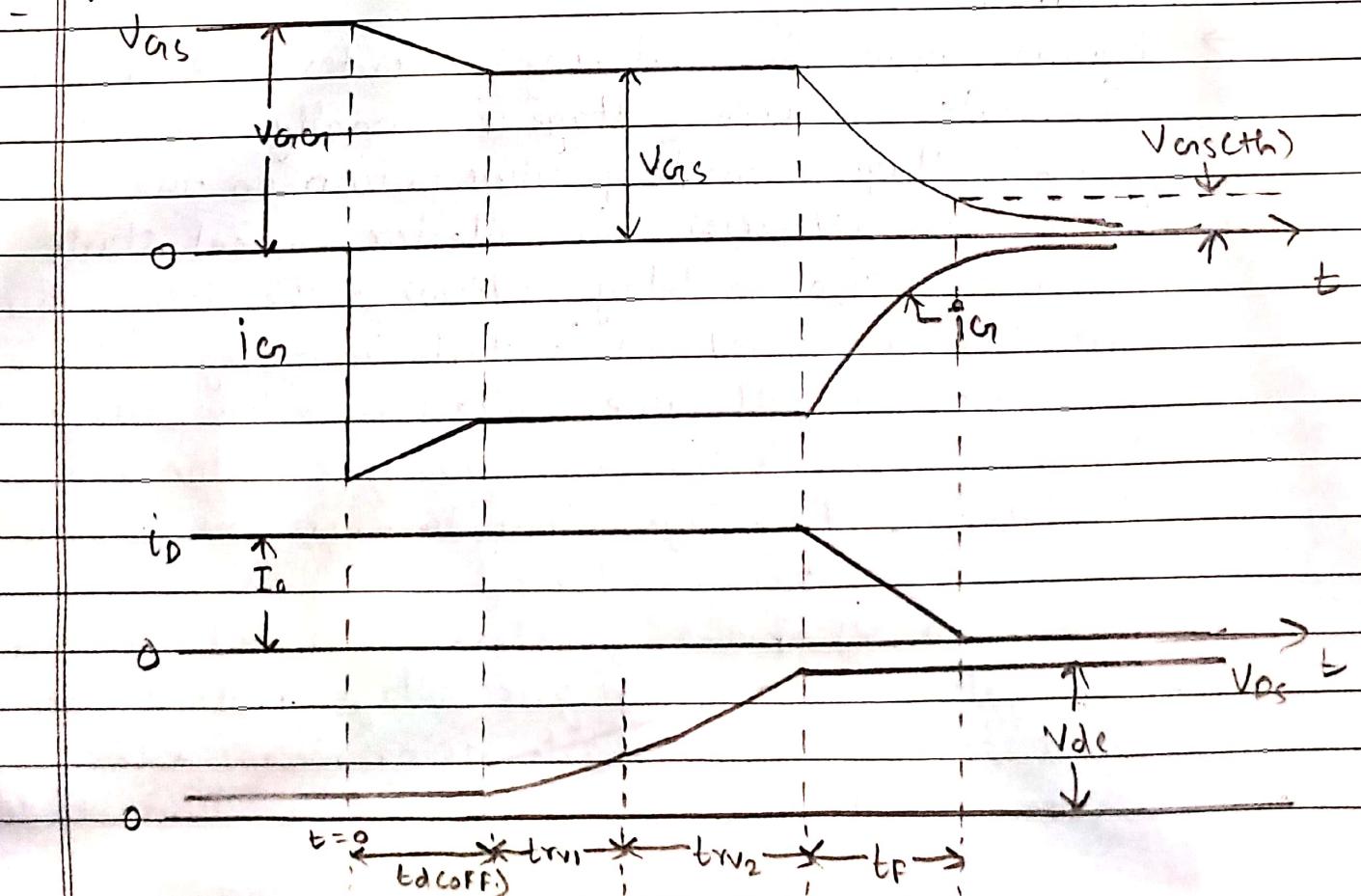


- The gate to source voltage changes from 0 to $+V_{GS(th)}$ at $t=0$
- This voltage is much higher than the minimum gate to source voltage $V_{GS(th)}$.
- * **Delay time ($t_{D(on)}$):** During the $t_{D(on)}$, the drain current remains zero and V_{DS} remains constant at V_{DC}
- The delay time is actually the time that is required to charge the input capacitance (C_{GS}) to the $V_{GS(th)}$
- * **The rise time (t_r):** The rise time t_r is the gate charging time. It is the time taken by V_{GS} to rise from the threshold voltage $V_{GS(th)}$ to the full gate voltage V_{GSP}
- The time t_r required for the drain current to rise from

0 to I_0 is the current rise time t_r . The V_{ds} remains constant during the rise time interval

- At the end of rise time interval, the drain current reaches its maximum value I_0 and V_{ds} starts decreasing.
- The reduction in V_{ds} from V_{de} to $V_{ds(\text{con})}$ takes place in two distinct time intervals t_{FV1} and t_{FV2} .
- At the end of interval t_{FV2} , the V_{ds} finally reaches its on-state value $V_{ds(\text{con})}$ and the turn-on process of the MOSFET gets complete.
- During the two intervals t_r and t_{FV1} , the drain current and V_{ds} both have substantially high values.
- Therefore, the power dissipated in the power MOSFET will be extremely large.
- To reduce this power loss, the turn-on time of the MOSFET should be minimized.

* Turn-off characteristics:



- The turn off process of the MOSFET is based on an inverse sequence of operation that occurred during turn on
 - * Turn-off delay time $t_{d(\text{OFF})}$: It is the time required for the input capacitance C_{GS} to discharge completely. V_{GS} needs to reduce significantly before V_{DS} starts rising. The time intervals tr_{V1} and tr_{V2} should be as short as possible to reduce the power dissipation taking place in a power MOSFET.
 - * The Fall time t_f : This is the time required for the input capacitance C_{GS} to discharge from the pinch-off region to the threshold voltage, because if $V_{\text{GS}} \leq V_{\text{GS}(\text{th})}$, then the power MOSFET will be turned off. The total turn off time is given by,
- $$t_{\text{OFF}} = t_{d(\text{OFF})} + \text{tr}_{V1} + \text{tr}_{V2} + t_f$$

Q.9 Draw and explain the switching characteristics of IGBT.

- Fig (a) shows the switching characteristics of IGBT. The gate to source voltage is normally negative. This voltage is made positive to turn-on the IGBT. When $V_{\text{GS}} > V_{\text{GS}(\text{th})}$, the collector current starts increasing. Turn-on delay, $t_{d(\text{ON})}$ is the delay when gate drive is applied and i_c starts increasing. When i_c increases to its full value, collector-emitter voltage starts falling. 'tri' is the rise time of collector and t_{fV} is the fall time of voltage. Thus, turn-on time of IGBT is,
- $$t_{\text{ON}} = t_{d(\text{ON})} + \text{tri} + t_{fV}$$
- The turn off of the IGBT is initiated by reducing the gate voltage. When gate voltage falls to the value equal to V_{GS1} , V_{CE} starts rising. V_{GS1} is the voltage where IGBT comes out of saturation. Turn-off delay

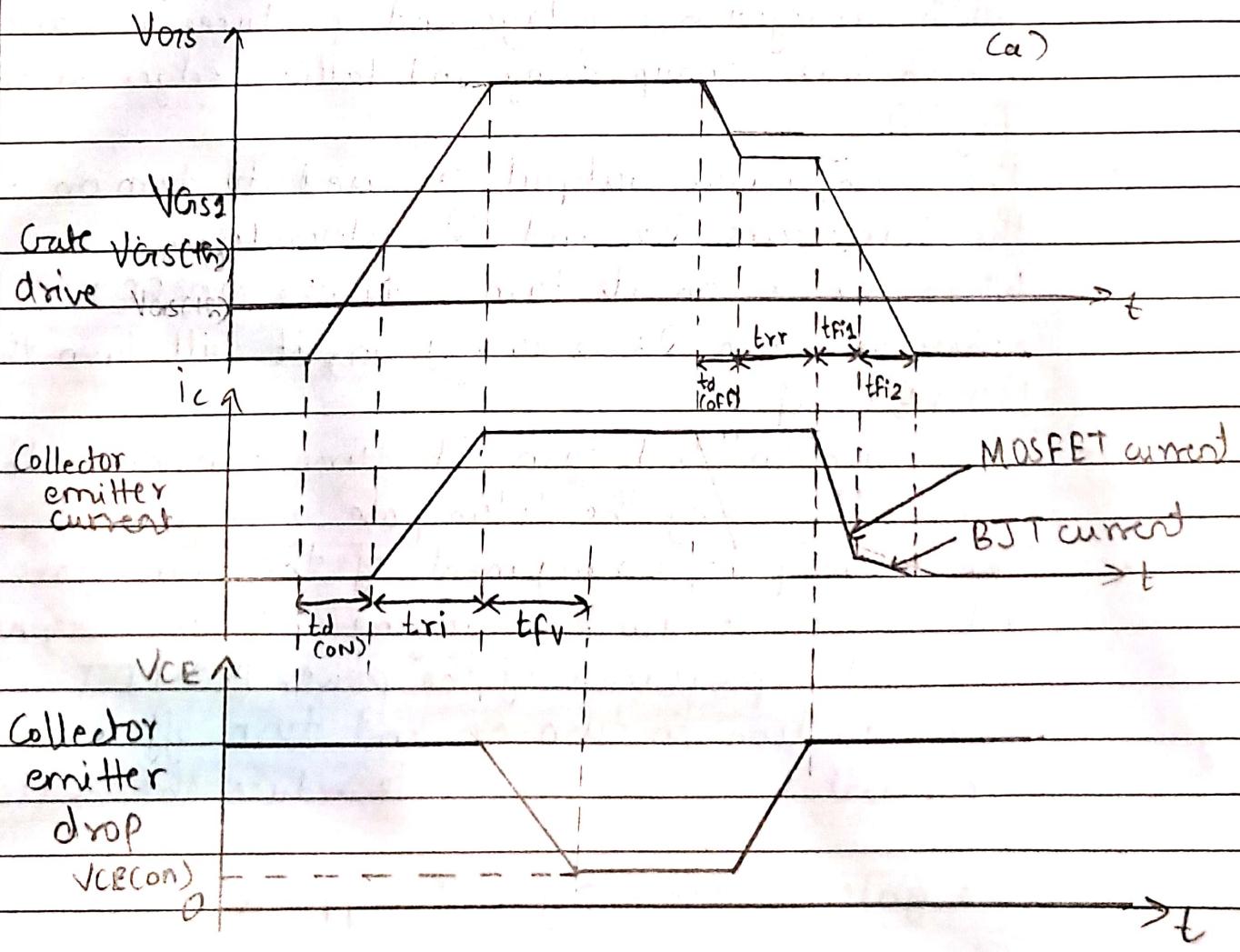
$t_{d(\text{OFF})}$ is the delay time when gate voltage is reduced and V_{CE} starts increasing. When V_{CE} reaches to supply voltage, i_c starts reducing, i_c reduces fast till V_{CE} reaches to $V_{OVS(\text{th})}$. This fast decay is i_c is basically due to internal MOSFET. Then V_{CE} goes to zero and becomes negative. But i_c keeps on flowing for some time. This is internal BJT current. This current flows due to stored carriers in the drift region. Hence, turn off time of IGBT is higher than TGBT. The turn-off time of TGBT will be,

$$t_{\text{off}} = t_{d(\text{OFF})} + t_{rv} + t_{f1} + t_{f2}$$

Here, t_{rv} is voltage rise time

t_{f1} is MOSFET current fall time

t_{f2} is BJT current fall time.



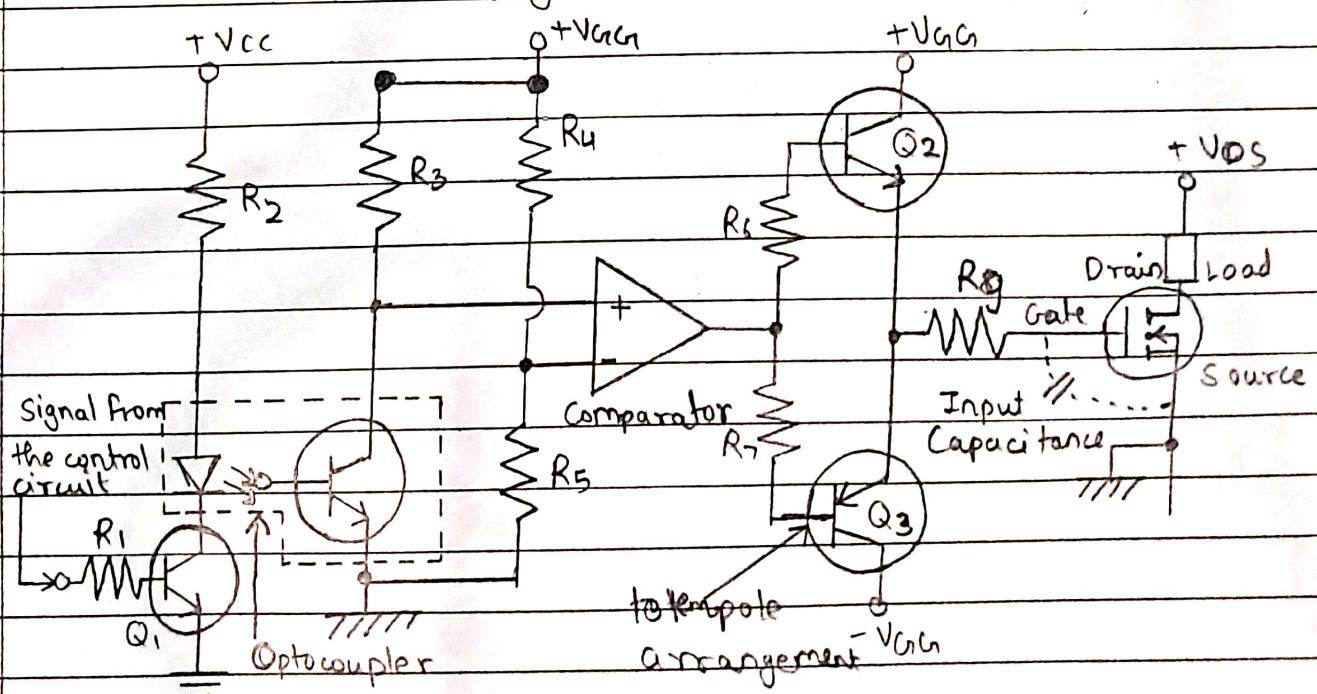
Q.10 Explain isolated gate drive circuit for MOSFET and explain its operation.

- A typical gate driving circuit is as shown in Fig(a)
- The totem-pole arrangement of the driver transistors Q₂ and Q₃ is for quick charging and discharging of the input capacitance of MOSFET.
- The signal from the control circuit is applied to the base of transistor Q₁.
- The opto coupler couples this signal to the input of the comparator.
- The opto coupler isolates the control circuit from the high power circuit.
- The comparator compares the output of opto coupler with a reference voltage and produces a waveform which has sharp rising and falling edges as shown in Fig(b).
- The comparator output is used to turn on and off the transistors Q₂ and Q₃ alternately.
- When Q₂ is on it turns ON the MOSFET whereas when Q₃ is turned on, it will turn the MOSFET off.
- The turn-on and turn-off time can be further reduced by using the totem-pole arrangement.
- The totem-pole arrangement of the transistors Q₂ and Q₃ ensure quick charging and discharging of the input capacitance of the power MOSFET.
- The reduction in turn-on and turn-off time is important because it helps to reduce the switching loss.
- The gate resistance R_g will suppress oscillations.

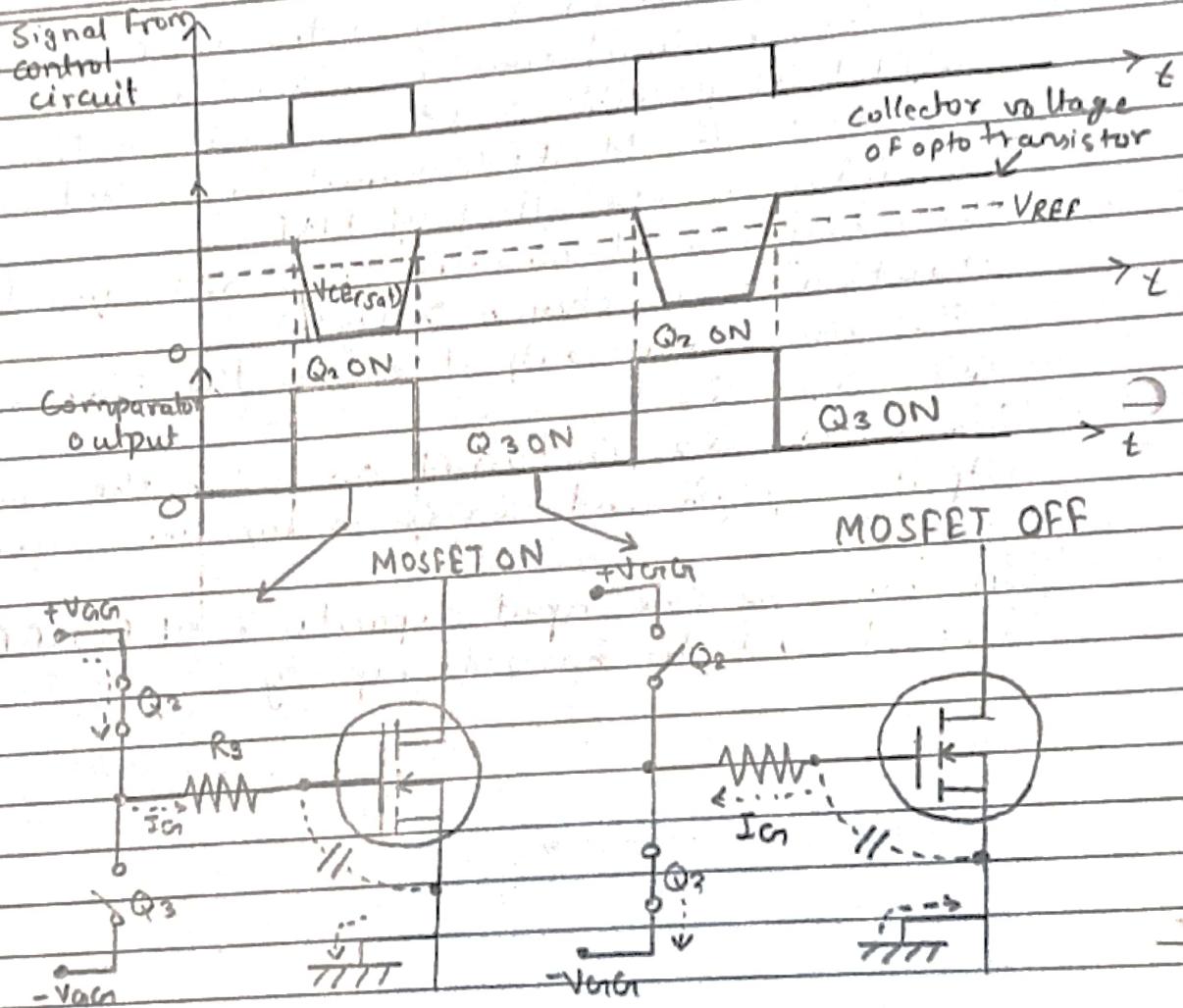
generated due to stray inductance

- The driver circuit must be placed as close to the MOSFET as possible and the wires from the drive circuit to the MOSFET must be twisted in order to minimize the effect of EMI.
 - The waveforms at various points and equivalent circuits are as shown in Fig (b)
 - The comparator output drives the transistors Q_2 and Q_3
 - Transistor Q_2 is turned on when the comparator output is high and Q_3 is on for low comparator output.
 - In this way the input capacitance of MOSFET is charged and discharged rapidly.

Fig (a)



Q.10 Explain



Q.11 Compare SCR, MOSFET, IGBT and GTO.

Parameter	SCR	MOSFET	IGBT	GTO
i) Symbol				

Parameter	SCR	MOSFET	IGBT	GTTO
2) Switching Frequency	500 Hz	100 kHz	20 kHz	2 kHz
3) On-state drop voltage	< 2 Volts	4-5 Volts	3 Volts	3 Volts
4) Maximum VI ratings	10 kV/5 kA	600 V/200 A	60-1.5 kV/400 A	5 kV/5 kA
5) Snubbers	Unpolarized	Not essential	Not essential	Both optional
6) Type of device	Minority carrier	Majority carrier	Minority carrier	Minority carrier
7) Communication circuit	Necessary	Not Necessary	Not Necessary	Not Necessary
8) Gate drive current	Current	Voltage	Voltage	Voltage
9) Temperature coefficient	Negative	Positive	Flat	Negative
10) Applications	DC motor drives, inverters, rectifiers etc	AC motor control, SMPS, DC choppers etc	SMPS, BLDC drives, AC motor control, UPS, etc	Inverters, UPS, DC motor drives, etc