

The capacitor voltage and secondary pulses are as shown in Figs. 1.14.11(c) and (d) respectively.

These pulses are used as triggering pulses for the SCR.

As the capacitor discharges and V_C reaches the point voltage V_V , the UJT is turned off and the capacitor starts charging again, through R.

The charging rate of the capacitor is decided by the value of R.

Therefore it is possible to change the firing angle α by varying the potentiometer R. The firing angle can be changed from 0 to 180°.

Resistance R_2 of Fig. 1.14.10 will partly compensate for the effect of temperature on the oscillator frequency.

Synchronization :

The voltage across the zener diode is used as supply voltage for the relaxation oscillator.

This voltage (V_z) passes through zero at $\omega t = 0, 2\pi, 3\pi, \dots$ etc. as shown in Fig. 1.14.11(b).

Therefore the capacitor voltage also becomes zero at these instants of time.

Thus we achieve the synchronization with the zero crossing instants of supply voltage.

Expression for frequency of relaxation oscillator :

The expression for the frequency of relaxation oscillator, is given by :

$$f = \frac{1}{T}$$

$$\text{But } T \approx T_1 \therefore f = \frac{1}{T_1} = \frac{1}{RC \log_e [1/(1-\eta)]} \quad \dots(1.14.3)$$

Design equations for UJT relaxation oscillator :

The important design equations for the UJT relaxation oscillator are as follows :

$$T = RC \log_e \left[\frac{1}{1-\eta} \right] \quad \dots(1.14.4)$$

$$f = \frac{1}{RC \log_e [1/(1-\eta)]} \quad \dots(1.14.5)$$

$$V_p = \eta V_{BB} + V_D \quad \dots(1.14.6)$$

From Fig. 1.14.11 it is clear that $\alpha = \omega T$.

$$\therefore \alpha = \omega RC \log_e \left[\frac{1}{1-\eta} \right] \quad \dots(1.14.7)$$

$$R_2 = \frac{10^4}{\eta V_{BB}}$$

- The maximum value of R,

$$R_{max} = \frac{V_{BB} - V_p}{I_p} \quad \dots(1.14.8)$$

- The minimum value of R,

$$R_{min} = \frac{V_{BB} - V_V}{I_V} \quad \dots(1.14.9)$$

Where V_p = Peak voltage of UJT

V_V = Valley point voltage of UJT.

I_p = Peak current

I_V = Valley point current

Features of UJT triggering circuit :

1. Firing angle can be changed from 0 to 180°.
2. Firing angle does not depend on supply (mains) voltage fluctuations.
3. Isolation between gate and anode circuits is provided.
4. It can be used for triggering more than one SCR at a time.
5. This circuit is synchronized with the ac mains.

Design example :

Ex. 1.14.1 : Design the triggering circuit for SCR using UJT. The UJT parameters are : $V_{BB} = 30V$, $\eta = 0.51$, $I_p = 10 \mu A$, $V_V = 3.5 V$, $I_V = 10 mA$ frequency of oscillations is 50 Hz, width of the trigger pulse 50 μS .

Soln. :

- The peak voltage,

$$V_p = \eta V_s + V_D \quad \dots(1)$$

$$\therefore V_p = (0.51 \times 30) + 0.7 = 16 V \quad \dots(2)$$

- The UJT will be triggered when the capacitor voltage $V_C = V_p = 16$ Volts. The capacitor will then discharge through the UJT and R_3 from V_p to V_V . The discharge time "T₂" should be equal to the gate pulse width i.e. 50 μ sec.

To calculate the value of R_1 :

\therefore Discharge equation is,

$$V_V = (V_p - V_D) e^{-T_2/R_1 C} \quad \dots(3)$$

- Assuming, $C = 0.1 \mu F$ and substituting other values,

$$3.5 = (16 - 0.7) e^{-T_2/0.1 \times 10^{-6} R_1}$$

$$\therefore \frac{-T_2}{0.1 \times 10^{-6} R_1} = -1.475$$

$$\text{But } T_2 = 50 \mu \text{ sec}$$



$$\therefore R_1 = \frac{50 \times 10^{-6}}{0.1 \times 10^{-6} \times 1.475}$$

$$= 338.96 \approx 339 \Omega \quad \dots \text{Ans.}$$

- R_1 should be higher than or equal to 339Ω . The preferred value in 10 % tolerance range is 390Ω .

To calculate the value of R :

- The expression for the total time is,

$$T = T_1 + T_2 \quad \dots(4)$$

$$\text{But } T = \frac{1}{f} = \frac{1}{50} = 20 \text{ ms}$$

$$\therefore T_1 = T - T_2 = (20 \times 10^{-3}) - (50 \times 10^{-6})$$

$$= 19.95 \text{ ms}$$

- The expression for T_1 is given by Equation (1.14.4) as :

$$T_1 = RC \log_e \left[\frac{1}{1-\eta} \right]$$

$$\therefore R = \frac{T_1}{C \log_e [1/(1-\eta)]}$$

$$= \frac{19.95 \times 10^{-3}}{0.1 \times 10^{-6} \log_e [1/(1-0.51)]}$$

$$= 279.66 \text{ k}\Omega \quad \dots \text{Ans.}$$

To verify if R is in the specified limits :

- The value of R should be between R_{\max} and R_{\min} specified by Equations (1.14.8) and (1.14.9) respectively.

$$\therefore R_{\max} = \frac{V_{BB} - V_P}{I_P} = \frac{30 - 16}{10 \times 10^{-6}} = 1.4 \text{ M}\Omega$$

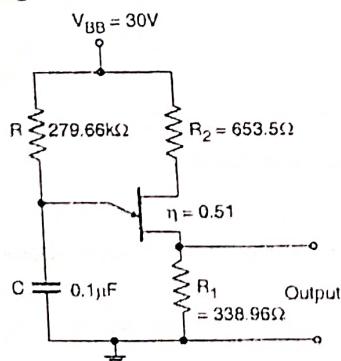
$$R_{\min} = \frac{V_{BB} - V_V}{I_V} = \frac{30 - 3.5}{10 \times 10^{-3}} = 2.65 \text{ k}\Omega$$

- Thus R is in the specified limits.

To calculate R_2 :

$$R_2 = \frac{10^4}{\eta V_{BB}} = \frac{10^4}{0.51 \times 30} = 653.5 \Omega \quad \dots \text{Ans.}$$

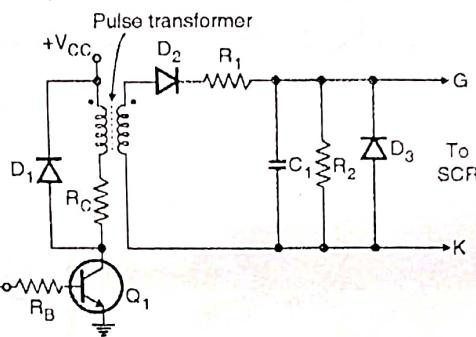
- This completes the design. The relaxation oscillator is as shown in Fig. P. 1.14.1.



(1-87) Fig. P. 1.14.1 : Final designed circuit

1.14.5 Pulse Amplifier Circuit :

- The triggering circuits discussed so far are very simple elementary circuits. In practice more sophisticated and complex triggering circuits using analog and digital ICs are used trigger SCRs connected in the converter, inverters or AC controllers.
- To avoid the loading of such control circuits, a pulse amplifier circuit is included between the low power IC triggering circuit and high power SCR.
- The pulse amplifier circuit is as shown in Fig. 1.14.12.



(1-92) Fig. 1.14.12 : Pulse amplifier circuit

- The functions of pulse amplifier circuit of Fig. 1.14.12 are as follows :

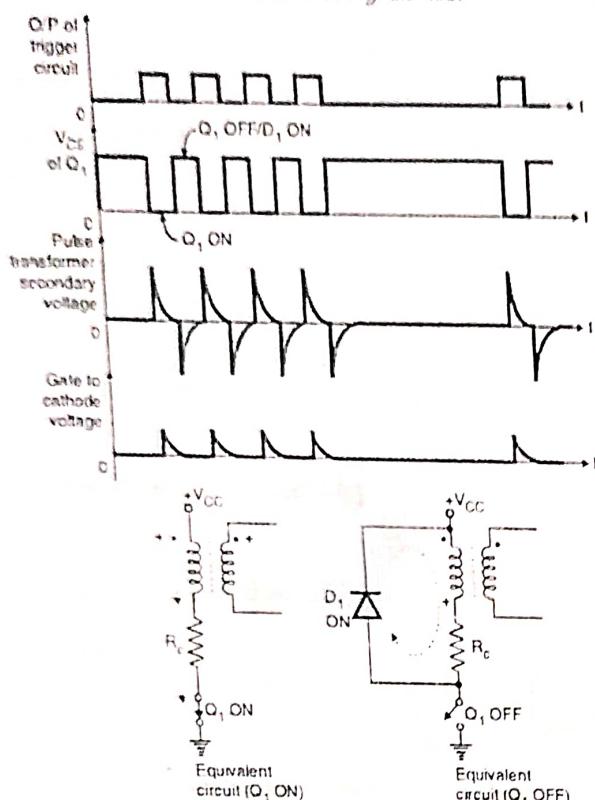
1. It amplifies the current to the required gate current level and avoids the loading of triggering circuit.
2. It provides isolation between the triggering circuit and SCR.

Operation :

- As soon as a trigger pulse is generated by the triggering circuit and applied to the base of transistor Q_1 , the transistor is turned on and goes into saturation (acts as a closed switch).
- The current starts flowing through the primary winding of the pulse transformer resistor R_C and Q_1 . The primary current is controlled by resistor R_C . Due to this current the voltage pulse is induced across the secondary winding of the pulse transformer.
- When the transistor Q_1 turns off, diode D_1 is forward biased due to self induced primary voltage. Freewheeling takes place through R_C and D_1 and the transistor is protected against damage due to excessive collector to emitter voltage.



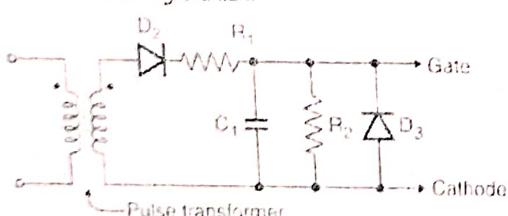
- The waveforms of pulse amplifying circuit and equivalent circuits are shown in Fig. 1.14.13.



(B-93) Fig. 1.14.13 : Waveforms and equivalent circuits of pulse amplifier

1.14.6 Gate Protection Circuit :

The protection circuit for gate cathode junction of SCR is as shown in Fig. 1.14.14.



(B-94) Fig. 1.14.14 : Gate protection circuit

Different components and their use is as follows :

- Pulse transformer :** It is used for coupling the gate triggering pulses to the gate magnetically. It isolates the low power triggering circuit from the high power anode circuit.
- R_1 is used to limit the gate current below its maximum allowable value.
- R_2 is connected to bypass the thermally generated leakage current. It helps to avoid undesired triggering of SCR at higher operating temperature.

- Diode D_2 :** This diode will allow only the positive pulses to pass through to the gate. This will avoid application of reverse voltage to the gate cathode junction.
- Diode D_3 :** This will protect the gate from the negative voltage that may get coupled from the anode side.
- Capacitor C_1 acts as a filter. It filters out any high frequency noise coupled to the gate terminal. This will avoid accidental triggering of SCR due to noise.

1.14.7 Comparison of Triggering Circuits :

Table 1.14.1 : Comparison of Triggering Circuits

Sr. No.	Parameter	R triggering	R-C triggering	UJT triggering
1.	Range of firing angle	0 to 90°	0 to 180°	0 to 180°
2.	Isolation of control circuit and power circuit.	Not included	Not included	Due to the use of pulse transformer isolation is provided.
3.	Firing of multiple SCRs	Not possible	Not possible	Possible due to pulse transformer (multiple secondary windings).
4.	Effect of supply fluctuations.	Value of α is not stable	Value of α is not stable	α remains stable
5.	Rating of triggering circuit components	Very high	Very high	Low
6.	Cost	Low	Cheap	Costlier than RC circuit
7.	Type of triggering	AC gate triggering	AC gate triggering	Pulsed triggering
8.	Synchronization with ac mains	Yes	Yes	Yes

1.14.8 Solved Examples :

Ex. 1.14.2 : A load of resistance 25Ω and inductance of 0.5 H is fed from dc supply of 90 V through a thyristor switch with latching current of 15 mA and fired by triggering pulse of $40 \mu\text{sec}$ duration. Find if the thyristor will turn on and operate.



Soln. :

Given : $R = 25 \Omega$, $L = 0.5 \text{ H}$, $V = 90 \text{ Volts}$, $I_L = 15 \text{ mA}$,

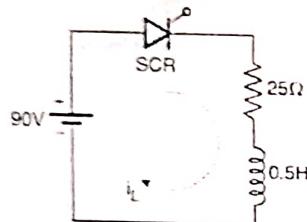
$$t = 40 \mu\text{sec}$$

- As soon as the SCR is turned on, the 90 V dc voltage gets connected across the RL load.
- The load current i_L starts increasing exponentially. The instantaneous load current is given by

$$i_L = I(1 - e^{-\frac{t}{RL}}) \quad \dots(1)$$

- where $I = V/R = 90/25 = 3.6 \text{ Amp}$, $t = 40 \mu\text{s}$, $R = 25\Omega$ and $L = 0.5 \text{ H}$
- Substituting these values in Equation (1), the load current 40 μs , after the application of gate pulse is equal to

$$\begin{aligned} i_L &= 3.6 [1 - e^{-\frac{40 \times 10^{-6}}{25 \times 0.5}}] = 3.6 [1 - 0.998] \\ &= 7.2 \times 10^{-3} = 7.2 \text{ mA} \end{aligned} \quad \dots(2)$$



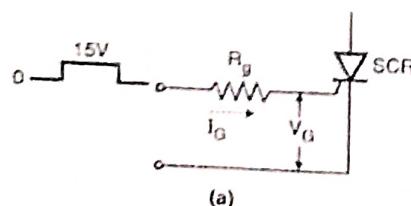
(a) Fig. P. 1.14.2

- In this way at the end of the gate triggering pulse of 40 μs duration, the load current and hence the anode current of SCR is only 7.2 mA which is less than its latching current (15 mA).
- Therefore SCR will not get latched into the on state and will turn off, as soon as the gate pulse extinguishes. Successful turn on hence will not be possible.

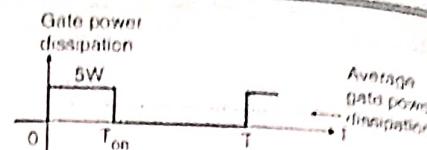
Ex. 1.14.3 : For SCR gate cathode characteristics is given by $V_g = 1 + 10 I_g$. Gate source voltage is a rectangular pulse of 15 V with 20 μsec duration for an average power dissipation of 0.3 Watts and peak gate drive power of 5 Watts. Calculate :

- Resistance to be connected in series with SCR gate
- Triggering frequency.
- Duty cycle of the triggering pulse. **(May, 11, 6 Marks)**

Soln. :



(a) Fig. P. 1.14.3(Contd...)



(b)

(I-96) Fig. P. 1.14.3

To calculate I_g :Given : $V_g = 1 + 10 I_g$

- As the gate pulse width is 20 μsec (less than 100 μsec) the dc data does not apply.
- If the gate pulse width has been more than 100 μsec , the relation $(1 + 10 I_g) = 0.3 \text{ W}$ will hold good. But as the data does not apply, we have

$$(1 + 10 I_g) I_g = 5 \text{ W}$$

$$\text{or } I_g + 10 I_g^2 - 5 = 0$$

$$\text{or } I_g = 0.659 \text{ Amp.}$$

∴ Amplitude of current pulse = 0.659 Amp. During the on time of the pulse

To calculate R_g :

$$V_{\text{trig.}} = V_g + I_g R_g$$

$$\therefore 15 = (1 + 10 I_g) + I_g R_g$$

$$\therefore R_g = 11.245 \text{ ohm.}$$

To calculate the duty cycle :

- Referring to Fig. P. 1.14.3(b) we can write that,

$$\text{Average gate power dissipation } P_{g(\text{av})} = \text{Duty cycle} \times P_{g(\text{pk})}$$

$$\therefore \text{Duty cycle, } D = \frac{P_{g(\text{av})}}{P_{g(\text{pk})}} = \frac{0.3}{5} \times 100\%$$

$$\therefore D = 6\% \quad \dots\text{Ans.}$$

To calculate triggering frequency :

$$\text{Duty cycle } D = \frac{T_{\text{on}}}{T} = 0.06$$

$$\therefore T = \frac{T_{\text{on}}}{0.06} = \frac{20 \mu\text{s}}{0.06} = 333.33 \mu\text{s}$$

$$\therefore \text{Triggering frequency } f = \frac{1}{T} = \frac{1}{333.33 \times 10^{-6}} \text{ Hz}$$

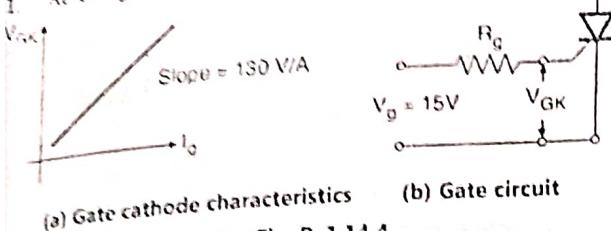
$$\therefore f = 3 \text{ kHz} \quad \dots\text{Ans.}$$

Ex. 1.14.4 : For SCR, the gate cathode characteristics has a straight line slope of 130 Volts per ampere. For a trigger voltage source of 15 Volts and allowable gate power dissipation of 0.5 Watts calculate the gate source resistance.

Dec. 10, Dec. 13, 6 Marks; Feb. 16, 4 Marks

Soln.:

1. Refer Figs. P. 1.14.4(a) and (b).



From Fig. P. 1.14.4(b), we can write,

$$V_g = I_g R_g + V_{GK} \quad \dots(1)$$

When SCR turns on, $V_{GK} = 0.7\text{ V}$

$$\begin{aligned} 15 &= I_g R_g + 0.7 \\ I_g R_g &= 14.3 \text{ V} \end{aligned} \quad \dots(2)$$

Gate power dissipation $P_g = I_g V_{GK}$

$$\begin{aligned} 0.5 &= I_g \times 0.7 \\ I_g &= 0.7142 \text{ A} \end{aligned} \quad \dots(3)$$

Substituting this value of I_g into Equation (2) we get,

$$\begin{aligned} 0.7142 R_g &= 14.3 \\ R_g &= 20 \Omega \end{aligned} \quad \dots\text{Ans.}$$

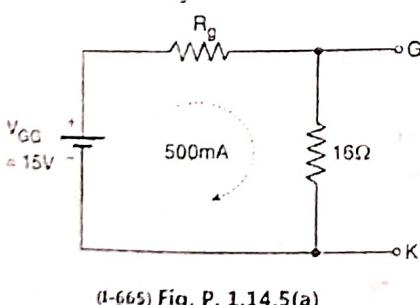
x. 1.14.5 : For a SCR the gate cathode characteristics is given by a straight line with a gradient of 16 Volts/Ampere passing through the origin. The maximum turn-on time is μs and the minimum gate current required to obtain this quick turn-on is 500 mA. If the gate source voltage is 15 V.

- i) Calculate the resistance to be connected in series with SCR gate.
 - ii) Compute the gate power dissipation, given that pulse width is equal to the turn-on time and average gate power dissipation is 0.3 W. Also compute the maximum triggering frequency that will be possible when pulse firing is used
- Dec. 09, 6 Marks; May 12, 10 Marks!**

Soln.:

Resistance in series with SCR gate :

The gradient of gate cathode is 16 V/A. Hence the gate cathode resistance is $R_{gk} = 16 \Omega$.



- Applying the KVL to the circuit shown in Fig. P. 1.14.5(a) we get,

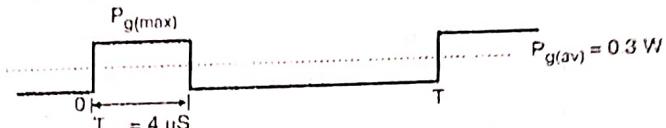
$$V_{GG} = I_g(R_g + 16)$$

$$\therefore \frac{15}{0.5} = R_g + 16$$

$$\therefore R_g = 14\Omega$$

...Ans.

- (b) Gate power dissipation :



- The maximum gate power dissipation,

$$\begin{aligned} P_{g(\max)} &= I_g^2 R_{gk} = (0.5)^2 \times 16 \\ &= 4 \text{ Watts} \end{aligned} \quad \dots\text{Ans.}$$

- (c) To calculate frequency :

- Refer Fig. P. 1.14.5(b). The average power dissipation is given by,

$$P_{g(\text{av})} = \text{Duty cycle} \times P_{g(\max)}$$

$$\therefore 0.3 = D \times 4$$

$$\therefore D = 0.3/4 = 0.075 \text{ or } 7.5\%$$

∴ One cycle period is given by $T = \frac{T_{on}}{D}$

$$\therefore T = \frac{4 \mu\text{s}}{0.075} = 53.33 \mu\text{s}$$

$$\therefore \text{Frequency } f = \frac{1}{T} = \frac{1}{53.33 \times 10^{-6}}$$

$$\therefore f = 18.750 \text{ kHz} \quad \dots\text{Ans.}$$

Ex. 1.14.6 : Latching current for a SCR inserted between a DC voltage source of 200 V and the load is 100 mA. Compute the minimum pulse width of the gate pulse current required to turn on this SCR in case the load consists of :

- (a) $L = 0.2 \text{ H}$ (b) $R = 20 \Omega$ in series with $L = 0.2 \text{ H}$.

Soln. :

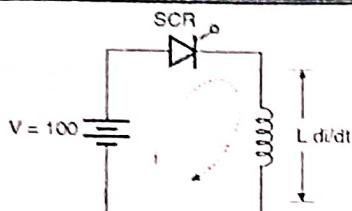
Part (a) :

Given : $V = 200\text{V}$, $I_{\text{latch}} = 100 \text{ mA}$, $L = 0.2\text{H}$.

- From the Fig. P. 1.14.6(a), as soon as the SCR turns on, voltage across the inductance is equal to 200 V.

$$\therefore L \frac{di}{dt} = 200 \quad \dots(1)$$

$$\therefore \frac{di}{dt} = \frac{200}{0.2} = 1000 \text{ Amp./sec.} \quad \dots(2)$$



(I-105) Fig. P. 1.14.6(a)

- The current through SCR will be equal to the latching current value $I_{latch} = 100 \text{ mA}$ when

$$di = 100 \text{ mA}$$

$$\therefore \text{From Equation (2), } \frac{100 \times 10^{-3}}{dt} = 1000$$

$$\therefore dt = \frac{100 \times 10^{-3}}{1000} = 100 \mu\text{s} \quad \dots \text{Ans.}$$

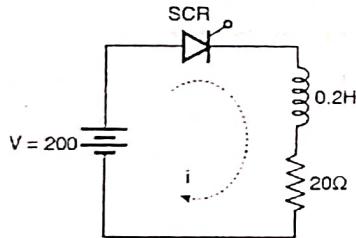
- Thus the minimum pulse width required to turn on the SCR is $100 \mu\text{s}$.

Part (b) :

Given : $V = 200 \text{ V}$, $I_{latch} = 100 \text{ mA}$, $L = 0.2 \text{ H}$, $R = 20 \Omega$

- Refer to Fig. P. 1.14.6(b). The instantaneous SCR current is given by,

$$i = \frac{V}{R} [1 - e^{-tR/L}] \quad \dots (3)$$



(I-106) Fig. P. 1.14.6(b)

- Let "t" be the minimum pulse width then for $i = I_{latch} = 100 \text{ mA}$. Equation (3) becomes,

$$100 \times 10^{-3} = \frac{200}{20} [1 - e^{-t \times 20/0.2}]$$

$$\therefore 1 \times 10^{-3} = 1 - e^{-100t}$$

$$\therefore e^{-100t} = 0.999 \therefore -100t = -1.0005 \times 10^{-3}$$

$$\therefore t = 10 \mu\text{s} \quad \dots \text{Ans.}$$

- The minimum width of gate pulse is $10 \mu\text{s}$.

Ex. 1.14.7 : Design the triggering circuit for SCR using UJT. The UJT parameters are, $V_S = 30 \text{ V}$, $\eta = 0.51$, $I_P = 10 \mu\text{A}$, $V_V = 3.5 \text{ V}$, $I_V = 10 \text{ mA}$ frequency of oscillations is 50 Hz , width of the trigger pulse $50 \mu\text{s}$.

Soln. :

- The peak voltage,

$$V_P = \eta V_S + V_D \quad \dots (1)$$

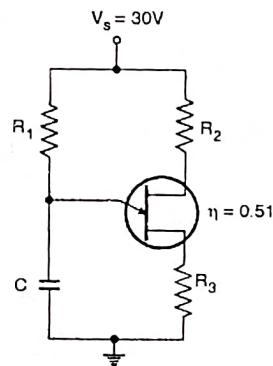
$$\therefore V_P = (0.51 \times 30) + 0.7 = 16 \text{ V} \quad \dots (2)$$

- The UJT will be triggered when the capacitor voltage $V_C = V_P = 16 \text{ Volts}$. The capacitor will then discharge through the UJT and R_3 from V_P to V_V . The discharge time " t_2 " should be equal to the gate pulse width i.e. $50 \mu\text{s}$.

∴ Discharge equation is

$$V_V = (V_P - V_D) e^{-t_2/R_3 C} \quad \dots (3)$$

Assuming $C = 0.1 \mu\text{F}$ and substituting other values,



(I-107) Fig. P. 1.14.7 : UJT relaxation oscillator

$$3.5 = (16 - 0.7) e^{-t_2/0.1 \times 10^{-6} R_3}$$

$$\therefore \frac{-t_2}{0.1 \times 10^{-6} R_3} = -1.475$$

$$R_3 = \frac{50 \times 10^{-6}}{0.1 \times 10^{-6} \times 1.475}$$

$$R_3 = 338.96 \approx 339 \Omega \quad \dots \text{Ans.}$$

- R_3 should be higher than or equal to 339Ω . The preferred value in 10% tolerance range is 390Ω .
- The charging of C takes place through R_1 . V_C varies between V_V and V_P and the charging time is " t_1 ".

$$\text{But } t_1 + t_2 = T = \frac{1}{f} \quad \dots (4)$$

$$\therefore t_1 + t_2 = \frac{1}{50} = 20 \text{ msec.}$$

$$\therefore t_1 = 20 \text{ ms} - 50 \mu\text{s} = 19.95 \text{ ms}$$

- The charging equation for C is

$$V_P = V_V + V_S (1 - e^{-t_1/R_1 C})$$

$$\therefore V_P - V_V = V_S (1 - e^{-t_1/R_1 C})$$

$$16 - 3.5 = 30 [1 - e^{-19.95 \times 10^{-6} / R_1 \times 0.1 \times 10^{-6}}]$$

$$0.4166 = \frac{1 - e^{-\frac{199500}{R_2}}}{1 - e^{-\frac{199500}{R_1}}}$$

$$0.5389 = \frac{1 - e^{-\frac{199500}{R_1}}}{1 - e^{-\frac{199500}{R_2}}}$$

$$\therefore R_2 = 370.132 \Omega \text{ or } 370.132 \text{ k}\Omega$$

The value of $R_2 = \frac{10^4}{2V_S}$

$$\therefore R_2 = \frac{10^4}{0.31 \times 30} \approx 653.5 \Omega$$

$$R_1 = 370.132 \Omega$$

$$R_2 = 653.5 \Omega$$

$$R_3 = 339 \Omega$$

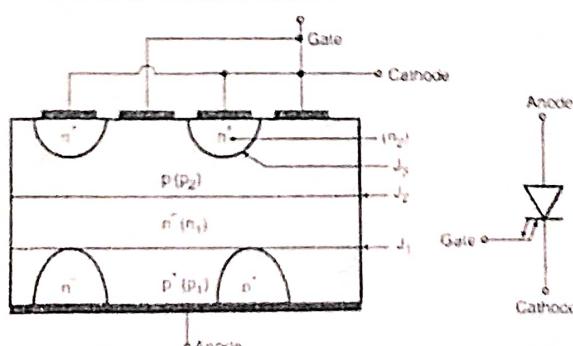
and $C = 0.1 \mu F/40 \text{ Volts.}$...Ans.

1.15 Gate Turn Off (GTO) Thyristor :

- SCRs have the largest current carrying capacity (several thousand amp) and they can block very high voltages (several thousand volts).
- But the major disadvantage of them is that once they are turned on, the gate will not have any control on their operation. SCRs once start conducting can be turned off by using external turn off circuits known as the commutation circuits.
- Therefore a new type of SCR called gate turn off (GTO) SCR is developed which can be turned off by using a negative gate current pulse.

1.15.1 Construction of GTO :

- The basic structure of the GTO is as shown in Fig. 1.15.1(a). As seen from the Fig. 1.15.1(a) it is basically a four layer structure similar to a conventional SCR.
- Fig 1.15.1(b) shows the circuit symbol for the GTO. As seen from the Fig 1.15.1(b) GTO is a three terminal device. Gate is control terminal.



(1.59) Fig. 1.15.1

Note the two arrows marked on the gate terminal. They indicate that the gate current for GTO can be either positive or negative. (Whereas in SCR the gate current is only positive).

Difference between GTO and SCR :

- There are a few significant differences between GTO and a conventional SCR.
- They are as follows :
 1. The gate and cathode structures of GTO are highly interdigitated as compared to those in SCRs with various types of geometrical forms.
 2. The cathode areas are usually formed by etching away the silicon surrounding the cathodes so that they appear as islands as shown in Fig. 1.15.1(a). At the time of packaging the cathode islands are directly connected to a metal heat sink. The cathode connection to the outside world is made with this metal heat sink directly.
 3. The third major corresponds to the anode region of GTO. (See Fig. 1.15.1(a)). In the P-type anode layer (P_1 layer) the n^+ regions penetrate at regular intervals. These n^+ regions make contact with the n^- region i.e. the base layer n_2 . This results in the so called "Shorted Anode Structure" of GTO.

1.15.2 Operating Principle of GTO :

- The turn on mechanism of GTO is exactly same as that of a conventional SCR. The dependence of GTO's break over voltage on the magnitude of gate current is also same as that of SCR.
- In short the working principle of GTO at the time of turn on and in the on state is same as that of SCR.
- However the operation at the time of turn off is entirely different. In order to turn off a conducting GTO, we have to apply a negative gate current pulse at the gate terminal.

1.15.3 GTO Turn off Mechanism :

- The basic operation of GTO is same as that of the conventional SCR.
 - But the major difference between them is that the conducting GTO can be turned off by applying a negative gate current to it. Thus a positive gate current turns it on and negative gate current turns it off.
- Refer to the equivalent circuit shown in Fig. 1.15.2

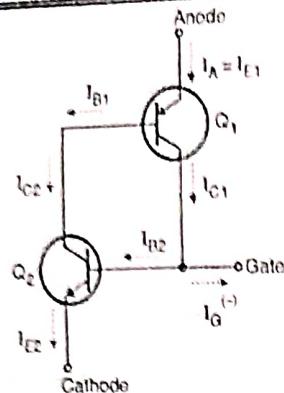


Fig. 1.15.2 : Two transistor model of GTO

- Both the transistors Q_1 and Q_2 are in saturation when the GTO is in its on state.
- However if the base current of Q_2 is briefly made less than the value needed for maintaining it in saturation, then Q_2 will come out of saturation and enter into its active state, this will reduce the regeneration and GTO will begin to turn off.
- In order to reduce the base current of Q_2 , a negative gate current $I_G^{(-)}$ must flow in the direction as shown in Fig. 1.15.2.
- It can be proved that the negative gate current required for turning off a conducting GTO is given by,

$$I_G^{(-)} > \frac{I_A}{\beta_{OFF}} \quad \dots(1.15.1)$$

Where $\beta_{OFF} = \frac{\alpha_2}{(\alpha_1 + \alpha_2 - 1)}$... (1.15.2)

- The parameter β_{OFF} is known as the **turn off gain**.
- Equation (1.15.1) clearly indicates that to turn off the GTO, a negative current $I_G^{(-)}$ must flow which is greater than the anode current divided by the turn off gain.

1.15.4 Magnitude of $I_G^{(-)}$ for Reliable Turn Off :

- From Equation (1.15.1) it is clear that the magnitude of $I_G^{(-)}$ for reliable turn off depends on the value of turn off gain β_{OFF} .
- Higher values of the turn off gain will reduce the required value of $I_G^{(-)}$.
- α_1 and α_2 are the transportation factors of the two transistors Q_1 and Q_2 and their values are always between 0 and 1. Therefore the practical values β_{OFF} will be between 3 to 5.

If β_{OFF} is between 3 to 5, then the magnitude of $I_G^{(-)}$ the negative gate current required for reliable turn off will be greater than $I_A / 3$ or $I_A / 5$.

- If the anode current $I_A \approx 600$ amp then $I_G^{(-)} > 200$ Amp or $I_G^{(-)} > 120$ Amp which is very high and the cost of the turn off circuit should be too high.
- If the actual negative current is not high enough then commutation failure will result i.e. GTO cannot be turned off. This is the biggest drawback of GTO.

Maximum controllable anode current :

- For a GTO, a maximum value of controllable anode current is defined. If the anode current is higher than this value then no gate current can turn off the conducting GTO.
- If we try to turn off a GTO with an anode current higher than the maximum controllable value then it will be damaged.

1.15.5 Static I-V Characteristics of GTO :

- The I-V characteristics of a GTO in the forward direction is same as that of the conventional SCR however in the reverse direction, the GTO breaks down at very low voltage.
- The reverse breakdown voltage is of the order of 20 to 30 V only.

GTO equivalent circuit :

- The equivalent circuit of GTO is same as that of the conventional SCR.
- The turn on mechanism is also same as that of the conventional SCR.

On State Characteristics :

- In the on-state, the GTO operates in a similar manner to the SCR.
- If the anode current remains above the holding current level then positive gate drive may be reduced to zero and the GTO will remain in conduction.
- However, as a result of the turn-off ability of the GTO, it has a higher holding current level than the standard SCR and, in addition, the cathode of the GTO is subdivided into small finger elements to assist turn-off.
- Thus, if the GTO anode current transiently dips below the holding current level, localized regions of the device may turn off, thus forcing a high anode current back into the GTO at a high rate of rise of anode current after this partial turn off.

- This situation could be potentially destructive.
- Therefore, it is recommended that the positive gate drive not be removed during conduction but held at a value I_{GON} where, I_{GON} is greater than the maximum critical trigger current (I_{GT}) over the expected operating temperature range of the GTO.

Off State Characteristics :

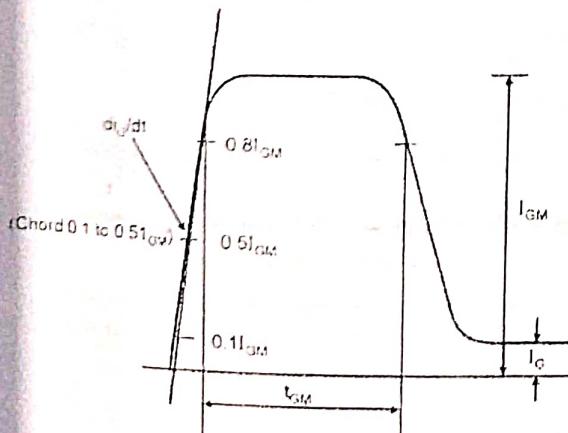
- Unlike the standard SCR, the GTO does not include cathode emitter shorts to prevent non-gated turn-on effects due to dv/dt -induced forward-biased leakage current.
- In the off-state of the GTO, steps should therefore be taken to prevent such potentially dangerous triggering.
- This can be accomplished by either connecting the recommended value of resistance between gate and cathode (R_{GK}) or maintaining a small reverse bias on the gate contact ($V_{RG} = 2$ V).
- This will prevent the cathode emitter from becoming forward-biased and will therefore sustain the GTO in the off state.

1.15.6 Switching Phases of GTO :

- The switching process of a GTO goes through four operating phases :
 1. turn-on
 2. on-state
 3. turn-off and
 4. off-state.

1. Turn on :

- A GTO has a highly interdigitized gate structure with no regenerative gate. Thus, it requires a large initial gate trigger pulse.
- A typical turn-on gate pulse and its important parameters are shown in Fig. 1.15.2(a).



(G-2960) Fig. 1.15.2(a) : Typical turn-on pulse of a GTO

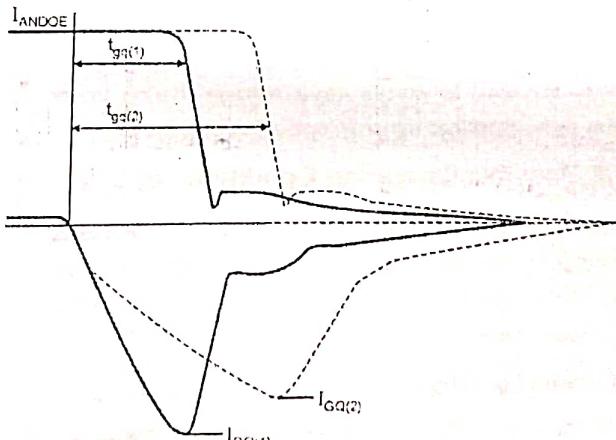
- Minimum and maximum values of I_{GM} can be derived from the device data sheet. A value of $dI_g = dt$ positioned against turn-on time is given under the device characteristics found on the data sheet.
- The rate of rise of gate current $dI_g = dt$ will affect the device turn-on losses. The duration of the I_{GM} pulse should not be less than half the minimum forward current given in data sheet ratings.

2. On-state :

- Once the GTO is turned on, forward gate current must be continued for the entire conduction period. Otherwise, the device will not remain in conduction during the on state period.

3. Turn off :

- The turn-off performance of a GTO is greatly influenced by the characteristics of the gate turn-off circuit.
- Thus the characteristics of the turn-off circuit must match with the de-icing requirements.
- Fig. 1.15.2(b) shows the typical anode and gate currents during the turn-off. The gate turn-off process involves the extraction of the gate charge, the gate avalanche period, and the anode current decay.



(G-2961) Fig. 1.15.2(b) : Anode and gate currents during turn-off

- The amount of charge extraction is a device parameter and its value is not affected significantly by the external circuit conditions.
- The initial peak turn-off current and turn-off time, which are important parameters of the turning-off process, depend on the external circuit components.
- The device data sheet gives typical values for I_{GA} .



4. Off state :

- During the off-state period, which begins after the fall of the tail current to zero, the gate should ideally remain reverse-biased.
- This reverse bias ensures maximum blocking capability and dv/dt rejection.

1.15.7 Important Characteristics of GTO :

- Some of the important characteristics of GTO are :
 1. Higher forward gate current :
 2. Less turn off time : - The forward (positive) gate current required to turn on a GTO is much higher than that of a conventional SCR of identical ratings.
- The turn on time of GTO (typically 1 μ s) is similar to that of a conventional SCR but the turn off time of GTO is much less (typically 1 μ s) than the turn off time of a conventional SCR (typically 5 to 30 μ s). Thus GTO can be used at a much higher switching frequency.

1.15.8 Important Ratings of GTO :

Sr. No.	Description	Value
1.	On-state voltage (V_T)	3.4 V
2.	Turn on time	1 μ s
3.	Turn off time	5 to 30 μ s
4.	Turn off gain	3 to 5
5.	Turn on gain	600

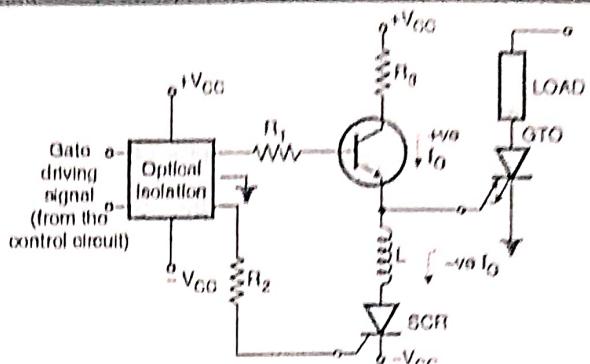
1.15.9 Drive Circuit Requirements :

- The requirements of the gate driving circuit for GTO are as follows :
 1. The positive gate current pulse required to be applied at the time of turn on should be large enough, so that the turn on is reliable and fast.
 2. The negative gate current should be large enough to ensure reliable turn off of GTO.
 3. The power and control circuits should be isolated from each other.

1.15.10 Drive Circuit for GTO :

Circuit diagram :

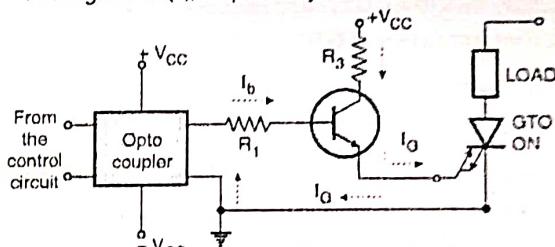
- The circuit diagram of gate drive circuit for a GTO is as shown in Fig. 1.15.3(a). It fulfills all the requirements of GTO driving circuit.



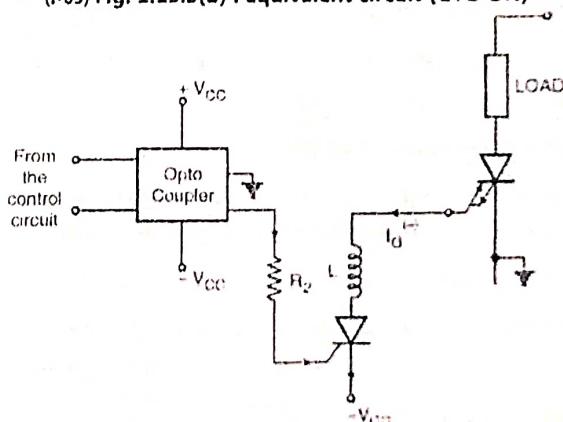
(I-62) Fig. 1.15.3(a) : Gate drive circuit for GTO

Operation :

- For successful turn off, the magnitude of negative gate current should be large. This current is supposed to flow for a short time.
- Therefore devices like SCR or MOSFET can be used to turn off the GTO. The turn on current requirement is less, therefore the BJT can be used.
- The inductance L is added in the turn off path to improve the turn off performance.
- The equivalent circuits for the two different operating conditions of the circuit are as shown in Fig. 1.15.3(b) and Fig. 1.15.3(c), respectively.



(I-63) Fig. 1.15.3(b) : Equivalent circuit (GTO ON)



(I-64(a)) Fig. 1.15.3(c) : Equivalent circuit (GTO OFF)

- Note the ground connection in Fig. 1.15.3(b). A separate power supply is used to generate the +Vcc and -Vcc supplies used for the driver and optical isolator.



1.15.11 Advantages of GTO over SCR :

1. No commutation circuit required to turn off the GTO. Hence reduction in size, weight and cost.
2. As the commutation inductors are not used, the associated audible noise and electromagnetic noise are absent.
3. GTOs can be used at higher switching frequencies than SCRs.
4. Efficiency of converters using GTO is better than that using conventional SCRs.

1.15.12 Advantages of GTO over BJT :

- GTOs are used in the low-power applications. In such applications GTOs have the following advantages over BJT :
 1. GTO has a higher forward blocking voltage capacity.
 2. On state gain is high (typically 600). On state gain is defined as the ratio of anode current to gate current.
 3. GTO needs only a short duration pulse to turn on while a BJT needs continuous base current.

1.15.13 Difference between Gating Characteristics of GTO and SCR :

Gating characteristics of GTO :

- GTO needs a short positive gate current pulse for turning on. It has a high turn on gain.
- A negative gate current of large magnitude is required to turn off the GTO.
- The turn off gain β_{off} of GTO is small, hence magnitude of negative I_G is large.
- In GTO, the gate has full control over the turn on and turn off process of the device.

Gating characteristics of an SCR :

- A short positive gate current pulse is required to turn on a SCR. But once turned on, the gate loses its control.
- SCR needs a forced commutation circuit to turn it off.
- To reduce the gate power dissipation pulsed triggering is preferred, over the continuous dc current triggering.

1.15.14 Applications of GTO :

1. Inverters
2. Uninterruptable power supplies (UPS)
3. DC motor drives

1.16 Comparison of GTO and SCR :

Table 1.16.1: Comparison of GTO and SCR

Sr. No.	Parameter	SCR	GTO
1.	Symbol :		
2.	Number of terminals	3	3
3.	Unidirectional / Bidirectional	Unidirectional	Unidirectional
4.	Controlled / Uncontrolled	Only turn on is controlled by the gate.	Turn on and turn off both are controlled by gate.
5.	Gate current	I_g can only be positive.	I_g can be positive or negative.
6.	Commutation circuit	Required	Not required.
7.	Gate-cathode structure	Not highly interdigitated.	Very highly interdigitated.
8.	Shorted anode structure	Not used.	Used.
9.	Value of I_G for turning on the device	Small	Large.
10.	Turn off time	5 to 30 μs	1 μs
11.	Switching frequency	Low	Higher than SCRs.
12.	Efficiency	Low	High.
13.	Applications	Controlled rectifiers, inverters, choppers, DC motor control.	Inverters, UPS, DC motor drives.

1.17 Importance of Series and Parallel Operation of SCRs :

- Before we understand about how to connect different power devices in series or parallel, we should know when to connect them so.
- Under one of the following circumstances the devices will have to be connected in series or parallel :
 1. When the total voltage to be handled is higher than the voltage rating of the individual devices, then the devices should be connected in series (example: HVDC system).



2. When the total current to be handled is higher than the current rating of the individual devices, then the devices should be connected in parallel.
3. The power devices with high voltage and current rating are very costly. Therefore instead of using a single high power device, it is always economical to use many low power devices in series or parallel.
4. High power devices are not easily available. Therefore it is better to connect many low power devices in series or parallel. This has an added advantage that if any of the devices connected in the series / parallel string becomes faulty, it is possible to replace it easily.

1.17.1 Series Connection of SCRs :

- In the applications like HVDC, the voltage to be handled is of the order few tens of kilovolts. We need to connect SCRs having lower voltage ratings in series with each other to withstand this voltage successfully.
- It is very important to ensure equal voltage sharing across the series connected SCRs. Why ? Because otherwise the voltage across an individual SCR can become higher than its rated voltage.
- This may damage that particular SCR. Therefore to avoid this, external circuit called "equalizing circuits" are required to be used to ensure equal voltage sharing.
- The equalizing circuits are of two types : static and dynamic.
- They are used to ensure equal voltage sharing under the static as well as dynamic operating conditions.

1.17.2 Possible Operating Conditions of SCR :

- The SCR can operate in any one of the following operating conditions. It is important to note that under all these operating conditions we must ensure equal voltage sharing.

 1. Forward blocking :
 - All the SCRs in the series string are forward biased, but they are not conducting. Therefore voltage across each SCR is positive and high.
 2. Reverse blocking :
 - All the SCRs are reverse biased and they are not conducting. Therefore voltage across each SCR is high and negative.
 - Under these two operating conditions, as the voltage across the SCRs is high, voltage equalization is a must.

The equalizing circuit used for these two conditions is "**STATIC EQUALIZING CIRCUIT**".

3. Partially turn on :

 - When the SCRs are in the transition state i.e. they are coming into conduction from the off state.
 - 4. Partially turn off (reverse recovery) :

 - When the SCRs are being turned off i.e. they are in transition state. Under these operating conditions the voltages across the SCRs are high.
 - Therefore voltage equalization is necessary. The equalizing circuit used for these two operating conditions is "**DYNAMIC EQUALIZING CIRCUIT**".

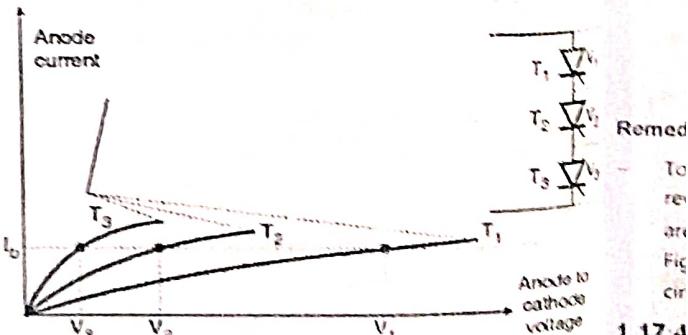
5. Forward conduction :

 - When all the SCRs are fully ON and carrying a forward current.
 - 6. Reverse conduction :

 - Under these two operating conditions, the voltage drop across the conducting SCRs is very small. Therefore unequal voltage sharing does not matter much. Therefore the equalizing circuit is not required for these two operating conditions.

1.17.3 Unequal Voltage Sharing in the Blocking State :

- The reason for unequal voltage sharing in the blocking state can be explained by using the characteristics shown in Fig. 1.17.1(a). Three thyristors are connected in series.



(1-1194) Fig. 1.17.1(a) : I - V characteristics of series connected thyristors

- See carefully the I - V characteristics of the series connected thyristors. All the thyristors are of identical batch number.
- However their characteristics are slightly different from each other.



Concentrate on that part of the characteristics where the thyristors are not conducting.

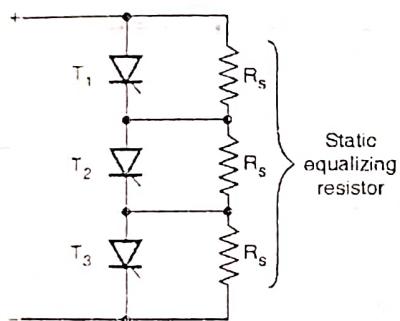
In this region the current through all the thyristors is the same, equal to I_b , the blocking current, but due to unequal "BLOCKING RESISTANCES" offered by the thyristors, the voltage drops across them are different. ($V_1 \neq V_2 \neq V_3$) from each other.

The blocking resistance is the resistance offered by the thyristor in the OFF state.

Similarly unequal voltage sharing will take place in the reverse blocking state as well.

Thus the cause behind unequal voltage sharing in the forward or reverse blocking state is unequal blocking resistances.

- This unequal voltage sharing is dangerous because the voltage appearing across the thyristor having the highest value of blocking resistance will be maximum (voltage V_1 in Fig. 1.17.1(a)).
- If this voltage is higher than its blocking capacity, then it will break down, which in turn will break down the whole series string.



(I-1195) Fig. 1.17.1(b) : Static equalizing circuit

Remedy :

- To have equal voltage sharing, under the forward and reverse blocking conditions, equal value resistances (R_s) are connected across thyristors as shown in Fig 1.17.1(b). This circuit is known as "static equalizing circuit".

1.17.4 Unequal Voltage Sharing during the Transition State :

- The static equalizing circuit cannot equalize the voltage across thyristors when they are being turned on or turned off. (Partially ON or partially OFF).

In the partially on and partially off states unbalanced transient voltage sharing will take place.

Unequal voltage sharing during turn on :

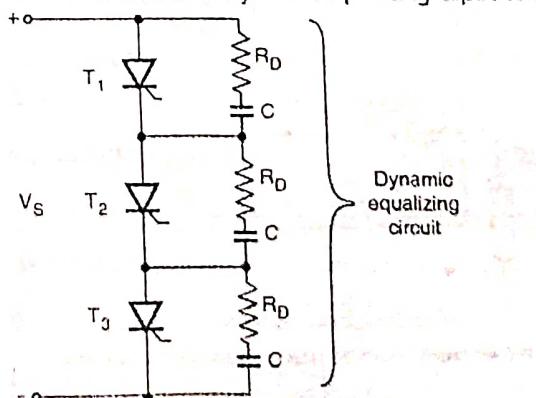
- At the time of turn on, ideally speaking all the thyristors should turn on simultaneously but practically the turn on delays of all the thyristors will not be identical. They will have different values.
- Some thyristors will be slow (longer turn on delay) and some of them will be fast (short turn on delay).
- Now what will be the effect of this ? Under the worst operating condition one thyristor is the slowest and all others are fastest.
- Then the slowest thyristors will come into conduction at the end (after all the other thyristors have come into conduction) and therefore full voltage will appear across it which may damage it.

Unequal voltage sharing during turn off :

- Similarly at the time of turn off, all the thyristors will not recover (turn off) at the same time. This happens due to unequal turn off delays of thyristors.
- Under the worst operating condition one thyristor is the fastest (recovers or turn off faster) and all the other thyristors are the slowest (recover slowly or turn off slowly).
- Then the fastest thyristor will turn off first and will have to bear the full voltage across it, which may damage it.

Remedy :

- In order to equalize the voltage sharing under the transient operating conditions we will have to connect a capacitor across each thyristor as shown in Fig. 1.17.2.
- Connection of the capacitor will slow down the rate of change of voltage across each thyristor. This will ensure that the fastest or slowest thyristor will not have to bear the full voltage across it under the transient operating conditions.
- Capacitor 'C' is known as dynamic equalizing capacitor.



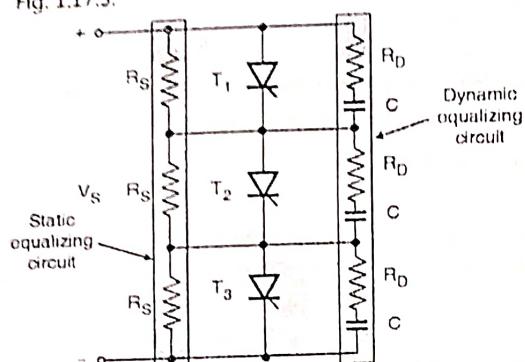
(I-1197) Fig. 1.17.2 : Dynamic equalizing circuit

Damping resistance R_D :

- The capacitors will charge when the thyristors are in the off state. Therefore as soon as the thyristors are turned on these capacitors will discharge through them.
- This discharge current must be limited to a safe value by connecting a damping resistance R_D in series with the capacitor as shown in Fig. 1.17.2.

The complete equalizing circuit :

- The complete equalizing circuit consists of the static as well as dynamic equalizing circuits as shown in Fig. 1.17.3.



(a-1198) Fig. 1.17.3 : Complete equalizing circuit

String Efficiency for Series Connection :

- The string efficiency for a series string is defined as :
- $$\eta = \frac{V_S}{n_s V_D} \quad \dots(1.17.1)$$
- Where V_S is the total applied voltage to a series string, n_s is the number of devices connected in series and V_D is voltage rating of the individual SCR.
 - Ideally the value of " η " should be 1 or 100%. But if $\eta = 100\%$ then each SCR will operate at its maximum rated voltage continuously (V_D).
 - Thus if $\eta = 100\%$ the possibility of device damage increases and the reliability of the string decreases.

Derating of the devices and reliability :

- Therefore in order to improve the reliability, the devices should be operated at lower voltage than their maximum rated voltage. This is called as "Derating" of the device.
- More the derating is, better will be the reliability. So in order to derate the devices we will have to add an extra device in the series string.

- The percent derating for the series connection is given by,

$$D_S = (1 - \eta) \times 100 \% \quad \dots(1.17.2)$$

- Derating increases the reliability of the series string.

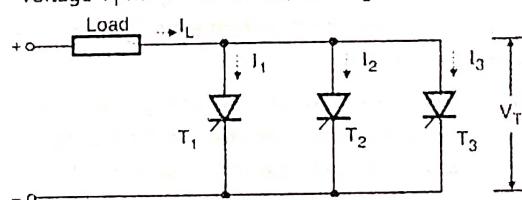
1.17.5 Parallel Operation of Thyristors :

- If the total load current to be handled is higher than the current rating of individual thyristor then the power devices are connected in parallel with each other.
- The current sharing must be properly done while connecting the devices in parallel, otherwise due to unequal current sharing, the device which draws more current will be damaged.
- Therefore by using external equalizing components, proper current sharing must be ensured. Before we find the remedy we must know the causes or reasons behind the unequal current sharing.

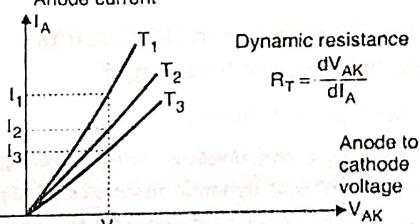
1.17.6 Causes for the Unbalance in Current Sharing :

(a) Effect of unequal dynamic resistance :

- The direct paralleling of the devices in this manner will lead to certain problems. The I-V characteristics in the on state of the three thyristors, connected in the parallel string are as shown in Fig. 1.17.4(a).
- It shows that the DYNAMIC RESISTANCE R_T of the thyristors (reciprocal of the slope of the characteristics in ON region of thyristors) are not equal.
- Due to unequal dynamic resistances, the current through the devices in the on state at the same terminal voltage V_T will be different (refer Fig. 1.17.4(b)).



(a) Parallel connection of thyristors
Anode current



(b) I-V characteristics in the ON state

(a-1200) Fig. 1.17.4



- The total load current $I_L = I_1 + I_2 + I_3$. From the Fig. 1.17.4(b), I_3 is the highest current and I_1 the lowest. Thus unequal current sharing takes place due to unequal on state resistances of the thyristors.

(b) Effect of unequal current sharing : (Thermal runaway)

- Due to unequal dynamic resistances, the currents through the thyristors are unequal. T_1 which has the lowest dynamic resistance draws the highest current (refer Fig. 1.17.4(b)).
- Due to this current flowing through T_1 , its junction temperature increases. This increase in junction temperature reduces the dynamic resistance of T_1 further.
- This in turn increases the current through it which will increase the junction temperature further and reduce the dynamic resistance still further.
- This process becomes cumulative and increases the current through T_1 to such an extent that it will be damaged. This phenomenon is known as **Thermal runaway**.
- In order to avoid the thermal runaway all, the thyristors operating in parallel must be operated at the same temperature by mounting them on a common heat sink.

(c) Unequal current sharing during turn on and turn off :

- Even though the devices connected in parallel are of the same make and identification number, they differ in turn on and turn off delays.
- During turn on, the fastest device (with minimum turn on time) will be turned on first and it will have to carry the entire load current till the other thyristor turn on completely.
- Similarly while switching off the string, the slowest device (with maximum turn off time) will be the last one to recover and has to carry the entire load current.
- Dynamic equalizing circuits must be used to force proper current sharing.

1.17.7 Current Sharing in DC Circuits (Static Current Sharing) :

(a) Proportional current sharing :

- In the dc circuits, the unequal current sharing takes place due to unequal dynamic resistance of thyristors and it can be compensated by connecting a resistance R_p in series with each thyristor as shown in Fig. 1.17.5(a).

- As shown, if the two thyristors that are to be connected in parallel have different forward current ratings I_1 and I_2 , then a resistance R_p in series with each one of them will ensure proper current sharing, i.e. in proportion with their current rating.

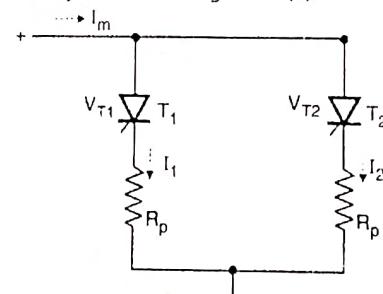
- Let V_{T1} and V_{T2} be the respective voltage drops across the two thyristors, at the forward currents I_1 and I_2 . As they are operating in parallel, the total voltage across them will be same.

$$\therefore V_{T1} + I_1 R_p = V_{T2} + I_2 R_p \quad \dots(1.17.3)$$

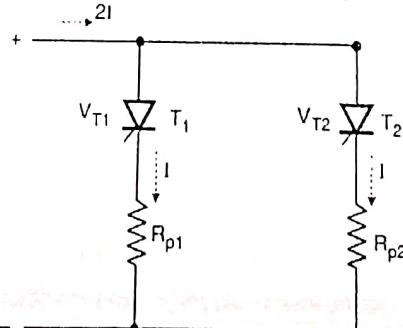
- If the values of V_{T1} , V_{T2} , I_1 and I_2 , V_{T3} are known, it is possible to find out the value of compensating resistance R_p .
- This method ensures that the total load current will be distributed in proportion with the current ratings of thyristors, instead of sharing it equally.

(b) Equal current sharing :

- If the two thyristors in parallel are having the identical current ratings, and equal current sharing is expected to take place, then the difference in their dynamic resistances can be compensated by connecting resistances R_{p1} and R_{p2} in series with T_1 and T_2 respectively as shown in Fig. 1.17.5(b).



(a) Proportional current sharing



(b) Equal current sharing

(I-1201) Fig. 1.17.5 : Current sharing in dc circuits

- Let V_{T1} and V_{T2} be the voltage drops across the two thyristors at forward current I_1 and I_2 as shown in Fig. 1.17.5(b).

- The resistors R_{10} and R_{20} are connected such that,

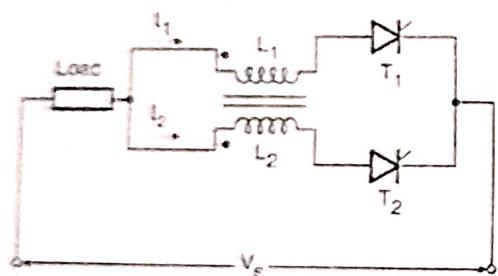
$$V_{R1} + I_1 R_{10} = V_{R2} + I_2 R_{20} \quad (1.17.4)$$

where, I = Equal current flowing through both the thyristors.

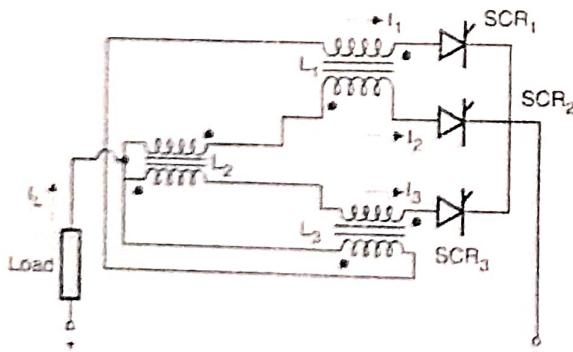
- The forced equal current sharing using externally connected resistors will be useful only under steady state but it cannot ensure equal current sharing in the transient state.
- Another disadvantage of this type of circuit is the large power loss taking place in the equalizing resistors. The more effective method uses the reactors in series with the thyristors instead of using resistors.

1.17.6 Current Sharing in AC Circuits (Dynamic Current Sharing) :

- In AC circuits the uniform current sharing can be achieved by magnetic coupling of parallel paths, as shown in Fig. 1.17.6(a).
- If the currents I_1 and I_2 are equal then the voltage drop in the series windings will be zero due to the mutual cancellation of flux linkage in the coils.
- But if the current through T_1 that is I_1 increases then voltages proportional to unbalance in current will be induced in the windings.



(a) Current sharing using magnetic coupling



(b) Current sharing using magnetic coupling

(I-1202) Fig. 1.17.6

Voltage in L_1 opposes the flow of current through and voltage in L_2 will assist the current through L_1 to attain parallel equilibrium.

- This action will continue to take place till the current sharing is achieved in AC circuits.
- The same principle can be used to have equal sharing currents with three or four SCRs connected in parallel, shown in Fig. 1.17.6(b).
- The reactors L_1, L_2, L_3, L_4 are more efficient as compared to the resistors as they consume less energy but are expensive.
- The most important magnetic requirements of reactors are : 1. high saturation and 2. low residual flux densities in order to provide as much change in flux in each cycle as possible.

1.17.9 String Efficiency and Derating :

- The string efficiency for the parallel string is defined as

$$\eta_p = I_m / n_p I_T \quad (1.17.5)$$

Where, I_m = Total forward current

n_p = Number of devices in parallel

I_T = Forward current rating of each thyristor

- The string efficiency is reduced by using more number of devices in the parallel string than actually required. But this will improve the reliability of the string.
- This will derate the devices and the percent derating is given by,

$$\% \text{Derating for parallel connection, } D_p = \left(1 - \frac{I_m}{n_p I_T} \right) \times 100\% \quad (1.17.6)$$

- If the percent derating is known, then we can calculate the number of devices required to be connected in parallel.
- Derating increases the reliability of the parallel string.

1.18 Series and Parallel Connection of GTO :

- It is possible to connect the GTO thyristors either in series and parallel.
- They are connected in series when the total operating voltage is higher than the breakdown voltage of a single GTO.

They are connected in parallel when the load current to be supplied is higher than the maximum current rating of a single GTO.

1.18.1 Series Connection of GTOs :

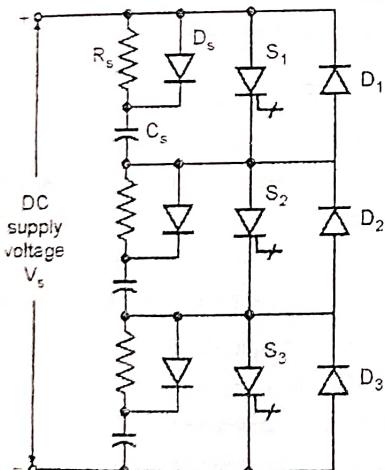
The series connection of GTO thyristors offers the benefits in terms of first-time and operating costs. In principle, the DC link voltage can be increased by increasing the number of GTO thyristors connected in series.

However, in practice special attention has to be paid to ensuring that the voltage is evenly distributed among the devices.

The possible problems that we can face after connecting GTO thyristors in series are of the unequal delay times and the unbalanced voltage distribution during turn-off.

During turn off, the fastest GTO turns off first, and has to bear the entire applied voltage across it.

Therefore, an equalizing circuit is used along with the series connected GTOs to ensure equal voltage distribution in the steady state and transient states of operation as shown in Fig. 1.18.1.



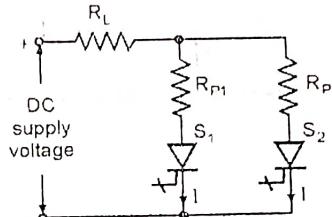
(G-2954) Fig. 1.18.1 : GTOs connected in series

- A number of important innovative steps were necessary before the required reliability and high efficiency could be ensured.
- One of them is to use more number of devices than actually required which results in the derating of devices and increase in string reliability as discussed for the SCR series connection.

1.18.2 Parallel Connection of GTOs :

GTO thyristors cannot be connected directly in parallel, as this would lead to an unequal distribution of the current.

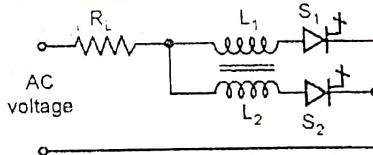
Therefore, as discussed for the parallel connection of SCRs, for a dc supply, we can connect a suitable resistor in series with each GTO as shown in Fig. 1.18.2, to ensure either equal current sharing or proportional current sharing among the parallel connected GTOs.



(G-2955) Fig. 1.18.2 : GTOs connected in parallel (dc circuit)

If the ac power is used then, we can use reactors in series with GTOs to ensure equal current sharing as shown in Fig. 1.18.3.

This is also similar to the technique used for SCRs.



(G-2956) Fig. 1.18.3 : GTOs connected in parallel (ac circuit)

Review Questions

- Explain the operation of SCR.
- Draw and explain the static I - V characteristics of SCR.
- Define and explain the holding current and latching current of SCR.
- Define and explain the break over voltage of SCR.
- Explain the effect of gate current magnitude on the operation of SCR.
- Define and explain various ratings of SCR.
- Define current ratings of SCR.
- Define RMS current rating of SCR.

Q. 9 Define I^2 tr

Q. 10 Explain how

Q. 11 State and SCR.

Q. 12 Explain th

Q. 13 Explain th

Q. 14 Explain th

Q. 15 Draw ar SCR.

Q. 16 Give adv SCR.

Q. 17 Define

Q. 18 With n

Q. 19 With r a GTO

Q. 20 State GTO

Q. 21 Expl

Q. 22 Give

Q. 23 Expl

Q. 24 Expl SC

Q. 25 Expl



- Q. 9 Define $I^2 t$ rating of SCR.
- Q. 10 Explain how to turn off a conducting SCR.
- Q. 11 State and explain the triggering requirements of SCR.
- Q. 12 Explain the resistive triggering circuit of SCR.
- Q. 13 Explain the RC triggering circuit of SCR.
- Q. 14 Explain the LUT triggering circuit for SCR.
- Q. 15 Draw and explain the dynamic characteristics of SCR.
- Q. 16 Give advantages, disadvantages and applications of SCR.
- Q. 17 Define GTO.
- Q. 18 With neat diagram explain the operation of a GTO.
- Q. 19 With neat diagram explain the turn off mechanism of a GTO.
- Q. 20 State and explain the triggering requirements of GTO.
- Q. 21 Explain a typical triggering circuit of GTO.
- Q. 22 Give applications of GTO.
- Q. 23 Explain the importance of series operation of SCRs.
- Q. 24 Explain the importance of parallel operation of SCRs.
- Q. 25 Explain the problem in direct series operation of SCRs.

Thyristors

- Q. 26 Explain the problem in direct parallel operation of SCRs.
- Q. 27 Explain how equal voltage sharing is ensured in series operation of SCRs.
- Q. 28 Explain how equal or proportional current sharing is ensured in parallel operation of SCRs.
- Q. 29 What are the differences between SCR and GTO?
- Q. 30 Define thyristor and name different thyristor devices.
- Q. 31 Compare SCR and GTO.
- Q. 32 Write a note on : Series and parallel operation of GTOs.
- Q. 33 Draw the static characteristics of SCR and explain different regions of operation.
- Q. 34 Draw the structure, symbol and V-I characteristics of a GTO.
- Q. 35 Draw the structure SCR and the two transistor equivalent of SCR. Explain its working.
- Q. 36 Give advantages and disadvantages of GTO.
- Q. 37 Explain the turn-off characteristics of SCR giving typical values of turn off time for normal and inverter grade SCRs.
- Q. 38 Why is reverse breakdown voltage greater than forward breakdown voltage in SCR?

Unit I

Chapter

2

Transistor Based Devices

Syllabus

Construction, VI characteristics (input, output and transfer if any), Switching characteristics of Power MOSFET and IGBT, Performance overview of Silicon, Silicon carbide and GaN based MOSFET and IGBT, Various repetitive and non-repetitive ratings of Power MOSFET and IGBT and their significance, Requirement of typical triggering / driver (such as opto isolator) circuits for various power devices, Importance of series and parallel operations of various power devices (No derivation and numerical).

Chapter Contents

- | | |
|---|--|
| 2.1 Power Transistors | 2.10 Static (I-V) Characteristic of IGBT |
| 2.2 Construction of Power BJT | 2.11 Principle of Operation of IGBT |
| 2.3 Static Characteristic of Power BJT | 2.12 IGBT Driving Circuits |
| 2.4 Power MOSFET | 2.13 Ratings of IGBT |
| 2.5 Gate Driving Requirements of a Power MOSFET | 2.14 Parallel Operation of IGBTs |
| 2.6 Ratings of Power MOSFET | 2.15 Comparison of Power Devices |
| 2.7 Parallel Operation of MOSFETs | 2.16 Isolation of Gate and Base Drives |
| 2.8 Insulated Gate Bipolar Transistor (IGBT) | 2.17 Silicon Carbide (SiC) Devices |
| 2.9 Construction of IGBT | 2.18 GaN Power Devices |

2.1 Power Transistors :

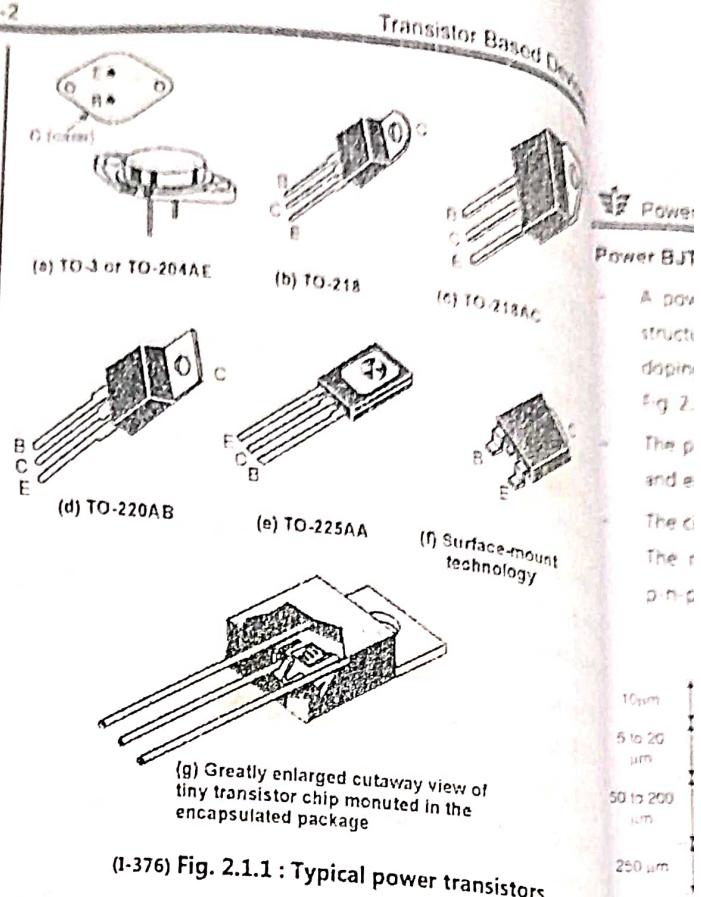
- Power transistors are used as switches in various power converters such as dc-dc converters and dc-ac converters.
- For operating them as switches, we should operate them in cut-off and saturation regions of operation.
- The power transistors can operate at much higher switching speeds as compared to those of thyristors.
- But their voltage and current ratings are much lower than those of the thyristors.
- Hence power transistors are preferred for the low and medium power applications.

2.1.1 Classification of Power Transistors :

- The power transistors can be classified broadly into four categories as follows :
 1. Bipolar junction transistors (BJTs).
 2. Metal-oxide-semiconductor field effect transistor (MOSFET).
 3. Static-induction transistors (SITs).
 4. Insulated-gate bipolar transistors (IGBTs).
- The selection of a particular device depends on the factors such as power handling capability, switching speed, on-state voltage drop and turn-on/turn-off delays.

2.1.2 Power BJT :

- Power transistors are used to handle large currents (typically more than 1 Amp) and/or large voltages.
- The power handling capacity of the power transistors is very large.
- They have to dissipate a large power in the form of heat.
- Therefore power transistors are available in special packages as shown in Fig. 2.1.1.
- The size of power transistors is larger than that of the low power transistor. This is necessary for dissipating more power.
- Sometimes power transistors are mounted on heatsinks.
- The heatsinks are made of metal and they increase the effective area of the power transistors.
- The increased area allows easy transfer of heat to take place from the device to atmosphere.



(I-376) Fig. 2.1.1 : Typical power transistors

2.2 Construction of Power BJT :

SPPU : May 10, Dec 11, Dec 12, May 13, Dec 14

University Questions

- Q. 1** With the help of structure explain the operation of power BJT. (May 10, 4 Marks)
- Q. 2** Draw the construction diagram of power BJT and explain its steady state characteristics. (Dec. 11, May 13, Dec. 13, 7 Marks)
- Q. 3** Draw the construction diagram of power BJT and explain its different switching limits. (Dec. 12, 5 Marks)

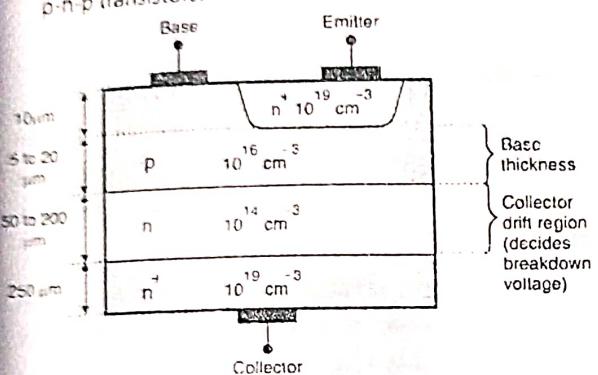
- The power bipolar junction transistor is supposed to block a high voltage in the off-state and have high current carrying capacity in the on-state.
- In order to have these characteristics the power bipolar junction transistor (BJT) must have a very different structure than a small low power BJT.
- Due to the modified structure the I-V characteristics and the switching behaviour of power BJT will be significantly different than its logical counterpart. The base drive circuits will be different, and protection circuits will have to be included alongwith a power BJT.

Power BJT structure :

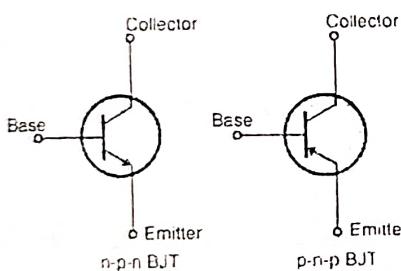
A power transistor has a vertically oriented four-layer structure of alternating p-type and n-type layers with doping similar to the n-p-n transistor as shown in Fig. 2.2.1(a).

The power transistor has three terminals collector, base and emitter.

The circuit symbol for the BJT is as shown in Fig. 2.2.1(b). The n-p-n transistors are more widely used than the p-n-p transistors.



(a) Vertical cross-section of a typical n-p-n bipolar transistor



(b) The circuit symbol for the power transistor

(I-377) Fig. 2.2.1

Why is the vertical structure used ?

The reason for using the vertical structure is that it increases the cross-sectional area through which the device current flows.

This will reduce the on-state resistance and hence the on-state power dissipation taking place in the transistor.

The vertical structure also minimizes the thermal resistance of the transistor (resistance offered to the flow of heat) and reduces the power dissipation.

Doping levels :

Fig. 2.2.1(a) shows the doping levels in each of the layers.

- The thickness of the different layers will have a significant effect on the characteristics of the device.
- As shown in Fig. 2.2.1(a) the emitter layer is heavily doped.
- The base is moderately doped. The (n⁻) region is known as the **collector drift region** and it is lightly doped.
- The (n⁻) region next to the drift region has doping level similar to that of emitter. This (n⁻) region serves the collector region.
- The base region (p) is moderately doped and it is thin as compared to the drift region.

What is the function of the (n⁻) drift layer ?

- If the structure of power transistor (Fig. 2.2.1(a)) is compared with that of a logic level transistor, it is found that the (n⁻) drift layer is the additional layer included in power transistors.
- Due to the low doping level, the (n⁻) drift layer will increase the voltage blocking capacity of the transistor. (This is explained later).
- The width of this layer will decide the breakdown voltage of power transistor.
- The disadvantage of including this layer is that the on-state device resistance increases, increasing the on-state voltage (V_{CE}) and the on state power loss ($V_{CE} \times I_C$) as well.

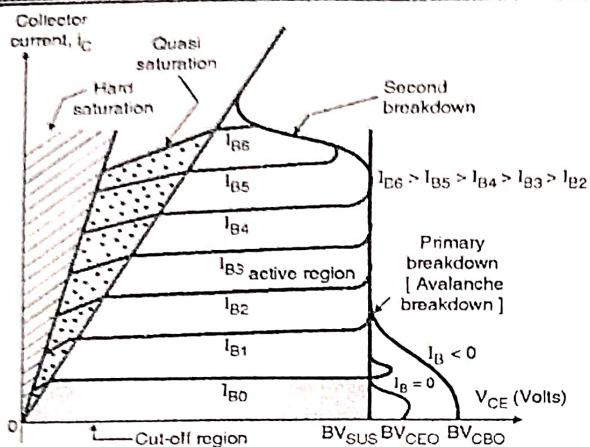
2.3 Static Characteristic of Power BJT :

SPPU, Dec. 09, Dec. 11, May 13, Dec. 13

University Questions

- Q. 1** Draw and explain static characteristics of power BJT. (Dec. 09, 6 Marks)
- Q. 2** Draw and explain steady state characteristics of power BJT with construction. (Dec. 11, 5 Marks)
- Q. 3** Draw the construction diagram of power BJT and explain its steady state characteristics. (May 13, Dec. 13, 7 Marks)

- The output characteristics of a typical n-p-n power transistor are as shown in Fig. 2.3.1.
- These curves have been plotted for different values of base currents.



(I-378) Fig. 2.3.1 : Current voltage characteristics of a n-p-n power transistor

- As seen from Fig. 2.3.1, the characteristics of a power transistor can be divided in four regions :
 1. Cut-off region
 2. Active region
 3. Quasi saturation region
 4. Hard saturation region
- Out of these, the cut-off, active and hard saturation regions are similar to those in the logic level transistors but the quasi saturation region is completely different.
- The status of the two junctions, the corresponding region of operation and the application of power transistor are shown in Table 2.3.1.

Table 2.3.1

Region of operation	Emitter junction	Collector junction	Transistor operates as
Cut-off	Reverse biased	Reverse biased	—o— (I-379)
Active	Forward biased	Reverse biased	Amplifier
Quasi saturation	Forward biased	Forward biased	—o—o— (I-380)
Hard saturation	Forward biased	Forward biased	—o—o— (I-381)

1. Cut-off region :

- The BE and CB both the junctions are reverse biased to operate the transistor in cut-off region.

- The base current $I_b = 0$ and the collector current is equal to the reverse leakage current I_{cfo} . The region below the characteristics for $I_b = 0$ is cut-off region.
- The power transistor offers a large resistance to the flow of current. Hence it is equivalent to an open switch.
- 2. Active region :**
 - The B-E junction is forward biased, and C-B junction is reverse biased to operate the transistor in the active region.
 - The collector current I_c increases slightly with increase in the voltage V_{ce} . However the collector current is largely dependent on the base current I_b .
 - At a fixed value of V_{ce} , if I_b is increased, then it will cause I_c to increase substantially.
 - This is because $I_c = \beta_{dc} I_b$. This relation is true only for the active region of operation.
 - The power transistor should be operated in this region, if it is to be used as an amplifier or as a series pass transistor in the voltage regulators.
 - The dynamic resistance of the transistor is large in this region.
 - So a large voltage appears across it.
 - The power dissipation of the power transistor is maximum when operated in the active region.
- 3. Quasi-saturation :**
 - The major difference between power transistor and logic level transistor is the region called "Quasi-saturation" as shown in Fig. 2.3.1.
 - This region exists due to the lightly doped drift layer present in the power transistors. Logic level transistors do not have this layer and so they do not exhibit the Quasi-saturation region.
 - Quasi-saturation region is between hard saturation and active regions. When the power transistor is to be operated at high switching frequency, it is operated in this region.
 - In this region the current gain β of the power transistor is lower than that in the active region.
 - Both the junctions of power transistor are forward biased, for operation in quasi-saturation.

The device offers a low resistance than that in the active region. Hence voltage drop across the power transistor is lower than that in the active region.

 - We can use the power transistor as a switch.



- Since the device does not go into deep saturation, we can turn-off the power transistor quickly.
- So we can switch the power transistor at a higher rate if operated in the quasi saturation region than that if operated in the hard saturation.

4. Hard saturation :

- By increasing the base current further, the power transistor can be pushed into the hard saturation from the quasi saturation. Hard saturation means deep saturation (deeper than the Quasi saturation).
- The resistance offered by the power transistor in this region is minimum. It is even less than that in the quasi saturation region.
- So the voltage across the power transistor and the power dissipation are minimum when operated in hard saturation.
- The transistor acts as a closed switch when biased in this region.
- However due to deep saturation, a longer time is required to turn-off the power transistor.
- Therefore hard saturation region is suitable only for the low frequency switching applications.

Both the junctions of the power transistor are forward biased for operating it in the hard saturation.
The collector current is not proportional to the base current any more. In fact I_C remains almost constant at $I_{C(\text{sat})}$ independent of the value of base current.

her features of the I-V characteristics :

1. The maximum collector to emitter voltage that can be sustained across the transistor when it is carrying a substantial collector current is usually called as $B V_{\text{SUS}}$. If voltage is increased beyond this the device will breakdown.
2. But if the base current is zero then the maximum collector to emitter voltage that can be sustained, increases to a value called as $B V_{\text{CEO}}$ i.e. the collector-emitter breakdown voltage when the base is open circuited.
3. The voltage $B V_{\text{CBO}}$ is the collector base breakdown voltage when the emitter is open circuited. This voltage is greater than $B V_{\text{CEO}}$.

Primary breakdown :

The region called primary breakdown as shown in Fig. 2.3.1 is due to the conventional avalanche breakdown of the collector-base junction and a large current flow is associated with it.

- The primary breakdown must be avoided due to the associated large power dissipation with it.
- The primary breakdown in power BJT is identical to that in the logic level transistor.

Second breakdown :

- The region labelled second breakdown shown in Fig. 2.3.1 is also to be avoided due to large power dissipation that accompanies it. From Fig. 2.3.1 it is clear that at large values of collector currents the collector emitter voltage decreases.
- Therefore the collector current increases and there is a rise in power dissipation.
- This power dissipation is not evenly distributed across the volume of the device. Instead it is concentrated in highly localized regions.
- Therefore the temperature of these local regions increases rapidly and the power transistor gets damaged.
- The second breakdown has been discussed in detail later in this chapter.

2.3.1 Operation of Power Transistor :

SPPU May 10

University Questions

Q. 1 With the help of structure explain the operation of power BJT. (May 10, 4 Marks)

- As we have already seen, the difference between the power transistor and that of a logic level transistor is that in the power transistor an additional region called collector drift region is included.
- However the basic mechanism of operation for the power transistors is same as that in the logic level transistors, even the current gain mechanism is similar.
- The collector drift region does not play any role when the power transistor is in the active region.
- The drift region only affects the breakdown voltage, on-state losses and switching time of a power transistor.

2.4 Power MOSFET :

- The long form of MOSFET is Metal Oxide Semiconductor Field Effect Transistor.
- The new power MOSFETs have improved current carrying capacity and higher off state blocking voltage capacity and they are replacing the power transistors in many applications.

- Power MOSFETs are capable of switching at very high frequencies up to about 100 kHz. This is much higher than the 10 kHz limit for power transistors.
- A power BJT is a current controlled device. The collector current is dependent on the base current hence the current is highly dependent on the junction temperature. This is a serious disadvantage of power BJT.
- To overcome this disadvantage, we can use a voltage controlled device such as a power MOSFET.
- The other advantage of MOSFET is that it requires only a small input current.
- Some of the important features of a power MOSFET are as follows :

Features of power MOSFET :

1. Low input current.
2. It is a voltage controlled device.
3. Switching speed is very high.
4. Switching speeds are of the order of nanoseconds.
5. They do not have the problem of second breakdown.

Types of MOSFETs :

- MOSFETs are of two types :
 1. Depletion-type MOSFET.
 2. Enhancement type MOSFET.
- MOSFET is a three terminal device. The terminals are Drain, Source and Gate.

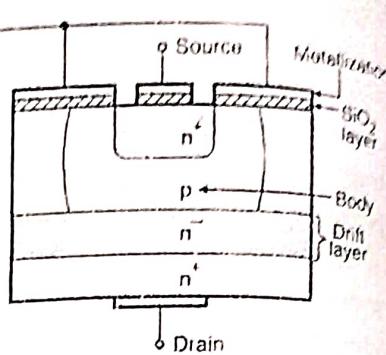
2.4.1 Structure of a Power MOSFET :

SPPU Dec 07, May 08, Dec 13, May 18.

University Questions

- Q. 1 Draw vertical structure of Power MOSFET. (Dec. 07, 2 Marks)
- Q. 2 Draw the vertical cross-section of a power MOSFET and explain the following :
 1. Reason for "body-source-short" in MOSFET structure.
 2. Presence of integral reverse diode in the structure. (May 08, 7 Marks)
- Q. 3 Draw construction diagram and explain switching characteristics of MOSFET. (Dec. 13, 7 Marks)
- Q. 4 Draw the construction of power MOSFET and explain I-V steady state characteristics of power MOSFET. Compare and contrast with SCR. (May 18, 7 Marks)

The power MOSFETs are generally enhancement type. In order to increase the voltage rating of enhancement MOSFET, a drift layer is included in Fig. 2.4.1.



(a-411) Fig. 2.4.1 : Basic structure of power MOSFET

- The power MOSFET has the vertically oriented four layered structure of alternate p and n layers as shown in Fig. 2.4.2(a). The symbols of a power MOSFET are shown in Fig. 2.4.2(b).
- The vertically oriented structure is used to minimize the area of current flow. This reduces the on-state resistance and therefore on-state loss are also reduced.
- The p-type middle layer is termed as "body". The body layer is the "drift region" and it is lightly doped compared to the drain and source layers. This region determines the breakdown voltage of the power MOSFET.

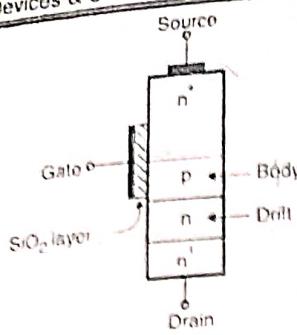
2.4.2 Simplified Structure of Power MOSFET

SPPU Dec 11, May 15, Feb 16, May 18

University Questions

- Q. 1 Draw n-channel enhancement power MOSFET. (Dec. 11, 2 Marks)
- Q. 2 Explain the construction of power MOSFET. n-channel enhancement power MOSFET. (Dec. 11, 2 Marks)
- Q. 3 Draw construction diagram of n-channel enhancement type MOSFET and explain its steady state characteristics. (May 15, Feb 16, 7 Marks)
- Q. 4 Draw the construction of power MOSFET and explain steady state characteristics of power MOSFET. Compare it with SCR and IGBT. (May 17, 7 Marks)

- Fig. 2.4.2(a) shows the simplified structure of power MOSFET and Fig. 2.4.2(b) shows the circuit symbols.



(I-411) Fig. 2.4.2(a) : Simplified structure of PMOS

The n-p-n-n' structure shown in the Fig. 2.4.2(a) is termed as enhancement mode n channel MOSFET.

A structure of a P-channel MOSFET has exactly the opposite doping profile.

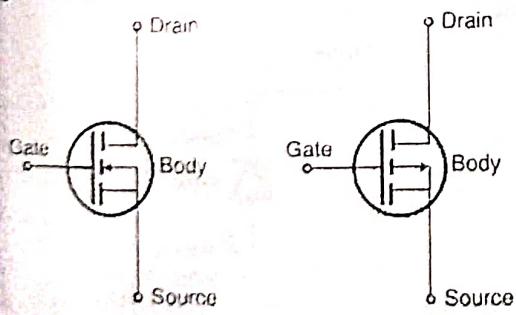
The doping in the two n' regions of Fig. 2.4.2(a) that means the "source" and "drain" is approximately the same in both the layers and it is quite large.

Three terminals are brought out for the user's access, which are drain, source and gate.

The body terminal is not brought out, instead it is shorted with the source terminal internally.

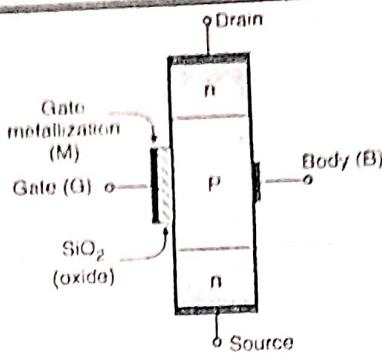
The direction of arrow on the body lead indicates the direction of current flow if the body source p-n junction were forward biased by removing the short link between body and source.

Therefore n-channel MOSFET has a P-type body region and the arrow points into the MOSFET symbol. (Refer to Fig. 2.4.2(b)).



(I-411) Fig. 2.4.2(b) : Circuit symbol

A more simplified structure of the enhancement power MOSFET is as shown in Fig. 2.4.3.



(Drift layer not shown)

(I-412) Fig. 2.4.3 : Structure of enhancement type MOSFET

- As seen from Fig. 2.4.3, the gate terminal is not connected directly to the semiconductor (P-layer), instead there exists an oxide layer (SiO₂) between the metal and semiconductor.
- The oxide layer acts as a layer of dielectric between the metal and the semiconductor to form a MOS (Metal Oxide Semiconductor) capacitance at the input of the MOSFET. This MOS capacitance does not exist in the low power JFET.
- The input capacitance of MOSFET is large (greater than 1000 pF). The SiO₂ oxide layer isolates the gate terminal from the body layer and gives the device insulating properties.

2.4.3 Principle of Operation :

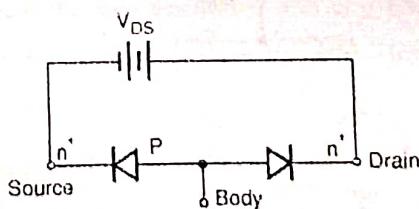
SPPU Dec. 07

University Questions

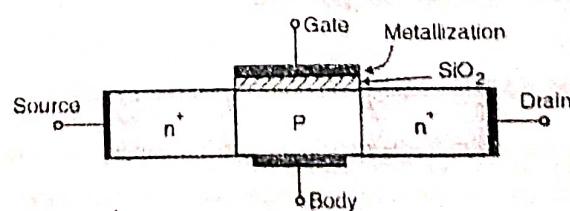
Q. 1 Explain operation of power MOSFET.

(Dec. 07, 2 Marks)

- With gate to source voltage $V_{GS} = 0$ the MOSFET is equivalent to two back to back diodes connected as shown in Fig. 2.4.4(a).



(a) Equivalent circuit of MOSFET for $V_{GS} = 0$



(b) Basic structure of MOSFET

(I-413) Fig. 2.4.4

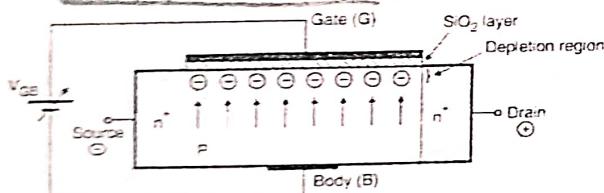
- The diodes are formed between n^+ and P-layers as shown. The basic structure of MOSFET is very much similar to the BJT.
- The only difference is the presence of the SiO_2 oxide layer that isolates the gate from the body region.
- When a positive gate to source voltage is applied, the MOSFET turns on.
- The operation takes place as explained as follows .

Operation :

- The basic structure of the n-type MOSFET is as shown in Fig. 2.4.4(b).
- Power MOSFET is a minority carrier device. The conduction takes place only due to electrons. Hence it is felt that the conduction cannot take place through a MOSFET from drain (n^+) to source (n^+) due to presence of P-layer (base layer) in between.
- But practically it is possible due to a phenomenon called "Inversion layer creation" which is explained with reference to Fig. 2.4.5 and Fig. 2.4.6.
- The operation of power MOSFETs can be divided into two steps :
 1. Formation of depletion region
 2. Creation of inversion layer.

1. Formation of depletion region :

- The MOSFET is forward biased by connecting a positive voltage to its drain terminal with respect to source terminal and the gate is made positive with respect to the body layer as shown in Fig. 2.4.5.

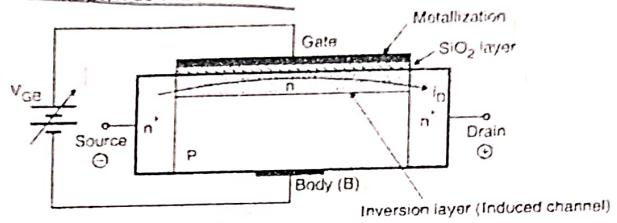


(2.4.5) Fig. 2.4.5 : Depletion layer creation

- The "P" layer of Fig. 2.4.5 consists of a large number of holes and few electrons. The holes are majority carriers.
- Hence they outnumber the electrons which are minority carriers, still the number of electrons present in the "P" layer is sufficiently large.
- Due to the positive voltage applied between gate and body as shown in Fig. 2.4.5, these electrons are attracted towards the gate and gather below the SiO_2 layer and produce depletion layer by combining with the holes that are present there.

2. Creation of inversion layer (Induced channel) :

- If the positive gate voltage is increased further, the number of electrons below the SiO_2 layer will be greater than the number of holes.
- Thus the conductivity of the part of P-layer close to SiO_2 layer will change from positive to negative.
- That means an n type of sub layer is formed below the SiO_2 layer as shown in Fig. 2.4.6.
- This process is known as **creation of the inversion layer**, and the process of generation of an inversion layer due to the externally applied gate voltage is known as the "field effect".



(2.4.6) Fig. 2.4.6 : Formation of an inversion layer

- The inversion layer is also called as the **induced channel**.
- This induced channel will connect the two n^+ layers on either sides of the P-region.
- In this way now the n-type channel gets created in the P-type body layer and conduction can take place through this layer as shown in Fig. 2.4.6.
- The resistance of the induced channel is dependent on the magnitude of gate to base (body) voltage. Higher the gate voltage less is the resistance. The MOSFET acts as a variable resistor.
- With increase in the gate to body voltage, the resistance will decrease.
- However this resistance cannot decrease below a certain minimum value; even with increase in the gate to body voltage.
- If the maximum specified value of gate voltage is exceeded then the SiO_2 layer will breakdown.

2.4.4 I-V (Static) Characteristic of MOSFET :

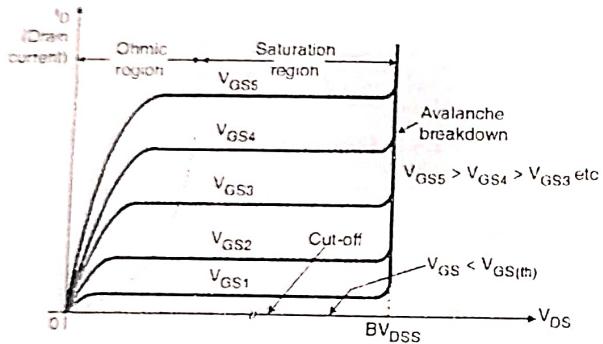
SPPU : May 10, May 15, Feb. 16, May 17,
May 18, Dec. 19

University Questions

- Q. 1 Draw and explain static characteristics of power MOSFET. (May 10, 4 Marks)

- Q. 2** Draw construction diagram of n-channel enhancement type MOSFET and explain its steady state characteristics. (May 15, Feb 16, 7 Marks)
- Q. 3** Draw the construction of power MOSFET and explain steady state characteristics of power MOSFET. Compare it with SCR and IGBT. (May 17, 7 Marks)
- Q. 4** Draw the construction of power MOSFET and explain I-V steady state characteristics of power MOSFET. Compare and contrast with SCR. (May 18, 7 Marks)
- Q. 5** Draw & explain steady state characteristics of power MOSFET. (Dec. 19, 6 Marks)

- The I-V characteristics of a power MOSFET is shown in Fig. 2.4.7(a).



Q-416) Fig. 2.4.7(a) : Output I-V characteristics of n channel enhancement mode VMOSFET

- The source terminal is common between the input and output of the MOSFET.
- The output characteristics, is a graph of drain current I_D versus drain to source voltage V_{DS} for different values of gate to source voltage V_{GS} as shown in Fig. 2.4.7(a).
- The saturation, cut-off and ohmic regions of the characteristics are also shown in Fig. 2.4.7(a).
- In the power electronic applications where the MOSFET is used as switch, the device must be operated in the cut-off and ohmic region when turned off and on respectively.
- The operation in the saturation region should be avoided to reduce the power dissipation in the on-state. (The on-state voltage across the MOSFET is high in the saturation region).
- The MOSFET is in the cut-off state when the gate source voltage V_{GS} is less than the threshold voltage $V_{GS(\text{th})}$.

- The device must withstand to the applied voltage and to avoid the breakdown the drain to source breakdown voltage should be greater than the applied voltage.
- The breakdown takes place due to the avalanche breakdown of the drain body junction.
- When a larger positive gate to source voltage is applied power MOSFET goes into the ohmic region where the drain to source voltage $V_{DS(\text{on})}$ is small.
- In this region of operation the power dissipation can be kept reasonably low, by minimizing the on state voltage.
- In the saturation region the drain current I_D is almost independent of the drain to source voltage V_{DS} . It is only dependent on the gate to source voltage V_{GS} .
- In the saturation region the gate voltage V_{GS} is greater than the threshold voltage $V_{GS(\text{th})}$ and the drain current increases with increase in V_{GS} .

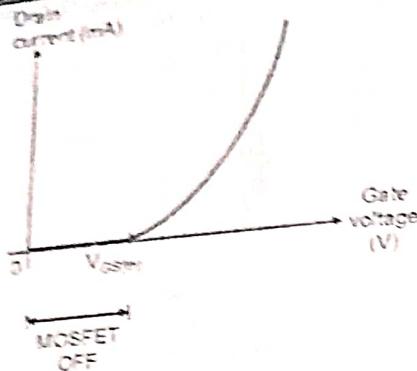
Conclusions from the static characteristics :

- The important conclusions from the static characteristics are as follows :
 1. The MOSFETs are voltage controlled devices i.e. the output current can be controlled by varying the gate to source voltage (V_{GS}).
 2. With increase in V_{GS} the drain current will increase.
 3. The gate to source voltage (V_{GS}) should be large enough to drive the MOSFET into ohmic region. Practically the minimum V_{GS} required is about 12 V. If V_{GS} is less than 12 V, the MOSFET will operate in the active region which is not desired.
 4. When the forward voltage V_{DS} applied to the MOSFET exceeds the breakdown voltage $B V_{DSS}$, the avalanche breakdown takes place. Operation above the breakdown voltage must be avoided, to protect the MOSFET.
 5. The second breakdown does not exist in MOSFETs.

Transfer Characteristic of MOSFET :

Definition :

- The transfer characteristic of a power MOSFET is a plot of drain current versus the gate voltage. The transfer characteristics of IGBT and MOSFET are similar.
- Fig. 2.4.7(b) shows the transfer characteristic of power MOSFET.

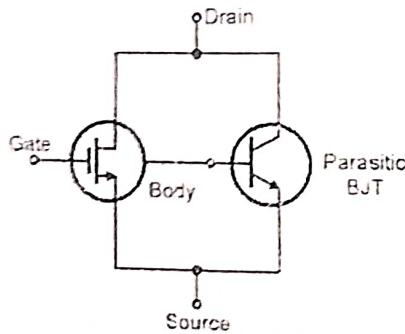


(Q-255) Fig. 2.4.7(b) : Transfer characteristic of power MOSFET

- The power MOSFET is in the off-state if the gate-source potential is below the threshold voltage.
- For gate voltages greater than the threshold voltage the transfer curve is linear over most of the drain-current range.
- Gate oxide breakdown and the maximum power MOSFET drain current limit the maximum gate-source voltage.

2.4.5 Equivalent Circuit of Power MOSFET :

- The switching characteristics of a power MOSFET can be divided into two parts :
 1. Turn-on characteristics
 2. Turn-off characteristics.
- Without any gate signal, the power MOSFET is equivalent to two diodes connected back to back or an N-P-N transistor.
- The equivalent circuit of the power MOSFET consists of a MOSFET and a BJT as shown in Fig. 2.4.8(a).



(I-417) Fig. 2.4.8(a) : Equivalent circuit of power MOSFET

- From the equivalent circuit it can be seen that the MOSFET and parasitic BJT are in parallel with each other.

Therefore due to some reason if the BJT is turned on, then the MOSFET will be bypassed. The power MOSFET will no more work like MOSFET.

- Once the parasitic BJT turns on, it cannot be turned off since the gate has no control over it.
- Then the device will remain continuously on, called as latch up problem which may lead to destruction.

The parasitic BJT in the equivalent circuit of Fig. 2.4.8(a) may turn-on due to the voltage drop across the body region. In order to avoid the turn-on of parasitic BJT the body and source layers are circuited externally as shown in Fig. 2.4.8(b).

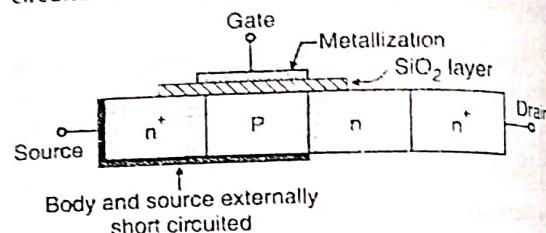
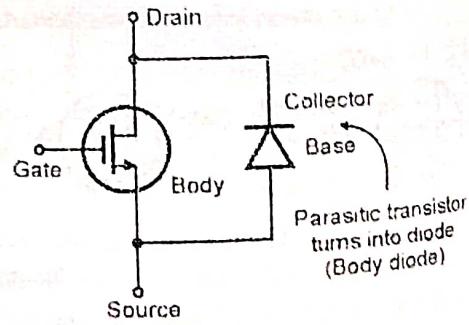


Fig. 2.4.8(b) : Power MOSFET with body source shorted externally to avoid the turn on of avoid the turn on of parasitic BJT

- Due to this connection the base and emitter terminals of the parasitic BJT are shorted so the parasitic BJT cannot turn on and the latch up cannot take place.
- The body drain junction acts as a diode (Fig. 2.4.8(c)). Turn-on voltage ($V_{DS(on)}$) and its current handling capability is very high and comparable to that of the MOSFET itself.
- When the source terminal is made positive with respect to drain, a current can flow through the body diode.



(I-418) Fig. 2.4.8(c)

- In the reverse biased condition (V_{DS} negative) the power MOSFET thus behaves like P-N junction diode.

Transistor Based
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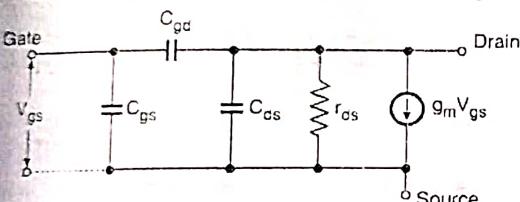
2.4.6 Switching Characteristic of MOSFETs :

SPPU [May 08, Dec. 09, Dec. 10, May 11 (May 12), Dec. 12, Dec. 13]

University Questions

- Q. 1** Draw the vertical cross-section of a power MOSFET and explain the following.
- Reason for "body-source-short" in MOSFET structure
 - Presence of integral reverse diode in the structure (May 08, 7 Marks)
- Q. 2** Draw and explain switching characteristics of MOSFET (Dec. 09, May 11, 6 Marks)
- Q. 3** Explain switching characteristics of MOSFET. (Dec. 10, 6 Marks)
- Q. 4** Explain the reason for body source short in MOSFET structure. (May 12, 6 Marks)
- Q. 5** Draw construction diagram and explain switching characteristics of power MOSFET (n-channel enhancement type). (Dec. 12, 7 Marks)
- Q. 6** Draw construction diagram and explain switching characteristics of MOSFET. (Dec. 13, 7 Marks)

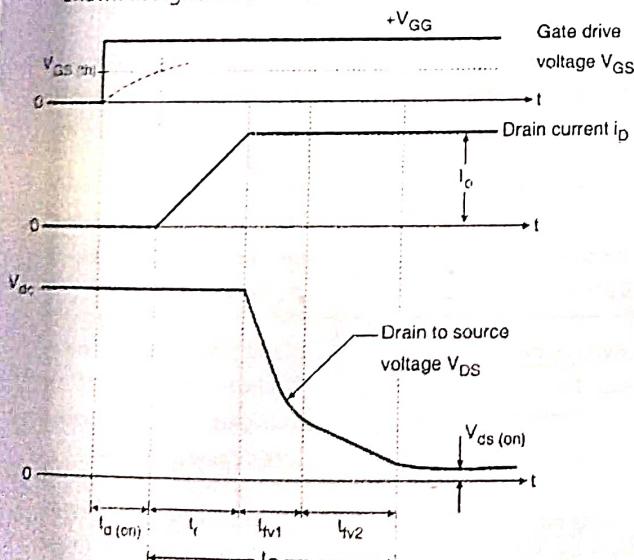
The switching model of MOSFETs is shown in Fig. 2.4.9.



(I-419) Fig. 2.4.9 : Switching model of MOSFETs

Turn-on Characteristics :

- The turn-on characteristics of a power MOSFET is as shown in Fig. 2.4.10.



(I-420) Fig. 2.4.10 : Turn-on characteristics of a power MOSFET

Transistor Based Devices

The gate to source voltage changes from 0 to $+V_{GS}$ at $t = 0$.

This voltage is much higher than the minimum gate to source voltage $V_{GS(on)}$.

Delay time $t_{d(on)}$:

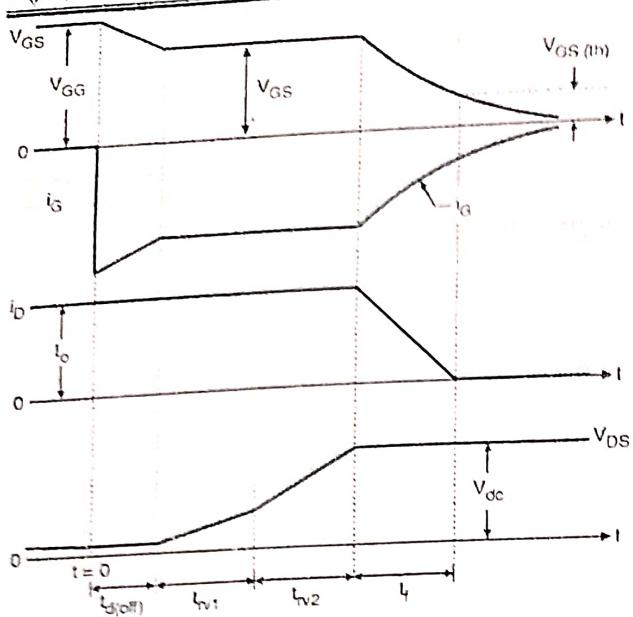
- During the turn-on delay time $t_{d(on)}$, the drain current remains zero and drain to source voltage V_{DS} remains constant at supply voltage V_{dc} .
- The delay time is actually the time that is required to charge the input capacitance C_{gs} to the threshold voltage $V_{GS(on)}$.

The rise time t_r :

- The rise time t_r is the gate charging time. It is the time taken by V_{GS} to rise from the threshold voltage $V_{GS(on)}$ to the full gate voltage V_{GS} .
- The time required for the drain current to rise from 0 to I_o is the current rise time t_r .
- The drain to source voltage remains constant during the rise time interval.
- At the end of the rise time interval, the drain current reaches its maximum value I_o and V_{DS} starts decreasing.
- The reduction in V_{DS} from V_{dc} to $V_{DS(on)}$ takes place in two distinct time intervals t_{fv1} and t_{fv2} .
- At the end of interval t_{fv2} the drain to source voltage finally reaches its on-state value $V_{DS(on)}$ and the turn-on process of the MOSFET gets complete.
- During the two intervals t_r and t_{fv1} the drain current and drain source voltage V_{DS} both have substantially high values.
- Therefore the power dissipated in the power MOSFET will be extremely large.
- To reduce this power loss, the turn-on time of the MOSFET should be minimized.

Turn-off Characteristics :

- The turn-off characteristics of a power MOSFET is as shown in Fig. 2.4.11.



(I-421) Fig. 2.4.11 : Turn-off characteristics of a power MOSFET

- The turn-off process of the MOSFET is based on an inverse sequence of operation that occurred during turn-on.

Turn-off delay time $t_{d(\text{off})}$:

- It is the time required for the input capacitance C_{gs} to discharge completely. V_{GS} needs to reduce significantly before V_{DS} starts rising.
- The time intervals t_{rv1} and t_{rv2} should be as short as possible to reduce the power dissipation taking place in a power MOSFET.

The fall time t_f :

- This is the time required for the input capacitance C_{gs} to discharge from the pinch-off region to the threshold voltage, because if $V_{GS} \leq V_{GS(\text{th})}$, then the power MOSFET will be turned off.
- The total turn-off time is given by,

$$t_{\text{off}} = t_{d(\text{off})} + t_{rv1} + t_{rv2} + t_f \quad \dots(2.4.1)$$

2.5 Gate Driving Requirements of a Power MOSFET :

SPPU Dec 16

University Questions

- Q. 1 Explain the gate drive circuit requirements for MOSFET & draw the sample drive circuit.
(Dec. 18, 6 Marks)

MOSFET is a voltage controlled device whereas BJT is a current controlled device.

The drive circuit requirements of MOSFET are therefore slightly different from those of the power BJT. The requirements are as follows :

- The gate drive circuit should provide large positive and negative gate current to charge and discharge the gate to source capacitance of MOSFET quickly while switching on and off the MOSFET respectively. This will reduce the switching times.
- It should provide a sufficiently high voltage between gate and source to turn-on the MOSFET.
- This voltage should be between $V_{GS(\text{max})}$ and $V_{GS(\text{threshold})}$. Typically V_{GS} is between 12 to 18 Volts to turn-on the MOSFET and $V_{GS} = 0$ Volts to turn it off.
- It should not leave the gate terminal of MOSFET open under any circumstances.
- This is essential to avoid the device damage due to static charge.
- The control and power circuits should be isolated from each other. An opto coupler can be used for this purpose.
- A current sensing circuit should be used to protect the MOSFET against drain over currents. MOSFETs cannot be protected using fuse links or semiconductor fuse.

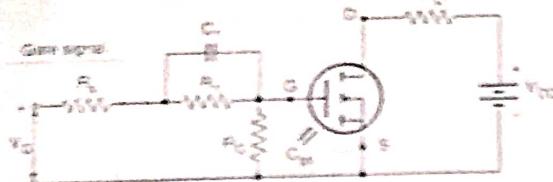
2.5.1 Gate Drive Circuit for MOSFETs :

SPPU May 11, Dec 12, Dec 18

University Questions

- Q. 1 Explain typical gate drive circuit for MOSFET.
(May 11, 4 Marks)
- Q. 2 Draw and explain gate drive circuit for MOSFET.
(Dec. 12, 5 Marks)
- Q. 3 Explain the gate drive circuit requirements for MOSFET & draw the sample drive circuit.
(Dec. 18, 6 Marks)

- MOSFET have a high gate to source capacitance C_{gs} .
- The input capacitance C_{gs} decides the turn-on time of a power MOSFET. The turn-on time depends on the time taken by this capacitance to charge to the adequate level of V_{GS} .
- Fig. 2.5.1 shows a gate driving circuit to ensure fast turn-on of a power MOSFET.

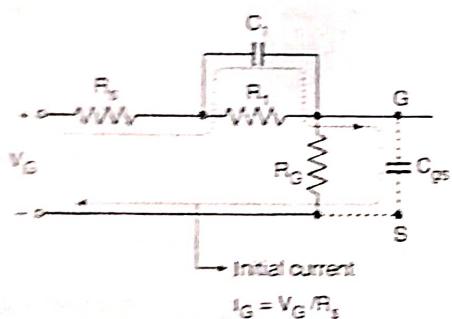


(a-424) Fig. 2.5.1 : Gate circuit for fast turn-on

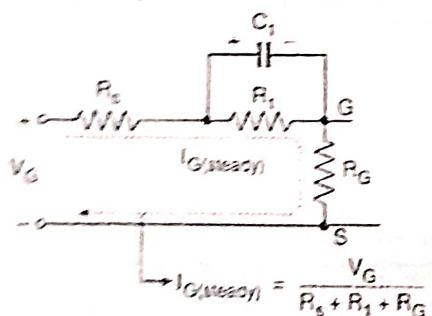
- The RC circuit is connected in order to reduce the turn-on time of the power MOSFET.
- This circuit helps to charge the gate to source capacitor C_{GS} faster.
- As soon as we turn-on the gate voltage V_G , the initial charging current of the capacitor is,

$$I_G = V_G / R_s \quad (2.5.1)$$

- This is because the initial current flows through R_s and C_1 as shown in the equivalent circuit of Fig. 2.5.2(a).
- After sometime C_1 and C_{GS} are fully charged and current gets diverted through R_1 and R_2 as shown in Fig. 2.5.2(b).



(a) Charging of C_{GS} is initially through R_s and C_1



(b) Steady state current flows through R_s , R_1 and R_2

(a-425) Fig. 2.5.2

Therefore the steady state value of gate current is given by,

$$I_{G, \text{steady}} = \frac{V_G}{(R_s + R_1 + R_2)} \quad (2.5.2)$$

Hence the corresponding value of gate to source voltage is,

$$V_{GS} = I_{G, \text{steady}} \times R_2 = \frac{R_2 V_G}{(R_s + R_1 + R_2)} \quad (2.5.3)$$

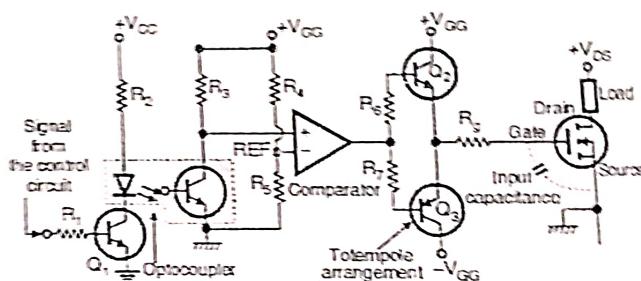
R_2 = Internal resistance of the external source.

2.5.2 A Typical Gate Drive Circuit for Higher Switching Speeds : SPPU : May 12

University Questions

Q. 1 Draw isolated gate drive circuit for MOSFET and explain its operation (May 12, 6 Marks)

- A typical gate driving circuit is as shown in Fig. 2.5.3(a).
- The totem-pole arrangement of the driver transistors Q_2 and Q_3 is for quick charging and discharging of the input capacitance of MOSFET.
- The signal from the control circuit is applied to the base of transistor Q_1 .



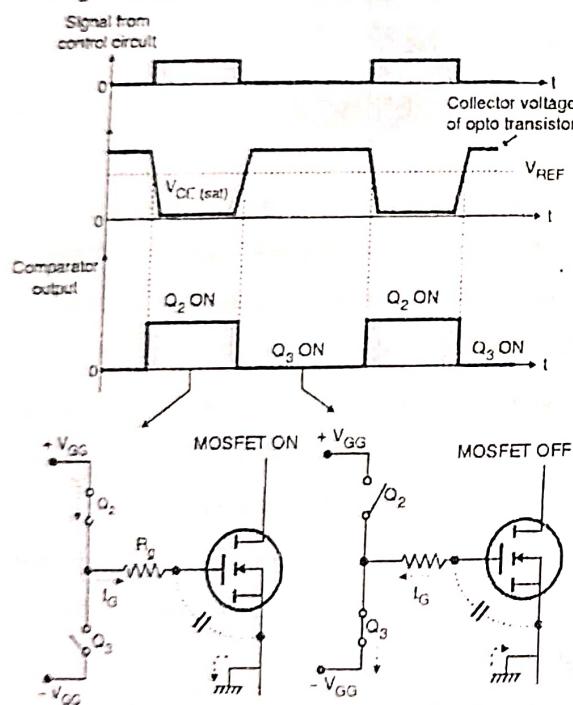
(a-426) Fig. 2.5.3(a)

- The opto coupler couples this signal to the input of the comparator.
- The opto coupler isolates the control circuit from the high power circuit.
- The comparator compares the output of opto coupler with a reference voltage and produces a waveform which has sharp rising and falling edges as shown in Fig. 2.5.3(b).
- The comparator output is used to turn-on and off the transistors Q_2 and Q_3 alternately.
- When Q_2 is on it turns ON the MOSFET whereas when Q_3 is turned on, it will turn the MOSFET off.
- The turn-on and turn-off time can be further reduced by using the **totem-pole arrangement** as shown in Fig. 2.5.3.
- The totem-pole arrangement of the transistors Q_2 and Q_3 ensure quick charging and discharging of the input capacitance of the power MOSFET.

- The reduction in turn-on and turn-off time is important because it helps to reduce the switching loss.
- The gate resistance R_g will suppress oscillations generated due to stray inductance.
- The driver circuit must be placed as close to the MOSFET as possible and the wires from the drive circuit to the MOSFET must be twisted in order to minimize the effect of EMI.
- The waveforms at various points and equivalent circuits are as shown in Fig. 2.5.3(b).
- The comparator output drives the transistors Q_2 and Q_3 . Transistor Q_2 is turned on when the comparator output is high and Q_3 is on for low comparator output.
- In this way the input capacitance of MOSFET is charged and discharged rapidly.

Waveforms :

- The waveforms of the gate driving circuit are as shown in Fig. 2.5.3(b).



(a-427) Fig. 2.5.3(b) : Waveforms and equivalent circuits

2.6 Ratings of Power MOSFET :

2.6.1 Absolute Maximum Ratings :

Definition :

- For power MOSFETs, the maximum allowable current, voltage, power dissipation and other characteristics are specified as maximum ratings.

- Maximum ratings must not be exceeded in order to guarantee the lifespan and reliability of devices.
- Maximum ratings are the highest absolute values that must not be exceeded even instantaneously under any conditions.
- The power MOSFETs are rated in terms of drain-to-source pin-to-pin voltage, power dissipation, operating temperature, and storage temperature.
- These characteristics are interrelated and cannot be considered separately.
- They also depend on external circuit conditions.
- Table 2.6.1 presents various absolute maximum ratings of a power MOSFET.

Table 2.6.1 : Absolute maximum ratings of power MOSFET

Sr. No.	Characteristic	Symbol	Unit	Description
1.	Drain-source voltage	V_{DSS}	V	The maximum voltage that can be applied across drain and source, with gate and source short circuited
2.	Gate-source voltage	V_{GSS}	V	The maximum voltage that can be applied across gate and source, with drain and source short circuited
3.	DC drain current	I_D	A	The maximum DC current that can pass through the drain to source
4.	Pulse drain current	I_{DP}	A	The maximum allowable peak drain current for pulsed operation
5.	Power dissipation ($T_c = 25^\circ C$)	P_D	W	The maximum power that can be dissipated by MOSFET
6.	Avalanche current	I_{AS}	A	The maximum peak non-repetitive current that is permitted under avalanche conditions
7.	Channel temperature	T_{CH}	°C	The maximum allowable chip temperature at which a MOSFET operates

Sl. No.	Characteristic	Symbol	Unit	Description
8.	Storage temperature range	T_{S0}	°C	The maximum temperature at which a MOSFET may be stored without voltage applying
9.	Isolation voltage	$V_{ISO(RMS)}$	V	The maximum voltage at which a MOSFET can maintain isolation between the designated point on the case and electrode leads

2.6.2 Different Ratings of Power MOSFET :

Refer Fig. 2.6.1 to understand the classification of various voltage and current ratings of a power MOSFET. MOSFET ratings are classified into voltage ratings, current ratings and other ratings.

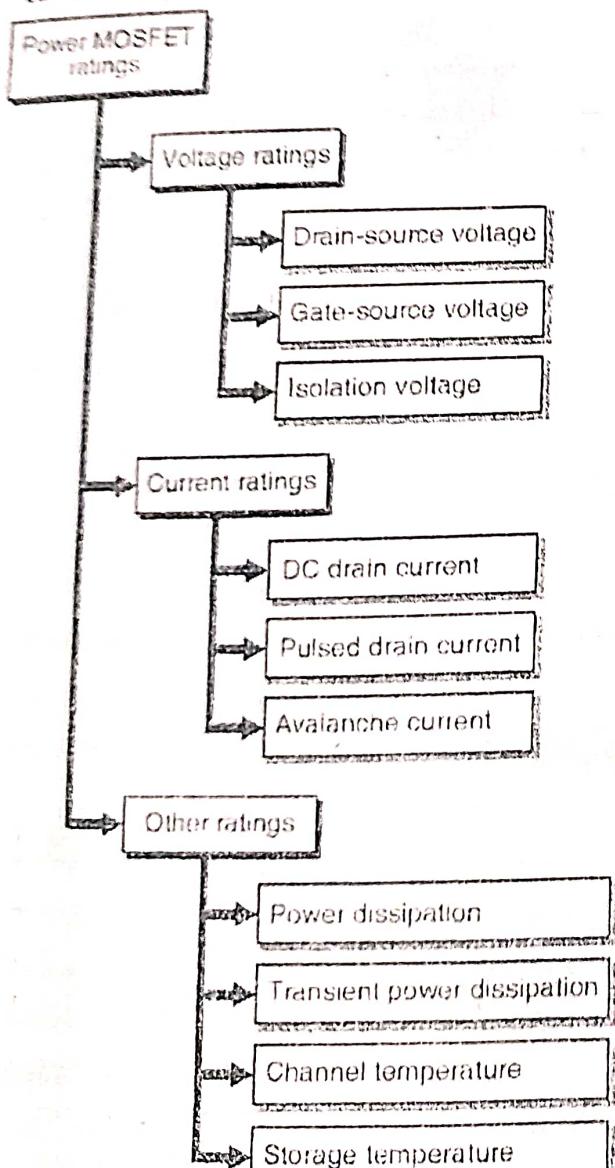


Fig. 2.6.1 : Classification of MOSFET ratings

2.6.3 Voltage Ratings :

- Following are the important voltage ratings of a power MOSFET :
 1. Drain-source voltage (V_{DSS})
 2. Gate-source voltage (V_{GSS})
 3. Isolation voltage (V_{ISO})
- 1. **Drain-source voltage (V_{DSS}) :**
 - The drain-source breakdown voltages of a power MOSFET are defined according to the gate-source bias conditions as follows :
 1. V_{DSS} : This is defined as the drain-source voltage with gate and source short-circuited ($V_{GS} = 0$). If we apply a drain-source voltage higher than the rated value, it may cause a MOSFET to enter the breakdown region and be permanently damaged.
 2. V_{DSX} : This is defined as the drain-source voltage with gate and source reverse-biased.
 3. In addition to V_{DSS} and V_{DSX} , two more voltage ratings V_{DSR} and V_{DSD} are also defined for power MOSFETs. (V_{DSR} is the drain-source voltage with a resistor inserted between gate and source. V_{DSD} is drain-source voltage with gate open-circuited.)
 - Due to the very high input impedance of power MOSFETs, they should not be used in V_{DSD} mode.
 - In this mode, the power MOSFETs are biased between gate and source due to electrostatic induction and enter the conduction mode.
 - Consequently, there is a high probability that they will be permanently damaged.
- 2. **Gate-source voltage (V_{GSS}) :**
 - V_{GSS} is defined as the maximum allowable gate-to-source voltage, when drain and source terminals are short-circuited.
 - The value of V_{GSS} depends on the dielectric strength of the gate oxide.
 - For MOSFETs, a permissible value is specified, taking practical voltage and reliability into consideration.
- 3. **Isolation voltage ($V_{ISO(RMS)}$) :**
 - For devices housed in a fully molded package, isolation voltage is defined as the level of electrical isolation between the designated point on the case and the internal circuit and electrode terminals.

- V_{DSRMS} is tested by applying AC voltage to the power MOSFET for a specified period of time. Isolation voltage is specified as the RMS value of the applied AC voltage.

2.6.4 Current Ratings :

- Following are the important current ratings of a power MOSFET :

1. DC drain current
2. Pulsed drain current
3. Avalanche current

1. DC drain current :

1. **Forward dc drain current (I_D)** : The forward dc drain current (I_D) is defined as the maximum continuous (DC) current that the power MOSFET can pass in the forward direction.

2. **Reverse dc drain current (I_{DR})** : It is defined as the maximum continuous (DC) current that the power MOSFET can pass in the reverse direction.

2. Pulsed drain current :

1. **Forward pulsed drain current (I_{DP})** : The forward pulsed drain current (I_{DP}) is defined as the maximum pulsed current that the power MOSFET can pass in the forward direction.

2. **Reverse pulsed drain current (I_{DPR})** : It is defined as the maximum pulsed current that the power MOSFET can pass in the reverse direction.

- Note that, the maximum current values in the forward direction depend on the power loss caused by drain-source on-state resistance, and those in the reverse direction are limited by the power loss due to the forward voltage across the anti-parallel diode.

3. Avalanche current (I_A) :

- When a power MOSFET operates at high speed as a switching device, a high surge voltage is applied across drain and source at the time of turn-off due to the self-inductance of a circuit and stray inductances.

- This surge voltage occasionally exceeds the rated voltage of the MOSFET, causing it to enter the breakdown region.

- At this time, avalanche current passes through the power MOSFET.

Avalanche current exceeding the current or energy limit causes permanent damage to the MOSFET. This phenomenon is called avalanche breakdown.

- The avalanche current I_A is defined as the maximum allowable avalanche current that can flow through a power MOSFET during the avalanche breakdown situation.

2.6.5 Other Ratings :

- Following are the important other ratings of a power MOSFET :

1. Power dissipation
2. Transient power dissipation
3. Channel temperature and
4. Storage temperature

1. Power dissipation :

- Power dissipation (PD) of a power MOSFET is defined as the maximum power that the MOSFET can dissipate continuously under the specified thermal conditions.

- The allowable power dissipation depends on the conditions under which the MOSFET is used (such as ambient temperature and heat dissipation conditions).

- We can calculate P_D as the maximum power dissipation for a device with an infinite heat sink at 25°C ambient as follows :

$$P_D = [T_{ch}(\max) - 25^\circ C] / R_{th(CH-C)} \quad \dots(2.6.1)$$

2. Transient power dissipation :

- P_{DP} , the maximum transient power dissipation, is calculated as follows using the transient thermal resistance value shown in individual MOSFET datasheets.

$$P_{DP} = [T_{ch}(\max) - 25^\circ C] / r_{th(CH-C)} \quad \dots(2.6.2)$$

3. Channel temperature :

- The channel temperature (T_{ch}) is defined as the maximum allowable chip temperature at which a MOSFET operates.

- The maximum channel temperature depends on the materials that constitute the power MOSFET and their reliability.

- The maximum channel temperature must be considered not only in terms of the functional operation of the power MOSFET, but also in terms of its reliability such as device degradation and lifetime.

4. Storage temperature :

- Storage temperature T_{sig} is the temperature range in which a power MOSFET can be stored without applying any voltage to it.

- The storage temperature range depends on the materials that constitute the power MOSFET and their reliability.

2.6.6 Safe-operating Area (SOA) of a Power MOSFET :

SPPU (May 19)

University Questions

- Q. 1** Describe the concept of safe operating areas of MOSFET & IGBT (May 19, 7 Marks)

Definition :

- The SOA is a graph of $\log V_{DS}$ on X-axis versus $\log I_D$ on Y-axis as shown in Fig. 2.6.2.
- In order to ensure a safe operation the device should not operate out of the SOA.
- Three factors determine the SOA of the MOSFET, I_{DM} the maximum drain current, T_j the junction temperature and the breakdown voltage $B V_{DSS}$.

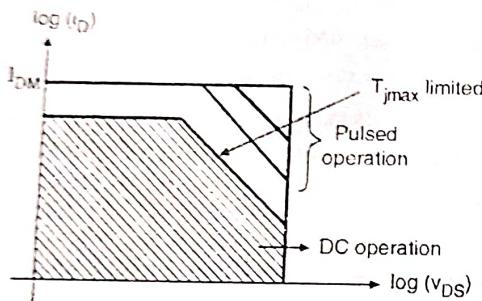


Fig. 2.6.2 : SOA of a n-channel enhancement mode MOSFET. Note that second breakdown is absent

- Note that the MOSFET does not have any second breakdown problem like BJT. The SOA for the DC operation is the shaded portion of Fig. 2.6.2 whereas for the switch mode applications the SOA is a square.
- The forward bias safe operating area (FBSOA) and the reverse bias safe operating area (RBSOA) for a power MOSFET are identical.

Conclusions :

- From the SOA it is evident that :
 - If the junction temperature (T_j) is increased then the MOSFET should be operated at reduced values of maximum drain current in order ensure safe operation.
 - DC operation means continuous operation of the device.

- For pulsed operation (discontinuous operation), the values of maximum drain currents would be higher than that for the continuous (DC) operation. As we reduce the pulse width the value of maximum drain current will increase without damaging the device.

2.7 Parallel Operation of MOSFETs :

- The SCRs have a negative temperature coefficient of resistivity. During current sharing if one SCR carries more current then its on state resistances decreases and its current increases further.
- This leads to the thermal runaway. Therefore forced equal current sharing and operating all the parallelly connected thyristors at the same temperature by mounting them on a common heat sink would help to have a safe operation.

Parallel operation of power MOSFETs :

- Due to the positive temperature coefficient, the parallel connection of power MOSFETs is much easier as compared to that of the power BJTs.
- In the parallel connection of two power MOSFETs if one of them draws more current than the other, its internal temperature will increase, this will increase its on state resistance, and will automatically reduce the current through it.
- In this way direct paralleling of power MOSFETs is possible and much easier as well.
- While paralleling the power MOSFETs it is necessary to take precautions to keep the parasitic oscillations as low as possible.
- For this the resistance in series with gate terminals must be chosen properly, also the gate driving circuit with a low output impedance must be used.
- All the equations derived for the forced current sharing in thyristors are applicable to the parallel operation of power MOSFETs.

Direct paralleling of power MOSFETs :

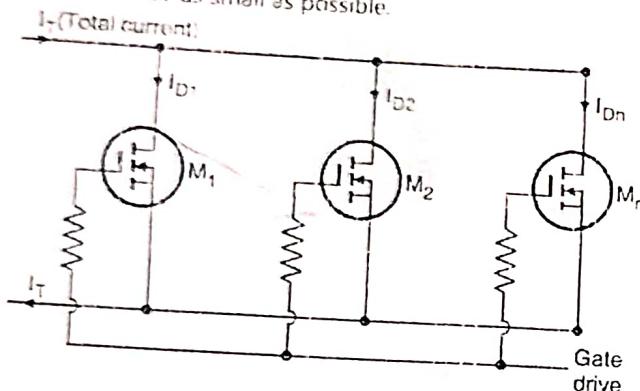
- The power devices like power transistors, power MOSFETs, IGBTs can be connected in parallel, directly that is without using any forced current sharing circuits.
- In case of power transistors, the collectors of all the transistors are connected together.

If the percent derating is known, then we can calculate the number of devices required to be connected in parallel.

Derating increases the reliability of the parallel connection.

2.7.1 Merits of a Power MOSFET

1. The input resistance of MOSFETs is high. They are voltage controlled devices. Therefore the driving circuit for MOSFET is simpler.
2. Power MOSFETs can operate at high switching frequency (typically up to 100 kHz). This is due to the fact that they are majority carrier devices.
3. The second breakdown does not take place in power MOSFETs.
4. MOSFETs have a positive temperature coefficient of resistivity. Therefore they are the easiest device to parallel.
5. Due to positive temperature coefficient, MOSFETs have a better thermal stability (no thermal runaway).
6. It is easy to turn-on and off the power MOSFET.
7. Due to very high input resistance, the power MOSFET requires extremely small input power, hence it can be driven from CMOS logic gate, shown in Fig. 2.7.2.

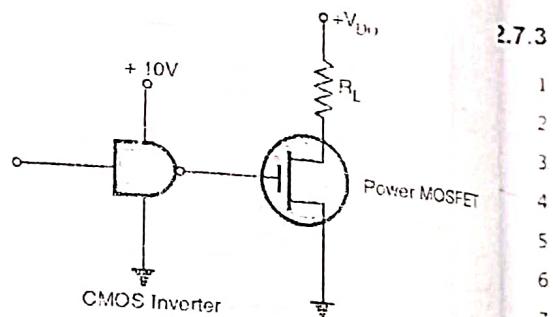


(I-430) Fig. 2.7.1 : Direct parallel connection of power MOSFETs

String Efficiency and Derating :

- The string efficiency for the parallel string is defined as,
- $$\eta_p = I_m / n_p I_f \quad \dots(2.7.1)$$
- Where, I_m = Total forward current
- n_p = Number of devices in parallel
 - I_f = Forward current rating of each MOSFET.
 - The string efficiency is reduced by using more number of devices in the parallel string than actually required because this will improve the reliability of the string.
 - This will derate the devices and the percent derating is given by,

$$\% \text{Derating for parallel connection, } D_p = \left(1 - \frac{I_m}{n_p I_f} \right) \times 100 \% \quad \dots(2.7.2)$$

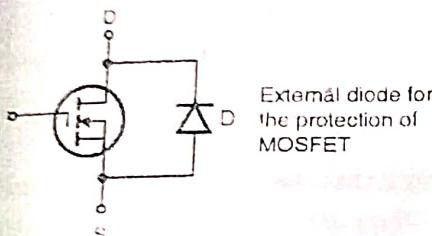


(I-428) Fig. 2.7.2 : A power MOSFET can be easily driven by CMOS inverter

8. The on-state resistance $R_{DS(on)}$ is extremely small.
9. Power MOSFETs have very low noise figures. So they are less noisy devices as compared to power BJT.
10. The threshold voltage $V_{GS(th)}$ ranges from 0.8 to 2 V. Hence MOSFET devices are compatible with TTL logic.
11. Due to the drift layer the breakdown voltages of power MOSFETs are high as compared to small signal MOSFET.

2.7.2 Demerits of a Power MOSFET :

1. The on-state voltage across a power MOSFET is high. Therefore the on-state power dissipation is very high as compared to that of a power transistor.
2. Power MOSFETs need special care while handling otherwise they can get damaged due to static electricity.
3. Power MOSFETs have asymmetric blocking capacity. They can block a high forward voltage but they cannot block high reverse voltage. Therefore to protect the power MOSFET we need to connect a diode across the MOSFET as shown in Fig. 2.7.3.



(0-429) Fig. 2.7.3

2.7.3 Applications of Power MOSFETs :

1. In high frequency inverter.
2. In the Switched Mode Power Supplies (SMPS).
3. In Uninterruptable Power Supplies (UPS).
4. In the output stage of audio or RF power amplifier.
5. Industrial process control.
6. Motor control applications.
7. Solenoid or relay driver.
8. Display driver.

2.8 Insulated Gate Bipolar Transistor (IGBT) :

SPPU Dec 15

University Questions

Q. 1 What is IGBT ? Explain with characteristics.

(Dec. 15, 6 Marks)

The power BJT has advantage of low on-state power dissipation, but it cannot be switched at faster rates due to longer turn-off time.

The power MOSFET can be switched at much higher frequency but has a drawback of higher on-state power loss.

- Therefore attempts were made to combine BJTs and MOSFETs monolithically on the same silicon wafer to develop a new device that will have the best qualities of both, BJT and MOSFET.
- The new device is known as Insulated Gate Bipolar Transistor (IGBT).
- Other names to this device are GEMFET, COMFET (conductivity modulated field effect transistor), IGT (Insulated Gate Transistor) and bipolar mode MOSFET or bipolar MOS transistor.

2.8.1 Features of IGBT :

- The important features of IGBT are as follows :
 1. Low on-state voltage drop.
 2. Low on-state power loss.
 3. It has a higher switching frequency than that of a power BJT.
 4. IGBT has the best qualities of BJT and MOSFET.

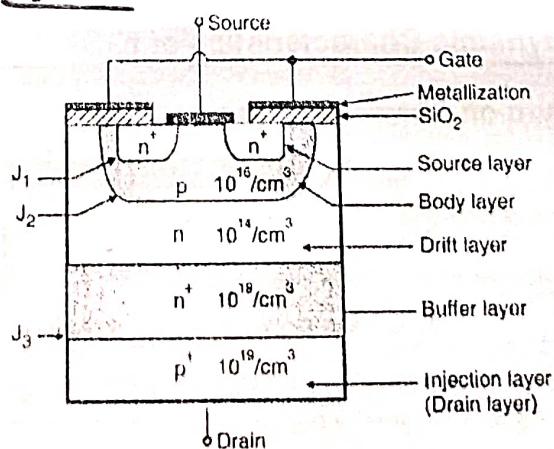
2.9 Construction of IGBT :

SPPU May 06, Dec 06, Dec 10,
May 13, Dec 13, Dec 15

University Questions

- Q. 1** Draw the vertical cross-section of an IGBT.
(May 06, Dec. 06, Dec. 10, 2 Marks)
- Q. 2** Draw construction diagram of IGBT and explain its switching characteristics. (May 13, 7 Marks)
- Q. 3** Draw construction diagram and explain switching characteristics of IGBT. (Dec. 13, 7 Marks)
- Q. 4** What is IGBT ? Explain with characteristics.
(Dec. 15, 6 Marks)

- The vertically oriented structure of IGBT is as shown in Fig. 2.9.1(a).

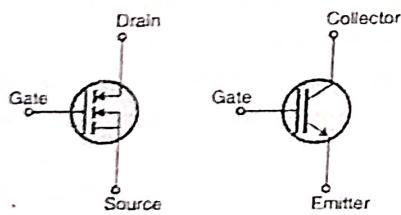


(0-431) Fig. 2.9.1(a) : Vertically oriented structure of IGBT, with doping densities

- Like all other devices IGBT also uses the vertically oriented structure in order to maximize the area available for the current flow.
- This will reduce the resistance offered to the current flow and hence the on-state power loss taking place in the device.
- The IGBT also uses highly interdigitated gate-source structure in order to reduce the possibility of source/emitter current crowding.**
- The doping levels used in different layers of IGBT are similar to those used in the comparable layers of the power MOSFET structures except for the body region.
- The main difference in the structure of IGBT as compared to that of a MOSFET is the existence of p^+ (injection layer or drain layer) layer that forms the drain of the IGBT.
- This device also uses the n^- type drain drift layer which improves its breakdown voltage capacity. This is same as that in case of power MOSFETs.
- It is also possible to make a p -channel IGBT by changing the doping type in each of the layers of the device.
- The n^+ buffer layer is not a must (It is an optional layer) for the operation of the IGBT and some IGBTs do not have it. (Sometimes IGBTs without a buffer layer are known symmetric IGBTs whereas those with the buffer layer are called as asymmetric IGBTs).**
- The n^+ buffer layer improves the operation of IGBT in two important aspects :
 1. It reduces the on-state voltage drop across the device and
 2. It shortens the turn-off time. But the drawback is that the buffer layer reduces the reverse blocking capacity of the IGBT to a great extent.

Circuit symbol for IGBT :

- The circuit symbols for an n -channel IGBT are as shown in Figs. 2.9.1(b) and (c).



(a-431) Fig. 2.9.1(b) and (c) : Circuit symbols for the n-channel IGBT

- As seen from the Figs. 2.9.1(b) and (c), IGBT is a three terminal device, gate being the control terminals. The directions of the arrowheads will reverse in a p -channel IGBT.
- The symbol shown in Fig. 2.9.1(b) is almost identical to that used for the n -channel power MOSFET, but with the addition of an arrowhead in the drain terminal pointing into the device.
- The symbol shown in Fig. 2.9.1(c) is used if IGBT is considered to be basically a BJT with MOSFET gate input.
- This device has a collector and emitter instead of a drain and source. The controlling terminal however is gate (G).
- This symbol indicates that the IGBT has output characteristics similar to power BJT and input characteristics similar to the power MOSFET.

2.9.1 Principle of Operation of IGBT :

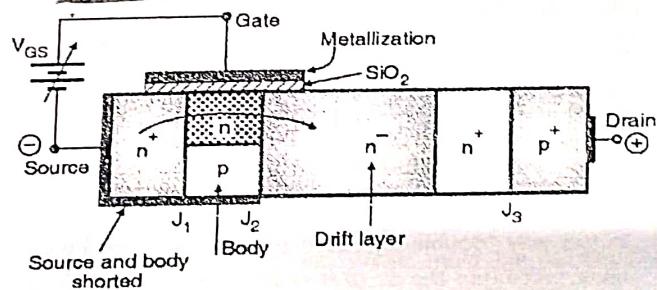
- The principle of operation of IGBT is similar to that of a MOSFET. The operation can be divided into two parts :

1. Creation of the inversion layer and
2. Conductivity modulation.

1. Creation of inversion layer :

- The operation of IGBT is based on the principle of creation of inversion layer which is same as that for the power MOSFET.**

- In IGBTs also when the positive gate to source voltage V_{GS} is greater than V_{GS} (threshold), n^- type inversion layer is created beneath the SiO_2 (oxide) layer as shown in Fig. 2.9.2(a).



n type inversion layer formed in the P type body layer, due to which a channel is formed for the conduction of current

(I-435) Fig. 2.9.2(a) : Creation of an inversion layer

- Due to the formation of n^- type induction layer in the p -type body layer, a channel is formed ($n^+ n^- n^-$) which helps to establish the electron current as shown in Fig. 2.9.2(a).

- The only difference between the MOSFET and IGBT is that there is no "conductivity modulation" of drift layer in MOSFET.
- Therefore the on-state resistance $R_{DS(on)}$ and hence the on-state power loss is very high in MOSFET.
- In IGBT however the conductivity modulation takes place which reduces the on state loss as explained as follows :

2. Conductivity modulation :

- In IGBT the conductivity modulation of the n^- drift layer takes place.
- The effect of conductivity modulation is reduction in the on-state resistance and hence the on-state power loss. Therefore the on-state losses in IGBT are less than that in MOSFET.
- The conductivity modulation in the n^- drift layer can be explained with the help of Figs. 2.9.2(a) and (b).
- Due to the application of forward voltage between drain (collector) and source (emitter) the junction J_3 is forward biased.
- Due to the creation of inversion layer, electrons from the source are injected into the n^- drift layer via the $n^- p n$ channel (Refer to Fig. 2.9.2(b)).

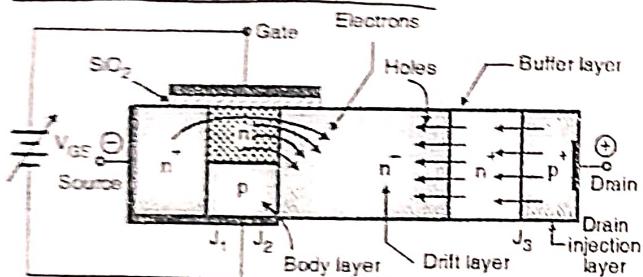


Fig. 2.9.2(b) : Conductivity modulation in IGBT

- As the junction J_3 is already forward biased, it will inject holes into the n^- buffer layer from p^+ layer.
- The electrons injected in the n^- drift layer create a space charge which will attract holes from the n^- buffer layer which were injected by the p^+ layer.
- In this way "double injection" (of electrons and holes) takes place into the n^- drift region from both sides as shown in Fig. 2.9.2 (b).
- This increases the conductivity of the drift region and reduces the resistance to its minimum. In this way the conductivity modulation will reduce the on-state voltage across the IGBT.

2.10 Static (I-V) Characteristic of IGBT :

SPPU Dec 06, Dec 10 May 13
Dec 13, Dec 16, Dec 16 March 19

University Question

- Q. 1 Draw the V-I characteristics of IGBT.
(Dec. 06, 2 Marks)
- Q. 2 Explain output characteristics of vertical cross section of IGBT.
(Dec. 10, 4 Marks)
- Q. 3 Draw construction diagram of IGBT and explain its switching characteristics.
(May 13, Dec. 13, 7 Marks)
- Q. 4 What is IGBT ? Explain with characteristics.
(Dec. 15, 6 Marks)
- Q. 5 Draw and explain steady state characteristics of IGBT
(Dec. 16, 7 Marks)
- Q. 6 Draw the V-I characteristics of IGBT. Mark & explain various operating regions & SOA of the IGBT.
(March 19, 4 Marks)

- The I-V characteristics of IGBT is as shown in Fig. 2.10.1.

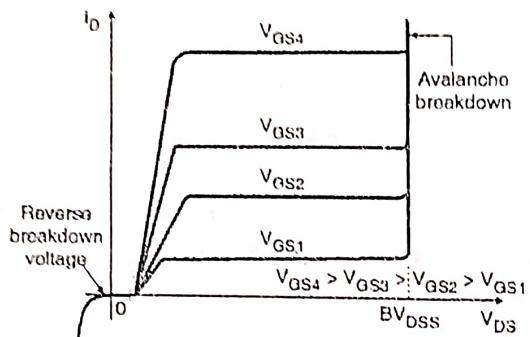


Fig. 2.10.1 : IGBT I-V characteristics

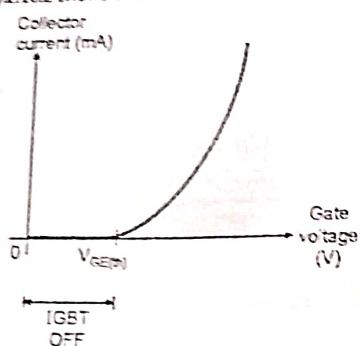
- In the forward direction they are similar to those of the logic level bipolar transistor, the only difference here is that the controlling parameter is the gate to source voltage V_{GS} , and the parameter being controlled is the drain current.
- Thus IGBT is a voltage controlled device with an insulated gate.
- The drain current increases with increase in V_{GS} at a constant value of V_{DS} .
- The IGBT possesses all the advantages of MOSFET due to the insulated gate. It also has all the advantages of the BJT due to bipolar conduction.
- As seen from the Fig. 2.10.1, the drain current (or the collector current) increases with increase in the voltage between gate and source (V_{GS}).
- Also note that the gate to source voltage V_{GS} is positive. BV_{DSS} is the forward breakdown voltage.

- This is the value of V_{GS} at which the avalanche breakdown takes place.
- At this point the voltage across the device and current through it both are high.
- Therefore the power dissipated in the device will be very large and will damage it. The device must be therefore operated below this voltage.

2.10.1 Transfer Characteristic of IGBT :

Definition :

- The transfer characteristic of an IGBT is a plot of collector current versus the gate voltage. The transfer characteristics of IGBT and MOSFET are similar.
- Fig. 2.10.2 shows the transfer characteristic of IGBT.



(G-2959(a)) Fig. 2.10.2 : Transfer characteristic of IGBT

- The IGBT is in the off-state if the gate-emitter potential is below the threshold voltage.
- For gate voltages greater than the threshold voltage the transfer curve is linear over most of the collector-current range.
- Gate oxide breakdown and the maximum IGBT collector current limit the maximum gate-emitter voltage.

2.11 Dynamic Characteristics of IGBT :

2.11.1 Turn-on Characteristics :

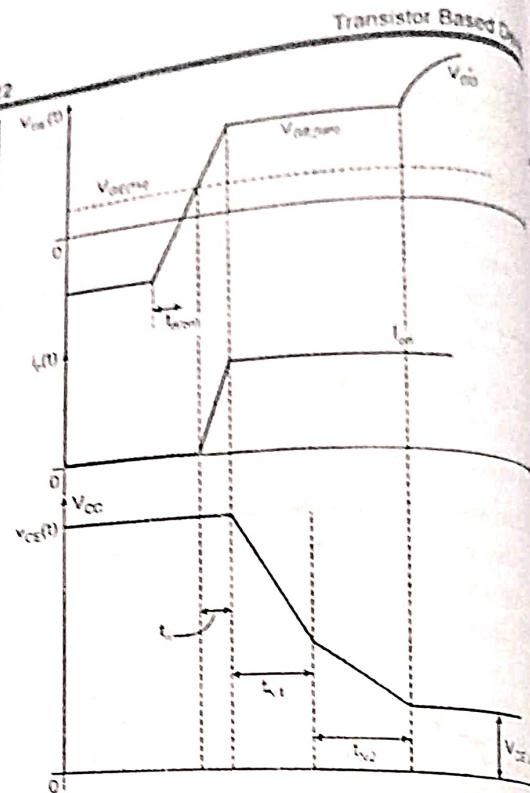
SPPU Dec 15, Aug 17

University Questions

- Q. 1 Explain switching characteristics of an IGBT.

(Dec. 15, 8 Marks, Aug. 17, 5 Marks)

- The switching waveforms of an IGBT during the process of turn on in a clamped inductive circuit are shown in Fig. 2.11.1.



(G-2957) Fig. 2.11.1 : The IGBT turn-on characteristics

The inductance-to-resistance (UR) time constant of an inductive load is assumed to be large compared to the switching frequency and therefore can be considered a constant current source I_∞ . The IGBT turn on switch performance is determined by its MOS input structure.

During t_{on} , the gate current charges the constant capacitance of the device, with a constant slope until the gate-emitter voltage reaches the threshold voltage $V_{GE(th)}$ of the device.

During the time duration t_1 , load current is transferred from the diode into the device and the collector current increases to its steady-state value.

The slope of this current and therefore t_1 is determined by the gate voltage rise time and transconductance.

As soon as the gate-emitter voltage reaches $V_{GE(on)}$ that will support the steady-state collector current $I_{C(on)}$, the collector-emitter voltage starts to decrease.

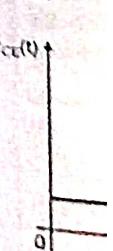
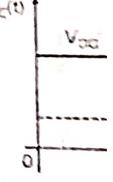
After this instant, there are two distinct intervals during IGBT turn-on.

In the first interval the collector-to-emitter voltage drops rapidly as the gate-drain capacitance C_{GD} of the MOSFET portion of IGBT discharges.

2.11.2 Turn-off Characteristics :

University Q. 1 Explain

Fig. 2.11.2 Turn-off voltage. Voltage voltage collector



(G-2958)

- At low collector-emitter voltage C_{dd} increases. A finite time is required for high-level injection conditions to set in the drift region.
- The p-n-p transistor portion of IGBT equivalent circuit has a slower transition to its on state than the MOSFET.
- The gate voltage starts rising again only after the transistor comes out of its saturation region into the linear region, when complete conductivity modulation occurs and the collector-emitter voltage reaches its final on state value.

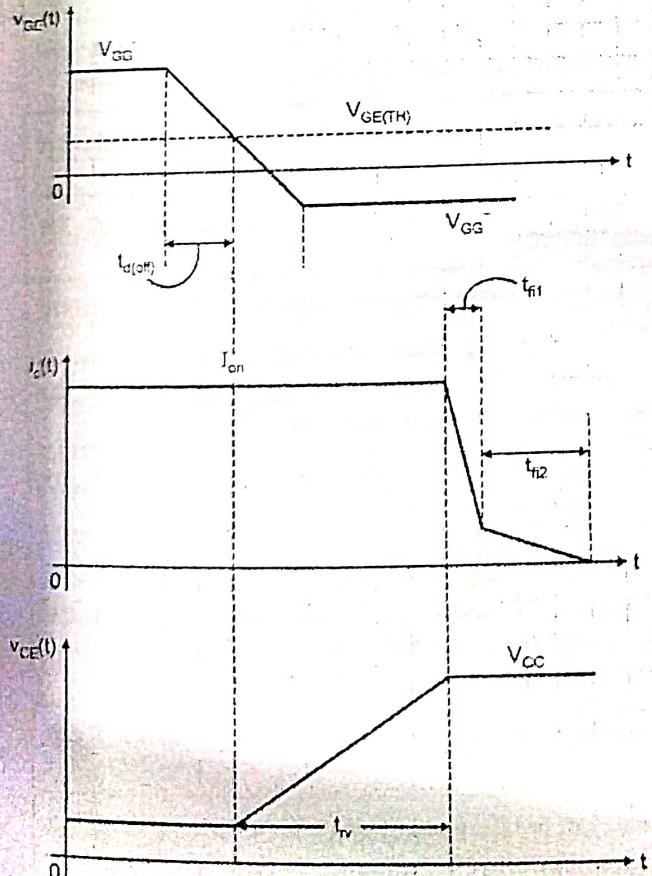
2.11.2 Turn-off Characteristics :

SPPU Dec. 15, Aug. 17

University Questions

Q. 1 Explain switching characteristics of an IGBT.
(Dec. 15, 8 Marks, Aug. 17, 5 Marks)

- Fig. 2.11.2 shows the turn off characteristics of an IGBT.
- Turn-off is initiated by removing the gate-emitter voltage.
- Voltage and current remain constant until the gate voltage reaches $V_{GE(on)}$ required to maintain the collector steady-state current as shown in Fig. 2.11.2.



(G-2958) Fig. 2.11.2 : The IGBT turn-off characteristics

- After this delay time ($t_{d(on)}$) the collector voltage rises, while the current is held constant.
- The gate resistance determines the rate of collector-voltage rise. As the MOS channel turns off, collector current decreases sharply during t_{f1} .
- The turn off delay time $t_{d(off)}$ and the voltage rise time t_{rV} is decided by the MOSFET portion of IGBT.
- When the collector voltage reaches the dc supply voltage, the freewheeling diode starts to conduct.
- However, the excess stored charge in the n-drift region during on-state conduction must be removed in order to turn off the device.
- The high minority-carrier concentration stored in the n-drift region supports the collector current after the MOS channel is turned off.
- Due to recombination of the minority carriers in the wide-base region the collector current decreases gradually, which results in a current tail.
- Because there is no access to the base of the p-n-p transistor in the equivalent circuit of IGBT, the excess minority carriers cannot be removed by reverse-biasing the gate.
- The t_{f2} interval is long because the excess carrier lifetime in this region is normally kept high to reduce the on-state voltage drop.
- In this interval, the collector-emitter voltage has reached the bus voltage. Therefore, a significant power loss occurs that increases with frequency.
- Therefore, the current tail limits the IGBT operating frequency and there is a trade-off between the on-state losses and faster switching times.
- For an on-state current of I_{on} , the magnitude of current tail, and time required for the collector current to decrease to 10% of its on-state value i.e. the turn-off (t_{off}) time, are approximated as:

$$I_c(t) = \alpha_{pnp} I_{on} e^{-(t/t_{HL})} \quad \dots(2.11.1)$$

$$t_{off} = \tau_{HL} \ln(10 \alpha_{pnp}) \quad \dots(2.11.2)$$

Where,

$$\alpha_{pnp} = \operatorname{sech}\left(\frac{l}{L_a}\right) \quad \dots(2.11.3)$$

α_{pnp} is the gain of the bipolar pnp-transistor, l is the undepleted base width and L_a is the ambipolar diffusion length and it is assumed that the high-level lifetime (τ_{HL}) is independent of the minority carrier injection during the collector current decay.



- Lifetime control techniques are used to reduce the lifetime (t_{HL}) and the gain of the bipolar transistor (α_{FNP}).
- As a result the magnitude of the current tail and t_{on} decrease.
- However, the conductivity modulation decreases, which increases the on-state voltage drop in the drift region. Therefore, higher speed IGBTs have a lower current rating.

2.12 IGBT Driving Circuits :

SPPU Dec. 10, May 13

University Questions

Q. 1 Draw and explain Gate Drive Circuit for IGBT.
(Dec. 10, 6 Marks; May 13, 5 Marks)

- The gate driving requirements for the IGBT and MOSFET are almost identical due to the fact that both these devices have the same structure on their input side i.e. between gate and source terminals.
- The IGBT also is therefore a voltage controlled device and to turn it on, sufficient positive voltage must be applied between its gate and source terminals.
- It has large input capacitance between its gate and source terminals, therefore the driver circuit must have a low output resistance, in order to minimize the turn-on and turn off time.
- A totem pole arrangement of driver transistors will satisfy all these requirements as shown in Fig. 2.12.1(a).
- A current sensing circuit is essential and as soon as the device current exceeds the rated value the gate drive to the IGBT must be blocked.
- This is the only way to protect the IGBT, as a fuse can not protect it.
- The isolation between control and power circuit can be provided by using an opto coupler.
- Nowadays IGBT and MOSFET driver circuits are available in IC form.
- The ICs available in the market are IR 2125 a single MOS driver and IR 2110 a double MOS driver IC.
- These ICs include all the desired features of an IGBT driver. The driver circuit requirements and precautions are as discussed below.

2.12.1 IGBT Drive Circuit Requirements :

SPPU Dec. 10, May 13, May 17

University Questions

- Q. 1** Draw and explain Gate Drive Circuit for IGBT.
(Dec. 10, 6 Marks, May 13, 5 Marks)
- Q. 2** Draw the circuit diagram of Gate Drive circuit for IGBT. Explain its operation. (May 17, 6 Marks)

- The gate circuit requirements of an IGBT are as follows.

1. Drive voltage :

- The IGBT is a voltage controlled device and has a high input capacitance between its gate and source terminals (like MOSFET).
- The on-state voltage across the IGBT depends largely on the gate to source voltage (V_{GS}). Therefore to keep the on-state voltage low a high positive gate to source voltage must be applied.
- However this voltage should not exceed the breakdown voltage of gate. Considering all these points the V_{GS} to be applied to the IGBT to turn it on must be about 15 Volts.
- During the off-state of IGBT a negative gate to source voltage must be applied to avoid malfunctioning of the IGBT. The reverse voltage should be greater than 2 Volts and typically it is 5 Volts.

2. Apply V_{GS} continuously :

- Adequate gate to source voltage must be applied "continuously" to the device during its on time. The IGBT like BJT and MOSFET will turn off as soon as the gate to source voltage is reduced to zero or removed.

3. Large output current of drive circuit :

- The output current of the drive circuit should be large enough to "charge" and "discharge" the gate source capacitance as quickly as possible.
- This will help in reducing the turn-on and turn off time for the IGBT, and hence reduce the switching losses taking place in the device.

4. Provide electrical isolation :

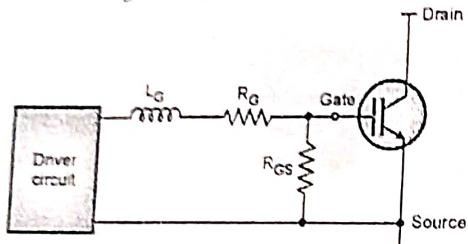
- The IGBT and its control circuit must be electrically isolated. The isolation can be provided by using either an opto isolator or a pulse transformer.
- Opto isolator is suitable for PWM applications where the pulse duration changes over a wide range, whereas the pulse transformers are suitable for high frequency switching with an ON/OFF ratio of 50% or less (to avoid saturation of the core of pulse transformer).

5. Drive circuit wiring should be short in length :

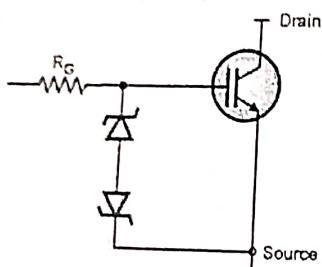
- The wiring from the drive circuit to IGBT must be as short as possible to avoid oscillations at the IGBT gate.
- The wires must be twisted to minimize the EMI.
- To protect against oscillation feedback, either increases the value of gate resistance R_G or reduce the value of gate to source resistance (R_{GS}). [See Fig. 2.12.1(a)]

6. Provide Gate over voltage protection :

- The IGBT gate to source breakdown voltage is ± 20 Volts.
- In order to protect the gate against accidental application of higher voltage than ± 20 Volts, zener diodes are connected between gate and source as shown in Fig. 2.12.1(b).



(a) Prevention of gate signal oscillations



(b) Gate over voltage protection

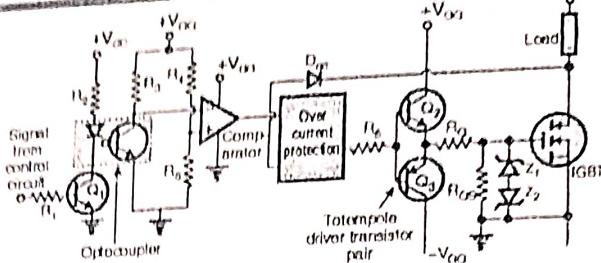
(I-442) Fig. 2.12.1

7. Over current protection must be included :

- The drain (collector) current of IGBT must be sensed by a current sensing circuit, and as soon as the drain current exceeds the maximum predefined safe value, the gate drive to the IGBT must be blocked.
- This is the only way to protect the IGBT as a fuse cannot protect it.

2.12.2 IGBT Driver Circuit :

- Fig. 2.12.2 shows the block diagram of the IGBT driver circuit, that fulfills all the requirements that are discussed so far.



(I-443) Fig. 2.12.2 : IGBT driver circuit

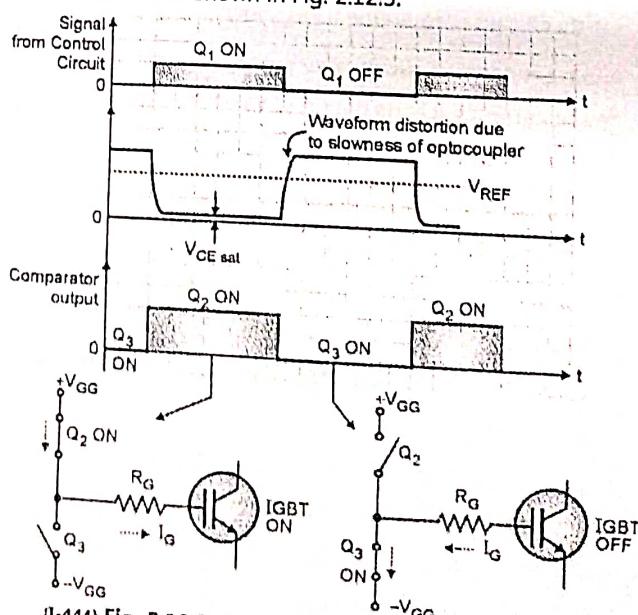
Operation of the driver :

- The diode D_{OC} in Fig. 2.12.2 is conducting under the normal operating conditions, and the comparator output is passed as it is to the totem-pole driver circuit consisting of transistors Q_2 and Q_3 . But as soon as the over current condition arises, the drain to source voltage increases rapidly, this will reverse bias the diode D_{OC} .
- As soon as D_{OC} is turned off, the comparator output is not allowed to pass through to the totem-pole driver circuit and the IGBT is quickly turned off.
- Thus by blocking the gate drive in the event of overcurrent we can protect an IGBT.
- Table 2.12.1 summarizes the operation of the overcurrent circuit.

Table 2.12.1

Operating condition	D_{OC} status	Gate drive
Normal $I_d < I_{d(\max)}$	Conducting	ON
Overcurrent $I_d > I_{d(\max)}$	OFF	Inhibited

- The waveforms and equivalent circuits for the drive circuit are as shown in Fig. 2.12.3.



(I-444) Fig. 2.12.3 : Waveforms and equivalent circuit

- The relation between drain to source voltage and drain current is as shown in Fig. 2.12.4. When a short circuit occurs, the IGBT drain current increases.

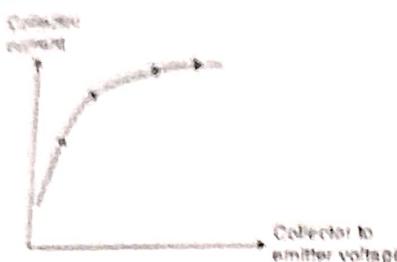


Fig. 2.12.4 : IGBT short circuit operation locus

- When it exceeds a critical value, the drain to source voltage increases rapidly. This increased voltage is an indication of over current.

2.13 Ratings of IGBT :

2.13.1 Maximum Ratings :

Definition :

- For IGBTs, the maximum allowable current, voltage, power dissipation, and other parameters are specified as maximum ratings.

- The maximum ratings of IGBTs must not be exceeded to ensure the expected useful life and reliability.
- The maximum ratings are limited by the circuit design, and manufacturing conditions, therefore differ from device to device.
- The absolute maximum ratings are the highest values that must not be exceeded during operation instantaneously.
- Exposure to a condition exceeding a maximum rating sometimes causes permanent degradation of electrical characteristics.

2.13.2 Absolute Maximum Ratings :

- All parameters are specified at 25°C ambient unless otherwise noted.
- Table 2.13.1 presents various absolute maximum ratings of a power MOSFET.

Table 2.13.1 : Absolute maximum ratings of IGBT

Sr. No.	Characteristic	Symbol	Unit	Definition
1.	Collector-emitter voltage	V_{CES}	V	The maximum allowable voltage that can be applied across collector and emitter, with gate and emitter short-circuited
2.	Gate-emitter voltage	V_{GES}	V	The maximum voltage that can be applied across gate and emitter, with drain and source short-circuited
3.	DC collector current	I_C	A	The maximum DC current that can pass through collector to emitter
4.	Pulsed collector current	I_{CP}	A	The maximum allowable peak collector current for pulsed operation
5.	Diode forward current	I_F	A	The maximum DC current that can flow through freewheeling diode in the forward direction
6.	Diode forward current (pulsed)	I_{FP}	A	The maximum pulsed current that can flow through freewheeling diode in the forward direction
7.	Collector Power dissipation	P_c	W	The maximum power that can be dissipated by an IGBT
8.	Short-circuit withstand time	t_{sc}		The maximum allowable period of time during which a device can be short-circuited under the specified conditions and after which it normally returns to the off state
9.	Junction temperature	T_j	°C	The maximum junction temperature at which an IGBT may operate
10.	Storage temperature range	T_{stg}	°C	The maximum temperature at which an IGBT may be stored without applying voltage or current

2.13.3 Voltage Ratings :

The voltage ratings of an IGBT are as follows :

1. Collector-emitter voltage
2. Gate-emitter voltage

1. Collector-emitter voltage (V_{ces}) :

The continuous collector-to-emitter voltage (V_{ces}) is defined as the maximum voltage that the collector-to-emitter junction can support at temperature of 25 °C, when gate and emitter terminals are shorted together.

2. Gate-to-emitter voltage (V_{GE}) :

- V_{GE} is defined as the allowable range of voltage between the gate and emitter terminals.
- Exceeding V_{GE} range may result in permanent device degradation due to oxide breakdown and dielectric rupture.
- Remaining within these ratings assures application reliability. This value, with reasonable guard band, is 100% tested and warranted.

2.13.4 Current Ratings :

The important current ratings of an IGBT are as follows :

1. DC Collector current
2. Pulsed collector current

1. DC (continuous) collector current :

It is defined as the maximum value of continuous or dc collector current that can flow through an IGBT at 25°C. This value depends on the temperature. With rise in temperature the maximum continuous current rating needs to be reduced for safety of device.

2. Pulsed collector current :

It is defined as the maximum allowable peak collector current for pulsed operation.

This rating indicates how much pulsed current the device can handle, which is significantly higher than the rated continuous current.

It is denoted by I_{CP} , the pulse width is limited by maximum junction temperature.

2.13.5 Other Ratings :

The other important ratings of an IGBT are as follows :

1. Collector power dissipation

2. Short-circuit withstand time

3. Junction temperature
4. Storage temperature range

1. Collector power dissipation :

- It is defined as the maximum power that can be dissipated by an IGBT at 25°C.
- Its value depends on the temperature. With increase in temperature we need to reduce the maximum power dissipation rating for safe operation of the device. This is known as derating of devices.

2. Short-circuit withstand time :

- It is defined as the maximum allowable time during which the device can be short-circuited under the specified conditions and after which it normally returns to the off state.

3. Junction temperature :

- It is defined as the range of junction temperatures over which an IGBT can operate. It is denoted by T_J .
- Usually, the junction temperature range of an IGBT is -55°C to 150°C.
- These limits are set to assure an acceptable lifetime of the product. Operating out of the temperature limits could damage the device affecting its lifetime.
- A reduction of operating junction temperature, every 10 °C doubles the device lifetime.

4. Storage temperature range :

- It is defined as the temperature range over which an IGBT may be stored without applying voltage or current.
- Usually, the storage temperature range of an IGBT is -55°C to 175°C.
- These limits are set to assure an acceptable lifetime of the product. Operating out of the temperature limits could damage the device affecting its lifetime.
- A reduction of operating junction temperature, every 10 °C doubles the device lifetime.

2.13.6 Safe Operating Area (SOA) of IGBT :

SPPU : March 19, May 19

University Questions

- Q. 1 Draw the V-I characteristics of IGBT. Mark & explain various operating regions & SOA of the IGBT. (March 19, 4 Marks)

2.13.3 Voltage Ratings :

The voltage ratings of an IGBT are as follows :

1. Collector-emitter voltage
2. Gate-emitter voltage

1. Collector-emitter voltage (V_{ces}) :

The continuous collector-to-emitter voltage (V_{ces}) is defined as the maximum voltage that the collector-to-emitter junction can support at temperature of 25 °C, when gate and emitter terminals are shorted together.

2. Gate-to-emitter voltage (V_{geo}) :

V_{geo} is defined as the allowable range of voltage between the gate and emitter terminals.

Exceeding V_{geo} range may result in permanent device degradation due to oxide breakdown and dielectric rupture.

Remaining within these ratings assures application reliability. This value, with reasonable guard band, is 100% tested and warranted.

2.13.4 Current Ratings :

The important current ratings of an IGBT are as follows :

1. DC Collector current
2. Pulsed collector current

1. DC (continuous) collector current :

It is defined as the maximum value of continuous or dc collector current that can flow through an IGBT at 25°C.

This value depends on the temperature. With rise in temperature the maximum continuous current rating needs to be reduced for safety of device.

2. Pulsed collector current :

It is defined as the maximum allowable peak collector current for pulsed operation.

This rating indicates how much pulsed current the device can handle, which is significantly higher than the rated continuous current.

It is denoted by I_{CP} the pulse width is limited by maximum junction temperature.

2.13.5 Other Ratings :

The other important ratings of an IGBT are as follows :

1. Collector power dissipation

2. Short-circuit withstand time

3. Junction temperature

4. Storage temperature range

5. Collector power dissipation :

- It is defined as the maximum power that can be dissipated by an IGBT at 25°C.
- Its value depends on the temperature. With increase in temperature we need to reduce the maximum power dissipation rating for safe operation of the device. This is known as **derating** of devices.

2. Short-circuit withstand time :

- It is defined as the maximum allowable time during which the device can be short-circuited under the specified conditions and after which it normally returns to the off state.

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- A reduction of operating junction temperature, every 10 °C doubles the device lifetime.

2.13.6 Safe Operating Area (SOA) of IGBT :

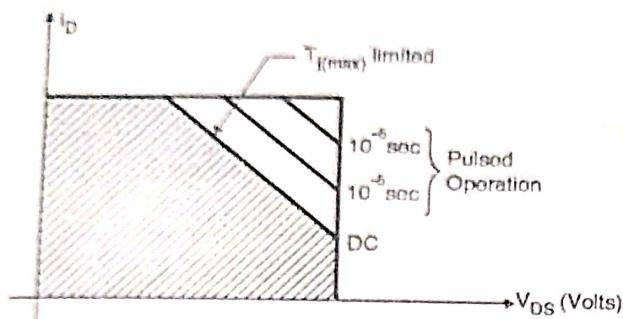
SRPPU : March 19, May 19.

University Questions

- Q. 1 Draw the V-I characteristics of IGBT. Mark & explain various operating regions & SOA of the IGBT. (March 19, 4 Marks)

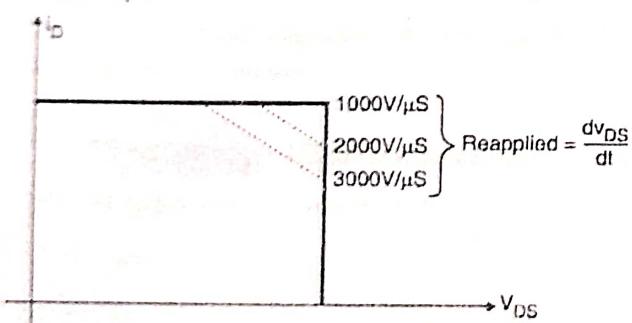
Q. 2 Describe the concept of safe operating areas of MOSFET & IGBT. (May 19, 7 Marks)

- The IGBTs have robust safe operating areas SOA both during turn-on and turn-off.
- The FBSOA is of a square shape identical to that of MOSFET, as shown in Fig. 2.13.1(a) if the turn-on times less than 1 ms.



(a-440) Fig. 2.13.1(a) : Forward bias safe operating area (FBSOA)

- For longer switching times the IGBT will face overheating problems ($T_{j\max}$ limitation), as shown in FBSOA and this is also identical to the behavior of MOSFET in FBSOA.
- The RBSOA is somewhat different from FBSOA, as shown in Fig. 2.13.1(b).
- The RBSOA has been made smaller as the rate of change of reapplied drain to source voltage dV_{DS}/dt increases to ensure safe operation.
- The reason for this restriction on dV_{DS}/dt is to avoid the latch ups.



(a-441) Fig. 2.13.1(b) : Reverse bias safe operating area (RBSOA)

- The maximum permissible junction temperature in commercially available IGBTs is 150°C.
- An important advantage of IGBT is that the on-state voltage $V_{DS(on)}$ remains almost constant even when the temperature varies between the room temperature and the maximum junction temperature.

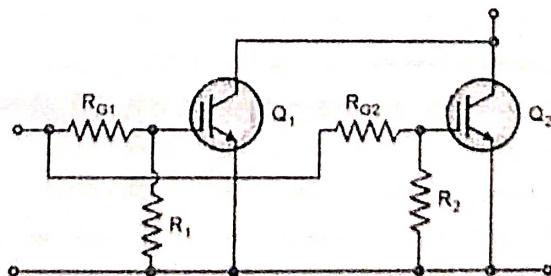
- This is because the IGBT has a flat temperature coefficient of resistivity, i.e. its resistance remains constant even with the temperature variations.
- The IGBT therefore does not suffer from the second breakdown problem. IGBTs can be very easily connected in parallel due to flat temperature coefficient of resistivity, without any external compensating circuit.

2.14 Parallel Operation of IGBTs :

- Parallel connection of more than one IGBTs is necessary when one IGBT of adequately high current rating is not available.
- The current rating of the parallel string is higher than that of a single device.
- Due to the flat temperature coefficient, the parallel connection of IGBTs is much easier as compared to that of the power BJTs.
- In the parallel connection of IGBTs if one of them draws more current than the other, there is no possibility of thermal runaway.
- Therefore, direct paralleling of IGBTs is possible and much easier as well.
- While paralleling the IGBTs it is necessary to take precautions to keep the parasitic oscillations as low as possible.
- For this the resistance in series with their gate terminals must be chosen properly, also the gate driving circuit with a low output impedance must be used.

Direct paralleling of power MOSFETs :

- The power devices like power transistors, power MOSFETs, IGBTs can be connected in parallel, directly that is without using any forced current sharing circuits.
- In case of IGBTs, the collectors and emitters of all the devices are connected together.
- A common gate driving signal is applied to all the gate terminals through suitable gate resistances as shown in Fig. 2.14.1.



(a-2461) Fig. 2.14.1 : Direct parallel connection of IGBTs



- In such direct paralleling of devices, in spite of all the precautions taken to select the devices with almost all identical parameters, the equal current sharing will not take place.
- Some of the devices will draw more current than the others. This is known as current unbalance.
- The factor which indicates the worst case current unbalance is known as the Unbalance factor which should be as small as possible.

String Efficiency and Derating :

- The string efficiency for the parallel string is defined as,
- $$\eta_p = I_m / n_p I_T \quad \dots(2.14.1)$$
- Where, I_m = Total forward current
- n_p = Number of devices in parallel
- I_T = Forward current rating of each IGBT.
- The string efficiency is reduced by using more number of devices in the parallel string than actually required because this will improve the reliability of the string.
 - This will derate the devices and the percent derating is given by,

$$\% \text{Derating for parallel connection, } D_p = \left(1 - \frac{I_m}{n_p I_T} \right) \times 100 \% \quad \dots(2.14.2)$$

- If the percent derating is known, then we can calculate the number of devices required to be connected in parallel.
- Derating increases the reliability of the parallel string.

2.14.1 Merits of IGBT :

SPPU May/11

University Questions

Q. 1 What are the advantages of IGBT over power MOSFET and power BJT ? (May 11, 6 Marks)

1. Easy to turn-on and off.
2. It is a voltage controlled device. Therefore driver circuit is simple and cheap.
3. Low on-state voltage drop. Therefore, low on-state power dissipation.
4. Switching frequency higher than that of a power BJT.
5. Does not need snubber circuit for its protection.
6. It has a flat temperature coefficient of resistivity. So it is easy to connect IGBTs in parallel with each other.

2.14.2 Demerits of IGBT :

1. It has an asymmetric blocking capacity. It cannot block high reverse voltages.
2. Switching frequency is not as high as that of a power MOSFET.
3. Problem of latch ups.
4. Excessive power dissipation can take place at the time of turn-off due to the "current tail" present in the turn-off characteristics.

2.14.3 Applications of IGBT :

- Some of the important applications of IGBT are :
 1. Switching Mode Power Supplies (SMPS)
 2. UPS systems (IGBT based inverters)
 3. AC motor controllers
 4. Choppers
 5. Inverters

2.14.4 Advantages of IGBT over BJT :

SPPU May/11

University Questions

Q. 1 What are the advantages of IGBT over power MOSFET and power BJT ? (May 11, 6 Marks)

1. It is a voltage controlled device so that gate driving is easy.
2. It can switch at higher frequency than BJT. Typically $f_{max} = 20$ kHz.
3. IGBTs can be easily connected in parallel.
4. Second breakdown does not take place.
5. IGBTs do not need snubber circuits for their protection.

2.14.5 Advantages of IGBT over MOSFET :

1. On-state voltage drop across IGBT is less than that across MOSFET.
2. Low on-state power dissipation.
3. IGBTs can handle larger power than MOSFETs.

2.15 Comparison of Power Devices :

SPPU May/11, Dec/11, Dec/12, Dec/13, Feb/16

May/17, May/18

University Questions

Q. 1 Compare SCR with power BJT. (May 11, 4 Marks)

Q. 2 Compare power MOSFET with IGBT.

(Dec. 11, 3 Marks, Dec. 13, 4 Marks)

- Q. 3** Compare power MOSFET with power BJT.
(Dec. 12, 5 Marks)
- Q. 4** Compare power MOSFET with SCR.
(Feb. 16, 6 Marks)
- Q. 5** Draw the construction of power MOSFET and explain steady state characteristics of power MOSFET. Compare it with SCR and IGBT.
(May 17, 7 Marks)

- Q. 6** Draw the construction of power MOSFET. Explain I-V steady state characteristics of MOSFET. Compare and contrast with SCR.

(May 18, 7)

2.16 Isolation

In order to operate as a switch, current or voltage saturation.

The control is given by emitter or base of the device.

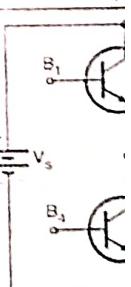
The power can be more than current controlled separated.

Fig. 2.16.1(a) shows the voltage V_g at the terminal GATE with respect to driving signal.

The logic reference point with respect to earth.

Transistors Q₃ and Q₄ connected in common-emitter configuration.

Note : That in either p-n-p or n-n-p connection,



(I-652) Fig. :

But we have which has connected instead the base B₁ and B₂.

Table 2.15.1 : Comparison between the SCR, BJT, MOSFET and IGBT

Sr. No.	Parameter	SCR	Power BJT	Power MOSFET	IGBT
1.	Operating frequency	400 to 500 Hz	10 kHz	100 kHz	10 kHz
2.	Trigger circuit	Current controlled needs single pulse to turn-on.	Current controlled needs continuous base drive	Voltage controlled needs continuous gate drive	Voltage controlled needs continuous gate drive
3.	On-state voltage drop.	< 2 Volts	< 2 Volts	4 – 5 Volts	3 Volts
4.	Snubbers	Necessary (unpolarised)	Necessary (polarised)	Snubber can be eliminated. If used a polarised snubber is used.	Snubber can be eliminated. If used a polarised snubber is used.
5.	Maximum ratings VI	10 kV/5000 Amp	2 kV/1000 A	600 V/200 Amp	1500 V/400 Amp
6.	Applications	DC motor drives, inverters, rectifiers	UPS, SMPS, static VAR systems, AC motor control, SMPS	AC motor control, SMPS	SMPS, BLDC drives, AC motor control
7.	Symbol				
8.	Type of device	Minority carrier	Minority carrier	Majority carrier	Minority carrier
9.	Voltage/current controlled	Current	Current	Voltage	Voltage
10.	Commutation circuit	Necessary	Not necessary	Not necessary	Not necessary
11.	Blocking capacity	Symmetrical	Asymmetrical	Asymmetrical	Asymmetrical
12.	Temperature coefficient	Negative	Negative	Positive	Flat
13.	Thermal runaway	Possible	Possible	Not present	Not present
14.	Parallel operation.	External equalizing circuit is necessary.	Equalizing circuit required	Easy to parallel	Easy to parallel

2.16 Isolation of Gate and Base Drives :

In order to operate a power transistor, MOSFET or IGBT as a switch we have to apply an appropriate base current or gate voltage to drive the device into saturation.

The control voltage is to be applied between base and emitter or between the gate and source terminals of the device.

The power circuits such as inverters, choppers etc. need more than one power devices and each one should be gated separately.

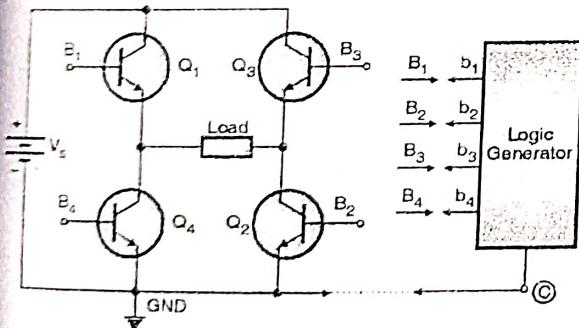
Fig. 2.16.1(a) shows a single phase inverter. The dc input voltage V_s is applied to it with respect to the ground terminal GND. A logic generator generates the base driving signals.

The logic generator generates four pulses with a reference point "C". These pulses are shifted in time with respect to each other as shown in Fig. 2.16.1(b).

Transistors Q_1 and Q_2 conduct simultaneously whereas Q_3 and Q_4 conduct simultaneously.

The common terminal "C" of the logic generator may be connected to the supply ground GND as shown by a dotted line in Fig. 2.16.1(a).

Note : That in place of transistors Q_1 to Q_4 we can connect either power MOSFETs or IGBTs.

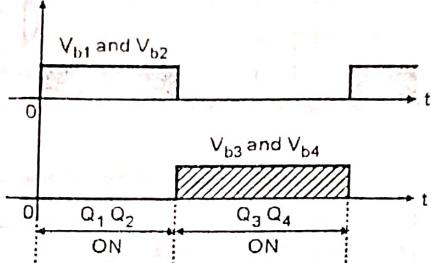


(I-652) Fig. 2.16.1(a) : Single phase inverter with logic generator

But we have a practical problem here. The terminal "b₁" which has a voltage V_{b1} with respect to C, cannot be connected directly to the base of Q_1 i.e. B₁.

Instead the signal V_{b1} should be applied between the base B₁ and emitter E₁ of transistor Q₁.

- Similarly V_{b1} should be applied between B₁ and E₁. Thus there is a need for isolation and interfacing circuits between the logic generator and power transistors Q₁ and Q₃.
- However the transistors Q₂ and Q₄ can receive their base voltages V_{b2} and V_{b4} directly without isolation or interference circuits.
- This is because their emitters are connected to the GND terminal which is in turn connected to point "C".



(I-653) Fig. 2.16.1(b) : Base driving signals for single phase inverter

- There are basically two ways of floating or isolating the control signals as follows :
 1. To use the pulse transformers.
 2. To use the opto couplers.

2.17 Silicon Carbide (SiC) Devices :

2.17.1 Silicon Carbide (SiC) :

- All the power semiconductor devices which we had discussed are silicon based devices. However these devices have a limitation on their performance due to the inherent characteristics of silicon.
- Hence the silicon based power devices are unable to meet the future demands of high voltage, high efficiency and high power density applications.
- The silicon carbide (SiC) is the only compound of silicon and carbon which does occur naturally but is extremely rare.
- This material has become the material of choice for the next generation power semiconductor devices, because as compared to silicon based devices, the SiC devices have the following advantages.

2.17.2 Advantages of SiC Devices :

- Some of the major advantages of SiC power devices are as follows :

1. SiC power devices have ten times higher dielectric breakdown field strength.
2. They have three times higher bandgap.
3. They have three times higher thermal conductivity.
4. SiC power devices offer lower switching loss.
5. They have lower ON state resistance.
6. They can operate at higher temperatures.
7. Their size is small.

2.17.3 Important Features :

- Some of the important features of SiC power devices are as follows :
 1. Higher breakdown voltage.
 2. Higher operating temperature ranges.
 3. Higher switching speeds.
 4. Lower ON state resistance.
 5. Reduced power loss.
 6. Smaller size.
 7. Higher efficiency due to reduced losses.
 8. Higher current density.
- Due to all these advantages, features, the silicon carbide power devices are finding more applications despite their high price as compared to silicon based devices.
- Some of the important applications of SiC devices are as follows :

2.17.4 Applications :

- Some of the major applications of SiC power devices are as follows :
 1. SMPS
 2. Solar inverters
 3. EV chargers
 4. UPS
 5. Induction heating equipments
 6. Motor drives
 7. Wind power converter.

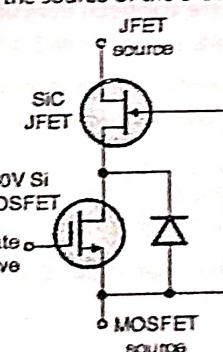
2.17.5 SiC in Power Electronics :

- Several power semiconductor devices are produced using SiC such as, Schottky diodes, Junction gate FETs (or JFETs) and MOSFETs, which are used in the high power switching applications.

- Silicon carbide is comprised of equal parts silicon and carbon via covalent bonding. This process leads to a highly ordered configuration.
- Therefore, the SiC is an extremely hard material. It is supposed to be the third known hardest substance on the earth.
- Several SiC based power devices have been successfully commercialized, the SiC market is still in an early stage.
- Today the only available SiC devices are Schottky diodes, JFETs, MOSFETs and BJTs.

2.17.6 SiC JFET :

- This device was relatively easy to implement and there were no reliability issues of gate oxide as observed in SiC MOSFETs.
- Therefore SiC JFET was commercialized earlier than other SiC switches. It is a normally ON switch.
- It can be implemented with either vertical or horizontal trench structure. The normally ON type JFET is also called as **depletion mode JFET**.
- It is turned OFF fully when the gate voltage is less than the pinch-off voltage (about -15 V). In the ON state it is equivalent to a **resistance** which can be minimized by keeping V_G slightly higher than zero.
- Generally a cascode driver is used for this JFET as shown in Fig. 2.17.1. A low voltage high current silicon MOSFET is connected to the source of the SiC JFET.



(1-2067) Fig. 2.17.1 : Conventional cascode drive circuit

- This is known as the cascode drive circuit. Typically a 30 V Si MOSFET with a few $m\Omega$ ON state resistance is used.
- In the normal operating conditions, the MOSFET conducts without any significant addition in the ON state resistance of JFET.

Transistor Based Devices

- But in case of start up and malfunction, the normally OFF MOSFET is turned OFF and pushes the source of JFET to a positive potential, with respect to its gate. Thus JFET is turned off, into a safe state.
- In the normal operation, the Si MOSFET drives the JFET. When the Si MOSFET is turned ON, the gate voltage of JFET becomes zero and the JFET would conduct.
- It is possible to allow the JFET to have a normally OFF characteristics by adjusting the thickness of the vertical channel and doping level.
- The normally OFF JFET is called as **Enhancement mode JFET**. It remains OFF when $V_G = 0$ V, and fully turns ON when $V_G = 2$ to 3 V. But this type has a larger resistance than the normally ON type device.

2.17.7 SiC MOSFET :

- Due to poor quality of oxide-semiconductor interface, the SiC MOSFETs were introduced after SiC JFETs.
- The other problem is the large threshold voltage instability. The gate oxide also degrades at a temperature which is less than the maximum junction temperature of SiC device.
- Despite these problems, the SiC MOSFET is still an attractive device because it is voltage controlled and normally an OFF type device.
- As compared to the Si MOSFETs, the SiC MOSFET have unique operating characteristics.
- In SiC MOSFETs the transition from ohmic to saturation region is not clearly defined as its Si counterpart.
- The nominal threshold voltage is around 2.5 V and the device does not turn ON fully unless V_{GS} is greater than 16 V.
- The recommended ON state V_{GS} is 20 V whereas the recommended OFF state V_{GS} is -2 V to -5 V.
- The important parameters of a SiC MOSFET are as shown in Table 2.17.1.

Table 2.17.1 : Parameters of SiC MOSFET

Sr. No.	Parameter	Value
1.	Gate threshold voltage V_1	3.2 to 4.8 V typical
2.	Drain current for $V_{GS} \approx 0$ i.e. I_{DSS}	250 μ A typical
3.	ON-state resistance	95 to 120 m Ω

Sr. No.	Parameter	Value
4.	Forward voltage of the body diode	3.5 V Typical
5.	Reverse recovery time of the body diode	140 nS minimum

- The temperature coefficient of ON state resistance of SiC MOSFET is higher than that of SiC JFET. This is an advantage due to wide bandgap.
- Also the gate leakage current of SiC MOSFET does not increase much with increase in temperature, whereas the leakage gate current of a Si MOSFET increases 100 times for a change in junction temperature from 25°C to 135°C.
- Also the reverse recovery time of the body diode in SiC MOSFET is much smaller compared to Si PN junction diode. This ensures increase in switching speed.

2.18 GaN Power Devices :

- Today a wide range of GaN (Gallium Nitride) devices are being volume produced, and are replacing the well established and widely used silicon based MOSFETs, in various applications.
- The GaN based power switching devices are used because they offer the following advantages.

2.18.1 Advantages of GaN Devices :

- Some of the major advantages of GaN power devices are as follows :
 1. Greater efficiency.
 2. Better and higher power handling.
 3. Other important performance attributes.
 4. The GaN power switching devices are being used in the following applications.

2.18.2 Applications of GaN Power Devices :

- Some of the major applications of GaN power devices are as follows :
 1. In power supplies.
 2. In the motor control applications.
 3. In other commercial and industrial applications.
 4. In the extremely stringent automotive applications.

2.18.3 Why GaN?

- The existing silicon based power MOSFETs have been very successful in a variety of power electronics application.
- There has been a continuous improvement in all the important attributes such as on state resistance $R_{DS(ON)}$, voltage ratings, switching speed, packaging etc.
- However, these improvements have almost reached to their best possible values and there is a very little chance of much further improvement in their values.
- The silicon MOSFET parameters have reached their limit due to the limit decided by the underlying fundamental physics of the material silicon and the associated processes.
- That is why a new material called Gallium Nitride (GaN) is used for the power devices instead of silicon.

2.18.4 Classification of GaN Devices :

- The GaN devices are broadly classified into two categories :
 1. Devices operating in enhancement mode.
 2. Devices operating in the depletion mode.
- The devices operating in the **depletion mode** are **normally ON** devices.
- In order to turn them OFF we need to apply a **negative gate voltage** with respect to the drain and source terminals.
- The **enhancement mode (e-mode)** GaN transistors are **normally OFF** devices and we can turn them on by applying a positive gate voltage.
- The **depletion mode** transistors have the **start up issues**. That is, when the power is applied, we have to apply a negative gate bias first, to turn it off, and avoid the **start up short circuit**.
- This problem can be solved and the depletion devices can be converted to **normally OFF** devices by packaging them in a **cascade** configuration with a low voltage silicon MOSFET.
- The **e-mode** devices do not conduct at all when there is a zero bias on the gate at the time of power ON. This is a **desired start up state**.

2.18.5 Advantages of GaN Over Silicon :

- GaN has the following advantages over silicon.
 1. Higher electric field strength.

Transistor Based

2. GaN devices have a smaller size for a given state resistance and breakdown voltage.
3. Lower ON state resistance for a given size.
4. Higher breakdown voltage for a given size.
5. Extremely high switching speed.
6. Very good reverse recovery performance.
7. Reduced losses.
8. Higher efficiency.

2.18.6 GaN Devices Versus Silicon MOSFET

Similarities :

- There are some important similarities between GaN devices and silicon MOSFETs. They are as given below
- 1. **The terminology is same :**
- Like a silicon MOSFET, the GaN transistor also has terminals, drain (D), gate (G) and source (S).
- 2. **Important parameters are same :**
- Like silicon MOSFETs, the important parameters of GaN transistor also are **ON state resistance** and **breakdown voltage**.
- 3. **Normally OFF devices :**
- Both Si-MOSFET and e-mode GaN transistor are normally OFF devices.
- 4. **Voltage driven devices :**
- GaN transistor also are voltage driven devices like silicon MOSFET.
- 5. **Input capacitance :**
- For both these devices, the input capacitance must be charged and discharged by their driver.
- The slew rate and the shape of driving waveform are important factors that determine the device performance.

Differences :

- 1. **Material :**
- The GaN is used instead of silicon.
- 2. **ON-state resistance :**
- An important specification for both these devices is their ON-state resistances. Its value is very low for GaN devices.
- Therefore static loss is reduced and efficiency increased for the GaN devices.

3. Input capacitance :

Due to the structure of GaN transistor, its input capacitance is very small as compared to that of a silicon MOSFET.

This increases the switching speed of the GaN devices (typically hundreds of MHz), way beyond that of silicon MOSFETs.

4. Higher breakdown voltage :

The GaN transistors have a higher breakdown voltage as compared to that of a silicon MOSFET.

2.18.7 Driver is Critical for GaN Success :

In order to operate the GaN transistor to its full specifications and avoid any unintended issues, its driver should be properly designed.

A driver acts as an interface between the low voltage microprocessor based controller and the high voltage high current power section.

The driver should supply the required current with an adequately high rate to quickly charge or discharge the input capacitance of the gate, to turn it on and off quickly.

The following three factors are important for the drivers of GaN devices.

Three important factors :

1. Maximum allowable gate voltage.
2. The gate threshold voltage.
3. The body diode voltage drop.

The ON state gate to source voltage ($V_{GS(ON)}$) of a GaN transistor is 6 V which is approximately half that of a MOSFET. This makes the driver design of GaN devices simpler.

The threshold gate voltage (V_t) for a GaN transistor is lower than that of a silicon MOSFET. This further simplifies the design of driver circuit.

The forward voltage drop of a GaN transistor is about a volt higher than that of a comparable silicon MOSFET.

2.18.8 Performance Parameters of GaN Devices :

Some important performance parameters of GaN transistors are as follows :

1. The dV/dt slew rates of GaN are higher than 100 V / nsec. This makes them faster than Si-MOSFETs.

2. The turn ON time of GaN is about 4 times faster while the turn OFF time is about 2 times faster than the Si-MOSFET.

3. For the comparable value of $R_{DS(on)}$, the total Miller charge for GaN devices is much lower than that for Si-MOSFET. Due to this also, the GaN transistor can be switched faster.

4. Sometimes a high dV/dt slew rate can create a shoot-through condition (which should be avoided). This could be avoided by minimizing the transition time of the GaN transistors by controlling the value of gate pull-up resistance.

5. The false turn on / turn off glitches and EMI should be avoided by properly designing the driver circuit.

- Gate driving ICs for GaN devices are available in the market which are capable of taking care of all the issues mentioned above.

- The inputs of GaN devices are TTL compatible, yet they can tolerate input voltages upto 14 V.

2.18.9 Disadvantages of GaN Devices :

1. At higher operating frequencies, there is a possibility of shoot-through or short circuit.
2. There is a possibility of false triggering.
3. There is a possibility of EMI at high operating frequency.

2.18.10 Comparision of GaN Transistor and Si-MOSFET :

Table 2.18.1 : Comparision of GaN Transistor and Si-MOSFET

Sr. No.	Parameter	Si-MOSFET	GaN Transistor
1.	Number of terminals.	3	3
2.	Normally OFF / Normally ON ?	Normally OFF	Normally OFF
3.	Voltage controlled or current controlled?	Voltage controlled	Voltage controlled
4.	Material used	Silicon	Gallium nitride
5.	ON – state resistance.	Low	Very low

Sr. No.	Parameter	Si-MOSFET	GaN Transistor
6.	Static power loss	Higher	Lower
7.	Efficiency	Lower	Higher
8.	Input capacitance	Large	Small
9.	Switching speed	High	Very high
10.	Breakdown voltage	High	Very high
11.	Gate threshold (V_T)	High	Low
12.	Forward voltage drop	Lower	Higher
13.	Turn on time	Slower	Faster
14.	Turn off time	Slower	Faster

Review Questions

- Q. 1 With the help of structure explain the operation of a power BJT.
- Q. 2 Draw and explain the static characteristics of a power BJT.
- Q. 3 Draw and explain the static characteristics of a power MOSFET.
- Q. 4 Explain the switching characteristics of power MOSFET.
- Q. 5 State the advantages of power MOSFET.
- Q. 6 State the disadvantages of power MOSFET.
- Q. 7 State applications of power MOSFET.
- Q. 8 Write a note on : Do's and Don't for a power MOSFET.
- Q. 9 State important features of IGBT.
- Q. 10 Draw the structure of an IGBT and explain the function of each layer.
- Q. 11 Explain the principle of operation of IGBT.
- Q. 12 With the help of neat diagram explain the static characteristics of an IGBT.
- Q. 13 Draw and explain the dynamic characteristics of an IGBT.
- Q. 14 Explain the FBSOA and RBSOA of IGBT.
- Q. 15 IGBT is superior to power BJT and power MOSFET . Justify.
- Q. 16 Write note on - drive circuit requirements of IGBT.
- Q. 17 Write note on - protection of IGBT against over current.
- Q. 18 Explain with necessary diagrams the principle of operation of an IGBT.
- Q. 19 What is the reason behind latch ups in IGBT ? How to eliminate them ?
- Q. 20 Write a note on-latch ups in IGBT.
- Q. 21 Name the power devices which you will select for following requirements :
- (a) Capability to withstand very high forward and reverse voltage.
 - (b) Inverter with very high frequency above 100 kHz.
 - (c) Protection of devices against fault conditions to be simple.
- Q. 22 Explain the equivalent circuit of IGBT.
- Q. 23 Draw and explain typical gate drive circuit for an IGBT. List advantages of IGBT over power MOSFET and power BJT.
- Q. 24 State the advantages of SiC devices over silicon devices.
- Q. 25 What are the important features of SiC devices.
- Q. 26 State the applications of SiC devices.
- Q. 27 Explain the operation of SiC power MOSFET.
- Q. 28 What are the advantages of GaN devices ?
- Q. 29 State the applications of GaN devices.
- Q. 30 What are the advantages of GaN over silicon ?
- Q. 31 Compare GaN devices with Silicon MOSFET.
- Q. 32 Discuss the performance parameters of GaN power devices.

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