ES7210 User Guide

(Rev.1.00)

ES7210 User Guide

ES7210 is a high performance, low power, 4 channel audio ADC for microphone array application. It integrates four PGAs for quad differential inputs, MIC1P & MIC1P, MIC2P & MIC 2N, MIC 3P & MIC 3N and MIC4P & MIC4N. The PGAs have programable gain range from 0dB to +37.5dB in 3dB/step.

ES7210 is easy to use, utilizing the differential inputs and the internal PGA to interface with microphone and boost the microphone signal level. One ES7210 can interface with four microphones. It also can be interfaced with line input if the internal PGA gain is +0dB.

Also, ES7210 has digital microphone interface for PDM digital microphone application. In digital domain, it provides 0dB to 42dB gain control for digital microphone level with 6dB/step.

ES7210 has TDM mode to cascade multiple ES7210 devices. Its TDM cascading mode makes it easy to connect with DSP.

ES7210 supports standard audio clocks (256Fs, 384Fs, 512Fs, etc.), USB clocks (12/24 MHz), and some nonstandard clocks (25 MHz, 26 MHz, etc.). According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz. ES7210 can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

ES7210 is very suitable for music and voice application, such as Microphone Array, Far field voice capture, Smart speaker, Conference system, Sound bar, Audio Interface, etc.

Features

1. Supports I2S, Left Justified and DSP-A/B digital format, supports Master or Slave mode.
2. Supports standard audio clock, such as 11.2896MHZ, 12.288MHZ, etc. Supports nonstandard clock, such as 12MHZ, 24MHZ, 13MHZ, 26MHZ, etc.
3. Supports 256 or 384 LRCK ratio. Also, it supports nonstandard LRCK ratio without obvious performance degraded.
4. Quad differential line-inputs or differential microphone inputs
5. Quad programable gain preamplifiers with gain range from +0dB to +37.5dB.
6. Supports PDM digital microphone interface with digital amplifiers providing gain control from +0dB to +42dB
7. I2C controls port to read/write internal register.
8. TDM mode to cascade multiple ES7210 for microphone array application or conference system.
9. Has standby capability to save power consumption.

ADC Performance

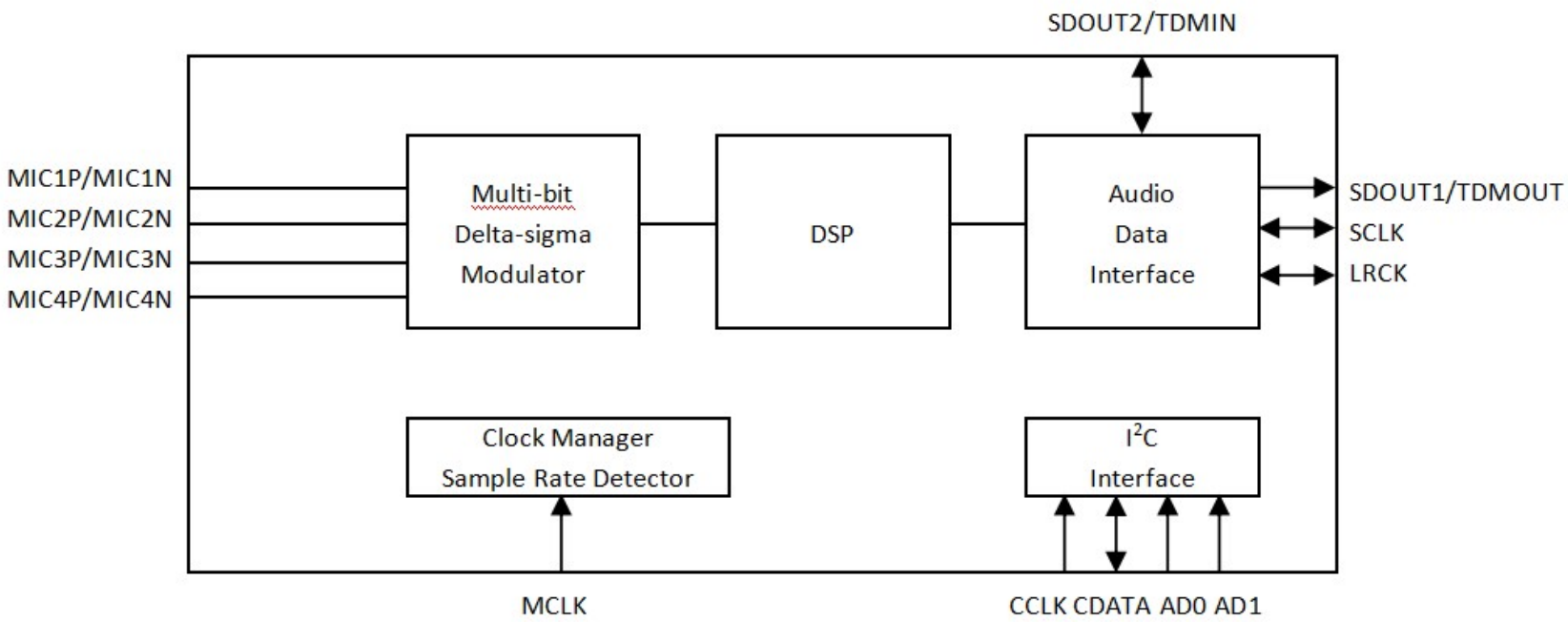
1. -85dB THD+N
2. 102dB SNR @ +0dB PGA gain, 92dB SNR @ +27dB PGA gain
3. 24-bit, 8 to 200 kHz sampling frequency
4. Quad differential line inputs or microphone inputs

Package Outline

1. ES7210 QFN-32, 4mm × 4mm

ES7210 User Guide

1 BLOCK DIAGRAM



ES7210 Block Diagram

SIGNAL PATH

ES7210 has quad differential inputs, MIC1P & MIC1P, MIC2P & MIC 2N, MIC 3P & MIC 3N and MIC4P & MIC4N, followed by quad PGAs with gain range from +0dB to +37.5dB. Then, the internal high performance multi-bit delta-sigma audio ADC does analog to digital converting. At last digital signal should be outputted on ASDOUT pin.

The maximum input level of these line inputs is 1Vrms.

2 Recommended Operating Condition and Power Consumption

The following Table shows the recommended operating condition of ES7210.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDD	1.6	3.3	3.6	V
VDDP	1.6	3.3	3.6	V
VDDA	1.6	3.3	3.6	V
VDDM	1.6	3.3	3.6	V

Below Table lists power consumption in normal mode and standby mode.

	Clock Condition	Ivddp(mA) （VDDP = 3.3V）	Ivddd(mA) （VDDD = 3.3V）	Ivdda(mA) （VDDA = 3.3V）
Normal Mode	MCLK=12.288MHZ LRCK = 48KHZ	0.00	10.88	10.08
	MCLK=6.144MHZ LRCK = 48KHZ	0.00	5.77	10.08
	MCLK=6.144MHZ LRCK = 24KHZ	0.00	5.79	10.08
	MCLK=4.096MHZ LRCK = 16KHZ	0.00	3.99	10.08
	MCLK=2.048MHZ LRCK = 16KHZ	0.00	2.38	10.08
Standby Mode	Standby Mode 1: R6=0x5C R7=0xFF R8=0x4B R9=0x9F	0.00	0.68	0.67
	Standby Mode 2: R6=0x5C R7=0x3F R8=0x4B R9=0x9F	0.00	0.68	0.01
	Standby Mode 3: Stop MCLK and I2S CLK, R6=0x5C,R7=0x3F,R8=0x4B, R9=0x9F	0.00	0.09	0.01

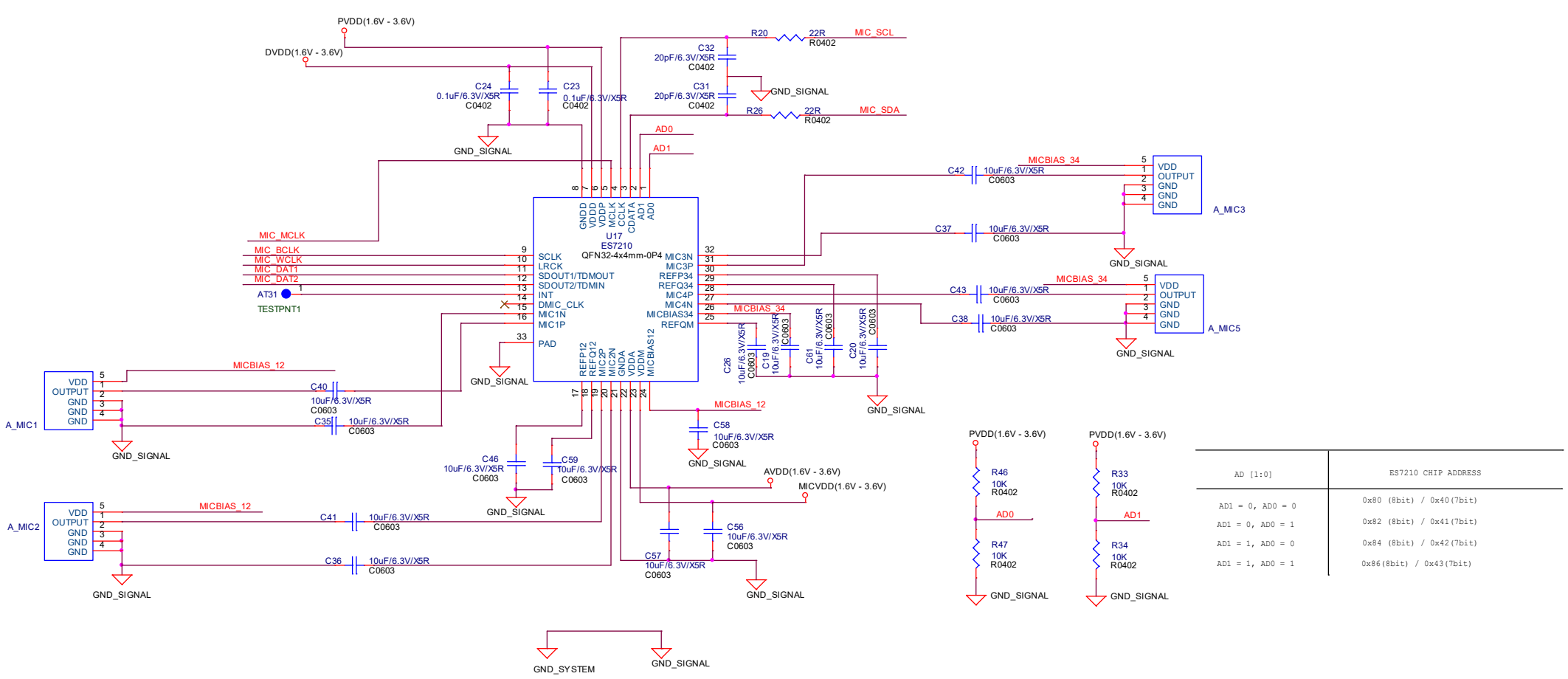
3 Application Circuit and PCB Layout Guide

This section provides some guideline about circuit schematic and PCB layout.

3.1 ES7210 Application Circuit for Analog Microphone

Below circuit schematic is ES7210 Application Circuit for analog microphone. It illustrates the details about microphone interface, I2C, ground and power supply.

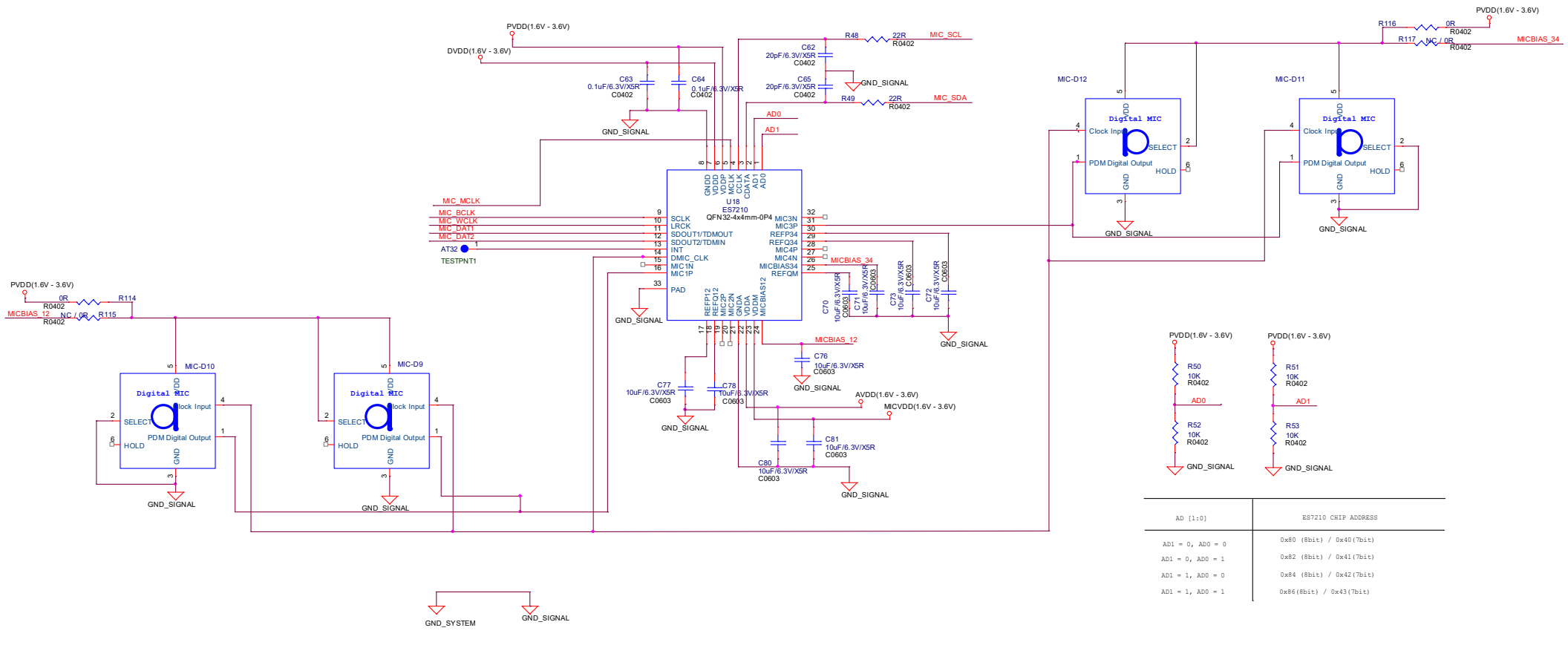
This application circuit doesn't illustrate the TDM mode of ES7210. Please refer to the application circuit of ES7210 TDM mode in section 4.8 "TDM mode".



3.2 ES7210 Application Circuit for PDM Digital Microphone

Below circuit schematic is ES7210 Application Circuit for PDM digital microphone. It illustrates the details about PDM digital microphone interface, I2C, ground and power supply.

This application circuit doesn't illustrate the TDM mode of ES7210. Please refer to the application circuit of ES7210 TDM mode in section 4.8 "TDM mode".

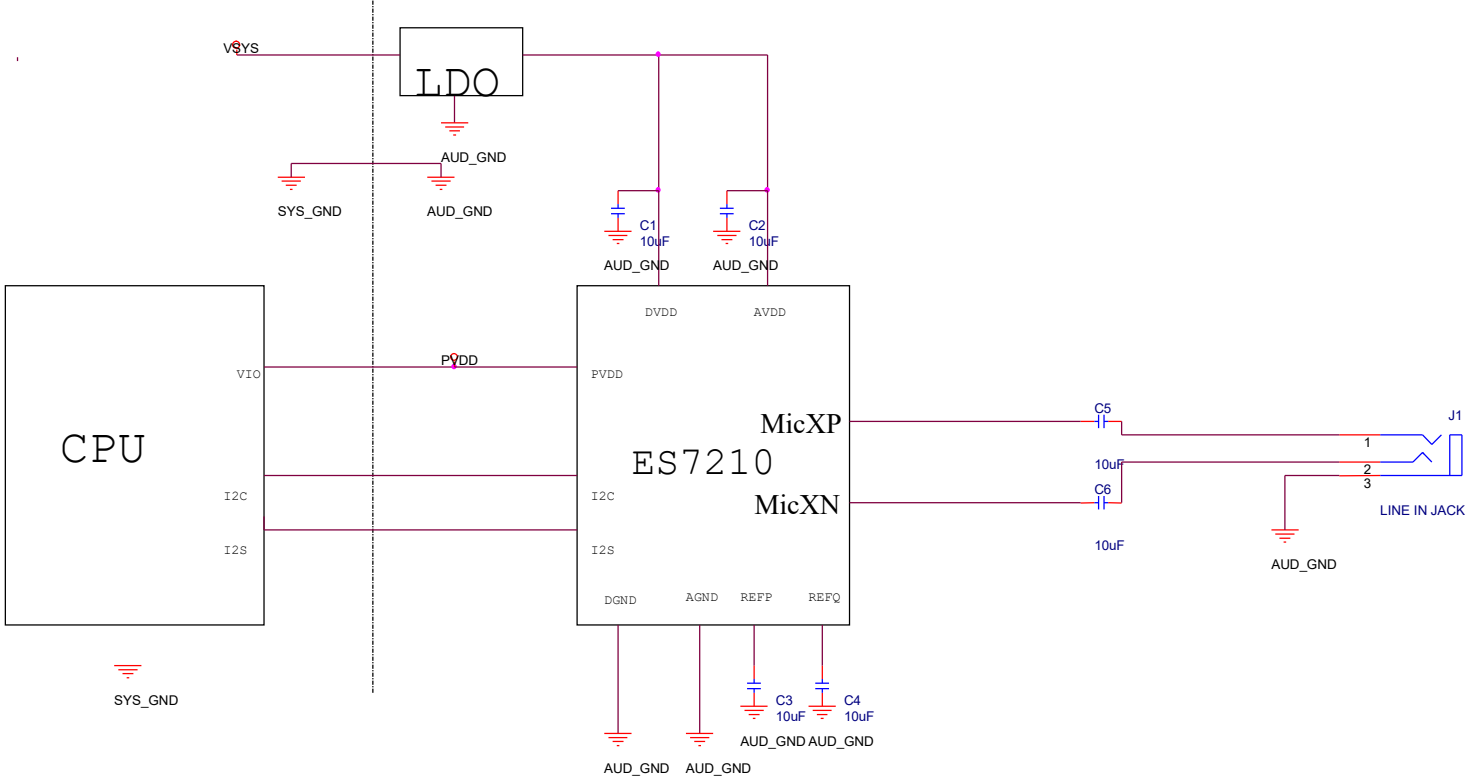


3.3 PCB Layout Guide

As with any high-resolution audio converter, designing with ES7210 requires careful attention to PCB layout if its potential performance is to be realized.

3.3.1 The Power supply, Grounding, Decoupling and Filters

The power supply of ES7210 must be isolate from system power supply. A LDO specified for ES7210 is recommended in order to get the best audio performance. Usually, GNDD and GNDA must be connect to the same analog ground plane, and then join into system ground at a single point nearby the power supply. It is important to prevent high frequency noise or high current noise from going into audio ground plane. Below diagram illustrates ES7210 power supply and grounding.

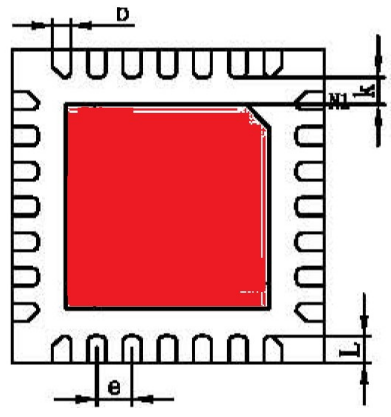


There need some decoupling and filter capacitors on VDDD, VDDA, MICBIAS, REFP and REFQ pins. These decoupling and

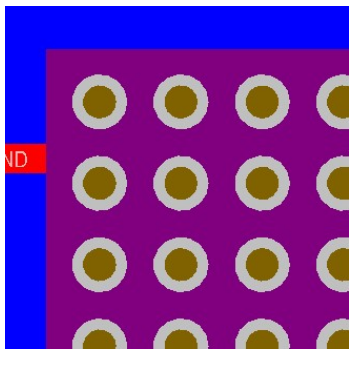
filter capacitors must be as near to ES7210 package as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from MICBIAS, REFP and REFQ in order to avoid unwanted coupling to ADC modulators. The filter capacitors on REFP and REFQ pins, especially 0.1uF capacitor, must be positioned to minimize the electronic path from these reference pins to GND.

3.3.2 The Thermal Pad of ES7210

There is a thermal pad on the bottom of ES7210 package. The following drawing shows this thermal pad.

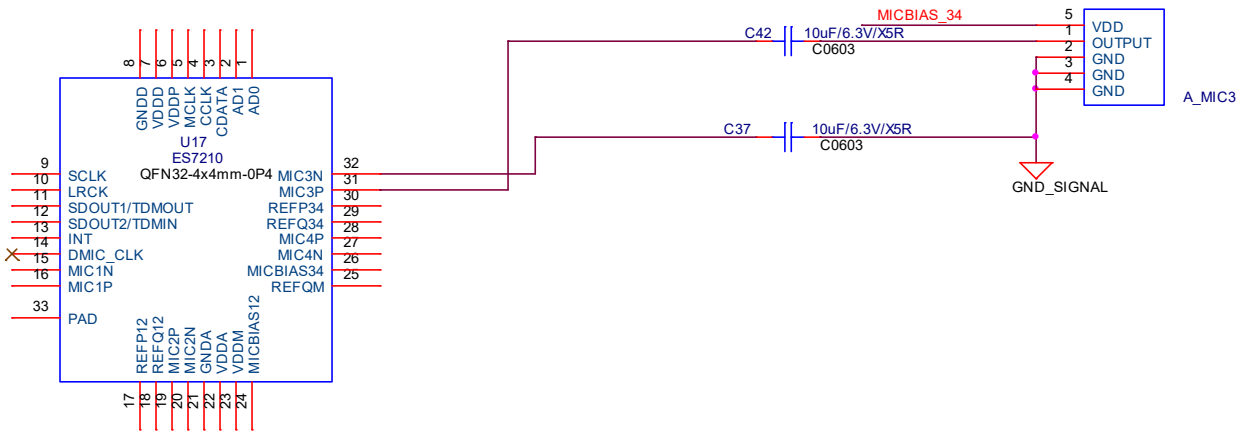


In practical system, the thermal pad must be connected to ground plane by via. The following picture illustrates how the thermal pad is connected to ground plane.



3.4 Microphone Circuit

ES7210 has four differential inputs, MIC1P & MIC1P, MIC2P & MIC 2N, MIC 3P & MIC 3N and MIC4P & MIC4N, and these differential inputs can all be used as microphone interface. It is important note here that the analog input capacitors, such as C42 and C37, must be located near to the microphone. 4.7uF or 10uF ceramic capacitor is specific for these analog input capacitors. The PCB routes of MICxP and MICxN must be differential routes and must be shield by ground.



3.5 Microphone Bias Supply

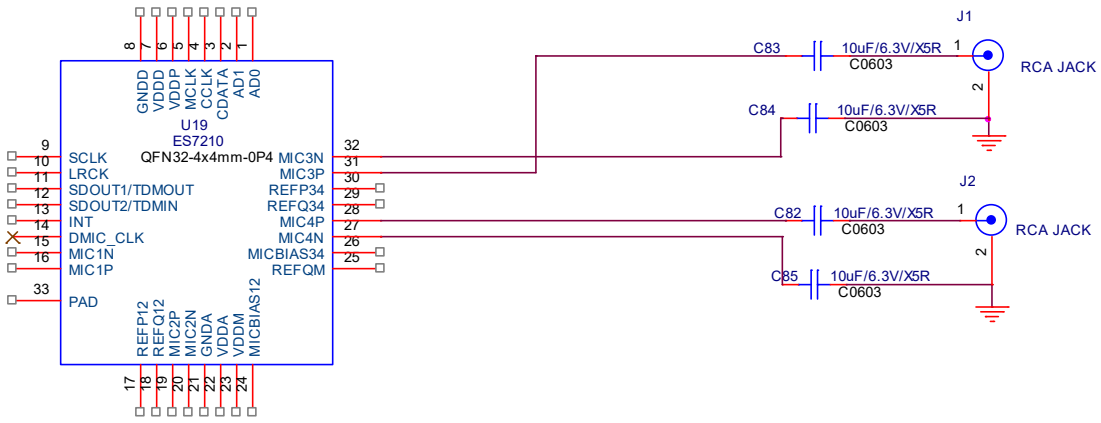
ES7210 has two microphone biases in each device, one microphone bias is MICBIAS12 and another is MICBIAS34. These two microphone bias are all derived from the VDDM power supply of ES7210. The voltage level of MICBIAS12 and MICBIAS34 are all programable via I2C.

Usually, 4.7uF or 10uF ceramic capacitor is specific for filter capacitors on MICBIAS12 and MICBIAS34.

3.6 Line input

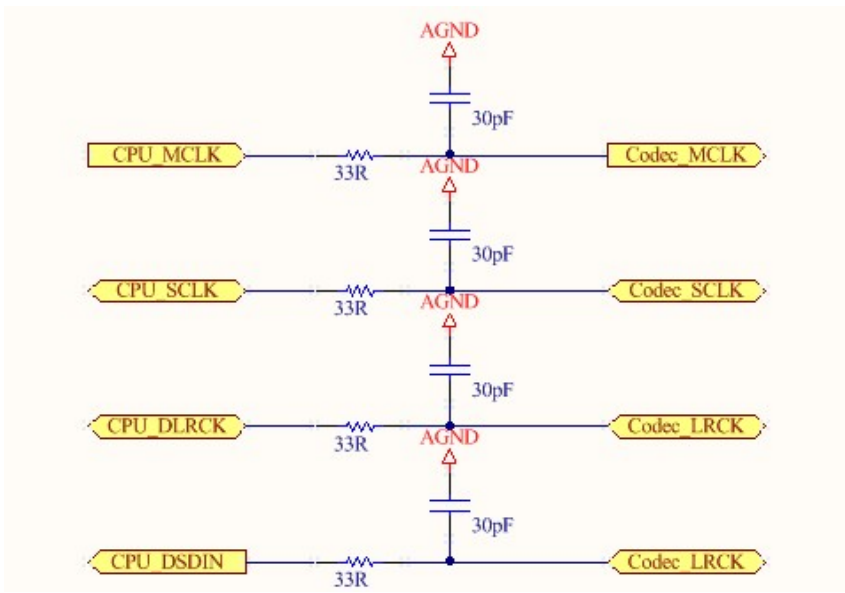
If the internal PGA gain is 0dB, the differential inputs of ES7210 can also be used as line inputs. Following circuit schematic illustrates the line input of ES7210. It is important note here that the analog input capacitors, such as C82, C83, C84 and C85, must be near to the line input jack. 4.7uF or 10uF ceramic capacitor is specific for these analog input capacitors.

The PCB routes of differential line inputs must be differential routes and must be shield by ground.



3.7 The Circuit Schematic for I2S

If the length of I2S clock is larger than 10cm, please use 30pF capacitors between I2S clock route and ground. For example,



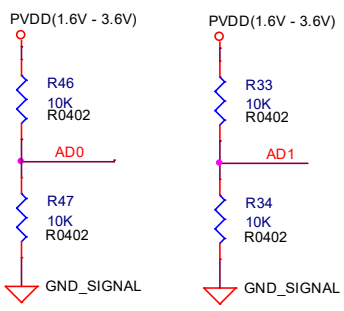
3.8 The Circuit Schematic of I2C

ES7210 has I2C control port to read / write internal register. Below schematic shows the circuit of I2C port. The R-C low pass filter is generally recommended for I2C bus to avoid high frequency noise. The I2C route must be shielded

by ground.

Pin1 (AD0) and Pin2 (AD1) are used to select the I2C chip address of ES7210. Following Table shows the definition of I2C chip address.

ES7210 I2C Chip Address	The Level of AD[1:0] pin
0x80 (8bit) / 0x40 (7bit)	AD1 =0, AD0 = 0
0x82 (8bit) / 0x41(7bit)	AD1 = 0, AD0 = 1
0x84 (8bit) / 0x42 (7bit)	AD1 =1, AD0 = 0
0x86(8bit) / 0x43(7bit)	AD1 = 1, AD0 = 1



AD [1:0]	ES7210 CHIP ADDRESS
AD1 = 0, AD0 = 0	0x80 (8bit) / 0x40(7bit)
AD1 = 0, AD0 = 1	0x82 (8bit) / 0x41(7bit)
AD1 = 1, AD0 = 0	0x84 (8bit) / 0x42(7bit)
AD1 = 1, AD0 = 1	0x86(8bit) / 0x43(7bit)

4 ES7210 Application

ES7210 operates in software mode, and it communicates with host device via I2C port. In ES7210, some internal registers are used for power control, PGA gain control, serial digital audio format selection, master or slave mode selection, TDM mode enable/disable and LRCK ratio selection, etc.

Multiple ES7210 can be cascaded for microphone array application. This TDM cascading mode is very useful in speech recognition, speech localization and conference system.

4.1 Register Map

	default	B7	B6	B5	B4	B3	B2	B1	B0
Reg.00	0x32	//////////////////	RST_MSTGEN	RST_ADC34_DIG	RST_ADC12_DIG	SEQ_DIS	RST_REGS	RST_DIG	CSM_ON
Reg.01	0x20	//////////////////	EXT_BCLKLRCK_OFF	MASTER_CLK_OFF	ADC34_MCLK_OFF	ADC12_MCLK_OFF	ANA34_CLK_OFF	ANA12_CLK_OFF	MCLK_OFF
Reg.02	0x02	DLL_BYPASS	CLKDBL_VALID	//////////////////	CLK_ADC_DIV				
Reg.03	0x04	MSTCLK_SRCSEL	M_BCLK_DIV						
Reg.04	0x01	//////////////////	//////////////////	//////////////////	//////////////////	M_LRCK_DIVH			
Reg.05	0x00	M_LRCK_DIVL							
Reg.06	0x00	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	DLL_POWER_DOWN	TDMIN_PDN_OFF	PUPDN_OFF
Reg.07	0x20	//////////////////	//////////////////	ADC_OSR					
Reg.08	0x10	LRCK_RATE_MODE				BCLK_INV_MODE	EQ_OFF	SPEED_MODE	MS_MODE
Reg.09	0x40	CHIPINI_LGTH							
Reg.10	0x40	PWRUP_LGTH							
Reg.11	0x00	CLEAR_RAM	FORCE_CSM			ADC34_MUTE_FLAG	ADC12_MUTE_FLAG	CSM_STATE	
Reg.12	0x00	//////////////////	//////////////////	//////////////////	//////////////////	INT_PULSESIZE		INT_ENABLE[1]	INT_ENABLE[0]
Reg.13	0x09	//////////////////	//////////////////	I2C_IBTHD_SEL	CLKDBL_PW_SEL	CLKDBL_PATH_SEL	LRCK_EXTEND	DELAY_SEL	
Reg.14	x	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////
Reg.15	x	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////
Reg.16	0x00	ADC34_DMIC_ON	ADC12_DMIC_ON	ADC34_DMIC_GAIN			ADC12_DMIC_GAIN		
Reg.17	0x00	SP_WL			SP_LRP	//////////////////	//////////////////	SP_PROTOCAL	
Reg.18	0x00	//////////////////	IBCLKLRCK_SEL	SP_SDOUT2_TRI	SP_SDOUT1_TRI	BCLKLRCK_TRI	CASCADE_CHIPFLAG	SDOUT_MODE	

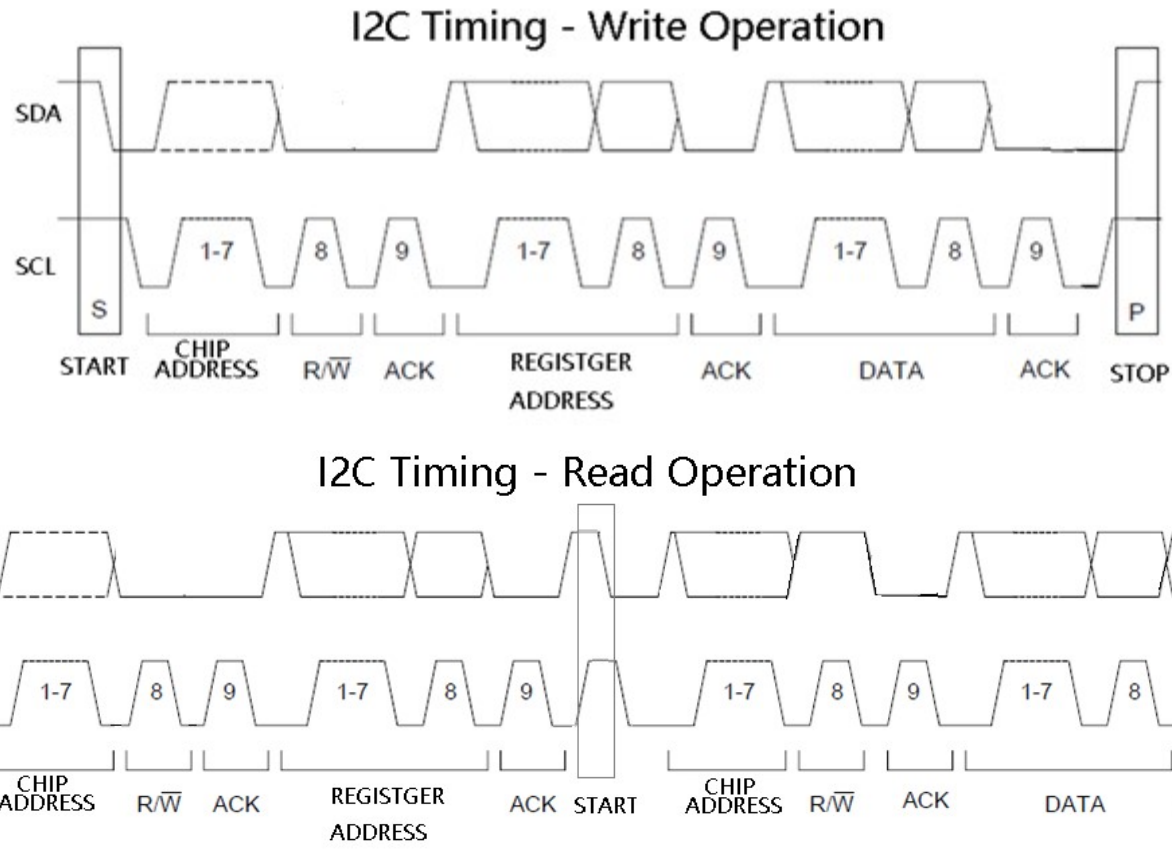
Reg.19	0x00	//////////////////	//////////////////	//////////////////	//////////////////	AUTOMUTE_ADC34_MUTE	AUTOMUTE_ADC12_MUTE	ADC_AUTOMUTE_SIZE	
Reg.20	0x00	ADC34_AUTOMUTE_NG				ADC34_AUTOMUTE_SEL		ADC4_SWMUTE_SEL	ADC3_SWMUTE_SEL
Reg.21	0x00	ADC12_AUTOMUTE_NG				ADC12_AUTOMUTE_SEL		ADC2_SWMUTE_SEL	ADC1_SWMUTE_SEL
Reg.22	0x00	//////////////////	//////////////////	//////////////////	//////////////////	ALC34_SEL		ALC12_SEL	
Reg.23	0x00	//////////////////	ALC_AUTOMUTE_GAIN			ALC_RAMP_RATE			
Reg.24	0xf7	ALC34_MAXLEVEL				ALC34_MINLEVEL			
Reg.25	0xf7	ALC12_MAXLEVEL				ALC12_MINLEVEL			
Reg.26	0x00	//////////////////	DIRECT_RAMP_RATE			//////////////////	//////////////////	ADC34_SAME_GAINON	ADC12_SAME_GAINON
Reg.27	0xbf	ADC4_DIRECT_DB							
Reg.28	0xbf	ADC3_DIRECT_DB							
Reg.29	0xbf	ADC2_DIRECT_DB							
Reg.30	0xbf	ADC1_DIRECT_DB							
Reg.31	x	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////
Reg.32	0x26	ADC34_CROSS		ADC34_USE_ADC12SW	ADC34_HPF_COEF2				
Reg.33	0x26	ADC34_4_POLARINV	ADC34_3_POLARINV	ADC34_OFFSET_REFRESHSW	ADC34_HPF_COEF1				
Reg.34	0x06	ADC12_CROSS		//////////////////	ADC12_HPF_COEF2				
Reg.35	0x26	ADC12_2_POLARINV	ADC12_1_POLARINV	ADC12_OFFSET_REFRESHSW	ADC12_HPF_COEF1				
Reg.36	0x11	EQ_B0S1S2_COEF							
Reg.37	0xff	EQ_B0S3S4_COEF							
Reg.38	0xff	EQ_B0S5S6_COEF							
Reg.39	0x0a	//////////////////	//////////////////	EQ_B0SIGN_COEF					
Reg.40	0xff	EQ_B1S1S2_COEF							
Reg.41	0xff	EQ_B1S3S4_COEF							
Reg.42	0xff	EQ_B1S5S6_COEF							
Reg.43	0x2a	//////////////////	//////////////////	EQ_B1SIGN_COEF					
Reg.44	0xff	EQ_B2S1S2_COEF							
Reg.45	0xff	EQ_B2S3S4_COEF							
Reg.46	0xff	EQ_B2S5S6_COEF							
Reg.47	0x2a	//////////////////	//////////////////	EQ_B2SIGN_COEF					
Reg.48	0xff	EQ_A1S1S2_COEF							
Reg.49	0xff	EQ_A1S3S4_COEF							
Reg.50	0xff	EQ_A1S5S6_COEF							
Reg.51	0x2a	//////////////////	//////////////////	EQ_A1SIGN_COEF					
Reg.52	0xff	EQ_A2S1S2_COEF							
Reg.53	0xff	EQ_A2S3S4_COEF							
Reg.54	0xff	EQ_A2S5S6_COEF							
Reg.55	0x2a	//////////////////	//////////////////	EQ_A2SIGN_COEF					
Reg.61	0x72	Chip_Type_ID1							
Reg.62	0x10	Chip_Type_ID0							
Reg.63	0x00	Chip_Version_ID							
Reg.64	0x80	PDN_ANA	VX2OFF	VX1SEL	//////////////////	VMIDLOW		VMIDSEL	
Reg.65	0x71	//////////////////	LVL_MICBIAS12			//////////////////	PGA12BIAS_SWH	ADC12BIAS_SWH	
Reg.66	0x71	//////////////////	LVL_MICBIAS34			//////////////////	PGA34BIAS_SWH	ADC34BIAS_SWH	
Reg.67	0x00	//////////////////	//////////////////	//////////////////	SELMIC1	MIC1GAIN_SETTING			
Reg.68	0x00	//////////////////	//////////////////	//////////////////	SELMIC2	MIC2GAIN_SETTING			
Reg.69	0x00	//////////////////	//////////////////	//////////////////	SELMIC3	MIC3GAIN_SETTING			
Reg.70	0x00	//////////////////	//////////////////	//////////////////	SELMIC4	MIC4GAIN_SETTING			
Reg.71	0x00	//////////////////	//////////////////	LP_VRP12	LP_PGA1OUT	LP_PGA1	LP_VCMMOD1	LP_FLASH1	LP_INT11
Reg.72	0x00	//////////////////	//////////////////	//////////////////	LP_PGA2OUT	LP_PGA2	LP_VCMMOD2	LP_FLASH2	LP_INT12
Reg.73	0x00	//////////////////	//////////////////	LP_VRP34	LP_PGA3OUT	LP_PGA3	LP_VCMMOD3	LP_FLASH3	LP_INT13
Reg.74	0x00	//////////////////	//////////////////	//////////////////	LP_PGA4OUT	LP_PGA4	LP_VCMMOD4	LP_FLASH4	LP_INT14

Reg.75	0xff	PDN_ADC12VREFGEN	PDN_MICBIAS12	PDN_PGA2	PDN_PGA1	PDN_MOD2	PDN_MOD1	MODTOP2_RST	MODTOP1_RST
Reg.76	0xff	PDN_ADC34VREFGEN	PDN_MICBIAS34	PDN_PGA4	PDN_PGA3	PDN_MOD4	PDN_MOD3	MODTOP4_RST	MODTOP3_RST

4.2 I2C Control Port

ES7210 supports standard I2C interface with maximum 400kbps rate. External host device can completely configure this device through writing to internal registers. The transfer rate of I2C can be up to 400kbps.

The following drawing illustrates the timing of I2C.



ES7210 has two chip address pins, AD1 and AD0, to set I2C chip address. The following table shows the chip address definition,

State of AD[1:0] pins	Chip Address
00	0x40(7bit) / 0x80 (8bit)
01	0x41(7bit) / 0x82 (8bit)
10	0x42(7bit) / 0x84 (8bit)
11	0x43(7bit) / 0x86 (8bit)

4.3 Soft Reset

In ES7210, register 0x00 is used for soft reset. If the reset bit is set to 1, the device will be in standby mode and has minimum power consumption.

It's important here that RESET bit must be cleared to 0 in normal mode. Otherwise, the device will be held in RESET state and can't be controlled with I2C.

The following table shows the soft reset register definition.

REGISTER 0X00 – RESET CONTROL, DEFAULT 00110010

Bit Name	Bit	Description
Reserved	7	Reserved
RST_MSTGEN	6	0 – normal 1 – reset master mode LRCK and SCLK
RST_ADC34_DIG	5	0 – normal 1 – reset ADC34
RST_ADC12_DIG	4	0 – normal 1 – reset ADC12
SEQ_DIS	3	Auto power sequence 0 – enable 1 – disable
RST_REGS	2	0 – normal 1 – reset control registers (except this bit)
RST_DIG	1	0 – normal 1 – reset digital (except control registers)
CSM_ON	0	Chip state machine power down 0 – disable 1 – enable

4.4 Time Control for Powerup / Chip initialization

In ES7210, there are two registers for device powerup time control. These two registers can be used to set the initialization time when device power up.

REGISTER 0X09 – TIME CONTROL 0 FOR CHIP INITIALIZATION, DEFAULT 010000

Bit Name	Bit	Description
CHIPINI_LGTH	7:0	Chip initial state period control: period=CHIPINI_LGTH/(LRCK frequency)

REGISTER 0X0A – TIME CONTROL 1 FOR CHIP INITIALIZATION, DEFAULT 010000

Bit Name	Bit	Description
PWRUP_LGTH	7:0	Power up state period control:

4.5 Master or Slave mode

ES7210 can operate in master mode or slave mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock. In slave mode, ES7210 detects MCLK/LRCK ratio automatically. In master mode, ES7210 generates LRCK and SCLK from MCLK according to the setting of LRCKDIV and BCLKDIV.

MS_MODE (Bit0 of register 0x08) is used to select master or slave mode.

MS_MODE = 0	ES7210 In Slave Mode
MS _MODE = 1	ES7210 In Master Mode

4.6 Speed Mode

ES7210 supports three speed modes: single speed mode and double speed mode. In single speed mode, LRCK frequency normally ranges from 8kHz to 48kHz; In double speed mode, LRCK frequency normally ranges from 64kHz to 96kHz;

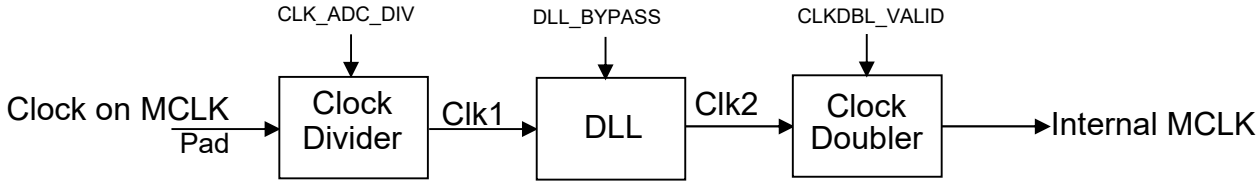
In slave mode, ES7210 detects speed mode automatically. In master mode, Bit[1] of register 0x08 is used to select proper speed mode.

REGISTER 0X08 – MODE CONFIG, DEFAULT 00010000

Bit Name	Bit	Description
SPEED_MODE	1	0 – Single speed mode 1 – Double speed mode

4.7 Internal clock diagram

The following diagram illustrates internal clock diagram in master mode. It is important note here that ES7210 can detect LRCK ratio automatically in slave mode



In this diagram, Clock divider has a ratio from 1 to 31. The frequency of CLK1 equals to MCLK/ratio, where ratio is the clock divider ratio.

The frequency of DLL output clock is 4 times of DLL input clock. So, if DLL_BYPASS is set to 0, the frequency of CLK2 should be 4×CLK1. If DLL_BYPASS is set to 1, the frequency of CLK2 should equal to CLK1.

The output frequency of clock doubler is 2 times of its input clock. So, if CLKDBL_VALID is set to 1, the frequency of internal MCLK should be 2×CLK2. If CLKDBL_VALID is 0, the internal MCLK should equal to CLK2.

The following is the definition for Clock divider ratio, DLL bypass mode and Clock doubler.

REGISTER 0X02 – MAIN CLOCK CONTROL, DEFAULT 00000010

Bit Name	Bit	Description
DLL_BYPASS	7	1 – bypass DLL 0 – not bypass DLL
CLKDBL_VALID	6	1 – use clock doubler 0 – not use clock doubler
Reserved	5	Reserved
CLK_ADC_DIV	4:0	ADC clock divide 0/1 – no divide 2 – divide by 2
		.... 31 – divide by 31

In single speed mode, the ratio between internal MCLK and LRCK must be higher than 512 while internal Equalizer enabled, and the ratio between internal MCLK and LRCK must be higher than 480 while internal Equalizer disabled. In single speed mode, the internal MCLK should be 16×ADC_OSR for the best anti-alias effect.

In double speed mode, the ratio between internal MCLK and LRCK must be higher than 256. ES7210 doesn't support Equalizer in double speed mode. In Double speed mode, the internal MCLK should be 8×ADC_OSR for the best anti-alias effect.

Following are some example for clock divider, DLL and clock doubler setting.

- Example 1, CPU/SOC provides 12.288MHz MCLK and 48KHz LRCK to ES7210, So the external MCLK/LRCK ratio is 256. In this clock condition, the clock divider ratio should be 1, and DLL should be bypassed. But clock doubler should be enabled to get internal clock which is 24.576MHz. Now the internal ADC clock is 24.576MHz, and it equals to 512 × LRCK.

- Example 2, CPU/SOC provides 18.432MHz MCLK and 48KHz LRCK to ES7210, So the MCLK/LRCK ratio is 384. In this clock condition, the clock divider ratio should be 3 to get 6.144MHz clock. DLL should be enabled to get 24.576MHz (4 × 6.144MHz) clock. The clock doubler should be disabled. Now the internal ADC clock is 24.576MHz, and it equals to 512 × LRCK.

Following is the register definition for internal clock management.

	default	B7	B6	B5	B4	B3	B2	B1	B0
Reg.01	0x20	//////////////////	EXT_BCLKLRCK_OFF	MASTER_CLK_OFF	ADC34_MCLK_OFF	ADC12_MCLK_OFF	ANA34_CLK_OFF	ANA12_CLK_OFF	MCLK_OFF
Reg.02	0x02	DLL_BYPASS	CLKDBL_VALID	//////////////////	CLK_ADC_DIV				
Reg.03	0x04	MSTCLK_SRCSEL	M_BCLK_DIV						
Reg.04	0x01	//////////////////	//////////////////	//////////////////	//////////////////	M_LRCK_DIVH			
Reg.05	0x00	M_LRCK_DIVL							
Reg.06	0x00	//////////////////	//////////////////	//////////////////	//////////////////	//////////////////	DLL_POWER_DOWN	TDMIN_PDN_OFF	PUPDN_OFF
Reg.07	0x20	//////////////////	//////////////////	ADC_OSR					
Reg.08	0x10	LRCK_RATE_MODE				BCLK_INV_MODE	EQ_OFF	SPEED_MODE	MS_MODE

1. Clock On/Off

Register0x01 is used for clock on or off. Internal clock can be turned off when ADC will be in standby or power down mode, this will reduce the current consumption. In normal mode, these clocks must be turned on.

REGISTER 0X01 – CLOCK OFF, DEFAULT 00100000

Bit Name	Bit	Description
Reserved	7	Reserved
EXT_SCLKLRCK_OFF	6	0 – turn on slave mode SCLK and LRCK i 1 – turn off slave mode SCLK and LRCK
MASTER_CLK_OFF	5	0 – turn on master mode SCLK and LRC 1 – turn off master mode SCLK and LRC
ADC34_MCLK_OFF	4	0 – turn on ADC34 master clock 1 – turn off ADC34 master clock
ADC12_MCLK_OFF	3	0 – turn on ADC12 master clock 1 – turn off ADC12 master clock
ANA34_CLK_OFF	2	0 – turn on ADC34 analog clock 1 – turn off ADC34 analog clock
ANA12_CLK_OFF		0 – turn on ADC12 analog clock

2. CLK_ADC_DIV

The CLK_ADC_DIV control bits in register0x02 is used for MCLK clock divider. This clock divider has a ratio from 1 to 31, to generate internal MCLK from external MCLK(clock signal on MCLK pin).

3. DLL

The clock signal output from MCLK clock divider will be inputted into internal DLL. The frequency of DLL output clock is four times of input clock. DLL can be by-passed if register0x02.bit7 (DLL_BYPASS) is set to 1.

If DLL is bypassed, the internal MCLK equals to the output clock of MCLK clock divider.

DLL can be powered down if register0x06.bit2(DLL_POWER_DOWN) is set to 1. Please note that MCLK must be stop before DLL power down.

4. Clock Doubler

The DLL output should be inputted into internal clock doubler which is a frequency doubling circuit. This clock doubler circuit can be disabled as well. Bit6 of register 0x02 is used to enable or disable clock doubler. If clock doubler is disabled, the internal MCLK equals to the DLL output clock. Then this internal MCLK should be used as internal ADC MCLK and analog clock.

5. BCLKDIV definition

In slave mode, BCLK(SCLK) is provided by host controller, such as CPU,MCU or DSP, etc., and BCLK(SCLK) is input pin.

In master mode, BCLK(SCLK) is output pin and ES7210 must generate a proper BCLK(SCLK) clock to host controller. BCLK(SCLK) is derived from MCLK clock by SCLK clock divider.

The SCLK clock divider has a multiplexer to select MCLK source. Bit7(MSTCLK_SRCSEL) of register0x03 is used to select MCLK source. If MSTCLK_SRCSEL is cleared to 0, the clock signal on MCLK pin is selected as source for SCLK clock divider. Otherwise, the internal clock from clock doubler is used as source for SCLK clock divider. The SCLK clock divider has a divider ratio from 1 to 127. Bit[6:0](M_SCLK_DIV) of Register 0x02 is used to set this divider ratio.

REGISTER 0X03 – MASTER CLOCK CONTROL, DEFAULT 00000100

Bit Name	Bit	Description
MSTCLK_SRCSEL	7	0 – MCLK from pad 1 – MCLK from clock doubler
M_SCLK_DIV	6:0	SCLK divide (use with MSTCLK_SRCSEL 0/1 – no dived 2 – divide by 2

6. LRCKDIV definition

In slave mode, LRCK pin is an input pin and host controller send proper LRCK clock to ES7210. ES7210 can detect MCLK/LRCK ratio automatically.

In master mode, LRCK is an output pin. ES7210 will generate a proper LRCK clock to host controller. LRCK is derived from MCLK clock by LRCK clock divider. Here, the MCLK clock is the output of multiplexer which is controlled by MSTCLK_SRCSEL (register0x03.bit7).

Register0x04 and Register0x05 are used to set the LRCK divider ratio.

7. BCLK INVERTED

In normal I2S/LJ/DSP format, the data bit is always transmitted at BCLK(SCLK) falling edge, and host controller receive data bit at BCLK(SCLK)rising edge. But some host controller maybe need to receive data bit at BCLK(SCLK) falling edge. Bit3(SCLK_INV_MODE) of register 0x08 is used to invert BCLK edge for transmit/receive data bit.

4.8 The Sample code for register configuration of Clock condition

The following sample code is an example for the clock register configuration in typical MCLK and LRCK condition.

```
static const struct _clock_coeff es7210_normal_clock_coeff[] =  {
    //mclk     , lrck,   ss_ds,  clk_adc_div,  dll_bypass,  doubler_enable,  osr,  mclk_src,  lrckh,  lrckl
    {12288000,  96000,   1,      1,           1,           1,               32,   0,         0x00,   0x80},
    {12288000,  48000,   0,      1,           1,           1,               32,   0,         0x01,   0x00},
    {12288000,  32000,   0,      3,           0,           0,               32,   0,         0x01,   0x80},
    {12288000,  24000,   0,      1,           1,           0,               32,   0,         0x02,   0x00},
    {12288000,  16000,   0,      3,           1,           1,               32,   0,         0x03,   0x00},
    {12288000,  12000,   0,      2,           1,           0,               32,   0,         0x04,   0x00},
    {12288000,  8000 ,   0,      3,           1,           0,               32,   0,         0x06,   0x00},

    {11298600,  88200,   1,      1,           1,           1,               32,   0,         0x00,   0x80},
    {11298600,  44100,   0,      1,           1,           1,               32,   0,         0x01,   0x00},
    {11298600,  22050,   0,      1,           1,           0,               32,   0,         0x02,   0x00},
    {11298600,  11025,   0,      2,           1,           0,               32,   0,         0x04,   0x00},

    {16384000,  64000,   1,      1,           1,           0,               32,   0,         0x01,   0x00},
    {16384000,  32000,   0,      1,           1,           0,               32,   0,         0x02,   0x00},
    {16384000,  16000,   0,      2,           1,           0,               32,   0,         0x04,   0x00},
    {16384000,  8000 ,   0,      4,           1,           0,               32,   0,         0x08,   0x00},

    {19200000,  96000,   1,      5,           0,           1,               40,   0,         0x00,   0xc8},
    {19200000,  64000,   0,      5,           0,           1,               30,   0,         0x01,   0x2c},
    {19200000,  48000,   0,      5,           0,           1,               40,   0,         0x01,   0x90},
    {19200000,  32000,   0,      5,           0,           0,               30,   0,         0x02,   0x58},
    {19200000,  24000,   0,      10,          0,           1,               40,   0,         0x03,   0x20},
    {19200000,  16000,   0,      10,          0,           0,               30,   0,         0x04,   0x80},
    {19200000,  12000,   0,      20,          0,           1,               40,   0,         0x06,   0x40},
    {19200000,  8000 ,   0,      30,          0,           1,               40,   0,         0x09,   0x60},

    {4096000 ,  16000,   0,      1,           1,           0,               32,   0,         0x01,   0x00},
    {4096000 ,  8000 ,   0,      1,           1,           0,               32,   0,         0x02,   0x00},

};
```

4.9 Serial Digital Audio Format

ES7210 supports I2S, Left Justified, DSP-A and DSP-B serial digital audio format with resolution from 16bits to 32bits.

The following is the register definition of serial digital audio format,

	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg0x11	SP_WL			SP_LRP			SP_PROTOCAL		0x00
	The data format of serial data port 000 - 24-bit 001 - 20-bit 010 - 18-bit 011 - 16-bit 100 - 32-bit			I2S/Left Justify case: 0: L/R normal polarity Left/Right=High/Low (LJ) Left/Right=Low/High (I2S) 1: L/R invert polarity Left/Right=Low/High (LJ) Left/Right=High/Low (I2S) DSP mode case: 0: Mode A, MSB is available on 2nd SCLK rising edge after LRCK rising edge 1: Mode B, MSB is available on 1st SCLK rising edge after LRCK rising edge			The protocol of serial data port 00 - I2S 01 - LJ 10 - not allowed 11 - DSP		

The following diagram illustrates the timing of serial digital audio format.

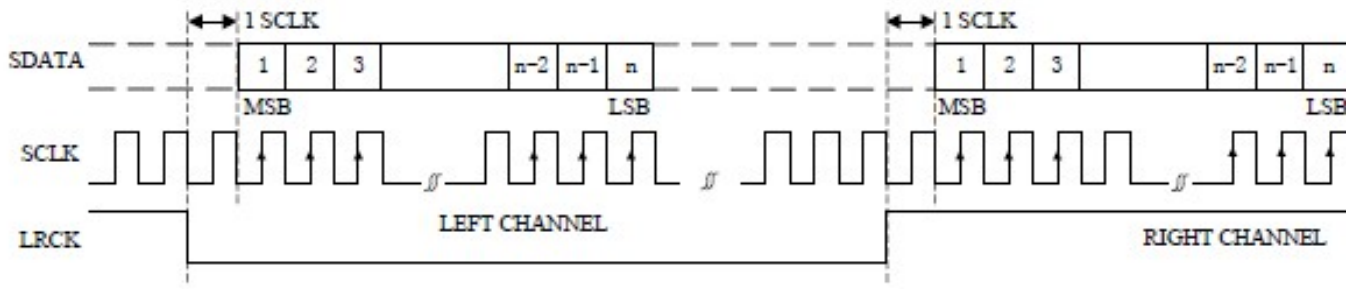


Figure 2 I²S Serial Audio Data Format Up To 24-bit

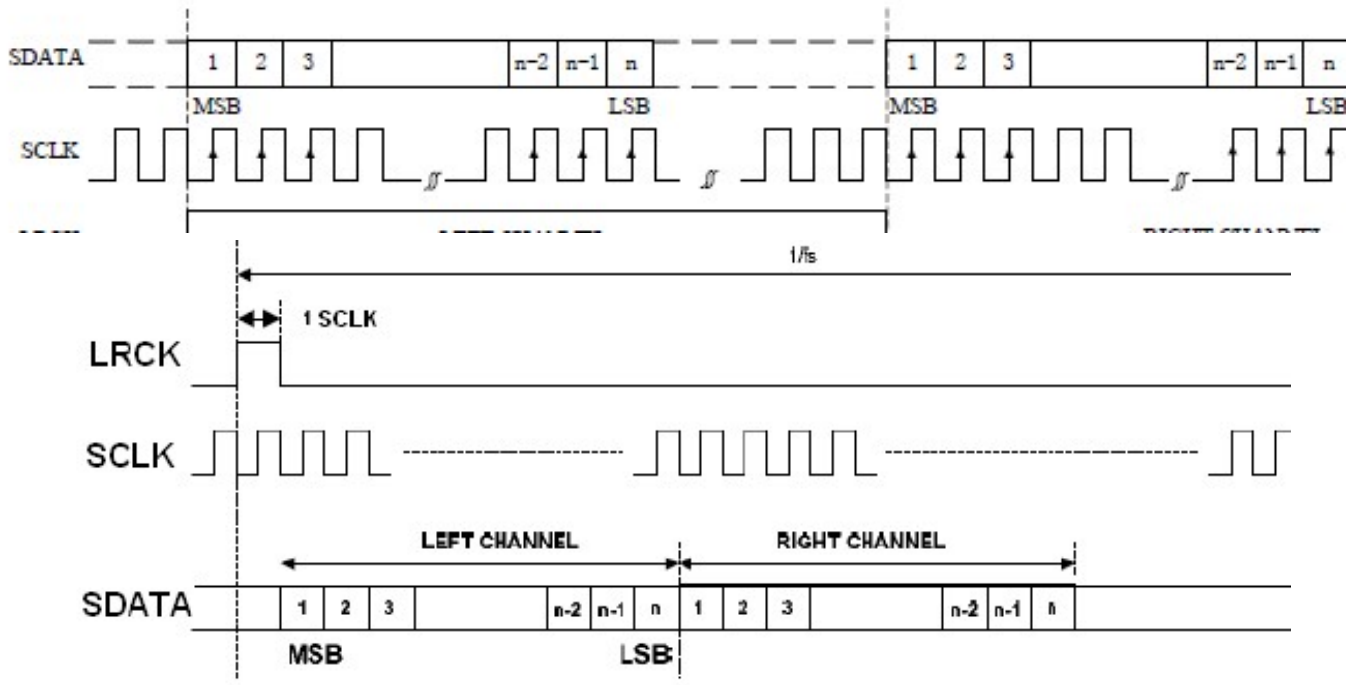
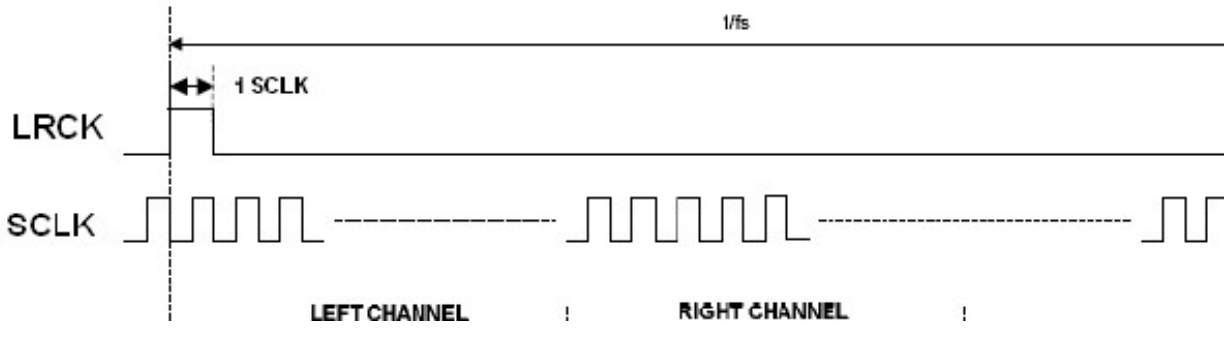


Figure 4 DSP/PCM Mode A

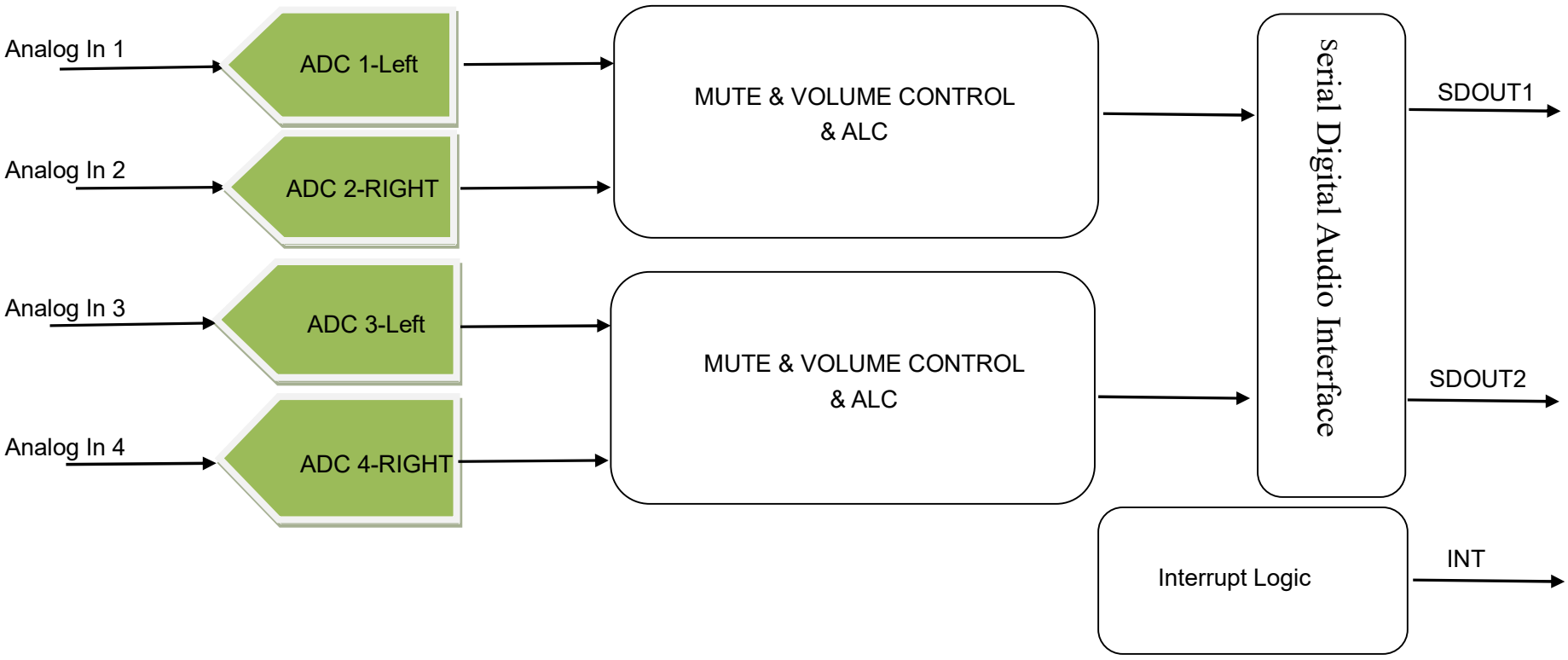


If application system doesn't need to get ADC data, some register control bits can be used to set the ADC data out to tri-state. BIT5(SP_SDOUT2_TRI) and BIT4(SP_SDOUT1_TRI) are used to set SDOUT1 and SDOUT2 pins to tri-state. BIT3(BCLKLRCK_TRI) is used to set LRCK and SCLK pins to tri-state mode.

	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg0x12		IBCLKLRCK_SEL	SP_SDOUT2_TRI	SP_SDOUT1_TRI	BCLKLRCK_TRI	CASCADE_CHIPFLAG	SDOUT_MODE		
		0-according to M/S mode 1-master mode's bclk/lrck as internal bclk/lrck before work	0 - original data 1 - SDOUT2 is tri state output	1 - original data 1 - SDOUT1 is tri state output	0 - original data 1 - BCLK/LRCK is tri state output	When set SDOUT_MODE=11 0 - last ES7210 in TDM 1 - not the last ES7210 in TDM	00:ADC12->SDOUT1,ADC34->SDOUT2 01: x1 LRCK TDM(DSP mode) 10: x1 LRCK TDM(I2S/LJ) 11: xN LRCK TDM		0x00

4.10 Digital Path

Below diagram shows the digital path of ES7210.



4.10.1 MUTE and AUTO MUTE

ES7210 has mute control which can mute ADC output. When mute control is set to 1, ADC always outputs all 0 or 1. Also, ES7210 has auto mute feature. If auto mute is enabled, ES7210 detect the input level automatically. ADC will be mute if the input level is lower than the threshold within a long duration. User can decide the threshold level and duration time.

REGISTER 0X13 – ADC AUTOMUTE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
AUTOMUTE_ADC34_MUTE	3	0 – normal 1 – auto mute ADC34
AUTOMUTE_ADC12_MUTE	2	0 – normal 1 – auto mute ADC12
ADC_AUTOMUTE_SIZE	1:0	auto mute window size 00 – 2048 LRCK 01 – 4096 LRCK 10 – 8192 LRCK 11 – 16384 LRCK

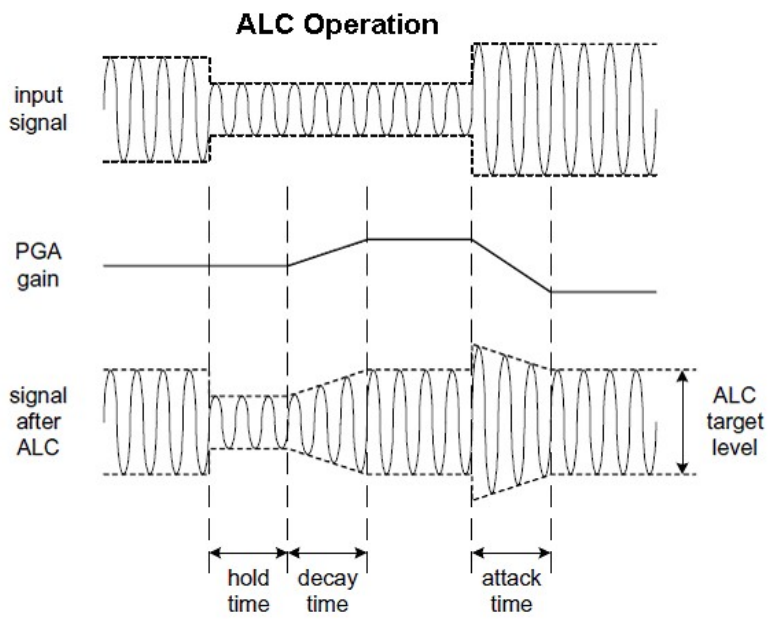
REGISTER 0X15 – ADC12 MUTE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC12_AUTOMUTE_NG	7:4	ADC auto mute noise gate 0000 – -96dB 0001 – -90dB 0010 – -84dB 0011 – -78dB 0100 – -72dB 0101 – -66dB 0110 – -60dB 0111 – -54dB 1000 – -51dB 1001 – -48dB 1010 – -45dB 1011 – -42dB 1100 – -39dB 1101 – -36dB 1110 – -33dB 1111 – -30dB
ADC12_AUTOMUTE_SEL	3:2	00 – normal 10 – select left data as left channel automute 01 – select right data as right channel automute 11 – select stereo automute
ADC2_SWMUTE_SEL	1	0 – normal 1 – mute ADC2 output to all 0
ADC1_SWMUTE_SEL	0	0 – normal 1 – mute ADC1 output to all 0

4.10.2 ALC and Volume Control

In applications that offer a recording feature, ALC is often desirable to keep the recorded signal at a constant level. For example, if recording voice, the signal may vary a great deal depending on how loud the user speaks or how close to the mouth the microphone is held. This will result in a recorded signal that is difficult to listen to when played back.

The purpose of the ALC is to keep a constant output volume irrespective of the input signal level. This is achieved by continually adjusting the PGA gain so that the signal level at the ADC output remains constant.



Setting up the ALC to be optimal for each recorded source such as voice, classical music, pop music, etc. is quite a complex process. Recommended setups have been provided as a base to work from. The resultant effect is very subjective and may vary between applications. Some further modifications may be required to optimize the feature for a specific application but the recommended settings should offer suitable solutions in most cases.

In ES7210,there are two ALC Control, ALC12_SEL and ALC34_SEL,Each ALC Control has four modes, ALC OFF, ALC on left channel, ALC on right channel and stereo ALC.

	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg0x16					ALC34_SEL		ALC12_SEL		
					00: alc off 10: left channel alc on 01: right channel alc on 11: stereo alc on		00: alc off 10: left channel alc on 01: right channel alc on 11: stereo alc on		0x00

If ALC is enabled, ES7210 will detect the input level automatically and update digital level dynamically. User can decide the threshold level, duration time, target level, etc.,.

	B7	B6	B5	B4	B3	B2	B1	B0	default
Reg0x1B	ADC4_DIRECT_DB								
Reg0x1C	ADC3_DIRECT_DB								
Reg0x1D	ADC2_DIRECT_DB								
Reg0x1E	ADC1_DIRECT_DB								
	ADC direct dB when ALC close,ALC max gain when ALC open 00h — -95.5dB 01h — -95dB …… BFh — 0dB(default) …… FFh — +32dB								0xBF

4.10.3 Interrupt

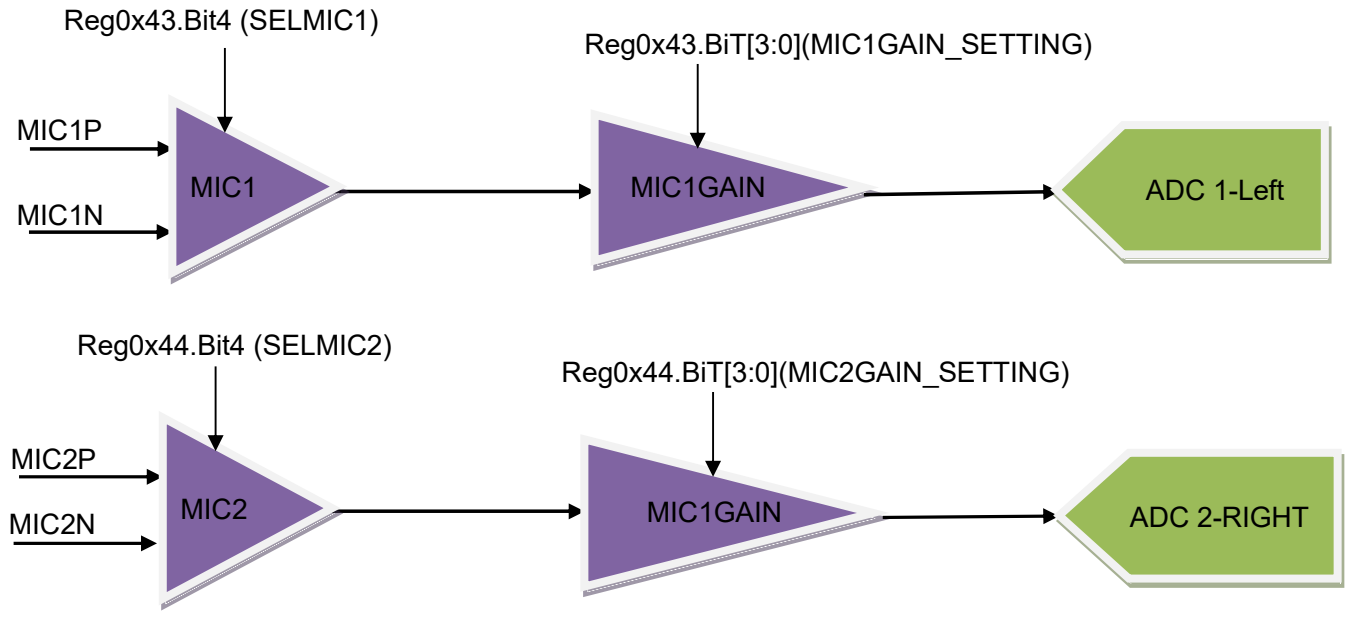
ES7210 has mute control which can Interrupt output. When Interupt control:INT_ENABLE is set to 1, ADC can output low pulse, pulse time is controlled by the INT_PULSESIZE.

REGISTER 0X0C – INTERRUPT CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
INT_PULSESIZE	3:2	00 – 256 LRCK 01 – 128 LRCK 10 – 32 LRCK 11 – 8 LRCK
INT_ENABLE[1]	1	0 – disable ADC34 interrupt 1 – enable ADC34 interrupt
INT_ENABLE[0]	0	0 – disable ADC12 interrupt 1 – enable ADC12 interrupt

4.11 Analog input

Below diagram shows the analog input path of ES7210.



In ES7210, there are four stereo differential analog inputs, Mic1P-Mic1N, Mic2P-Mic2N, Mic3P-Mic3N and Mic4P-Mic4N, followed by quad PGAs with gain range from 0dB to +37.5dB. SELMICX (bit4 of register 0x43~46) is used to enable or disable these differential inputs. If SELMICX = 1'b, the differential inputs is enabled. In register 0x43~46, Bit[3:0] are used to set the PGA gain. Below table shows the definition of PGA gain.

REGISTER 0X43 – MIC1 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC1	4	0 – deselect 1 – select MIC1P and MIC1N as input
MIC1GAIN_SETTING	3:0	0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

REGISTER 0X44 – MIC2 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC2	4	0 – deselect 1 – select MIC2P and MIC2N as input
MIC2GAIN_SETTING	3:0	0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB

REGISTER 0X45 – MIC3 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC3	4	0 – deselect 1 – select MIC3P and MIC3N as input
MIC3GAIN_SETTING	3:0	0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB

REGISTER 0X46 – MIC4 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC4	4	0 – deselect 1 – select MIC4P and MIC4N as input
MIC4GAIN_SETTING	3:0	0 – 0dB
		1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

4.12 MICBIAS VOLTAGE

Each ES7210 device has two MICBIAS voltage, MICBIAS12 and MICBIAS34, which can be microphone power supply. MICBIAS12 and MICBIAS34 all can drive two electret or MEMS microphones.

Some register control bits are used for set MICBIAS voltage level.

REGISTER 0X41 – MIC1/2 BIAS, DEFAULT 01110001

Bit Name	Bit	Description
Reserved	7	Reserved
LVL_MICBIAS12	6:4	111 – 2.87V (VDDM=3.3V) 110 – 2.78V 101 – 2.66V 100 – 2.55V 011 – 2.45V 010 – 2.36V 001 – 2.26V 000 – 2.18V

REGISTER 0X42 – MIC3/4 BIAS, DEFAULT 01110001

Bit Name	Bit	Description
Reserved	7	Reserved
LVL_MICBIAS34	6:4	111 – 2.87V (VDDM=3.3V) 110 – 2.78V 101 – 2.66V 100 – 2.55V 011 – 2.45V 010 – 2.36V

Bit6(PDN_MICBIAS12) of register 0x4b is the on/off control bit of MICBIAS12. Bit6(PDN_MICBIAS34) of register 0x4c is the on/off control bit of MICBIAS34. If PDN_MICBIAS12 is set to 1, MICBIAS12 voltage will be shut down. If PDN_MICBIAS34 is set to 1, MICBIAS34 voltage will be shut down as well.

4.13 Power Control

In ES7210, some registers are used for power control. The following shows the power control register definition.

REGISTER 0X47 – MIC1 LOW POWER, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
LP_VRP12	5	0 – normal 1 – low power
LP_PGA1OUT	4	0 – normal 1 – low power
LP_PGA1	3	0 – normal 1 – low power
LP_VCMMOD1	2	0 – normal 1 – low power
LP_FLASH1	1	0 – normal 1 – low power
LP_INT11	0	0 – normal 1 – low power

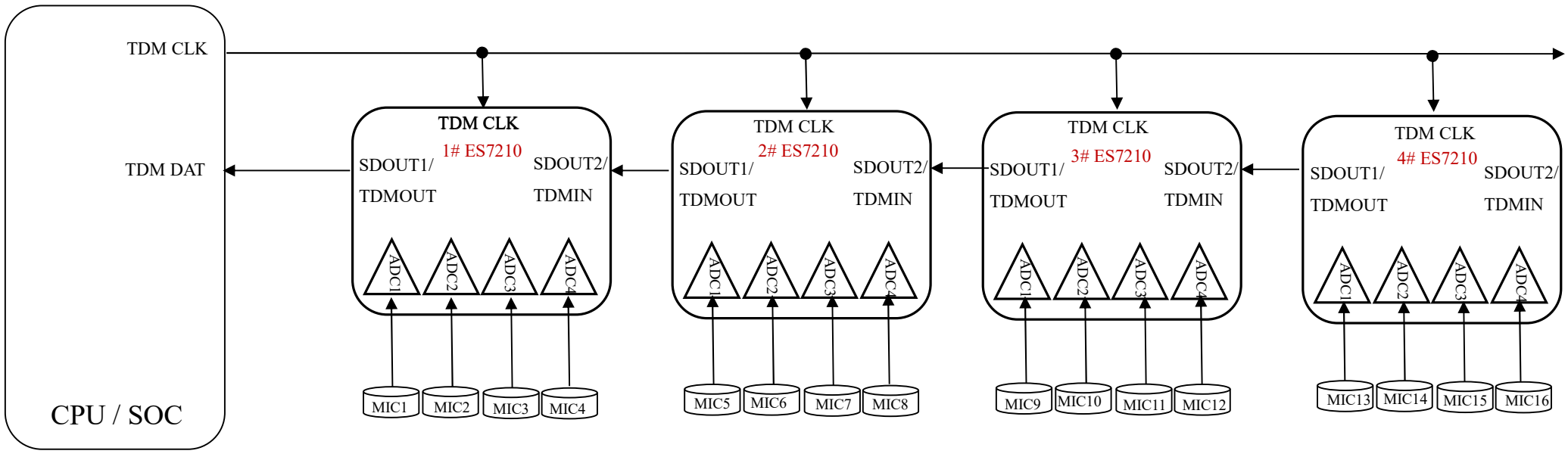
REGISTER 0X4B – MIC1/2 POWER DOWN, DEFAULT 11111111

Bit Name	Bit	Description
PDN_ADC12VREFGEN	7	0 – normal 1 – MIC1/2 reference power down
PDN_MICBIAS12	6	0 – normal 1 – MICBIAS12 power down
PDN_PGA2	5	0 – normal 1 – PGA2 power down
PDN_PGA1	4	0 – normal 1 – PGA1 power down
PDN_MOD2	3	0 – normal 1 – ADC2 power down
PDN_MOD1	2	0 – normal 1 – ADC1 power down
MODTOP2_RST	1	0 – normal 1 – reset ADC2 state machine to power down state
MODTOP1_RST	0	0 – normal 1 – reset ADC1 state machine to power down state

4.14 TDM Mode

ES7210 supports TDM mode to cascade multiple ES7210 devices. It has two TDM modes, 1×FS TDM mode and N×FS TDM mode. ES7210 supports I2S, Left Justified and DSP format in either TDM mode.

In TDM mode, up to 4 ES7210 devices can be cascaded, and up to 16 channels ADC data will be presented in one LRCK cycle. No Phase difference exists between these ADC data. The TDM mode makes ES7210 be ideal for microphone array application. The Below Diagram illustrates four ES7243 cascaded in TDM mode.



SDOUT_MODE (Bit[1:0]of Register 0x12) is used to enable or disable TDM mode. If TDM mode is enabled, in each ES7210 device, the SDOUT1 pin is used as TDM data out pin and SDOUT2 pin is used as TDM data input pin.

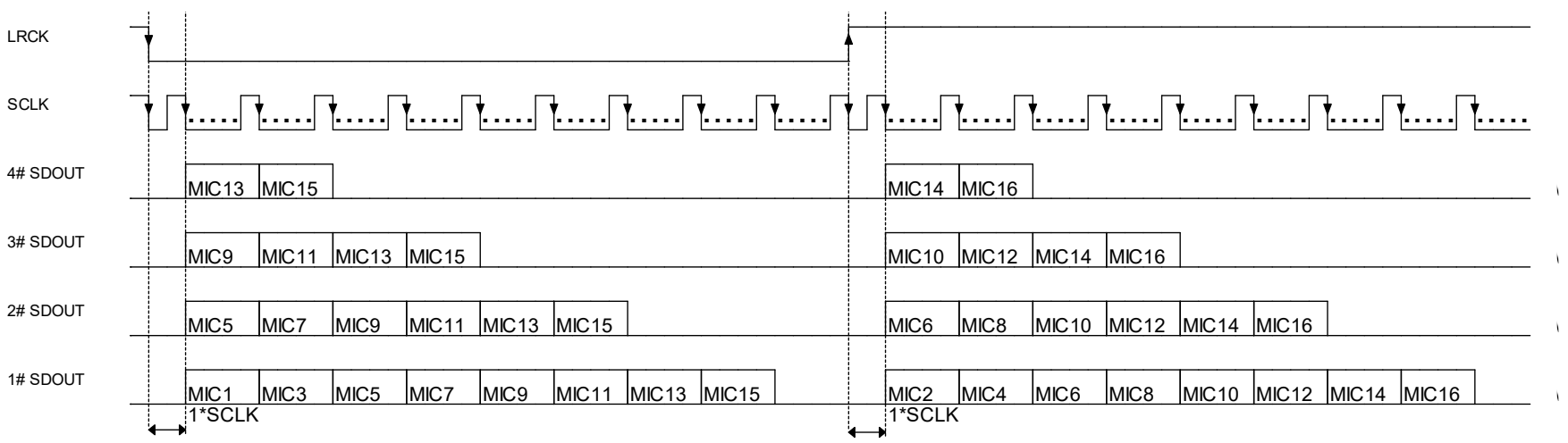
SDOUT_MODE = 00	TDM DISABLED	In this mode, TDM is disabled. In each device, the data of ADC1 & ADC2 output on SDOUT1, and the data of ADC3 & ADC4 output on SDOUT2.
SDOUT_MODE = 01	1×FS TDM mode, for DSP-A/B mode	In this mode, TDM is enabled. In each device, the SDOUT1 pin is used as TDM dataout, and the SDOUT2 is used as TDM datain.
SDOUT_MODE = 10	1×FS TDM mode, for I2S / LJ mode	
SDOUT_MODE = 11	N×FS TDM mode, for I2S, LJ or DSP mode	

4.14.11×FS TDM Mode Timing

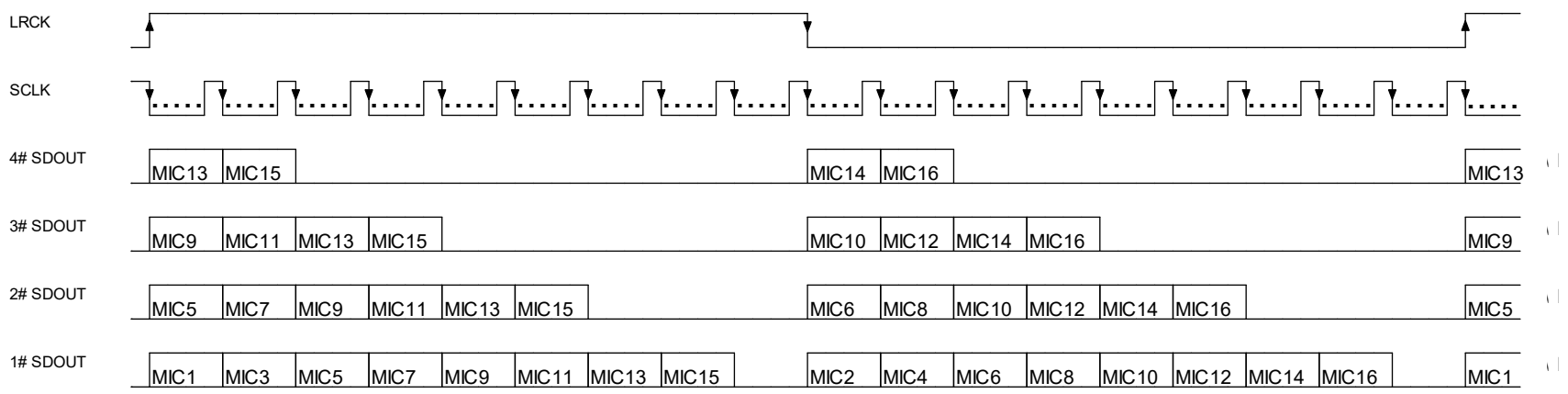
In 1×FS TDM mode, ES7210 can work in master or slave mode. In 1×FS TDM mode, ADC sample rate in ES7210 is equal to the LRCK frequency of I2S/TDM interface. For example, if CPU send a 16kHZ LRCK clock to ES7210, ES7210 will do analog-to-digital conversion at 16kHz sample rate in 1×FS TDM mode.

Here is an example that illustrates TDM clock timing and data slot while four ES7210 device cascaded in 1×FS TDM mode. In 1×FS TDM mode, each of ADC will do analog-to-digital conversion at the same moment, so that there is no phase difference between these ADC data.

The following diagram illustrates the timing and data slot of 1×FS TDM mode in I2S and Left Justified digital audio format.

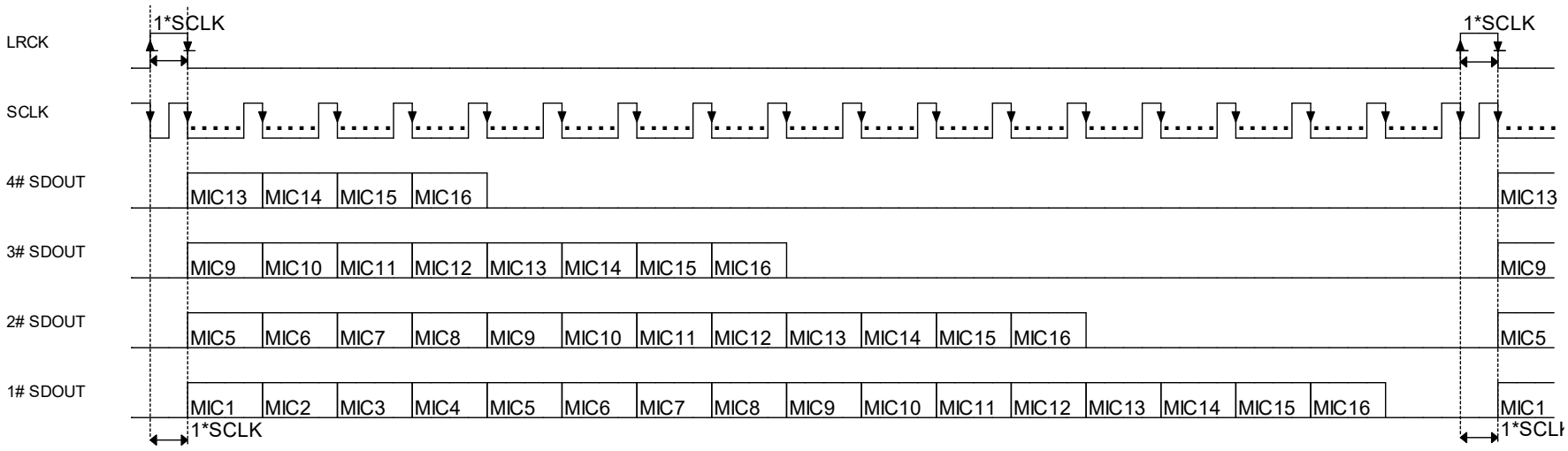


TDM Timing and Data Slot In I2S 1×FS TDM mode

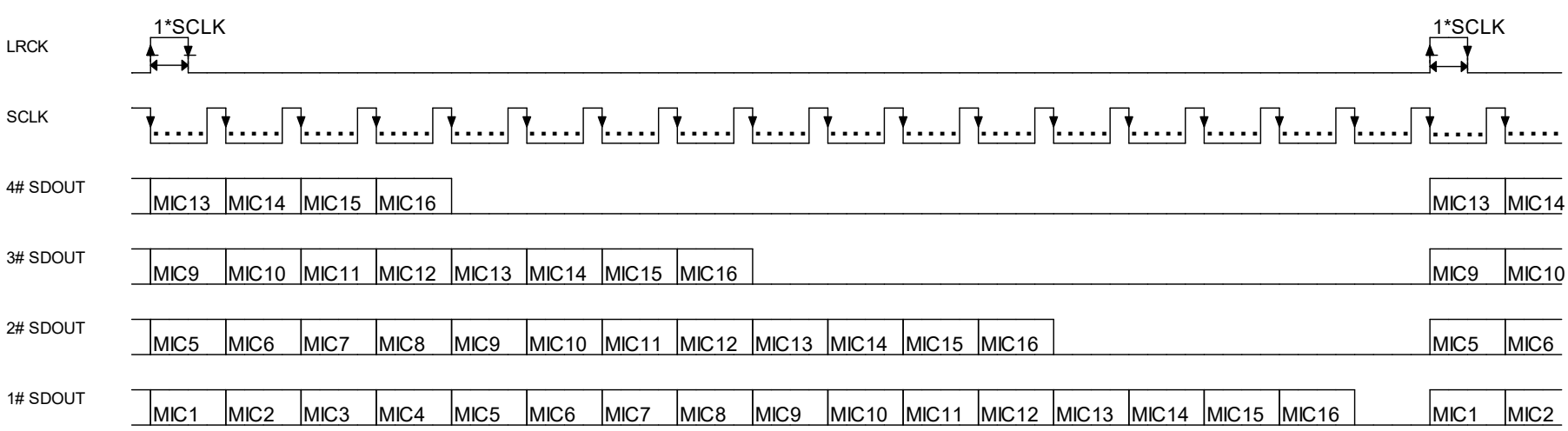


TDM Timing and Data Slot In Left Justified 1×FS TDM mode

The following diagram illustrates the timing and data slot of 1×FS TDM mode in DSP-A and DSP-B digital audio format.



TDM Timing and Data Slot In DSP-A TDM Mode



TDM Timing and Data Slot In DSP-B TDM Mode

4.14.2 N×FS TDM Mode Timing

In N×FS TDM mode, ES7210 can work in master or slave mode. In N×FS TDM mode, each ES7210 works in FS sample rate while N×FS sample rate exists in the TDM/I2S interface, where N equals to twice as much as number of ES7210 device. For example, if system needs to get ADC data in 16kHz sample rate while two ES7210 devices are cascaded for voice capture, in N×FS TDM mode, CPU must send 4×16kHz (64kHz) LRCK frequency to ES7210. Each of ES7210 device will do analog-to-digital conversion in 16kHz sample rate, and will transmit ADC data with higher speed(4×16kHz) to ensure CPU get all ADC data in one cycle of 16kHz sample rate. Each of ADC will do analog-to-digital conversion at the same moment, so that there is no phase difference between these ADC data.

It's important here that there is a start flag bit in the ADC data. In the first data slot of N×FS TDM mode, the start flag bit is set to one, and start flag bit will be clear to zero in others TDM data slot. If the data length is 16bits or 24bits, the LSB is the start flag bit. If the data length is 32bits, the bit8 is the start flag bit.

Bit[7:4](LRCK_RATE_MODE) in register 0x08 configs N coefficient. Please refer to below table for N coefficient.

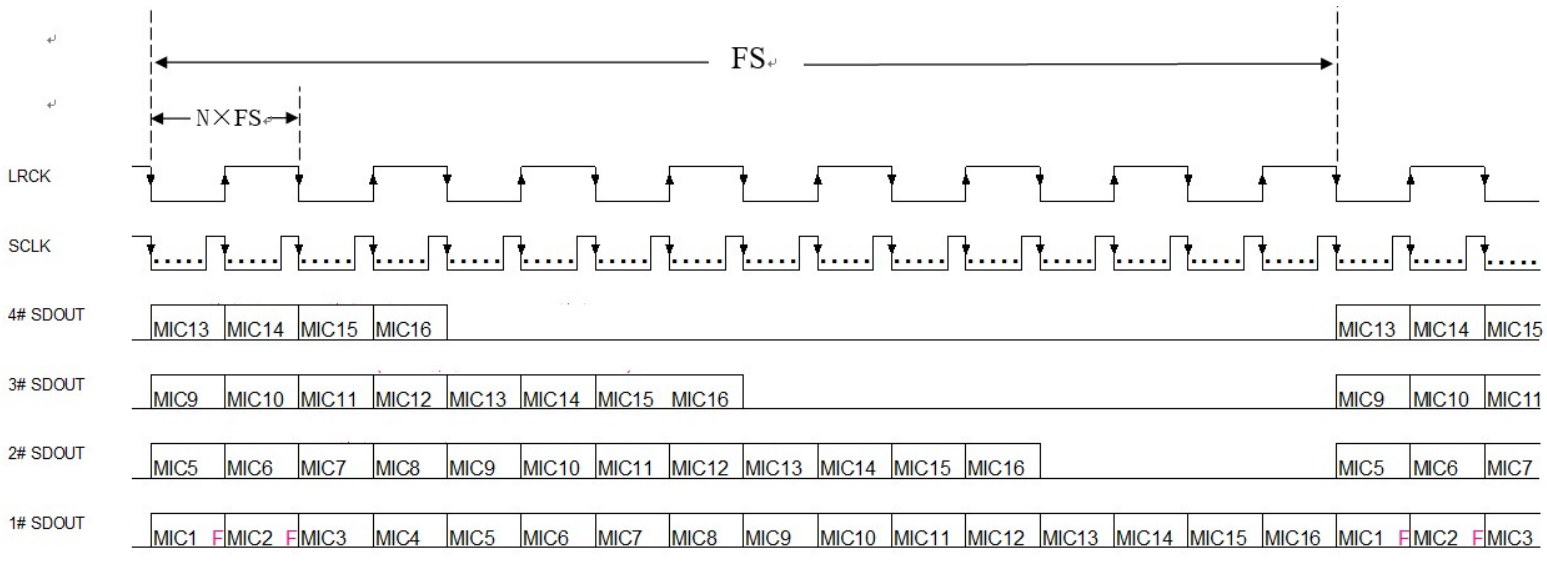
REGISTER 0X08 – MODE CONFIG, DEFAULT 00010000

Bit Name	Bit	Description
LRCK_RATE_MODE	7:4	When set SDOUT_MODE=11 0/1 – 2 channels 2 – 4 channels 3 – 6 channels 4 – 8 channels 5 – 10 channels 6 – 12 channels 7 – 14 channels 8 – 16 channels Other – reserved

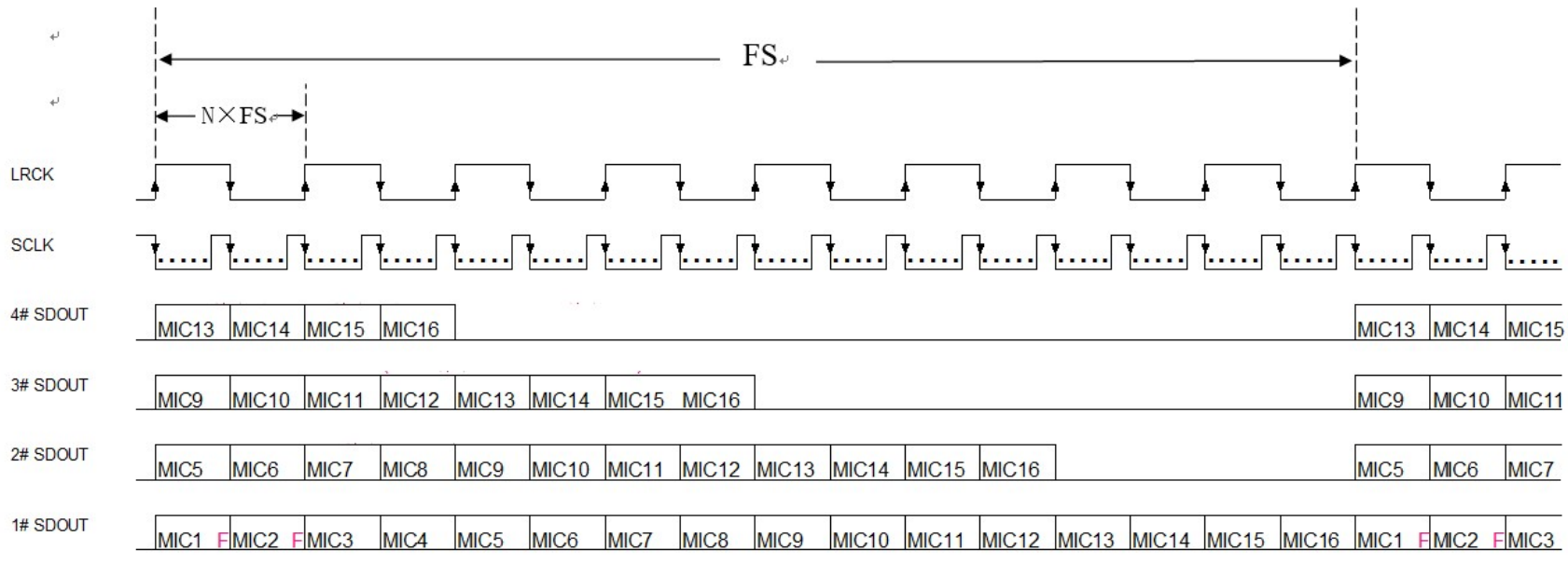
Here "channels" is the number of microphones in TDM mode. If only two microphones are used for voice capture, LRCK_RATE_MODE can be 0 or 1. If 16 microphones are used, LRCK_RATE_MODE should be 8. Each of ES7210 device in TDM link will do analog-to-digital conversion in (N×FS / LRCK_RATE_MODE) sample rate. So LRCK_RATE_MODE is very important for N×FS TDM mode.

Here is an example that illustrates TDM clock timing and data slot while four ES7210 device cascaded in N×FS TDM mode.

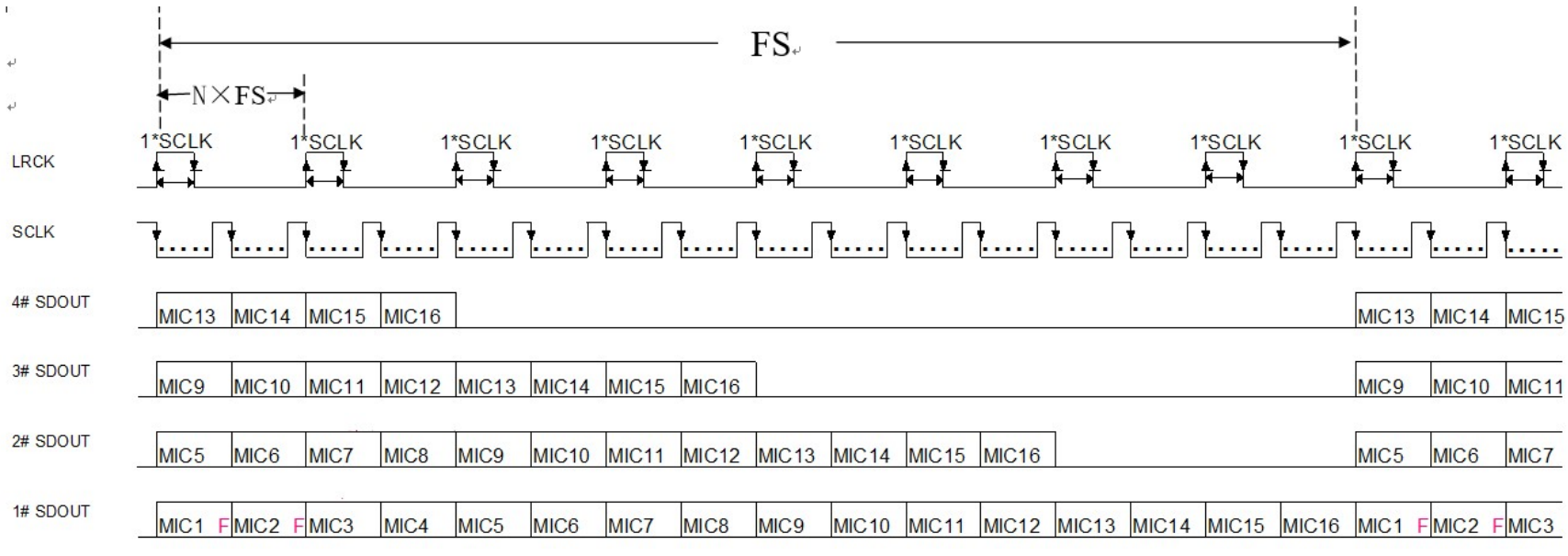
The following diagram illustrates the timing and data slot of N×FS TDM mode in I2S or Left Justified digital audio format.



TDM Timing and Data Slot In I2S N×FS TDM Mode, where F is the flag bit.



TDM Timing and Data Slot In Left Justified N×FS TDM Mode, where F is the flag bit.

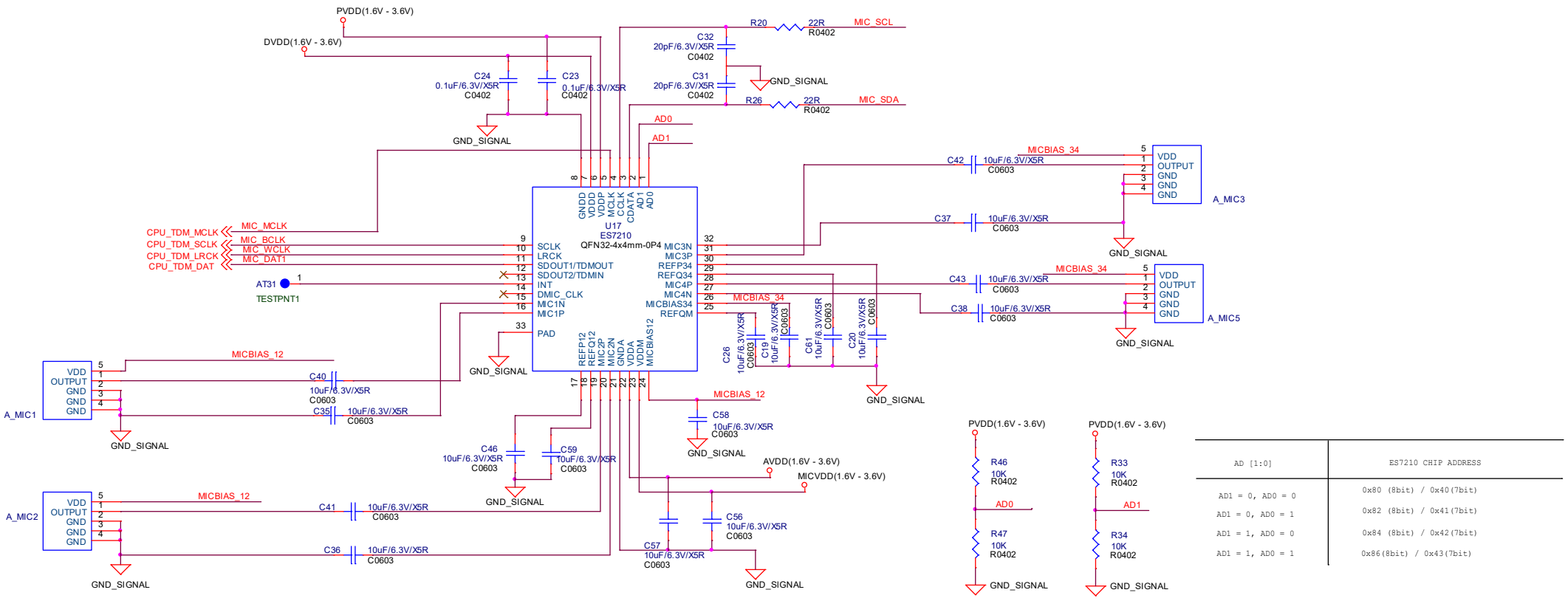


TDM Timing and Data Slot In DSP-A/B N×FS TDM Mode, where F is the flag bit.

4.14.3 TDM Mode With One ES7210 Device

If there are four microphones in application system, only one ES7210 device will be used for voice capture. If TDM is enabled, the SDOUT1 pin is used as TDM data out, and the SDOUT2 can be float or pulled down to ground.

The below circuit schematic illustrates TDM mode of standalone ES7210.

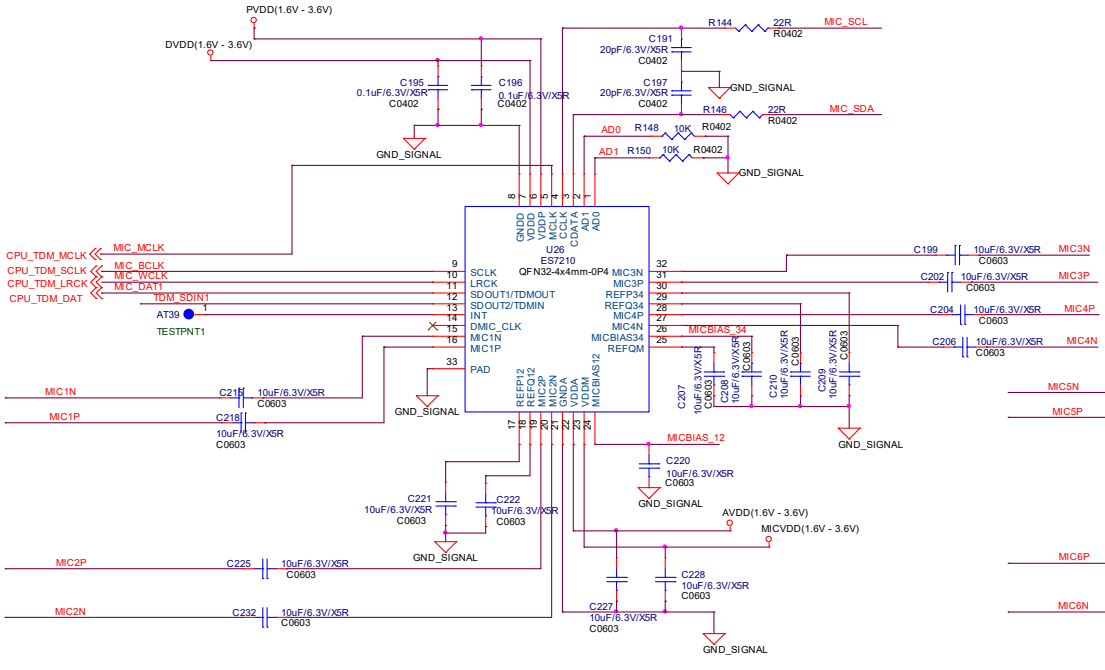


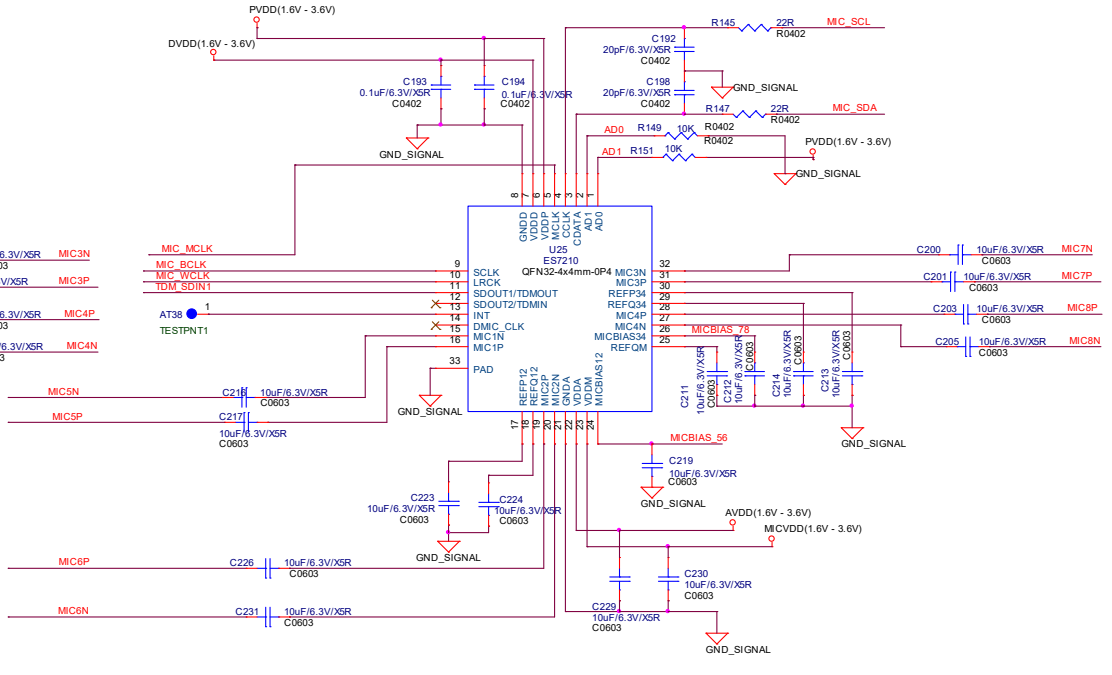
AD [1:0]	ES7210 CHIP ADDRESS
AD1 = 0, AD0 = 0	0x80 (8bit) / 0x40(7bit)
AD1 = 0, AD0 = 1	0x82 (8bit) / 0x41(7bit)
AD1 = 1, AD0 = 0	0x84 (8bit) / 0x42(7bit)
AD1 = 1, AD0 = 1	0x86(8bit) / 0x43(7bit)

4.14.4 TDM Mode With Two ES7210 Devices

If there are eight microphones in application system, two ES7210 devices will be used for voice capture. If TDM is enabled, the TDMIN pin of the last device in TDM link should be float or pulled down to ground.

The below circuit schematic illustrates TDM mode of two ES7210 cascaded.

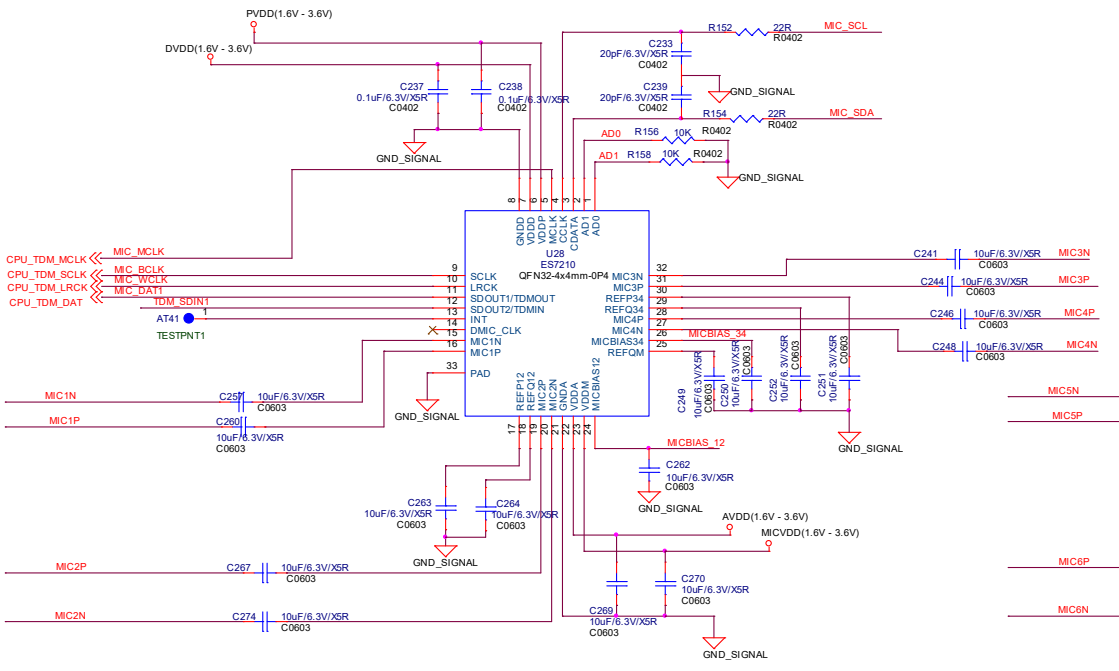


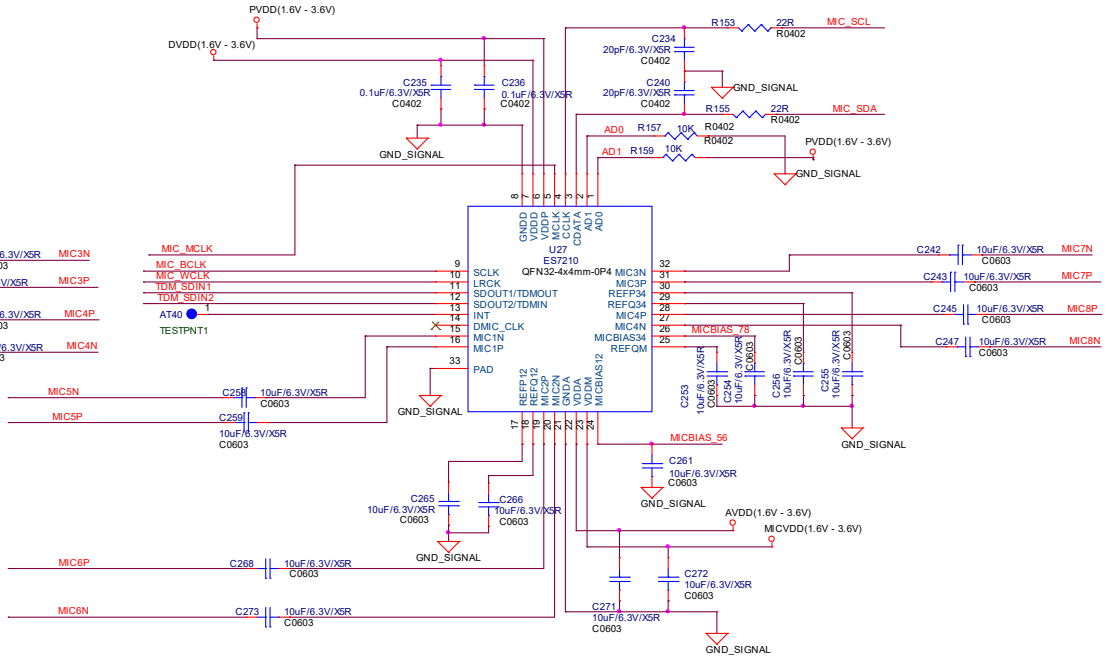


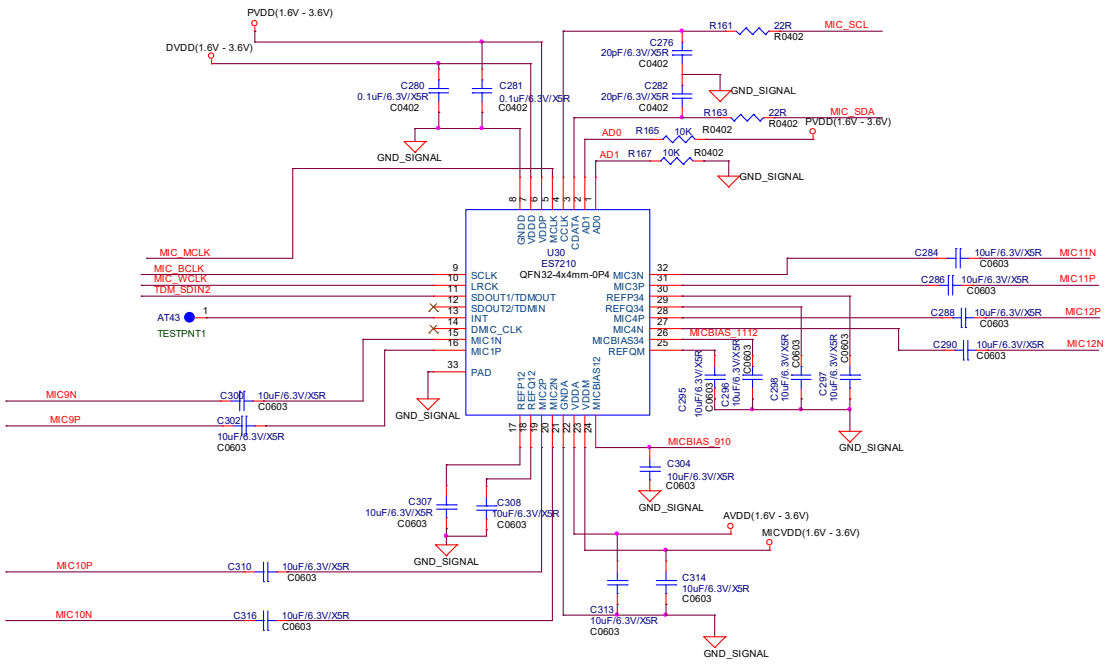
4.14.5 TDM Mode With Three ES7210 Devices

If there are 12 microphones in application system, three ES7210 devices will be used for voice capture. If TDM is enabled, the TDMIN pin of the last device in TDM link should be float or pulled down to ground.

The below circuit schematic illustrates TDM mode of three ES7210 cascaded.

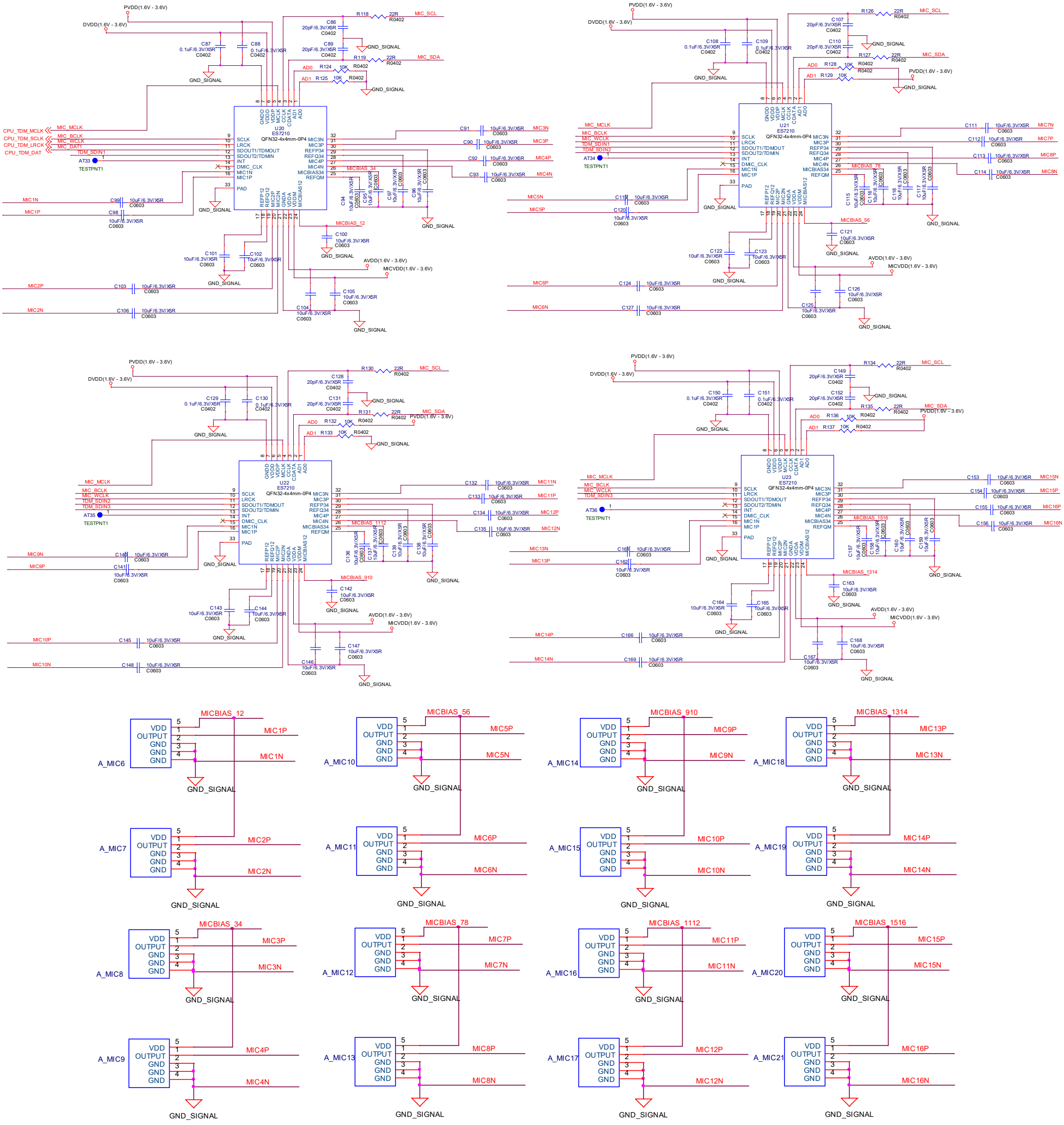






4.14.6 TDM Mode With Four ES7210 Devices

Below schematic shows four ES7210 devices cascaded in TDM mode. The TDMIN pin of the last device in TDM link will be float or pulled down to ground.



5 Register Configuration for ES7210

The Register configuration includes ADC start up, ADC Standby and ADC Cascading mode, etc.

5.1 The Sequence – TDMIN-IIS 30DB

WriteReg(0x09, 0x30);
WriteReg(0x0A, 0x30);
WriteReg(0x23, 0x26);
WriteReg(0x22, 0x06);
WriteReg(0x21, 0x26);
WriteReg(0x20, 0x06);
WriteReg(0x11, 0x60);
WriteReg(0x12, 0x02);
WriteReg(0x40, 0xC3);
WriteReg(0x41, 0x70);
WriteReg(0x42, 0x70);
WriteReg(0x43, 0x1A);
WriteReg(0x44, 0x1A);
WriteReg(0x45, 0x1A);
WriteReg(0x46, 0x1A);
WriteReg(0x47, 0x08);
WriteReg(0x48, 0x08);
WriteReg(0x49, 0x08);
WriteReg(0x4A, 0x08);
WriteReg(0x07, 0x20);
WriteReg(0x02, 0xC1);
WriteReg(0x06, 0x04);
WriteReg(0x4B, 0x0F);
WriteReg(0x4C, 0x0F);
WriteReg(0x00, 0x71);
WriteReg(0x00, 0x41);

5.2 The Sequence –Master

WriteReg(0x01, 0x40);
WriteReg(0x08, 0x11);
WriteReg(0x03, 0x04);
WriteReg(0x04, 0x01);
WriteReg(0x05, 0x00);
WriteReg(0x00, 0x01);

5.3 The Sequence – N*TDMIN-IIS 30DB

WriteReg(0x00, 0xFF);
WriteReg(0x00, 0x32);
WriteReg(0x09, 0x30);
WriteReg(0x0A, 0x30);
WriteReg(0x23, 0x26);
WriteReg(0x22, 0x06);
WriteReg(0x21, 0x26);
WriteReg(0x20, 0x06);
WriteReg(0x08, 0x40);
WriteReg(0x11, 0x60);
WriteReg(0x12, 0x03);
WriteReg(0x40, 0xC3);
WriteReg(0x41, 0x70);
WriteReg(0x42, 0x70);
WriteReg(0x43, 0x1A);

WriteReg(0x44, 0x1A);
WriteReg(0x45, 0x1A);
WriteReg(0x46, 0x1A);
WriteReg(0x47, 0x08);
WriteReg(0x48, 0x08);
WriteReg(0x49, 0x08);
WriteReg(0x4A, 0x08);
WriteReg(0x07, 0x20);
WriteReg(0x02, 0xC4);
WriteReg(0x06, 0x04);
WriteReg(0x4B, 0x0F);
WriteReg(0x4C, 0x0F);
WriteReg(0x00, 0x71);
WriteReg(0x00, 0x41);

5.4 The Sequence – Auotmute+int

WriteReg(0x0C, 0x03);
WriteReg(0x13, 0x0C);
WriteReg(0x14, 0x5C);
WriteReg(0x15, 0x5C);

5.5 The sequence for Standby mode

WriteReg(0x4B, 0xFF);
WriteReg(0x4C, 0xFF);
WriteReg(0x0B, 0xD0);
WriteReg(0x40, 0x80);
WriteReg(0x01, 0x7F);
WriteReg(0x06, 0x07);