A+B

BET- C202 (CSE/ME)
SEMESTER EXAMINATION- MAY 2024
CLASS: B.TECH SEMESTER: II
ELECTRONIC DEVICES

Time: 3 hours **Max. Marks: 70**

Note: Question Paper is divided into two sections: **A and B**. Attempt both the sections as per given instructions.

SECTION-A (SHORT ANSWER TYPE QUESTIONS)

Instructions: Answer any ***five*** questions in about 150 words each. Each question carries six marks. **(5 X 6 = 30 Marks)**

		CO	BL
Q-1	Analyze band structure of an open-circuited pn-junction.	3	4
Q-2	Explain hall effect principle with its applications.	2	2
Q-3	Define avalanche and ZENER breakdown mechanism in diode.	1	1
Q-4	Define Ebers–moll model of BJT.	1	1
Q-5	Explain the concept of ac and dc load line in BJT characteristics.	2	2
Q-6	Analyze graphically, the static and dynamic resistance of diode and approximate equivalent model of practical and ideal diode.	3	4
Q-7	Define the working of pn junction as clippers and clampers circuit.	1	1
Q-8	Define the pinch-off voltage of a JFET.	1	1
Q-9	Explain the working of transistor as amplifiers, which configuration is mostly preferred?	2	2
Q-10	Define the merits and demerits of FET over BJT.	1	1

SECTION-B (LONG ANSWER TYPE QUESTIONS)

Instructions: Answer any ***four*** questions in detail. Each question carries 10 marks.

(4 X 10 = Marks)

		CO	BL
Q-1	Design a voltage regulator that will maintain an output voltage of 20V across a 1-kΩ load with an input that will vary between 30 and 50V. That is, determine the proper value of R_S and the maximum current I_{ZM}.	5	6
Q-2	Compare different configurations of BJT.	4	4

Q-3	Analyze the ac model of BJT as an amplifier in COMMON-EMITTER configuration using h-parameters, that is, small signal model.	3	4
Q-4	Explain the circuit diagram for collector-to-base, emitter-feedback bias and self-bias with their respective thermal stability equations.	2	2
Q-5	Explain FET biasing, that is, Fixed-bias configuration, Self-bias configuration, Voltage-Divider biasing with their graphically solutions.	2	2
Q-6	Define the term Fermi-energy in semiconductors, and position of Fermi-level at different temperature and at different doping level in n-type semiconductor.	1	1
Q-7	Analyze the circuits for half and full wave rectifiers using PN-junction diode.	3	4
Q-8	Define the internal structure of JFET with its input and transfer characteristics.	1	1

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