ESC201T : Introduction to Electronics

HW11: Solution

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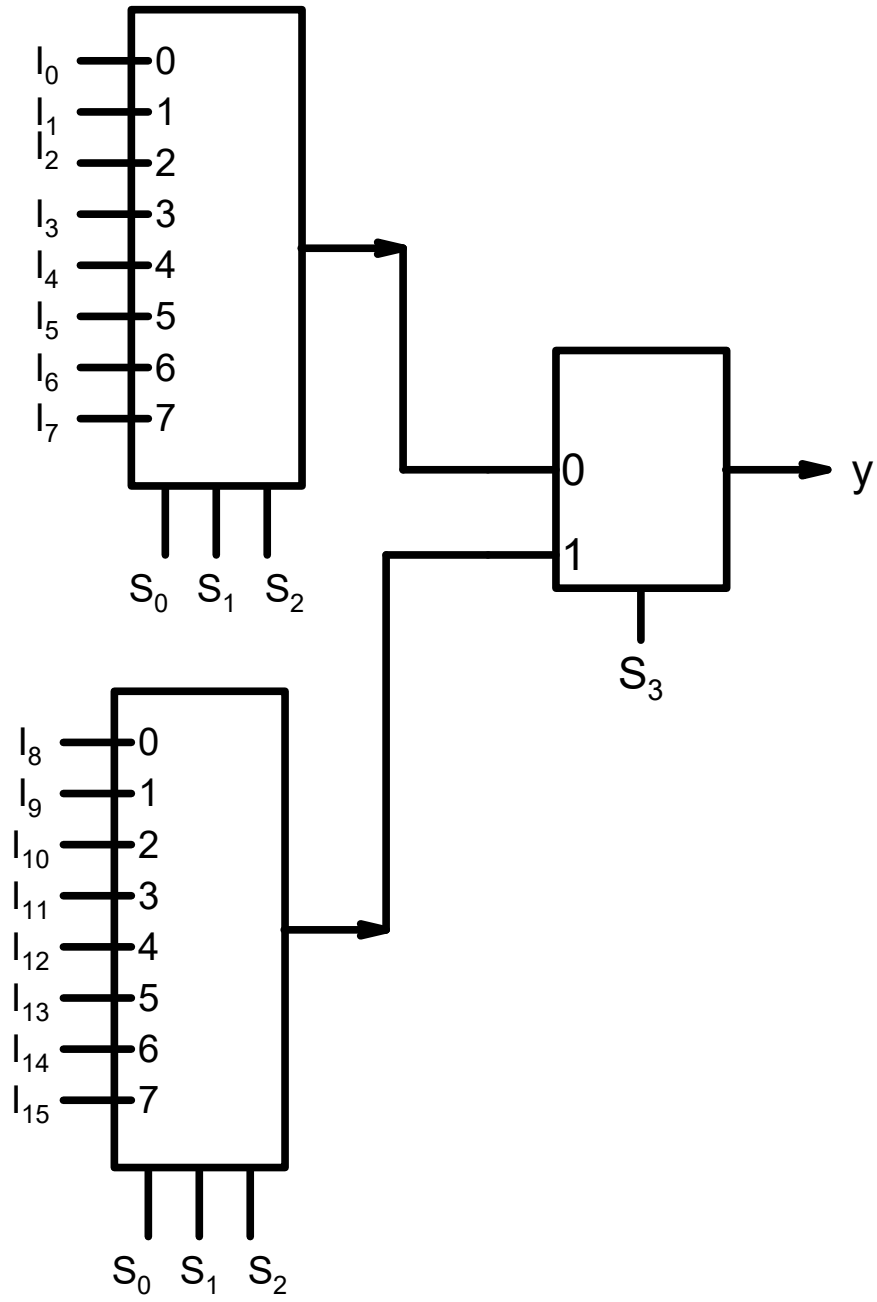
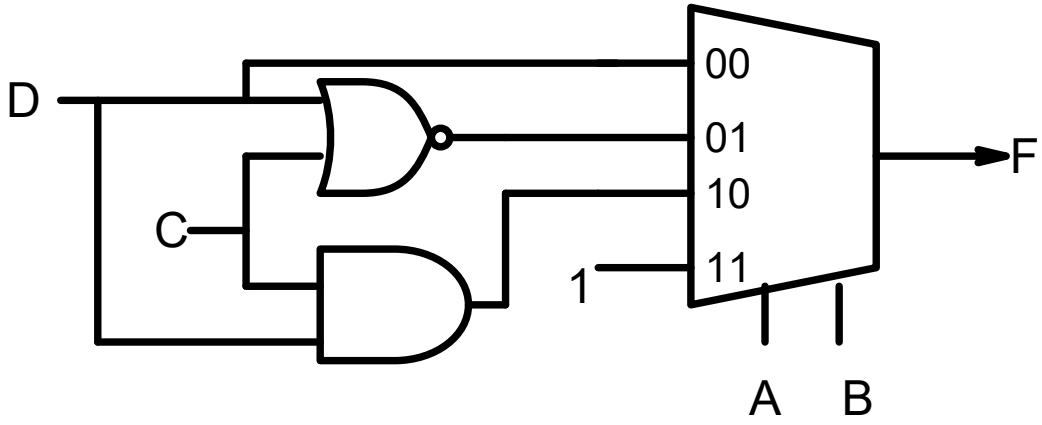
Q.1 Construct a 16 x 1 multiplexer with two 8 to 1 and one 2 to 1 multiplexers. Use block diagrams



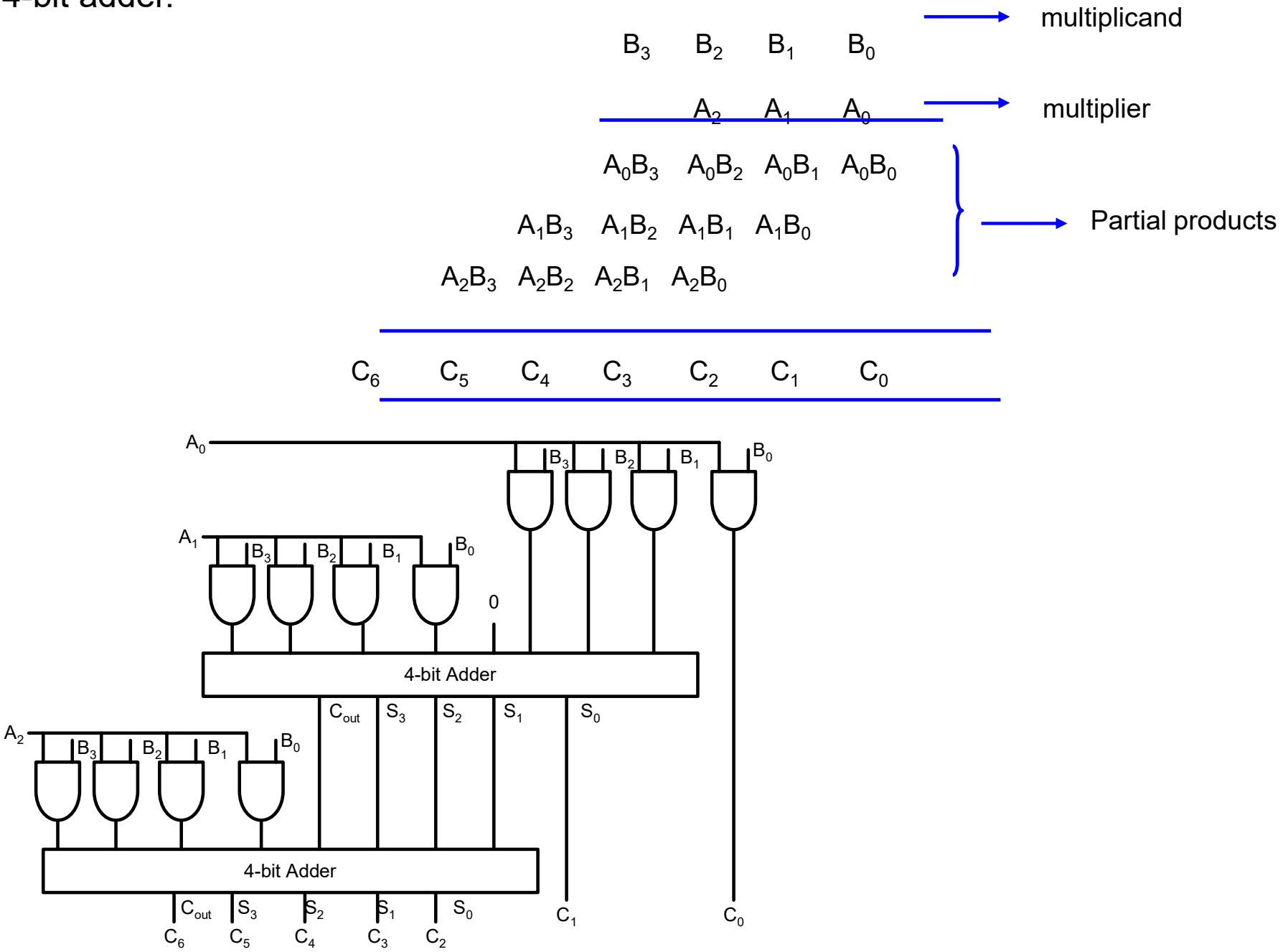
Q.2 Implement the following Boolean function using one 4 to 1 multiplexer and external gates. (Hint: Connect inputs A and B to the control or selection lines of the mux and then use basic gates to apply appropriate combinations of C & D to the input lines of the Mux.) .

$$F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$$

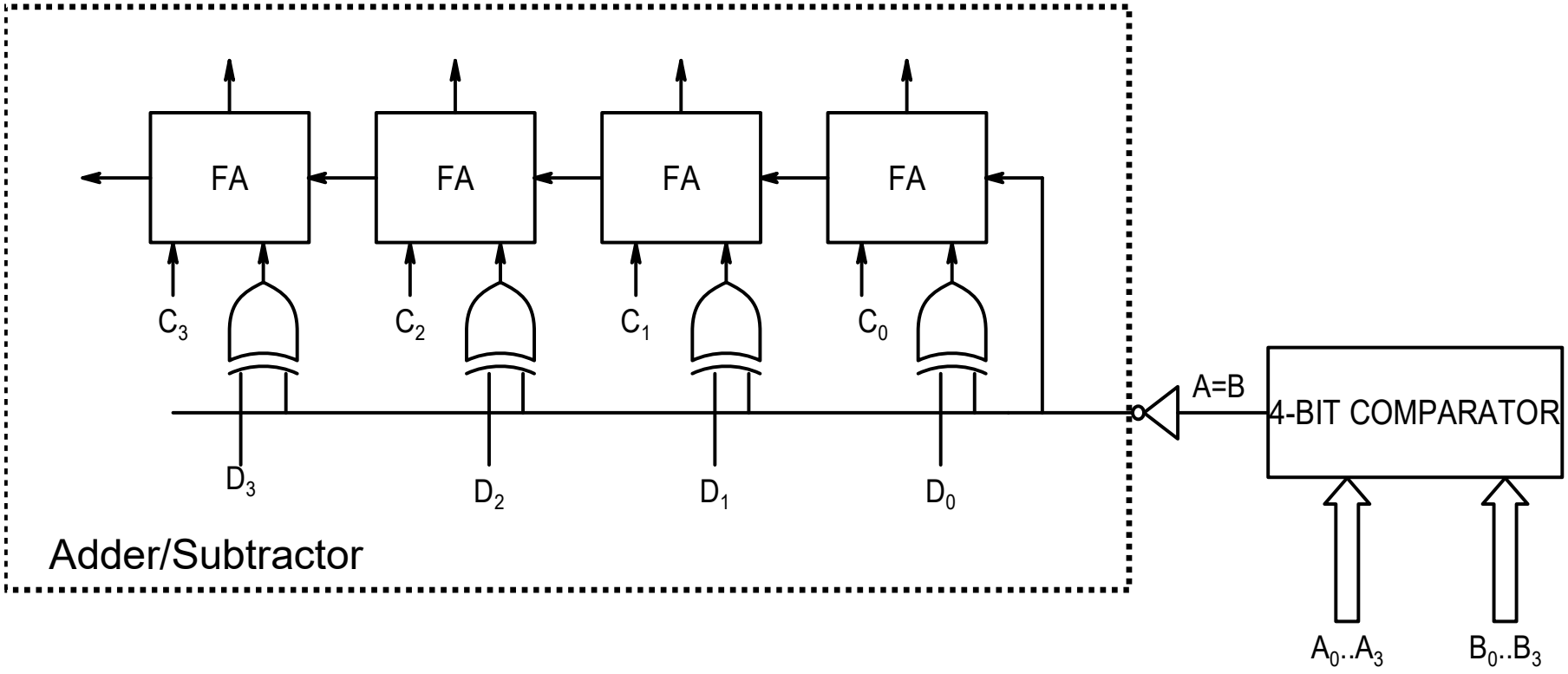
AB	CD	F	
00	00	0	
00	01	1	F=D
00	10	0	
00	11	1	
01	00	1	
01	01	0	$F=\overline{C}\,\overline{D}$
01	10	0	
01	11	0	
10	00	0	
10	01	0	F=C D
10	10	0	
10	11	1	
11	00	1	
11	01	1	F=1
11	10	1	
11	11	1	



Q.3 Show how one can multiply a 4-bit number A with a 3-bit number B using basic gates and 4-bit adder.



Q.4 Design a circuit that would implement the following function:
IF (A = B) then Y = C + D ELSE Y = C-D. A ,B,C, D are four bit numbers



Q.5 A PN flip-flop has four operations, reset to 0, hold, complement and set to 1 when inputs PN are 00,01,10,11 respectively. Tabulate the characteristic table, excitation table and show how the PN FF can be converted to a D FF.

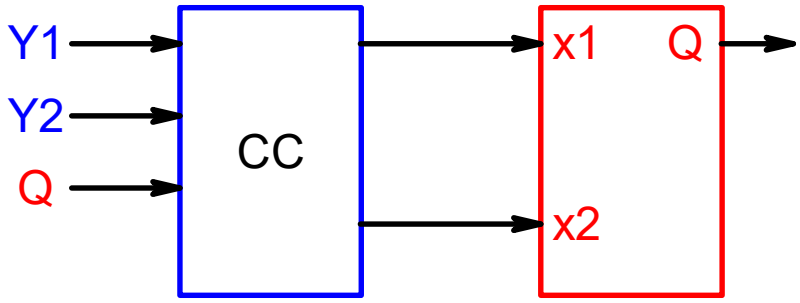
P N	Q(t+1)	State
0 0	0	Reset
0 1	Q(t)	Hold
1 0	$\overline{Q}$(t)	Toggle
1 1	1	Set

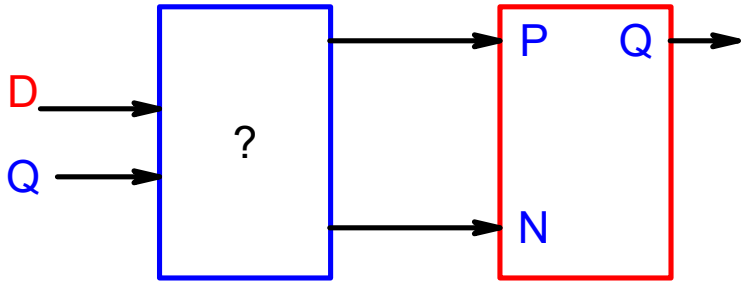
characteristic table

Q(t)	Q(t+1)	P N
0	0	0 X
0	1	1 X
1	0	X 0
1	1	X 1

excitation table

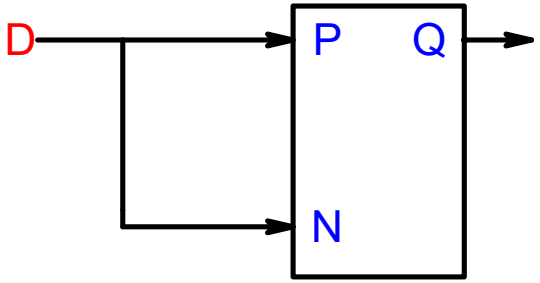
General circuit for converting a FF with inputs X1, X2 into a different FF with inputs Y1, Y2.



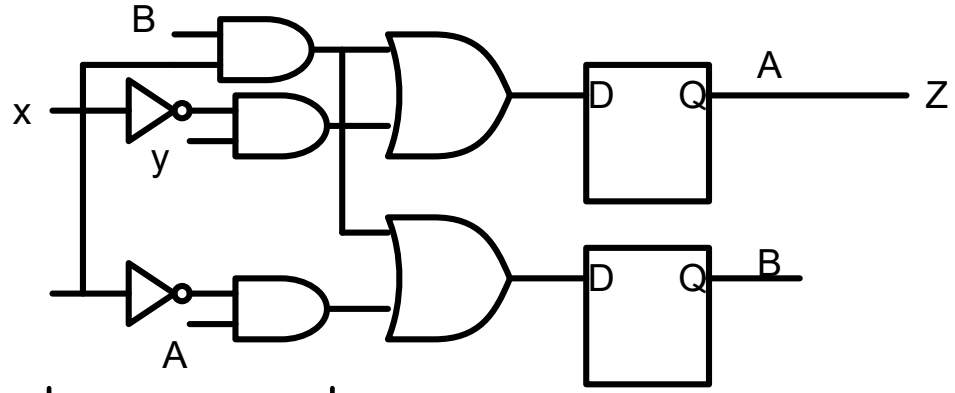


D	Q	Q(t+1)	P	N
0	0	0	0	X
0	1	0	X	0
1	0	1	1	X
1	1	1	X	1

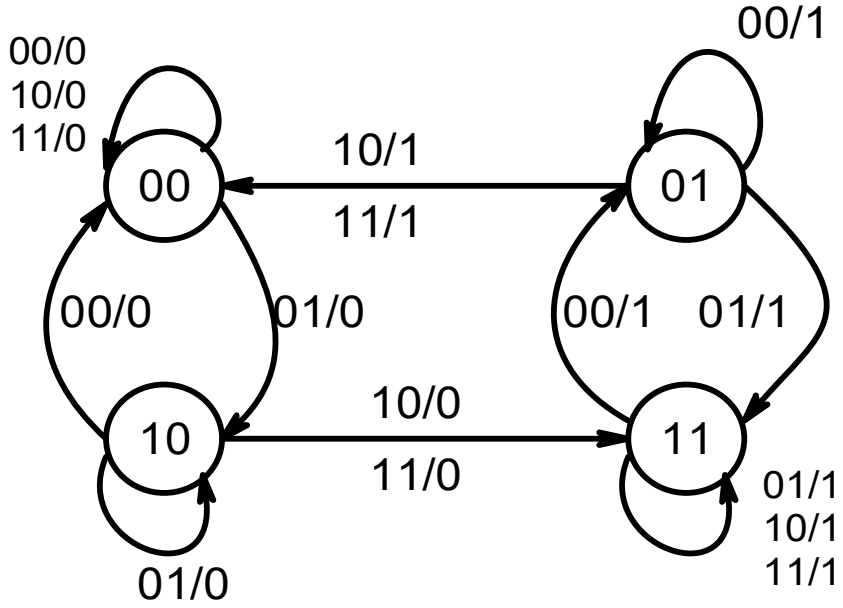
$\rightarrow$ P = N = D



Q.6 A sequential circuit with two flip-flops A and B, two inputs x, y and a output z has the following behavior: $A(t+1) = \bar{x}.y + x.B$; $B(t+1) = \bar{x}.A + x.B$; $z = A$. Draw the logic diagram of the circuit, list the state table and draw the state transition graph.

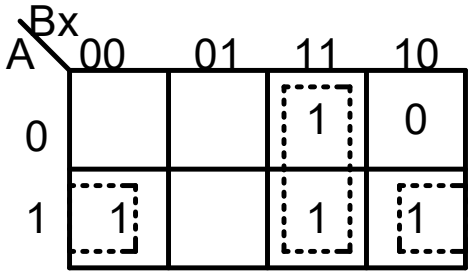


Present State		Input		Next State		
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	0
0	1	0	1	1	1	0
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1
1	0	0	1	1	0	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

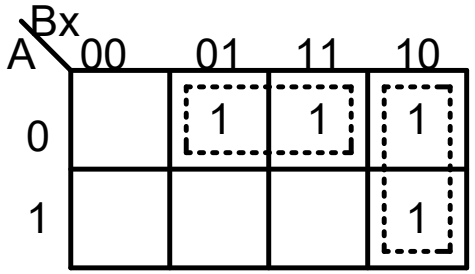


Q.7 Design a sequential circuit with two D flip-flops A and B and one input x such that when x = 0, the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10 and back to 00, and repeats.

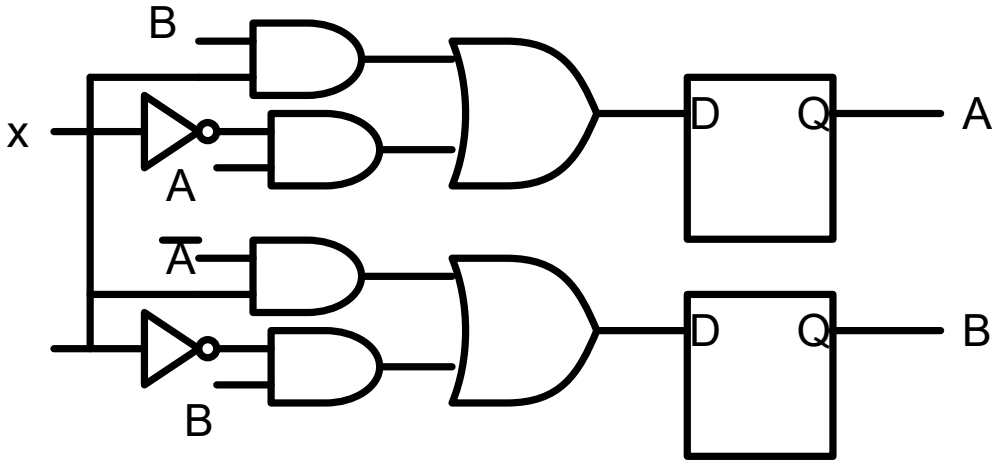
Present State		Input	Next State			
A	B	x	A	B	D_A	D_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	1	1	1
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	1	0	1	0



$$D_A = A.\overline{x} + B.x$$

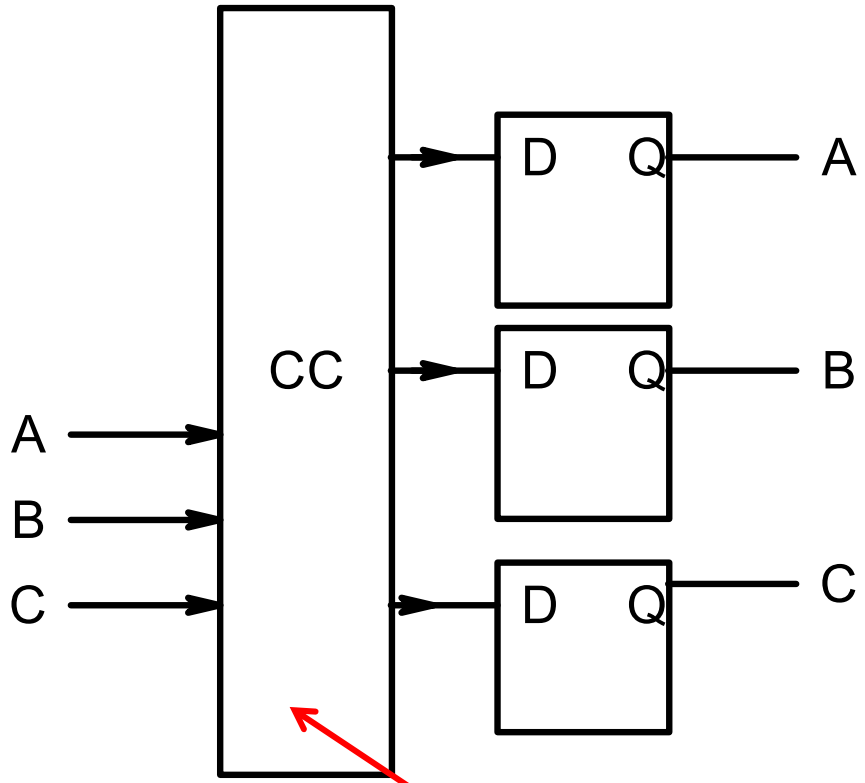


$$D_B = \overline{A}.x + B.\overline{x}$$



Q.8 Design a synchronous counter that goes through the following repeating sequence 0, 2, 1, 4, 3,6,5,7.

1. There are 8 states, so 3 FFs are required.
2. Let the FFs be D type

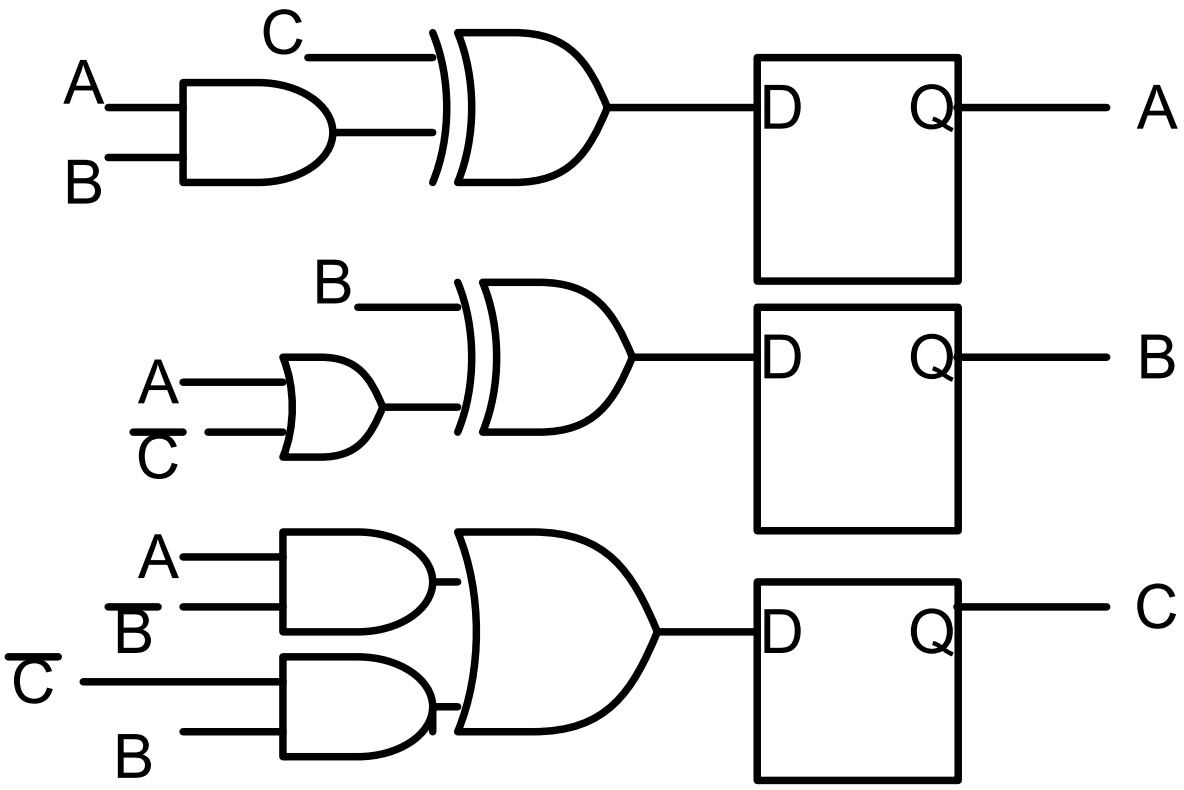


3. Build the state Transition table and determine the required values for FF inputs

PS	NS			
A B C	A B C	D_A	D_B	D_C
0 0 0	0 1 0	0	1	0
0 1 0	0 0 1	0	0	1
0 0 1	1 0 0	1	0	0
1 0 0	0 1 1	0	1	1
0 1 1	1 1 0	1	1	0
1 1 0	1 0 1	1	0	1
1 0 1	1 1 1	1	1	1
1 1 1	0 0 0	0	0	0

4. Find expressions for D_A D_B and D_C and Synthesize the combinational circuit

$$D_A = C.\overline{(A.B)} + \overline{C}.(AB) \quad ; \quad D_B = B.\overline{(A + \overline{C})} + \overline{B}.(A + \overline{C}) \; ; \; D_C = A.\overline{B} + B.\overline{C}$$



Q.9 Design a synchronous counter using T flip-flops that goes through the following repeating sequence 0, 1,3,7,6,4. Take the unused states as don't care states. Check if the circuit corrects itself if by chance it happens to go to one of the unused states. If not, correct the problem

PS A B C	NS A B C	T_A T_B T_C
0 0 0	0 0 1	0 0 1
0 0 1	0 1 1	0 1 0
0 1 1	1 1 1	1 0 0
1 1 1	1 1 0	0 0 1
1 1 0	1 0 0	0 1 0
1 0 0	0 0 0	1 0 0

T_A

A \ BC	00	01	11	10
0	0	0	1	x
1	1	x	0	0

$$T_A = \overline{A}.B + A\overline{B}$$

T_B

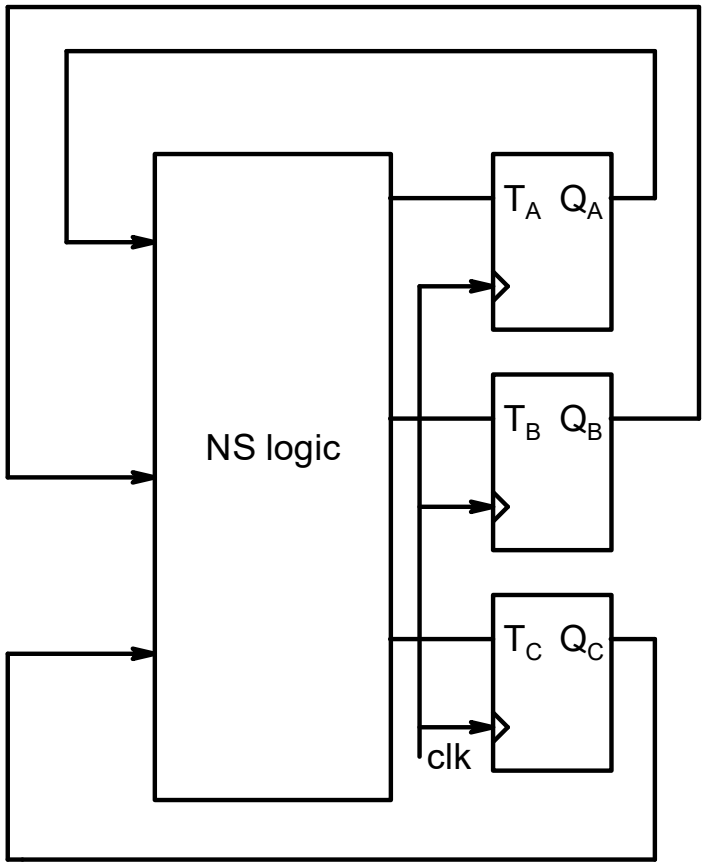
A \ BC	00	01	11	10
0	0	1	0	x
1	0	x	0	1

$$T_B = \overline{B}.C + B\overline{C}$$

T_C

A \ BC	00	01	11	10
0	1	0	0	x
1	0	x	1	0

$$T_C = \overline{A}.\overline{C} + AC$$



Unused states are ABC = 010 and 101

For 010, TA = 1, TB = 1, TC = 1 so the next state is 101 which is an unused state as well

For ABC = 101 state: TA = TB=TC = 1 so the next state will be 010 which is unused state. Thus we see that if the counter goes into one of the unused states, it will not be able to recover to a proper used state.

$$T_A = \overline{A}.B + A\overline{B} \qquad T_B = \overline{B}.C + B\overline{C}$$

$$T_C = \overline{A}.\overline{C} + AC$$

A way to avoid this problem is to modify the transition table so that if the counter goes to a unused state, it then transitions to a used state say 000.

PS A B C	NS A B C	T_A T_B T_C
0 0 0	0 0 1	0 0 1
0 0 1	0 1 1	0 1 0
0 1 1	1 1 1	1 0 0
1 1 1	1 1 0	0 0 1
1 1 0	1 0 0	0 1 0
1 0 0	0 0 0	1 0 0
0 1 0	0 0 0	0 1 0
1 0 1	0 0 0	1 0 1

T_A

A \ BC	00	01	11	10
0	0	0	1	0
1	1	1	0	0

$$T_A = \overline{A}.B.C + A\overline{B}$$

T_B

A \ BC	00	01	11	10
0	0	1	0	1
1	0	0	0	1

$$T_B = \overline{A}\overline{B}.C + B\overline{C}$$

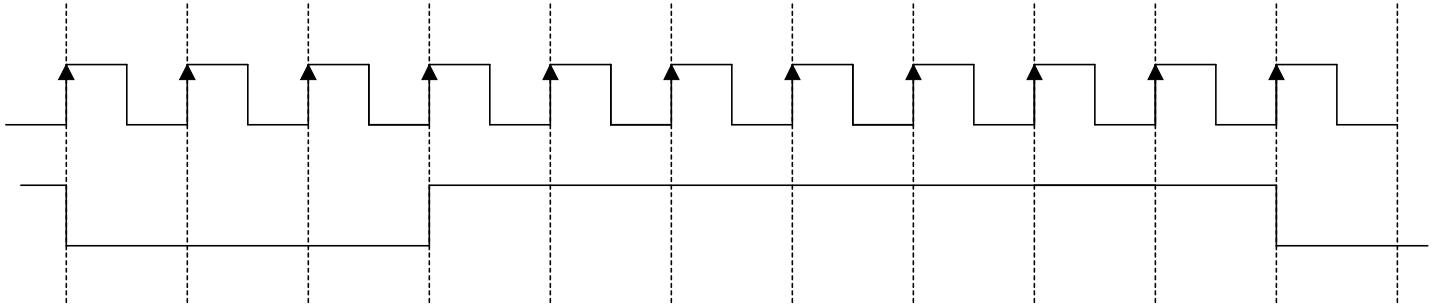
T_C

A \ BC	00	01	11	10
0	1	0	0	0
1	0	1	1	0

$$T_C = \overline{A}.\overline{BC} + AC$$

Note that the Boolean expressions and thus the combinational logic has become more complex.

Q.10 From a frequency of 10KHz, generate a signal of frequency 1KHz having the following waveform



We need a divide by 10 counter so 4 FFs are required. A possible state transition of the counter:

Note that FF A output will have the required waveform.

A B C D
0 0 0 0
0 0 0 1
0 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1
1 0 0 0
1 0 0 1

PS A B C D	NS A B C D	T_A T_B T_C T_D
0 0 0 0	0 0 0 1	0 0 0 1
0 0 0 1	0 0 1 0	0 0 1 1
0 0 1 0	1 0 1 1	1 0 0 1
1 0 1 1	1 1 0 0	0 1 1 1
1 1 0 0	1 1 0 1	0 0 0 1
1 1 0 1	1 1 1 0	0 0 1 1
1 1 1 0	1 1 1 1	0 0 0 1
1 1 1 1	1 0 0 0	0 1 1 1
1 0 0 0	1 0 0 1	0 0 0 1
1 0 0 1	0 0 0 0	1 0 0 1

$$T_D = 1$$

PS				NS							
A	B	C	D	A	B	C	D	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	1	0	1	1	1	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

T_C

AB \ CD	00	01	11	10
00	0	1	x	0
01	x	x	x	x
11	0	1	1	0
10	0	0	1	x

$$T_C = CD + BD + \overline{A}.D$$

T_B

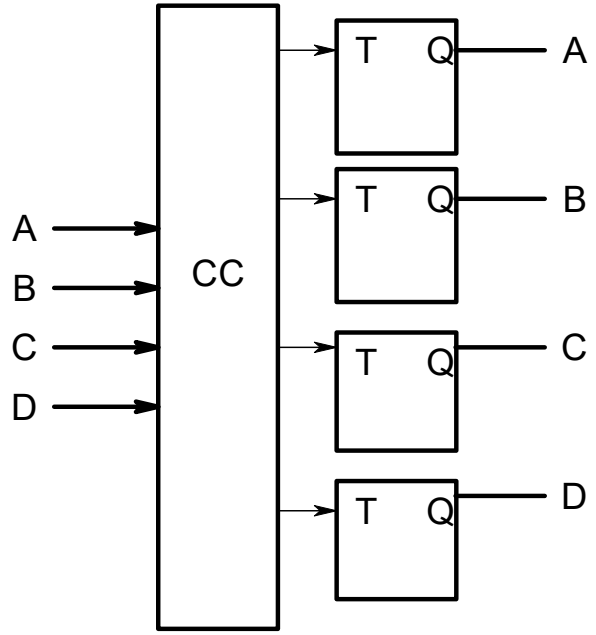
AB \ CD	00	01	11	10
00	0	0	x	0
01	x	x	x	x
11	0	0	1	0
10	0	0	1	x

$$T_B = CD$$

T_A

AB \ CD	00	01	11	10
00	0	0	x	1
01	x	x	x	x
11	0	0	0	0
10	0	1	0	x

$$T_A = \overline{A}.C + A\overline{B}\overline{C}D$$



Using the derived expressions the combinational circuit can be synthesized.

Q.11 Suppose a 4-bit ripple counter is available with a asynchronous reset input. Show how you can construct a counter which has the count sequence 0-1-2-3-4-5-6-7-8-9-10-11-12-0….