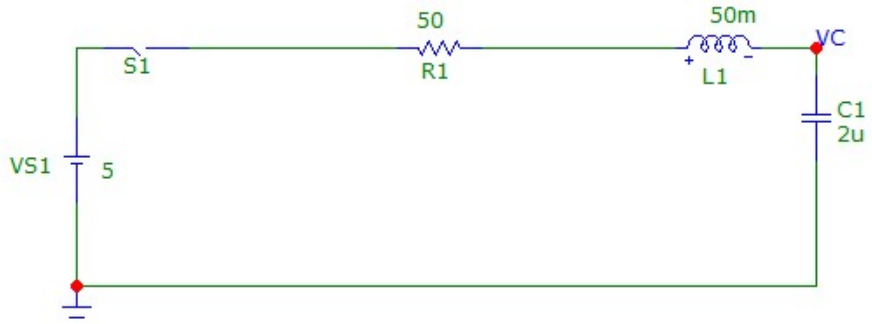
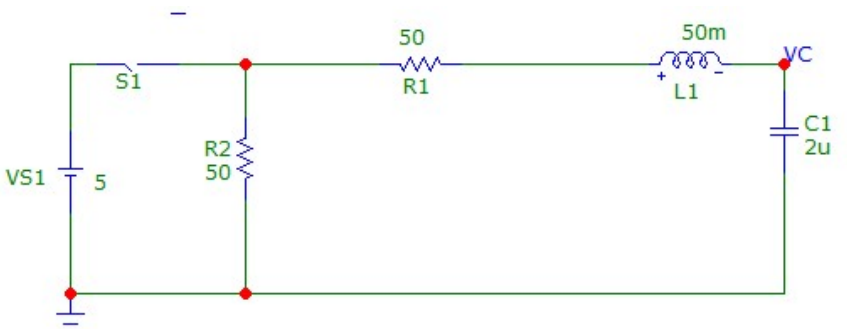
ESC201T: Introduction to Electronics

HW - 4 **Date: 24.9.2020**

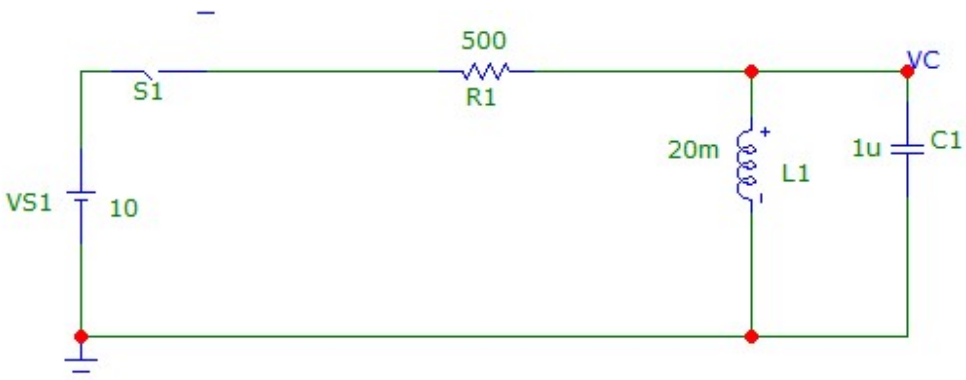
Q.1 In the circuit shown below, determine the frequency of oscillation that will be observed in the capacitor voltage after switch S1 is closed. Determine the time at which the output voltage Vo will settle to within 5% of its final value.



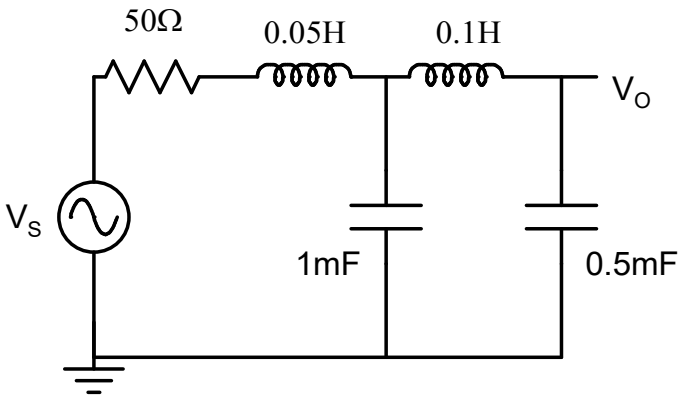
Q.2 After the circuit shown above has reached steady state, the switch S1 is opened and an additional resistor is included to provide a current path as shown below. Sketch the qualitative variation of current and capacitor voltage. What is the maximum value of R2 for which oscillations in current would be observed?



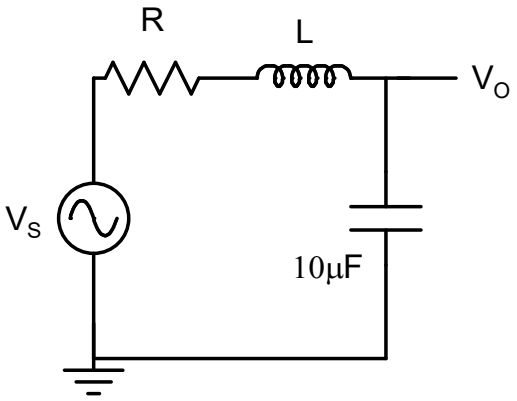
Q.3 Sketch and explain the qualitative variation of current and capacitor voltage in the parallel LCR circuit shown below after switch S1 is closed



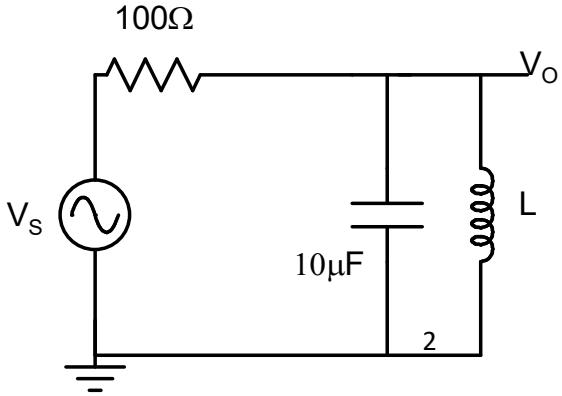
Q.4 Determine the output voltage as a function of time using the method of phasors for an input voltage of $V_S = 5Cos(100t)$.



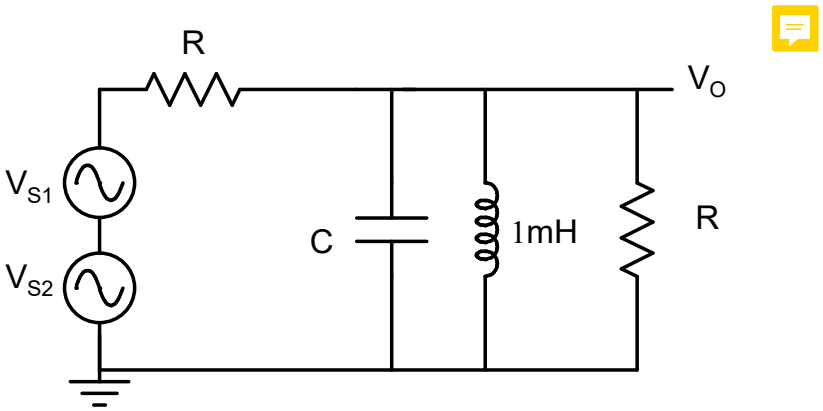
Q.5 A student applied $V_S = 10VCos(100t)$ as input to the circuit shown below and claimed that he measured V_O = **100VSin(100t)** across the capacitor. Is that possible? If so determine suitable values for inductor and resistor for such a condition to occur? Comment about the concept of voltage division in this case.



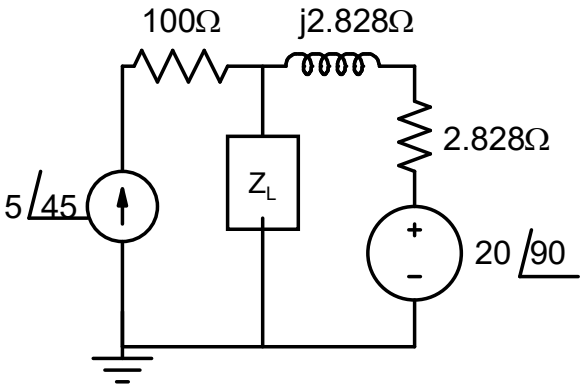
Q.6 Determine suitable value for inductance such that output voltage V_O is maximum. For this value of inductance determine current in all the components (R,L and C). Assume that $V_S = 10VCos(100t)$.



Q.7 In the circuit shown below assume that the two input sinusoidal voltage sources represent two different radio channels. Determine suitable value of capacitor such that we can listen to channel-1 (represented by source V_{S1}) of frequency f_1 = 1000KHz. Determine also suitable value of R such that interference due to the second channel of frequency f_2 = 1100KHz is negligible (say power at the output due to V_{s2} is a factor of 1000 less than that due to V_{s1}) . V_o represents the output voltage. Use suitable approximations to simplify analysis.



Q.8 Use Thevenin's theorem to determine Z_L such that maximum power is dissipated in the load impedance Z_L. Determine also the power dissipated in Z_L and power supplied by each source.



Q.9 For the circuit shown below, determine the power factor for the power supplied by the input. Determine a suitable value of capacitor which when connected in parallel to the source can raise the power factor to unity.