```
#
# 1 481C7631
#
# -----TAG BITS DONT MATCH - MISS-----
#
# 1 481C7631
#
# ------TAG BITS MATCH, HENCE HIT-------
#
# 0 582C7632
#
# -----TAG BITS DONT MATCH - MISS-----
#
# 0 594C7615
#
# -----TAG BITS DONT MATCH - MISS-----
#
# 0 621C7600
#
# -----TAG BITS DONT MATCH - MISS-----
#
# 1 111C762C
#
# -----TAG BITS DONT MATCH - MISS-----
#
# 9 0000
#
# -------------------------------Contents of INSTRUCTION CACHE-------------------------------
# TRACE Address = 0
# SET NUMBER          = 0
# TAG3 = 0       TAG2 = 0        TAG1 = 0        TAG0 = 0
# STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU3 = 0       LRU2 = 0        LRU1 = 0        LRU0 = 0
# VALID3 = 0     VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# ---INSTRUCTION CACHE statistics---
# Total Number of instruction reads  = 0
# Total Number of instruction writes = 0
# Total Number of instruction hits   = 0
# Total Number of instruction misses = 0
# Denominator cannot be zero (ie, data_miss and data_hit is zero)
# ------------------------------------------------------------------------------Contents of DATA CACHE-----------------------------------------------------------------------------------------
# TRACE ADDRESS = 0
# SET NUMBER   = 0
# TAG7 = 0       TAG6 = 0        TAG5 = 0        TAG4 = 0        TAG3 = 0        TAG2 = 0        TAG1 = 0        TAG0 = 0
# STATE7 = INVALID  STATE6 = INVALID  STATE5 = INVALID  STATE4 = INVALID  STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU7 = 0       LRU6 = 0        LRU5 = 0        LRU4 = 0        LRU3 = 0        LRU2 = 0        LRU1 = 0        LRU0 = 0
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# VALID7 = 0     VALID6 = 0      VALID5 = 0      VALID4 = 0      VALID3 = 0      VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# -----DATA CACHE statistics-----
# Total Number of data reads  = 3
# Total Number of data writes = 3
# Total Number of data hits   = 1
# Total Number of data misses = 5
# DATA CACHE HIT ratio = 16.666667
#
#
#
# Trace filename formatting is incorrect
# -------------------------------Contents of INSTRUCTION CACHE-------------------------------
# TRACE Address = 0
# SET NUMBER          = 0
# TAG3 = 0       TAG2 = 0        TAG1 = 0        TAG0 = 0
# STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU3 = 0       LRU2 = 0        LRU1 = 0        LRU0 = 0
# VALID3 = 0     VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# ---INSTRUCTION CACHE statistics---
# Total Number of instruction reads  = 0
# Total Number of instruction writes = 0
# Total Number of instruction hits   = 0
# Total Number of instruction misses = 0
# Denominator cannot be zero (ie, data_miss and data_hit is zero)
# ------------------------------------------------------------------------------Contents of DATA CACHE-----------------------------------------------------------------------------------------
# TRACE ADDRESS = 0
# SET NUMBER   = 0
# TAG7 = 0       TAG6 = 0        TAG5 = 0        TAG4 = 0        TAG3 = 0        TAG2 = 0        TAG1 = 0        TAG0 = 0
# STATE7 = INVALID  STATE6 = INVALID  STATE5 = INVALID  STATE4 = INVALID  STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU7 = 0       LRU6 = 0        LRU5 = 0        LRU4 = 0        LRU3 = 0        LRU2 = 0        LRU1 = 0        LRU0 = 0
# DIRTY7 = 0     DIRTY6 = 0      DIRTY5 = 0      DIRTY4 = 0      DIRTY3 = 0      DIRTY2 = 0      DIRTY1 = 0      DIRTY0 = 0
# VALID7 = 0     VALID6 = 0      VALID5 = 0      VALID4 = 0      VALID3 = 0      VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# -----DATA CACHE statistics-----
# Total Number of data reads  = 3
# Total Number of data writes = 3
# Total Number of data hits   = 1
# Total Number of data misses = 5
# DATA CACHE HIT ratio = 16.666667
#
# ** Note: $stop    : testbench.sv(57)
#    Time: 125 ns  Iteration: 0  Instance: /SplitL1Cache_tesbench
# Break in Module SplitL1Cache_tesbench at testbench.sv line 57
```

```
#
# -----TAG BITS DONT MATCH - MISS-----
# ------Communication with L2------
# Data Cache : Read from L2 <582c7632>
#
#
# 0 594C7615
#
# -----TAG BITS DONT MATCH - MISS-----
# ------Communication with L2------
# Data Cache : Read from L2 <594c7615>
#
#
# 0 621C7600
#
# -----TAG BITS DONT MATCH - MISS-----
# ------Communication with L2------
# Data Cache : Read from L2 <621c7600>
#
#
# 1 111C762C
#
# -----TAG BITS DONT MATCH - MISS-----
# --------------Communication with L2--------------
# Data Cache : Read for Ownership(RFO) from L2 <111c762c>
# Data Cache : Write to L2 <111c762c>
#
#
# 9 0000
#
# ------------------------------Contents of INSTRUCTION CACHE------------------------------
# TRACE Address = 0
# SET NUMBER          = 0
# TAG3 = 0       TAG2 = 0        TAG1 = 0        TAG0 = 0
# STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU3 = 0       LRU2 = 0        LRU1 = 0        LRU0 = 0
# VALID3 = 0     VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# ---INSTRUCTION CACHE statistics---
# Total Number of instruction reads  = 0
# Total Number of instruction writes = 0
# Total Number of instruction hits   = 0
# Total Number of instruction misses = 0
# Denominator cannot be zero (ie, data_miss and data_hit is zero)
# ------------------------------------------------------------------------------Contents of DATA CACHE-------------------------------------------------------------------------------------
# TRACE ADDRESS = 0
# SET NUMBER   = 0
```

```
# STATE7 = INVALID  STATE6 = INVALID  STATE5 = INVALID  STATE4 = INVALID  STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU7 = 0        LRU6 = 0        LRU5 = 0        LRU4 = 0        LRU3 = 0        LRU2 = 0        LRU1 = 0        LRU0 = 0
# DIRTY7 = 0      DIRTY6 = 0      DIRTY5 = 0      DIRTY4 = 0      DIRTY3 = 0      DIRTY2 = 0      DIRTY1 = 0      DIRTY0 = 0
# VALID7 = 0      VALID6 = 0      VALID5 = 0      VALID4 = 0      VALID3 = 0      VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# -----DATA CACHE statistics-----
# Total Number of data reads  = 3
# Total Number of data writes = 3
# Total Number of data hits   = 1
# Total Number of data misses = 5
# DATA CACHE HIT ratio = 16.666667
#
#
#
# Trace filename formatting is incorrect
# ------------------------------Contents of INSTRUCTION CACHE------------------------------
# TRACE Address = 0
# SET NUMBER          = 0
# TAG3 = 0        TAG2 = 0        TAG1 = 0        TAG0 = 0
# STATE3 = INVALID  STATE2 = INVALID  STATE1 = INVALID  STATE0 = INVALID
# LRU3 = 0        LRU2 = 0        LRU1 = 0        LRU0 = 0
# VALID3 = 0      VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# ---INSTRUCTION CACHE statistics---
# Total Number of instruction reads  = 0
# Total Number of instruction writes = 0
# Total Number of instruction hits   = 0
# Total Number of instruction misses = 0
# Denominator cannot be zero (ie, data_miss and data_hit is zero)
# ------------------------------------------------------------------------------Contents of DATA CACHE-----------------------------------------------------------------------------------------
# TRACE ADDRESS = 0
# SET NUMBER   = 0
# TAG7 = 0        TAG6 = 0        TAG5 = 0        TAG4 = 0        TAG3 = 0        TAG2 = 0        TAG1 = 0        TAG0 = 0
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# LRU7 = 0        LRU6 = 0        LRU5 = 0        LRU4 = 0        LRU3 = 0        LRU2 = 0        LRU1 = 0        LRU0 = 0
# DIRTY7 = 0      DIRTY6 = 0      DIRTY5 = 0      DIRTY4 = 0      DIRTY3 = 0      DIRTY2 = 0      DIRTY1 = 0      DIRTY0 = 0
# VALID7 = 0      VALID6 = 0      VALID5 = 0      VALID4 = 0      VALID3 = 0      VALID2 = 0      VALID1 = 0      VALID0 = 0
#
# -----DATA CACHE statistics-----
# Total Number of data reads  = 3
# Total Number of data writes = 3
# Total Number of data hits   = 1
# Total Number of data misses = 5
# DATA CACHE HIT ratio = 16.666667
#
# ** Note: $stop    : testbench.sv(57)
#    Time: 125 ns  Iteration: 0  Instance: /SplitL1Cache tesbench
```