ECE 571

INTRO TO SYSTEM VERILOG

(Winter 2024)

A PROJECT REPORT

TEAM-13

submitted in partial fulfillment of the requirements
for the award of the degree of

Master of Science
in
ELECTRICAL AND COMPUTER ENGINEERING

Guide: Professor Mark Faust

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CONTENTS

Introduction:

The 8088 microprocessor, developed by Intel in the late 1970s, is a 16-bit microprocessor that gained significant popularity in early personal computers. It's part of the x86 family of processors, which continues to be a dominant architecture in computing today. The 8088 has an 8-bit external data bus, which means it can transfer data in 8-bit chunks, and a 20-bit address bus, allowing it to address up to 1 MB of memory. Its compatibility with existing 8-bit hardware and software made it a cost-effective choice for early PC manufacturers. The 8088 was notably used in IBM's first personal computer, the IBM PC, released in 1981, which played a pivotal role in shaping the modern PC industry.

The Intel 8088 microprocessor features a set of pins that serve various functions essential for its operation. Here's a brief overview of its pin configuration:

1. Data Bus (D0-D7): Eight pins dedicated to transferring data between the processor and external devices.
2. Address Bus (A0-A19): A 20-bit address bus used for addressing memory locations and I/O devices.
3. Control Bus (e.g., ALE, DT/R, DEN, etc.): Pins responsible for controlling various operations such as address and data bus multiplexing, bus status, and device enablement.
4. Power and Ground Pins: Pins for supplying power (VCC) and grounding (GND) the microprocessor.
5. Clock Pins (CLK): Pins for receiving the system clock signal to synchronize internal operations.
6. Interrupt and Status Pins (INTR, NMI, etc.): Pins related to interrupt handling and processor status.
7. Bus Control Pins (e.g., MN/MX, RD, WR, etc.): Pins for controlling bus operations like memory or I/O read/write cycles, and bus status.
8. Miscellaneous Pins (e.g., TEST, RESET, READY, etc.): Pins for testing, resetting, and indicating the readiness of the processor.

These pins collectively enable the 8088 to communicate with memory, input/output devices, and other components within a computer system, facilitating its operation as a central processing unit.

Significance:

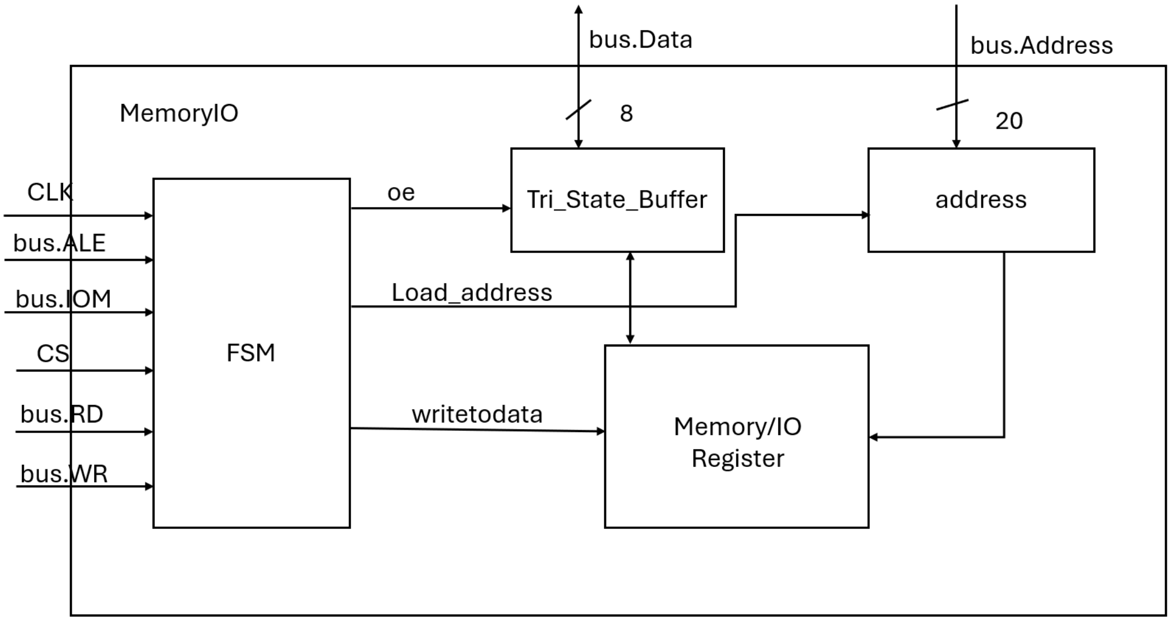
Understanding the functionality of pins and control signals of 8088 through simulating and observing the wave forms.

Objective:

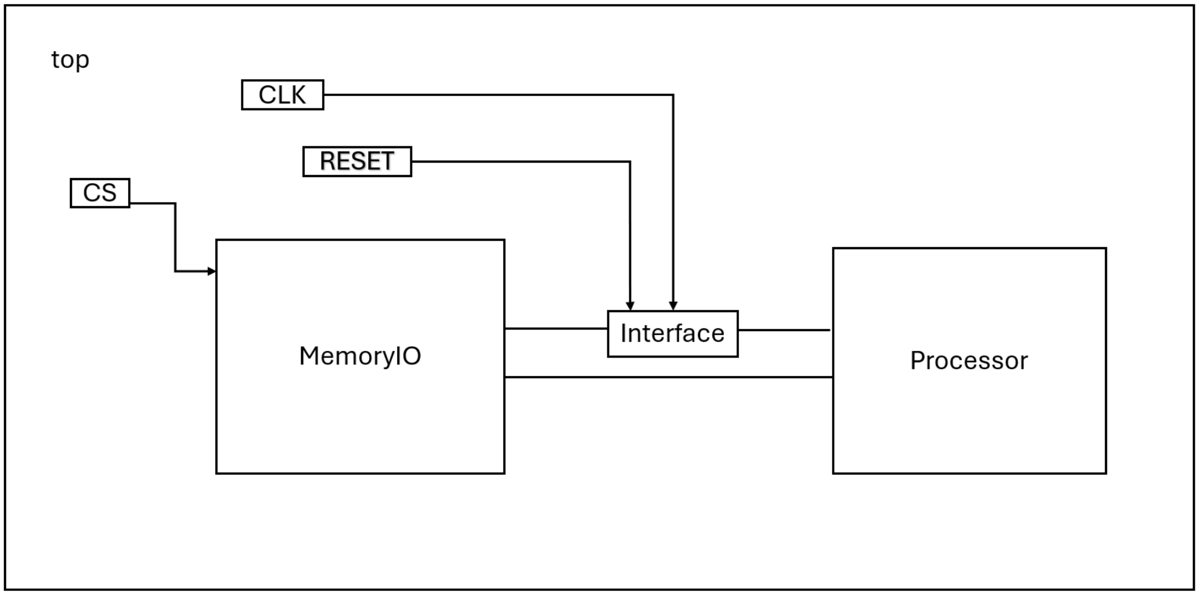
The main objective of this project is to design a controller which captures the signals from processor and do the following memory and I/O operations.

In this project, we designed a synthesizable FSM for 8088 bus-compatible memory or I/O modules, incorporating CS and OE inputs and implemented the FSM as a one-hot Moore machine. Modified the top-level module to instantiate two 512KiB memories and two I/O devices and adjusted the busops.txt file accordingly. Created an interface for 8088 pins with Processor and Peripheral mod ports and modified the top-level module to instantiate and use this interface

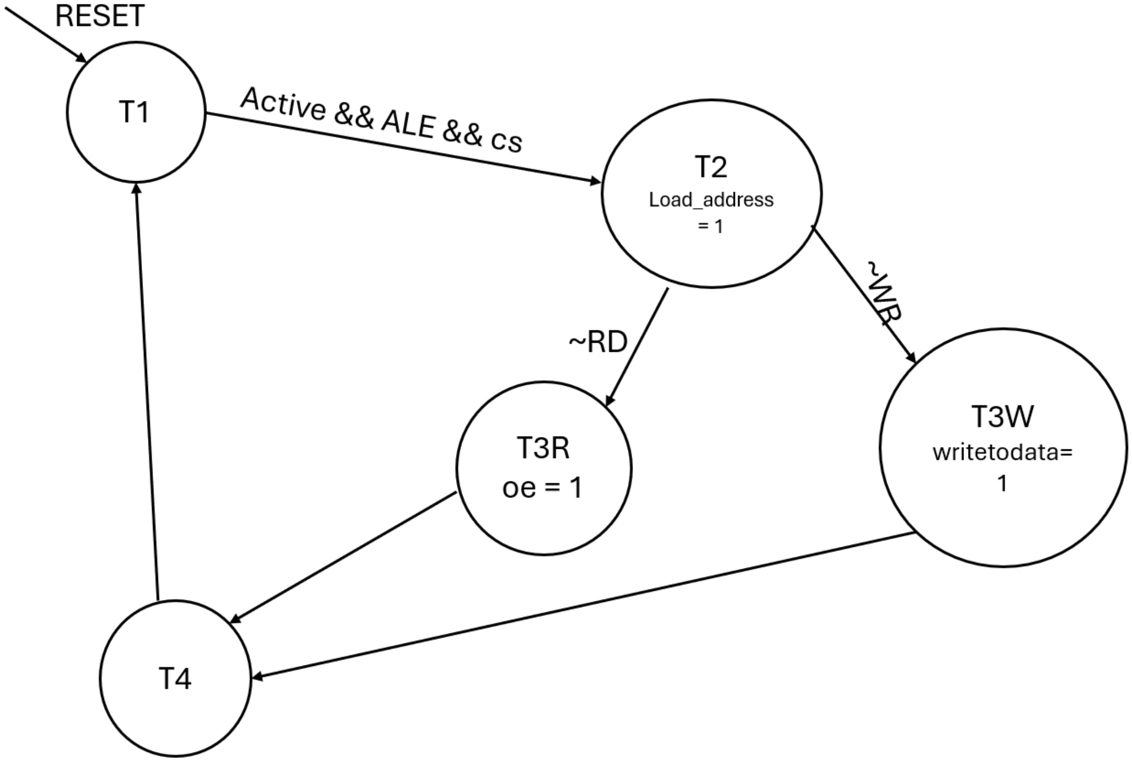
Black Box:



Block Diagram:



State Transition Diagram for FSM:



We used 3 parameters:
Parameter1: “Active” used to activate certain module. If Active == 0 then the module is disabled. We used this parameter in top module.
Parameter2: “Choosing” used to choose the text file.
Parameter3: “”msize_low and msize_high” are used to specify the width of memory.

Verification Tests

We have created 3 busops files for testing. They are

For busopsIO(IO specified operations)

100	I	R	0x0FF04
101	I	R	0x0FF04
201	I	R	0x2FF08
351	I	R	0x21D02
401	I	W	0x31C01
450	I	R	0x31C01
550	I	W	0x0FF01
551	I	W	0x0FF05
650	I	R	0x0FF01
700	I	R	0x0FF05

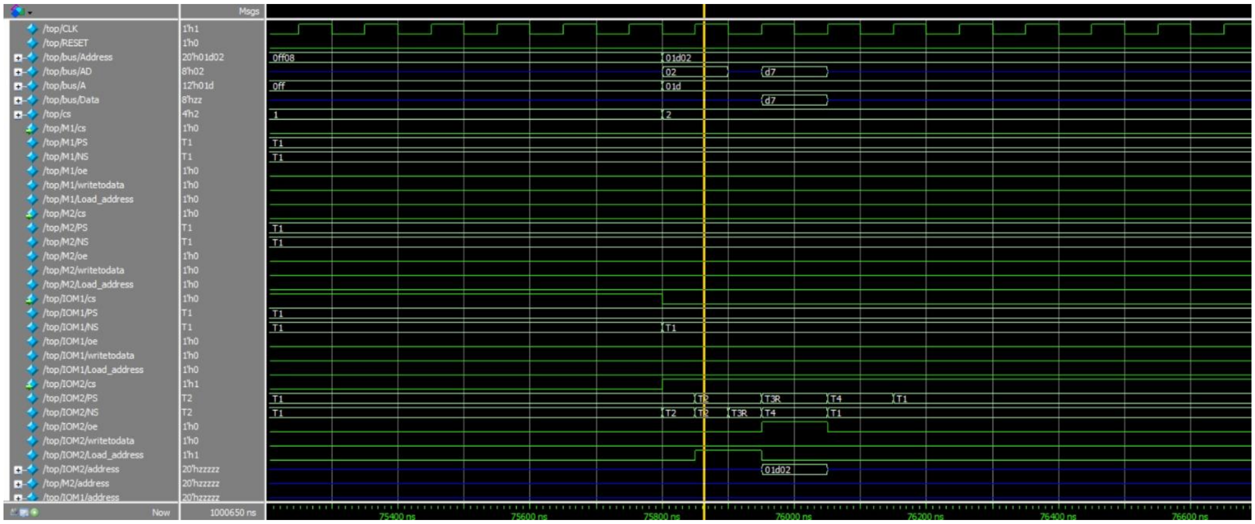
For busopsM(Memory specified operations)

100	M	R	0x00506
101	M	R	0x60607
200	M	W	0xF3333
250	M	R	0xF3333
255	M	R	0x90505
352	M	W	0x44444
353	M	W	0x00404
400	M	R	0x44444
453	M	R	0x00404

For busops(Overall Operations)

100	M	R	0x00506
101	M	R	0x60607
200	M	W	0xF3333
250	M	R	0xF3333
255	M	R	0x90505
352	M	W	0x44444
353	M	W	0x00404
400	M	R	0x44444
500	I	R	0x0FF04
601	I	W	0x2FF08
701	I	R	0x2FF08
751	I	R	0x21D02
801	I	W	0x31C01
850	I	R	0x31C01

Below is the wave for busops file:



	Msgs
/top/CLK	1'h1
/top/RESET	1'h0
/top/bus/Address	20'h01d02
/top/bus/AD	8'h02
/top/bus/A	12'h01d
/top/bus/Data	8'hzz
/top/cs	4'h2
/top/M1/cs	1'h0
/top/M1/PS	T1
/top/M1/NS	T1
/top/M1/oe	1'h0
/top/M1/writetodata	1'h0
/top/M1/Load_address	1'h0
/top/M2/cs	1'h0
/top/M2/PS	T1
/top/M2/NS	T1
/top/M2/oe	1'h0
/top/M2/writetodata	1'h0
/top/M2/Load_address	1'h0
/top/IOM1/cs	1'h0
/top/IOM1/PS	T1
/top/IOM1/NS	T1
/top/IOM1/oe	1'h0
/top/IOM1/writetodata	1'h0
/top/IOM1/Load_address	1'h0
/top/IOM2/cs	1'h1
/top/IOM2/PS	T2
/top/IOM2/NS	T2
/top/IOM2/oe	1'h0
/top/IOM2/writetodata	1'h0
/top/IOM2/Load_address	1'h1
/top/IOM2/address	20'hzzzzz
/top/M2/address	20'hzzzzz
/top/IOM1/address	20'hzzzzz
Now	1000650 ns

Github Link: https://github.com/DivyasriAyluri/Team13_SVProject

References:

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