ASSIGNMENT 3

Satwik Banchhor(2018CS10385)
Diwakar Prajapati(2018CS10330)

AIM - Make a MIPS Processor in VHDL.

DESIGN DETAILS

There is a memory array of 32 bits std_logic_vector of size 4096.
The first 1000 memory address is used for storing program and the rest is used as memory to read and write data or text.

There is also a register array of 32 bits std_logic_vector of size 32.

There are two functions one for initialising memory array and one for initialise register array. Memory array loads instructions into it. Register array is initialises with all zero bits.
We have implemented only six instructions:add, sub, all, srl, lw, sw.

The program is terminated as it see an instruction with all zeroes. The program also terminates if an instruction tries to write on the address of the program.

Implementation:
First the opcode is read and decided whether the instruction is R format or I format, based on the format **rs**, **rt**, **rd**, **shamt**, **func**, **lw** and **sw** is initialised.
The processor takes exactly one cycle per execution of an instruction and overall it takes one extra cycle. In the first cycle only reading the instruction and the variable op, rs, rt, rd, shame, fun, lw, sw is initialised. From the next instruction, it executes the instruction of last program counter and reads the instruction for the current program counter.

To test the Processor, change the path of the input.txt and regin.txt to initialise the memory and the address.