LAB 06 Part 02 – Report

1) Compare your system's performance with the cache-less one from part 1, using test programs, and write a brief report

First when we considering lab 06 part 01, there we do not use cache memory. So data Memory is directly access by CPU. In that case we can see for every memory related instructions we have to stall our CPU for 5 cycles for Data memory Read or Write operations.

In that case, we got much more delay with directly accessing Data memory. So we have to use more efficient way to Data memory accessing. That we brought into implementing Cache memory module.

Cache memory is an extremely fast memory type that acts as a buffer between RAM and the CPU. It holds frequently requested data and instructions so that they are immediately available to the CPU when needed. Cache memory is used to reduce the average time to access data from the Main memory.

In the case of holding frequently using data, we might get an opportunity to get use them again with less access time to them.

So, I have Use SAME INSTUCTIONS of part 01 and part 02 and compared them..

This is Example: - INSTRUCTION SET

1) loadi 1 0x02
2) loadi 2 0x04
3) swi 2 0x8C >>Write miss no dirty
4) lwi 4 0x8C >> read hit
5) loadi 3 0x8A
6) swd 2 3 >>Write miss no dirty
7) lwd 5 3 >>read hit
8) add 5 5 2
9) add 4 4 1

With the Part 01 implementation(non cache) , 3 4 6 7 instructions are stall the cpu as they want to use Data memory for reading or writing processes.

But in part 02 implementation(with cache) , only 3 , 6 instructions are stall the cpu. As 4 and 7 instruction doesn’t want to access Data memory as cache has there needed data.

As this is initially situation for cache memory filling, these two stalls happen. But most of time data memory will not use when cache memory filled rather than miss. And also we have used only 32 byte cache. If it is larger, more hits can get occur.