CALCULATION OF FIFO DEPTH - MADE EASY

Compiled by

Putta Satish

FIFO DEPTH CALCULATION - MADE EASY

We need to employ an asynchronous FIFO between two modules working at different clock domains when some amount of data has to be transmitted from one module to the other to avoid the data loss. FIFO is required, only when you are slow at reading and fast in writing to buffer the data which is not read by the slower module.

The depth (size) of the FIFO should be in such a way that, the FIFO can store all the data which is not read by the slower module. FIFO will only work if the data comes in bursts; you can't have continuous data in and out. If there is a continuous flow of data, then the size of the FIFO required should be infinite. You need to know the burst rate, burst size, frequencies, etc. to determine the appropriate size of FIFO.

> **The logic in fixing the size of the FIFO is to find the no. of data items which are not read in a period in which writing process is done. In other words, FIFO depth will be equal to the no. of data items that are left without reading. With this logic, I tried to fix the size of FIFO required in different scenarios without using any standard formulas which can't be used in every scenario.**

The following examples describe the different possible scenarios in which Asynchronous FIFO is required. In the following examples, I considered that, the module 'A' wants to send some data to the module 'B'.

Case – 1 : $f_A > f_B$ with no idle cycles in both write and read.

Writing frequency = f_A = 80MHz.
Reading Frequency = f_B = 50MHz.
Burst Length = No. of data items to be transferred = 120.
There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.

Sol :

- ✓ Time required to write one data item = $\dfrac{1}{80\ MHz}$ = 12.5 nSec.
- ✓ Time required to write all the data in the burst = 120 * 12.5 nSec. = 1500 nSec.
- ✓ Time required to read one data item = $\dfrac{1}{50\ MHz}$ = 20 nSec.
- ✓ So, for every 20 nSec, the module B is going to read one data in the burst.
- ✓ So, in a period of 1500 nSec, 120 no. of data items can be written.
- ✓ And the no. of data items can be read in a duration of 1500 nSec = $\left(\dfrac{1500\ nSec}{20\ nSec}\right) = 75$
- ✓ The remaining no. of bytes to be stored in the FIFO = 120 – 75 = 45.
- ✓ So, the FIFO which has to be in this scenario must be capable of storing 45 data items.

So, the minimum depth of the FIFO should be 45.

Case – 2 : $f_A > f_B$ with one clk cycle delay between two successive reads and writes.

Sol :

This is just, to create some sort of confusion. This scenario is no way different from the previous scenario (case -1), because, always, there will be one clock cycle delay between two successive reads and writes. So, the approach is same as the earlier one.

<u>Case – 3</u> : $f_A > f_B$ with idle cycles in both write and read.

Writing frequency = f_A = 80MHz.
Reading Frequency = f_B = 50MHz.
Burst Length = No. of data items to be transferred = 120.
No. of idle cycles between two successive writes is = 1.
No. of idle cycles between two successive reads is = 3.

<u>Sol</u> :

✓ The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every **two** clock cycles, one data is written.

✓ The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every **four** clock cycles, one data is read.

✓ Time required to write one data item = $2 * \dfrac{1}{80\ MHz}$ = 25 nSec.

✓ Time required to write all the data in the burst = 120 * 25 nSec. = 3000 nSec.

✓ Time required to read one data item = $4 * \dfrac{1}{50\ MHz}$ = 80 nSec.

✓ So, for every 80 nSec, the module B is going to read one data in the burst.

✓ So, in a period of 3000 nSec, 120 no. of data items can be written.

✓ The no. of data items can be read in a period of 3000 nSec = $\left(\dfrac{3000\ nSec}{80\ nSec}\right) = 37.5 \simeq 37$

✓ The remaining no. of bytes to be stored in the FIFO = 120 – 37 = 83.

✓ So, the FIFO which has to be in this scenario must be capable of storing 83 data items.

So, the minimum depth of the FIFO should be 83.

<u>Case – 4</u> : $f_A > f_B$ with duty cycles given for wr_enb and rd_enb.

Writing frequency = f_A = 80MHz.
Reading Frequency = f_B = 50MHz.
Burst Length = No. of data items to be transferred = 120.
Duty cycle of wr_enb (write enable) = 50 % = ½.
Duty cycle of wr_enb (write enable) = 25 % = ¼.

<u>Sol</u> :

This scenario is no way different from the previous scenario (case - 3), because, in this case also, one data item will be written in 2 clock cycles and one data item will be read in 4 clock cycles.

Note : Case - 2 and Case - 4 are explained to make everyone understand that the same question can be asked in a different way.

Case – 5 : $f_A < f_B$ with no idle cycles in both write and read (i.e., the delay between two consecutive writes and reads is one clock cycle).

       Writing frequency = f_A = 30MHz.
       Reading Frequency = f_B = 50MHz.
       Burst Length = No. of data items to be transferred = 120.
       There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.

Sol :

- ✓ In this case, a FIFO of depth '1' will be sufficient because, there will not be any data loss since the reading is faster than writing.

Case – 6 : $f_A < f_B$ with idle cycles in both write and read (duty cycles of wr_enb and rd_enb can also be given in these type of questions).

       Writing frequency = f_A = 30MHz.
       Reading Frequency = f_B = 50MHz.
       Burst Length = No. of data items to be transferred = 120.
       No. of idle cycles between two successive writes is = 1.
       No. of idle cycles between two successive reads is = 3.

Sol :

- ✓ The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every **two** clock cycles, one data is written.
- ✓ The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every **four** clock cycles, one data is read.
- ✓ Time required to write one data item = $2 * \dfrac{1}{30\ MHz}$ = 66.667 nSec.
- ✓ Time required to write all the data in the burst = 120 * 66.667 nSec. = 8000 nSec.
- ✓ Time required to read one data item = $4 * \dfrac{1}{50\ MHz}$ = 80 nSec.
- ✓ So, for every 80 nSec, the module B is going to read one data item in the burst.
- ✓ So, in a period of 8000 nSec, 120 no. of data items can be written.
- ✓ The no. of data items can be read in a period of 8000 nSec = $\left(\dfrac{8000\ nSec}{80\ nSec}\right) = 100$
- ✓ The remaining no. of bytes to be stored in the FIFO = 120 – 100 = 20.
- ✓ So, the FIFO which has to be in this scenario must be capable of storing 20 data items.

So, the minimum depth of the FIFO should be 20.

Case – 7 : $f_A = f_B$ **with no idle cycles in both write and read (i.e., the delay between two consecutive writes and reads is one clock cycle).**

        Writing frequency = $f_A = f_B$ = 30MHz.
        Burst Length = No. of data items to be transferred = 120.
        There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.

Sol :

- ✓ FIFO is not required if there is no phase difference between clk_A and clk_B.
- ✓ A FIFO of depth '1' will be sufficient if there is some phase difference between clk_A and clk_B.

Case – 8 : $f_A = f_B$ **with idle cycles in both write and read (duty cycles of wr_enb and rd_enb can also be given in these type of questions).**

        Writing frequency = f_A = 50MHz.
        Reading Frequency = f_B = 50MHz.
        Burst Length = No. of data items to be transferred = 120.
        No. of idle cycles between two successive writes is = 1.
        No. of idle cycles between two successive reads is = 3.

Sol :
- ✓ The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every **two** clock cycles, one data is written.
- ✓ The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every **four** clock cycles, one data is read.
- ✓ Time required to write one data item = $2 * \dfrac{1}{50\ MHz}$ = 40 nSec.
- ✓ Time required to write all the data in the burst = 120 * 40 nSec. = 4800 nSec.
- ✓ Time required to read one data item = $4 * \dfrac{1}{50\ MHz}$ = 80 nSec.
- ✓ So, for every 80 nSec, the module B is going to read one data item in the burst.
- ✓ So, in a period of 4800 nSec, 120 no. of data items can be written.
- ✓ The no. of data items can be read in a period of 4800 nSec = $\left(\dfrac{4800\ nSec}{80\ nSec} \right) = 60$
- ✓ The remaining no. of bytes to be stored in the FIFO = 120 – 60 = 60.
- ✓ So, the FIFO which has to be in this scenario must be capable of storing 60 data items.

So, the minimum depth of the FIFO should be 60.

Case – 9 : If the data rates are given as follows.

> Writing Data = 80 DATA/100 Clock (Randomization of 20 Data's)
> Outgoing Data= 8 DATA/10 Clock.
> Burst size = 160

Sol :

- ✓ The given specifications indicate that the Writing Frequency is equal to reading frequency.
- ✓ But, both reading and writing can happen at any random instants with the constraints that "writing of 80 data items will be completed in 100 cycles" and "reading of 8 data items will be completed in 10 cycles".
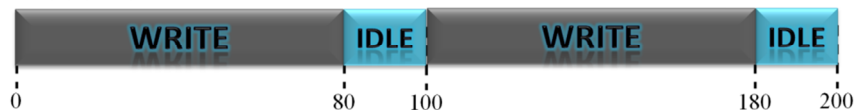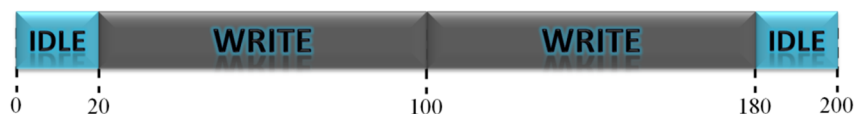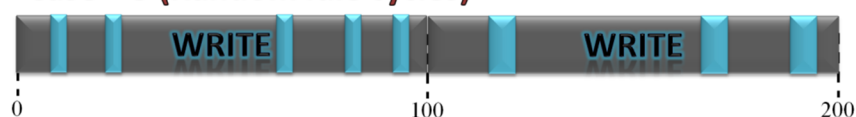- ✓ The following are possibilities.

Case - 1
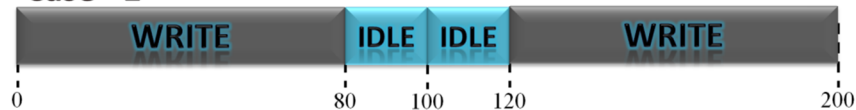
Case - 2

Case - 3

Case - 4

Case – 5 (Random Idle cycles)

- ✓ The following are the observations from the above diagram.

Case	No. of cycles taken to complete write
1	200
2	200
3	180
4	160
5	200

- ✓ To obtain safer FIFO size, we need to consider the worst case scenario for the data transfer across the FIFO under consideration to avoid the data loss.
- ✓ For worst case scenario, the difference between the data rate between write and read should be maximum. Hence, for write operation, maximum data rate should be considered and for read operation, minimum data rate should be considered.
- ✓ The maximum data rate for the write is in case – 4. (Write operation is completed in minimum no. of cycles in this case). So, consider the case - 4 for further calculations.
- ✓ So, in a period of 160 clock cycles, 160 no. of data items can be written.
- ✓ The data rate for the read is 8 data / 10 clock cycles.
- ✓ The no. of data items can be read in a period of 160 clock cycles = $\left(\frac{160*8}{10}\right) = 128$
- ✓ The remaining no. of bytes to be stored in the FIFO = 160 – 128 = 32.
- ✓ So, the FIFO which has to be in this scenario must be capable of storing 32 data items.

So, the minimum depth of the FIFO should be 32.

Case – 10 : Specifications can be given in a different way. (Understanding the specifications is important here)

Given the following FIFO rules, how deep does the FIFO need to be to prevent underflow or overflow?

Frequency (clk A) = frequency (clk B)/4
Period (en_B) = period (clk_A)*100
Duty cycle (en_B) = 25%

Sol :
- ✓ Assume some numerical values, if the specifications are in this way.
- ✓ Assume frequency of clk_B = 100MHz
- ✓ So, the frequency of clk_A = 100MHz /4 = 25MHz.
- ✓ In the specifications given, the burst length is specified indirectly. The burst length is 100.
- ✓ Time required to write one data item = $\frac{1}{25\ MHz}$ = 40 nSec.
- ✓ Time required to write all the data in the burst = 100 * 40 nSec. = 4000 nSec.
- ✓ And the duty cycle of en_B is 25 % means that, out of 4000 nSec in which the writing process is completed, reading is done only in a period of 1000 nSec (25% of 4000 nSec.)
- ✓ So, the FIFO should be capable of holding the data which is being written in the remaining 3000 nSec.
- ✓ The no. of data items can be read in a period of 3000 nSec = $\left(\frac{3000\ nSec}{40\ nSec}\right) = 75$

So, the minimum depth of the FIFO should be 75.