GNN-Based Depth Predictor

Accelerating Hardware with AI

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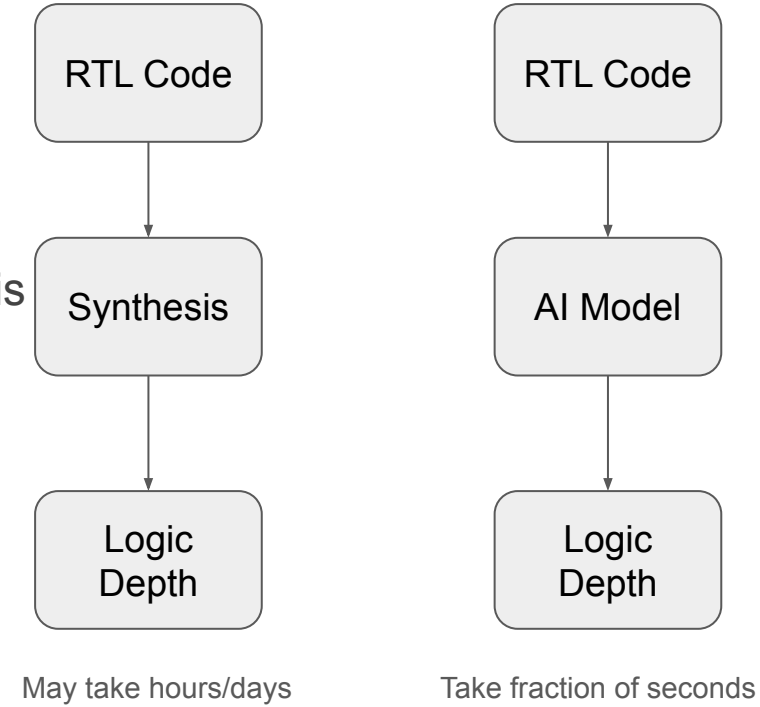
Agenda

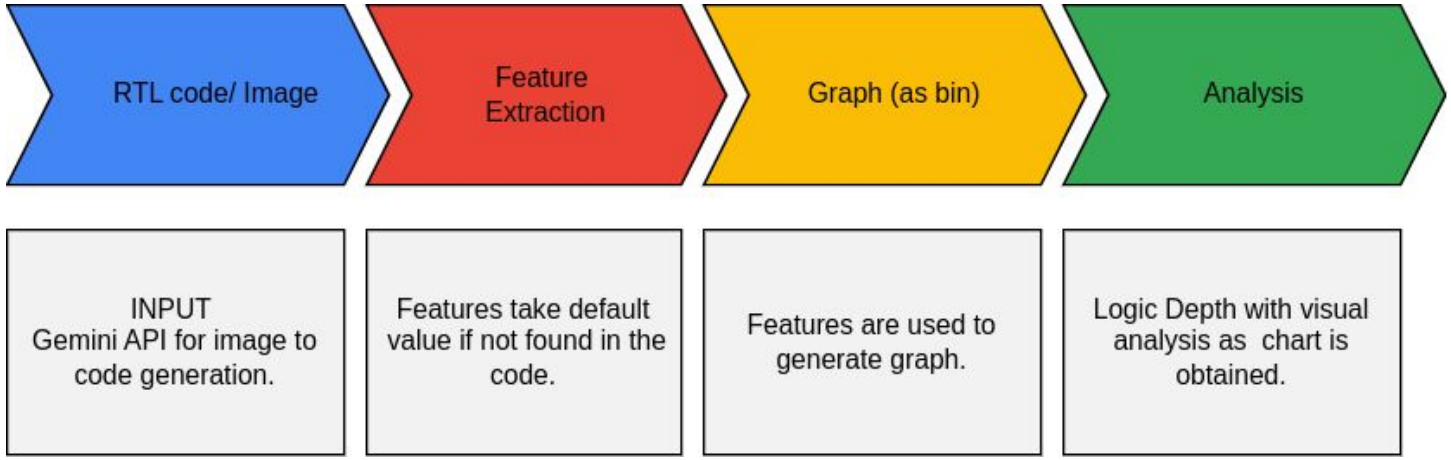
- Problem Statement
- Proposed Solution
- Model Architecture
- Results & Metrics
- Comparison
- Future Scope
- Innovation
- Demo

1. Problem Statement

- **What:** Predict Combinational Logic Depth from RTL code.
- **Why:** Fabrication based timing analysis takes hours/days, slowing project timelines.
- **For Whom:** Hardware designers working on IP/SoC designs.



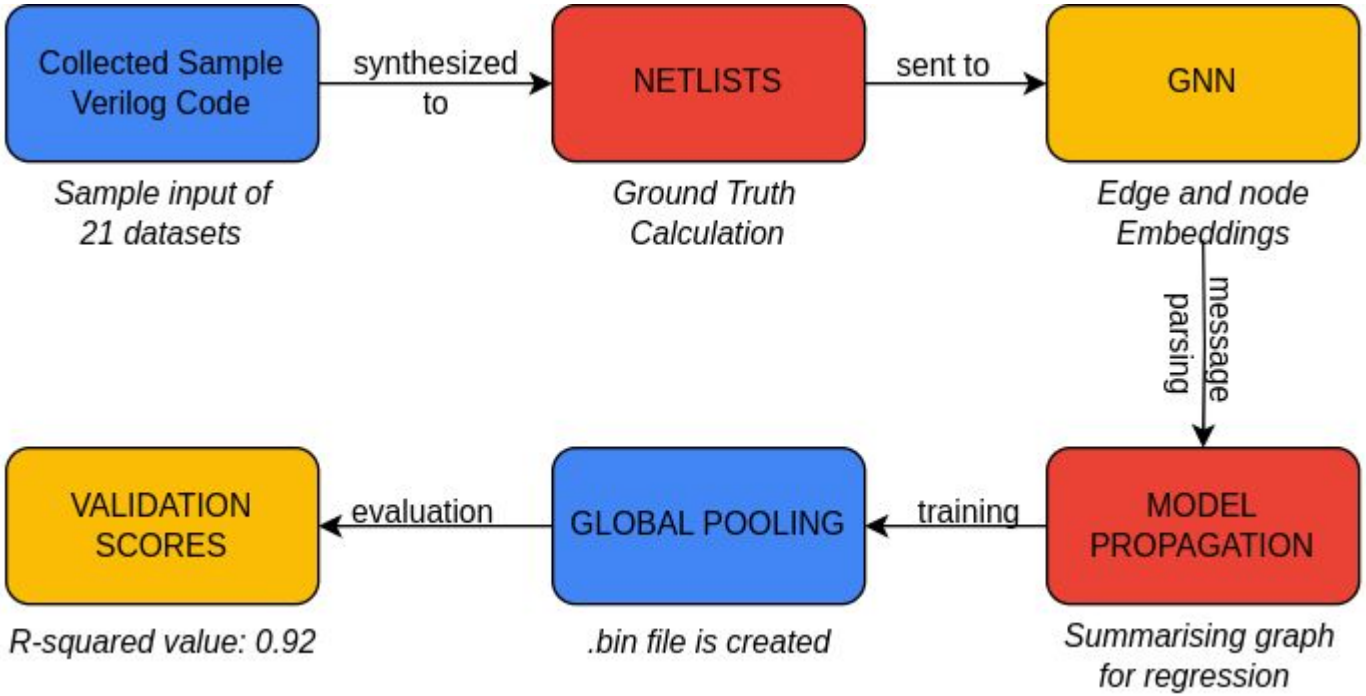
2. Proposed Solution



Model.pth is used for inferencing on Graph generated

Tools Used: PyTorch, PyVerilog, Streamlit

3. Model Architecture



4. Results & Metrics

Training Data

Name	r2 Score	Time (s)
blabla	0.96157	1.4866
usb_cdc_core	0.97505	0.35034
BM64	0.97664	0.79075
salsa20	0.92088	1.4051
aes128	0.02668	4.41911
wbqspiflash	0.98398	1.14926
cic_decimator	0.98398	1.14926
aes256	0.99221	1.21171
des	0.99712	0.14436
aes_cipher	0.99221	1.21171
picorv32a	0.9784	0.07533
zipdiv	0.9784	0.07533
genericfir	0.9784	0.07533
usb	0.9784	0.07533

Testing Data

Name	r2 Score	Time (s)
jpeg_encoder	0.88197	4.81004
usbf_device	0.92518	1.16081
aes192	0.86051	4.43995
xtea	0.91354	0.2356
spm	0.92559	0.69624
y_huff	0.92559	0.69624
synth_ram	0.8656	0.34025

Accuracy: R^2 Score: 0.92
Inference Speed: Milliseconds per signal vs. 2–8 hours for synthesis

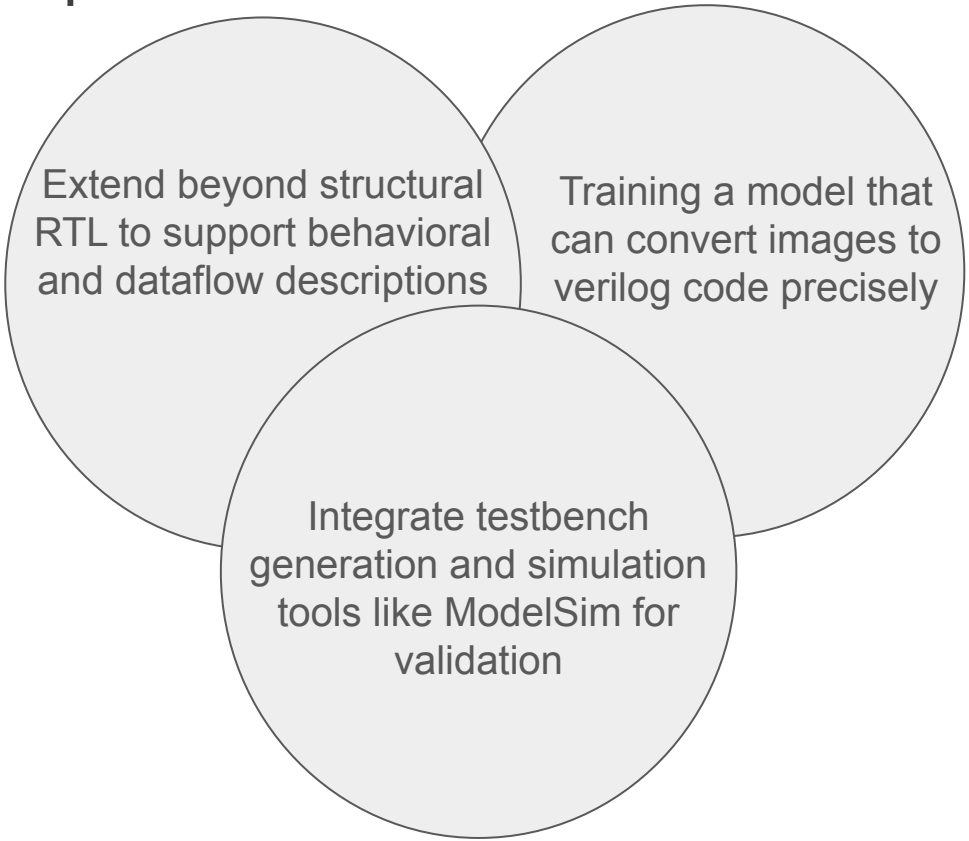
5. Comparison

XGBoost: Fails to capture hierarchical graph dependencies effectively.

GAT: Good accuracy but suffers from slow inference speed.

RNNs: Struggle to model complex graph-based relationships.

6. Future Scope



7. Innovation:

Scalability for Complex IPs and SoCs

- Works with Verilog RTL designs, making it suitable for large-scale System-on-Chip (SoC) projects.

Reducing Time-to-Market

- By eliminating multiple synthesis iterations, the AI model helps accelerate chip development cycles.

Data-Driven Learning for Better Accuracy

- Using datasets from previous synthesis runs, the model improves its predictions, making it more reliable over time.

Fast Detection of Timing Violations

- Early identification of signals exceeding timing constraints, preventing late-stage design rework.

Project Resources:

- Working Demo:

Thank you

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