KTU NOTES

The learning companion.

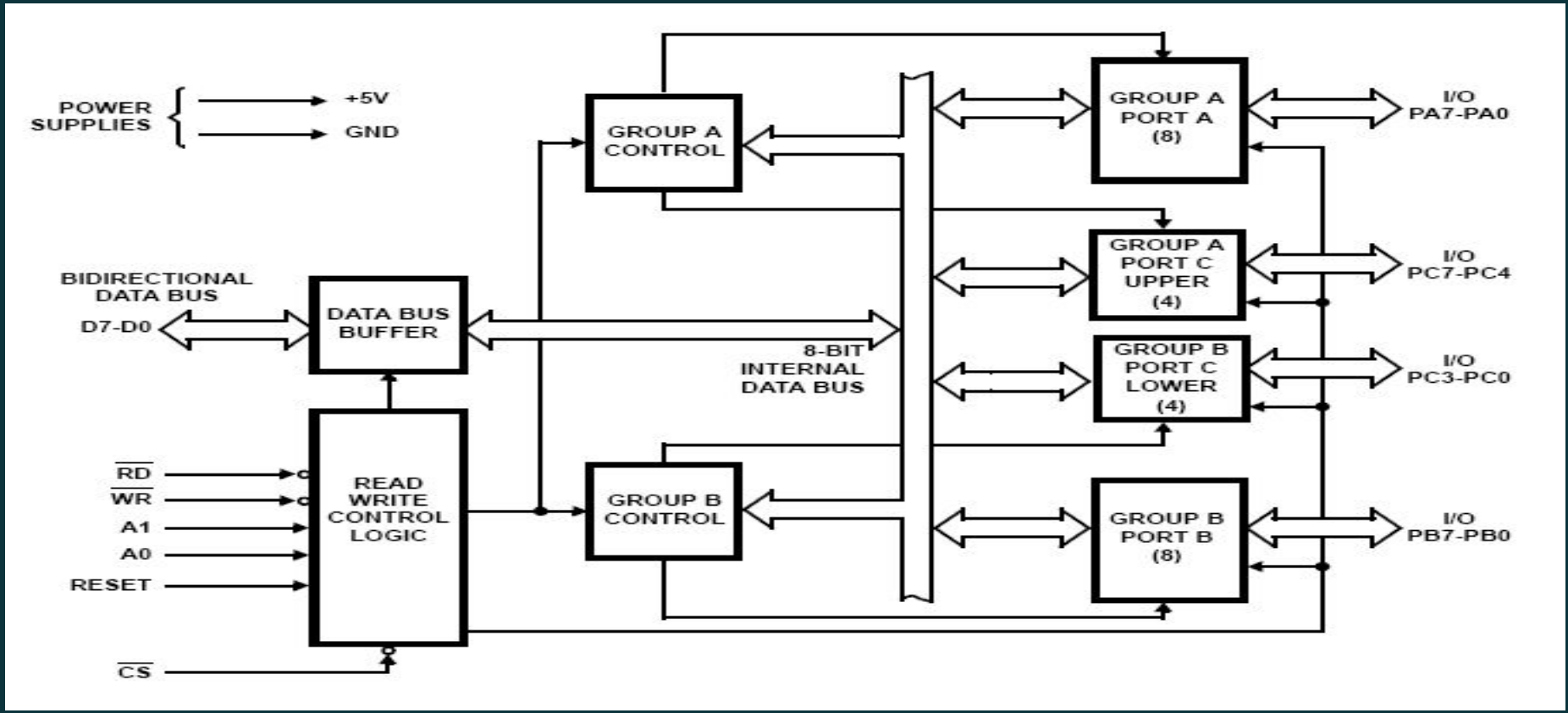
KTU STUDY MATERIALS | SYLLABUS | LIVE NOTIFICATIONS | SOLVED QUESTION PAPERS

8255 - Programmable Peripheral Interface (PPI) / Programmable I/O port (PIO)

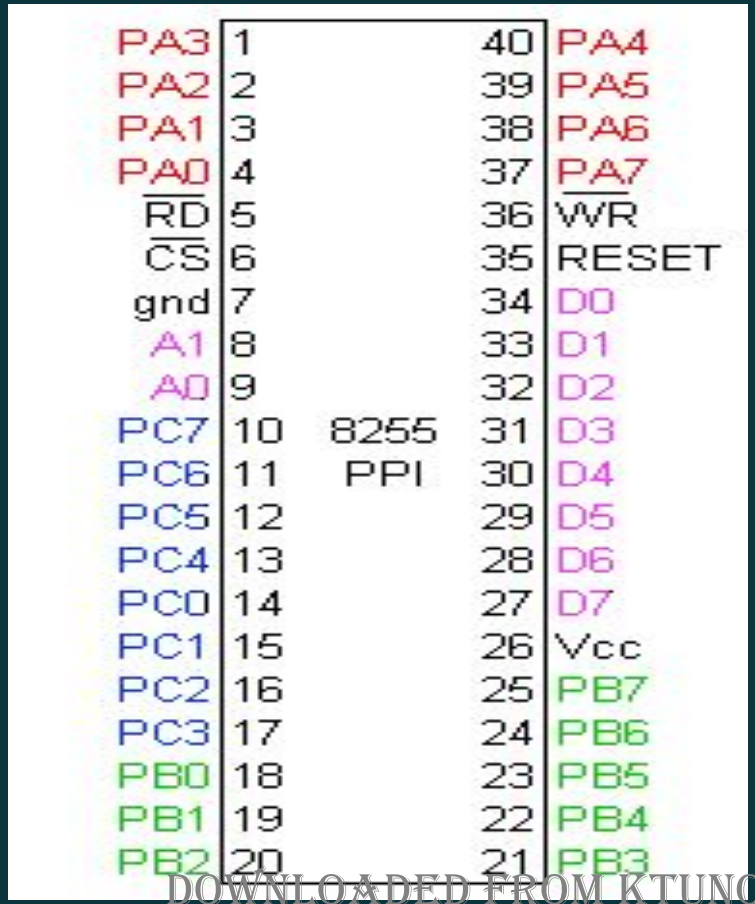
- It is an I/O port chip used for interfacing I/O devices with microprocessor system.
- It is device used to implement parallel data transfer between processor and slow peripheral devices like ADC, DAC, keyboard, 7-segment display, lCD etc.
- It is a programmable device.

- 8255A has three ports
  - PORT A
  - PORT B
  - PORT C
- **Port A** and **Port B** are 8 bit parallel ports (PA0 - PA7 & PB0 - PB7)
- **Port C** can be split into two parts, i.e. PORT C lower (PC0 - PC3) and PORT C upper (PC7 - PC4)
- These three ports are further divided into two groups,
  - i.e. *Group A* includes PORT A and upper PORT C.
  - *Group B* includes PORT B and lower PORT C
- These two groups can be programmed in three different modes.

Block Diagram-8255



Pin Diagram



Function of pins:

- Data bus(D_0-D_7):These are 8-bit bi-directional buses, connected to 8086 data bus for transferring data.

- $\overline{CS}$: This is Active Low signal. It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255 and the CPU.

- $\overline{Read}$: This is Active Low signal, when it is Low the microprocessor reads data from a selected I/O port of 8255A.

- $\overline{Write}$: This is Active Low signal, when it is Low the microprocessor writes data into a selected I/O port .

- Address (A_0-A_1):This is used to select the ports.

A1	A0	Select
0	0	PA
0	1	PB
1	0	PC
1	1	Control word reg.

- RESET: This is used to reset the device.
- PA_0-PA_7:It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.
- PB_0-PB_7:Similar to PA
- PC_0-PC_7:This is also 8-bit bidirectional I/O pins. These lines are divided into two groups.
  - PC_0 to PC_3(Lower Groups)
  - PC_4 to PC_7 (Higher groups)

  These two groups working in separately using 4 data's.

Data Bus buffer:

- D_0-D_7 is a 8-bit bidirectional Data bus.
- Used to interface between 8255 data bus with system bus.
- Pins D_0-D_7 and data pins of microprocessor are connected.
- The direction of data buffer is decided by Read/Control Logic.

Read/Write Control Logic:

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	*Input (Read) cycle*
0	1	0	0	0	Port A to data bus
0	1	0	0	1	Port B to data bus
0	1	0	1	0	Port C to data bus
0	1	0	1	1	CWR to data bus

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	*Output (Write) cycle*
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

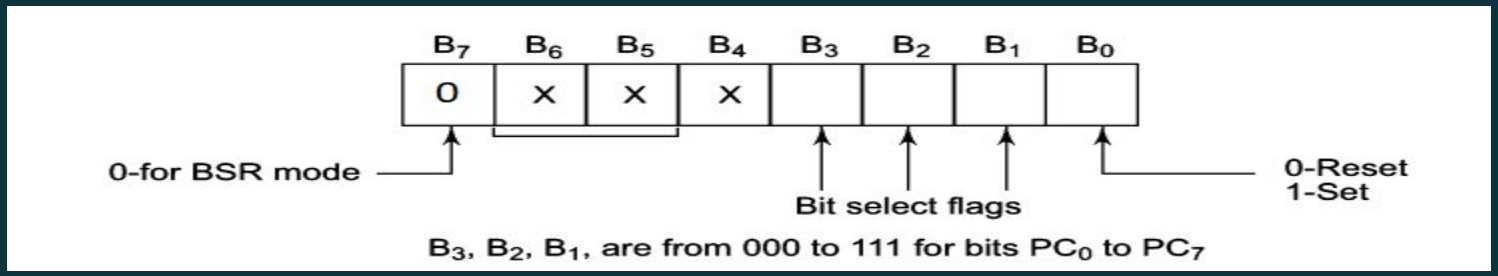
$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	*Function*
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

Modes of operation of 8255

- BSR (Bit Set-Reset mode)
- I/O mode
  - Mode-0 (simple I/O mode)
  - Mode-1 (Handshake I/O mode or strobed I/O mode)
  - Mode-2 (Bidirectional I/O mode or strobed bidirectional I/O mode)

BSR (Bit Set-Reset mode)

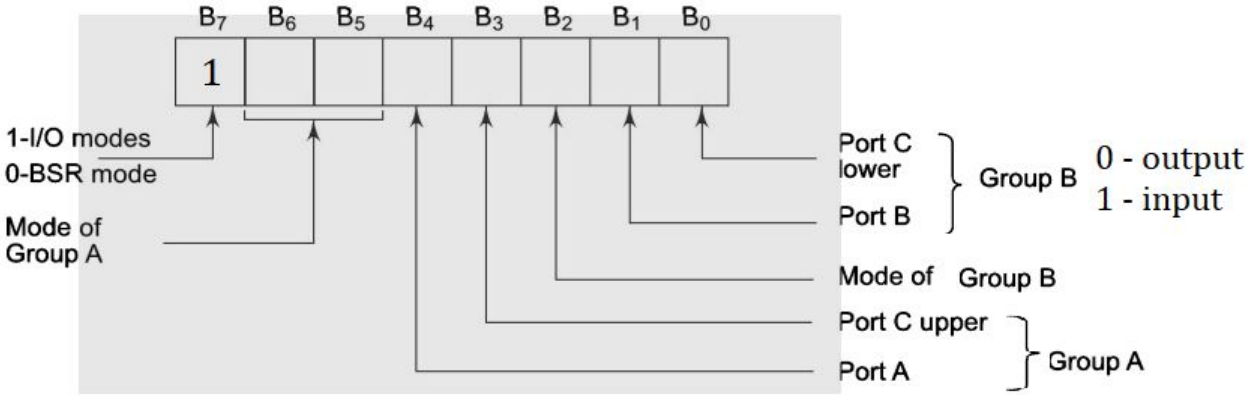
- Only for Port C
- Used to set or reset individual bits of Port C
- The control word register (CWR) format for BSR mode is



B_3	B_2	B_1	*Selected Bits of port C*
0	0	0	PC0
0	0	1	PC1
0	1	0	PC2
0	1	1	PC3
1	0	0	PC4
1	0	1	PC5
1	1	0	PC6
1	1	1	PC7

I/O modes

- CWR format



Group A modes

B_6	B_5	Mode
0	0	mode 0
0	1	mode 1
1	0	mode 2
1	1	x

Group B modes

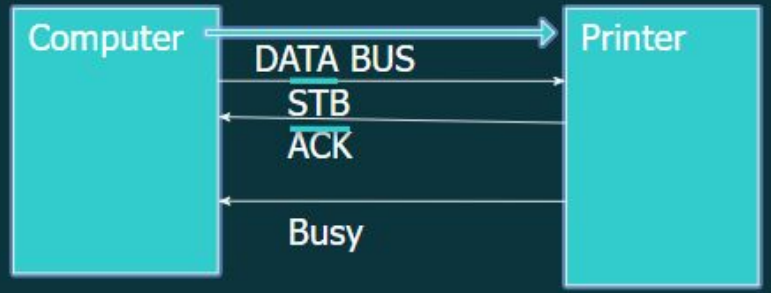
B2	Mode
0	mode 0
1	mode 1

Mode 0 (simple I/O mode)

- In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports.
- Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched.
- Ports do not have interrupt capability.
- Ports in mode 0 is used to interfaces LEDs, Hexa keypad and 7 segment LEDS to the processor.

Mode 1

- In this mode, Port A and B is used as 8-bit I/O ports.
- They can be configured as either input or output ports.
- Each port uses three lines from port C as handshake signals.
- Inputs and outputs are latched
- In this mode, input or output is transferred by hand shaking Signals.
- Handshaking signals is used to transfer data between whose data transfer rate are not same.



Mode 2

- In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1.
- Port A uses five signals from Port C as handshake signals for data transfer.
- The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.
- This mode allows bidirectional data transfer over a single 8-bit data bus using handshake signals.
- This feature is possible only Group A

8254/8253 - Programmable Interval Timer (PIT)

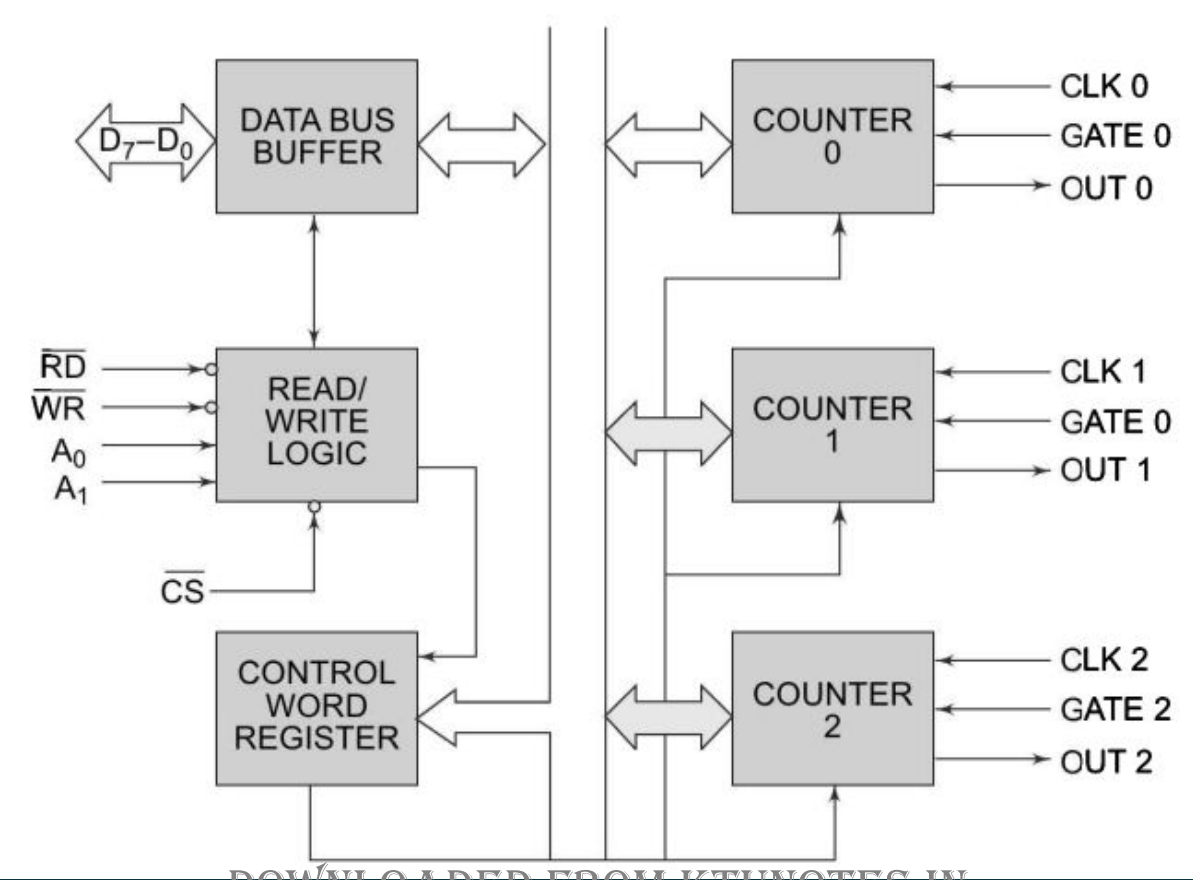
- The Intel 8254 is a Programmable Interval Timers (PTI) designed for microprocessors to perform timing and counting functions using three independent 16-bit counters.

- Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for “OUT” output.

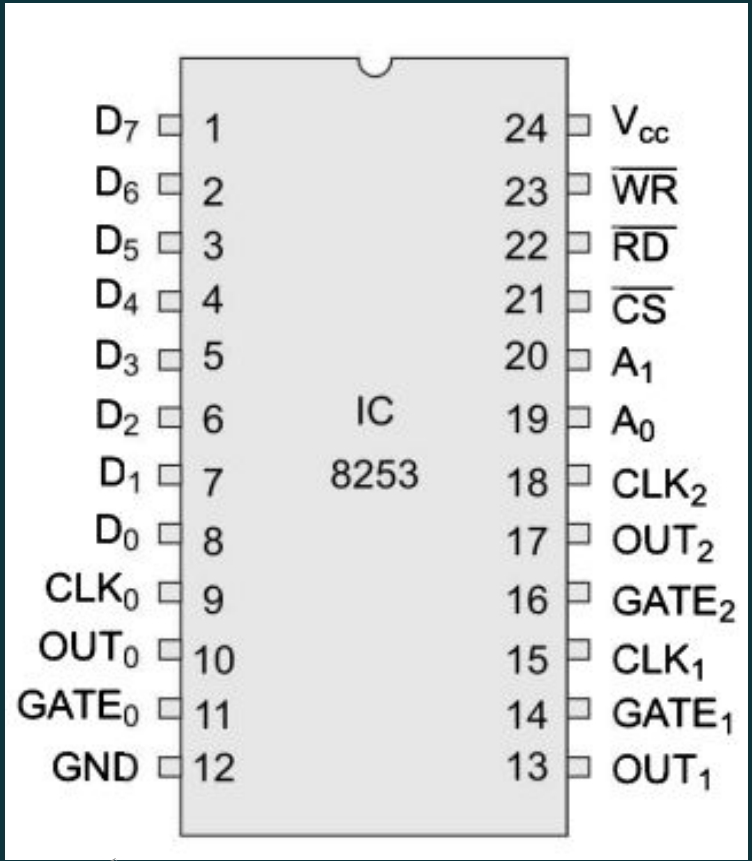
- Each counter is capable of handling clock inputs up to 10 MHz.

- *To operate a counter, a 16-bit count is loaded in its register. On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.*

Internal Block Diagram - 8254



Pin Diagram



Function of pins:

- $\overline{CS}$ - Chip select: when it is low, enables the communication between 8086 and 8254.
- $\overline{WR}$: when it is low, the CPU output data for mode information is load to the counters.
- $\overline{RD}$: when it is low,the CPU reads data from counter.
- A0-A1: These pins are connected to address bus. These are used to select one of the three counters.
- D0-D7: These are tri-state bidirectional data bus used to interface 8254 to the system data bus.

- CLK0, CLK1 and CLK2: These are clock signals for counter0, counter1 and counter2.
- GATE0, GATE1 and GATE2: These are gate terminals for counter0, counter1 and counter2.
- OUT0, OUT1and OUT2: These are output terminals for counter0, counter1 and counter2.

Block diagram description:

- Data Bus Buffer:
  - It is a bi-directional, 8-bit buffer, which is used to interface the 8254 to the system data bus.
  - It has three basic functions Programming the modes of 8254. Loading the count registers. Reading the count values.
- Read/Write Logic:
  - It includes 5 signals, i.e. RD, WR, CS and the address lines A0 & A1.
  - In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively.
  - In the memory mapped I/O mode, these are connected to MEMR and MEMW.

- Writing and reading the counter value is done using IN and OUT instructions.
- Address lines A0 & A1 of 8086 are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address.
- The control word register and counters are selected according to the signals on lines A0 & A1.

Selected Operations for Various Control Inputs of 8254

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	*Selected Operation*
0	1	0	0	0	Write Counter 0
0	1	0	0	1	Write Counter 1
0	1	0	1	0	Write Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation (tristated)
0	1	1	×	×	No Operation (tristated)
1	×	×	×	×	Disabled (tristated)

- Counters:
  - Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD.
  - Its input and output is configured by the selection of modes stored in the control word register.
  - The programmer can read the contents of any of the three counters without disturbing the actual counting process - “on the fly” reading of counters.

- Control Word Register:
  - 8-bit register
  - The bits D7 and D6 of the control word are to select one of the 3 counters.
  - D5 and D4 are for loading /reading the count.
  - D3,D2 and D1 are for the selection of operating mode of the selected counter.
  - D0 for to select whether the counter is operated in binary or BCD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Control Word Format

SC_1	SC_0	OPERATION
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

SC-Select Counter Bit Definitions

RL_1	RL_0	OPERATION
0	0	Latch Counter for 'ON THE FLY' reading
0	1	Read/Load Least Significant Byte only
1	0	Read/Load MSB only
1	1	Read/Load LSB first then MSB

RL-Read/Load Bit Definitions

M_2	M_1	M_0	Selected Mode
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

$M_2M_1M_0$ Mode Select Bit Definitions

BCD	Operation
0	Hexadecimal Count
1	BCD Count

HEX/BCD Bit Definition

Control Word Format and Bit Definitions

- Counter Latch Command:

  In this method, an appropriate control word is written into the control register to latch a count in the output latch, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high order byte.

- Read-Back Command:

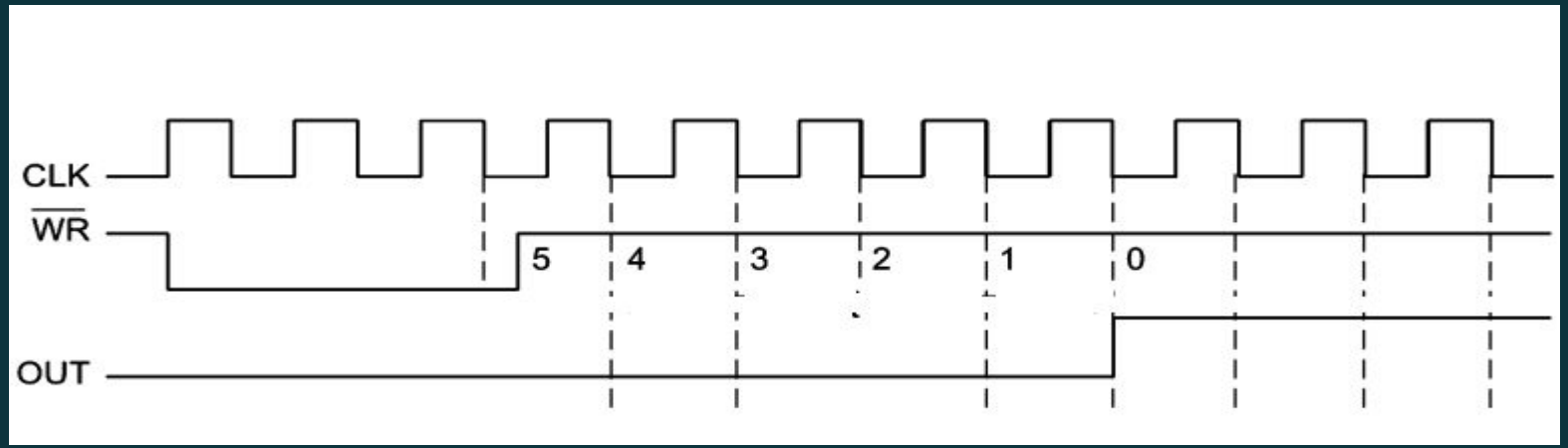
  This method allows the user to check the count value, programmed Mode, and current status of the OUT pin and Null count flag of the selected counter(s)

Operating modes of 8254

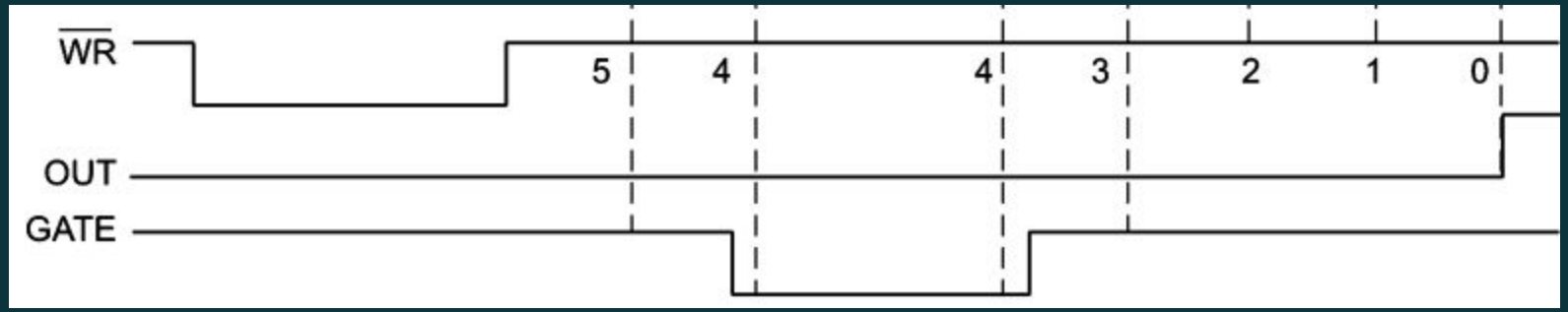
- 6 operating modes:
    1. Mode 0 (Interrupt on terminal count)
    2. Mode 1 (programmable Monoshot)
    3. Mode 2 (Rate Generator)
    4. Mode 3 (Square Wave Generator)
    5. Mode4(Software Triggered Strobe)
    6. Mode 5 (Hardware Triggered Strobe)

Mode 0 (Interrupt on terminal count)

- In this mode OUT is initially low.
- Once a count is loaded the counter is decremented after every cycle (falling edge) and when count reaches zero, the OUT goes high.
- This can be used as an interrupt.
- The OUT remains high until a new count or command word is loaded.

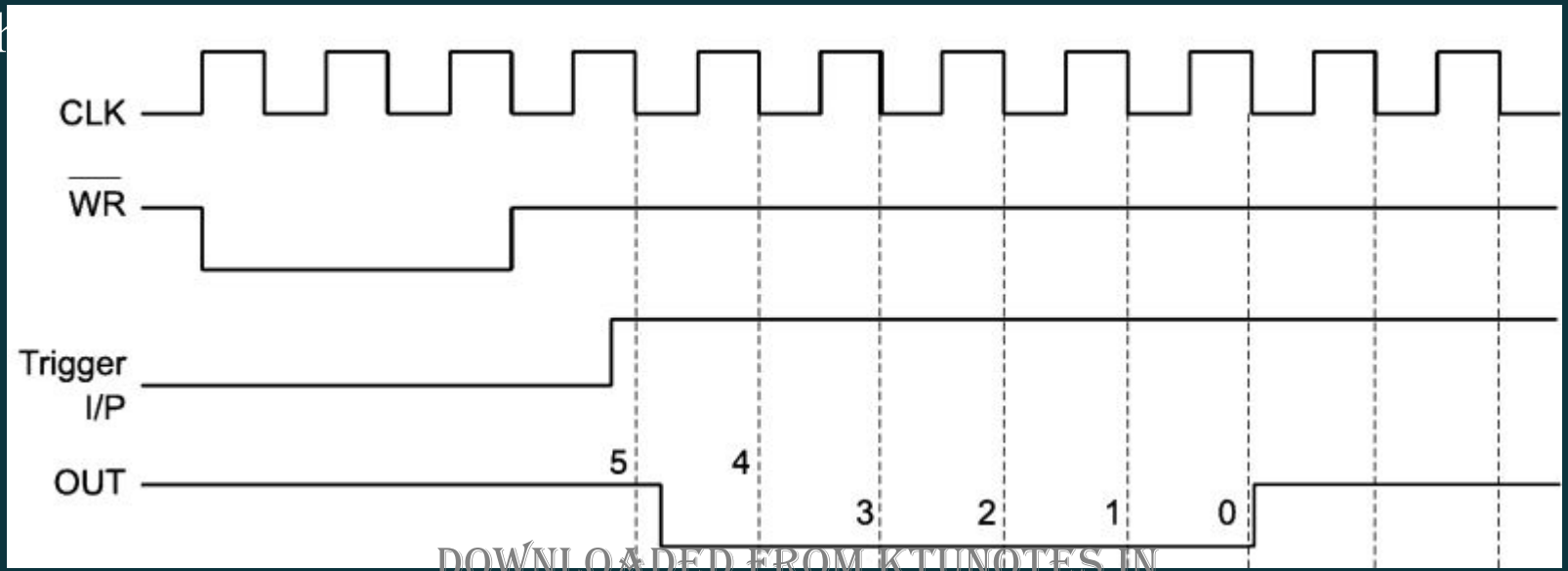


- GATE signal should be HIGH for normal counting. When GATE goes LOW counting is terminated and the current count is latched till GATE goes HIGH again.



Mode 1 (programmable Monoshot)

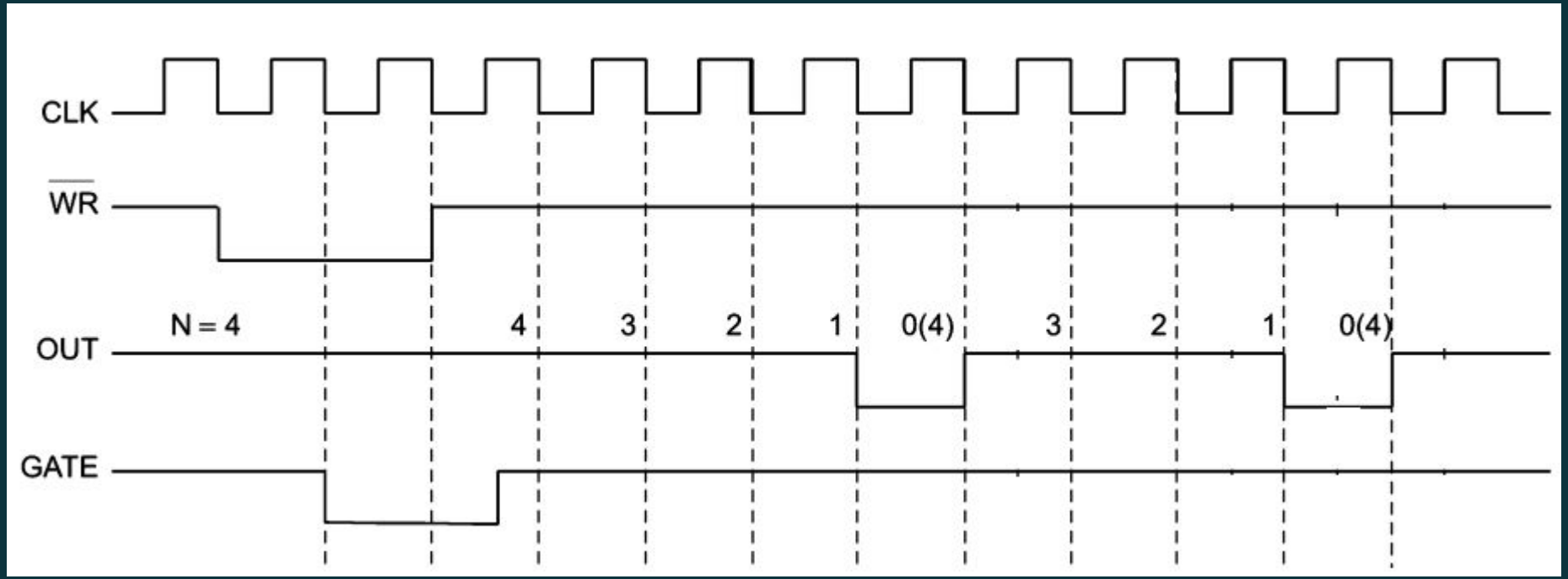
- In this mode OUT is initially high.
- In this mode 8254 can be used as a monostable multivibrator.
- GATE is used as trigger.
- When gate is triggered, the OUT goes low and at the end of count it goes h



Mode 2 (Rate generator)

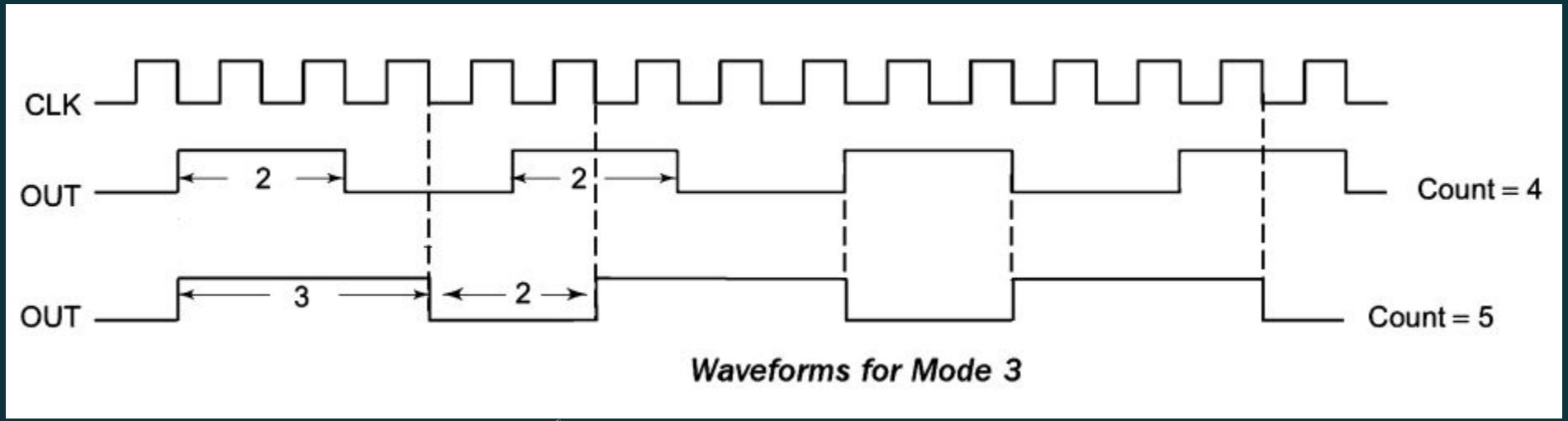
- The mode is used to generate a pulse equal to given clock period at a given interval.
- When a count is loaded, the OUT stays high until count reaches 1 and then OUT goes low for 1 clock period then gets reloaded automatically and this is how pulse gets generated continuously.
- GATE signal should be HIGH. When GATE goes LOW counting is terminated and the current count is latched till GATE goes HIGH again.

Mode 2 - waveforms



Mode 3 (Square wave generator)

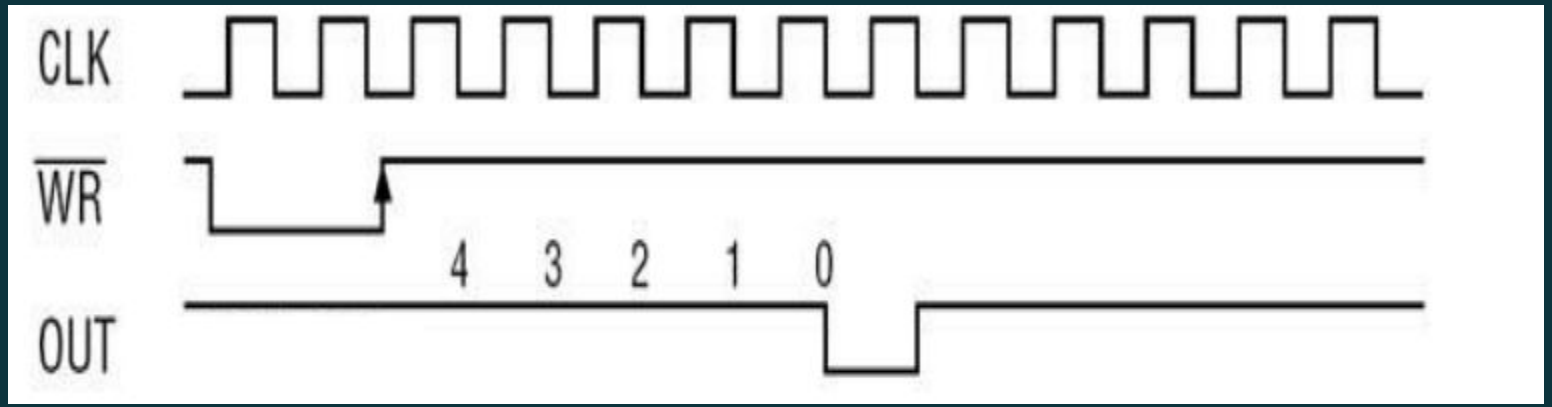
- In this mode a continuous square wave with period equal to count (N) is generated.
- The frequency of square wave = frequency of clock divide by count = f/N
- If count (N) is odd pulse stay high for (N + 1)/2 and low for (N - 1)/2



Waveforms for Mode 3

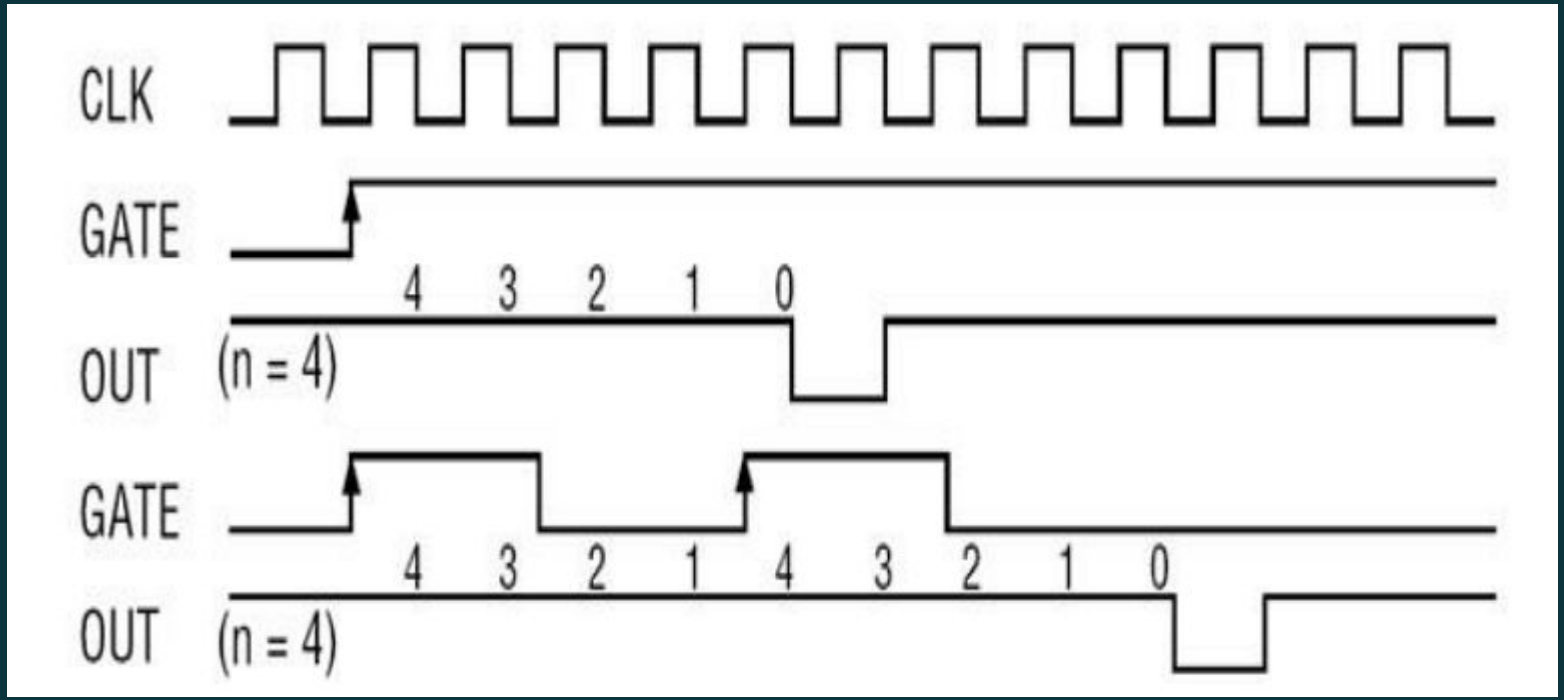
Mode 4 (Software trigger strobe)

- In this mode OUT is initially high
- It goes low for one clock period at the end of count.
- This low pulse can be used as strobe while interfacing 8086 with other peripherals.
- The count must be reloaded for subsequent outputs.



Mode 5 (Hardware trigger strobe)

- Same as mode 4 except that it is triggered by rising pulse at gate.



8257
DIRECT MEMORY ACCESS (DMA) CONTROLLER

- It is designed by Intel **to transfer data at the fastest rate**. It allows the **device to transfer the data directly to/from memory** without any interference of the CPU.
- Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory.
- The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

The sequences of operations performed by a DMA are :

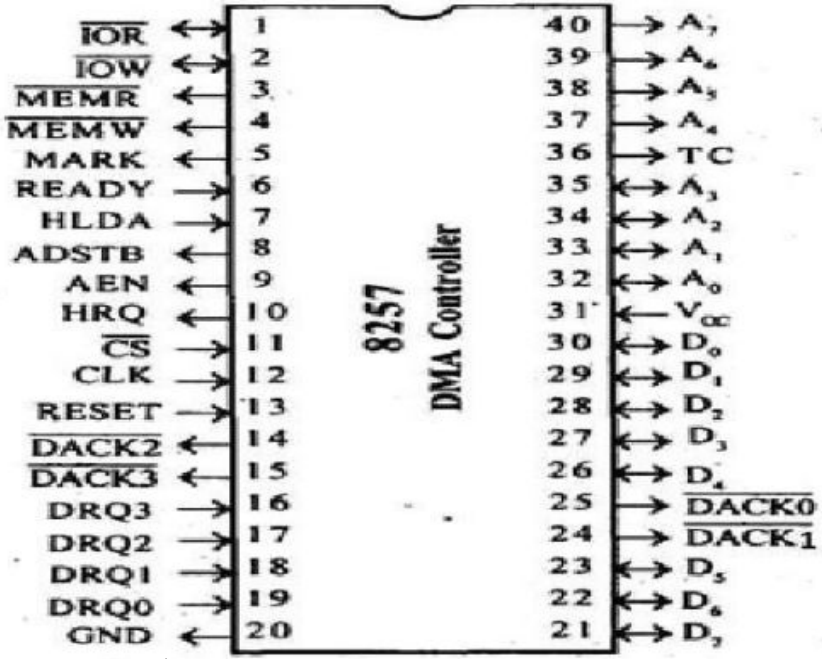
1. Initially, when any device has to send data to the memory, the device has to send DMA request (DRQ) to DMA controller.
2. The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA signal.
3. Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU will relinquish the bus and acknowledges the HOLD request through HLDA signal.
4. Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the memory interfaced with Microprocessor and I/O devices.

FEATURES OF 8257

- It has four channels that can be used over four I/O devices. Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently. Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e., **Master mode and Slave mode**.

8257 PIN DESCRIPTION

The pin configuration of DMA Controller (8257) is shown in Figure and the descriptions are as follows:



DRQ0−DRQ3 These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ0 has the highest priority and DRQ3 has the lowest priority.

DACKo − DACK3 These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

Do − D7 These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch.

IOR It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK It is a clock frequency signal which is required for the internal operation of 8257.

RESET This signal is used to RESET the DMA controller by disabling all the DMA channels.

Ao - A3 These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS It is an active-low chip select line.

READY It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW It is the active-low state signal which is used to write the data to the addressed memory location during DMA write operation.

ADSTB - strobe It is a control output line used to split data and address line through Latches.

AEN This signal is used to disable the address bus/data bus.

TC It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

MARK The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc It is the power signal which is required for the operation of the circuit.

INTERNAL ARCHITECTURE OF 8257:

The functional Block Diagram of DMA controller(8257) is shown in Figure and the description are as follows: It consists of five functional blocks:

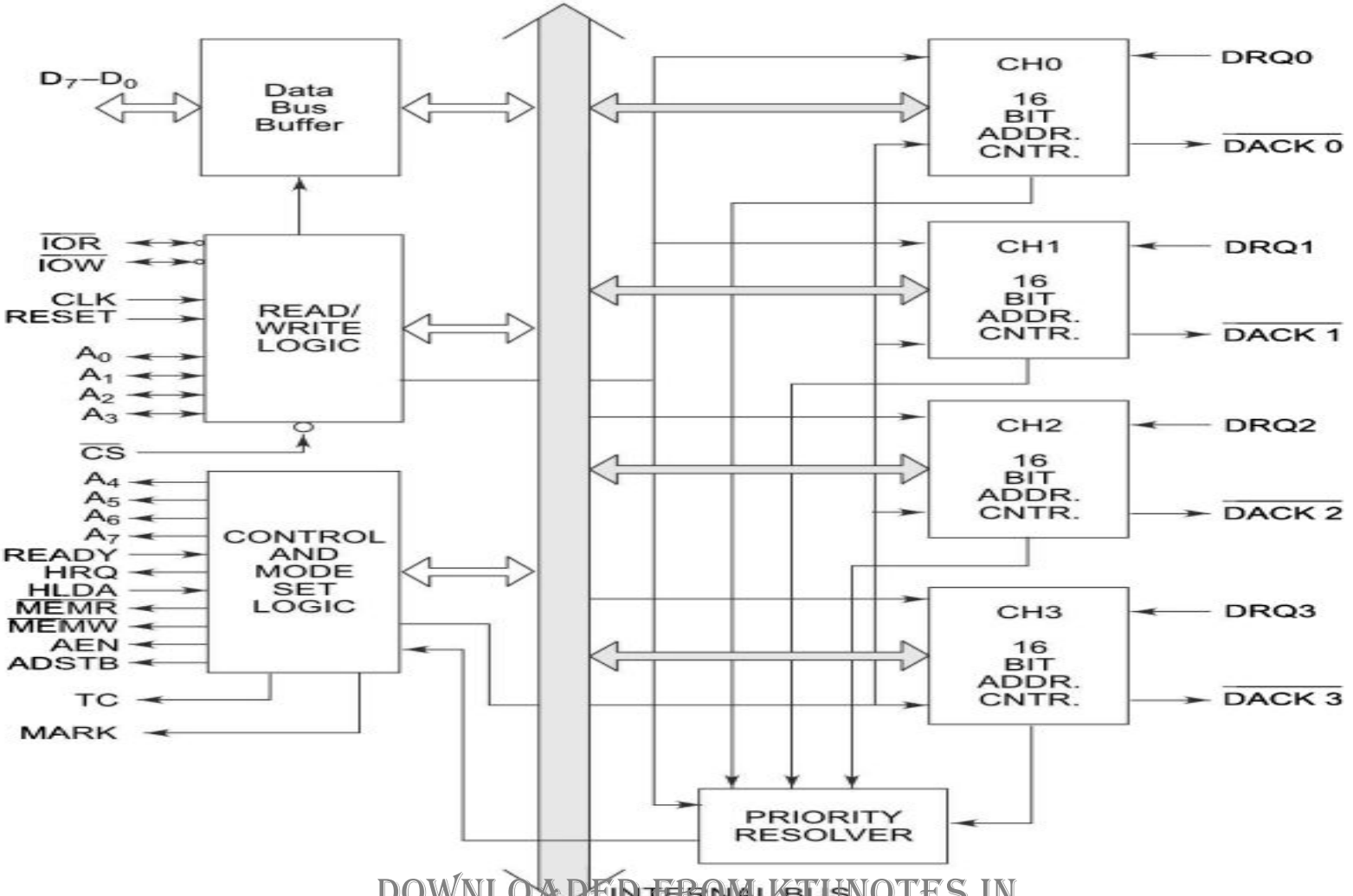
a) Data bus buffer

b) Control logic

c) Read/write logic

d) Priority Resolver

e) DMA channels



Data Bus Buffer: 8-bit Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

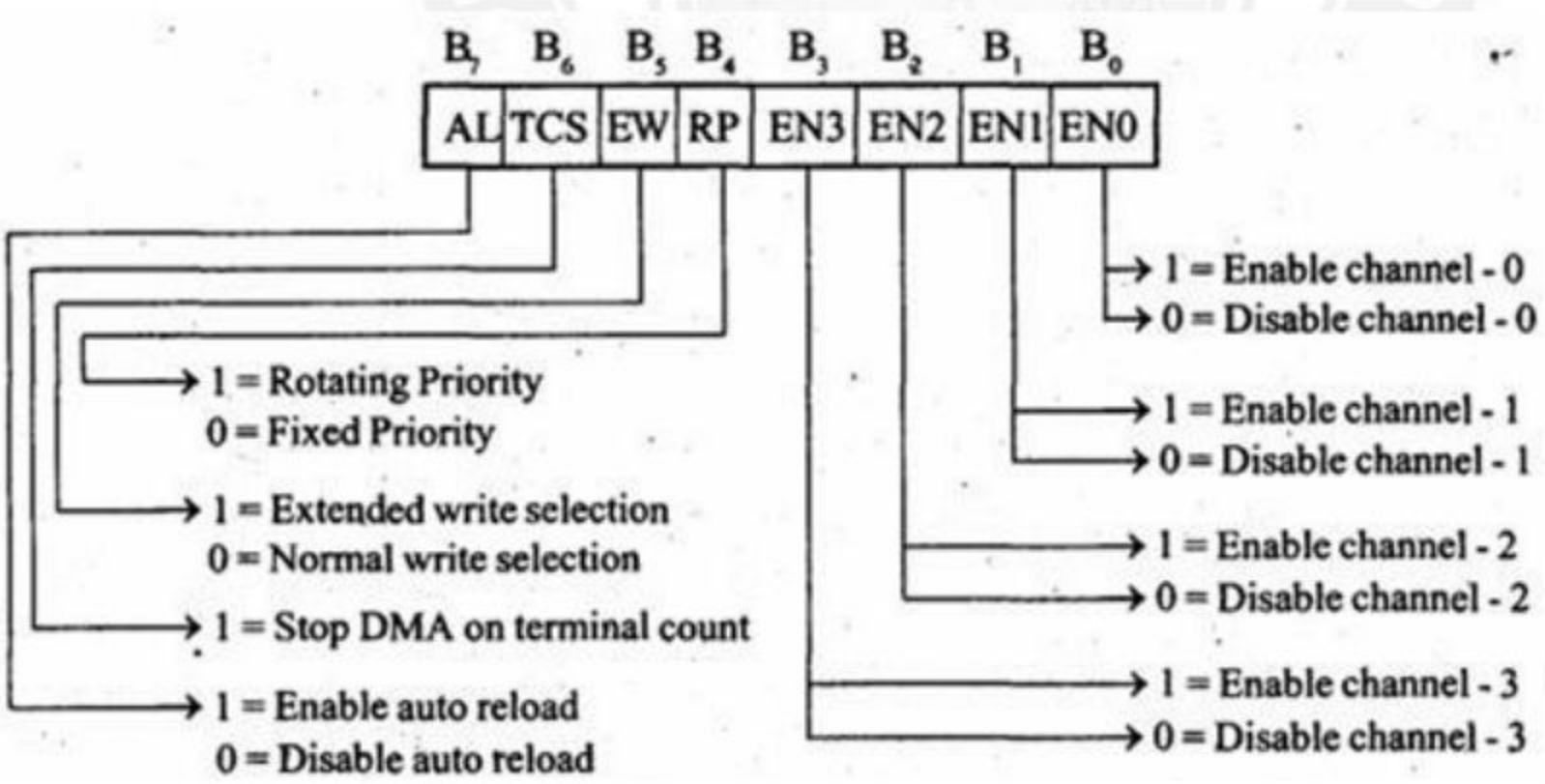
Read/Write Logic: In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the Ao-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the selected register depending upon whether IOW or IOR signal is activated.In master mode, the read/write logic generates the IOR and IOW signals to control the dataflow to or from the selected peripheral.

Read/Write Logic: In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the Ao-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the selected register depending upon whether IOW or IOR signal is activated.In master mode, the read/write logic generates the IOR and IOW signals to control the dataflow to or from the selected peripheral.

Priority Resolver: The priority resolver resolves the priority of the four DMA channels depending upon whether **normal priority or rotating priority** is programmed.

Register Organisation of 8257: The 8257 performs DMA operation over four independent DMA channels with the following Registers.

1. **DMA Address Register** Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel.
2. **Terminal Count Registers** Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.
3. **Mode Set Register** The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation as shown in Figure.



4. **Status register** The lower order 4-bits of this register contain the terminal count status for the four individual channels.If any of these bits is set, it indicates that the specific channel has reached the terminal count condition. Update flag is used in auto-reload mode. The update flag is set every time, the channel 2 registers are loaded with contents of the channel 3 registers in auto-reload.