ELECTRONIC
DEVICES
& CIRCUITS
second edition

David A. Bell

http://keralatechnologicaluniversity.blogspot.com

Electronic Devices
and Circuits

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2nd Edition

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to my wife Evelyn

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Preface

This is the second edition of *Fundamentals of Electronic Devices*, now renamed *Electronic Devices and Circuits* to more correctly describe the contents of the book. As in the first edition, my objectives are to clearly explain the operation of all important electronic devices in general use today and to give the reader a thorough understanding of the characteristics, parameters, and circuit applications of each device. In addition, I attempt to show a basic approach to designing each device into practical circuits.

The book is intended for use in electronics technology courses, whether two-, three-, or four-year courses. It should also prove useful as a reference handbook for practicing technicians, technologists, and engineers.

The text commences with the study of basic semiconductor theory and *pn*-junction theory which is essential for an understanding of all solid-state devices. Each different device is then treated in appropriate depth, beginning, of course, with the semiconductor diode, then the bipolar transistor. Transistor bias circuits, single-stage amplifiers, multistage amplifiers, and oscillator circuits are all covered. Discrete component circuit coverage and

integrated circuit applications are combined. The integrated circuit operational amplifier and its basic applications are explained in the chapters on multistage amplifiers and oscillators.

Although useful background information for each device is included in the book, every effort has been made to eliminate unnecessary material. For example, transistor and integrated circuit fabrication techniques are covered only from the point of view of how device performance is affected.

As well as bipolar transistors and integrated circuits, other devices covered include: Zener diode, JFET, MOSFET, VMOS FET, tunnel diode, SCR, UJT, PUT, photoconductive cell, solar cell, phototransistor, LED, LCD, piezoelectric crystal, VVC diode, and thermistor. Since electron tubes are still in wide use in existing equipment, the final chapter covers its varied forms: vacuum diode, triode, tetrode, pentode, and, of course, the very important cathode-ray tube.

Throughout the book many examples are employed to explain practical applications of each device. Instead of rigorous analysis methods, practical approximations are used wherever possible, and the origin of each approximation is explained. Manufacturers' data sheets are referred to where appropriate. Problems are provided at each chapter end, and answers to all problems are found in the back of the book. Glossaries of important terms are also included at the end of each chapter.

The mathematics level throughout the text does not go beyond algebraic equations and logarithms, simply because no higher math is necessary to fulfill the purpose of the book. It is expected that students will have already studied basic electricity.

DAVID A. BELL

Basic
Semiconductor
Theory

The function of an *electronic device* is to control the movement of *electrons*. The first step in a study of such devices is to understand the electron (or what it is believed to be), and how it is associated with the other components of the atom. After such an understanding is reached the bonding forces holding atoms together within a solid and the movement of electrons from one atom to another must be investigated. This leads to an understanding of the differences between *conductors*, *insulators*, and *semiconductors*.

1-1
Introduction

The atom is believed to consist of a central *nucleus* surrounded by orbiting *electrons* (see Fig. 1-1). Thus, it may be compared to a planet with satellites in orbit around it. Just as satellites are held in orbit by an attractive force of gravity due to the mass of the planet, so each electron is held in orbit by an *electrostatic* force of attraction between it and the nucleus.

1-2
The Atom

The electrons each have a negative electrical charge of 1.602×10^{-19} *coulombs* (C), and some particles within the nucleus have a positive charge of the same magnitude. Since opposite charges attract, a force of attraction

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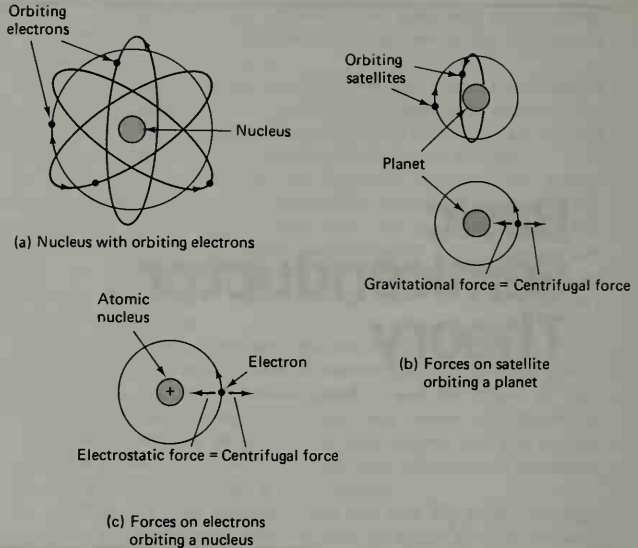
Figure 1-1. Planetary atom.

exists between the oppositely charged electron and nucleus. As in the case of the satellites, the force of attraction is balanced by the centrifugal force due to the motion of the electrons around the nucleus [Fig. 1-1(b) and (c)].

Compared to the mass of the nucleus, electrons are relatively tiny particles of almost negligible mass. In fact, we may think of them simply as little particles of negative electricity having no mass at all.

The nucleus of an atom is largely a cluster of two types of particles, *protons* and *neutrons*. Protons have a positive electrical charge, equal in magnitude (but opposite in polarity) to the negative charge on an electron. A neutron has no charge at all. Protons and neutrons each have masses about 1800 times the mass of an electron. For a given atom, the number of protons in the nucleus normally equals the number of orbiting electrons.

Since the protons and orbital electrons are equal in number and equal and opposite in charge, they neutralize each other electrically. For this reason, all atoms are normally electrically neutral. If an atom loses an electron, it has lost some negative charge. Therefore, it becomes positively charged and is referred to as a *positive ion*. Similarly, if an atom gains an additional electron, it becomes *negatively* charged and is termed a *negative ion*.

The differences between atoms consist largely of dissimilar numbers and arrangements of the three basic types of particles. However, all electrons

are identical, as are all protons and all neutrons. An electron from one atom could replace an electron in any other atom. Different materials are made up of different types of atoms, or differing combinations of several types of atoms.

The number of protons (or electrons) in an atom is referred to as the *atomic number* of the atom. The *atomic weight* is approximately equal to the total number of protons and neutrons in the nucleus of the atom. The atom of the semiconductor element *silicon* has 14 protons and 14 neutrons in its nucleus, as well as 14 orbital electrons. Therefore, the atomic number for silicon is 14, and its atomic weight is approximately 28.

Atoms may be conveniently represented by the two-dimensional diagrams shown in Fig. 1-2. It has been found that electrons can occupy only certain orbital rings or *shells* at fixed distances from the nucleus, and that each shell can contain only a particular number of electrons. The electrons in the outer shell determine the electrical (and chemical) characteristics of each particular type of atom. These electrons are usually referred to as *valence electrons*. An atom may have its outer or *valence shell* completely filled or only partially filled.

The atoms of two important semiconductors, *silicon* (Si) and *germanium* (Ge), are illustrated in Fig. 1-2. It is seen that each of these atoms have four electrons in a valence shell that can contain a maximum of eight. Thus, we say that their valence shells have four electrons and four *holes*. A *hole* is defined simply as an absence of an electron in a shell where one could exist. Even though their valence shells have four holes, both silicon and germanium atoms are still electrically neutral, because the total number of orbital electrons equals the total number of protons in the nucleus.

(a) Germanium atom   (b) Silicon atom
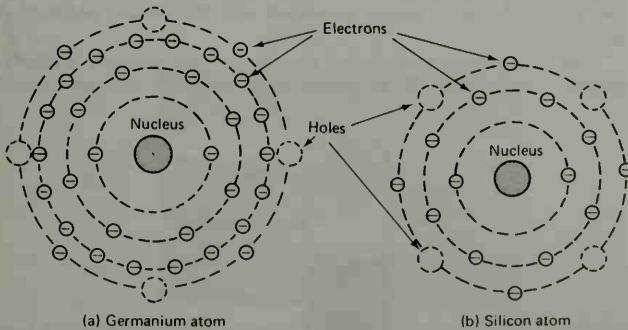
Figure 1-2. Two-dimensional representation of silicon and germanium atoms.

The closer an electron is to the nucleus, the stronger are the forces that bind it. Each shell has an *energy level* associated with it which represents the amount of energy that would have to be supplied to extract an electron from the shell. Since the electrons in the valence shell are farthest from the nucleus, they require the least amount of energy to extract them from the atom. Conversely, those electrons closest to the nucleus require the greatest energy application to extract them from the atom.

The energy levels considered above are measured in *electron volts* (eV). An *electron volt* is defined as the amount of energy required to move one electron through a potential difference of one volt.

1-4
Energy Bands

So far the discussion has concerned a system of electrons around one isolated atom. The electrons of an isolated atom are acted upon only by the forces within that atom. However, when atoms are brought closer together as in a solid, the electrons come under the influence of forces from other atoms. The energy levels that may be occupied by electrons merge into bands of energy levels. Within any given material there are two distinct *energy bands* in which electrons may exist, the *valence band* and the *conduction band*. Separating these two bands is an *energy gap* in which no electrons can normally exist. This gap is termed the *forbidden gap*. The valence band, conduction band, and forbidden gap are shown diagrammatically in Fig. 1-3.

Electrons within the conduction band have become disconnected from atoms and are drifting around within the material. Conduction band electrons may be easily moved around by the application of relatively small amounts of energy. Much larger amounts of energy must be applied to extract an electron from the valence band or to move it around within the valence band. Electrons in the valence band are usually in normal orbit around a nucleus. For any given type of material, the forbidden gap may be large, small, or nonexistent. The distinction between conductors, insulators, and semiconductors is largely concerned with the relative widths of the forbidden gap.

It is important to note that the energy band diagram is simply a graphic representation of the energy levels associated with electrons. To
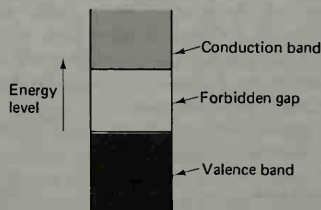
Figure 1-3. Energy band diagram.

repeat, those electrons in the valence band are actually in orbit around the nucleus of an atom; those in the conduction band are drifting about in the spaces between atoms.

Conduction occurs in any given material when an applied voltage causes electrons within the material to move in a desired direction. This may be due to one or both of two processes, *electron motion* and *hole transfer*. In electron motion, *free electrons* in the conduction band are moved under the influence of the applied electric field. Since electrons have a negative charge, they are repelled from the negative terminal of the applied voltage, and attracted toward the positive terminal. Hole transfer involves electrons which are still attached to atoms, i.e., those in the valence band.

If some of the energy levels in the valence band are not occupied by electrons, there are holes where electrons could exist. An electron may jump from one atom to fill the hole in another atom. When it jumps, the electron leaves a hole behind it, and we say that the hole has moved in the opposite direction to the electron. In this way a current flows which may be said to be due to hole movement.

In Fig. 1-4(a), the applied potential causes an electron to jump from atom y to atom x. In doing so, it fills the hole in the valence shell of atom x, and leaves a hole behind it in atom y as shown in Fig. 1-4(b). If an electron now jumps from atom z, under the influence of the applied potential, and fills the hole in the valence shell of atom y, it leaves a hole in atom z [Fig. 1-4(c)]. Thus, the hole has been caused to move from atom x to atom y to atom z.

Holes may be thought of as positive particles, and as such they move through an electric field in a direction opposite to that of the electrons; i.e.,
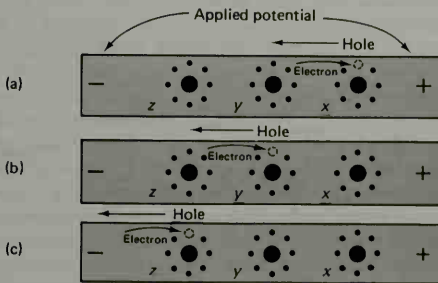
Figure 1-4. Conduction by hole transfer. (a) Electron jumps from atom y to atom x. (b) It fills the hole in atom x and leaves a hole in atom y. (c) If an electron jumps from atom z to atom y, it will leave a hole in atom z.

positive particles are attracted toward the negative terminal of an applied voltage. It is usually more convenient to think in terms of hole movement, rather than in terms of electrons jumping from atom to atom.

Since the flow of electric current is constituted by the movement of electrons in the conduction band and holes in the valence band, electrons and holes are referred to as *charge carriers*. Each time a hole moves, an electron must be supplied with sufficient energy to enable it to escape from its atom. Free electrons require less application of energy than holes to move them, because they are already disconnected from their atoms. For this reason, electrons have *greater mobility* than holes.

The unit of electric current is the *ampere* (A). An ampere may be defined as that current which flows when one coulomb of charge passes a given point in one second. From this definition we can calculate the number of electrons involved in a current of one ampere. Since the charge on one electron is 1.602×10^{-19} C, the number of electrons with a total charge of 1 C is $1/(1.602 \times 10^{-19}) \approx 6.25 \times 10^{18}$. When one microampere ($\mu A$) flows (i.e., 1×10^{-6} A), electrons are passing at the rate of 6.25×10^{12} per second, or $1\ \mu A = 6,250,000,000,000$ electrons per second.

1-6
Conventional Current and Electron Flow

In the early days of electrical experimentation it was believed that a positive charge represented an increased amount of electricity and that a negative charge was a reduced quantity. Thus, it was assumed that current flowed from positive to negative. This is a convention that remains in use today even though current is now known to be a movement of electrons from negative to positive (see Fig. 1-5).
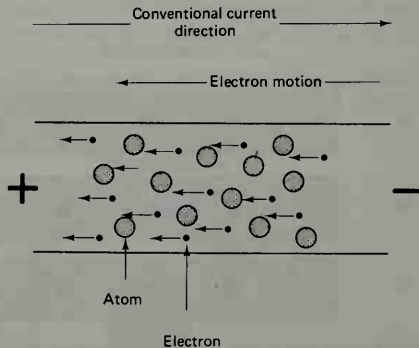
Figure 1-5. Conventional current direction is from positive to negative. Electron flow is from negative to positive.

Current flow from positive to negative is referred to as the conventional direction of current. *Electron flow from negative to positive is known as the* direction of electron flow.

It is important to understand both conventional current direction and electron flow. Every graphic symbol used to represent an electronic device has an arrowhead which indicates conventional current direction. A consequence of this is that electronic circuits are most easily explained by using current flow from positive to negative. However, to understand how each device operates, it is necessary to think in terms of electron movement.

Whether a material is a conductor, a semiconductor, or an insulator depends largely upon what happens to the outer-shell electrons when the atoms bond themselves together to form a solid. In the case of copper, the easily detached valence electrons are given up by the atoms. This creates a great mass of free electrons (or *electron gas*) drifting about through the spaces between the copper atoms. Since each atom has lost a (negative) electron, it becomes a *positive ion*. The electron gas is, of course, negatively charged; consequently, an electrostatic force of attraction exists between the positive ions and the electron gas. This is the *bonding force* that holds the material together in a solid. In the case of copper and other metals, the bonding force is termed *metallic bonding* or sometimes *electron gas bonding*. This type of bonding is illustrated in Fig. 1-6(a).

In the case of silicon, which has four outer-shell electrons and four holes, the bonding arrangement is a little more complicated than for copper. Atoms in a solid piece of silicon are so close to each other that the outer-shell electrons behave as if they were orbiting in the valence shells of two atoms. In this way each valence-shell electron fills one of the holes in the valence shell of a neighboring atom. This arrangement, illustrated in Fig. 1-6(b), forms a bonding force known as *covalent bonding*. In covalent bonding every valence shell of every atom appears to be filled, and consequently there are no holes and no free electrons drifting about within the material. The same is true for germanium atoms. When semiconductor material is prepared for device manufacture, the atoms within the material are aligned into a definite three-dimensional pattern or *crystal lattice*. Each atom is covalently bonded to the four surrounding atoms.

In some insulating materials, notably rubber and plastics, the bonding process is also covalent. The valence electrons in these bonds are very strongly attached to their atoms, so the possibility of current flow is virtually zero. In other types of insulating materials, some atoms have parted with outer-shell electrons, but these have been accepted into the orbit of other atoms. Thus, the atoms are *ionized*; those which gave up electrons have become *positive ions*, and those which accepted the electrons become *negative ions*. This creates an electrostatic bonding force between the atoms, termed *ionic bonding*. The situation is illustrated in Fig. 1-6(c), which shows how the negative and positive ions may be arranged together in groups.

Positive ions

Free electrons

(a) Metallic bonding

Shared valence electrons

(b) Covalent bonding

Positive ion

Negative ion
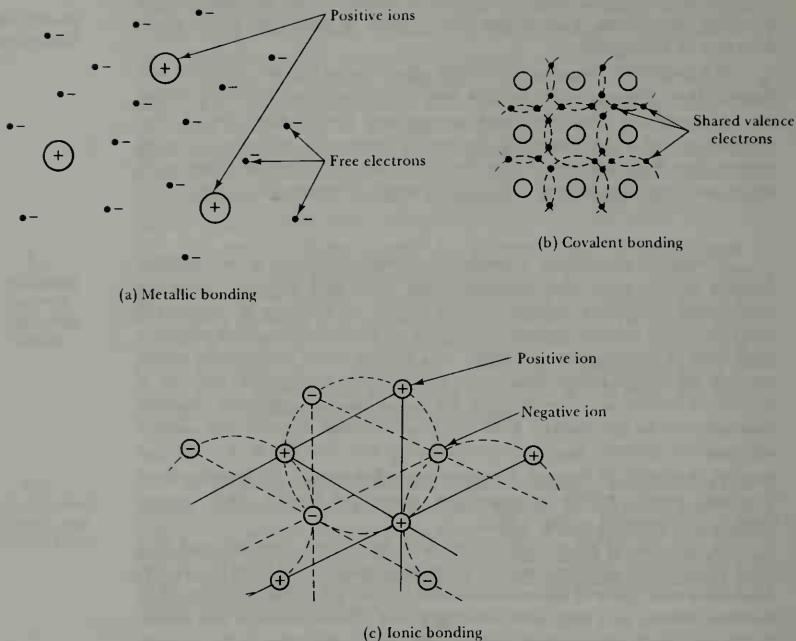
(c) Ionic bonding

Figure 1-6. Atomic bonding in conductors, semiconductors, and insulators.

1-8
Conductors,
Insulators,
and
Semi-
conductors

As seen in the energy band diagrams of Fig. 1-7, *insulators* have a wide forbidden gap, *semiconductors* have a narrow forbidden gap, and *conductors* have no forbidden gap at all. In the case of insulators, there are practically no electrons in the conduction band of energy levels, and the valence band is filled. Also, the forbidden gap is so wide [Fig. 1-7(a)] that it would require the application of very large amounts of energy (approximately 6 eV) to cause an electron to cross from the valence band to the conduction band. Therefore, when a voltage is applied to an insulator, conduction cannot occur either by electron motion or hole transfer.

For semiconductors at a temperature of absolute zero ($-273.15°C$) the valence band is usually full, and there may be no electrons in the conduction band. However, as shown in Fig. 1-7(b), the semiconductor forbidden gap is very much narrower than that of an insulator, and the application of small amounts of energy (1.2 eV for silicon and 0.785 eV for germanium) can raise electrons from the valence band to the conduction band. Sufficient thermal

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(a) Insulator   (b) Semiconductor   (c) Conductor
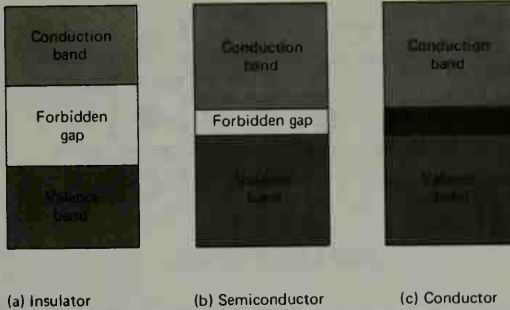
Figure 1-7. Energy band diagrams for insulator, semiconductor, and conductor.

energy for this purpose is made available when the semiconductor is at room
temperature. If a potential is applied to the semiconductor, conduction
occurs both by electron movement in the conduction band and by hole
transfer in the valence band.

In the case of conductors [Fig. 1-7(c)] there is no forbidden gap, and
the valence and conduction energy bands overlap. For this reason, very large
numbers of electrons are available for conduction, even at extremely low
temperatures.

Typical resistance values for a 1-cubic-centimeter sample are

Conductor	$10^{-6} \, \Omega/cm^3$
Semiconductor	$10 \, \Omega/cm^3$
Insulator	$10^{14} \, \Omega/cm^3$

Pure semiconductor material is referred to as *intrinsic* material. Before
semiconductor material can be used for device manufacture, impurity atoms
must be added to it. This process is called *doping*, and it improves the
conductivity of the material very significantly. Doped semiconductor
material is termed *extrinsic* material. Two different types of doping are
possible, *donor* doping and *acceptor* doping. *Donor* doping generates free
electrons in the conduction band (i.e., electrons that are not tied to an
atom). *Acceptor* doping produces valence band holes, or a shortage of valence
electrons in the material.

Donor doping is effected by adding impurity atoms which have five
electrons and three holes in their valence shells. The impurity atoms form
covalent bonds with the silicon or germanium atoms; but since semiconduc-
tor atoms have only four electrons and four holes in their valence shells, one

1-9
Semi-
conductor
Doping

9
Semiconductor
Doping

Fifth valence electron
from impurity atom
becomes free electron
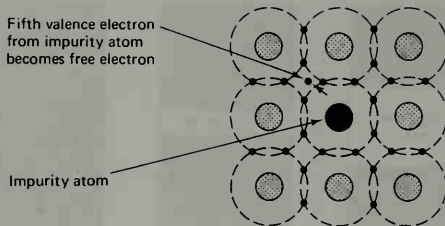
Impurity atom

Figure 1-8. Donor doping.

spare valence-shell electron is produced for each impurity atom added. Each spare electron produced in this way enters the conduction band as a free electron. In Fig. 1-8 there is no hole for the fifth electron from the outer shell of the impurity atom; therefore, it becomes a free electron. Since the free electrons have negative charges, donor-doped material is known as *n-type* semiconductor material.

Free electrons in the conduction band are easily moved around under the influence of an electric field. Therefore, conduction occurs largely by electron motion in donor-doped semiconductor material. The doped material remains electrically neutral (i.e., it is neither positively nor negatively charged), because the total number of electrons (including the free electrons) is still equal to the total number of protons in the atomic nuclei. (The number of protons in each impurity atom is equal to the number of orbital electrons.) The term *donor doping* comes from the fact that an electron is donated to the conduction band by each impurity atom. Typical donor impurities are *antimony*, *phosphorus*, and *arsenic*. Since these atoms have five valence electrons, they are referred to as *pentavalent* atoms.

In *acceptor doping*, impurity atoms are added with outer shells containing three electrons and five holes. Suitable atoms with three valence electrons (which are called *trivalent*) are *boron*, *aluminum*, and *gallium*. These atoms form bonds with the semiconductor atoms, but the bonds lack one electron for a complete outer shell of eight. In Fig. 1-9 the impurity atom illustrated has only three valence electrons; therefore, a hole exists in its bond with the surrounding atoms. Thus, in acceptor doping *holes* are introduced into the valence band, so that conduction may occur by the process of hole transfer.

Since holes can be said to have a *positive* charge, acceptor-doped semiconductor material is referred to as *p-type* material. As with *n*-type material, the material remains electrically neutral, because the total number of orbital electrons in each impurity atom is equal to the total number of protons in its atomic nucleus. Holes can *accept* a free electron, hence the term *acceptor* doping.

Even in *intrinsic* (undoped) semiconductor material at room temperature there are a number of free electrons and holes. These are due to
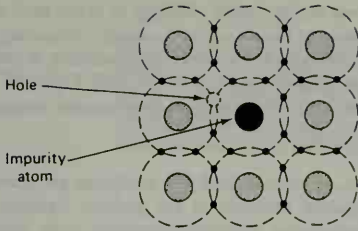
Figure 1-9. Acceptor doping.

thermal energy causing some electrons to break the bonds with their atoms and enter the conduction band, so creating pairs of holes and electrons. The process is termed *hole–electron pair generation*, and its converse is a process called *recombination*. As the name implies, recombination occurs when an electron falls into a hole in the valence band. Since there are many more electrons than holes in *n*-type material, *electrons* are said to be the *majority carriers*, and holes are said to be *minority carriers*. In *p*-type material holes are the *majority carriers* and electrons are *minority carriers*.

When a conductor is heated, the atoms (which are in fixed locations) tend to vibrate, and the vibration impedes the movement of the surrounding electron gas. This means that there is a reduction in the flow of the electrons that constitute the electric current, and we say that the conductor resistance has increased. A conductor has a positive temperature coefficient of resistance, i.e., a resistance which increases with increase in temperature.

When semiconductor material is at absolute zero, there are practically no free electrons in the conduction band and no holes in the valence band. This is because all electrons are in normal orbit around the atoms. Thus, at absolute zero, a semiconductor behaves as an insulator. When the material is heated, electrons break away from their atoms and move from the valence band to the conduction band. This produces holes in the valence band and free electrons in the conduction band. Conduction can then occur by electron movement and by hole transfer. Increasing application of thermal energy generates an increasing number of hole–electron pairs. As in the case of a conductor, thermal vibration of atoms occurs in a semiconductor. However, there are very few electrons to be impeded compared to the dense electron gas in a conductor. The thermal generation of electrons is the dominating factor, and the current increases with temperature increase. This represents a decrease in semiconductor resistance with temperature increase, i.e., a *negative temperature coefficient*. An exception to this rule is heavily doped semiconductor material, which may behave more like a conductor than a semiconductor.

1-10
Effects of
Heat and
Light

Just as thermal energy causes electrons to break their atomic bonds, so hole–electron pairs may be generated by energy imparted to the semiconductor in the form of light. If the material is intrinsic, it may have few free electrons when not illuminated, and thus a very high *dark resistance*. When illuminated, its resistance decreases and may become comparable to that of a conductor.

1-11
Drift Current
and
Diffusion
Current

In free space, an electric field will accelerate an electron in a straight line from the negative terminal to the positive terminal of the applied voltage. In a conductor or a semiconductor at room temperature, a free electron under the influence of an electric field will move toward the positive terminal of the applied voltage, but it will continually collide with atoms along the way. The situation is illustrated in Fig. 1-10. Each time the electron strikes an atom, it rebounds in a random direction. The presence of the electric field does not stop the collisions and random motion, but it does cause the electron to drift in the direction of the applied electric force. Current produced in this way is known as *drift current*, and it is the usual kind of current flow that occurs in a conductor.

Figure 1-11 illustrates another kind of current. Suppose a concentration of one type of charge carriers occurs at one end of a piece of semiconductor material. Since the charge carriers are either all electrons or all holes, they have the same polarity of charge, and thus there is a force of repulsion between them. The result is that there is a tendency for the charge carriers to move gradually (or diffuse) from the region of high carrier density to one of low density. This movement continues until all the carriers are evenly distributed throughout the material. Any movement of charge carriers constitutes an electric current, and this type of movement is known as *diffusion current*. Both *drift current* and *diffusion current* occur in semiconductor devices.
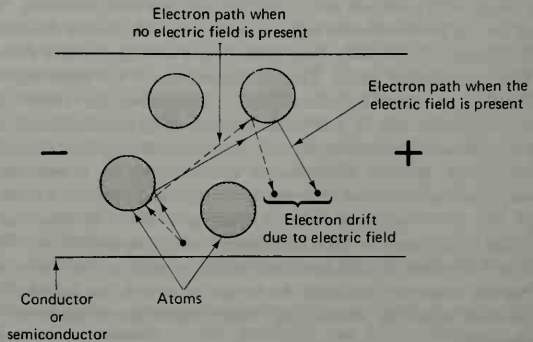
Figure 1-10.   Drift current.
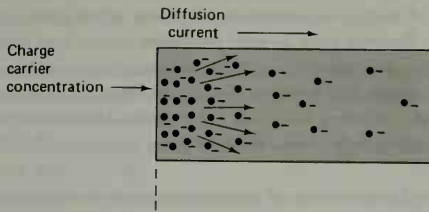
Figure 1-11. Diffusion current.

Nucleus. Central portion or core of the atom.

Electron. Very small negatively charged particle.

Electronic charge. 1.602×10^{-19} C.

Proton. Positively charged particle contained in the nucleus of an atom.

Neutron. Particle with no electrical charge, contained in the nucleus of an atom.

Shell. Path of electron orbiting around nucleus.

Atomic weight. Approximately the total number of protons and neutrons in the nucleus of an atom.

Atomic number. The number of protons or orbiting electrons in an atom.

Positive ion. Atom that has lost an electron.

Negative ion. Atom that has gained an electron.

Germanium atom. Atom of semiconductor material, has four electrons and four holes in its outer shell.

Silicon atom. Atom of semiconductor material, has four electrons and four holes in its outer shell.

Hole. Absence of an electron where one could exist.

Energy level of shell. Amount of energy required to extract a particular electron from its atomic shell.

Electron volt (eV). Energy required to move one electron through a potential difference of one volt.

Energy band. Group of energy levels that may be occupied by electrons.

Conduction band. Energy band of electrons that have escaped from atomic orbits.

Valence band. Energy band of electrons that are in normal atomic orbits.

Forbidden gap. Energy band at which electrons normally do not exist.

Charge carrier. Electron or hole.

Mobility. Ease (or difficulty) with which a charge carrier may be moved around.

Conventional current direction. Current flow from positive to negative.

Electron flow direction. Electron motion from negative to positive.

Ionic bond. Electrostatic attraction when one atom gives an electron to another. Bonding force in some insulators.

Metallic bond. Electrostatic attraction between large numbers of electrons and the atoms that have released them. Bonding force in conductors.

Covalent bond. Bonding force that binds atoms which share electrons and holes in their outer shells. Bonding force in semiconductors and some insulators.

Electron gas. Large number of electrons available for current carrying in a conductor.

Doping. Addition of impurity atoms to change electrical characteristics of semiconductor material.

Donor atoms. Impurity atoms which release additional electrons within semiconductor material.

Acceptor atoms. Impurity atoms which release additional holes within semiconductor material.

p-type semiconductor. Semiconductor that has been doped with acceptor atoms.

n-type semiconductor. Semiconductor that has been doped with donor atoms.

Intrinsic. Name given to undoped semiconductor, or to material doped equally with both types of impurities.

Extrinsic. Name given to doped semiconductor material.

Majority carriers. Type of charge carriers which are in the majority in a given material (electrons in n-type, holes in p-type).

Drift current. Electrons moving randomly from one atom to another being made to drift in a desired direction under the influence of an electric field.

Diffusion current. Charge carrier movement resulting from an initial concentration of charge carriers.

Minority carriers. Type of charge carriers which are in the minority in a given material (holes in n-type, electrons in p-type).

Temperature coefficient. Ratio of resistance change to temperature change.

Dark resistance. Resistance of unilluminated semiconductor.

Crystal lattice. Three-dimensional pattern in which atoms align themselves in a solid.

Hole–electron pair. A valence-band hole and a conduction-band electron produced by energy causing the breaking of atomic bonds.

Recombination. Holes and electrons recombining, i.e., the conduction-band electron fills the valence-band hole.

1-1. Describe the atom and draw a two-dimensional diagram to illustrate your description. Compare the atom to a planet with orbiting satellites.

1-2. What is meant by *atomic number* and *atomic weight*? State the atomic number and atomic weight for silicon.

1-3. Name the three kinds of bonds that hold atoms together in a solid. What kind of bonding might be found in (a) conductors, (b) insulators, (c) semiconductors?

1-4. Explain the bonding process in silicon and germanium. Use illustrations in your answer.

1-5. Draw sketches to show the bonding process in conductors and insulators.

1-6. What is meant by energy levels and energy bands?

1-7. Define *conduction band*, *valence band*, and *forbidden gap* and explain their origin.

1-8. Draw the band structure for, and explain the difference between, conductors, insulators, and semiconductors.

1-9. Define *intrinsic* semiconductors and *extrinsic* semiconductors. How can extrinsic material be made intrinsic?

1-10. What is meant by *majority carriers* and *minority carriers*? Which are majority carriers and why in (a) donor-doped material, (b) acceptor-doped material?

1-11. Define acceptor doping and explain how it is effected. Use illustrations in your answer.

1-12. Repeat Question 1-11 for donor doping.

1-13. What are the names given to acceptor-doped material and donor-doped material? Explain why.

1-14. Draw a sketch to show the process of current flow by hole movement. Which have greater mobility, electrons or holes? Explain why.

1-15. Explain what happens to resistance with increase in temperature in the case of (a) a conductor, (b) a semiconductor, (c) a heavily doped semiconductor. What do you think would happen to the resistance of an insulator with increase in temperature? Why?

1-16. Explain *diffusion current* and *drift current*. Use illustrations in your answer.

1-17. Explain *conventional current direction* and direction of *electron motion*. State why each is important.

pN –
Junction
Theory

2-1
Introduction

The *pn*-junction is basic to all but a few semiconductor devices. Thus, it is important that the electronics student gain a thorough understanding of *pn*-junction theory. This requires an appreciation of the forces that act upon charge carriers crossing the junction, and an understanding of the effects of externally applied bias voltages. A knowledge of the junction equivalent circuits is also important.

2-2
The
pn-Junction

Figure 2-1 represents a *pn*-junction formed by two blocks of semiconductor material, one of *p*-type material and the other of *n*-type material. On the *p*-side the small broken circles represent holes, which are the majority carriers in the *p*-type material. The dots on the *n*-side represent free electrons within the *n*-type material. The holes on the *p*-side are fixed in position because the atoms in which they exist are part of the crystal structure. Normally they are uniformly distributed throughout the *p*-type material. Similarly, the electrons on the *n*-side are uniformly distributed throughout the *n*-type material.
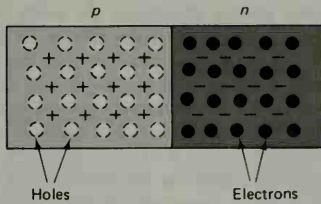
Figure 2-1. Initial condition of charge carriers at pn-junction.

Because holes and electrons are close together at the junction, some free electrons from the n-side are attracted across the junction and fill holes on the p-side. They are said to *diffuse* across the junction, i.e., flow from a region of high carrier concentration to one of lower concentration (see Section 1-11). The free electrons crossing the junction create negative ions on the p-side by giving some atoms one more electron than their total number of protons. They also leave positive ions behind them on the n-side (atoms with one less electron than the number of protons). The process is illustrated in Fig. 2-2(a).

Before the charge carriers diffused across the junction, both the n-type and the p-type material were electrically neutral. However, as negative ions are created on the p-side of the junction, the region of the p-side close to the junction acquires a negative charge. Similarly, the positive ions created on the n-side give the n-side a positive charge. The accumulated negative charge on the p-side tends to repel electrons that are crossing from the n-side,

(a) Diffusion of charge carriers across pn-junction.

Holes cross (create negative ion)

Electrons cross (leave positive ion)

Positive potential due to positive ions

(b) Junction barrier potential and electric field.

Negative potential due to negative ions

Repels holes

Repels electrons

Electric field at junction
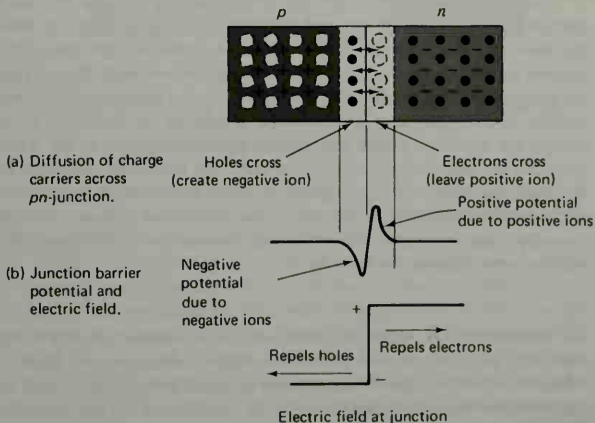
Figure 2-2. Charge carrier diffusion across junction, and junction barrier potential.

and the accumulated positive charge on the *n*-side tends to repel holes crossing from the *p*-side. Thus, it becomes difficult for more charge carriers to diffuse across the junction. The final result is that a *barrier potential* is created at the junction, negative on the *p*-side and positive on the *n*-side [Fig. 2-2(b)]. The electric field produced by the barrier potential is large enough to prevent any further movement of electrons and holes across the junction.

By considering doping densities, electronic charge, and temperature, it is possible to calculate the magnitude of the barrier potential. Typical barrier potentials at room temperature are 0.3 V for germanium junctions and 0.7 V for silicon.

The movement of charge carriers across the junction leaves a layer on either side which is depleted of charge carriers. This is the *depletion region* shown in Fig. 2-3(a). On the *n*-side, the depletion region consists of donor impurity atoms which have lost the free electron associated with them, and have thus become positively charged. On the *p*-side, the region is made up of acceptor impurity atoms which have become negatively charged by losing the hole associated with them (i.e., the hole is filled by an electron).

On each side of the junction, an equal number of impurity atoms are involved in the depletion region. If the two blocks of material have equal doping densities, the depletion layers on each side of the junction are equal in thickness [Fig. 2-3(a)]. If the *p*-side is more heavily doped than the *n*-side, as shown in Fig. 2-3(b), the depletion region penetrates more deeply into the *n*-side in order to include an equal number of impurity atoms on each side of the junction. Conversely, if the *n*-side is the most heavily doped, the depletion region penetrates deeper into the *p*-type material.

It has been shown that the electric field produced by the barrier potential at the junction opposes the flow of electrons from the *n*-side and the flow of holes from the *p*-side. Since electrons are the majority charge carriers in the *n*-type material, and holes are the majority charge carriers in the *p*-type material, it can be seen that the barrier potential *opposes the flow of majority carriers*. Also, any free electrons generated on the *p*-side by thermal energy are attracted across the positive potential barrier to the *n*-side since electrons are negatively charged. Similarly, the thermally generated holes on the *n*-side are attracted to the *p*-side through the negative barrier presented to them at the junction. Electrons on the *p*-side and holes on the *n*-side are minority charge carriers. Therefore, the barrier potential *assists the flow of minority carriers* across the junction.

To Summarize: A region depleted of charge carriers spreads across both sides of a *pn*-junction, and penetrates deeper into the more lightly doped side. The depletion region encompasses an equal number of ionized atoms of opposite polarity, on opposite sides of the junction. A barrier potential exists due to the depletion effect, positive on the *n*-side and negative on the *p*-side of the junction. The electric field from the barrier potential prevents the flow of majority carriers and assists the flow of minority carriers from each side.

(a) Equal doping densities

Depletion region

p

n

Equal number of ions on each side

Layer of negative ions (depleted of holes)

Layer of positive ions (depleted of electrons)

(b) Unequal doping densities

Depletion region (wide on n side)

Heavily doped

Lightly doped

p

n

Layer of negative ions

Equal number of ions on each side

Layer of positive ions
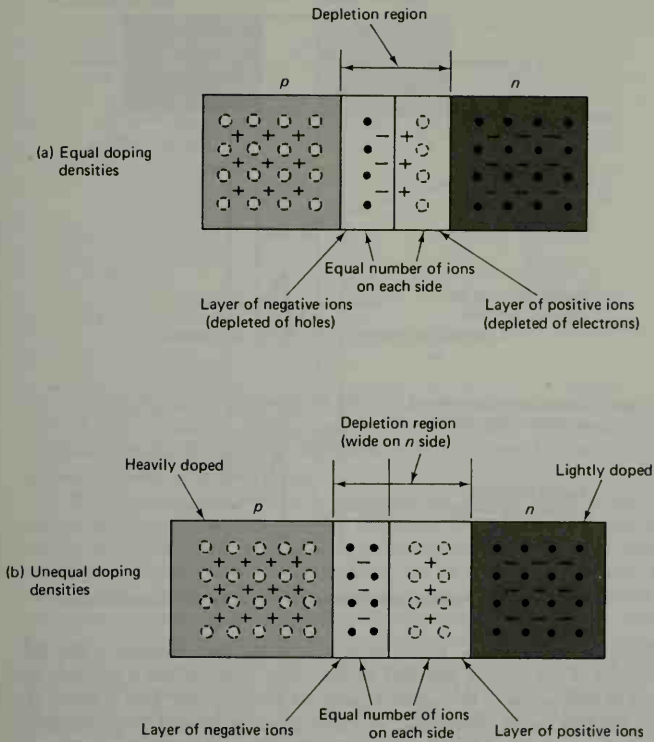
Figure 2-3. Junction depletion region.

If an external bias voltage is applied positive to the n-side and negative to the p-side of a pn-junction, electrons from the n-side are attracted to the positive bias terminal, and holes from the p-side are attracted to the negative terminal. Thus, as shown in Fig. 2-4, holes from the impurity atoms on the p-side of the junction are attracted away from the junction, and electrons are attracted away from the atoms on the n-side of the junction. In this way the depletion region is widened, and the barrier potential is increased by the magnitude of the applied voltage. With the barrier potential and the resultant electric field increase, there is no possibility of majority carrier current flow across the junction. In this case, the junction is said to be *reverse biased*.

Although there is no possibility of a majority carrier current flowing across a reverse-biased junction, minority carriers generated on each side can
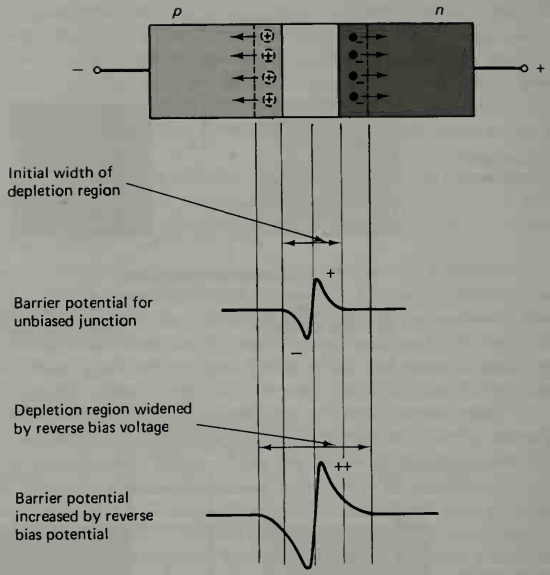
Figure 2-4. Barrier potential and depletion region at reverse-biased junction.

still cross the junction. Electrons in the *p*-side are attracted across the junction to the positive potential on the *n*-side. Holes on the *n*-side may be said to flow across to the negative potential on the *p*-side. This is shown by the junction *reverse characteristic*, or graph of *reverse current* (I_R) plotted to a base of *reverse voltage* (V_R) (Fig. 2-5). Only a very small reverse bias voltage is necessary to direct all available minority carriers across the junction, and when all minority carriers are flowing across, further increase in bias voltage will not increase the current. This current is referred to as a *reverse saturation current*, and is designated I_S.

I_S is normally a very small current. For silicon, it is typically less than 1 μA, while for germanium it may exceed 10 μA. This is because there are more minority charge carriers available in germanium than in silicon, since charge carriers are more easily detached from germanium atoms.

A reverse-biased *pn*-junction can be represented by a very large resistance. From Fig. 2-5, it is seen that with 5-V reverse bias and $I_S = 10$ μA, the *reverse resistance* is

$$R_R = \frac{5 \text{ V}}{10 \text{ }\mu\text{A}} = 500 \text{ } k\Omega$$
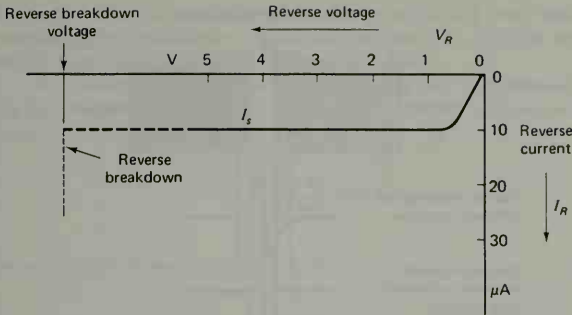
Figure 2-5. pn-junction reverse characteristics.

For a silicon junction with an I_S of about 0.1 μA and a reverse voltage of 5 V, R_R is 50 MΩ. In practice, the reverse resistance is normally not specified; instead, the effect of reverse saturation current I_S is taken into account for each particular circuit.

If the reverse bias voltage is increased, the velocity of the minority charge carriers crossing the junction is increased. These high-energy charge carriers strike the atoms within the depletion region and may cause large numbers of charge carriers to be knocked out of the atoms (*ionization by collision*). When this happens, the number of charge carriers *avalanches*, and a large current flows across the junction. This phenomenon, known as *reverse breakdown*, occurs at a particular reverse voltage (the *reverse breakdown voltage*) for a given pn-junction (see Fig. 2-5). Unless the current is limited by a suitable series resistor, the junction may be destroyed. Reverse breakdown is employed in a device known as a *breakdown diode*, discussed in Chapter 11.

Consider the effect of an external bias voltage applied with the polarity shown in Fig. 2-6: positive on the p-side, negative on the n-side. The holes on the p-side, being positively charged particles, are repelled from the positive bias terminal and driven toward the junction. Similarly, the electrons on the n-side are repelled from the negative bias terminal and driven toward the junction. The result is that the depletion region is reduced in width, and the barrier potential is also reduced. If the applied bias voltage is increased from zero, the barrier potential gets progressively smaller until it effectively disappears, and charge carriers can easily flow across the junction. Electrons from the n-side are then attracted across to the positive bias terminal on the p-side, and holes from the p-side flow across to the negative terminal on the n-side. Thus, a majority carrier current flows, and the junction is said to be *forward biased*.

**2-4
Forward-
Biased
Junction**

Narrowed depletion region
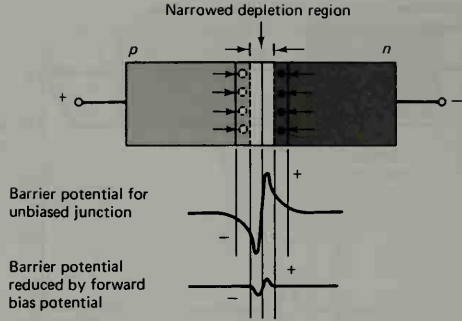
Figure 2-6. Barrier potential at forward-biased junction.

Figure 2-7 shows the forward current (I_F) plotted against forward voltage (V_F) for typical germanium and silcon *pn*-junctions. In each case, the graph is known as the *forward characteristic* of the (silicon or germanium) junction. It is seen that very little forward current flows until V_F exceeds the junction barrier potential (0.3 V for germanium, 0.7 V for silicon). The characteristics follow an exponential law. As V_F is increased to the *knee* of the characteristic, the barrier potential is progressively reduced to zero, allowing more and more majority charge carriers to flow across the junction. Beyond
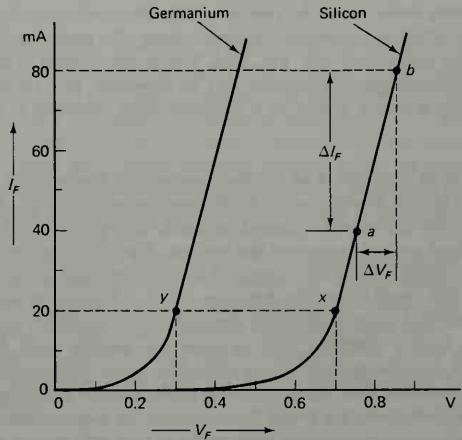
Figure 2-7. *pn*-junction forward characteristics.

the knee of the characteristic, the barrier potential has been completely overcome, I_F increases almost linearly with increase in V_F, and the combined semiconductor blocks are simply behaving as a resistor.

It is obvious that a forward-biased junction can be represented by a very low resistance. From point x on Fig. 2-7, the *forward resistance* for silicon is calculated as

$$R_F = \frac{0.7 \text{ V}}{20 \text{ mA}} = 35 \ \Omega$$

For germanium, from point y on Fig. 2-7,

$$R_F = \frac{0.3 \text{ V}}{20 \text{ mA}} = 15 \ \Omega$$

In practice, R_F is normally not used; instead the *dynamic resistance* (r_d) of the junction is determined. This quantity is also known as the *incremental resistance* or *ac resistance*. The dynamic resistance is measured as the reciprocal of the slope of the forward characteristic beyond the knee.

Suppose the current and voltage conditions are changed from point a to point b on Fig. 2-7. The change in forward voltage is $\Delta V_F \simeq 0.1$ V, and the change in forward current is $\Delta I_F \simeq 40$ mA, as illustrated. The resistance change r_d is calculated as

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{0.1 \text{ V}}{40 \text{ mA}} = 2.5 \ \Omega$$

As discussed in Section 2-3, the reverse current I_S is made up of minority charge carriers crossing the junction. When the temperature of semiconductor material is increased, the additional thermal energy causes more electrons to break away from atoms. This creates more hole–electron pairs and generates more minority charge carriers. Therefore, I_S increases as junction temperature rises.

I_S can be shown to be dependent upon electronic charge, doping density, and junction area, as well as temperature. With the exception of temperature, all these factors are constant for a given junction; thus I_S is altered only by temperature change. It has been found that I_S approximately doubles for each 10°C increase in temperature. Hence, for a given junction, there is a definite I_S level for each temperature level (Fig. 2-8).

It has been shown that I_S increases with increase in temperature. It can also be shown that the forward current I_F is proportional to I_S. Therefore, as illustrated by the vertical line in Fig. 2-9(a), for a fixed level of

2-5
Temperature
Effects
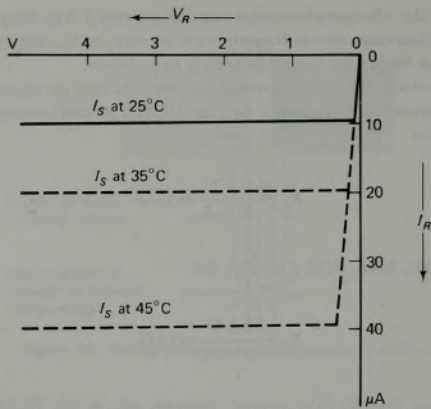
Figure 2-8. Temperature effect on reverse characteristics.
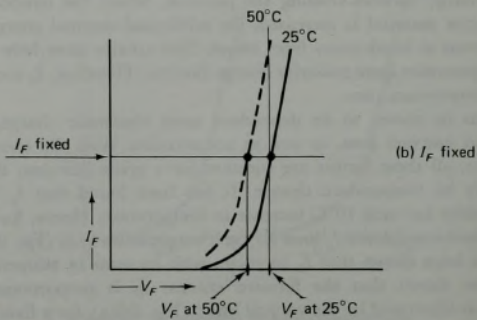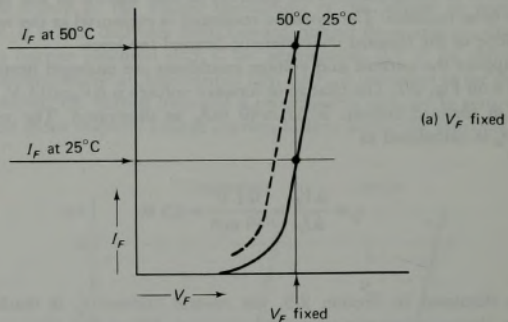
Figure 2-9. Temperature effect on forward characteristics.

V_F, I_F increases as the junction temperature increases. If I_F (at the increased temperature) is measured for several levels of V_F and the results plotted, it is seen that the characteristic is moved to the left. The horizontal line on Fig. 2-9(b) shows that, if I_F is held constant while the junction temperature is changing, the foward voltage, V_F, decreases with junction temperature increase (i.e., V_F has a negative temperature coefficient). It is found that the temperature coefficient for the forward voltage of a pn-junction is approximately -1.8 mV/°C for silicon and -2.02 mV/°C for germanium.

The depletion layer of a pn-junction is a region depleted of charge carriers. Therefore, as an insulator or a dielectric medium situated between two low-resistance regions, it is a capacitor. The value of the *depletion layer capacitance*, designated C_{pn}, may be calculated from the usual formula for a parallel plate capacitor. A typical value of C_{pn} is 40 picofarads (pF). Since the width of the depletion layer can be changed by altering the reverse-bias voltage, the capacitance of a given junction may be controlled by the applied bias. This property is utilized in a variable-capacitance device known as a *varicap* or *varactor* (Chapter 19).

Consider a forward-biased junction carrying a current I_F. If the applied voltage is suddenly reversed, I_F ceases immediately, leaving some majority charge carriers in the depletion region. These charge carriers must flow back out of the depletion region, which is widened when reverse biased. The result is that, when a forward-biased junction is suddenly reversed, a reverse current flows which is large initially and slowly decreases to the level of I_S. The effect may be likened to the discharging of a capacitor, and so it is represented by a capacitance known as the *diffusion capacitance* C_d. It can be shown that C_d is proportional to the forward current I_F. This is to be expected, since the number of charge carriers in the depletion region must be directly proportional to I_F. A typical value of diffusion capacitance C_d is 0.02 μF, which is very much greater than the depletion layer capacitance, C_{pn}.

The effect produced by C_d is variously known as *recovery time*, *carrier storage*, or, in junctions with a heavily doped p-region, as *hole storage*. The diffusion capacitance becomes very important in devices which are required to switch rapidly from forward to reverse bias (see Section 3-11).

A reverse-biased junction can be simply represented as the reverse resistance R_R in parallel with the depletion layer capacitance C_{pn} [Fig. 2-10(a)].

The equivalent circuit for a forward-biased junction is represented by the dynamic resistance r_d in parallel with the diffusion capacitance C_d. A battery (to represent the barrier potential) must be included in series with r_d. The complete equivalent circuit for a forward-biased junction is shown in Fig. 2-10(b).

25
Junction
Equivalent Circuit

2-6
Junction
Capacitance

2-7
Junction
Equivalent
Circuit

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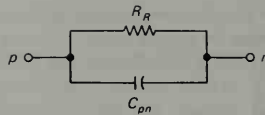
(a) Equivalent circuit
   for reverse biased
   junction
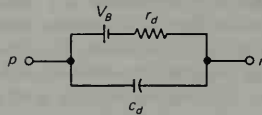
(b) Equivalent circuit
   for forward biased
   junction

Figure 2-10. Equivalent circuits for *pn*-junction.

Glossary of Important Terms

Barrier potential. Potential at a *pn*-junction, resulting from charge carriers crossing the junction. Typically, 0.3 V for germanium, 0.7 V for silicon.

Depletion region. Narrow region depleted of charge carriers.

Reverse saturation current. Minority charge carrier current that flows across a reverse-biased junction.

Avalanche effect. Charge carriers increasing in number by knocking other charge carriers out of atoms.

Reverse breakdown. Junction breakdown under the influence of a large reverse-bias voltage.

Forward current. Current that flows across a forward-biased *pn*-junction.

Depletion layer capacitance. Junction capacitance due to depletion region.

Diffusion capacitance. Junction capacitance due to forward current.

Varicap. Variable capacitance device utilizing the depletion layer capacitance.

Varactor. Same as *varicap*.

Reverse resistance. Resistance of a reverse-biased junction.

Forward resistance. Resistance of a forward-biased junction.

Reverse characteristic. Plot of reverse current to base of junction reverse-bias voltage.

Forward characteristic. Plot of forward current to base of junction forward-bias voltage.

Dynamic resistance. Reciprocal of the slope of the forward characteristic beyond the knee.

Incremental resistance. Same as dynamic resistance.

AC resistance. Same as dynamic resistance.

Recovery time. Effect of diffusion capacitance on time required to change the current crossing a forward-biased junction.

Carrier storage. Same as *recovery time*.

Hole storage. Same as *recovery time*.

Reverse bias. Voltage applied to junction, positive to n-side, negative to p-side.

Forward bias. Voltage applied to junction, positive to p-side, negative to n-side.

Review Questions

2-1. Using illustrations, explain how the depletion region at a pn-junction is produced. List the characteristics of the depletion region.

2-2. Draw a sketch to show the barrier potential at a pn-junction, with (a) equal doping, and (b) unequal doping of each side. Show the relative widths of the depletion region on each side of the junction and the polarity of the barrier potential.

2-3. A bias is applied to a pn-junction, positive to the p-side, negative to the n-side. Show, by a series of sketches, the effect of this bias upon: depletion region width, barrier potential, minority carriers, majority carriers. Briefly explain the effect in each case.

2-4. Repeat Question 2-3 for a bias applied negative to the p-side, positive to the n-side.

2-5. Sketch the voltage-current characteristics for a pn-junction (a) with forward bias, (b) with reverse bias. Show how temperature change affects the characteristics.

2-6. State typical values for the depletion layer capacitance and diffusion capacitance and briefly explain the origin of each. Which of the two is more important at (a) a forward-biased junction, (b) a reverse-biased junction?

2-7. Draw the equivalent circuits for forward-biased and reverse-biased junctions. Identify the components of each.

2-8. From the forward and reverse characteristics shown in Fig. 2-11, determine R_F, r_d, R_R, and I_S. Define each quantity.
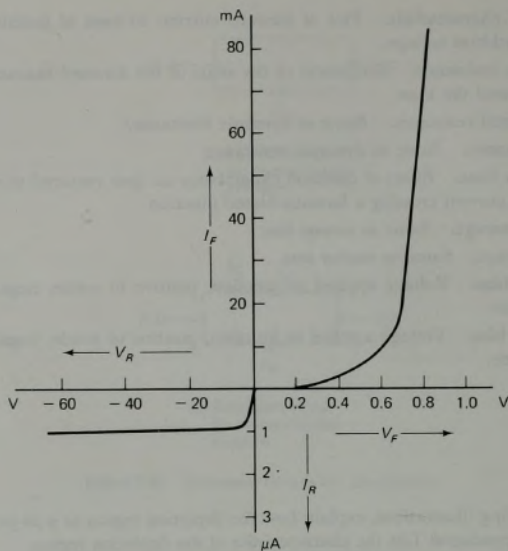
Figure 2-11.

2-9. State typical values of reverse saturation current for silicon and germanium junctions. Explain the origin of reverse saturation current.

2-10. State typical values of barrier potential for silicon and germanium junctions. Explain the origin of the barrier potential.

2-11. What effect does the barrier potential have upon majority charge carriers and minority charge carriers? Briefly explain.

The Semiconductor Diode

The term *diode* indicates a two-electrode device. The semiconductor diode is simply a *pn*-junction. The two sides of the junction are provided with connecting terminals or leads. A diode is a one-way device, offering a low resistance when forward biased, and behaving almost as an insulator (or opened switch) when reverse biased. One of the most important applications of the diode is as a rectifier.

3-1
Introduction

The symbol for the diode is an arrowhead and bar, as shown in Fig. 3-1. The arrowhead indicates the *conventional direction of current flow* when forward biased, i.e., from the positive terminal through the device to the negative terminal. The *p*-side of the diode is always the positive terminal for forward bias and is designated the *anode*. The *n*-side is called the *cathode* and is the negative terminal when the device is forward biased.

3-2
Diode Symbol
and
Appearance

29

Positive terminal
for forward bias

Negative terminal
for forward bias

I_F

+

−

Anode (p-type)

Cathode (n-type)

Arrowhead indicates
convention current
direction when
forward biased

Figure 3-1. Diode symbol.

0.3 cm

(a) Low current
diode

0.5 cm

(b) Medium current
diode

3.5 cm
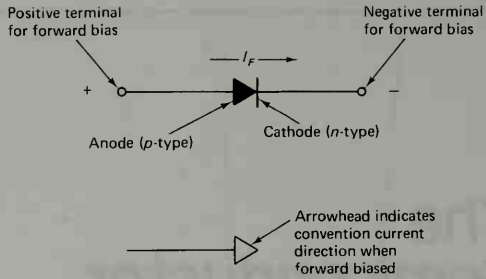
(c) High current
diode
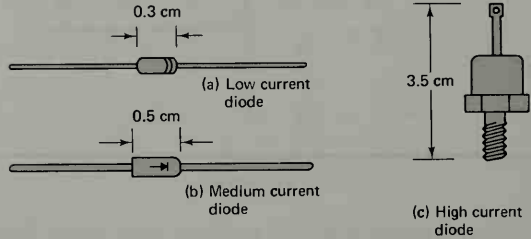
Figure 3-2. Typical low, medium, and high-current diodes.

Figure 3-2 shows the appearance of low-, medium-, and high-current diodes. The body of the low-current device may be only 0.3 cm long. The cathode is usually denoted by a color band, and several bands may be used to color code the device's type number. This type of diode is capable of passing approximately 100 mA of forward current. It can also survive about 75-V reverse bias without breaking down, and its reverse saturation current at 25° C is typically less than 1 μA.

The medium-current diode shown in Fig. 3-2(b) can typically pass a forward current of about 400 mA and can survive over 200 V of reverse bias. The anode and cathode terminals may be indicated by a diode symbol on the side of the device or by colored bands close to the cathode end. Low- and medium-current diodes are usually mounted by soldering their leads to connecting terminals. Heat generated in the device is then carried away by air convection and by conduction along the connecting leads. High-current

diodes, or power diodes [Fig. 3-2(c)], generate a lot of heat, and air convection would be completely inadequate. Such devices are designed for bolt mounting to a metal *heat sink* which will conduct the heat away. Power diodes can pass forward currents of many amperes and can survive several hundred volts of reverse bias.

One of the most common methods used for diode construction is the *alloy* technique. In this method, a *pn*-junction is formed by melting a tiny pellet of aluminum (or some other *p*-type impurity) upon the surface of an *n*-type crystal. Similarly, an *n*-type impurity may be melted upon the surface of a *p*-type crystal. The process is illustrated in Fig. 3-3(a).

Aluminum or indium pellet

Anode

p-region

n-type substrate

Cathode

(a) Alloy diode

Silicon oxide

p-type impurities diffusing

Anode

Plated contacts

p-region

n-type substrate

Cathode
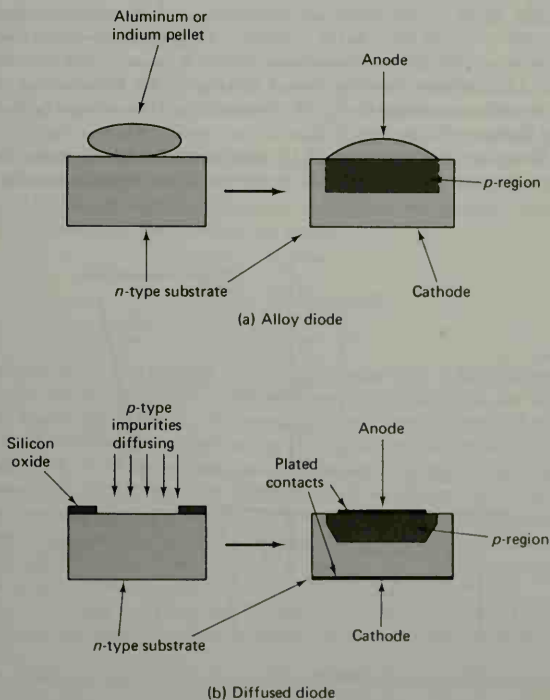
(b) Diffused diode

Figure 3-3. Fabrication of alloy and diffused diodes.

Another method employed in diode manufacture is *diffusion* construction, illustrated in Fig. 3-3(b). When an n-type semiconductor is heated in a chamber containing an acceptor impurity in vapor form, some of the acceptor atoms are diffused (or absorbed) into the n-type crystal. This produces a p-region in the n-type material, and thus creates a pn-junction. By uncovering only part of the n-type material during the diffusion process (the remainder has a thin coating of silicon dioxide), the size of the p-region can be limited. Metal contacts are finally electroplated on the surface of each region for connecting leads.

The diffusion technique lends itself to the simultaneous fabrication of many hundreds of diodes on one small disc of semiconductor material. This process is also used in the production of transistors and integrated circuits.

3-4
Diode
Characteristics
and
Parameters

The diode is essentially a pn-junction and its characteristics and parameters are those discussed in Chapter 2. Figure 3-4 shows the characteristics of a typical low-current silicon diode. It is seen that the forward current (I_F) remains low (less than 1 mA) until the forward-bias voltage (V_F) exceeds approximately 0.7 V. Beyond this bias voltage I_F increases almost linearly with increase in V_F.

Since the reverse current (I_R) is very much smaller than the forward current, the reverse characteristic is plotted to an expanded scale. I_R is
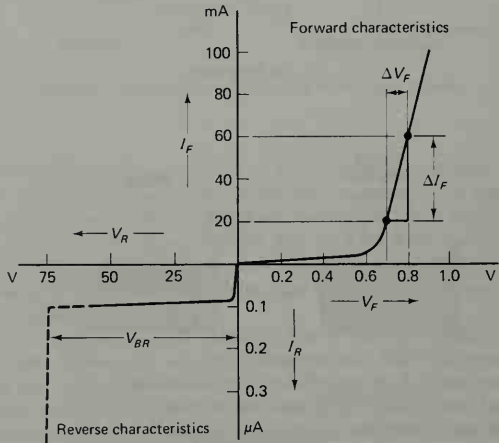
Figure 3-4. Forward and reverse characteristics for a typical low-current silicon diode.

shown to be on the order of nanoamperes and is almost completely un-affected by increases in reverse-bias voltage. As already explained in Chapter 2, I_R is largely a minority carrier reverse saturation current (I_S). Nonlinearity of I_R occurs because some minority charge carriers leak along the junction surface, and this current component increases with increase in reverse-bias voltage. For the characteristics in Fig. 3-4, I_R is less than 1/10,000 of the lowest normal forward current. Therefore, I_R is quite negligible when compared to I_F, and the reverse-biased diode may be considered almost as an insulator or an open switch.

If the reverse voltage V_R is increased to 75 V for a diode with the characteristics of Fig. 3-4, the device will go into *reverse breakdown*. This is shown by the broken line on the reverse characteristic. Reverse breakdown can destroy a diode unless the current is limited by means of a suitable resistor connected in series with the device. The resistor value must be selected to keep the device power dissipation ($V_R \times I_R$) below the maximum specified by the manufacturer.

The diode parameters of greatest interest are *forward volt drop* (V_F), *dynamic resistance* (r_d), *reverse saturation current* (I_S), and *reverse breakdown voltage* (V_{BR}). The maximum forward current ($I_{F_{(max)}}$) is also important. All these quantities are normally listed on the device data sheet provided by the manufacturer. For the characteristics in Fig. 3-4, V_F is 0.7 to 0.9 V, I_S is approximately 0.1 μA, and V_{BR} is 75 V. The dynamic resistance is de-termined by calculating the reciprocal of the slope of the forward character-istic beyond the knee. As shown in the figure,

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{0.1 \text{ V}}{40 \text{ mA}} = 2.5 \ \Omega$$

Figure 3-5 shows a diode connected in series with a 100-Ω resistance (R_L) and a supply voltage (V_S). The polarity of V_S is such that the diode is forward biased; consequently, the current in the circuit is identified as I_F.

To determine the voltage across the diode and the current flowing through it, a *dc load line* must be superimposed on the diode forward characteristics. The dc load line illustrates all dc conditions that could exist within the circuit for given values of V_S and R_L. Since the load line is always straight, it can be constructed by plotting any two corresponding current and voltage points and then drawing a straight line through them. The process is demonstrated in Example 3-1.

To determine two points on the load line, a formula relating voltage, current, and resistance must first be derived from the circuit. From Fig. 3-5,

Supply voltage (V_S) = (volts drop across R_L) + (volts drop across diode)

$$V_S = I_F R_L + V_F \tag{3-1}$$
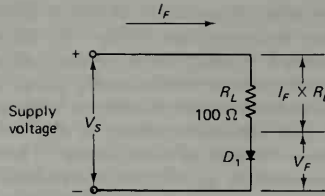
Figure 3-5. Diode and resistor in series.

Example 3-1

Draw the dc load line for the circuit shown in Fig. 3-5. The diode characteristics are given in Fig. 3-6.

solution

From Eq. (3-1),

$$V_S = I_F R_L + V_F$$

When $I_F = 0$,

$$V_S = 0 + V_F$$

Therefore, the diode voltage is

$$V_F = V_S = 5 \text{ V}$$

Plot point A on the diode characteristics at $I_F = 0$ and $V_F = 5$ V. When $V_F = 0$.

$$V_S = I_F R_L + 0$$

$$I_F = \frac{V_S}{R_L}$$

$$= \frac{5\text{V}}{100\Omega} = 50 \text{ mA}$$

Plot point B on the diode characteristic at $I_F = 50$ mA and $V_F = 0$. Now draw the dc load line through points A and B.

Since the relationship between the diode forward voltage V_F and the forward current I_F is defined by the diode characteristic, there is only one point on the dc load line at which the diode voltage and current are compatible with the circuit conditions. That is point Q, termed the *quiescent*
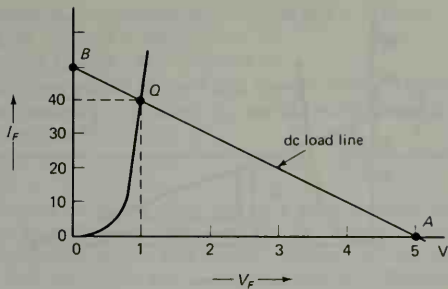
Figure 3-6. Plotting the dc load line for a diode circuit.

point or *dc bias point*, where the load line intersects the diode characteristic. This may be checked by substituting the values of I_F and V_F at point Q into Eq. (3-1).

From point Q on Fig. 3-6, $I_F = 40$ mA and $V_F = 1$ V. Equation (3-1) states that $V_S = I_F R_L + V_F$; therefore, $V_S = (40$ mA $\times 100$ $\Omega) + 1$ V $= 5$ V. No other values of I_F and V_F on the diode characteristics can satisfy Eq. (3-1).

In the circuit of Fig. 3-5, the resistor R_L determines the slope of the dc load line, and the supply voltage V_S determines the point A on the load line. Therefore, the quiescent conditions for the circuit can be altered by changing either R_L or V_S.

When designing a diode circuit, it may be desired to use a given supply voltage and set up a specified forward current. In this case, point A and the Q point are first plotted, and the dc load line is drawn. R_L is then calculated by determining the slope of the load line. The problem could also occur in another way. For example, R_L and the required I_F are known, and V_S has to be determined. This problem is solved by plotting points B and Q and drawing the load line through them. The supply voltage is then read as V_F at point A.

For the circuit shown in Fig. 3-5, determine a new value of load resistance which will give a forward current of 30 mA.

Example 3-2

solution

From Eq. (3-1), $V_F = V_S - I_F R_L$.
When $I_F = 0$, $V_F = 5$ V.
Plot point A on the characteristics (Fig. 3-7) at $I_F = 0$ and $V_F = 5$ V.
Point Q is plotted on the device characteristic at $I_F = 30$ mA. The new dc load line is now drawn through points A and Q, and R_L is determined as the
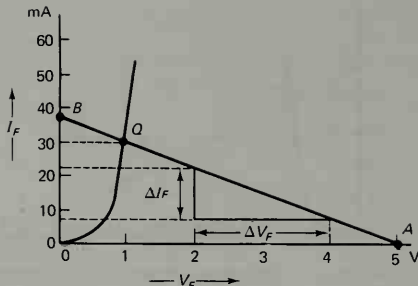
Figure 3-7. Determining the value of R_L for a given supply voltage and forward current.

reciprocal of the slope of the load line.

$$R_L = \frac{\Delta V_F}{\Delta I_F} = \frac{2\ \text{V}}{15\ \text{mA}} = 133\ \Omega$$

Example 3-3   For the circuit of Fig. 3-5, determine a new value of V_S which will give $I_F = 50$ mA.

solution

Plot point Q on the forward characteristic at $I_F = 50$ mA (Fig. 3-8). V_F at the Q point is 1.1 V. To find another point on the load line, the voltage change across the diode for a given change in I_F is calculated.
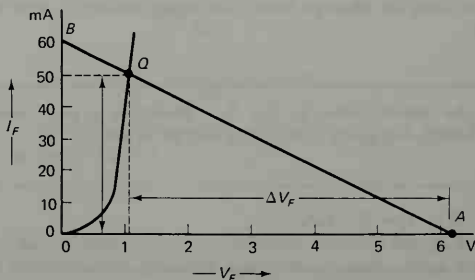
Figure 3-8. Determining the value of supply voltage required for a given R_L and I_F.

When I_F changes from 50 mA to zero, $\Delta I_F = 50$ mA
and $\Delta V_F = \Delta I_F R_L = 50$ mA $\times 100$ $\Omega = 5$ V.
The new value of V_F is $(1.1$ V $+ 5$ V$) = 6.1$ V.

Point A is now plotted at $I_F = 0$ and $V_F = 6.1$ V (Fig. 3-8). The dc load
line is drawn through points A and Q, and the value of supply voltage is
read from point A as $V_S = 6.1$ V.

The previous discussion refers only to a forward-biased diode. For a
reverse-biased diode a similar approach can be taken. To determine the
exact levels of reverse current and voltage, the load line can be drawn as
before, but this time upon the reverse characteristic. Equation (3-1) is
applicable, but instead of forward voltage and current, the reverse quantities
are substituted [see Fig. 3-9(a)]. The equation becomes

$$V_S = I_R R_L + V_R \tag{3-2}$$

A dc load line drawn upon the device reverse characteristics would be
almost vertical [see Fig. 3-9(b)]. Usually, such a load line is not drawn,
because the diode reverse current can easily be determined from the device
reverse characteristics. On Fig. 3-9(b), at $V_R = 50$ V, I_R is approximately 1.5
μA. At $V_R = 10$ V, I_R is around 1 μA.

(a) Diode circuit
with reverse
bias voltage

(b) Reverse characteristic
and dc load line
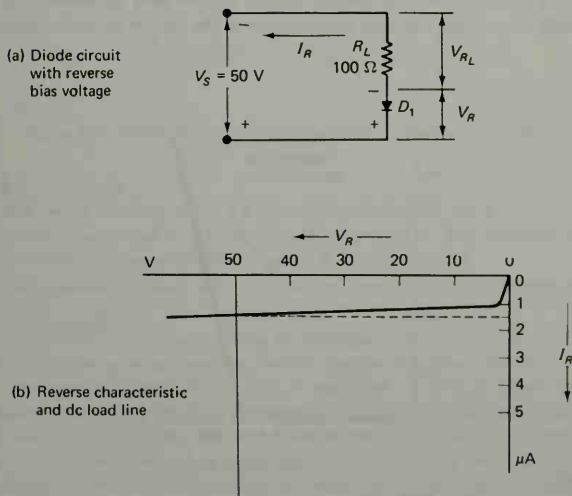
Figure 3-9. Drawing the dc load line on diode reverse characteristics.

When designing a diode circuit, a straight-line approximation of the diode forward characteristic is sometimes employed. This approximation is called the *piecewise linear characteristic*. The piecewise linear characteristic may be constructed by simply drawing a straight line on the near linear portion of the characteristic and extending it to the horizontal axis, as shown in Fig. 3-10. Notice that the straight line cuts the horizontal axis approximately at $V_F = 0.7$ V, i.e., at the barrier potential (V_B). For germanium diode characteristics the straight line would meet the horizontal axis at approximately $V_F = 0.3$ V.

The reciprocal of the slope of the near linear portion of the diode characteristics is the dynamic resistance r_d. From Fig. 3-10, an equation may be determined relating V_F, I_F, and V_B.

$$V_F = V_B + I_F r_d \tag{3-3}$$

If the diode forward characteristic is not available, the piecewise linear characteristic may be constructed from a knowledge of the dynamic resistance r_d and the barrier voltage V_B. The value of r_d is usually available from the manufacturer's data sheet, and V_B is approximately 0.7 V for a silicon diode and 0.3 V for a germanium device.

The diode piecewise linear characteristic is reasonably accurate only for values of I_F above the knee of the diode forward characteristic. Therefore, this approximate characteristic should be used only for diodes that are normally biased into the near-linear region of the device forward characteristics.
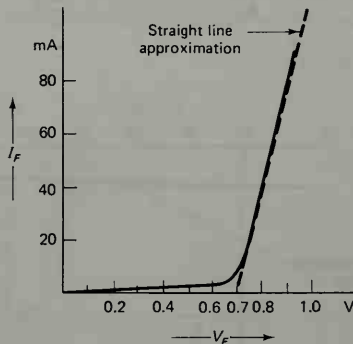
Figure 3-10. Diode piecewise linear characteristics.

Example 3-4

Draw the piecewise linear characteristic for a silicon diode with a dynamic resistance r_d of 3.2 Ω. The maximum forward current I_F is 100 mA.

solution

Convenient I_F and V_F scales are set up as shown in Fig. 3-11, with I_F going to its maximum value of 100 mA. Since the device is silicon, a V_B of 0.7 V is marked at point K. Point L is determined from Eq. (3-3):

$V_F = V_B + I_F r_d$.
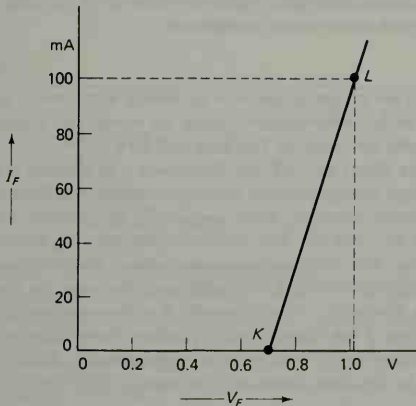
Figure 3-11. Diode piecewise linear characteristics drawn from V_B and r_d.

Take $I_F = 100$ mA.
Then $V_F = 0.7$ V + (100 mA × 3.2 Ω) = 0.7 V + 0.32 V = 1.02 V.
Point L is now plotted at $I_F = 100$ mA and $V_F = 1.02$ V. The piecewise linear characteristic is drawn by joining points K and L together.

The equivalent circuits for a forward-biased and reverse-biased diode are exactly the same as those discussed in Section 2-7. The equivalent circuit for the forward-biased diode may be modified to form a *small-signal ac equivalent circuit*. This circuit is employed for diodes which are maintained in a forward-bias condition, but which are subjected to small variations in I_F and V_F. The small-signal ac equivalent circuit is drawn (see Fig. 3-12) by dropping the battery representing the barrier potential from the circuit of Fig. 2-10(b).

3-7
Diode
Equivalent
Circuit

39
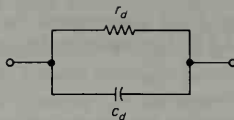
Figure 3-12. Small-signal ac equivalent circuit for forward-biased diode.

Diodes are frequently connected with other components in circuits which must be *ac analyzed*. An example of this is an amplifier, which must be analyzed to determine its gain, input impedance, etc. In this circumstance, the diode ac equivalent circuit is employed.

3-8
Diode Data
Sheet

To select the proper diode for a particular application, the data sheets provided by device manufacturers must be consulted. Portions of typical diode data sheets are shown in Fig. 3-13 and 3-14.

Most data sheets start off with the device type number at the top of the page, and a short descriptive title, e.g., *silicon rectifier* or *diffused silicon switching diode*. Immediately following, there are usually mechanical data, perhaps a description of the package, and an illustration showing the package shape and dimensions. The absolute maximum ratings at 25° C are then listed. These are maximum voltages, currents, etc., that can be applied without destroying the device. It is very important that these ratings not be exceeded, otherwise failure of the diode is quite possible. For reliability, the absolute maximum ratings should not even be approached. Also, the maximum ratings must be adjusted downward for operation at temperatures greater than 25° C.

There is normally a list of other electrical characteristics for the device following the absolute maximum ratings. An understanding of all the parameters specified on a data sheet will not be achieved until circuit design is studied. However, some of the most important parameters are considered below:

V_{RM} *Peak reverse voltage (or peak inverse voltage)*   This is the absolute peak of voltage that may be applied in reverse across the diode.

V_{BR} *Reverse breakdown voltage*   The minimum reverse voltage at which the device may break down.

I_F *Steady-state forward current*   This is the maximum current that may be passed continuously through the diode. It is usually specified for 25° C, and must be derated for operation at higher temperatures.

$I_{FM(surge)}$ *Peak surge current*   This current may be passed for the time period specified through a diode operating below the specified temperature. The surge current is very much higher than the normal

SO-1000 VOLTS • 1 AMP AVG

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• mechanical data

THE LEADS ARE ELECTRICALLY INSULATED FROM THE CASE
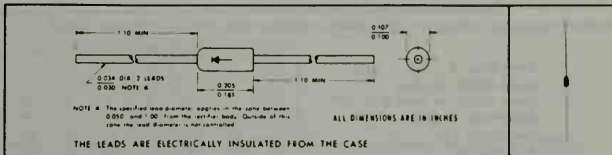
• absolute maximum ratings at specified ambient† temperature

		1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	UNIT
V_{RM}	Peak Reverse Voltage from $-65°C$ to $-175°C$ (See Note 1)	50	100	200	400	600	800	1000	v
V_R	Steady State Reverse Voltage from 25°C to 75°C	50	100	200	400	600	800	1000	v
I_O	Average Rectified Forward Current from 25°C to 75°C (See Notes 1 and 2)	1							a
$I_{FM(rep)}$	Repetitive Peak Forward Current, 10 cycles, at (or below) 75°C (See Note 3)	10							a
$I_{FM(surge)}$	Peak Surge Current, One Cycle, at (or below) 75°C (See Note 3)	30							a
$T_{A(opr)}$	Operating Ambient Temperature Range	-65 to -175							°C
T_{stg}	Storage Temperature Range	-65 to -200							°C
	Lead Temperature ¾ Inch from Case for 10 Seconds	350							°C

NOTES 1 These values may be applied continuously under single-phase 60 cps, half sine wave operation with resistive load. Above 75°C derate I_O according to Figure 1

2 This rectifier is a lead-conduction cooled device. At (or above) ambient temperatures of 75°C, the lead temperature ¾ inch from case must be no higher than 5°C above the ambient temperature for these ratings to apply

3 These values apply for 60 cps half sine waves when the device is operating at (or below) rated values of peak reverse voltage and average rectified forward current. Surge may be repeated after the device has returned to original thermal equilibrium

* Indicates JEDEC registered data

† The ambient temperature is measured at a point 2 inches below the device. Natural air cooling shall be used

Figure 3-13. Diode data sheet. (Courtesy of Texas Instruments, Inc.)

TYPES 1N914, 1N914A, 1N914B, 1N915, 1N916, 1N916A, 1N916B and 1N917
DIFFUSED SILICON SWITCHING DIODES

• Extremely Stable and Reliable High–Speed Diodes

mechanical data

ALL DIMENSIONS IN INCHES
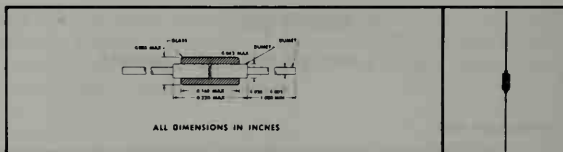
absolute maximum ratings at 25°C ambient temperature (unless otherwise noted)

		1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
V_R	Reverse Voltage at — 65 to + 150°C	75	75	75	50	75	75	75	30	v
I_o	Average Rectified Fwd. Current	75	75	75	75	75	75	75	50	ma
I_o	Average Rectified Fwd. Current at + 150°C	10	10	10	10	10	10	10	10	ma
i_f	Recurrent Peak Fwd. Current	225	225	225	225	225	225	225	150	ma
$i_{f(surge)}$, Surge Current, 1 sec		500	500	500	500	500	500	500	300	ma
P	Power Dissipation	250	250	250	250	250	250	250	250	mw
T_A	Operating Temperature Range	— 65 to + 175								°C
T_{stg}	Storage Temperature Range	. 200								°C

maximum electrical characteristics at 25°C ambient temperature (unless otherwise noted)

		1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
BV_R	Min Breakdown Voltage at 100 μa	100	100	100	65	100	100	100	40	v
I_R	Reverse Current at V_R	5	5	5	5	5	5	5		μa
I_R	Reverse Current at — 20 v	0.025	0.025	0.025		0.025	0.025	0.025		μa
I_R	Reverse Current at — 20 v at 100°C	3	3	3	5	3	3	3	25	μa
I_R	Reverse Current at — 20 v at + 150°C	50	50	50		50	50	50		μa
I_R	Reverse Current at — 10 v				0.025				0.05	μa
I_R	Reverse Current at — 10 v at 125°C									μa
I_F	Min Fwd Current at $V_F = 1$ v	10	20	100	50	10	20	30	10	ma
V_F	at 250 μa								0.64	v
V_F	at 1.5 ma								0.74	v
V_F	at 3.5 ma								0.63	v
V_F	at 5 ma			0.72	0.73			0.73		v
V_F	Min at 5 ma				0.60					v
C	Capacitance at $V_R = 0$	4	4	4	4	2	2	2	2.5	pf

operating characteristics at 25°C ambient temperature (unless otherwise noted)

		1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
t_{rr}	Max Reverse Recovery Time	**4 *8	**4 *8	**4 *8	*10	**4 *8	**4 *8	**4 *8	*3	nsec
										nsec
V_f	Fwd Recovery Voltage (50 ma Peak Sq. wave, 0.1 μsec pulse width, 10 nsec rise time, 5 kc to 100 kc rep. rate)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	v

* Trademark of Texas Instruments
* Lamatron (10 ma I_F; 10 ma I_R; recover to 1 ma)
** EG&G (10 ma I_F; 6v V_R; recover to 1 ma)

Figure 3-14. Low-current diode data sheet. (Courtesy of Texas Instruments, Inc.)

maximum forward current. It is a current that may flow briefly when a circuit is first switched on.

I_R *Static reverse current*   The reverse saturation current for a specified reverse-bias voltage and maximum device temperature.

V_F *Static forward voltage drop*   The maximum forward volt drop for a given forward current and device temperature.

P *Continuous power dissipation, at 25° C*   The maximum power that the device can safely dissipate on a continuous basis in free air. This rating must be downgraded at higher temperatures, and may be upgraded when the device is mounted on a heat sink.

C_T *Total capacitance*   Maximum capacitance for a forward-biased diode at a specified forward current.

t_{rr} *Reverse recovery time*   Maximum time for the device to switch from *on* to *off*.

3-9
Half-Wave
Rectification

3-9.1
Basic Half-Wave Rectifier

The basic diode half-wave rectifier circuit is shown in Fig. 3-15. An alternating voltage is applied to a single diode connected in series with a load resistor (R_L). The diode is forward biased during the positive half-cycle of the input waveform, and reverse biased during the negative half-cycle.
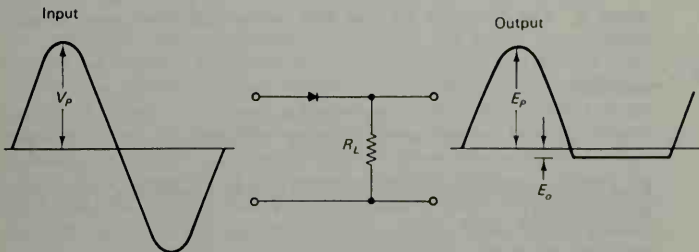
(a) Basic rectifier circuit showing input and output waveforms
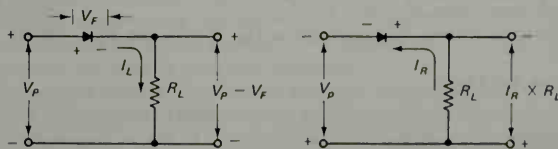
(b) Effect of positive input

(c) Effect of negative input

Figure 3-15. Basic half-wave rectifier circuit.

Substantial current flows through R_L only during the positive half-cycles of the input. During the negative half-cycles, the diode behaves almost as an open circuit. The output voltage developed across R_L is a series of positive half-cycles of alternating voltage, with intervening small constant negative voltage levels.

When the diode is forward biased [Fig. 3-15(b)], the voltage drop across it is V_F, and the output voltage is (input voltage) $- V_F$. The peak output voltage is

$$E_P = V_P - V_F \tag{3-4}$$

and the peak load current is

$$I_P = \frac{V_P - V_F}{R_L} \tag{3-5}$$

During the negative half-cycle of the input waveform [Fig. 3-15(c)] the reverse-biased diode offers a very high resistance, so that only a very small reverse current (I_R) flows. In this case the output voltage is

$$E_O = -I_R \times R_L \tag{3-6}$$

Example 3-5   A diode connected as shown in Fig. 3-15 has the characteristics shown in Fig. 3-16. R_L is 500 Ω, and the input voltage has a peak amplitude of 50 V. Calculate the positive and negative peaks of output voltage developed across R_L. Also determine the peak load current and diode power dissipation.

solution

$$I_F = I_L \approx \frac{V_P}{R_L} = \frac{50 \text{ V}}{500 \text{ }\Omega} = 100 \text{ mA}$$

From the forward characteristics in Fig. 3-16, when $I_F = 100$ mA, $V_F = 0.9$ V. From Eq. (3-4),

$$E_P = 50 \text{ V} - 0.9 \text{ V}$$

Peak output voltage, $E_P = 49.1$ V.
From the reverse characteristics in Fig. 3-16, when $V_R = -50$ V, $I_R = -1$ μA.
From Eq. (3-6),

$$E_O = -1 \text{ }\mu\text{A} \times 500 \text{ }\Omega$$

Negative output voltage, $E_O = -0.5$ mV.
From Eq. (3-5),

$$I_P = \frac{V_P - V_F}{R_L} = \frac{50 \text{ V} - 0.9 \text{ V}}{500 \text{ }\Omega}$$
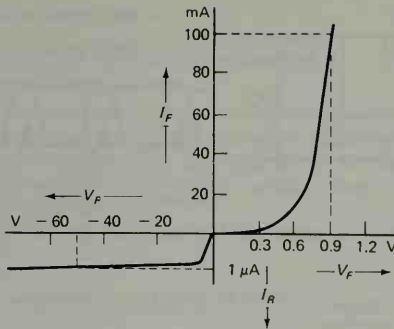
Figure 3-16. Diode characteristics for Example 3-5.

Peak load current, $I_P = 98.2$ mA.
When forward biased, the **diode peak power dissipation** is

$$P_D = V_F \times I_P = 0.9 \text{ V} \times 98.2 \text{ mA}$$

$$= 88.38 \text{ } mW$$

When an alternating voltage is rectified, the output is a series of positive (or negative) half-cycles of the input waveform. It is still not direct voltage. To convert to direct voltage (dc) a *smoothing circuit* (or *filter*) is employed. Figure 3-17 shows a half-wave rectifier circuit with a single capacitive filter. The capacitor, termed a *reservoir capacitor*, becomes charged up almost to the input peak voltage when the diode is forward biased. When the diode is reverse biased, the capacitor partially discharges through the load. Since the capacitor always has some positive charge, the diode becomes forward biased only near the peaks of input voltage. At this time, it passes a current pulse to the capacitor to replace the charge lost to the load. The result is that the output is a direct voltage with a superimposed *ripple* waveform. The amplitude of the ripple voltage depends upon the load resistance and capacitor values. For half-wave rectification, the ripple voltage frequency is the same as the input frequency.

The required value of the reservoir capacitor depends upon the load current and the acceptable ripple voltage amplitude. Consider the ripple waveform illustrated in Fig. 3-18. V_r is the peak-to-peak ripple voltage, $E_{O(\max)}$ is the maximum output level, and $E_{O(\min)}$ is the minimum output level. Time t_1 is the interval between input current pulses, i.e., the time during which the reservoir capacitor is being discharged by the load current. Time t_2 is the duration of the input current pulse that recharges the

3-9.2
*Half-Wave
Rectifier with
Capacitor
Smoothing*
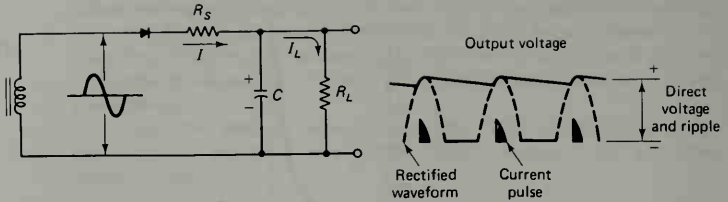
Figure 3-17. Circuit and output waveform for a half-wave rectifier with capacitor smoothing.
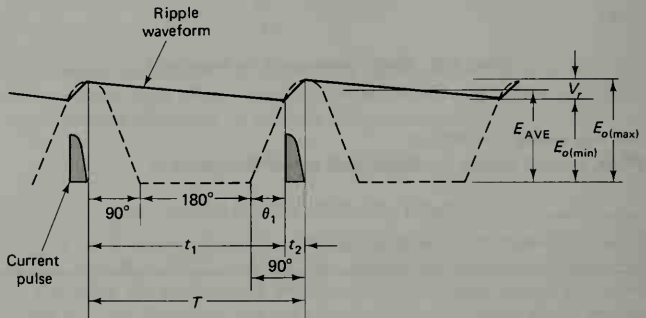
Figure 3-18. Output from half-wave rectifier with capacitor smoothing circuit.

capacitor. From the figure it is seen that time t_1 depends upon the sum of the degrees through which the input waveform passes while the output is going from $E_{O(\max)}$ to $E_{O(\min)}$. Knowing the input frequency, the total time t_1 can be determined. Then using t_1, I_L and V_r, the reservoir capacitor value can be calculated.

$$E_{O(\min)} = E_{O(\max)} \sin \theta_1$$

$$\sin \theta_1 = \frac{E_{O(\min)}}{E_{O(\max)}} \tag{3-7}$$

$$t_1 = (\text{time for } 90°) + (\text{time for } 180°) + (\text{time for } \theta_1°) \tag{3-8}$$

Taking the load current as a constant quantity which is discharging the capacitor between input pulses, the simple formula $C = Q/V$ may be used to calculate the reservoir capacitor value. Since $Q = It$,

$$C = \frac{I_L \times t_1}{V_r} \tag{3-9}$$

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The time t_2 can be determined as

$$t_2 = (\text{time for } 90°) - (\text{time for } \theta_1°) \qquad (3\text{-}10)$$

Determine the reservoir capacitor value for a half-wave rectifier and smoothing circuit to supply 20 V to a load of 500 Ω. Maximum ripple amplitude is to be 10% of the average output voltage, and the input frequency is 60 hertz (Hz).

Example 3-6

solution

Ripple voltage amplitude = V_r = 10% of 20 V = 2 V.

$$E_{O(\min)} = 20 \text{ V} - 1 \text{ V} = 19 \text{ V}$$
$$E_{O(\max)} = 20 \text{ V} + 1 \text{ V} = 21 \text{ V}$$

From Eq. (3-7),

$$\sin \theta_1 = \frac{19}{21} = 0.905 \quad \therefore \quad \theta_1 \approx 65°$$

Since the input frequency is 60 Hz, the time period of the input waveform is

$$T = \tfrac{1}{60} = 16.6 \text{ ms}$$

and since T is the time for $360°$,

$$\text{time for } 180° = 16.6 \text{ ms} \times \left(\tfrac{180}{360}\right) = 8.3 \text{ ms}$$
$$\text{time for } 90° = 4.16 \text{ ms}$$
$$\text{time for } \theta_1 = 16.6 \text{ ms} \times \left(\tfrac{65}{360}\right) = 3 \text{ ms}$$

From Eq. (3-8),

$$t_1 = 4.16 + 8.3 + 3 \text{ ms} = 15.5 \text{ ms}$$

Load current is

$$I_L = \frac{E_O}{R_L} = \frac{20 \text{ V}}{500 \, \Omega} = 40 \text{ mA}$$

From Eq. (3-9),

$$C = \frac{40 \text{ mA} \times 15.5 \text{ ms}}{2 \text{ V}} = 310 \, \mu\text{F}$$

The rectifier diode used in a circuit such as that shown in Fig. 3-17 must be specified in terms of the currents and voltages that it will be subjected to. The calculated values are the minimums that the device must survive. Obviously, the selected diode should be able to survive greater voltage and current levels than the calculated minimum values.

The capacitor is discharged by I_L flowing for time $(t_1 + t_2)$, and recharged by a current flowing for time t_2. The recharging current is referred to as the *peak repetitive current* and is designated $I_{FM(rep)}$. $I_{FM(rep)}$ is directly proportional to I_L and $(t_1 + t_2)$ and inversely proportional to t_2. For example, if a load current of 1 A flows for a period of 10 ms, then to recharge the capacitor in 1 ms a current of 10 A must flow for the 1 ms time period.

$$I_{FM(rep)} = \frac{I_L(t_1 + t_2)}{t_2} \qquad (3\text{-}11)$$

In the circuit shown in Fig. 3-17, R_S is a small-value resistance known as the *surge limiting resistor*. As its name suggests, the purpose of R_S is to limit any surge of current that may pass through the diode. Such a surge occurs when the supply is first switched on to the rectifier circuit. Before switch-on, the capacitor normally contains no charge, and at switch-on it will initially behave as a short circuit. If switch-on occurs at the instant of peak input voltage, the initial *surge current* flowing will be

$$I_{F(surge)} = \frac{V_P}{R_S}$$

If the diode can survive a specified maximum surge current, $I_{FM(surge)}$, then the surge limiting resistance is selected as

$$R_S = \frac{V_P}{I_{FM(surge)}} \qquad (3\text{-}12)$$

When the half-wave rectifier circuit is operating, the capacitor charge remains approximately at $+V_P$ (see Fig. 3-17). This means that the diode cathode voltage is always approximately $+V_P$. At the peak of the negative half-cycle the input voltage at the diode anode is $-V_P$. In this case the maximum reverse voltage across the diode is

$$E_R = 2V_P \qquad (3\text{-}13)$$

Example 3-7   Specify the diode required for the half-wave rectifier circuit referred to in Example 3-6. Select a suitable device from the data sheets in Figs. 3-13 and 3-14, and calculate the required value of R_s.

From Eq. (3-10),

$$t_2 = 4.16 \text{ ms} - 3 \text{ ms} = 1.16 \text{ ms}$$

and from Eq. (3-11),

$$I_{FM(\text{rep})} = \frac{40 \text{ mA} \times (16.6 \text{ ms})}{1.16 \text{ ms}}$$

The diode peak repetitive current $I_{FM(\text{rep})} \approx 570$ mA.
The diode average forward current is $I_0 = I_L = 40$ mA.
From Eq. (3-4),

$$V_P = E_P + V_F = E_{O(\text{max})} + V_F$$

Taking the typical V_F for a silicon diode as 0.7 V,

$$V_P = 21 + 0.7 \text{ V} = 21.7 \text{ V}$$

and from Eq. (3-13),

$$E_R = 2 \times 21.7 \text{ V}$$

The diode maximum reverse voltage, $E_R = 43.4$ V.

In Fig. 3-13, the 1N4001 is stated as having $V_R = 50$ V, $I_0 = 1$ A, $I_{FM(\text{rep})} = 10$ A. Therefore, its specification is better than required for this application. Any one of the 1N4002 through 1N4007 rectifiers could also be used, but they have progressively higher reverse voltage specifications, and they are all more expensive than the 1N4001. The 1N914 through 1N916 diodes (Fig. 3-14) have large enough reverse voltage specifications for this application, but since the maximum recurrent peak forward current is 225 mA, none of them is suitable.

For the 1N4001,

$$I_{FM(\text{surge})} = 30 \text{ A}$$

Use Eq. (3-12):

$$R_s = \frac{V_p}{I_{FM(\text{surge})}}$$
$$= \frac{27.1 \text{ V}}{30 \text{ A}} = 0.7 \ \Omega$$

Two types of full-wave rectifier circuits are shown in Figs. 3-19 and 3-20. The circuit in Fig. 3-19 uses only two diodes, but its power must be supplied from a transformer with a center-tapped secondary winding. When

3-10
Full-Wave
Rectification
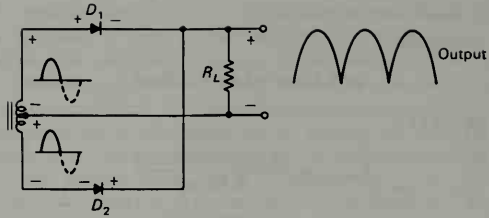
Figure 3-19. Full-wave rectifier circuit using two diodes and a center-tapped transformer.

(a) Bridge rectifier showing input and output

(b) During positive half cycle

(c) During negative half cycle
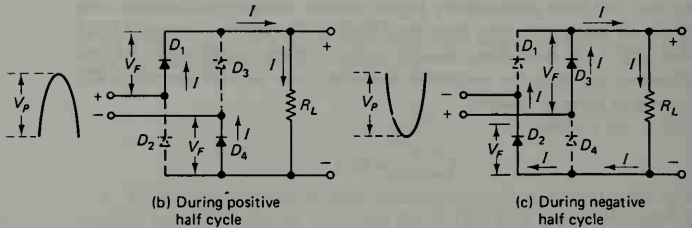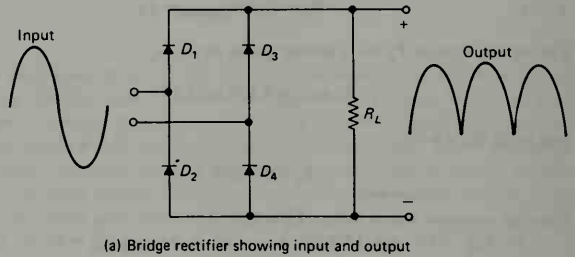
Figure 3-20. Full-wave bridge rectifier circuit.

the transformer output voltage is positive at the top, as shown in the figure, D_1 is forward biased and D_2 is reverse biased. During the negative half-cycle of transformer output, D_2 is forward biased and D_1 is reverse biased. The result is a load waveform composed of continuous positive half-cycles of the diode input waveform, i.e., full-wave rectification.

Because center-tapped transformers are usually more expensive and require much more space than additional diodes, the *bridge rectifier* shown in

Fig. 3-20 is the circuit most frequently used for full-wave rectification. During the positive half-cycle of input voltage to the bridge rectifier, diodes D_1 and D_4 conduct as shown in Fig. 3-20(b). At same time diodes D_2 and D_3 are reverse biased. Figure 3-20(c) shows diodes D_2 and D_3 forward biased during the negative half-cycle of input, while D_1 and D_4 are reverse biased. The result is that both positive and negative half-cycles of the input are passed to load resistance R_L. Also, the negative half-cycles are inverted, so that the output is a continuous series of positive half-cycles of alternating voltage.

Since the bridge rectifier has two forward-biased diodes in series with the supply voltage and R_L, the output voltage amplitude is

$$E_P = V_P - 2V_F \qquad (3\text{-}14)$$

Full-wave rectifier circuits also require smoothing circuits to convert the pulsating output to direct voltage. Figure 3-21 shows that for full-wave rectification the capacitor discharge time is considerably less than with the half-wave rectifier circuit. This means that, for a given load current and ripple voltage, the reservoir capacitor and diode peak repetitive current can both be much smaller.

From Fig. 3-21, the time t_1 becomes

$$t_1 = (\text{time for } 90^\circ) + (\text{time for } \theta_1^\circ) \qquad (3\text{-}15)$$

For the two-diode full-wave rectifier circuit in Fig. 3-19, the maximum diode reverse voltage is $E_R = 2V_P$, just as for the half-wave rectifier. This is not true in the case of the bridge rectifier circuit. Referring again to Fig. 3-20(b), note that the peak cathode voltage of D_3 is $V_P - (V_F$ across $D_1)$. Also note that the anode voltage of D_3 is zero. Therefore, the maximum reverse
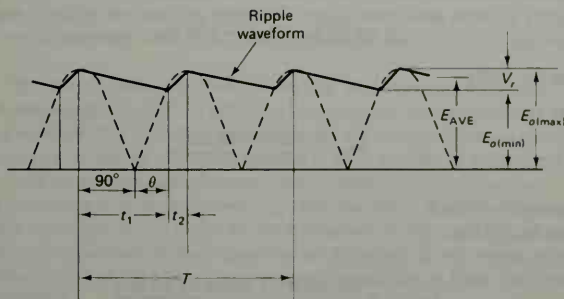
Figure 3-21. Output from full-wave rectifier with capacitor smoothing circuit.

voltage across D_3 and all other diodes is V_P.

$$E_R = V_P \qquad (3\text{-}16)$$

Apart from Eqs. (3-14) to (3-16), all other equations derived for the half-wave rectifier and smoothing circuit also apply to the bridge rectifier.

Example 3-8

Determine the reservoir capacitor value and specify the diodes for a bridge rectifier and smoothing circuit to supply the load specified in Example 3-6.

solution

From Examples 3-6 and 3-7,

$$V_r = 2 \text{ V}$$

$$E_{O(min)} = 19 \text{ V}$$

$$E_{O(max)} = 21 \text{ V}$$

$$\theta_1 = 65°$$

$$\text{time for } 90° = 4.16 \text{ ms}$$

$$\text{time for } \theta_1 = 3 \text{ ms}$$

$$I_L = 40 \text{ mA}$$

$$t_2 = 1.16 \text{ ms}$$

From Eq. (3-15),

$$t_1 = 4.16 \text{ ms} + 3 \text{ ms} = 7.16 \text{ ms}$$

From Eq. (3-9),

$$C = \frac{40 \text{ mA} \times 7.16 \text{ ms}}{2 \text{ V}}$$

Capacitor C = 143 μF.
From Eq. (3-11),

$$I_{FM(rep)} = \frac{40 \text{ mA} \times (7.16 \text{ ms} + 1.16 \text{ ms})}{1.16 \text{ ms}}$$

Diode peak repetitive current, $I_{FM(rep)} \approx 287$ mA.
Since each pair of diodes is conducting on alternate half-cycles:
Diode average forward current,

$$I_0 = I_L/2$$

$$= 40 \text{ mA}/2 = 20 \text{ mA}$$

From Eqs. (3-14) and (3-16),

$$E_R = V_P = 21 \text{ V} + 2(0.7 \text{ V})$$

Diode maximum reverse voltage, $E_R = 22.4$ V.
Once again a 1N4001 is better than required.

There are a great many circuit applications for semiconductor diodes other than rectification. Some of these require the diodes to switch very rapidly from forward to reverse bias, and vice versa. Most diodes will switch rapidly into the forward-biased condition, however, there is always a longer switch-off time due to the diffusion capacitance. This switch-off time, designated as the *reverse recovery time* (t_{rr}), limits the maximum frequency at which the device may be operated.

Figure 3-22(a) illustrates the effect of an input pulse on the diode current. When the pulse goes negative, instead of switching *off* sharply, the diode conducts in reverse. The reverse current (I_R) is initially equal to I_F, but it gradually falls off to the reverse saturation current level (I_S). The reverse current occurs because at the instant of reverse bias there are charge carriers crossing the junction depletion region, and these must be removed. The reverse recovery time is the time required for the current to decrease to I_S.

The reverse recovery time is usually measured in *nanoseconds* (ns), which are seconds $\times 10^{-9}$. Typical values of t_{rr} for switching diodes range from 4 to 50 ns. The switching time obviously limits the maximum operating frequency of the device. If reverse current is to be avoided or minimized, the diode must be switched off relatively slowly. Figure 3-22(b) shows that, if the input frequency is such that $T = 2 \times t_{rr}$, then the diode is conducting almost as much in reverse as it is in the forward direction. In this case it is no longer behaving as a one-way device. To minimize the effect of the reverse current, the time period of the operating frequency should be at least ten times t_{rr} [Fig. 3-22(c)].

3-11
Diode Switching Time and Frequency Response

(a) Reverse recovery time

(b) Effect of t_{rr} with high frequency input

(c) t_{rr} effect with low frequency input
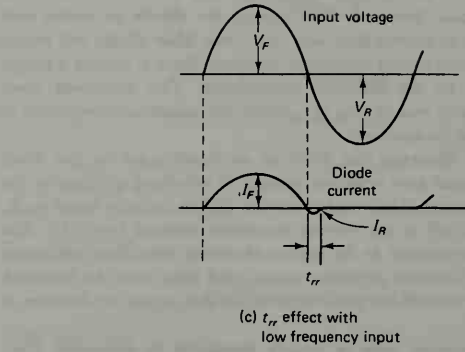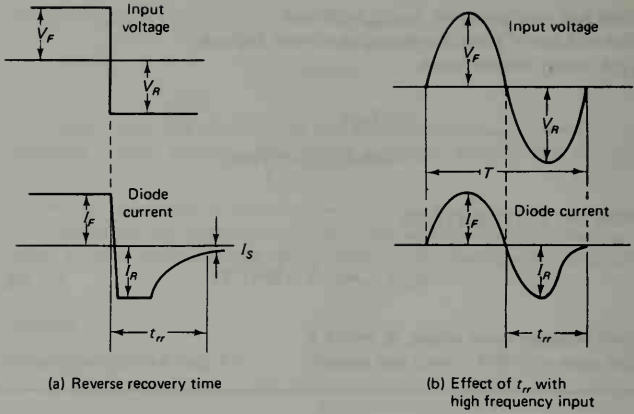
Figure 3-22. Reverse recovery time and its effect on high- and low-frequency inputs.

Example 3-9   Calculate the maximum operating frequency for a diode with reverse recovery time of 4 ns.

solution

$$T \approx 10 \times t_{rr}$$

Therefore,

$$f_{(max)} = \frac{1}{T} = \frac{1}{10 \times t_{rr}}$$

$$= \frac{1}{10 \times 4 \times 10^{-9}} = 25 \text{ MHz}$$

A logic circuit produces an output voltage which is either *high* or *low*, depending upon the levels of several input voltages. The two basic logic circuits are the *AND gate* and the *OR gate*.

Figure 3-23 shows the circuit diagram of a diode AND gate. The circuit has a single output terminal at the diode common anodes and three inputs at the device cathode terminals. (An AND gate could have almost any number of input terminals from 2 up to perhaps 50.) The diode anodes are connected via resistor R_1 to a supply of $V_{CC} = 5$ V.

If one or more of the input terminals is grounded, current flows from the supply through R_1 and through the forward-biased diodes to ground. In this case, the output voltage is just V_F above ground (0.7 V for silicon). The output is said to be *low*. When input levels of 5 V are applied to all three input terminals, none of the diodes is forward biased, and no significant volt drop occurs across R_1. Thus, the output voltage is equal to V_{CC}, and it is referred to as a *high* output level.

The AND gate gives a low output voltage when one or more of its inputs are low and a high output when input *A* is high *and* input *B* is high *and* input *C* is high. Hence the name AND gate.
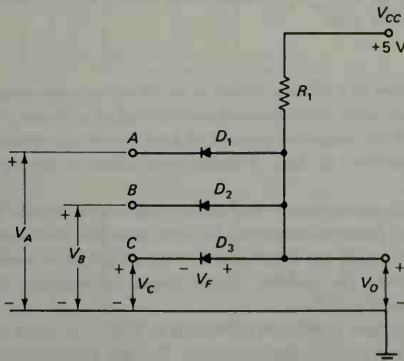
Figure 3-23. Circuit of a three-input diode AND gate.
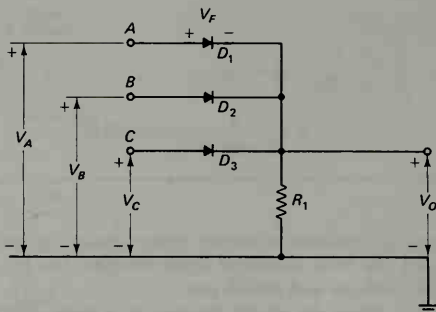
Figure 3-24. Circuit of a three-input diode OR gate.

The circuit diagram of a three-input terminal *OR gate* is shown in Fig. 3-24. Again, the gate could have two or more inputs. It is fairly obvious that the output voltage of the OR gate is *low* when all three inputs are low. Now suppose that a $+5$-V input is applied to terminal A, while terminals B and C remain grounded. Diode D_1 becomes forward biased, and its cathode voltage (i.e., the output voltage) is $+(5 \text{ V} - V_F)$. The output is *high*. Diodes D_2 and D_3 are reverse biased with $+V_0$ on the anodes and ground at the cathodes.

As its name implies, the OR gate produces a *high* output when a high input level is applied to terminal A *or* terminal B *or* terminal C.

Both AND and OR gates can be designed and constructed using discrete components. Alternatively, small integrated-circuit (IC) packages are available, each of which contain many diodes already fabricated in the form of the desired gate.

3-13
Diode Clipper
Circuits

The function of a clipper circuit is to *clip off* an unwanted portion of a waveform. A half-wave rectifier can be described as a clipper, since it passes only the positive (or negative) portion of an alternating waveform and clips off the other portion. In fact, a diode *series clipper* is simply a half-wave rectifier circuit.

Figure 3-25 shows *negative* and *positive series clipper circuits*. It is seen that in each case the diode is connected in *series* with the load resistor R_L. The negative clipper passes the positive half-cycle of the input and removes the negative half-cycle. The positive clipper passes the negative half-cycle and clips off the positive portion.

Two *shunt clipper circuits* are illustrated in Fig. 3-26. Here the diodes are connected in *shunt* (or parallel) with R_L. For the *negative shunt clipper*, Fig. 3-26(a), diode D_1 is reverse biased while the input is positive. Only a small volt drop occurs across R_1, due to the output current I_o. This means that the
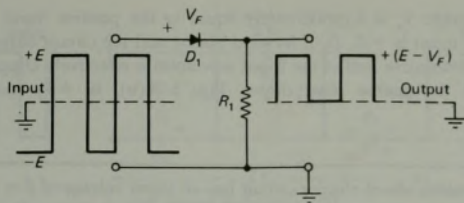
(a) Negative series clipper
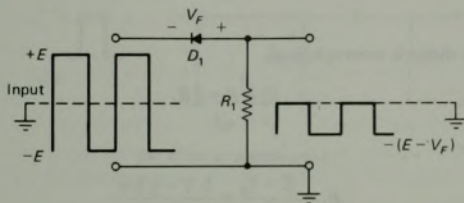
(b) Positive series clipper

Figure 3-25. Negative and positive series clipping circuits.
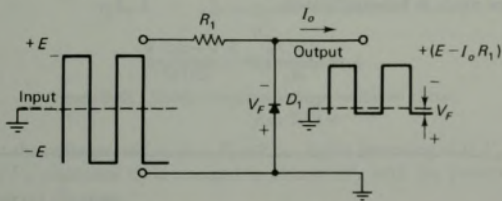
(a) Negative shunt clipper
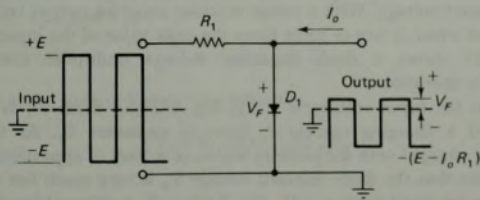
(b) Positive shunt clipper

Figure 3-26. Negative and positive shunt clipping circuits.

output voltage V_o is approximately equal to the positive input peak $+E$. When the input is $-E$, D_1 if forward biased and the circuit output becomes $-V_F$. The negative half of the input waveform is effectively clipped off. The output of the *positive shunt clipper*, Fig. 3-26(b), is $+V_F$ and $-E$, as illustrated.

Example 3-10   A positive shunt clipper circuit has an input voltage of $E = \pm 5$ V. The negative output voltage is to be -4.5 V when I_o is 2 mA. Determine the value of R_1, and specify the diode forward current and reverse voltage.

solution

When the diode is reverse biased,

$$V_0 = E - I_o R_1$$

Therefore,

$$R_1 = \frac{E - V_0}{I_o} = \frac{5 \text{ V} - 4.5 \text{ V}}{2 \text{ mA}}$$

$$= 250 \ \Omega$$

Diode reverse voltage is $V_R \simeq E = 5$ V.
When the diode is forward biased,

$$I_F \simeq \frac{E - V_F}{R_1} = \frac{5 \text{ V} - 0.7 \text{ V}}{250 \ \Omega}$$

$$= 17.2 \text{ mA}$$

3-14
Voltage
Multiplier
Circuit

The dc output voltage obtainable from an ordinary (half-wave or full-wave) rectifier circuit with a smoothing capacitor cannot be larger than the peak input voltage. With a *voltage multiplier circuit* an output voltage can be produced which is two or more times the peak value of the input voltage. Figure 3-27 shows a diode–capacitor voltage multiplier circuit and illustrates its operation.

When the input voltage is $+V_P$, Fig. 3-27(b), diode D_1 is forward biased, and a charging current I_1 flows to capacitor C_1. At this time C_1 becomes charged with the polarity shown to a level of approximately V_P. This assumes that the diode forward voltage V_F is very much less than V_P.

When the input goes to $-V_P$, Fig. 3-27(c), D_1 is reverse biased, and D_2 becomes forward biased. The voltage V_2 applied to the circuit of C_2 and D_2 is the sum of the input voltage $-V_P$ and V_{C1}. Note that the polarities are

(a) Voltage multiplier circuit

(b) Effect of positive input

(c) Effect of negative input
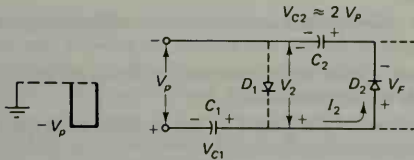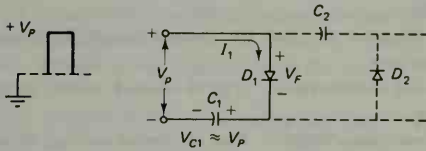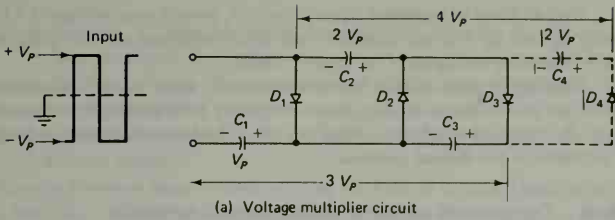
Figure 3-27. Diode–capacitor voltage multiplier circuit.

such that the voltages add to give $V_2 \simeq 2V_P$. Again assuming that V_F is much less than V_2, capacitor C_2 is charged to almost $2V_P$ with the polarity shown on the circuit diagram.

Now consider the effect on D_3 and C_3 when the input goes positive once again. Referring to Fig. 3-27(a), the voltage V_3 is the sum of $+V_P$ (at the input), V_{C1}, and V_{C2}.

$$V_3 = V_P + V_{C1} + V_{C2}$$

Taking careful note of the voltage polarities,

$$V_2 = V_P + (-V_P) + 2V_P$$
$$= 2V_P$$

Capacitor C_3 is charged to $2V_P$ with the polarity illustrated. The total voltage measured across capacitors C_1 and C_3 is now $3V_P$.

The addition of capacitor C_4 and diode D_4 gives a total voltage of $4V_P$ across C_2 and C_4. Further capacitor and diode additions produce progressively increasing multiples of the input voltage.

One application of this circuit is found in some pocket calculators which use gas-discharge display devices requiring perhaps 200 V to operate them. By means of a voltage multiplier circuit the low-level battery voltage is increased to the desired potential.

Glossary of Important Terms

Diode. Two-electrode device—a pn-junction with terminals.

Anode. Positive terminal for forward-biased diode—the p-side of a pn-junction.

Cathode. Negative terminal for forward-biased diode—the n-side of a pn-junction.

Diode forward characteristics. Plot of forward current versus forward-bias voltage.

Diode reverse characteristic. Plot of reverse current versus reverse-bias voltage.

Piecewise linear characteristic. Straight-line approximation of diode characteristic.

DC load line. Line plotted on diode characteristics to represent all circuit conditions.

Quiescent point. Point on characteristics at which device is biased, defined by device current and voltage.

Dynamic resistance. Reciprocal of the slope of a forward-biased diode characteristic beyond the knee.

Small-signal ac equivalent circuit. Equivalent circuit for forward-biased diode experiencing small changes in forward current.

Reverse saturation current. Small, temperature-dependent, constant current that flows across a reverse-biased junction.

Peak repetitive current. Maximum short-term forward current pulse that may be repeated continuously through a diode.

Half-wave rectifier. Diode circuit which passes only the positive (or negative) half-cycles of an alternating input voltage.

Full-wave rectifier. Diode circuit which converts an alternating input voltage to a continuous series of positive (or negative) half-cycles.

Bridge rectifier. Full-wave rectifier circuit using four diodes.

Capacitor smoothing circuit. Capacitor and resistor circuit employed to convert the output waveform of a rectifier to direct voltage.

Reservoir capacitor. Large capacitor used in a capacitor smoothing circuit.

Ripple. Small alternating voltage superimposed upon the direct voltage output of a capacitor smoothing circuit.

Peak repetitive current. Peak level of recurring pulse of current through a rectifier.

Surge current. Current which may flow through a rectifier for a short time when the supply is switched on.

Surge limiting resistor. Resistor connected in series with a rectifier to limit the surge current.

Average forward current. Average current flowing when a rectifier is forward biased.

Reverse recovery time. Time required for a diode to switch from *on* to *off*.

AND gate. Logic circuit which provides an output when inputs are present at terminals A and B and C, etc.

OR gate. Logic circuit which provides an output when an input is present at terminals A or B or C, etc.

Positive clipper. Clipper circuit which removes the positive portion of an input.

Negative clipper. Clipper circuit which removes the negative portion of an input.

Voltage multiplier circuit. Diode capacitor circuit which produces a direct output voltage which is a multiple of the supply voltage.

Review Questions

3-1. Sketch the symbol for a semiconductor diode, labeling the anode and cathode, and showing the polarity and current direction for forward bias. Also show the direction of movement of charge carriers when the device is (a) forward biased, and (b) reverse biased.

3-2. Sketch typical forward and reverse characteristics for a germanium diode and for a silicon diode. Discuss the characteristics, and show the effects of temperature change.

3-3. Draw the small-signal ac equivalent circuit for a forward-biased diode, and briefly explain its origin.

3-4. Sketch a half-wave rectifier circuit and a two-diode full-wave rectifier. Explain the operation of each and show the output waveforms that would result in each case for a sinusoidal ac input.

3-5. Sketch the circuit of a bridge rectifier and explain its operation. Show the output waveform that results from a sinusoidal ac input.

3-6. Sketch a capacitor smoothing circuit for use with a rectifier. Show the output waveform when the smoothing circuit is connected to (a) a half-wave rectifier, (b) a full-wave rectifier. In each case assume a sinusoidal input and explain the shape of the output waveform.

3-7. Define the following quantities: peak reverse voltage, reverse breakdown voltage, steady-state forward current, peak surge current, static reverse current, peak repetitive current, reverse recovery time.

3-8. Sketch the circuit of a diode AND gate. Briefly explain the circuit operation.

3-9. Repeat Question 3-8 for a diode OR gate.

3-10. Sketch the circuit of a positive series clipper circuit and show the input and output waveforms. Repeat for a negative series clipper.

3-11. Repeat Question 3-10 for a positive shunt clipper and for a negative shunt clipper.

3-12. Sketch a voltage multiplier circuit which will double the supply voltage. Briefly explain how the circuit operates and show how additional stages should be added to increase the voltage multiplying effect.

Problems

3-1. A diode having the characteristic shown in Fig. 3-28 is required to pass 75 mA from a supply of 5 V. Draw the dc load line and determine the resistance that must be connected in series with the diode. If the supply is reduced to 3.5 V, what will be the new value of I_F?
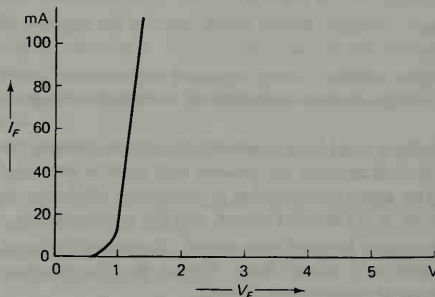
Figure 3-28.

3-2. A diode with the forward characteristic shown in Fig. 3-29 is connected in series with a 250-Ω resistance and a 5-V supply. Determine the diode current, and find the new current when the resistance is changed to 100 Ω.
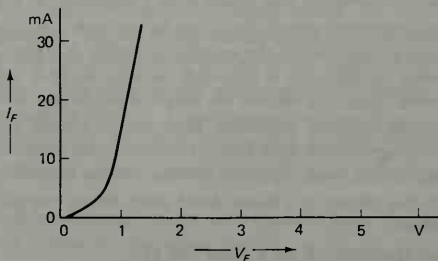
Figure 3-29.

3-3. A 60-V reverse bias is applied to a diode with the characteristics shown in Fig. 3-30. Determine the current that flows, and estimate the current level when the device temperature is increased by 10° C.
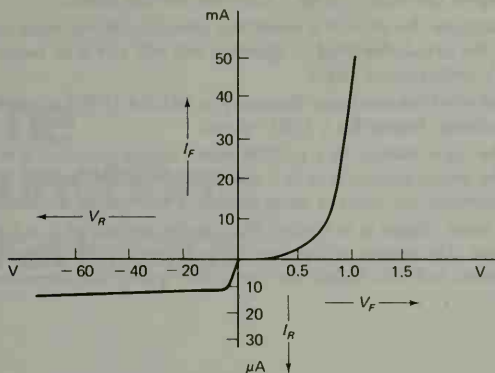
Figure 3-30.

3-4. Draw the piecewise linear characteristic for a silicon diode with a 3-Ω dynamic resistance and a maximum forward current of 75 mA.

3-5. For the diodes in Questions 3-3 and 3-4 draw the piecewise linear characteristics, and determine the values of dynamic resistance in each case.

3-6. A diode which has the characteristics shown in Fig. 2-11 is to pass a forward current of 20 mA when the supply is 1 V. Determine the value of resistance that must be connected in series with the diode. Also determine the level of forward current that flows when the resistance is doubled.

3-7. If the diode described in Question 3-6 is connected in series with a 1.5-V supply and a 20-Ω resistor, determine the current that flows (a) when the diode is forward biased, (b) when reverse biased.

3-8. A diode which has the characteristics given in Fig. 3-30 is employed as a half-wave rectifier. The series resistor R_L is 1 kΩ, and the input voltage amplitude is ± 50 V. Calculate the positive and negative amplitudes of the output waveform. Also calculate peak load current and diode peak power dissipation.

3-9. Determine the value of reservoir capacitor for a half-wave rectifier and smoothing circuit to supply 12 V to a 100-Ω load. Maximum ripple voltage amplitude is to be 20% of the average output voltage, and input frequency is 60 Hz.

3-10. Specify the diode required for the circuit described in Question 3-9.

Select a suitable device from the data sheets in Figs. 3-13 and 3-14. Also calculate the required value of the surge limiting resistance.

3-11. Repeat Question 3-9 for a full-wave rectifier circuit.

3-12. Repeat Question 3-10 for a full-wave rectifier circuit.

3-13. Calculate the value of a smoothing capacitor which, when connected to the circuit described in Question 3-8, will give a dc output with a 1-V peak-to-peak ripple.

3-14. Calculate the maximum frequency at which a 1N914 diode should be operated. Repeat for a 1N917 diode.

3-15. The input voltage to a positive shunt clipper circuit is $E = \pm 15$ V. The output current is to be 5 mA when the output voltage is -14 V. Determine the value of series resistance and specify the diode.

3-16. A shunt clipper is to remove the negative portion of a ± 7-V square wave. The output voltage is to be at least $+5.7$ V when the output current is 3 mA. Sketch the circuit and specify the components.

The Junction Transistor

A *bipolar junction transistor* (BJT) has two *pn*-junctions; thus, an understanding of its operation can be obtained by applying *pn*-junction theory. The currents that flow in a transistor are similar to those that flow across a single junction, and the transistor equivalent circuit is simply an extension of the *pn*-junction equivalent circuit. Since the transistor is a three-terminal device, there are three possible sets of current–voltage characteristics by which its performance may be specified.

4-1
Introduction

A junction transistor is simply a sandwich of one type of semiconductor material (*p*-type or *n*-type) between two layers of the other type. The cross-sectional view of a layer of *n*-type material between two layers of *p*-type is shown in Fig. 4-1(a). This is described as a *pnp transistor*. Figure 4-1(b) shows an *npn transistor*, consisting of a layer of *p*-type material between two layers of *n*-type. For reasons which will be understood later, the center layer is called the *base*, one of the outer layers is called the *emitter*, and the other outer layer is referred to as the *collector*. The emitter, base, and collector are

4-2
Transistor
Operation

65
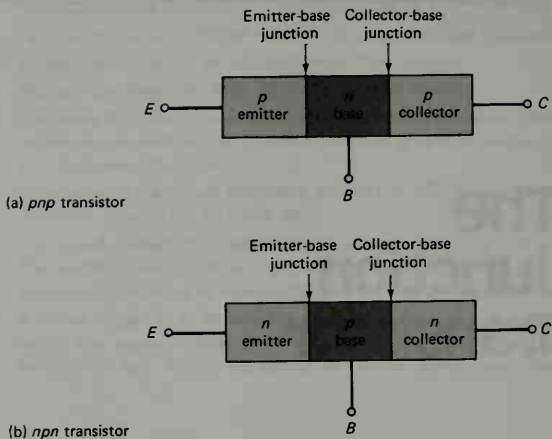
Figure 4-1. *pnp* and *npn* transistors.

provided with terminals which are appropriately labeled E, B, and C. Two *pn*-junctions exist within each transistor; the *collector–base junction* and the *emitter–base junction*. Each of these junctions has all the characteristics discussed in Chapters 2 and 3.

Figure 4-2(a) and (b) illustrates the depletion regions, barrier potentials, and electric fields at the junctions of *pnp* and *npn* transistors. These were originally explained in Section 2-2. Although it is not shown in the illustrations, the center layer in each case is made very much narrower than the two outer layers. Also, the outer layers are much more heavily doped than the center layer. This causes the depletion regions to penetrate deeply into the base, and thus the distance between the emitter–base (EB) and collector–base (CB) depletion regions is minimized. Note that the barrier potentials and electric fields are positive on the base and negative on the emitter and collector for the *pnp* device, and negative on the base and positive on the emitter and collector for the *npn* device.

Consider the *npn* transistor shown in Fig. 4-3. For normal (linear) transistor operation, the EB junction is forward biased and the CB junction is reverse biased. (Note the battery polarities). The forward bias at the EB junction causes electrons to flow from the *n*-type emitter to the *p*-type base. The electrons are "emitted" into the base region, hence the name *emitter*. Holes also flow from the *p*-type base to the *n*-type emitter, but since the base is much more lightly doped than the collector, almost all the current flow across the EB junction consists of electrons entering the base from the emitter. Therefore, electrons are the majority carriers in an *npn* device.

(a) pnp transistor

Depletion regions penetrating deeply into lightly doped base

Barrier potentials: positive on the n side, negative on the p side

Electric field at junction

(b) npn transistor

Depletion regions penetrating deeply into lightly doped base

Barrier potentials: positive on n side, negative on p side

Electric field at junctions
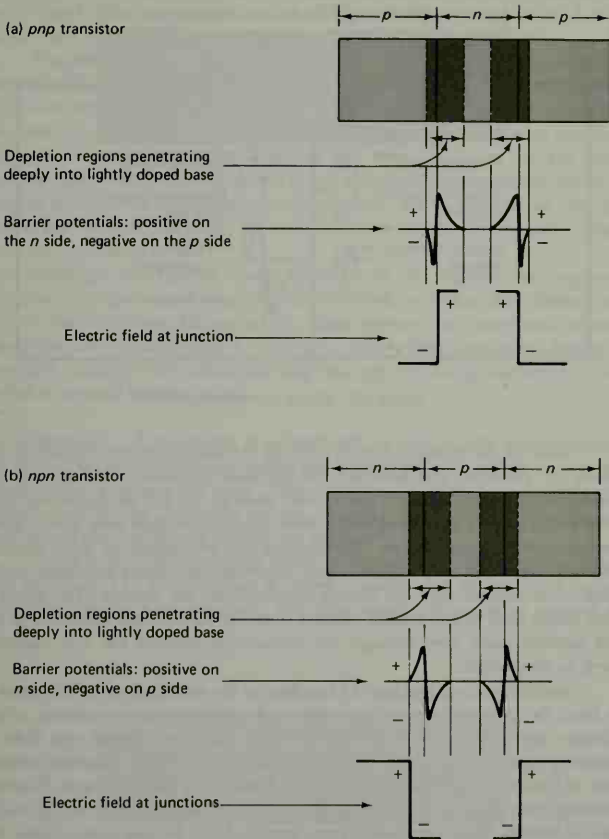
Figure 4-2. Barrier potentials and depletion regions for unbiased pnp and npn transistors.

The reverse bias at the CB junction causes the depletion region at that junction to be widened and to penetrate deeply into the base, as shown in Fig. 4-3. Thus, the electrons crossing from the emitter to the base arrive quite close to the negative–positive electric field at the CB depletion region. Since electrons have a negative charge, they are drawn across the CB junction by this electric field. They are "collected."
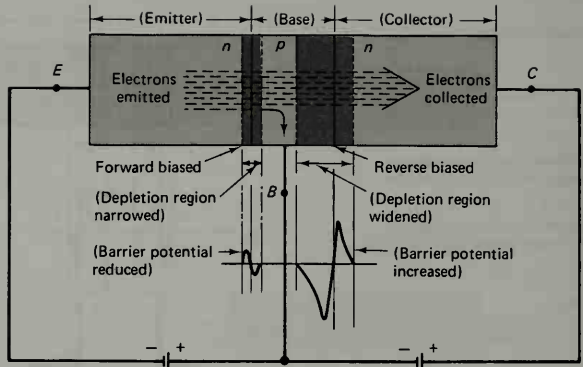
Figure 4-3. Biased *npn* transistor.

Some of the charge carriers entering the base from the emitter do not reach the collector, but flow out via the base connection and around the base–emitter bias circuit. However, the path to the CB depletion region is very much shorter than that to the base terminal, so that only a very small percentage of charge carriers flows out of the base terminal. Also, because the base region is very lightly doped, there are few holes available in the base to recombine with the charge carriers from the emitter. The result is that about 98% of the charge carriers from the emitter are collected at the CB junction, and flow through the collector circuit via the bias batteries back to the emitter.

Another way of looking at the effect of the reverse-biased CB junction is from the point of view of minority and majority charge carriers. It has already been shown that a reverse-biased junction opposes the flow of majority carriers and assists the flow of minority carriers. Majority carriers are, of course, holes coming from the *p*-side of a junction and electrons coming from the *n*-side. Minority carriers are holes coming from the *n*-side and electrons from the *p*-side (see Section 1-9). In the case of the *npn* transistor, the charge carriers arriving at the CB junction are electrons (from the emitter) traveling through the *p*-type base. Consequently, to the CB junction they appear as minority charge carriers, and the reverse bias assists them to cross the junction.

Since the EB junction is forward biased, it has the characteristics of a forward-biased diode. Substantial current will not flow until the forward bias is about 0.7 V for a silicon device or about 0.3 V for germanium. Reducing the level of the EB bias voltage in effect reduces the *pn*-junction forward bias and thus reduces the current that flows from the emitter through the base to the collector. Increasing the EB bias voltage increases this current. Reducing the bias voltage to zero, or reversing it, cuts the current off completely. Thus,

variation of the small forward-bias voltage on the EB junction controls the emitter and collector currents, and the EB controlling voltage source has to supply only the small base current.

The *pnp* transistor behaves exactly the same as an *npn* device, with the exception that the majority charge carriers are holes. As illustrated in Fig. 4-4, holes are emitted from the *p*-type emitter across the forward-biased EB junction into the base. In the lightly doped *n*-type base, the holes find few electrons to recombine with. Some of the holes flow out via the base terminal, but most are drawn across to the collector by the positive–negative electric field at the reverse-biased CB junction. As in the case of the *npn* device, the forward bias at the EB junction controls the collector and emitter currents.

Although one type of charge carrier is in the majority, two types of charge carrier (holes and electrons) are involved in current flow through an *npn* or *pnp* transistor. Consequently, these devices are sometimes termed *bipolar junction transistors* (BJT). This is to distinguish them from *field-effect transistors* (Chapter 12), which use only one type of charge carriers and are therefore termed *unipolar devices*.

To Summarize: A transistor is a sandwich of *pnp* or *npn* semiconductor material. The outer layers are called the emitter and the collector, and the center layer is termed the base. Two junctions are formed, with depletion regions and barrier potentials set up at each. The barrier potentials are negative on the *p*-side and positive on the *n*-side.

The EB junction is forward biased, so that charge carriers are emitted into the base. The CB junction is reverse biased, and its depletion region penetrates deeply into the base. The base section is made as narrow as
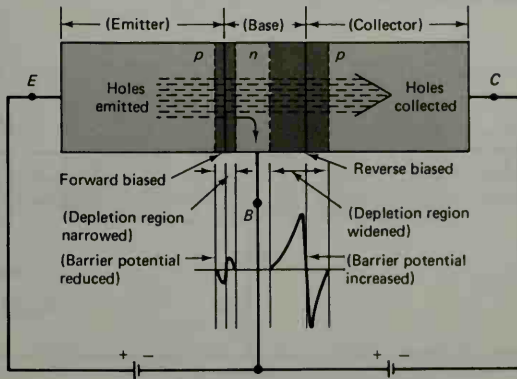
Figure 4-4. Biased *pnp* transistor.

possible so that charge carriers can easily move across from emitter to collector. The base is also lightly doped, so that few charge carriers are available to recombine with the majority charge carriers from the emitter. Most charge carriers from the emitter flow out through the collector; few flow out through the base. Variation of the EB junction bias voltage alters the base, emitter, and collector currents.

4-3
Transistor
Currents

The various current components which flow within a transistor are once again illustrated in Fig. 4-5. The current flowing into the emitter terminal is referred to as the *emitter current* and identified as I_E. For the *pnp* device shown, I_E can be thought of as a flow of holes from the emitter to the base. Note that the indicated I_E direction external to the transistor is the conventional current direction. *Base current* I_B and *collector current* I_C are also shown external to the transistor as conventional current direction. Both I_C and I_B flow out of the transistor while I_E flows into the transistor. Therefore,

$$I_E = I_C + I_B \qquad (4\text{-}1)$$

As already discussed, almost all of I_E crosses to the collector, and only a small portion flows out of the base terminal. The portion of I_E which flows across the collector–base junction is designated $\alpha_{dc}I_E$, where α_{dc}(alpha dc) is typically 0.96 to 0.99.Thus,α_{dc} I_E is typically 96% to 99% of I_E.

Because the CB junction is reverse biased, a very small reverse saturation current flows across the junction. This is shown as I_{CBO} in Fig. 4-5, and it is termed the *collector-to-base leakage current*. I_{CBO} is made up of minority charge carriers, which in the case of a *pnp* device are holes moving from the n-type base to the p-type collector.
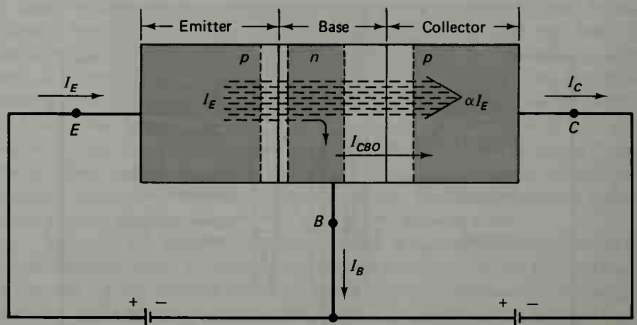
Figure 4-5. Currents in a *pnp* transistor.

The collector current is obviously the sum of $\alpha_{dc}I_E$ and I_{CBO}:

$$I_C = \alpha_{dc}I_E + I_{CBO} \qquad (4\text{-}2)$$

Rearranging Eq. (4-2),

$$\alpha_{dc} = \frac{I_C - I_{CBO}}{I_E} \qquad (4\text{-}3)$$

Since I_{CBO} is very much smaller than I_C, an approximation for α_{dc} is

$$\alpha_{dc} \approx \frac{I_C}{I_E} \qquad (4\text{-}4)$$

Therefore, α_{dc} is approximately the ratio of collector current to emitter current. α_{dc} is also referred to as the *common base current gain factor*. When using *h-parameters* (Section 4-9), the designation h_{FB} may be employed instead of α_{dc}.

Using Eq. (4-1) to substitute for I_E into Eq. (4-2),

$$I_C = \alpha_{dc}(I_C + I_B) + I_{CBO}$$
$$= \alpha_{dc}I_C + \alpha_{dc}I_B + I_{CBO}$$
$$I_C(1 - \alpha_{dc}) = \alpha_{dc}I_B + I_{CBO}$$

or

$$I_C = \frac{\alpha_{dc}I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}} \qquad (4\text{-}5)$$

All the foregoing formulas are just as valid for an *npn* transistor as for a *pnp* device.

Calculate the values of collector current and emitter current for a transistor with $\alpha_{dc} = 0.98$ and $I_{CBO} = 5$ μA. The base current is measured as 100 μA.

Example 4-1

solution

From Eq. (4-5),

$$I_C = \frac{\alpha_{dc}I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}}$$

Therefore,

$$I_C = \frac{0.98 \times 100 \ \mu A}{1 - 0.98} + \frac{5 \ \mu A}{1 - 0.98}$$
$$= 4.9 \ mA + 0.25 \ mA = 5.15 \ mA$$

From Eq. (4-1),

$$I_E = I_C + I_B$$

Therefore,

$$I_E = 5.15 \ mA + 100 \ \mu A = 5.25 \ mA$$

According to Eq. (4-4), the ratio of I_C to I_E should approximately equal α_{dc}. Checking: $5.15 \ mA / 5.25 \ mA \approx 0.98$.

Equation (4-5) may be written as

$$I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO} \qquad (4\text{-}6)$$

where $\beta_{dc} = \alpha / (1 - \alpha)$. Because I_{CBO} is very much less than I_B, an approximation for Eq. (4-6) is $I_C \approx \beta_{dc} I_B$. Therefore,

$$\beta_{dc} \approx \frac{I_C}{I_B} \qquad (4\text{-}7)$$

Thus, β_{dc} (beta$_{dc}$) is approximately the ratio of collector current to base current. β_{dc} is also referred to as the *dc common emitter current gain factor*, and the designation h_{FE} (Section 4-9) is frequently used instead of β_{dc}.

Example 4-2   The collector and base currents of a certain transistor are measured as

$$I_C = 5.202 \ mA, \qquad I_B = 50 \ \mu A, \qquad I_{CBO} = 2 \ \mu A$$

(a) Calculate α_{dc}, β_{dc}, and I_E.
(b) Determine the new level of I_B required to make $I_C = 10 \ mA$.

solution (a)

From Eq. (4-6), $I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO}$.

$$\text{Therefore,} \quad 5.202 \ mA = (\beta_{dc} \times 50 \ \mu A) + (\beta_{dc} + 1) 2 \ \mu A$$
$$= \beta_{dc} (50 \ \mu A + 2 \ \mu A) + 2 \ \mu A$$

$$\beta_{dc} = \frac{5.202 \text{ mA} - 2 \text{ } \mu A}{52 \text{ } \mu A} = 100$$

From Eq. (4-1), $I_E = I_C + I_B$.

Therefore, $I_E = 5.202 \text{ mA} + 50 \text{ } \mu A = 5.252 \text{ mA}$

From Eq. (4-2), $I_C = \alpha_{dc} I_E + I_{CBO}$.

Therefore, $5.202 \text{ mA} = (\alpha_{dc} \times 5.252 \text{ mA}) + 2 \text{ } \mu A$

$$\alpha_{dc} = \frac{5.202 \text{ mA} - 2 \text{ } \mu A}{5.252 \text{ mA}} = 0.99$$

solution (b)

From Eq. (4-6), $I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO}$.

Therefore, $10 \text{ mA} = (100 \times I_B) + (101 \times 2 \text{ } \mu A)$

$$I_B = \frac{10 \text{ mA} - 202 \text{ } \mu A}{100} = 97.98 \text{ } \mu A$$

The symbols employed for *npn* and *pnp* transistors are shown in Fig. 4-6(a) and (b). The arrowhead is always at the emitter terminal, and in each case its direction *indicates the conventional direction of current flow*. For the *npn* transistor, the arrowhead points from the *p*-type base to the *n*-type emitter terminal. For the *pnp* transistor, it points from the *p*-type emitter toward the *n*-type base terminal. Thus, the arrowhead is always from *p* to *n*.

The bias and supply voltage polarities for *npn* and *pnp* transistors are shown in Fig. 4-7. As was the case with the transistor type, the bias polarities are indicated by the arrowhead direction. For an *npn* transistor [Fig. 4-7(a)]

4-4
Transistor
Symbols
and Voltages

(a) *npn* transistor symbol (b) *pnp* transistor symbol

n-type collector

p-type base

n-type emitter

Arrowhead is in conventional current direction, from *p* to *n*

p-type collector

n-type base

p-type emitter
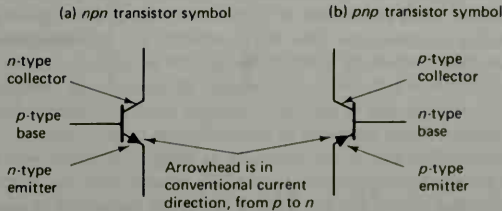
Figure 4-6. Transistor symbols.

(a) *npn* bias polarities   (b) *pnp* bias polarities
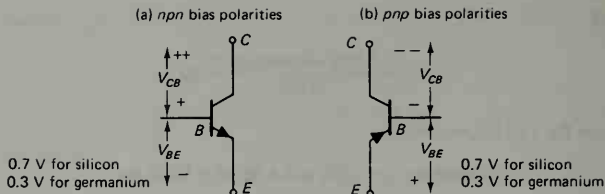
Figure 4-7. Transistor bias voltage polarities.

the base is biased positive with respect to the emitter, and the arrowhead points from the (positive) base to the (negative) emitter. The collector is then biased to a higher positive level than the base. For a *pnp* device [Fig. 4-7(b)], the base is negative with respect to the emitter. The arrowhead points from the (positive) emitter to the (negative) base, and the collector is then more negative than the base.

Typical base–emitter voltages for both *npn* and *pnp* transistors are 0.7 V for silicon and 0.3 V for germanium. Typical collector-to-base voltages might be anything from 0 to 20 V for most types of transistors, although in many cases the collector-to-base voltage may be greater than 20 V.

The transistor is normally operated with its CB junction reverse biased and its BE junction forward biased. In the case of a switching transistor (i.e., a transistor that is not operated as an amplifier but is either switched *on* or *off*), the CB junction may become forward biased, but only by about 0.5 V. Also in transistor switching circuits (and some others) the BE junction can become reverse biased. Most transistors will not survive more than about 5 V of reverse bias on the BE junction.

4-5
Common
Base
Characteristics

4-5.1
*Common
Base
Circuit
Connection*

To investigate the characteristics of a two-terminal device (such as a diode), several levels of forward or reverse bias voltage are applied and the corresponding currents that flow are measured. The characteristics of the device are then derived by plotting the graphs of current against voltage. Since a transistor is a three-terminal device, there are three possible configurations in which it may be connected to study its characteristics. From each of these configurations three sets of characteristics may be derived.

Consider Fig. 4-8. A *pnp* transistor is shown connected with its base terminal common to both the input (EB) voltage and the output (CB) voltage. For this reason, the transistor is said to be connected in *common base* configuration. Voltmeters and ammeters are connected to measure input and output voltages and currents.
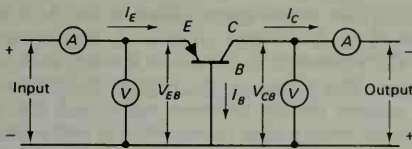
Figure 4-8. Circuit for determining common base characteristics.

To determine the input characteristics, the output (CB) voltage is maintained constant, and the input (EB) voltage is set at several convenient levels. For each level of input voltage, the input current I_E is recorded. I_E is then plotted versus V_{EB} to give the *common base input characteristics* shown in Fig. 4-9.

Since the EB junction is forward biased, the common base input characteristics are essentially those of a forward biased *pn* junction. Figure 4-9 also shows that for a given level of input voltage more input current flows when higher levels of CB voltage are employed. This is because larger CB (reverse bias) voltages cause the depletion region at the CB junction to penetrate deeper into the base of the transistor, thus shortening the distance and the resistance between the EB and CB depletion regions.

*4-5.2
Input
Characteristics*

The emitter current (I_E) is held constant at each of several fixed levels. For each fixed level of I_E, the output voltage (V_{CB}) is adjusted in convenient steps, and the corresponding levels of collector current (I_C) are recorded. In this way, a table of values is obtained from which a family of output characteristics may be plotted. In Fig. 4-10 the corresponding I_C and V_{CB} values obtained when I_E was held constant at 1 mA are plotted, and the resultant characteristic is identified as $I_E = 1$ mA. Similarly, other characteristics are plotted for $I_E = 2$ mA, 3 mA, etc.

*4-5.3
Output
Characteristics*
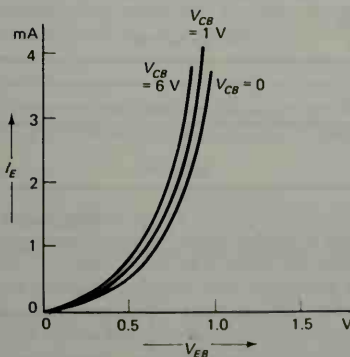
Figure 4-9. Common base input characteristics.

The common base output characteristics in Fig. 4-10 show that for each fixed level of I_E, I_C is almost equal to I_E and appears to remain constant when V_{CB} is increased. In fact, there is a very small increase in I_C with V_{CB} increase. This is because the increase in collector-to-base bias voltage (V_{CB}) expands the CB depletion region, and thus shortens the distance between the two depletion regions. With I_E held constant, however, the I_C increase is so small that it is usually noticeable only for large V_{CB} variations.

As shown in Fig. 4-10, when V_{CB} is reduced to zero I_C still flows. Even when the externally applied bias voltage is zero, there is still a barrier potential existing at the CB junction, and this assists the flow of I_C. The charge carriers which make up I_C constitute minority carriers as they cross the CB junction. Thus, the reverse-bias voltage (V_{CB}) and the (unbiased) CB barrier potential assist the flow of the I_C charge carriers. To stop the flow of charge carriers the CB junction has to be forward biased. Consequently, as illustrated, I_C is reduced to zero only when V_{CB} is increased positively. The region of the graph for CB forward biased is known as the *saturation region* (Fig. 4-10). The region in which the junction is reverse biased is named the *active region*, and this is the region in which a transistor is normally operated.

If the reverse-bias voltage on the CB junction is allowed to exceed the maximum safe limit specified by the manufacturer, device breakdown may occur. Breakdown, illustrated by the broken lines on Fig. 4-10, can be caused by either (or both) of two effects. One of these is the same effect which causes diode breakdown. The other effect is the result of the CB depletion region penetrating into the base until it makes contact with the EB depletion region. This condition is known as *punch through* or *reach through*. When it occurs large currents can flow, possibly destroying the device. The extension of the depletion region is, of course, the direct result of increase in
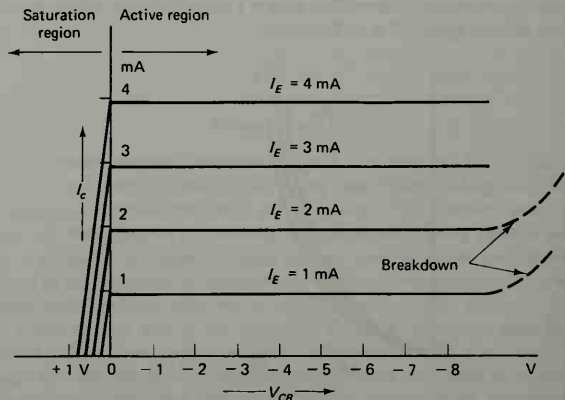
Figure 4-10. Common base output characteristics (or collector characteristics).
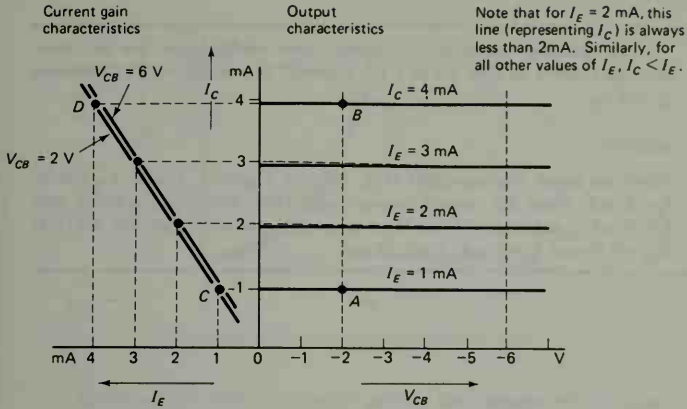
Figure 4-11. Derivation of common base current gain characteristics.

V_{CB}. Therefore, it is very important to maintain V_{CB} below the maximum safe limit specified by the device manufacturer.

The *current gain characteristics* (also referred to as *forward transfer characteristics*) (Fig. 4-11) are obtained experimentally by holding V_{CB} fixed at a convenient level, and recording the I_C levels measured for various settings of I_E. I_C is then plotted versus I_E, and the resultant graph is identified according to the V_{CB} level.

The current gain characteristics can also be derived from the common base output characteristics as illustrated in Fig. 4-11. A vertical line is drawn through a selected value of V_{CB}, and corresponding values of I_E and I_C are read off along this line. The values of I_C are then plotted versus I_E, and the characteristic is labeled with the V_{CB} employed.

From the common base output characteristics shown in Fig. 4-11, **Example 4-3** derive the current gain characteristics for $V_{CB} = 2$ V and for $V_{CB} = 6$ V.

solution

On the output characteristics draw a vertical line at $V_{CB} = 2$ V (Fig. 4-11). Where the line intersects the output characteristics at point A, read $I_C = 0.95$ mA for $I_E = 1$ mA. Now plot point C at $I_C = 0.95$ mA on the vertical axis and $I_E = 1$ mA on the lefthand horizontal axis. Returning to the output characteristics, read $I_C = 3.95$ mA at $I_E = 4$ mA and $V_{CB} = 2$ V, point B. Now plot point D at $I_C = 3.95$ mA on the vertical axis and $I_E = 4$ mA on the horizontal axis. Draw a line through points C and D to give the current gain characteristic for $V_{CB} = 2$ V. Repeat the above procedure for $V_{CB} = 6$ V.

Example 4-4   A transistor connected in common base configuration has the characteristics shown in Figs. 4-9 to 4-11. $V_{EB} = 0.7$ V and $V_{CB} = 6$ V. Determine I_E and I_C.

solution

From the input characteristics (Fig. 4-9), at $V_{BE} = 0.7$ V and $V_{CB} = 6$ V, $I_E \approx 2$ mA. From the output characteristics (Fig. 4-10), at $V_{CB} = 6$ V and $I_E = 2$ mA, $I_C \approx 1.95$ mA. From the current gain characteristics (Fig. 4-11), at $V_{CB} = 6$ V and $I_E = 2$ mA, $I_C \approx 1.95$ mA.

4-6
Common Emitter Characteristics

4-6.1
Common Emitter Circuit Connection

Figure 4-12 shows the circuit employed for determining transistor common emitter characteristics. The input voltage is applied between B and E terminals, and the output is taken at C and E terminals. Therefore, the E terminal is common to both input and output. Input and output voltages and currents are measured by voltmeters and ammeters as shown.

4-6.2
Input Characteristics

To determine the input characteristics, V_{CE} is held constant, and I_B levels are recorded for several levels of V_{BE}. I_B is then plotted versus V_{BE}, as shown in Fig. 4-13. It can be seen that the common emitter input characteristics (like the common base input characteristics) are those of a forward-biased pn-junction. However, I_B is only a small portion of the total current (I_E) which flows across the forward-biased BE junction. Figure 4-13 also shows that, for a given vlaue of V_{BE}, less I_B flows when higher levels of V_{CE} are employed. This is because the higher levels of V_{CE} provide greater CB junction reverse bias, resulting in greater depletion region penetration into the base, and causing the distance between the CB and EB depletion regions to be shortened. Consequently, more of the charge carriers from the emitter flow across the CB junction and fewer flow out via the base terminal.
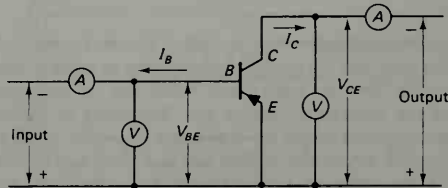
Figure 4-12. Circuit for determining common emitter characteristics.
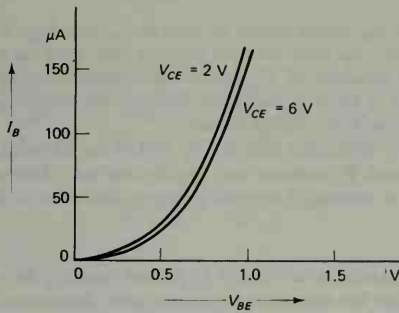
Figure 4-13. Common emitter input characteristics.

To determine a table of values for plotting the common emitter output characteristics, I_B is maintained constant at several convenient levels. At each fixed level of I_B, V_{CE} is adjusted in steps, and the corresponding values of I_C are recorded. For each level of I_B, I_C is plotted versus V_{CE}. This gives a family of characteristics which are typically as illustrated in Fig. 4-14.

Since I_E is not held constant, as in the case of the common base output characteristics, the shortening of the distance between the depletion regions (when V_{CE} is increased) draws more charge carriers from the emitter to the collector. Thus, I_C increases to some extent with increase in V_{CE}, and the slope of the common emitter characteristics is much more pronounced than that of the common base characteristics. Also, note that I_C now reduces to zero when V_{CE} becomes zero. This is because the voltage plotted on the
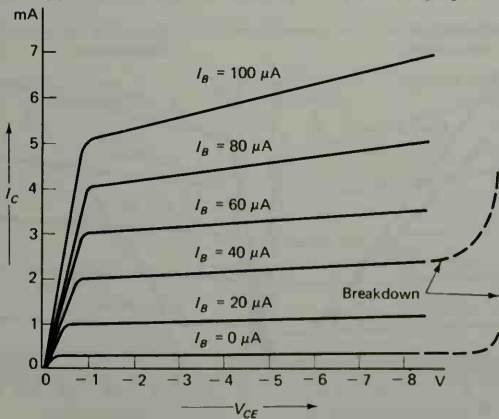
Figure 4-14. Common emitter output characteristics (or collector characteristics).

horizontal axis is V_{CE}, which equals the sum of V_{CB} and V_{BE}. At the "knee" of the characteristic, the collector–base junction bias (V_{CB}) has been reduced to zero. Further reduction in V_{CE} causes the collector–base junction to be forward biased. The forward bias repels the minority charge carriers which constitute I_C, and so I_C is reduced to zero.

As shown by the broken lines in Fig. 4-14, if the CE voltage exceeds a maximum safe level, I_C increases very rapidly and may destroy the device. As in the case of common base configuration, this effect is due to *punch through*.

**4-6.4
Current Gain
Characteristics**

These characteristics are simply I_C plotted versus I_B for various fixed values of V_{CE}. Like the common base current gain characteristics, they can be obtained experimentally or determined from the output characteristics. To experimentally obtain the required table of values, V_{CE} is held at a selected level, and the base current (I_B) is adjusted in convenient steps. At each step of I_B, the value of I_C is observed and recorded. Figure 4-15 shows the derivation of the current gain characteristics from the common emitter output characteristics. The procedure is exactly the same as for the common base current gain characteristics, with the exception that I_C is plotted against I_B instead of I_E.

Example 4-5

Determine the value of I_B and I_C for a device with the characteristics shown in Figs. 4-13 to 4-15 when V_{BE} is 0.7 V and $V_{CE} = 6$ V. Also calculate the transistor β value.
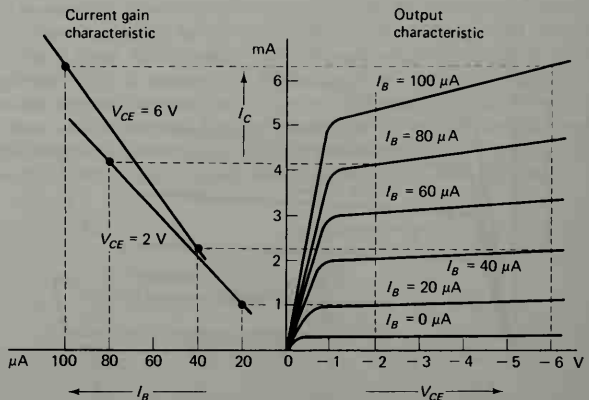
Figure 4-15. Derivation of common emitter current gain characteristics.

solution

From the input characteristics (Fig. 4-13), when $V_{BE} = 0.7$ V and $V_{CE} = 6$ V, $I_B \approx 60$ μA. From the output characteristics (Fig. 4-14), when $V_{CE} = 6$ V and $I_B = 60$ μA, $I_C \approx 3.3$ mA. From the current gain characteristics (Fig. 4-15), when $V_{CE} = 6$ V and $I_B = 60$ μA, $I_C \approx 3.3$ mA. The current gain value at this point is

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{3.3 \text{ mA}}{60 \text{ μA}} = 55$$

In the circuit arrangement of Fig. 4-16 the collector terminal is common to both input CB voltage and output CE voltage. Using this circuit, the common collector input, output, and current gain characteristics can be determined. The output and current gain characteristics are shown in Fig. 4-17. The common collector output characteristics are I_E plotted versus V_{CE} for several fixed values of I_B. The common collector current gain characteristics are I_E plotted versus I_B for several fixed values of V_{CE}.
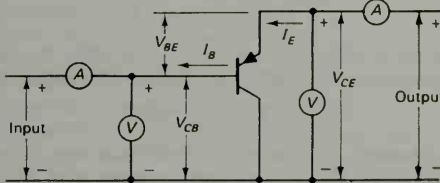
Figure 4-16. Circuit for determining common collector characteristics.
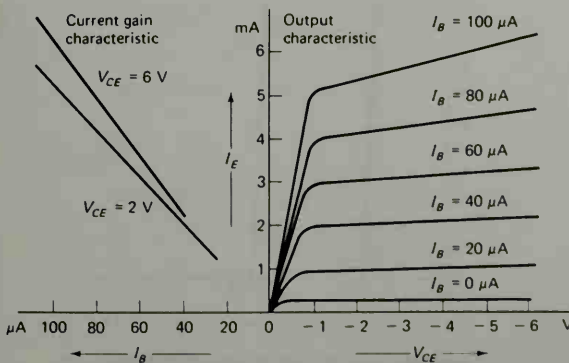
Figure 4-17. Common collector output and current gain characteristics.

It will be recalled that the common emitter output characteristics are I_C plotted against V_{CE}, and that the common emitter current gain characteristics are I_C plotted against I_B. Since I_C is approximately equal to I_E, the common collector output and current gain characteristics are practically identical to those of the common emitter circuit.

The common collector input characteristics illustrated in Fig. 4-18 are quite different from either common base or common emitter input characteristics. The difference is due to the fact that the input voltage V_{CB} is largely determined by the level of CE voltage (Fig. 4-16). This is because when the transistor is biased on V_{BE} will remain around 0.7 V for a silicon transistor (0.3 V for germanium), and V_{CE} may be much larger than 0.7 V. From Fig. 4-16,

$$V_{CE} = V_{CB} + V_{BE}$$

or

$$V_{BE} = V_{CE} - V_{CB}$$

Consider the characteristic for $V_{CE} = 2$ V (Fig. 4-18). At $I_C = 100$ μA (point 1), $V_{CB} \approx 1.3$ V and

$$V_{BE} = V_{CE} - V_{CB}$$
$$= 2 \text{ V} - 1.3 \text{ V} = 0.7 \text{ V}$$

Now suppose V_{CE} is maintained constant at 2 V while the input voltage (V_{CB}) is increased to 1.5 V (point 2). The base–emitter voltage becomes

$$V_{BE} = 2 \text{ V} - 1.5 \text{ V} = 0.5 \text{ V}$$

Because V_{BE} is reduced, I_B is reduced from 100 μA to zero.

Similarly, when V_{CE} is maintained constant at 4 V and V_{CB} is increased from 3.3 to 3.5 V, I_B is reduced from 100 μA to zero.
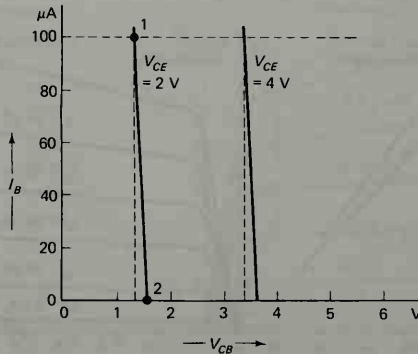
Figure 4-18. Common collector input characteristics.

A transistor consists of two pn-junctions with a common center block. Therefore, to represent a transistor equivalent circuit, it should be possible to use two pn-junction equivalent circuits. This has been done in Fig. 4-19, with the exception that r_c now represents the CB junction resistance, r_e represents the BE junction resistance, and r_b represents the resistance of the base region which is common to both junctions. Junction capacitances C_{BE} and C_{BC} are also included.

If the transistor equivalent circuit were simply left as a combination of resistances and capacitances, it could not account for the fact that most charge carriers from the emitter flow out of the collector terminal. To accommodate this phenomenon, a current generator is included in parallel with r_c and C_{BC}. The current generator is given the value αI_e, where $\alpha = I_c / I_e$.

Since an input voltage would be applied between B and E, and the output taken across C and B, the circuit of Fig. 4-19 is a *common base* equivalent circuit. The equivalent circuit could easily be rearranged in common emitter or common collector configuration. *Note that the currents are designated I_b, I_c, and I_e instead of I_B, I_C, and I_E. This indicates that the quantities involved are ac quantities rather than dc; i.e., we are considering current variations rather than steady-state quantities. In the T-equivalent circuit the parameters r_c, r_b, r_e, and α are also ac parameters.*

Referring to Fig. 4-19, r_e represents the ac resistance of the forward-biased BE junction. Therefore, r_e is fairly small. On the other hand, r_c represents the resistance of the CB junction, which is normally reverse biased for transistor operation. Therefore, r_c has a high value. The resistance of the base region represented by r_b depends upon the doping density of the base material. Usually, r_b is larger than r_e, but very much smaller than r_c.
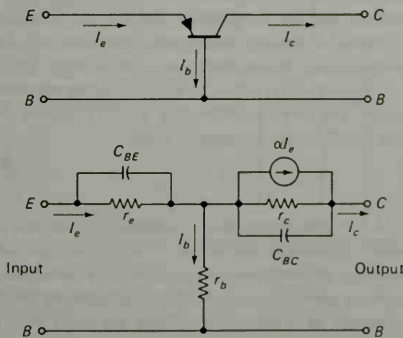
Figure 4-19. T-equivalent circuit of transistor (common base).
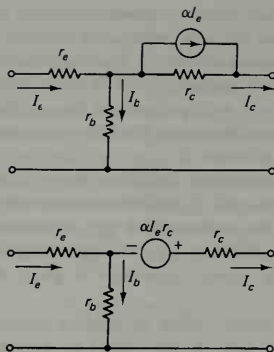
Figure 4-20. Transistor low-frequency ac equivalent circuits.

Typical values for the resistive components are

$$r_e = 25 \ \Omega$$

$$r_b = 100 \text{ to } 300 \ \Omega$$

$$r_c = 1 \text{ M}\Omega$$

The BE junction capacitance (C_{BE}) is the capacitance of a forward-biased pn-junction, and the CB capacitance (C_{CB}) is that of a reverse-biased junction. At medium and low frequencies the junction capacitances may be neglected. Also, instead of having the current generator (αI_e) in parallel with r_c, a voltage generator may be employed in series with r_c. The voltage of this generator is $\alpha I_e r_c$. Two circuits, either of which may be employed at medium and low frequencies, are now available (Fig. 4-20). They are each referred to as the *T-equivalent circuit*, or the *r-parameter circuit*.

4-9
h-Parameters

In Section 4-8 it was shown that transistor circuits can be represented by an *r*-parameter equivalent circuit (or T-equivalent circuit). In circuits involving more than a single transistor, analysis by *r*-parameters can become extremely difficult. A more convenient set of parameters for circuit analysis is the *hybrid parameters* or *h-parameters*. These are used only for ac circuit analysis, although dc current gain factors are also expressed as *h*-parameters.

In Fig. 4-21 a common emitter h-parameter equivalent circuit is compared with a common emitter r-parameter equivalent circuit. In each case a load resistance R_L is included, as well as a signal source V_s and R_s.

The input to the h-parameter circuit is represented as an input resistance h_{ie} in series with a voltage $h_{re} \times V_{ce}$. Looking at the r-parameter circuit, it is seen that a change in output current I_c causes a voltage variation across r_e, i.e., a voltage *fed back* to the input. In the h-parameter circuit this feedback voltage is represented as a portion (h_{re}) of the output voltage V_{ce}.

The output of the h-parameter circuit is represented as an output resistance $1/h_{oe}$ in parallel with a current generator $h_{fe} \times I_b$, where I_b is the base current variation, or ac base current. Therefore, $h_{fe}I_b$ is produced by the input current I_b, and it divides between the device output resistance and the load R_L. I_c is shown as the current passed to R_L. Again, looking at the r-parameter equivalent circuit, it is seen that all the generator current (αI_e) does not flow out through the load resistor; part of it flows through r_c.

The h-parameter equivalent circuit separates the input and output parts of the circuit, and consequently simplifies circuit analysis.
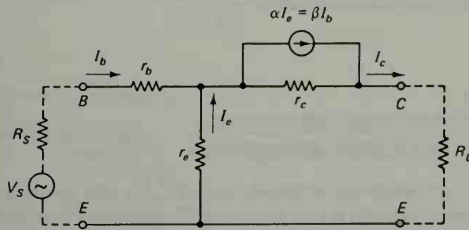
Common emitter r-parameter
equivalent circuit
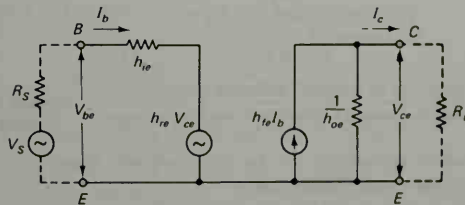
Common emitter h-parameter
equivalent circuit

Figure 4-21. Comparison of r-parameter and h-parameter equivalent circuits.

Definition of the Common Emitter h-Parameters.

h_{ie} = input resistance = $\dfrac{\Delta V_{BE}}{\Delta I_B}\bigg|_{V_{CE}}$

$\quad = \dfrac{V_{be}}{I_b}\bigg|_{V_{CE}}$ \quad (using ac quantities)

$\quad$ = ratio of $\dfrac{\text{variation in (input) base emitter voltage}}{\text{variation in (input) base current}}$ \quad (when V_{CE} is held constant)

h_{re} = reverse voltage transfer ratio = $\dfrac{\Delta V_{BE}}{\Delta V_{CE}}\bigg|_{I_B}$

$\quad = \dfrac{V_{be}}{V_{ce}}\bigg|_{I_B}$

$\quad = \dfrac{\text{variation in (input) base emitter voltage}}{\text{variation in (output) collector to emitter voltage}}$ \quad (when I_B is held constant)

h_{fe} = forward current transfer ratio = $\dfrac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}}$

$\quad = \dfrac{I_c}{I_b}\bigg|_{V_{CE}}$

$\quad = \dfrac{\text{variation in (output) collector current}}{\text{variation in (input) base current}}$ \quad (when V_{CE} is held constant).

The dc forward current transfer ratio (β_{dc}) is also written as h_{FE}. Note that to indicate that this is a dc parameter the subscript FE is used instead of fe.

h_{oe} = output conductance = $\dfrac{\Delta I_C}{\Delta V_{CE}}\bigg|_{I_B}$

$\quad = \dfrac{I_c}{V_{ce}}\bigg|_{I_B}$ \quad (in siemens (S))

$\quad = \dfrac{\text{variation in (output) collector current}}{\text{variation in (output) collector to emitter voltage}}$ \quad (when I_B is held constant)

The above parameters can be experimentally determined or can be derived from the device characteristics.

Example 4-6
For the common emitter output and current gain characteristics shown in Fig. 4-22, determine the value of h_{oe} and h_{fe} when $I_c = 3.5$ mA and $V_{CE} = 4.5$ V.
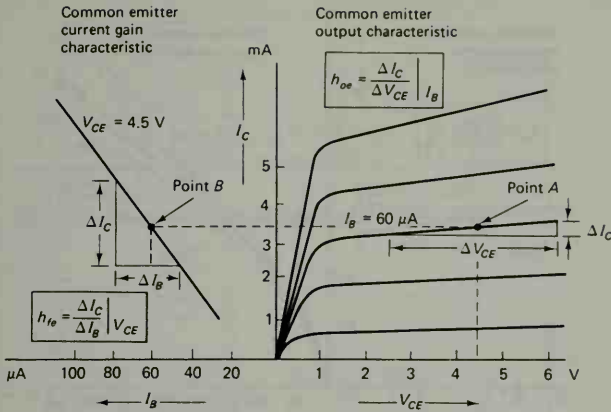
Figure 4-22. Derivation of h_{oe} and h_{fe} from characteristics.

solution

From the *output characteristics*,

$$\frac{\Delta I_C}{\Delta V_{CE}}\bigg|_{I_B} = h_{oe} = \text{output conductance}$$

From the *current gain characteristics*,

$$\frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}} = h_{fe} = \text{forward current transfer ratio}$$

From point A on Fig. 4-22, at $I_C = 3.5$ mA and $V_{CE} = 4.5$ V,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}\bigg|_{(I_B = 60\ \mu A)} \approx \frac{0.35\ \text{mA}}{3.5\ \text{V}} = 1 \times 10^{-4}\text{S}$$

From point B on Fig. 4-22, at $I_C = 3.5$ mA and $V_{CE} = 4.5$ V,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{(V_{CE} = 4.5\ V)} \approx \frac{2.1\ \text{mA}}{35\ \mu A} = 60$$

From the common emitter input and reverse transfer characteristics, determine the values of h_{ie} and h_{re} for $V_{CE} = 4.5$ V and $I_C = 3.5$ mA.

Example 4-7
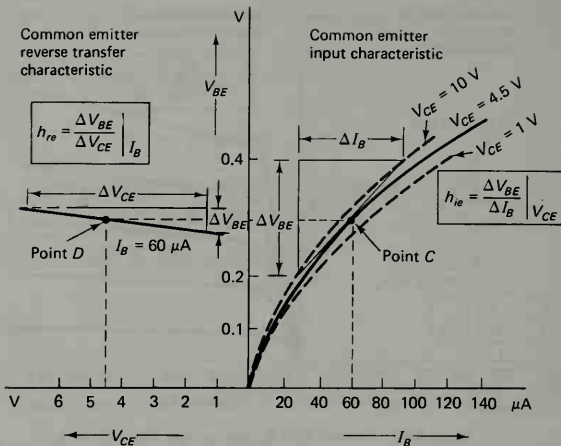
Figure 4-23. Derivation of h_{ie} and h_{re} from characteristics.

solution

When $I_C = 3.5$ mA and $V_{CE} = 4.5$ V, $I_B = 60$ μA (Fig. 4-22).
From point C on Fig. 4-23,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}\bigg|_{(V_{CE} = 4.5 \text{ V})} \approx \frac{0.2 \text{ V}}{60 \text{ μA}} = 3.3 \text{ k}\Omega$$

From point D on Fig. 4-23,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\bigg|_{(I_B = 60 \text{ μA})} \approx \frac{0.03 \text{ V}}{6 \text{ V}} = 5 \times 10^{-3}$$

(*Note that the common emitter reverse transfer characteristic can be determined from the family of input characteristics, Fig. 4-13, simply by drawing a horizontal line for a given level of base current and reading V_{be} for various levels of V_{CE}.*)

For common collector and common base configurations, the h-parameters are defined in a similar way to the common emitter h-parameters, and they may also be derived from the CE and CB characteristics. For common collector, the suffix c replaces the e used in common emitter, and for common base the suffix b is employed. The common collector and common base h-parameter circuits are shown in Figs. 4-24 and 4-25, respectively.
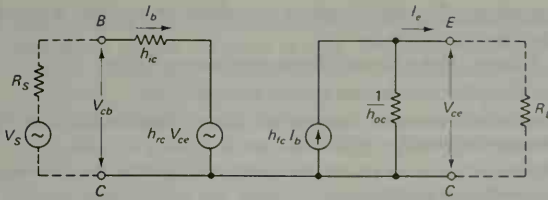
Figure 4-24. Common collector *h*-parameter circuit.
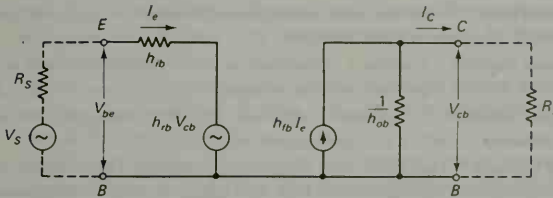
Figure 4-25. Common base *h*-parameter circuit.

*Glossary of
Important
Terms*

Emitter. The portion of a transistor which emits charge carriers into the central base region.

Base. The central portion of a transistor, situated between the emitter and the collector.

Collector. The portion of a transistor which collects the charge carriers from the base region.

Collector–base junction. *pn*-junction between collector and base.

Emitter–base junction. *pn*-junction between emitter and base.

I_E, **emitter current.** Current entering or leaving the emitter terminal.

I_B, **base current.** Current entering or leaving the base terminal.

I_C, **collector current.** Current entering or leaving the collector terminal.

I_{CBO}, **collector base leakage current.** Minority charge carrier current that flows across a reverse-biased collector–base junction.

Bipolar transistor. *pnp* or *npn* transistor.

α_{dc}, **alpha dc.** The fraction of the emitter current that is collected at the collector–base junction, typically 0.98.

β_{dc}, **beta dc.** Current gain factor: I_C/I_B.

α, **alpha.** Ratio of I_C change to I_E change. The ac equivalent of α_{dc}.

β, **beta.** Ratio of I_C change to I_B change. The ac equivalent of β_{dc}.

npn **transistor.** Transistor made of a sandwich of a central *p* region and two outer *n* regions.

pnp transistor.   Transistor made of a sandwich of a central n region and two outer p regions.

V_{CB}.   Voltage applied across collector and base terminals.

V_{BE}.   Voltage across base and emitter terminals.

r_e.   Portion of transistor T-equivalent circuit connected to the emitter terminal, typically $r_e = 25 \ \Omega$.

r_b.   Portion of transistor equivalent circuit connected to the base terminal, typically 100 to 300 Ω.

r_c.   Portion of transistor equivalent circuit connected to collector terminal, typically 1 MΩ.

Common base.   Transistor connection in which base terminal is common to both input and output voltages.

Common emitter.   Transistor connection in which emitter terminal is common to both input and output voltages.

Common collector.   Transistor connection in which collector terminal is common to both input and output voltages.

Punch through.   Condition that occurs when collector–base depletion region spreads throughout the base and causes transistor breakdown.

Reach through.   Same as *punch through*.

r-parameter equivalent circuit.   Circuit redrawn with transistor replaced with its equivalent parameters.

T-equivalent circuit.   Same as *r-parameter equivalent circuit*.

h-parameters.   Parameters employed in a transistor ac equivalent circuit which isolate input and output terminals from each other.

Hybrid parameters.   Same as *h-parameters*.

h_{ie}.   Common emitter input resistance for h-parameter equivalent circuit.

h_{re}.   Common emitter reverse transfer ratio for h-parameter equivalent circuit.

h_{FE}.   Common emitter dc forward current transfer ratio. Same as β_{dc}.

h_{oe}.   Common emitter output conductance for h-parameter equivalent circuit.

h_{fe}.   Common emitter ac forward current transfer ratio for h-parameter equivalent circuit.

Review Questions

4-1.   Draw sketches to show unbiased *pnp* and *npn* junction transistors in block form. Show the depletion region widths and barrier potentials. Briefly explain.

4-2.   Repeat Question 4-1 for a correctly biased *pnp* transistor. Label each block according to its function, and show the direction of movement of charge carriers and the type of carriers involved. Briefly explain the transistor operation.

4-3.   Repeat Question 4-2 for a correctly biased *npn* transistor.

4-4. Draw a sketch to show the various current components in a transistor, and briefly explain the origin of each. Derive an expression for the collector current I_C in terms of base currents I_B and reverse saturation current I_{CBO}. Define α_{dc} and β_{dc} and state typical values for each.

4-5. Sketch the circuit symbols for *pnp* and *npn* transistors. Label each type, show the polarity of bias and supply voltages, and state typical voltage values.

4-6. Sketch and explain the shape of common base input and output characteristics. Also, explain how the characteristics are determined experimentally.

4-7. Sketch and explain the shape of the common base current gain characteristics. Explain how the characteristics may be determined experimentally.

4-8. Sketch and explain the shape of the common emitter input and output characteristics. Explain how the characteristics are determined experimentally.

4-9. Sketch and explain the shape of the common emitter current gain characteristics. Explain how the characteristics may be determined experimentally.

4-10. Sketch the common collector input, output, and current gain characteristics, and explain their shape.

4-11. Sketch the T-equivalent circuit for a transistor. Name each component and discuss its origin. Also, show the simple form of equivalent circuit for low-frequency calculations.

4-12. Sketch the *h*-parameter equivalent circuit for the common emitter configuration. Correctly label all resistors, currents, and voltages.

4-13. Repeat Question 4-12 for the common collector configuration.

4-14. Repeat Question 4-12 for the common base configuration.

4-15. Define h_{oe}, h_{fe}, h_{ie}, and h_{re}.

4-1. Calculate the values of I_C and I_E for a transistor with $\alpha_{dc} = 0.97$ and $I_{CBO} = 10 \ \mu A$, I_B is measured as 50 μA. **Problems**

4-2. For a certain transistor $I_C = 5.255$ mA, $I_B = 100 \ \mu A$, and $I_{CBO} = 5 \ \mu A$:
(a) Calculate α_{dc}, β_{dc}, and I_E.
(b) Determine the new level of I_B required to make $I_C = 15$ mA.

4-3. Calculate the collector and emitter current levels for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 1 \ \mu A$, when the base current is 20 μA.

4-4. The following current measurements were made on a particular transistor in a circuit:

$$I_C = 12.427 \text{ mA}, \qquad I_B = 200 \ \mu A, \qquad I_{CBO} = 7 \ \mu A$$

(a) Determine I_E, β_{dc}, and α_{dc}.

(b) Determine the new level of I_C which will result from reducing I_B to 150 μA.

4-5.   Determine the values of I_B and I_C for a device with the characteristics shown in Figs. 4-13 to 4-15 when V_{BE} is 0.6 V and $V_{CE} = 6$ V.

4-6.   From the common base output characteristics in Fig. 4-10, derive the current gain characteristics for $V_{CB} = -5$ V.

4-7.   A transistor has the characteristics shown in Figs. 4-9 to 4-11. Determine I_E and I_C when $V_{BE} = 0.8$ V and $V_{CB} = 6$ V.

4-8.   Using the common emitter output characteristics shown in Fig. 4-14, derive the current gain characteristic for $V_{CE} = 3$ V. Also determine the value of h_{fe} when $I_C \approx 2$ mA and $V_{CE} \approx 3$ V.

4-9.   From the common emitter current gain and output characteristics in Fig. 4-15, determine h_{oe} and h_{fe} when $V_{CE} \approx -2$ V and $I_C \approx 3$ mA.

4-10.   From the common emitter input characteristics in Fig. 4-13, determine h_{ie} when $I_B = 100$ μA and $V_{CE} = 6$ V.

Transistor Biasing

A dc load line, similar to those for diodes and other electronic devices, may be drawn on the transistor characteristics in order to study the currents and voltages in a particular circuit. The *dc bias point*, or *quiescent point*, is the point on the load line which represents the currents in a transistor and the voltages across it when no signal is applied; i.e., it represents the dc bias conditions. The stability of the bias point may be affected by variations in parameters from one transistor to another or by temperature variations.

The value of h_{FE} (or β_{dc}) for a given type of transistor has a wide tolerance. A typical h_{FE} specification is

$$h_{FE} = \frac{\text{minimum value}}{25} \qquad \frac{\text{typical}}{50} \qquad \frac{\text{maximum value}}{75}$$

As will be seen, the typically wide tolerance of h_{FE} can affect the bias conditions, and thus determine the type of bias circuit that must be used. Temperature variations can also affect bias point stability.

To study the effects of bias conditions on the performance of the common emitter circuit, it is necessary to draw a dc load line on the transistor output characteristics. Consider the circuit and characteristics shown in Fig. 5-1.

If the circuit was to be used as an amplifier, the input terminals would be base and emitter. The output would be taken from collector and emitter. The emitter terminal is common to both input and output, so the configuration is identified as a *common emitter circuit*.

Note that the polarity of the transistor terminal voltage in Fig. 5-1(a) is such that the base–emitter junction is forward biased, and the collector–base junction is reverse biased. These are the normal bias polarities for the device.

From Fig. 5-1(a), the collector emitter voltage is

$$V_{CE} = (\text{supply volts}) - (\text{volt drop across } R_L).$$

Therefore,

$$V_{CE} = V_{CC} - I_C R_L \tag{5-1}$$

(a) Common emitter circuit
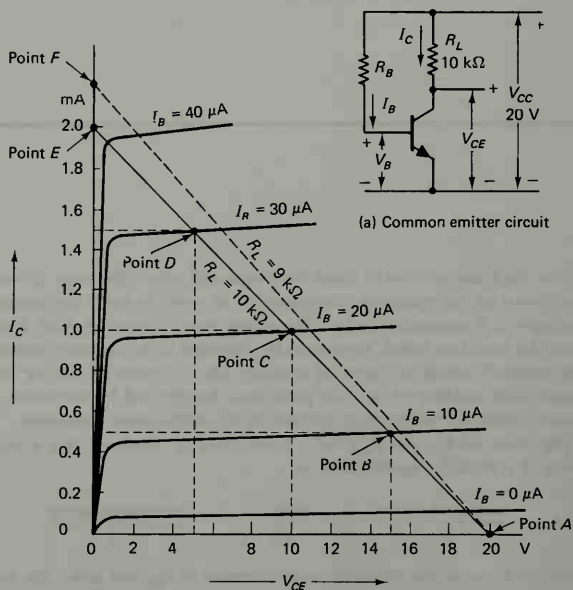
(b) Common emitter characteristics and load line

Figure 5-1. Plotting the dc load line.

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If the base bias voltage V_B is such that the transistor is not conducting, then $I_C = 0$ and $V_{CE} = V_{CC} - (0 \times R_L) = V_{CC} = 20$ V. Therefore, when $I_C = 0$, $V_{CE} = 20$ V. This point is plotted on the output characteristics as point A.

Suppose that V_B is increased until $I_C = 0.5$ mA; then $V_{CE} = 20$ V $-$ $(0.5$ mA $\times 10$ kΩ) $= 20$ V $- 5$ V $= 15$ V, and thus when $I_C = 0.5$ mA, $V_{CE} = 15$ V. This point (point B) is now plotted on the output characteristics. Continuing the above process, several sets of corresponding values of I_C and V_{CE} are obtained and plotted on the common emitter output characteristics:

$$I_C = 1 \text{ mA}, \qquad V_{CE} = 10 \text{ V}, \qquad \text{point } C$$
$$I_C = 1.5 \text{ mA}, \qquad V_{CE} = 5 \text{ V}, \qquad \text{point } D$$
$$I_C = 2 \text{ mA}, \qquad V_{CE} = 0 \text{ V}, \qquad \text{point } E$$

The line drawn through these points is straight and is the *dc load line* for $R_L = 10$ kΩ. Since the load line is straight, it could be produced by plotting only two points and drawing a line through them. The most convenient two points in this case are point A and point E.

$$\text{At point } A, \qquad I_C = 0 \quad \text{and} \quad V_{CE} = V_{CC} = 20 \text{ V}$$
$$\text{At point } E, \qquad V_{CE} = 0 \quad \text{and} \quad I_C = \frac{V_{CC}}{R_L} = 2 \text{ mA}$$

The dc load line is a plot of I_C against V_{CE} for a given value of R_L and a given level of V_{CC}. Thus, it represents all collector current levels and corresponding collector–emitter voltages that can exist in the circuit. For example, a point plotted from $I_C = 1.5$ mA and $V_{CE} = 16$ V would not appear on the dc load line in Fig. 5-1. Therefore, the load line shows that this combination of voltage and current levels could not exist in this particular circuit. Knowing any one of I_C, I_B, or V_{CE}, it is easy to determine the other two from the load line.

The load line in Fig. 5-1 applies only for the case of $V_{CC} = 20$ V and $R_L = 10$ kΩ. If either of these conditions is changed, a new dc load line must be drawn.

Draw the dc load line for the circuit and characteristics of Fig. 5-1 when R_L is changed to 9 kΩ.

Example 5-1

solution

When $I_C =$ zero, $V_{CE} = V_{CC} = 20$ V.
Therefore, plot point A at $I_C =$ zero and $V_{CE} = 20$ V.
When $V_{CE} = 0$ V, $I_C = V_{CC}/R_L = 20$ V/9 k$\Omega = 2.2$ mA.
Therefore, plot point F at $V_{CE} = 0$ V, and $I_C = 2.2$ mA. Now join points A and F together to draw the load line for $R_L = 9$ kΩ.
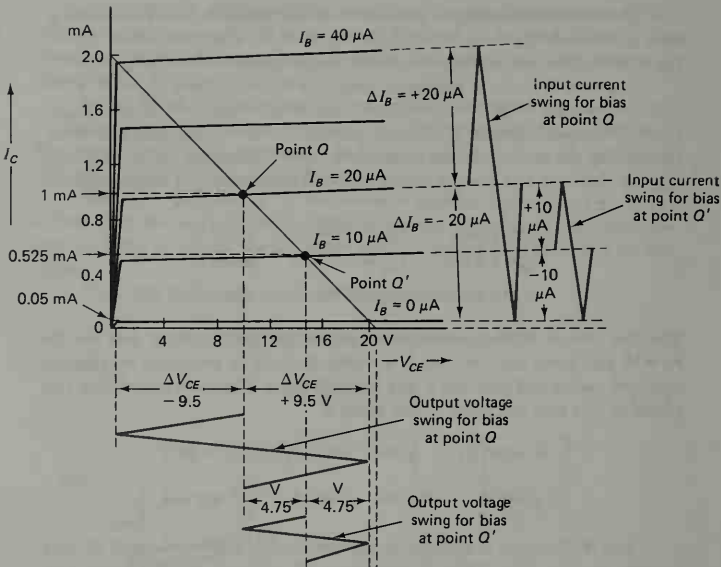
Figure 5-2. Bias point selection.

In designing a circuit, a point on the load line is selected as the *dc bias point*, or *quiescent point*. This bias point specifies the I_C and V_{CE} that exist when no input signal is applied. When an input signal is applied, I_B varies according to the signal amplitude and causes I_C to vary, consequently producing an output voltage variation.

Consider the 10-kΩ dc load line shown in Fig. 5-2, for the circuit of Fig. 5-1(a). Suppose the dc bias conditions are set up as at point Q.

At point Q: $I_B = 20$ μA, $I_C = 1$ mA, and $V_{CE} = 10$ V.

When I_B is increased from 20 μA to 40 μA, I_C becomes 1.95 mA and $V_{CE} = V_{CC} - (I_C \times R_L) = 20 - (1.95 \text{ mA} \times 10 \text{ kΩ}) = 0.5$ V.

Therefore, increasing I_B by 20 μA (from 20 μA to 40 μA) caused V_{CE} to decrease by 9.5 V (from 10 V to 0.5 V), or a $\Delta I_B = +20$ μA caused a $\Delta V_{CE} = -9.5$ V.

When I_B is decreased from 20 μA to 0 μA, I_C becomes 0.05 mA and $V_{CE} = V_{CC} - (I_C \times R_L) = 20 - (0.05 \text{ mA} \times 10 \text{ kΩ}) = 19.5$ V, or a $\Delta I_b = -20$ μA caused a $\Delta V_C = +9.5$ V.

Thus, if the circuit is biased to point Q, where $I_C = 1$ mA and $V_{CE} = 10$ V, an ac input could be provided to produce an output voltage swing (ΔV_{CE}) of ±9.5 V.

Suppose, instead of being biased to point Q, the circuit is biased to point Q'. At point Q',

$$I_C = 0.525 \text{ mA} \quad \text{and} \quad V_{CE} = 14.75 \text{ V}$$
$$\Delta I_B = \pm 10 \text{ } \mu\text{A}, \qquad \Delta I_C = \pm 0.475 \text{ mA}, \qquad \Delta V_{CE} = \pm 4.75 \text{ V}$$

The maximum equal positive and negative variations in V_{CE} are now ± 4.75 V. This is also referred to as the *maximum undistorted output*, because any larger output amplitude would be a distorted waveform; i.e., the negative output change would be larger than the positive output change.

At all bias points above or below point Q, it is seen that the maximum *equal* positive and negative variation in V_{CE} will be less than ± 9.5 V. Therefore, for maximum undistorted output voltage variations, the bias point must be selected at the center of the load line. In some cases, maximum possible output voltage variation will *not* be required, and then the bias point can be at any other suitable point on the load line.

A transistor with the output characteristics shown in Fig. 5-3 is connected as a common emitter amplifier. If $R_L = 2.2$ kΩ, $V_{CC} = 18$ V, and $I_B = 40$ μA, determine the device bias conditions and estimate the maximum undistorted output.

Example 5-2

solution

The circuit is the same as that shown in Fig. 5-1(a), but with $R_L = 2.2$ kΩ and $V_{CC} = 18$ V.
Use Eq. (5-1): $V_{CE} = V_{CC} - I_C R_L$.
When $I_C = 0$,

$$V_{CE} = V_{CC} = 18 \text{ V}$$

Plot point A on Fig. 5-3 at $I_C = 0$, $V_{CE} = 18$ V.
When $V_{CE} = 0$,

$$I_C = V_{CE}/R_L = \frac{18 \text{ V}}{2.2 \text{ k}\Omega} \simeq 8.2 \text{ mA}$$

Plot point B on Fig. 5-3 at $I_C = 8.2$ mA, $V_{CE} = 0$ V.
·Draw the dc load line from points A to B. Where the load line intersects the $I_B = 40$ μA characteristic at point Q, read the bias conditions as $I_C = 4.25$ mA and $V_{CE} = 8.7$ V.

When I_B is increased to 80 μA (point Q_1), V_{CE} is decreased from 8.7 to 1.2 V; i.e., $\Delta V_{CE} = 7.5$ V. When I_B is reduced to zero μA (point Q_2), V_{CE} increases from 8.7 to 16.7 V, and $\Delta V_{CE} = 8$ V.

The *maximum undistorted output* is ± 7.5 V.
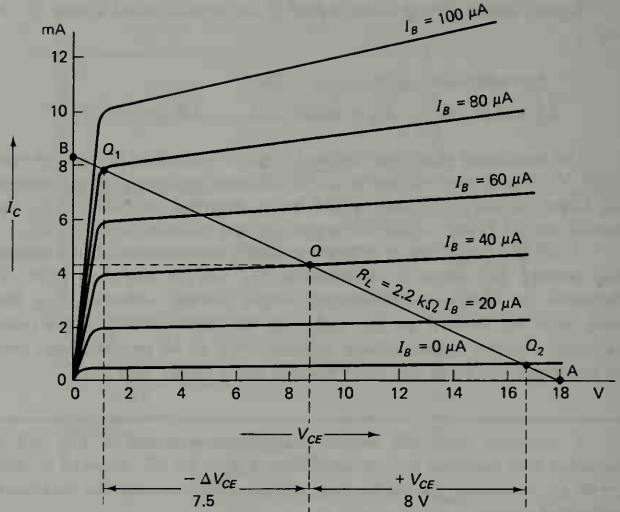
Figure 5-3. Determination of bias conditions and maximum undistorted outputs.

5-3
Fixed
Current
Bias

The bias arrangement shown in Fig. 5-4 [and in Fig. 5-1(a)] is known as *fixed current bias*. The base current I_B is fixed by the bias voltage V_{CC} and the resistor R_B.

From Fig. 5-4,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5-2}$$

Note that because V_{CE}, V_{BE}, and R_B are constant quantities, I_B remains fixed at a particular level. In this circuit I_B is not affected by the transistor h_{FE} value.
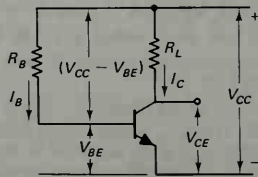
Figure 5-4. Fixed current bias.

Design of bias circuits must begin with a specification of the supply voltage and the required I_C and V_{CE}. Alternatively, R_L and V_{CE} may be specified and I_C calculated. The procedure is best understood by considering a design example.

99
Fixed
Current
Bias

Design a fixed current bias circuit using a silicon transistor having an h_{FE} value of 50 typical, 25 minimum, and 75 maximum. V_{CC} is 10 V, and the dc bias conditions are to be $V_{CE} = 5$ V and $I_C = 1$ mA. Calculate the maximum and minimum levels of I_C and V_{CE}.

Example 5-3

solution

First design the circuit, using the typical value of $h_{FE} = 50$.

value of R_L

From Eq. (5-1)

$$V_{CE} = V_{CC} - I_C R_L$$

and

$$R_L = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 \text{ V} - 5 \text{ V}}{1 \text{ mA}} = 5 \text{ k}\Omega$$

value of R_B

$$I_B \approx \frac{I_C}{h_{FE}} = \frac{(1 \times 10^{-3})}{50} = 20 \text{ }\mu\text{A}$$

From Eq. (5-2),

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 \text{ V} - 0.7 \text{ V}}{20 \text{ }\mu\text{A}} = 465 \text{ k}\Omega$$

If h_{FE} has a typical value of 50, then the bias conditions should be $V_{CE} = 5$ V and $I_C = 1$ mA as desired. Now calculate the bias conditions when h_{FE} is 25 and 75.

When $h_{FE} = 25$, I_B remains equal to $(V_{CC} - V_{BE})/R_B = 20\ \mu A$

and
$$I_C \simeq h_{FE}I_B = 25 \times 20\ \mu A$$
$$= 0.5\ mA$$
$$V_{CE} = V_{CC} - I_C R_L = 10\ V - (0.5\ mA \times 5\ k\Omega)$$
$$= 7.5\ V$$

When $h_{FE} = 75$, I_B remains equal to $(V_{CC} - V_{BE})/R_B = 20\ \mu A$

and
$$I_C \simeq h_{FE}I_B = 75 \times 20\ \mu A$$
$$= 1.5\ mA$$
$$V_{CE} = V_{CC} - I_C R_L = 10\ V - (1.5\ mA \times 5\ k\Omega)$$
$$= 2.5\ V$$

From Example 5-3 it is seen that, although the circuit was designed for $I_C = 1$ mA and $V_{CE} = 5$ V, the actual bias conditions may be anywhere between $I_C = 0.5$ to 1.5 mA and $V_{CE} = 2.5$ to 7.5 V. This wide range results from the spread in possible values of h_{FE}. The fixed current bias technique is *not* a very satisfactory method of obtaining good bias point stability.

In Example 5-3, R_L and R_B as calculated are *not* standard resistance values. In practice the nearest standard values should be selected, and this affects the actual I_C and V_{CE} levels obtained. The following examples continue to use nonstandard resistance values as calculated. This is to permit comparison of the performance of the three basic bias circuits.

5-4
Collector-
to- Base
Bias

In the collector-to-base bias circuit (Fig. 5-5)) the base resistor R_B is connected to the collector of the transistor. This makes the circuit design a little more complicated, but improves the dc bias conditions. To understand how the bias stability is improved, observe that the voltage across R_B is
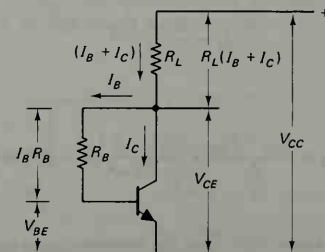
Figure 5-5. Collector-to-base bias.

dependent upon V_{CE}. If I_C becomes larger than the design value, it causes an increased voltage drop across R_L. This results in a smaller level of V_{CE}, which in turn causes I_B to be smaller than its design level. But since $I_C \simeq h_{FE} I_B$, I_C will also tend to be reduced.

From Fig. 5-5,

$$V_{CC} = R_L(I_B + I_C) + V_{CE} \qquad (5\text{-}3)$$

and

$$V_{CE} = I_B R_B + V_{BE} \qquad (5\text{-}4)$$

Design a collector-to-base bias circuit for the conditions specified in Example 5-3, and calculate the maximum and minimum levels of I_C and V_{CE}. **Example 5-4**

solution

First design the circuit, using $h_{FE} = 50$.
From Eq. (4-7),

$$I_B \approx \frac{I_C}{h_{FE}} = \frac{1 \text{ mA}}{50} = 20 \ \mu\text{A}$$

Rearranging Eq. (5-4),

$$R_B = \frac{V_{CE} - V_{BE}}{I_B}$$

$$= \frac{5 \text{ V} - 0.7 \text{ V}}{20 \ \mu\text{A}} = 215 \text{ k}\Omega$$

From Eq. (5-3),

$$R_L = \frac{V_{CC} - V_{CE}}{I_B + I_C}$$

$$= \frac{10 \text{ V} - 5 \text{ V}}{20 \ \mu\text{A} + 1 \text{ mA}} = 4.9 \text{ k}\Omega$$

The circuit has been designed to give $V_{CE} = 5$ V and $I_C = 1$ mA when $h_{FE} = 50$. Now determine the bias conditions when h_{FE} is 25 and when h_{FE} is 75. In this circuit I_B does *not* remain constant when h_{FE} changes.
From Eqs. (5-3) and (5-4),

$$V_{CC} = R_L(I_B + I_C) + I_B R_B + V_{BE}$$

Then, since $I_B \simeq I_C / h_{FE}$,

$$V_{CC} = R_L \left(\frac{I_C}{h_{FE}} + I_C \right) + \frac{I_C}{h_{FE}} R_B + V_{BE}$$

$$= I_C \left[R_L \left(\frac{1}{h_{FE}} + 1 \right) + \frac{R_B}{h_{FE}} \right] + V_{BE}$$

When $h_{FE} = 25$,

$$10 \text{ V} = I_C \left[4.9 \text{ k}\Omega \left(\frac{1}{25} + 1 \right) + \frac{215 \text{ k}\Omega}{25} \right] + 0.7 \text{ V}$$

giving

$$I_C = 0.68 \text{ mA}$$

Substituting $I_B = I_C / h_{FE}$ into Eq. (5-4),

$$V_{CE} = \frac{I_C}{h_{FE}} R_B + V_{BE}$$

$$= \left(\frac{0.68 \text{ mA}}{25} \times 215 \text{ k}\Omega \right) + 0.7 \text{ V} = 6.55 \text{ V}$$

For $h_{FE} = 75$,

$$10 \text{ V} = I_C \left[4.9 \text{ k}\Omega \left(\frac{1}{75} + 1 \right) + \frac{215 \text{ k}\Omega}{75} \right] + 0.7 \text{ V}$$

or

$$I_C = 1.19 \text{ mA}$$

and

$$V_{CE} = \left(\frac{1.19 \text{ mA}}{75} \times 215 \text{ k}\Omega \right) + 0.7 \text{ V} = 4.1 \text{ V}$$

For the collector-to-base bias circuit in Example 5-4, $I_C = 0.68$ to 1.19 mA and $V_{CE} = 4.1$ to 6.55 V. This is an improvement over the fixed current bias circuit.

5-5
Emitter
Current
Bias
(or Self-Bias)

An *emitter current bias* circuit is shown in Fig. 5-6. Resistors R_1 and R_2 divide the supply voltage V_{CC} to provide a fixed bias voltage (V_B) at the transistor base. Also, a resistor R_E is included in series with the emitter terminal of the transistor. The voltage drop across R_E is $V_E = I_E \times R_E$, and
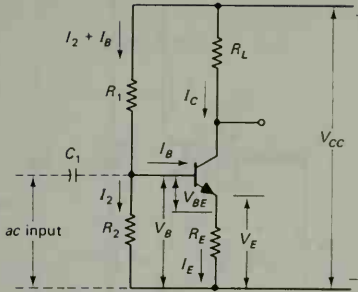
Figure 5-6. Emitter current bias.

$V_E = V_B - V_{BE}.$

Therefore,
$$I_E = \frac{V_B - V_{BE}}{R_E} \qquad (5\text{-}5)$$

if $V_B \gg V_{BE}$, $I_E \approx V_B / R_E$ and is very stable no matter what the value of h_{FE}. Since $I_C \approx I_E$, the collector current is also a stable quantity in this circumstance.

The discussion above assumes that V_B is an extremely constant level of bias voltage. This requires that $R_1 \| R_2$ be *not* very much larger than R_E. If $R_1 \| R_2$ is very much larger than R_E, then the circuit performance becomes similar to the fixed current bias circuit.

To obtain a very stable bias voltage, R_1 and R_2 should be selected as small as possible, so that variations in I_B have little effect on the level of V_B. However, since the ac input is coupled via C_1 to the transistor base (see Fig. 5-6), R_1 and R_2 should be made as large as possible to maintain a high input resistance. A rule-of-thumb approach is to make I_2 (flowing through R_1 and R_2) approximately equal to the collector current I_C. When *thermal stability* is considered, it will be seen that this rule-of-thumb can be very effective.

Using an approximation, this kind of bias circuit can be very easily analyzed to determine I_C and V_{CE}. The approximation is normally quite reasonable. Base current I_B is assumed to be very much smaller than the current I_2 through resistor R_2. This allows V_B to be calculated from the supply voltage V_{CC} and potential divider R_1 and R_2.

$$V_B \approx V_{CC} \times \frac{R_2}{R_1 + R_2} \qquad (5\text{-}6)$$

and

$$I_E = \frac{V_B - V_{BE}}{R_E} \qquad (5\text{-}7)$$

$$I_C \approx I_E$$
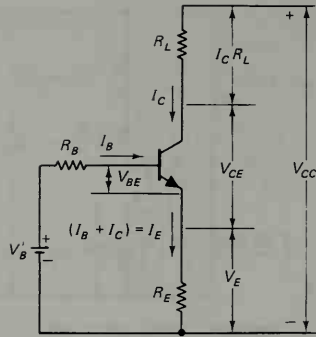
Figure 5-7. Emitter current bias showing bias voltage and source resistance.

Therefore,

$$V_{CE} = V_{CC} - I_E(R_L + R_E) \qquad (5\text{-}8)$$

To rigorously assess the performance of the emitter current biased circuit, it should be redrawn as in Fig 5-7. The bias resistances are replaced with their Thévenin equivalent circuit, in which $V_B' = V_{CC} \times R_2/(R_1 + R_2)$ and $R_B = R_1 \| R_2$.

From Fig. 5-7,

$$V_{CC} = I_C R_L + V_{CE} + R_E(I_B + I_C) \qquad (5\text{-}9)$$

and

$$V_B' = I_B R_B + V_{BE} + R_E(I_B + I_C) \qquad (5\text{-}10)$$

Example 5-5

Using the circuit conditions specified for the last two examples, design an emitter current bias circuit, and investigate the effects of h_{FE} spread.

solution

As before, first design the circuit using the specified typical value of $h_{FE} = 50$.

In this case it will be necessary to use $V_{CC} = 15$ V, so that $I_C R_L = 5$ V, $V_{CE} = 5$ V, and $V_E = 5$ V.

$$I_C R_L = 5 \text{ V}$$

or

$$R_L = \frac{5 \text{ V}}{1 \text{ mA}} = 5 \text{ k}\Omega$$

and

$$V_E = (I_C + I_B)R_E$$

Since $I_B \simeq I_C / h_{FE}$,

$$V_E = \left(I_C + \frac{I_C}{h_{FE}} \right) R_E$$

Substituting values,

$$5\text{ V} = \left(1\text{mA} + \frac{1\text{ mA}}{50} \right) R_E$$

$$R_E = 4.9\text{ k}\Omega$$

Let

$$I_2 = I_C = 1\text{ mA}$$

then

$$R_2 = \frac{V_B}{I_2} = \frac{V_E + V_{BE}}{I_2} = \frac{5\text{ V} + 0.7\text{ V}}{1\text{ mA}}$$

$$= 5.7\text{ k}\Omega$$

and

$$I_B = \frac{I_C}{h_{FE}} = \frac{1\text{ mA}}{50} = 20\ \mu\text{A}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2 + I_B} = \frac{15\text{ V} - 5.7\text{ V}}{1\text{ mA} + 20\ \mu\text{A}}$$

$$= 9.1\text{ k}\Omega$$

Now calculate the bias conditions for $h_{FE} = 25$ and 75:

$$V'_B = V_{CC} \times \frac{R_L}{R_1 + R_2}$$

$$= 15\text{ V} \times \frac{5.7\text{ k}\Omega}{9.1\text{ k}\Omega + 5.7\text{ k}\Omega}$$

$$\approx 5.8\text{ V}$$

and

$$R_B = R_1 \| R_2 = 5.7\text{ k}\Omega \| 9.1\text{ k}\Omega$$

$$= 3.5\text{ k}\Omega$$

From Eq. (5-10),

$$V'_B = I_B R_B + V_{BE} + R_E(I_B + I_C)$$

substitute

$$I_B \simeq \frac{I_C}{h_{FE}}$$

Thus

$$V_B' = \frac{I_C}{h_{FE}} R_B + V_{BE} + R_E\left(\frac{I_C}{h_{FE}} + I_C\right)$$

which gives

$$V_B' - V_{BE} = I_C\left[\frac{R_B}{h_{FE}} + R_E\left(\frac{1}{h_{FE}} + 1\right)\right]$$

or

$$I_C = \frac{V_B' - V_{BE}}{(R_B/h_{FE}) + R_E(1/h_{FE} + 1)}$$

for $h_{FE} = 25$,

$$I_C = \frac{5.8 \text{ V} - 0.7 \text{ V}}{(3.5 \text{ k}\Omega/25) + 4.9 \text{ k}\Omega(1/25 + 1)}$$
$$= 0.97 \text{ mA}$$

for $h_{FE} = 75$,

$$I_C = \frac{5.8 \text{ V} - 0.7 \text{ V}}{(3.5 \text{ k}\Omega/75) + 4.9 \text{ k}\Omega(1/75 + 1)}$$
$$= 1.02 \text{ mA}$$

From Eq. (5-9),

$$V_{CE} = V_{CC} - I_C R_L - R_E\left(\frac{I_C}{h_{FE}} + I_C\right)$$

For $h_{FE} = 25$,

$$V_{CE} = 15 \text{ V} - (0.97 \text{ mA} \times 5 \text{ k}\Omega) - 4.9 \text{ k}\Omega\left(\frac{0.97 \text{ mA}}{25} + 0.97 \text{ mA}\right)$$
$$= 5.2 \text{ V}$$

For $h_{FE} = 75$,

$$V_{CE} = 15 \text{ V} - (1.02 \text{ mA} \times 5 \text{ k}\Omega) - 4.9 \text{ k}\Omega\left(\frac{1.02 \text{ mA}}{75} + 1.02 \text{ mA}\right)$$
$$= 4.9 \text{ V}$$

For the emitter current bias circuit in Example 5-5, I_C is 0.97 to 1.02 mA, and V_{CE} is 4.9 to 5.2 V.

Examples 5-3 to 5-5 show the three types of basic bias circuits. Each circuit employs a transistor with a typical h_{FE} value of 50 and maximum and minimum values of 75 and 25, respectively. Each circuit was designed for $V_{CE} = 5$ V and $I_C = 1$ mA. The maximum and minimum levels of I_C and V_{CE} were calculated as:

For fixed current bias,

$$I_C = 0.5 \text{ to } 1.5 \text{ mA} \quad \text{and} \quad V_{CE} = 2.5 \text{ to } 7.5 \text{ V}$$

For fixed collector to base bias,

$$I_C = 0.68 \text{ to } 1.19 \text{ mA} \quad \text{and} \quad V_{CE} = 4.1 \text{ to } 6.55 \text{ V}$$

For emitter current bias,

$$I_C = 0.97 \text{ to } 1.02 \text{ mA} \quad \text{and} \quad V_{CE} = 4.9 \text{ to } 5.2 \text{ V}$$

Clearly, the emitter current bias circuit is the most stable of the three.

Transistors can be seriously affected by temperature. Two of the most temperature-sensitive quantities are the base–emitter voltage V_{BE} and the collector–base reverse saturation current I_{CBO}. The temperature coefficient of V_{BE}, $(\Delta V_{BE}/\Delta T)$, is approximately -2.2 mV/°C for a silicon transistor, and -1.8 mV/°C for a germanium device. I_{CBO} approximately doubles for each 10°C temperature increase.

An increase in I_{CBO} will cause I_C to increase, and an I_C increase will raise the temperature of the collector–base junction. The junction temperature increase will generate more minority carriers, and so increase I_{CBO} still further. The effect is cumulative, so that a considerable increase in I_C may be produced. This could result in a significant shift in the dc operating point, or, in the worst case, I_C may keep on increasing until the collector–base junction is burned out. This effect is known as *thermal runaway*. Measures taken to avoid it are similar to those required for good bias stability with spread in h_{FE} values.

Changes in V_{BE} may also produce significant changes in I_C and consequently in the dc operating point. However, because of the possibility of thermal runaway, the I_{CBO} changes are by far the most important. The thermal stability of a circuit is assessed by deriving a *stability factor S*.

$$S = \frac{\Delta I_C}{\Delta I_{CBO}} \qquad (5\text{-}11)$$

The minimum value that S can have is one; i.e., if I_{CBO} increases by 1 μA, I_C will increase by at least 1 μA. For $S = 50$, $\Delta I_C = 50 \times \Delta I_{CBO}$. A stability factor of 50 is considered poor, while $S = 10$ is good.

To find S for a given circuit, an expression for I_C is derived and then altered to study the effect of changes in the various currents. From Eq. (4-6), a general expression relation I_B, I_{CBO}, and I_C is

$$I_C = h_{FE}I_B + (1 + h_{FE})I_{CBO}$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ΔI_B and I_C changes by ΔI_C, so the equation becomes:

$$\Delta I_C = h_{FE}\Delta I_B + (1 + h_{FE})\Delta I_{CBO}$$

or

$$1 = h_{FE}\frac{\Delta I_B}{\Delta I_C} + (1 + h_{FE})\frac{\Delta I_{CBO}}{\Delta I_C}$$

$$1 - h_{FE}\frac{\Delta I_B}{\Delta I_C} = (1 + h_{FE})\frac{\Delta I_{CBO}}{\Delta I_C}$$

$$\frac{\Delta I_{CBO}}{\Delta I_C} = \frac{1 - h_{FE}(\Delta I_B/\Delta I_C)}{1 + h_{FE}}$$

$$S = \frac{\Delta I_C}{\Delta I_{CBO}} = \frac{1 + h_{FE}}{1 - h_{FE}(\Delta I_B/\Delta I_C)} \tag{5-12}$$

Equation (5-12) is a general expression for S. To evaluate S, an expression for $\Delta I_B/\Delta I_C$ must be derived for each particular circuit.

From Eq. (5-2),

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

When I_B changes by ΔI_B, V_{CC} and V_{BE} are unaffected, and since I_C is not involved in the equation,

$$\frac{\Delta I_B}{\Delta I_C} = 0$$

Substituting into Eq. (5-12),
For fixed current bias,

$$S = \frac{1 + h_{FE}}{1 - 0}$$

$$= 1 + h_{FE} \tag{5-13}$$

In the bias design examples, h_{FE} ranged from 25 to 75. This gives a value of S from 26 to 76. Thus, the fixed current bias circuit has poor thermal stability as well as poor stability against h_{FE} spread.

From Eqs. (5-3) and (5-4),

$$V_{CC} = R_L(I_C + I_B) + R_B I_B + V_{BE}$$
$$= I_C R_L + I_B(R_L + R_B) + V_{BE}$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ΔI_B and I_C changes by ΔI_C, there is no effect upon V_{CC} and V_{BE}, and the equation becomes

$$0 = \Delta I_C R_L + \Delta I_B(R_L + R_B)$$

or

$$-\Delta I_C R_L = \Delta I_B(R_L + R_B)$$
$$\frac{\Delta I_B}{\Delta I_C} = \frac{-R_L}{R_L + R_B}$$

Substituting this expression into Eq. (5-12),
For collector to base bias,

$$S = \frac{1 + h_{FE}}{1 + h_{FE}\left(\dfrac{R_L}{R_L + R_B}\right)} \qquad (5-14)$$

Using the h_{FE} and resistance values from Example 5-4, S ranges from 17 to 28.

This is an improvement over the fixed current bias stability factor, but in many cases it may be unacceptable. From the expression for S, it is seen that, for a small value of S, R_B must be as small as possible.

From Eq. (5-10),

$$V_B' = I_C R_E + I_B(R_E + R_B) + V_{BE}$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ΔI_B and I_C changes by ΔI_C, there is no change in V_B' and V_{BE}, and the equation becomes

$$0 = \Delta I_C R_E + \Delta I_B(R_E + R_B)$$

or

$$-\Delta I_C R_E = \Delta I_B(R_E + R_B)$$
$$\frac{\Delta I_B}{\Delta I_C} = \frac{-R_E}{R_E + R_B}$$

Substituting into Eq. (5-12),
For emitter current bias

$$S = \frac{1 + h_{FE}}{1 + h_{FE}\left(\dfrac{R_E}{R_E + R_B}\right)} \qquad (5-15)$$

For $I_2 = I_C$, as in Example 5-4, $S \simeq 1.7$, which is a very good stability factor. Also, for $R_B = R_E$, $S \approx 2$; for $R_B = 5R_E$, $S \simeq 6$; and for $R_B \ll R_E$, $S \simeq 1$.

It is seen that the emitter current bias circuit can be the most stable of all three circuits considered. This is the case for temperature variations, as well as for effects of h_{FE} spread.

5-8
AC Bypassing and the AC Load Line

5-8.1
AC Bypassing

In the discussion on the collector-to-base bias circuit, it was explained that an increase in I_B would produce a decrease in V_{CE}, which tends to cancel the original increase in I_B. This, of course, is the effect that produces good dc bias stability. However, the same conditions exist when an ac signal is applied to the base for amplification. The voltage change at the collector tends to cancel the ac input signal, and this can result in the circuit having a very low ac gain, as well as affecting its input impedance. The effect is termed *ac degeneration*, and it must be eliminated if reasonable ac voltage amplification is to be achieved.

Figure 5-8(a) shows how ac degeneration is eliminated in the collector-to-base bias circuit. Instead of using a single bias resistor, two approximately equal resistors, R_{B1} and R_{B2}, are employed. The two must add up to the required value of R_B. A *bypass capacitor* (C_B) is connected from the junction of R_{B1} and R_{B2} to the low-voltage supply terminal, as shown. C_B behaves as a short circuit to ac signals, and the ac equivalent of the circuit is then as shown in Fig. 5-8(b). R_{B1} and R_{B2} are in parallel with the input and output, respectively, and since they are large-value resistances they have virtually no effect on the ac gain of the circuit. The dc bias stability is, of course, unaffected by the presence of C_B.

Emitter current biased circuits also suffer ac degeneration, and a bypass capacitor C_E must be employed, as shown in Fig. 5-9. From the circuit analysis in Chapter 6 the expression for the voltage gain of a common emitter circuit with a resistance in series with the emitter terminal is

$$A_v = \frac{-h_{FE}R_L}{h_{ie} + R_E(1 + h_{fe})}$$

Thus, it is seen that the presence of R_E can keep the amplifier gain uselessly low. C_E has the effect of ac short circuiting R_E to achieve a reasonable voltage gain.

5-8.2
The AC Load Line

The total dc load in series with the transistor in Fig. 5-9 is $(R_L + R_E)$. Thus, the dc load line is drawn for the resistance $(R_L + R_E)$. With R_E bypassed by C_E, the ac load is R_L, and a new *ac load line* must be drawn to
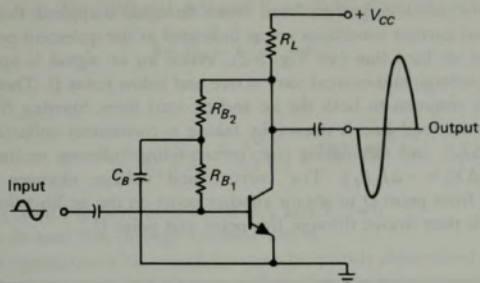
(a) Connection of bypass capacitor
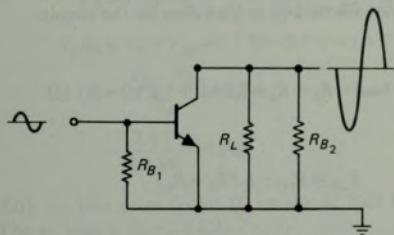
(b) ac equivalent circuit

Figure 5-8. Elimination of ac degeneration in collector-to-base bias circuit.

Figure 5-9. Elimination of ac degeneration in emitter current biased circuit.

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describe the circuit ac performance. When no signal is applied, the transistor voltage and current conditions are as indicated at the quiescent point (point Q) on the dc load line (see Fig. 5-2). When an ac signal is applied, the transistor voltage and current vary above and below point Q. Therefore, the Q point is common to both the ac and dc load l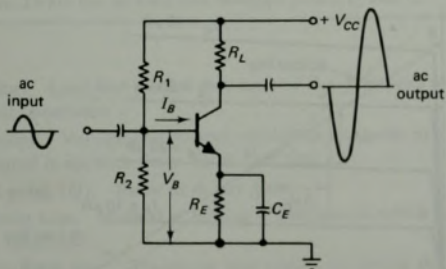ines. Starting from the Q point, the ac load line is drawn by taking a convenient collector current change (ΔI_C), and calculating the corresponding collector emitter voltage change $(\Delta V_C = -\Delta I_C R_L)$. The current and voltage changes are then measured from point Q to obtain another point on the ac load line. The ac load line is then drawn through this point and point Q.

Example 5-6
The common emitter circuit shown in Fig. 5-9 has $V_{CC} = 20$ V, $R_L = 3.9$ kΩ, $R_E = 1.2$ kΩ, $R_1 = 12$ kΩ, and $R_2 = 2.2$ kΩ. R_E is bypassed to ac signals by the large capacitor C_E, and the transistor employed has the characteristics shown in Fig. 5-10. Draw the dc and ac load lines for the circuit.

solution

$$\text{Total dc load} = R_L + R_E = 3.9 \text{ k}\Omega + 1.2 \text{ k}\Omega = 5.1 \text{ k}\Omega$$

and

$$V_{CE} = V_{CC} - I_C(R_L + R_E)$$

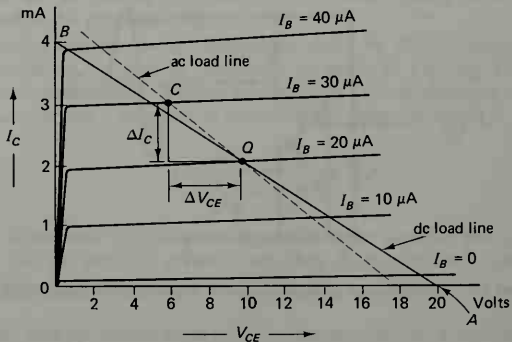When $I_C = 0$,

$$V_{CE} = V_{CC} = 20 \text{ V}$$

Figure 5-10. Plotting the ac load line.

Plot point A on Fig. 5-10 at $I_C = 0$ and $V_{CE} = 20$ V. When $V_{CE} = 0$,

$$0 = V_{CC} - I_C(R_L + R_E)$$

Therefore,

$$I_C = \frac{V_{CC}}{R_L + R_E} = \frac{20 \text{ V}}{5.1 \text{ k}\Omega} = 3.92 \text{ mA}$$

Plot point B on Fig. 5-10 at $I_C = 3.92$ mA and $V_{CE} = 0$.
Draw the dc load line through points A and B.

The approximate bias conditions can be quickly determined by assuming that the base current (I_B) is too small to affect the base bias voltage (V_B). Thus,

$$V_B \approx V_{CC} \times \frac{R_2}{R_1 + R_2} = \frac{20 \text{ V} \times 2.2 \text{ k}\Omega}{12 \text{ k}\Omega + 2.2 \text{ k}\Omega} = 3.1 \text{ V}$$

and

$$I_E R_E = V_B - V_{BE} = 3.1 \text{ V} - 0.7 \text{ V} = 2.4 \text{ V}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} \approx I_C$$

$$= \frac{2.4 \text{ V}}{1.2 \text{ k}\Omega} = 2 \text{ mA}$$

Mark the bias point (point Q) on the dc load line at $I_C = 2$ mA (Fig. 5-10). The ac load is $R_L = 3.9$ kΩ.

Taking $\Delta I_C = 1$ mA, $\Delta V_{CE} = -\Delta I_C R_L = -(1 \text{ mA} \times 3.9 \text{ k}\Omega) = -3.9$ V. Therefore, when I_C increases by 1 mA (from point Q), V_{CE} decreases by 3.9 V. Plot ΔI_C and ΔV_{CE} on Fig. 5-10 to obtain point C as another point on the ac load line. Draw the ac load line through points Q and C.

DC load line. Load line plotted on transistor characteristics to represent all circuit conditions.

Glossary of Important Terms

DC bias point. Voltage and current conditions that exist in a circuit when no signal is applied. Point on dc load line.

Quiescent point (Q). Same as *dc bias point*.

Fixed current bias. Method of biasing a transistor in which base current is held constant.

Collector-to-base bias. Transistor bias circuit in which the base is connected via a resistor to the collector.

Emitter current bias. Transistor bias circuit in which a resistor is connected in the emitter circuit.

Self-bias. Same as *emitter current bias*.

Thermal runaway. Transistor destruction by overheating, due to unstable bias circuit.

Thermal stability factor (S). The ratio of variation in I_C to variations in I_{CBO}.

AC degeneration. Loss of ac circuit gain, due to factors which produce good dc bias stability.

Review Questions

5-1. Sketch a fixed-current bias circuit (a) using an *npn* transistor; (b) using a *pnp* transistor. In each case show the supply voltage polarity and current directions.

5-2. For a fixed-current bias circuit, derive an equation relating I_C to the supply voltage, circuit resistors, and transistor h_{FE} value. Also derive an equation for the transistor collector voltage V_C.

5-3. Repeat Question 5-1 for collector-to-base bias.

5-4. Repeat Question 5-2 for collector-to-base bias.

5-5. Repeat Question 5-1 for emitter-current bias.

5-6. Repeat Question 5-2 for emitter-current bias (a) using an approximate method; (b) for a rigorous analysis.

5-7. Compare the three basic bias circuits with regard to the stability of collector current I_C against changes in h_{FE}.

5-8. Discuss the thermal stability of a transistor circuit, and define the stability factor S. Compare the three basic bias circuits with regard to stability factor S.

5-9. Explain what is meant by *ac degeneration*, and show how it may be eliminated in collector-to-base bias and emitter current bias circuits.

Problems

5-1. For the common emitter circuit and output characteristics shown in Fig. 5-1, plot the dc load line for the following conditions:
(a) $V_{CC} = 15$ V, $R_L = 7.5$ kΩ.
(b) $V_{CC} = 12$ V, $R_L = 8$ kΩ.
In each case, select the best dc bias point, and specify it in terms of I_C and V_{CE}.

5-2. A circuit with the same configuration and transistor characteristics as shown in Fig. 5-1 is to have the following dc bias conditions:

$$V_{CE} = 9 \ V, \qquad I_C = 2 \text{ mA}$$

If V_{CC} is 18 V, plot the bias point on the characteristics, draw the load line, and determine the required value of R_L.

5-3. For a fixed-current bias circuit, $R_B = 200$ kΩ, $R_L = 2$ kΩ, and $V_{CC} = 10$ V. Assuming $V_{BE} = 0.7$ V, find the dc operating point when $h_{FE} = 50$. Also determine the changes in operating point when h_{FE} has a minimum value of 40 and a maximum value of 60.

5-4. A transistor having the output characteristics shown in Fig. 4-14 is connected as a common emitter amplifier. If $R_L = 1.2$ kΩ, $V_{CC} = 7.5$ V, and $I_B = 40$ μA, determine the device bias conditions, and estimate the maximum peak-to-peak undistorted output voltage.

5-5. A fixed current bias circuit has $R_L = 3.3$ kΩ and $V_{CC} = 15$ V. The transistor has a typical $h_{FE} = 60$, with minimum and maximum values of 30 and 90, respectively. Select a value of R_B to give $V_{CE} = 5$ V for the typical h_{FE} value. Also determine the upper and lower limits of V_{CE}.

5-6. A collector-to-base bias circuit is to be designed to have a V_{CE} of 12 V. $R_L = 2.2$ kΩ, $V_{CC} = 20$ V, and the transistor h_{FE} ranges from 40 minimum to 80 typical to 120 maximum. Determine the required value of R_B and calculate the upper and lower limits of V_{CE}.

5-7. A collector-to-base circuit has $R_L = 3.3$ kΩ, $V_{CC} = 15$ V, and $R_B = 330$ kΩ. The silicon transistor employed has an $h_{FE} = 60$ typical, 20 minimum, and 100 maximum. Determine the typical, minimum, and maximum levels of V_{CE}.

5-8. Design a collector-to-base bias circuit using a silicon transistor which has $h_{FE} = 80$ typical, 60 minimum, and 100 maximum. A 25-V supply is to be used, and the dc bias conditions are to be $V_{CE} = 10$ V and $I_C = 3$ mA. Calculate the maximum and minimum levels of V_{CE}.

5-9. The emitter current bias circuit shown in Fig. 5-6 has $R_L = 2.2$ kΩ, $R_E = 3.3$ kΩ, $R_1 = 6.8$ kΩ, $R_2 = 4.7$ kΩ, and $V_{CC} = 15$ V. The transistor employed is silicon and has $h_{FE} = 150$ typical, 100 minimum, and 200 maximum. Calculate the typical, minimum, and maximum levels of V_{CE}.

5-10. Design an emitter current bias circuit using a silicon transistor with $h_{FE} = 60$ typical. The supply is $V_{CC} = 30$ V, and the bias conditions are to be $V_{CE} = 10$ V and $I_C = 1$ mA. Determine values for R_L, R_E, R_1, and R_2. Also calculate the maximum and minimum levels of V_{CE} if maximum $h_{FE} = 80$ and minimum $h_{FE} = 40$.

5-11. An emitter current bias circuit is to be designed to have $V_{CE} = 8$ V. The available supply is $V_{CC} = 20$ V, and the transistor has an h_{FE} which ranges from 40 minimum to 80 typical to 120 maximum. Load resistance $R_L = 6$ kΩ. Select suitable values for R_E and bias resistances R_1 and R_2, and calculate the maximum and minimum levels for V_{CE}.

5-12. Determine the stability factor S for each of the circuits in Problems 5-3, 5-6, and 5-9.

5-13. The circuit designed in Question 5-11 uses a transistor with the characteristics shown in Fig. 5-1. Draw the dc load line, determine the bias conditions, and draw the ac load line.

5-14. Draw the dc and ac load lines for the circuit of Question 5-9. The transistor characteristics are as shown in Fig. 5-10.

6

Basic
Transistor
Circuits

6-1
Introduction

There are three basic transistor circuit configurations—*common emitter*, *common collector*, and *common base*. All transistor circuits, however complicated, are based on these three configurations.

The common emitter circuit is by far the most frequently used of the three. It has good voltage gain and high input impedance. The common collector circuit has a voltage gain of only 1, but it also has a very high input impedance and a very low output impedance. The common base circuit combines good voltage gain with the disadvantage of a very low input impedance. However, the common base circuit can operate satisfactorily at much higher frequencies than the common emitter circuit.

For each of the basic circuits, and for circuits consisting of more than one stage, the gains and impedances may be calculated from a knowledge of the h-parameter equivalent circuit.

6-2
Common
Emitter
Circuit

An *npn* transistor is shown in Fig. 6-1 with a load resistor ($R_L = 10$ kΩ) in series with the collector terminal. A collector supply voltage ($V_{CC} = 20$ V) is provided with a polarity that reverse biases the collector–base junction. A
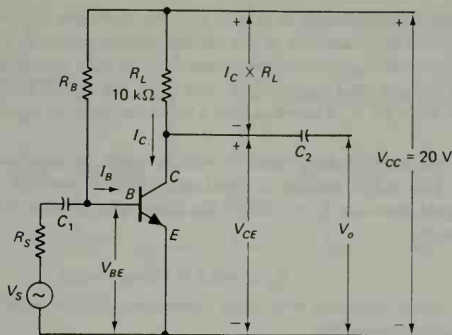
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Figure 6-1. Common emitter circuit.

base current I_B is also provided via R_B, and this results in a forward bias (V_{BE}) at the base–emitter junction. (This is *fixed current bias* as described in Section 5-3.)

A signal voltage V_s having a source resistance R_s is capacitor coupled via C_1 to the transistor base. The output is derived via another capacitor C_2 connected to the transistor collector. Both capacitors are open circuit to direct currents, but offer a very low impedance to ac signals. If the signal source were direct connected instead of capacitor coupled, there would be a low resistance path from the base to the negative supply line, and this would affect the circuit bias conditions. Similarly, an external load directly connected to the transistor collector might alter the collector voltage.

Assume that R_B is selected to give a base current of $I_B = 20$ μA. Also, let the *dc current gain factor* of the transistor be $h_{FE} = 50$. Then

$$I_C \approx h_{FE} I_B$$
$$= 50 \times 20 \times 10^{-6} = 1 \text{ mA}$$

The voltage drop across R_L is $I_C R_L = 1 \text{ mA} \times 10 \text{ k}\Omega = 10$ V, and the collector to emitter voltage V_{CE} is $V_{CC} - (I_C R_L) = 20$ V $- 10$ V $= 10$ V.

The circuit dc conditions have been established as $I_B = 20$ μA, $I_C = 1$ mA, $V_{CE} = 10$ V, $V_{CC} = 20$ V.

If V_{BE} is increased until $I_B = 25$ μA,

$$I_C \approx h_{FE} I_B$$
$$= 50 \times 25 \times 10^{-6} = 1.25 \text{ mA}$$

The voltage drop across R_L is $I_C R_L = 1.25 \text{ mA} \times 10 \text{ k}\Omega = 12.5$ V, and $V_{CE} = V_{CC} - I_C R_L = 20$ V $- 12.5$ V $= 7.5$ V.

When I_B is 20 μA, $V_{CE} = 10$ V, and when I_B is 25 μA, $V_{CE} = 7.5$ V.

Hence, for an increase in I_B of 5 μA, V_{CE} decreases by 2.5 V (i.e., V_{CE} changed by the same amount as the voltage change across R_L).

Similarly, if V_{BE} is decreased until I_B is 15 μA, I_C becomes $= 50 \times 15 \times 10^{-6} = 0.75$ mA and $I_C R_L = 0.75$ mA $\times 10$ k$\Omega = 7.5$ V. Thus, $V_{CE} = 20$ V $- 7.5$ V $= 12.5$ V. Therefore, for a 5-μA decrease in I_B, V_{CE} increases by 2.5 V.

The variation in base–emitter voltage could be produced by the ac signal V_s. This might require a signal amplitude of perhaps ± 10 mV. If $V_s = \pm 10$ mV produces $V_o = \pm 2.5$ V, the signal may be said to be amplified by a factor of

$$V_o / V_s = 2.5 \text{ V} / 10 \text{ mV} = 250$$

or *circuit amplification* $= 250$.

The transistor current and voltage variations have no effect on the supply voltage (V_{CC}). So, when assessing the ac performance of the circuit, V_{CC} can be treated as a short circuit. The coupling capacitor C_1 also becomes a short circuit to ac signals. Redrawing the circuit of Fig. 6-1 with V_{CC} and C_1 shorted gives the ac equivalent circuit shown in Fig. 6-2.

In Fig. 6-2 the circuit input terminals are the base and the emitter, and the output terminals are the collector and the emitter. Thus, the emitter is common to both input and output, and the circuit is designated *common emitter*, or sometimes *grounded emitter*. It is also seen from the figure that resistors R_B and R_L are in parallel with the circuit input and output terminals, respectively.

6-3
Common
Emitter
h-Parameter
Analysis

The *h*-parameter equivalent of the common emitter circuit in Fig. 6-1 is shown in Fig. 6-3. Figure 6-3 is drawn simply by replacing the transistor in the common emitter ac equivalent circuit (Fig. 6-2) with its *h*-parameter equivalent circuit. When an external emitter resistance (R_E) is included in the circuit, as shown in Fig. 6-4(a), the *h*-parameter equivalent circuit becomes that of Fig. 6-4(b).
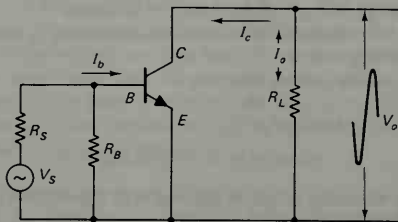

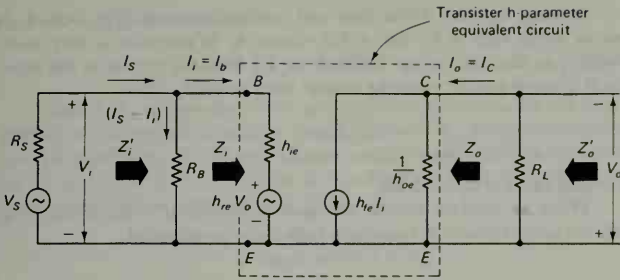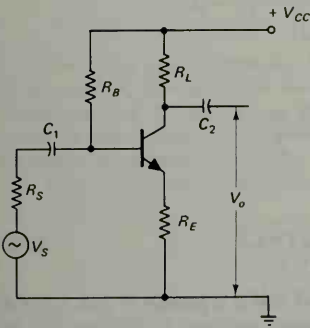**Figure 6-2.** Common emitter ac equivalent circuit.

Figure 6-3. Common emitter *h*-parameter equivalent circuit.

(a) CE circuit with emitter resistance

(b) *h*-parameter equivalent circuit for CE circuit with R_E
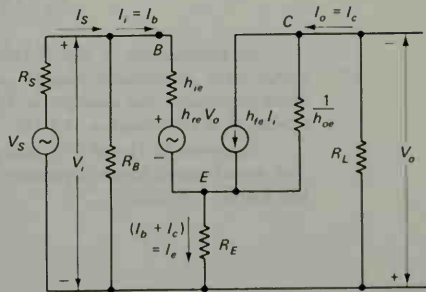
Figure 6-4. CE circuit with emitter resistance and *h*-parameter equivalent circuit.

The current directions and voltage polarities shown in Figs. 6-3 and 6-4(b) are those that occur when the input signal goes positive. The *h*-parameter circuits could be analyzed rigorously to obtain exact expressions for voltage and current gains as well as input and output impedances. However, with a knowledge of the circuit operation and of typical *h*-parameter values, approximations may be made to quickly produce useful and reasonably accurate expressions for calculations of circuit performance.

Looking into the device base and emitter terminals (Fig. 6-3), h_{ie} is seen in series with $h_{re}V_o$. For a CE circuit h_{re} is normally a very small quantity, so that the voltage fed back $(h_{re}V_o)$ from the output to the input circuit is much smaller than the voltage drop across h_{ie}. Thus,

$$Z_i \approx h_{ie} \tag{6-1}$$

A typical value of h_{ie} is 1.5 kΩ.

When an external emitter resistance is connected in the circuit (Fig. 6-4), the calculation of Z_i becomes a little more complicated.

$$\begin{aligned}
V_i &= I_b h_{ie} + I_e R_e \quad \text{(again ignoring } h_{re}V_o)\\
&= I_b h_{ie} + R_E(I_b + I_c)\\
&= I_b h_{ie} + R_E I_b + R_E h_{fe} I_b\\
&= I_b \big[h_{ie} + R_E(1 + h_{fe}) \big]
\end{aligned}$$

and

$$Z_i = \frac{V_i}{I_i} = \frac{V_i}{I_b}$$

Therefore,

$$Z_i = h_{ie} + R_E(1 + h_{fe}) \tag{6-2}$$

An examination of Eq. (6-2) shows that it is possible to look at a CE circuit with an external emitter resistance and very quickly estimate its input impedance. For example, in Fig. 6-4(a), if $R_E = 1$ kΩ, $h_{ie} = 1.5$ kΩ, and $h_{fe} = 50$, Z_i is calculated as 52.5 kΩ.

Equations (6-1) and (6-2) give the input impedance to the device base. The actual circuit input impedance is R_B in parallel with Z_i [see Figs. 6-3 and 6-4(b)]. Therefore,

$$Z_i' = R_B \| Z_i \tag{6-3}$$

Since output voltage variations have little effect upon the input of a CE circuit, only the output half of the circuit need be considered in determining the output impedance. Looking into the collector and emitter terminals, a large resistance $(1/h_{oe})$ is seen. Thus,

$$Z_o \approx 1/h_{oe} \tag{6-4}$$

Z_o is the device output impedance. The actual circuit output imped-

ance is Z_o in parallel with R_L.

$$Z_o' = 1 / h_{oe} \| R_L \qquad (6\text{-}5)$$

Since $1/h_{oe}$ is typically 1 MΩ and R_L is usually very much less than 1 MΩ, the circuit output impedance is approximately R_L. Using this information it is possible to tell the approximate output impedance of a CE circuit just by looking at it. If R_L in Figs. 6-3 and 6-4 is 10 kΩ, then the circuit output impedance is approximately 10 kΩ.

$$\text{Voltage gain} = A_v = V_o / V_i$$

6-3.3
Voltage Gain

From Fig. 6-3, $V_o = I_c R_L$ and $V_i = I_b h_{ie}$. Therefore,

$$A_v = \frac{I_c R_L}{I_b h_{ie}} = \frac{I_c}{I_b} \times \frac{R_L}{h_{ie}} = \frac{-h_{fe} R_L}{h_{ie}} \qquad (6\text{-}6)$$

The minus sign indicates that V_o is 180° out of phase with V_i. (When V_i increases, V_o decreases, and vice versa.) Knowing the appropriate h-parameters and R_L, the voltage gain of a CE circuit can be quickly estimated. Using typical values such as $R_L = 10$ kΩ, $h_{fe} = 50$, and $h_{ie} = 1.5$ kΩ, a typical CE voltage gain is -330.

With an external emitter resistance (R_E) in the circuit,

$$\begin{aligned} V_i &= I_b h_{ie} + I_e R_E \\ &= I_b h_{ie} + R_E (I_b + I_c) \\ &= I_b h_{ie} + R_E I_b (1 + h_{fe}) \\ &= I_b \left[h_{ie} + R_E (1 + h_{fe}) \right] \end{aligned}$$

and

$$A_v = \frac{V_o}{V_i} = \frac{I_c R_L}{I_b \left[h_{ie} + R_E (1 + h_{fe}) \right]} = \frac{-h_{fe} R_L}{h_{ie} + R_E (1 + h_{fe})} \qquad (6\text{-}7)$$

Usually $R_E(1 + h_{fe}) \gg h_{ie}$ so that

$$A_v \approx -R_L / R_E$$

Using this expression, the voltage gain of a CE circuit with an external emitter resistance can easily be estimated. If in Fig. 6-4 $R_L = 10$ kΩ and $R_E = 1$ kΩ, the circuit voltage gain is approximately -10.

It is interesting to note that Eqs. (6-6) and (6-7) can each be written as

$$A_v = \frac{-h_{fe}(\text{load resistance})}{(\text{input resistance})}$$

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b}$$

Therefore,

$$A_i = h_{fe} \qquad (6\text{-}8)$$

This expression is true for CE circuits both with and without R_E. However, it is the device current gain, *not* the circuit current gain. Examination of Fig. 6-3 or Fig. 6-4(b) shows that the signal current (I_s) divides between R_B and Z_i.

The voltage developed across R_B and Z_i in parallel is

$$V_i = I_s \left[\frac{R_B \times Z_i}{R_B + Z_i} \right]$$

and $I_b = V_i / Z_i$. Therefore,

$$I_b = \frac{I_s}{Z_i} \left[\frac{R_B \times Z_i}{R_B + Z_i} \right] = \frac{I_s R_B}{R_B + Z_i}$$

and

$$I_s = \frac{I_b (R_B + Z_i)}{R_B}$$

The circuit current gain is

$$A_i' = \frac{I_c}{I_s} = \frac{I_c R_B}{I_b (R_B + Z_i)}$$

$$A_i' = \frac{h_{fe} R_B}{R_B + Z_i} \qquad (6\text{-}9)$$

Once again, knowing the appropriate h-parameters, the circuit current gain can be quickly estimated just by looking at the circuit. For such typical values as $h_{fe} = 50$, $h_{ie} = 1.5$ kΩ, and $R_B = 33$ kΩ, the CE circuit current gain is approximately 48.

The power input $P_i = V_i \times I_i$ and power output $P_o = V_o \times I_o$. Therefore, the power gain $A_p = (P_o / P_i) = (V_o \times I_o)/(V_i \times I_i) = (V_o / V_i) \times (I_o / I_i)$

or

$$A_p = A_v \times A_i \qquad (6\text{-}10)$$

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Equation (6-10) gives the device power gain. To determine the circuit power gain, the circuit current gain A_i' must be employed.

$$A_p' = A_v \times A_i' \qquad (6\text{-}11)$$

Using the typical values previously calculated, $A_i = 50$ and $A_v = 330$, a typical CE power gain is 16,500. If an unbypassed emitter resistance (R_E) is included in the circuit, the value of A_v is reduced and, consequently, the A_p is also reduced.

Without R_E in the Circuit

Input impedance $Z_i \approx h_{ie} = 1.5 \text{ k}\Omega$ typically

Circuit input impedance $Z_i' \approx R_B \| Z_i$

Output impedance $Z_o \approx 1/h_{oe} = 1 \text{ M}\Omega$ typically

Circuit output impedance $Z_o' \approx R_L \| 1/h_{oe}$

Circuit voltage gain $A_v \approx \dfrac{h_{fe} R_L}{h_{ie}} = 330$ typically

Current gain $A_i \approx h_{fe} = 50$ typically

Circuit current gain $A_i' \approx \dfrac{h_{fe} R_B}{R_B + Z_i}$

Power gain $A_p = A_v \times A_i = 16,500$ typically

Circuit power gain $A_v' = A_v \times A_i'$

With R_E Included in the Circuit

Input impedance $Z_i \approx h_{ie} + R_E(1 + h_{fe})$

Circuit input impedance $Z_i' \approx R_B \| Z_i$

Voltage gain $A_v \approx R_L / R_E$

The common emitter circuit has good voltage gain with phase inversion; i.e., the output voltage decreases when the input voltage increases, and vice versa. The CE circuit also has good current gain and power gain, and relatively high input and output impedances. As a voltage amplifier, the CE circuit is by far the most frequently used of all three basic transistor circuit configurations.

In the common emitter circuit shown in Fig. 6-5 the device parameters are $h_{ie} = 2.1 \text{ k}\Omega$, $h_{fe} = 75$, and $h_{oe} = 10^{-6}$ S. Calculate the input and output impedances, and the voltage, current, and power gains.
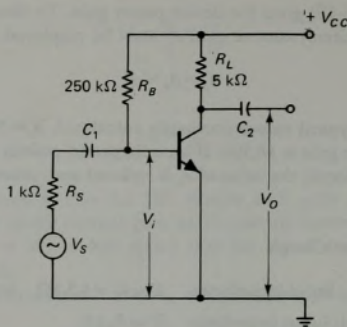
Example 6-1

Figure 6-5. Circuit for Example 6-1.

solution

From Eq. (6-1), $Z_i \approx h_{ie} = 2.1$ kΩ.

From Eq. (6-3), the circuit input impedance is

$$Z_i' = 2.1 \text{ kΩ} \| 250 \text{ kΩ} = 2.09 \text{ kΩ}$$

From Eq. (6-4), $Z_o \approx 1/h_{oe} = 1$ MΩ, and from Eq. (6-5), the circuit output impedance is

$$Z_o' = 1 \text{ MΩ} \| 5 \text{ kΩ} = 4.98 \text{ kΩ}$$

From Eq. (6-6),

$$A_v = \frac{-75 \times 5 \text{ kΩ}}{2.1 \text{ kΩ}} = -179$$

From Eq. (6-8), $A_i \approx h_{fe} = 75$, and from Eq. (6-9), the circuit current gain is

$$A_i' = \frac{75 \times 250 \text{ kΩ}}{250 \text{ kΩ} + 2.1 \text{ kΩ}} = 74.4$$

From Eq. (6-11),

$$A_p' = 179 \times 74.4 \approx 13,300$$

Example 6-2

Determine the effect on the performance of the common emitter circuit in Example 6-1 when a 1-kΩ emitter resistance is included in the circuit.

solution

From Eq. (6-2), $Z_i = 2.1$ k$\Omega + (76 \times 1$ k$\Omega) = 78.1$ kΩ, and from Eq. (6-3), the circuit input impedance is

$$Z_i' = 78.1 \text{ k}\Omega \| 250 \text{ k}\Omega = 59.5 \text{ k}\Omega$$

From Eqs. (6-4) and (6-5), the circuit output impedance is

$$Z_o' = 4.98 \text{ k}\Omega$$

From Eq. (6-7),

$$A_v = \frac{-75 \times 5 \text{ k}\Omega}{2.1 \text{ k}\Omega + (76 \times 1 \text{ k}\Omega)} = -4.8$$

From Eq. (6-8), $A_i \approx 75$, and from Eq. (6-9), the circuit current gain is

$$A_i' = \frac{75 \times 250 \text{ k}\Omega}{59.5 \text{ k}\Omega + 250 \text{ k}\Omega} = 60.6$$

From Eq. (6-11)

$$A_p' = 4.8 \times 60.6 = 291$$

In the common collector circuit, the load resistor (R_L) is in series with the transistor emitter terminal. In the circuit shown in Fig. 6-6, the collector supply is 20 V and the base bias voltage V_B is derived from V_{CC} via the
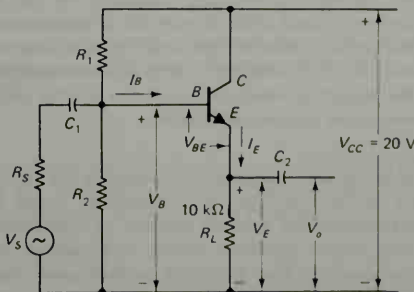
6-4
Common
Collector
Circuit

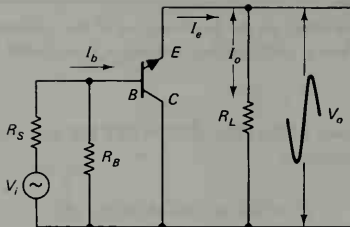**Figure 6-6.** Common collector circuit.

Figure 6-7. Common collector ac equivalent circuit.

potential divider R_1 and R_2. In this case, V_B is *not* equal to the base–emitter junction voltage V_{BE}, but is equal to the sum of V_{BE} and V_E.

Suppose $I_E = 1$ mA; then $V_E = I_E \times R_L = 1$ mA $\times 10$ k$\Omega = 10$ V. If $V_{BE} = 0.7$ V, then $V_B = V_{BE} + V_E = 10.7$ V and the collector–emitter voltage $V_{CE} = V_{CC} - V_E = 20$ V $- 10$ V $= 10$ V.

If the transistor dc current gain $(h_{FE} = I_C/I_B)$ is 50, then I_E/I_B also approximately equals 50. For $I_E = 1$ mA, $I_B \approx (1 \times 10^{-3})/50 = 20$ μA.

The dc conditions of the circuit are: $I_B = 20$ μA, $I_E = 1$ mA, $V_{CE} = 10$ V, $V_{CC} = 20$ V, and $V_B = 10.7$ V.

As in the case of the common emitter circuit, any increase or decrease in V_B causes I_B to vary, and consequently produces a variation in I_E and V_E. If I_B is made to vary by ± 5 μA, then I_E increases or decreases by approximately $h_{FE} \times \Delta I_B$. $\Delta I_E = 50 \times (\pm 5 \times 10^{-6})$ or ± 0.25 mA. The variation in V_E is $\Delta V_E = \Delta I_E \times R_L = \pm 0.25$ mA $\times 10$ k$\Omega = \pm 2.5$ V.

Since $V_B = (V_{BE} + V_E)$, any increase or decrease in V_E requires an equal variation in V_B. For $\Delta V_E = \pm 2.5$ V, $\Delta V_B \approx \pm 2.5$ V.

It can also be stated that an input voltage variation of $\Delta V_B = \pm 2.5$ V at the base produces an output at the emitter of approximately $\Delta V_E = \pm 2.5$ V. Thus, the emitter voltage may be said to follow the base voltage, and this gives the circuit its other name, which is *emitter follower*.

The supply voltage and coupling capacitors (in Fig. 6-6) may be replaced with short circuits in order to study the ac performance. This gives the common collector ac equivalent circuit of Fig. 6-7. Note that R_B is the parallel combination of R_1 and R_2. The input terminals are base and collector, and the output terminals are the emitter and the collector. Hence, the name *common collector* (or *grounded collector*).

6-5
Common
Collector
h-Parameter
Analysis

Figure 6-8 shows the h-parameter equivalent of the practical common collector circuit of Fig. 6-6. The CC h-parameter circuit is drawn by replacing the transistor in the common collector ac equivalent circuit (Fig. 6-7) with its h-parameter equivalent circuit. The current directions and voltage polarities shown in Fig. 6-8 are those that occur when the input signal goes positive.
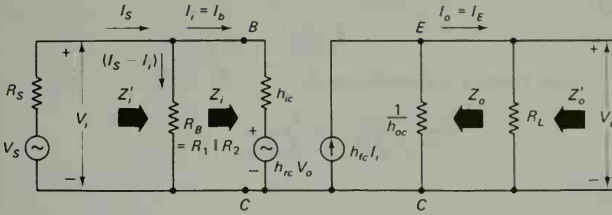
Figure 6-8. Common collector h-parameter equivalent circuit.

In making approximations to arrive quickly at expressions for CC gains and impedances, it is necessary to note that $h_{rc} = 1$; i.e., all of V_o is fed back to the input.

$$
\begin{aligned}
V_i &= I_b h_{ic} + V_o \\
&= I_b h_{ic} + I_e R_L \\
&= I_b h_{ic} + R_L I_b h_{fc} \\
&= I_b (h_{ic} + h_{fc} R_L)
\end{aligned}
$$

6-5.1
*Input
Impedance*

and

$$
\begin{aligned}
Z_i &= V_i / I_i = V_i / I_b \\
&= h_{ic} + h_{fc} R_L
\end{aligned}
\tag{6-12}
$$

Equation (6-12) is similar to the expression for the input impedance of a CE circuit with an external emitter resistor [Eq. (6-2)]. Using Eq. (6-12), it is possible to look at a CC circuit and very quickly estimate its input impedance. If R_L is 1 kΩ, h_{ic} is 1.5 kΩ, and h_{fc} is 51, Z_i is calculated as 52.5 kΩ.

The input impedance determined from Eq. (6-12) is, of course, the input impedance of the transistor. To obtain the circuit input impedance, the parallel combination of R_B and Z_i must be calculated.

$$
Z_i' = R_B \| Z_i
\tag{6-13}
$$

In the CC circuit any variation in output voltage will have a significant effect on the input circuit. To determine Z_o, the signal voltage is assumed to be zero, and I_o is calculated in terms of V_o.

6-5.2
*Output
Impedance*

$$
Z_o = \frac{V_o}{I_o}
$$

and

$$I_o = h_{fe} I_i$$

With $V_S = 0$, I_i is produced by V_o:

$$I_i = \frac{V_o}{h_{ie} + (R_B \| R_S)}$$

and

$$I_o = h_{fe} I_i = \frac{h_{fe} V_o}{h_{ie} + (R_B \| R_S)}$$

Therefore,

$$Z_o = \frac{V_o}{I_o} = \frac{h_{ie} + (R_B \| R_S)}{h_{fe}} \qquad \text{(6-14)}$$

Note that the output impedance is (h_{ie} + the total impedance in series with the base terminal) all divided by h_{fe}. It is interesting to compare this to the input impedance, which is ($h_{ie} + h_{fe}$ times the impedance in series with the emitter terminal). As with Z_i, it is possible to look at a CC circuit and quickly estimate Z_o. For $h_{ie} = 1.5$ kΩ, $R_B = 5$ kΩ, $R_S = 5$ kΩ, and $h_{fe} = 51$, Z_o is calculated as 78.4 Ω.

Once again the above equation for output impedance refers to the device only. For the circuit output impedance, R_L is in parallel with Z_o.

$$Z_o' = R_L \| Z_o \qquad \text{(6-15)}$$

Since R_L is usually much larger than Z_o

$$Z_o' \approx Z_o$$

6-5.3
Voltage Gain

$$A_v = V_o / V_i$$
$$V_o = I_e R_L = h_{fe} I_b R_L$$

and

$$I_b = (V_i - V_o) / h_{ie}$$

Therefore,

$$V_o = \frac{h_{fe} R_L}{h_{ie}} (V_i - V_o)$$

and

$$V_o\left[1 + \frac{h_{fe}R_L}{h_{ie}}\right] = \frac{h_{fe}R_L V_i}{h_{ie}}$$

$$A_v = \frac{V_o}{V_i} = \frac{h_{fe}R_L/h_{ie}}{1 + (h_{fe}R_L/h_{ie})}$$

$$\approx 1 \qquad (6\text{-}16)$$

This agrees with what was previously discovered about the CC amplifier, i.e., that it has a voltage gain of approximately 1, and that there is no phase shift between input and output.

$$A_i = I_o/I_i = I_e/I_b$$

$$= h_{fe} \qquad (6\text{-}17)$$

Equation (6-17) gives the device current gain. Since the signal current I_s divides between R_B and Z_i (see Fig. 6-8), the circuit current gain is smaller than the device current gain. Using the same reasoning employed to arrive at the current gain for the CE circuit [Eq. (6-9)], the CC circuit current gain is

$$A_i' = \frac{h_{fe}R_B}{R_B + Z_i} \qquad (6\text{-}18)$$

For the CC circuit R_B is usually very much smaller than Z_i, so that R_B has quite a significant effect upon the circuit current gain. Using the typical values previously employed, $Z_i = 52.5$ kΩ, $R_B = 5$ kΩ, and $h_{fe} = 51$, A_i is 51 and A_i' becomes 4.4.

The equation for CC power gain is derived exactly as for the CE circuit [Eq. (6-10)]:

$$A_p = A_v \times A_i$$

and since $A_v \approx 1$,

$$A_p \approx A_i \qquad (6\text{-}19)$$

The circuit power gain is

$$A_p' \approx A_i' \qquad (6\text{-}20)$$

Using the typical values of A_i and A_i' already calculated, a typical value of A_p is 51 and A_p' is 4.4.

6-5.6
*Summary of
Typical CC
Circuit
Performance*

Input impedance $Z_i \approx h_{ie} + h_{fe}R_L = 52.5 \text{ k}\Omega$ typically

Circuit input impedance $Z_i' \approx R_B \| Z_i$

Output impedance $Z_o \approx \dfrac{h_{ie} + (R_B \| R_S)}{h_{fe}} = 78.4 \ \Omega$ typically

Circuit output impedance $Z_o' \approx R_L \| Z_o$

Voltage gain $A_v \approx 1$

Current gain $A_i \approx h_{fe} = 51$ typically

Circuit current gain $A_i' \approx \dfrac{h_{fe}R_B}{R_B + Z_i}$

Power gain $A_p \approx A_i$

Circuit power gain $A_p' \approx A_i'$

It is seen that the common collector circuit provides current gain and power gain, but no voltage gain. The input impedance is also very high, and the output impedance is very low. This high Z_i–low Z_o characteristic allows the amplifier to be applied where a low impedance load is to be supplied with a signal from a high impedance source. In this application it is known as a *buffer amplifier*.

Example 6-3

In the common collector circuit in Fig. 6-9, the transistor parameters are $h_{ie} = 2.1 \text{ k}\Omega$ and $h_{fe} = 76$. Calculate the circuit input and output impedances, and the voltage, current, and power gains.
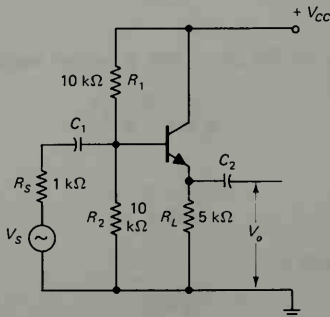

Figure 6-9. Circuit for Example 6-3.

From Eq. (6-12); $Z_i \approx 2.1$ k$\Omega + (76 \times 5$ k$\Omega) = 382.1$ kΩ, and from Eq. (6-13), the circuit input impedance is

$$Z_i' = 382.1 \text{ k}\Omega \| 10 \text{ k}\Omega \| 10 \text{ k}\Omega \| 10 \text{ k}\Omega = 4.94 \text{ k}\Omega$$

From Eq. (6-14), $Z_o \approx [2.1$ k$\Omega + (1$ k$\Omega \| 10$ k$\Omega \| 10$ k$\Omega)]/76 = 38.6$ Ω.
From Eq. (6-15) the actual circuit output impedance is

$$Z_o' = 38.6 \ \Omega \| 5 \text{ k}\Omega = 38.3 \ \Omega$$

From Eq. (6-16), $A_o \approx 1$.
From Eq. (6-17), $A_i = 76$.
From Eq. (6-18), the actual circuit current gain is

$$A_i' = \frac{76 \times (10 \text{ k}\Omega \| 10 \text{ k}\Omega)}{382.1 \text{ k}\Omega + (10 \text{ k}\Omega \| 10 \text{ k}\Omega)} = 0.98$$

From Eq. (6-20), the power gain is

$$A_o \times A_i' = 1 \times 0.98 = 0.98$$

The common base circuit shown in Fig. 6-10 has its load resistance (R_L) connected in series with the collector terminal of the transistor. An emitter resistance (R_E) is also included to avoid short circuiting the ac input, which is applied to the transistor emitter terminal. The base voltage (V_B) is
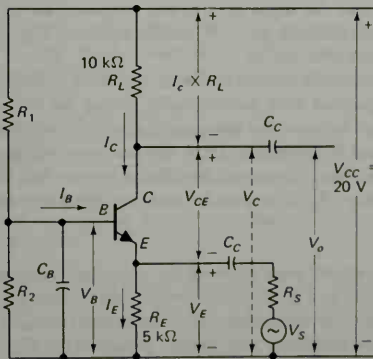
6-6
Common
Base
Circuit

Figure 6-10. Common base circuit.

the sum of $I_E R_E$ and V_{BE}. V_B is derived from V_{CC} by the potential divider R_1 and R_2. A capacitor C_B is provided at the transistor base so that V_B will not vary when an input voltage is applied to the transistor emitter. The output is taken from the transistor collector terminal as shown.

For the circuit of Fig. 6-10, let $I_E = 1$ mA.
Then

$$V_E = I_E R_E = 1 \text{ mA} \times 5 \text{ k}\Omega = 5 \text{ V},$$

and $V_B = V_E + V_{BE} = 5.7$ V (for a silicon transistor).

Also, $I_B \approx I_E / h_{FE} = 20$ μA (typically, for $h_{FE} = 50$),
and

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_L - I_E R_E \approx V_{CC} - I_E(R_L + R_E) \\ &= 20 \text{ V} - 1 \text{ mA}(10 \text{ k}\Omega + 5 \text{ k}\Omega) \\ &= 5 \text{ V} \end{aligned}$$

and

$$V_C = V_{CC} - I_C R_L = 10 \text{ V}$$

The circuit dc conditions are now defined as $I_C \approx I_E = 1$ mA, $V_B = 5.7$ V, $V_{CE} \approx 5$ V, and $V_C = 10$ V.

An ac input signal (V_i) at the emitter will cause the base–emitter voltage (V_{BE}) to change, thus changing I_B and I_C.

When V_i is positive going, V_{BE} is reduced. This causes I_B to be reduced, and consequently I_C becomes smaller. If V_{BE} is reduced (by $+ V_i$) until $I_B = 15$ μA, then $I_C = h_{FE} I_B = 50 \times 15$ μA $= 0.75$ mA, and $V_C = V_{CC} - I_C R_L = 20$ V $- (0.75$ mA $\times 10$ k$\Omega) = 12.5$ V.

When $I_B = 20$ μA, $V_C = 10$ V, and when $+ V_i$ changed I_B to 15 μA, V_C became 12.5 V; i.e., V_C changed from 10 to 12.5 V.

It is seen that the input of $+ V_i$ has produced an output of $+ 2.5$ V. Similarly, an equal input of $- V_i$ would increase V_{BE}, I_B, and I_C, and produce an output of $- 2.5$ V.

The ac equivalent circuit is drawn as before by replacing the supply voltage and capacitors with short circuits, giving the circuit shown in Fig. 6-11. V_i is applied between the base and the emitter, and the output is taken from the base and the collector. Thus, the base terminal is common to both input and output, and the circuit is called a *common base* circuit. Note that the emitter resistor (R_E) is in parallel with the input terminals.

6-7
Common
Base
h-Parameter
Analysis

The h-parameter equivalent of the practical common base circuit of Fig. 6-10 is shown in Fig. 6-12. As always, this is done by substituting, the transistor h-parameter circuit into the ac equivalent circuit (Fig. 6-11). Once again the current directions and voltage polarities (in Fig. 6-12) are shown for a positive-going input signal. It is important to note that Fig. 6-12 is
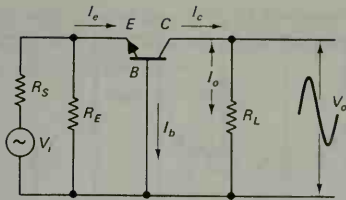
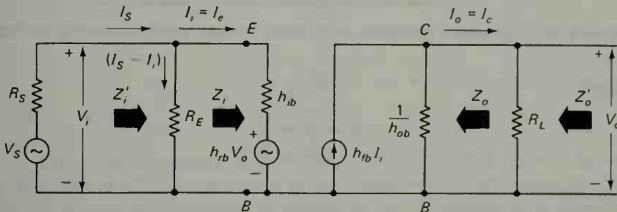Figure 6-11. Common base ac equivalent circuit.

Figure 6-12. Common base *h*-parameter equivalent circuit.

drawn on the assumption that the base of the transistor is ac shorted to ground via capacitor C_B (see Fig. 6-10). If C_B is not present, the parallel combination of R_1 and R_2 appears in series with the transistor base terminal, and the *h*-parameter equivalent circuit becomes that shown in Fig. 6-13, where $R_B = R_1 \| R_2$. As will be seen, the omission of C_B can seriously affect the circuit performance.

In the CB circuit, only a fraction of the voltage is fed back to the input; i.e., h_{rb} is very small. Therefore, $(h_{rb} V_o)$ can be neglected when deriving approximate expressions for CB gains and impedances.

Neglecting $(h_{rb} \times V_o)$ in Fig. 6-12 gives

$$Z_i \approx h_{ib} \qquad (6\text{-}21)$$

A typical value of h_{ib} is 30 Ω. When capacitor C_B is absent, Z_i must be determined from Fig. 6-13.

$$V_i = I_e h_{ib} + I_e R_B - I_c R_B$$
$$= I_e h_{ib} + I_e R_B - I_e h_{fb} R_B$$
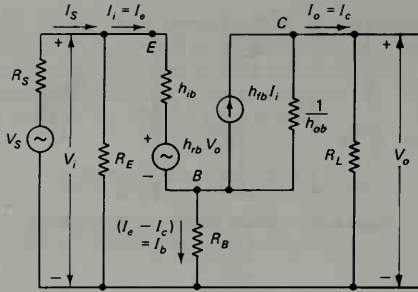$$= I_e \left[h_{ib} + R_B - h_{fb} R_B \right]$$

Figure 6-13. h-parameter equivalent of CB circuit without bypass capacitor at the base.

and

$$Z_i = \frac{V_i}{I_i} = \frac{V_i}{I_e}$$

Therefore,

$$Z_i = h_{ib} + R_B(1 - h_{fb}) \tag{6-22}$$

Using typical values of $R_1 = 33$ kΩ and $R_2 = 22$ kΩ, R_B is calculated as 13.2 kΩ. For $h_{ib} = 30$ Ω, $h_{fb} = 0.98$, and $R_B = 13.2$ kΩ, a typical value of Z_i is 294 Ω. This is considerably larger than the 30-Ω value of Z_i when the base shunting capacitor is present. Once again, it is possible to very quickly tell the circuit input impedance, almost just by looking at the circuit.

Equations (6-21) and (6-22) give the input impedance to the emitter terminal of the transistor. The actual circuit input impedance is Z_i in parallel with R_E.

$$Z_i' = Z_i \| R_E \tag{6-23}$$

6-7.2
Output
Impedance

Looking into the collector and base terminals of the CB circuit, a large resistance $(1/h_{ob})$ is seen. Since the output circuit has little effect upon the input of a common base circuit, the output impedance may be taken as $1/h_{ob}$. Thus,

$$Z_o \approx \frac{1}{h_{ob}} \tag{6-24}$$

As always, the equation for Z_o gives the device output resistance. The actual circuit output resistance is R_L in parallel with Z_o.

$$Z_o' = R_L \| Z_o \tag{6-25}$$

R_L is usually much smaller than $1/h_{ob}$, so the circuit output impedance is approximately R_L. Here again a circuit output impedance can be quickly estimated just by looking at the circuit.

$$A_v = \frac{V_o}{V_i}$$

From Fig. 6-12, $V_o = I_c R_L$ and $V_i \approx I_e h_{ib}$. Thus,

$$A_v \approx \frac{I_c R_L}{I_e h_{ib}}$$

or

$$A_v \approx \frac{h_{fb} R_L}{h_{ib}} \tag{6-26}$$

Using typical values of $h_{fb} = 0.98$, $R_L = 10$ kΩ, and $h_{ib} = 30$ Ω, the voltage gain is 327. This is similar to the typical voltage gain calculated for the CE circuit. No minus sign is present in the CB voltage gain equation, indicating that the output voltage is in phase with the input voltage. Note also that Eq. (6-26) was derived for the circuit with the base bypass capacitor included (Fig. 6-12). When C_b is absent, V_o and V_i are derived as follows from Fig. 6-13:

$$V_o = I_c R_L$$

and

$$V_i = I_e h_{ib} + I_e R_B - I_c R_B$$
$$= I_e h_{ib} + I_e R_B - I_e h_{fb} R_B$$
$$= I_e \left[h_{ib} + R_B (1 - h_{fb}) \right]$$
$$A_v = \frac{I_c R_L}{I_e \left[h_{ib} + R_B (1 - h_{fb}) \right]}$$
$$= \frac{h_{fb} R_L}{h_{ib} + R_B (1 - h_{fb})} \tag{6-27}$$

Again taking typical values of $h_{fb} = 0.98$, $R_L = 10$ kΩ, $h_{ib} = 30$ Ω, $R_1 = 33$ kΩ, and $R_2 = 22$ kΩ, A_v is 33.3. This is significantly smaller than the typical voltage gain of 327 obtained when C_B is included in the circuit. Note that Eqs. (6-26) and (6-27) can each be written as

$$A_v = \frac{h_{fb} \times (\text{output impedance})}{\text{input impedance}}$$

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_e}$$

$$= h_{fb} \qquad (6\text{-}28)$$

A typical value of h_{fb} is 0.98. Equation (6-28) applies for the circuit both with C_B included and without C_B. Once again, the expression developed for current gain represents the current gain of the device. The signal current is divided between R_E and Z_i, giving a lower value of circuit current gain than that obtained by the use of Eq. (6-28).

$$A_i' = \frac{h_{fb}R_E}{R_E + Z_i} \qquad (6\text{-}29)$$

Since R_E is usually much greater than Z_i for a CB circuit, the value of A_i' is usually approximately equal to h_{fb}.

The formula for CB power gain is the same as for all other circuits.

$$A_p = A_v \times A_i \qquad (6\text{-}30)$$

Where A_i' is significantly different from A_i, the circuit power gain becomes

$$A_p = A_v \times A_i' \qquad (6\text{-}31)$$

Using the typical values of $A_v = 327$ and $A_i = 0.98$, A_p is 320. Without C_B in the circuit, a typical A_v is 33.3 and A_p is 32.7.

With C_B Included in the Circuit

Input impedance $\quad Z_i \approx h_{ib} = 30\ \Omega \quad$ typically

Circuit input impedance $\quad Z_i' \approx h_{ib} \| R_E$

Output impedance $\quad Z_o \approx \dfrac{1}{h_{ob}} = 1\ \text{M}\Omega \quad$ typically

Circuit output impedance $\quad Z_o' \approx R_L \| \dfrac{1}{h_{ob}}$

Voltage gain $\quad A_v \approx \dfrac{h_{fb}R_L}{h_{ib}} = 327 \quad$ typically

Current gain $\quad A_i = h_{fb} = 0.98 \quad$ typically

Circuit current gain $\quad A_i' = \dfrac{h_{fb}R_E}{R_E + Z_i}$

Power gain $\quad A_p = A_v \times A_i = 320 \quad$ typically

Circuit power gain $\quad A_p' = A_v \times A_i$

With C_B Absent from the Circuit

137
Common
Base
h-Parameter
Analysis

Input impedance $Z_i \approx h_{ib} + R_B(1 - h_{fb})$

Circuit input impedance $Z_i' = R_E \| Z_i$

Voltage gain $A_v \approx \dfrac{h_{fb} R_L}{h_{ib} + R_B(1 - h_{fb})}$

The common base circuit provides voltage gain and power gain, but no current gain. Like the common emitter circuit, it has a high output impedance. But unlike the common emitter circuit, its input impedance is very low, and this renders it unsuitable for most voltage amplifier applications. It is normally applied only for very high frequency voltage amplification.

For the common base circuit in Fig. 6-14, the transistor parameters are $h_{ib} = 27.6 \ \Omega$, $h_{fb} = 0.987$, and $h_{ob} = 10^{-6}$ S. Calculate the values of input and output impedance, and the voltage, current, and power gains for the circuit.

Example 6-4

solution

From Eq. (6-21),

$$Z_i \approx 27.6 \ \Omega$$

From Eq. (6-23), the circuit input impedance is

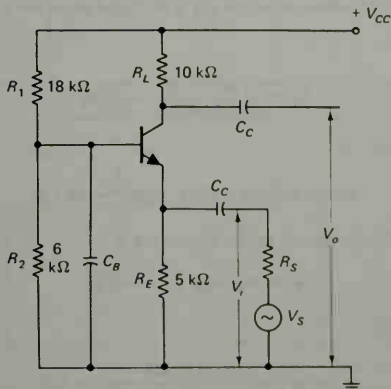$$Z_i' \approx 27.6 \ \Omega \| 5 \ \text{k}\Omega \approx 27.4 \ \Omega$$

Figure 6-14. Circuit for Example 6-4

From Eq. (6-24),

$$Z_o \approx \frac{1}{10^{-6}} \approx 1 \text{ M}\Omega$$

and from Eq. (6-25), the circuit output impedance is

$$Z_o' = R_L \| Z_o \approx 10 \text{ k}\Omega$$

From Eq. (6-26),

$$A_v \approx \frac{0.987 \times 10 \text{ k}\Omega}{27.6 \text{ }\Omega} = 358$$

From Eq. (6-28),

$$A_i = 0.987$$

From Eq. (6-29), the actual circuit current gain is

$$A_i' = \frac{0.987 \times 5 \text{ k}\Omega}{27.6 \text{ }\Omega + 5 \text{ k}\Omega} = 0.98$$

From Eq. (6-31), the power gain is

$$A_p = A_o \times A_i' = 358 \times 0.98 = 351$$

Example 6-5   Calculate the new values of input impedance and voltage gain for the circuit of Fig. 6-14 when capacitor C_B is removed from the circuit.

solution

$$R_B = \frac{18 \text{ k}\Omega \times 6 \text{ k}\Omega}{18 \text{ k}\Omega + 6 \text{ k}\Omega} = 4.5 \text{ k}\Omega$$

From Eq. (6-22),

$$Z_i = 27.6 \text{ }\Omega + 4.5 \text{ k}\Omega(1 - 0.987) = 86.1 \text{ }\Omega$$

From Eq. (6-23), the circuit input impedance is

$$Z_i' = 86.1 \text{ }\Omega \| 5 \text{ k}\Omega = 84.6 \text{ }\Omega$$

From Eq. (6-27),

$$A_v = \frac{0.987 \times 10 \text{ k}\Omega}{27.6 \text{ }\Omega + 4.5 \text{ k}\Omega(1 - 0.987)} = 115$$

When the output of one circuit (or one stage of an amplifier) is connected to the input of another stage, as shown in Fig. 6-15(a), the circuits are said to be connected in cascade. A signal applied at the input is amplified by the first stage and then further amplified by the second stage. If stage 1 has a voltage gain of 100, and stage 2 has a voltage gain of 200, then the overall voltage gain is (100×200) or 20,000. In calculating the gain of the first stage it must be noted that the input impedance of stage 2 is in parallel with the load resistance of stage 1, and this affects the voltage gain of stage 1.
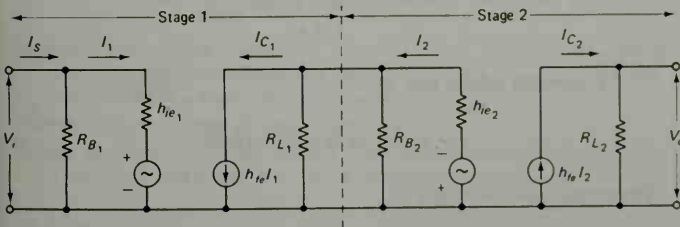
The first step in analyzing the circuit of Fig. 6-15(a) is to draw the ac equivalent circuit by replacing the supply voltage and all capacitors with short circuits. This gives the circuit shown in Fig. 6-15(b). The transistor
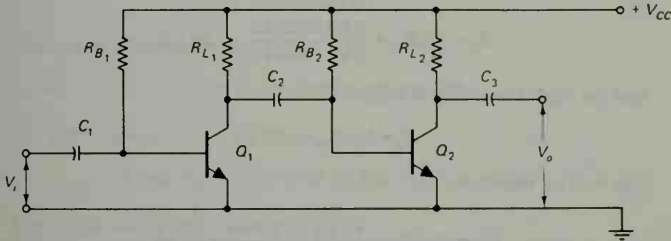
(a) Two staged cascaded CE amplifier circuit
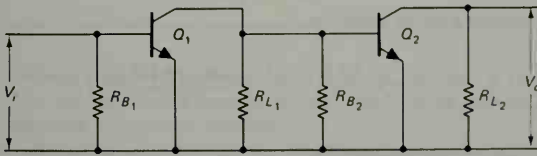
(b) ac equivalent circuit of two stage CE amplifier

(c) h-parameter equivalent circuit for two stage CE amplifier

Figure 6-15. Two-stage cascaded CE amplifier, ac equivalent, and h-parameter equivalent circuit.

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h-parameter equivalent circuits are next substituted into the ac equivalent circuit to give the *h*-parameter circuit of Fig. 6-15(c). The circuit is then analyzed stage by stage.

Example 6-6

In the circuit of Fig. 6-15, both transistors have $h_{fe} = 100$ and $h_{ie} = 2$ kΩ. Also, $R_{L1} = R_{L2} = 4.7$ kΩ and $R_{B1} = R_{B2} = 330$ kΩ. Calculate the input and output impedances of the circuit, and the overall voltage, current, and power gains.

solution

Circuit input impedance:

$$Z_{i1}' = h_{ie} \| R_{B1} = \frac{2 \text{ kΩ} \times 330 \text{ kΩ}}{2 \text{ kΩ} + 330 \text{ kΩ}} = 1.99 \text{ kΩ}$$

and the input impedance of stage 2 is

$$Z_{i2}' = h_{ie} \| R_{B2} = 1.99 \text{ kΩ}$$

The load on stage 1 is

$$R_{L1}' = R_{L1} \| Z_{i2}' = \frac{4.7 \text{ kΩ} \times 1.99 \text{ kΩ}}{4.7 \text{ kΩ} + 1.99 \text{ kΩ}} = 1.4 \text{ kΩ}$$

The voltage gain for stage 1 is

$$A_v = \frac{h_{fe}(R_{L1} \| Z_{i2}')}{h_{ie}} = \frac{100 \times 1.4 \text{ kΩ}}{2 \text{ kΩ}} = 70$$

The voltage gain for stage 2 is

$$A_v = \frac{h_{fe} R_{L2}}{h_{ie}} = \frac{100 \times 4.7 \text{ kΩ}}{2 \text{ kΩ}} = 235$$

The overall voltage gain is

$$A_v = A_{v1} \times A_{v2} = 70 \times 235 = 16,450$$

The current gain for stage 1 is

$$A_i = \frac{h_{fe} R_B}{R_B + Z_i}$$

where Z_i is the device input impedance.

$$Z_i = h_{ie} = 2 \text{ k}\Omega$$

$$A_i = \frac{100 \times 330 \text{ k}\Omega}{330 \text{ k}\Omega + 2 \text{ k}\Omega} = 99.4$$

Current I_{c1} in Fig. 6-15(c) is divided between h_{ie2} and the parallel combination of R_{L1} and R_{B2}.

$$A_{i2} = \frac{h_{fe2}(R_{B2} \| R_{L1})}{(R_{B2} \| R_{L1}) + h_{ie2}} = \frac{100 \times (4.7 \text{ k}\Omega \| 330 \text{ k}\Omega)}{(4.7 \text{ k}\Omega \| 330 \text{ k}\Omega) + 2 \text{ k}\Omega}$$

$$= \frac{100 \times 4.63 \text{ k}\Omega}{4.63 \text{ k}\Omega + 2 \text{ k}\Omega} = 69.8$$

The overall current gain is

$$A_i = A_{i1} \times A_{i2} = 99.4 \times 69.8 = 6938$$

The power gain is

$$A_p = A_v \times A_i = 1.645 \times 10^4 \times 6.938 \times 10^3 = 1.14 \times 10^8$$

The circuit output impedance is

$$Z_o \approx R_{L2} = 4.7 \text{ k}\Omega$$

Common emitter circuit. Transistor circuit in which the input is applied between base and emitter, and the output is taken across collector and emitter; used as a voltage amplifier.

Glossary of Important Terms

Common collector circuit. Transistor circuit in which the input is applied between base and collector, and the output is taken across emitter and collector; used as a high-input impedance, low-output impedance circuit.

Common base circuit. Transistor circuit in which the input is applied between emitter and base; and the output is taken across collector and base; used as a high-frequency amplifier.

Emitter follower. Same as *common collector circuit.*

Buffer amplifier. Amplifier with a high-input resistance, a low-output resistance, and a gain of 1; e.g., a common collector circuit.

6-1. Sketch a practical common emitter circuit showing all current dirrections and voltage polarities. Identify input and output and all components.

Review Questions

6-2. List the characteristics of a CE circuit and state its usual application.

6-3. Sketch the ac equivalent circuit for a CE circuit. Also sketch the h-parameter equivalent for the CE circuit. Identify all components and state typical values.

6-4. Sketch a practical CE circuit with an emitter resistance included. Show how the inclusion of R_E affects the h-parameter equivalent circuit.

6-5. Repeat Question 6-1 for a common collector circuit.

6-6. Repeat Question 6-2 for a CC circuit.

6-7. Repeat Question 6-3 for a CC circuit.

6-8. Repeat Question 6-1 for a common base circuit.

6-9. Repeat Question 6-2 for a CB circuit.

6-10. Repeat Question 6-3 for a CB circuit.

Problems

6-1. A common emitter circuit uses a transistor with $h_{fe} = 40$, $h_{ie} = 1$ kΩ, and $h_{oe} = 10^{-6}$ S. Load resistance R_L is 3.3 kΩ and bias resistance $R_B = 120$ kΩ. Calculate the input impedance, output impedance, voltage gain, current gain, and power gain.

6-2. If the circuit described in Problem 6-1 has a 330-Ω emitter resistance included, calculate the new values of all impedances and gains.

6-3. A common collector circuit employs a transistor with $h_{fe} = 40$ and $h_{ie} = 1$ kΩ. The load resistance $R_L = 20$ kΩ, and the bias resistances are $R_1 = 33$ kΩ, $R_2 = 47$ kΩ. The signal source has a resistance $R_S = 600$ Ω. Determine all impedances and gains for the circuit.

6-4. A common base circuit uses a transistor with $h_{ib} = 50$ Ω, $h_{fb} = 0.99$, and $h_{ob} = 10^{-6}$ S. The value of R_L is 3.9 kΩ and $R_E = 2.2$ kΩ. Determine all gains and impedances for the circuit.

6-5. The circuit of Problem 6-4 has bias resistances $R_1 = 27$ kΩ and $R_2 = 18$ kΩ. If no bypassing capacitor is provided at the base of the transistor, calculate the new values of input impedance, voltage gain, and power gain for the circuit.

6-6. A two-stage common emitter amplifier uses transistors which each have $h_{fe} = 80$ and $h_{ie} = 1.5$ kΩ. $R_{L1} = R_{L2} = 8.2$ kΩ and $R_{B1} = R_{B2} = 220$ kΩ. Calculate the input and output impedances of the circuit, and the overall voltage, current, and power gains.

6-7. A two-stage amplifier consists of two identical common emitter stages as described in Problem 6-1. Calculate the overall voltage and current gains of the circuit.

6-8. The common collector circuit described in Problem 6-3 is capacitor coupled to the output of the common emitter circuit in Problem 6-2. Calculate the overall voltage and current gains of the circuit.

Transistor and Integrated Circuit Fabrication

The methods employed to manufacture a transistor determine its electrical characteristics, and thus dictate the applications for which it may be used. For example, low-current, fast-switching transistors must be designed differently from high-power transistors.

An integrated circuit (IC) consists of many components making up a complete circuit in one small package. The major types of IC's are *monolithic*, *thin-film*, *thick-film*, and *hybrid* circuits. For mass production, the monolithic process is the most economical, but it does have some disadvantages.

7-1
Introduction

Current Gain. Good current gain requires that most charge carriers from the emitter pass rapidly to the collector. Thus, there should be little outflow of charge carriers via the base terminal, and there should be few carrier recombinations within the base region. These conditions dictate a very narrow, lightly doped base region.

7-2
Effects of Transistor Construction on Electrical Performance

High Power. High-power transistors must have large emitter surfaces to provide the required quantities of charge carriers. Large collector surface

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areas are also required to dissipate the power involved without overheating the collector–base junction.

Frequency Response. For greatest possible frequency response, the base region should be very narrow in order to ensure a short transit time of charge carriers from emitter to collector. Input capacitance must also be a minimum, and this requires a small area emitter–base junction, as well as a highly resistive (i.e., lightly doped) base region.

Since power transistors require large emission surfaces, and high-frequency performance demands small emitter–base areas, there is a conflict in high-frequency power transistors. To keep the junction area to a minimum and still provide adequate charge carrier emission, the emitter–base junction is usually in the form of a long thin zigzag strip.

Switching Transistors. Fast switching demands the same low junction capacitances that are required for good high-frequency performance. A good switching transistor must also have low *saturation voltages* and a short *storage time* (see Section 8-7). For low saturation voltages, the collector regions must have low resistivity. Short storage time demands fast recombinations of charge carriers left in the depletion region at the saturated (i.e., forward biased) collector–base junction. This fast recombination is assisted by additional doping of the collector with gold atoms.

Breakdown and Punch-Through. Since the collector–base junction is operated with reverse bias, the usable collector potential is limited by its reverse breakdown voltage. To achieve high breakdown voltages, either the collector region or the base region must be very lightly doped.

The depletion region at the collector–base junction penetrates deepest into the most lightly doped side. If the base is more lightly doped than the collector, the collector–base depletion region will penetrate deep into the base. If it spreads far enough into the base, it may link up with the emitter–base depletion region. When this happens, a state of *punch-through* is said to exist, and dangerously large currents may flow. To avoid punch-through, the collector region is sometimes more lightly doped than the base. The collector–base depletion region then spreads into the collector, rather than the base.

7-3
Processing of
Semiconductor
Materials

Preparation of Silicon and Germanium. Silicon is one of the commonest elements on the earth. It occurs as silicon dioxide (SiO_2) and as silicates, or mixtures of silicon and other materials. Germanium is derived from zinc or copper ores. When converted to bulk metal, both silicon and germanium contain large quantities of impurities. Both metals must be carefully refined before they can be used for device manufacture.

Semiconductor material is normally *polycrystalline* after it has been refined. This means that it is made up of many individual formations of

atoms with no overall fixed pattern of relationship between them. For use in transistors the material must be converted into *single crystal* material; i.e., it must be made to follow a single atomic formation pattern throughout.

In its final refined form for electronic device manufacture, the silicon or germanium is in single crystal bars about 2.5 cm in diameter and perhaps 30 cm long. The bars are sliced into disc-shaped wafers about 0.4 mm thick, and the wafers are polished to a mirror surface. Several thousand transistors are fabricated upon the surface of each wafer; then it is scribed and cut like glass.

Diffusion and Epitaxial Growth. When wafers of n-type material are heated to a very high temperature in an atmosphere containing p-type impurities [Fig. 7-1(a)] some of the impurities are absorbed or *diffused* into each wafer. The outer layer of the n-type material is converted into p-type.

The process can be continued by further heating the material in an atmosphere containing n-type impurities. Thus, the wafer can have an outer n-type layer, with a p-type layer just below it, and an n-type center. This is
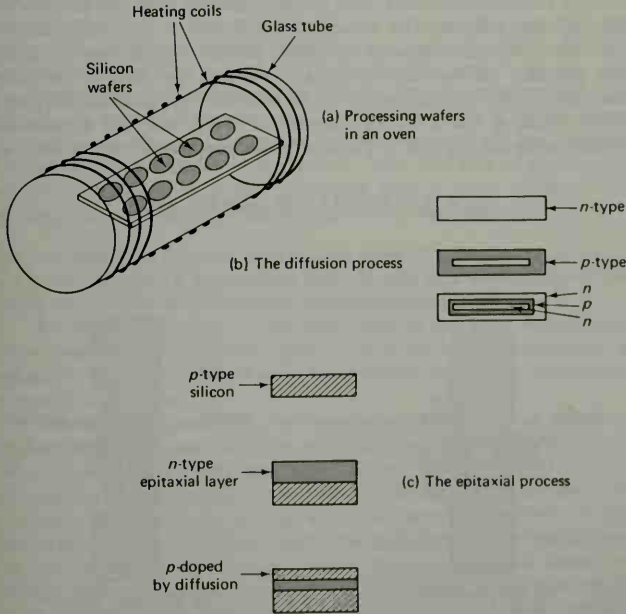

Figure 7-1. Diffusion and epitaxial growth.

the *diffusion process* illustrated in Fig. 7-1(a) and (b). Since the process is very slow (about 2.5 μm/hour), very narrow diffused regions can be accurately produced by careful timing.

The epitaxial process [Fig. 7-1(c)] is similar to the diffusion process, except that atoms of germanium or silicon are contained in the gas surrounding the semiconductor wafer. The semiconductor atoms in the gas *grow* on the wafer in the form of a very thin layer. This layer is single crystal material, and may be *p*-type or *n*-type, according to the impurity content in the gas. The epitaxial layer may then be doped by the diffusion process.

7-4
Transistor
Fabrication

Alloy Transistors. For manufacture of *alloy transistors*, single crystal *n*-type wafers are cut up into many small sections or *dice*, which each form the substrate for one transistor. A small pellet of *p*-type material is melted on one side of the substrate until it partially penetrates and forms an alloy with the substrate [Fig. 7-2(a)]. This process, which forms a *pn*-junction, is then repeated on the other side of the substrate to form a *pnp* transistor. One of the *pn*-junctions has a large area, and one has a small area. The small-area junction becomes the emitter–base junction, and the large one becomes the collector–base junction. One reason for this is that the large area junction will most easily collect most of the charge carriers emitted from the small-area junction. Another more important reason is that most of the power dissipation in the transistor occurs at the collector–base junction. Suppose a silicon transistor has a collector current of $I_C = 10$ mA and a collector–emitter voltage of $V_{CE} = 10$ V. The total power dissipated in the transistor is

$$P = V_{CE} \times I_C = 10 \text{ V} \times 10 \text{ mA} = 100 \text{ mW}$$

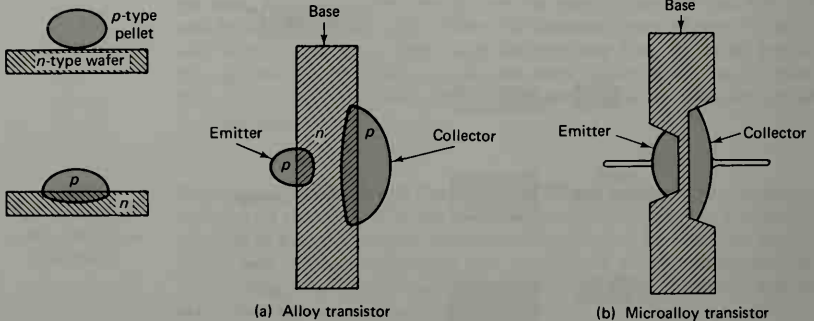(a) Alloy transistor   (b) Microalloy transistor

Figure 7-2. Alloy and microalloy transistors.

The emitter–base voltage is $V_{BE} = 0.7$ V, and the collector–base voltage is

$$V_{CB} = V_{CE} - V_{BE} = 10 \text{ V} - 0.7 \text{ V} = 9.3 \text{ V}$$

The power dissipated at the emitter–base junction is

$$V_{BE} \times I_C = 0.7 \text{ V} \times 10 \text{ mA} = 7 \text{ mW}$$

At the collector-base junction, the power dissipated is

$$V_{CB} \times I_C = 9.3 \text{ V} \times 10 \text{ mA} = 93 \text{ mW}$$

Microalloy Transistors. Because very narrow base widths are difficult to obtain with alloy transistors, they cannot be made to perform well at high frequencies. To improve the high-frequency performance, holes are first etched partially into the substrate from each side, leaving a very thin portion between. By a plating process, surfaces of impurity material are formed on each side of the thin n-type portion [Fig. 7-2(b)]. Heat is then applied to alloy the impurities into the base region. This process results in very thin base regions and good high-frequency performance.

Microalloy Diffused Transistors. In microalloy transistors, the collector– base depletion region penetrates deeply into the very thin base. Thus, a major disadvantage is that *punch-through* can occur at very low collector voltages. In microalloy diffused transistors the substrate used is initially undoped. After the holes are etched in each side of the wafer to produce the thin base region, the base is doped by diffusion from the collector side. The diffusion can be carefully controlled so that the base region is heavily doped at the collector side, with the doping becoming progressively less until the material is almost intrinsic at the emitter. With this kind of doping, the collector–base depletion region penetrates only a short distance into the base, and much higher punch-through voltages are achieved.

Diffused Mesa. In the production of mesa transistors, the thin wafer is kept as a whole disc (i.e., it is not diced first). Several thousand transistors are simultaneously formed on the wafer, by the diffusion process.

As illustrated in Fig. 7-3 the main body of the wafer becomes the n-type collectors, the diffused p-regions become the bases, and the final n regions are the emitters. Metal strips are deposited on the base and emitter surfaces to form contacts.

The individual transistors could be separated by the usual process of scribing lines on the surface of the wafer and breaking it into individual units. This would give a very rough edge, however, and there would likely be high leakage between collector and base. So, before cutting the disc, the transistors are isolated by etching away the unwanted portions of the diffused area to form separating *troughs* between devices. This leaves the base and emitter regions projecting above the main wafer which forms the collector region. This is the *mesa* structure. The narrow base widths which can be achieved by the diffusion process make the mesa transistor useful at very high frequencies.
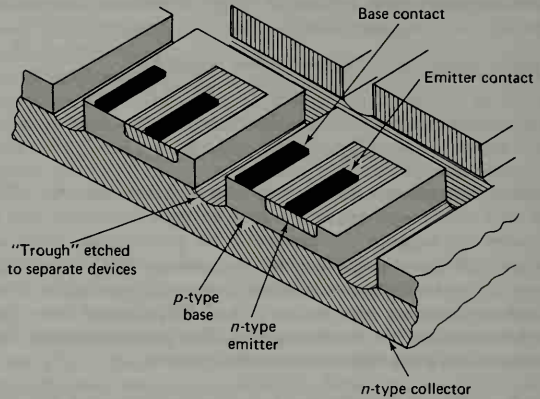
Figure 7-3. Mesa transistors.

Epitaxial Mesa. One of the disadvantages of the process just described is that because the collector region is highly resistive diffused mesa transistors have a high *saturation voltage* (see Sect. 8-7). Such devices are unsuitable for saturated switching applications. This same characteristic (high collector resistance) is desirable to give high punch-through voltages. One way to achieve both high punch-through voltage and low saturation levels is to employ the epitaxial process.

Starting with a low-resistive (i.e., highly doped) wafer, a thin, highly resistive epitaxial layer is grown. This layer becomes the collector, and the base and emitter are diffused as before. The arrangement is illustrated in Fig. 7-4. Now the punch-through voltage is high because the collector–base depletion region spreads deepest into the lightly doped collector. Saturation voltage is low, because the collector region is very narrow, and the main body of the wafer through which collector current must flow has a very low resistance.
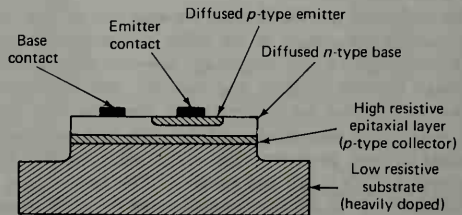
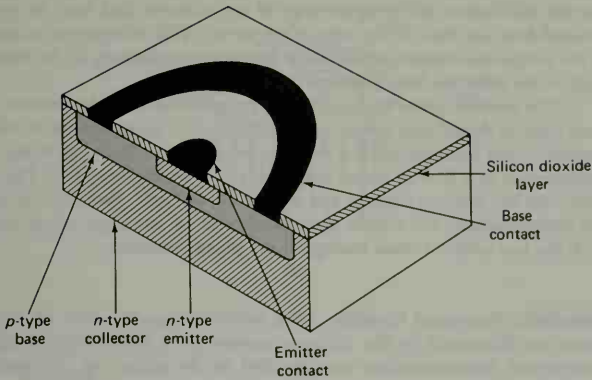**Figure 7-4.** Epitaxial mesa transistor.

Figure 7-5. Planar transistor.

Diffused Planar Transistor. In all the previously described transistors the collector–base junction is exposed (within the transistor package), and substantial charge carrier leakage can occur at the junction surface. In the planar transistor (Fig. 7-5) the collector–base junction is covered with a layer of silicon dioxide. This construction gives a very low collector–base leakage current. I_{CBO} may be typically 0.1 nA.

Annular Transistor. A problem which occurs particularly with *pnp* planar transistors is the *induced channel*. This results when a relatively high voltage is applied to the silicon dioxide surface, e.g., a voltage at one of the terminals. Consider the *pnp* structure shown in Fig. 7-6. If the surface of the silicon dioxide becomes positive, minority charge carriers within the lightly doped *p*-type substrate are attracted by the positive potential. The minority charge
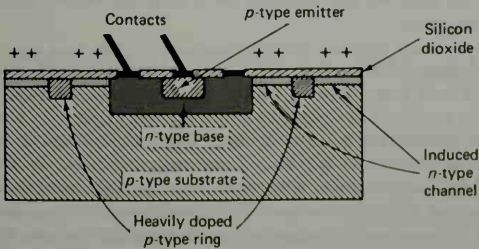
Figure 7-6. Annular transistor.

carriers concentrate at the upper edge of the substrate and form an n-type channel from the base to the edge of the device. This becomes an extension of the n-type base region and results in charge carrier leakage at the exposed edge of the collector–base junction.

The problem arises because the p-type/substrate is highly resistive. If it were heavily doped with p-type charge carriers, the concentration of n-type carriers would be absorbed; i.e., electrons would be swallowed by holes. The introduction of a heavily doped p-type ring around the base, as in Fig. 7-6, interrupts the induced channel and isolates the collector–base junction from the device surface. The annual transistor, therefore, is a high-voltage device with the low collector–base leakage of the planar transistor.

7-5
Integrated
Circuit
Fabrication

Monolithic Integrated Circuits. In a *monolithic integrated circuit* all components are fabricated by the diffusion process on a single chip of silicon. Component interconnections are provided on the surface of the structure and external connecting wires are taken out to terminals as illustrated in Fig. 7-7(a). Although the monolithic circuit has distinct disadvantages, the vast majority of integrated circuits use this type of construction because it is the most economical process for mass production.

Thin-Film Integrated Circuits. Thin-film integrated circuits are constructed by depositing films of conducting material on the surface of a glass or ceramic base. By controlling the width and thickness of the films, and using different materials selected for their resistivity, resistors and conductors are fabricated. Capacitors are produced by sandwiching a film of insulating oxide between two conducting films. Inductors are made by depositing a spiral formation of film. Transistors and diodes cannot be produced by thin-film techniques; tiny discrete components must be connected into the circuit.

One method employed to produce thin films is *vacuum evaporation*, in which vaporized material is deposited on a substrate contained in a vacuum. In another method, called *cathode sputtering*, atoms from a cathode made of the desired film material are deposited on a substrate located between a cathode and an anode.

Thick-Film Integrated Circuits. *Thick-film* integrated circuits are sometimes referred to as *printed thin-film circuits*. In this process *silk-screen printing* techniques are employed to create the desired circuit pattern on a ceramic substrate. The screens are actually made of fine stainless steel wire mesh, and the *inks* are pastes which have conductive, resistive, or dielectric properties. After printing, the circuits are high temperature fired in a furnace to fuse the films to the substrate. Thick-film passive components are fabricated in the same way as those in thin-film circuits. As with thin-film circuits, active components must be added as separate devices. A portion of a thick-film circuit is shown in Fig. 7-7(b).
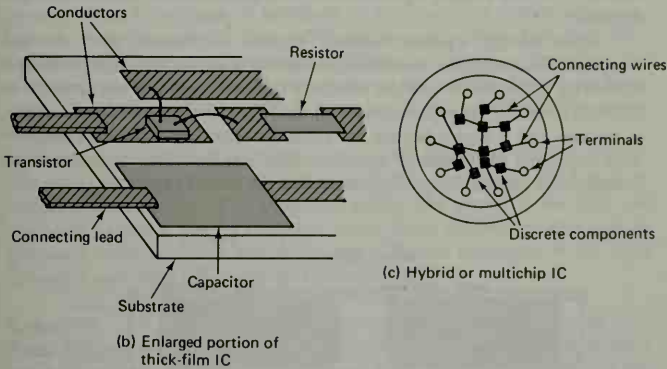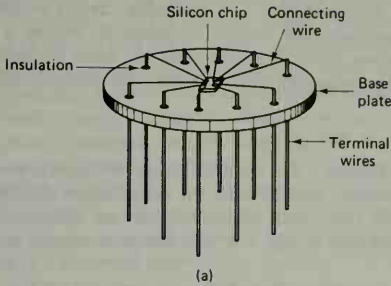
Figure 7-7. Construction of monolithic, thick-film, and hybrid integrated circuits.

Integrated circuits produced by *thin-* or *thick-film* techniques usually have better component tolerances and give better high-frequency performance than monolithic integrated circuits.

Hybrid or Multichip Integrated Circuits. Figure 7-7(c) illustrates the structure of a *hybrid* or *multichip integrated circuit*. As the name implies, the circuit is constructed by interconnecting a number of individual chips. The active components are diffused transistors or diodes. The passive components may be groups of diffused resistors or capacitors on a single chip, or they may be thin-film components. Wiring or a metalized pattern provides connections between chips.

Like thin- and thick-film IC's, multichip circuits usually have better performance than monolithic circuits. Although the process is too expensive for mass production, multichip techniques are quite economical for small quantities and are frequently used as prototypes for monolithic integrated circuits.

7-6
Integrated
Circuit
Components

Transistors and Diodes. The epitaxial planar diffusion process described in Section 7-3 is normally employed for the manufacture of IC transistors and diodes. Collector, base, and emitter regions are diffused into a silicon substrate, as illustrated in Fig. 7-8, and surface terminals are provided for connection.

In discrete transistors the substrate is normally used as a collector. If this were done with transistors in a monolithic integrated circuit, all transistors fabricated on one substrate would have their collectors connected together. For this reason, separate collector regions must be diffused into the substrate.

Even though separate collector regions are formed, they are not completely isolated from the substrate. Figure 7-8 shows that a pn-junction is formed by the substrate and the transistor collector region. If the circuit is to function correctly, these junctions must never become forward biased. Thus, in the case of a p-type substrate, the substrate must always be kept negative with respect to the transistor collectors. This requires that the substrate be connected to the most negative terminal of the circuit supply.
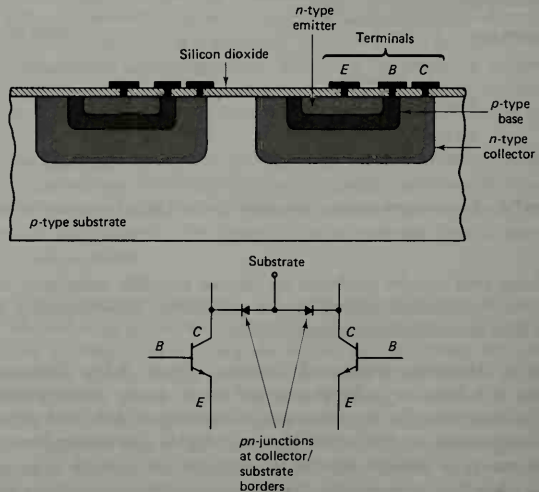

Figure 7-8. Effect of IC collector–substrate junctions.

The unwanted, or *parasitic junctions*, even when reverse biased, can still affect the circuit performance. The junction reverse leakage current can be a serious problem in circuits that are to operate at very low current levels. The capacitance of the reverse-biased junction can affect the circuit high-frequency performance, and the junction breakdown voltage imposes limits on the usable level of supply voltage. All these factors can be minimized by using highly resistive material for the substrate; i.e., if it is very lightly doped, it will behave almost as an insulator.

Integrated circuit diodes are usually fabricated by diffusion exactly as transistors. Only two of the regions are used to form one *pn*-junction, or the collector region may be connected directly to the base region so that the device operates as a saturated transistor.

Resistors. Since the resistivity of semiconductor material can be altered with doping density, resistors can be produced by doping strips of material as required. The range of resistor values that may be produced by the diffusion process varies from ohms to hundreds of kilohms. The typical tolerance, however, may be no better than $\pm 5\%$, and may even be as high as $\pm 20\%$. On the other hand, if all resistors are diffused at the same time, then the tolerance ratio can be good. For example, several resistors having the same nominal value may all be $+20\%$ in error and have actual resistance values within a few percent of each other.

Another method of producing resistors for integrated circuits uses the thin-film technique. In this process a metal film is deposited on a glass or silicon dioxide surface. The thickness, width, and length of the film are regulated to give a desired resistance value. Since diffused resistors can be processed while diffusing transistors, the diffusion technique is the least expensive and, therefore, the most frequently used.

Capacitors. All *pn*-junctions have capacitance, so capacitors may be produced by fabricating suitable junctions. As in the case of other diffused components, parasitic junctions are unavoidable. Both the parasitic and the main junction must be kept reverse biased to avoid direct current flow. The depletion region width and, therefore, the junction capacitance also vary with changes in reverse bias. Consequently, for reasonable stability in capacitor values, a dc reverse bias much greater than signal voltages must be maintained across the junction.

Integrated circuit capacitors may also be fabricated by utilizing the silicon dioxide surface layer as a dielectric. A heavily-doped *n*-region is diffused to form one plate of the capacitor. The other plate is formed by depositing a film of aluminum on the silicon dioxide which forms on the wafer surface. With this type of capacitor, voltages of any polarity may be employed, and the breakdown voltage is very much larger than that for diffused capacitors. The junction areas available for creation of integrated circuit capacitors are very small indeed, so that only capacitances of the order of picofarads are possible.

Low-power transistors may simply be encapsulated in resin and the connecting leads left protruding [Fig. 7-9(a)]. This has the advantage of cheapness, but offers a limited range of operating temperature. In another method of low-power transistor packaging [illustrated in Fig. 7-9(b)], the device is hermetically sealed in a metal can. The transistor is first mounted with its collector in contact with a heat-conducting metal base plate. Wires, which are insulated from the base plate, pass through the plate for emitter and base connections. The collector connecting wire is then welded directly to the heat-conducting plate, and the covering metal can is finally welded to the base plate.

For high-power transistor packaging, a sealed can (TO -3) is usually employed [Fig. 7-10(a)]. In this case, however, the heat-conducting plate is much larger and is designed for mounting directly on a heat sink. Connecting pins are provided for the base and the emitter, and the collector connection is made by means of the metal base plate. This is not the only form of power transistor package. For higher power dissipation there are stud-mounted devices [Fig. 7-10(b)], and for lower dissipation applications plastic packages are used [Fig. 7-10(c)].

Integrated circuits, like all semiconductor devices, must be packaged to provide mechanical protection and terminals for electrical connection. Several standard packages in general use are illustrated in Fig. 7-11.
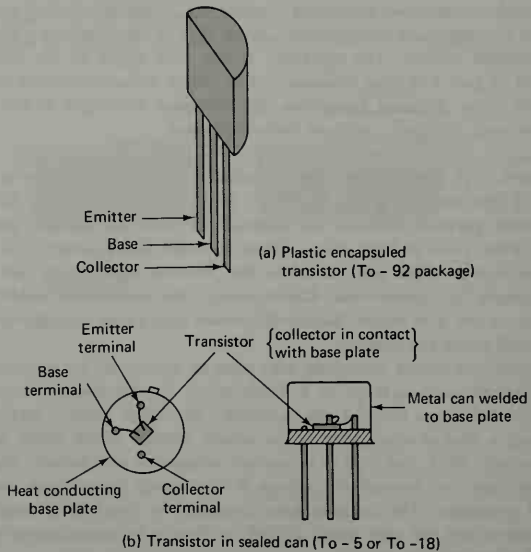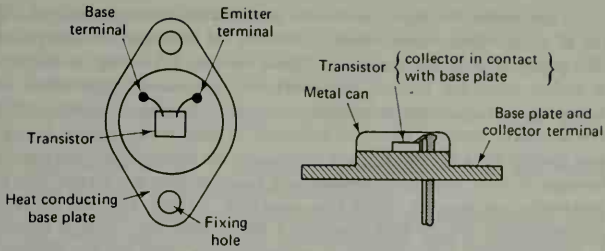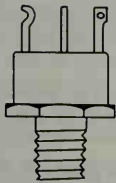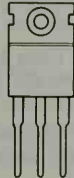

(a) Plastic encapsuled transistor (To – 92 package)

(b) Transistor in sealed can (To – 5 or To –18)

Figure 7-9. Low-power transistor packaging.

(a) Sealed can package (T_O – 3)

(b) Stud mounted type   (c) Plastic package
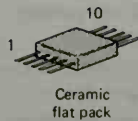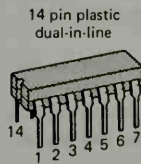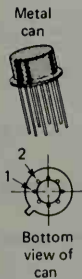
Figure 7-10. Power transistor packages.

Figure 7-11. Integrated circuit packages.

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The metal can type of container provides electromagnetic shielding for the IC chip, which cannot be obtained with the plastic or ceramic packages. The plastic dual-in-line package is much cheaper than other packages, and is widely used for general industrial and consumer applications where high-temperature performance is not required. Ceramic or metal containers are necessary where a circuit is subjected to high temperatures. Flat packs and dual-in-lines are much more convenient for circuit board use than cans, because of their lead arrangement and because they are flatter and allow greater circuit densities. TO-3 type cans [Fig. 7-10(a)] are used for packaging integrated circuits that dissipate a lot of heat, e.g., voltage regulators. Large integrated circuits such as microprocessor units use the dual-in-line type of package with perhaps 40 connecting pins.

Glossary of Important Terms

Single crystal material. Semiconductor material in which the atoms are aligned into a definite pattern throughout.

Diffusion process. Process in which semiconductor material is heated in atmosphere containing impurity atoms which soak, or diffuse, into the material.

Epitaxial growth. Layer formation of silicon or germanium atoms upon semiconductor wafer when it is heated in an atmosphere containing semiconductor atoms.

Alloy transistor. Device manufactured by a process in which small pellets of semiconductor are melted into a semiconductor wafer.

Microalloy. Transistor manufacturing technique in which holes are etched in a wafer before the alloying process.

Microalloy diffused. Extension of microalloy technique with impurities diffused into base region.

Diffused mesa. Diffused transistor with base and emitter regions raised above the main body of the semiconductor wafer.

Epitaxial mesa. Mesa transistor which is formed by epitaxial growth process.

Diffused planar. Diffused transistor in which collector–base junction is buried inside the wafer.

Annular transistor. Diffused planar transistor with added ring of heavily doped substrate around the base region.

Thick-film IC. Integrated circuit constructed by silk-screen printing techniques, using conducting and insulating inks.

Hybrid IC. Integrated circuit constructed by interconnecting several individual chip components in one package.

Multichip IC. Same as *hybrid IC*.

Monolithic integrated circuit. Integrated circuit in which components are fabricated on a single chip of silicon.

Thin-film IC. Integrated circuit constructed by depositing thin metallic films on a glass or ceramic base.

7-1. Explain the various requirements that must be fulfilled in the fabrication of transistors for maximum performance with respect to (a) current gain, (b) power dissipation, (c) frequency response, (d) switching response, (e) breakdown voltage.

7-2. Describe the process of preparing semiconductor material for device manufacture.

7-3. Explain the process of diffusion and epitaxial growth, and discuss their application to transistor manufacture.

7-4. Describe the microalloy and microalloy diffusion techniques for transistor manufacture. Explain the advantages and disadvantages of these transistors.

7-5. Using sketches, explain the diffused mesa and epitaxial mesa transistors. Discuss the reason for the mesa construction and the advantages and disadvantages of mesa transistors.

7-6. Explain the manufacturing process for diffused planar and annular transistors, and discuss their advantages and disadvantages.

7-7. Show that most of the power dissipation in a transistor occurs at the collector–base junction.

7-8. Briefly explain the thin-film and thick-film methods of integrated circuit manufacture, and discuss their advantages and disadvantages.

7-9. Using illustrations, explain the fabrication process for monolithic integrated circuits. Discuss the advantages and disadvantages of monolithic IC's.

7-10. Draw a sketch to show the construction of two diffused integrated circuit transistors. Sketch the circuit diagram of the two devices, showing the parasitic components. Explain the circuit and state any precautions necessary in the use of the device.

7-11. Briefly explain how diodes, resistors, and capacitors are fabricated in monolithic integrated circuits.

7-12. Draw sketches to illustrate typical transistor and integrated circuit packages. Briefly explain.

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CHAPTER
8

Transistor Specifications and Performance

The electrical characteristics for each type of transistor are specified on a data sheet published by the device manufacturer. The specifications must be correctly interpretated if transistor failure is to be avoided and optimum performance achieved. The maximum power that may be dissipated in the device is normally listed for a temperature of 25° C. This must be derated for operation at higher temperatures. Transistor cutoff frequency is usually defined for the case of a common base circuit. There is an equation which relates the common emitter cutoff frequency to the common base cutoff frequency. Other items that depend upon the circuit configuration are input capacitance, noise figure, current gain, and switching time.

To select a transistor for a particular application, the data sheets provided by device manufacturers must be consulted. Portions of typical data sheets are shown in Figs. 8-1 and 8-2.

Most data sheets start off with the device type number at the top of the page, a descriptive title, and a list of major applications of the device. This is

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2N3903 (SILICON)
2N3904

$V_{CB} = 60$ V
$I_C = 200$ mA
$C_{ob} = 4.0$ pf (max)

CASE 29
(TO-92)

NPN silicon annular transistors, designed for general purpose switching and amplifier applications, features one-piece, injection-molded plastic package for high reliability. The 2N3903 and 2N3904 are complementary with types 2N3905 and 2N3906, respectively.

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CB}	60	Vdc
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Emitter-Base Voltage	V_{EB}	6	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ $T_A = 60°C$	P_D	210	mW
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	310 2.81	mW $mW/°C$
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	$°C/mW$
Junction Operating Temperature	T_J	135	$°C$
Storage Temperature Range	T_{stg}	-55 to +135	$°C$

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Base Breakdown Voltage ($I_C = 10 \mu Adc, I_E = 0$)	BV_{CBO}	60	—	Vdc
Collector-Emitter Breakdown Voltage* ($I_C = 1$ mAdc)	$BV_{CEO}*$	40	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu Adc, I_C = 0$)	BV_{EBO}	6	—	Vdc
Collector Cutoff Current ($V_{CE} = 40$ Vdc, $V_{OB} = 3$ Vdc)	I_{CEX}	—	50	nAdc
Base Cutoff Current ($V_{CE} = 40$ Vdc, $V_{OB} = 3$ Vdc)	I_{BL}	—	50	nAdc

*Pulse Test Pulse Width 300 μsec, Duty Cycle = 2% V_{OB} Base Emitter Reverse Bias

Figure 8-1. Typical transistor data sheet.

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ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain *	h_{FE}*			—
(I_C = 0.1 mAdc, V_{CE} = 1 Vdc) 2N3903		20	—	
2N3904		40	—	
(I_C = 1.0 mAdc, V_{CE} = 1 Vdc) 2N3903		35	—	
2N3904		70	—	
(I_C = 10 mAdc, V_{CE} = 1 Vdc) 2N3903		50	150	
2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1 Vdc) 2N3903		30	—	
2N3904		60	—	
(I_C = 100 mAdc, V_{CE} = 1 Vdc) 2N3903		15	—	
2N3904		30	—	
Collector-Emitter Saturation Voltage*	$V_{CE(sat)}$*			Vdc
(I_C = 10 mAdc, I_B = 1 mAdc)		—	0.2	
(I_C = 50 mAdc, I_B = 5 mAdc)		—	0.3	
Base-Emitter Saturation Voltage*	$V_{BE(sat)}$*			Vdc
(I_C = 10 mAdc, I_B = 1 mAdc)		0.65	0.85	
(I_C = 50 mAdc, I_B = 5 mAdc)		—	0.95	
SMALL SIGNAL CHARACTERISTICS				
High Frequency Current Gain 2N3903	$|h_{fe}|$	2.5	—	—
(I_C = 10 mA, V_{CE} = 20 V, f = 100 mc) 2N3904		3.0	—	
Current-Gain—Bandwidth Product 2N3903	f_T	250	—	mc
(I_C = 10 mA, V_{CE} = 20 V, f = 100 mc) 2N3904		300	—	
Output Capacitance	C_{ob}	—	4	pf
(V_{CB} = 5 Vdc, I_E = 0, f = 100 kc)				
Input Capacitance	C_{ib}	—	8	pf
(V_{OB} = 0.5 Vdc, I_C = 0, f = 100 kc)				
Small Signal Current Gain 2N3903	h_{fe}	50	200	—
(I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc) 2N3904		100	400	
Voltage Feedback Ratio 2N3903	h_{re}	0.1	5.0	X10^{-4}
(I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc) 2N3904		0.5	8.0	
Input Impedance 2N3903	h_{ie}	0.5	8	Kohms
(I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc) 2N3904		1.0	10	
Output Admittance	h_{oe}	1.0	40	μ mhos
(I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc) Both Types				
Noise Figure	NF			db
(I_C = 100 μA, V_{CE} = 5 V, R_g = 1 Kohms, 2N3903		—	6	
Noise Bandwidth = 10 cps to 15.7 kc) 2N3904		—	5	
SWITCHING CHARACTERISTICS				
Delay Time	V_{CC} = 3 Vdc, V_{OB} = 0.5 Vdc,	t_d	—	35	nsec
Rise Time	I_C = 10 mAdc, I_{B1} = 1 mA	t_r	—	35	nsec
Storage Time	V_{CC} = 3 Vdc, I_C = 10 mAdc, 2N3903	t_s	—	175	nsec
	I_{B1} = I_{B2} = 1 mAdc 2N3904		—	200	
Fall Time		t_f	—	50	nsec

*Pulse Test: Pulse Width = 300 μsec, Duty Cycle = 2% V_{OB} = Base Emitter Reverse Bias

Figure 8-1.   (cont.)

FOR POWER-AMPLIFIER APPLICATIONS

mechanical data

ALL JEDEC TO-3 DIMENSIONS AND NOTES ARE APPLICABLE
THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE

DIMENSIONS ARE IN INCHES
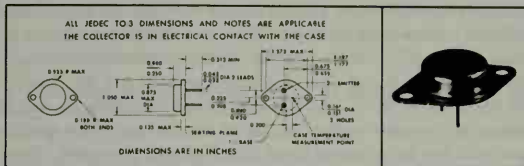
absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	70 V
Emitter-Base Voltage	7 V
Continuous Collector Current	15 A
Continuous Base Current	7 A
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	115 W
Operating Case Temperature Range . . . . −65°C to 200°C
Storage Temperature Range . . . . −65°C to 200°C
Lead Temperature $\frac{1}{16}$ Inch from Case for 10 Seconds	235°C

NOTES: 1. This value applies when the base-emitter resistance $R_{BE} = 100\ \Omega$

2. Derate linearly to 200°C case temperature at the rate of 0.66 W/deg.

'electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 200$ mA, $I_B = 0$,	See Note 6	60		V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	$I_C = 200$ mA, $R_{BE} = 100\ \Omega$		70		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 30$ V, $I_E = 0$			0.7	mA
I_{CEV}	Collector Cutoff Current	$V_{CE} = 100$ V, $V_{BE} = -1.5$ V			5	mA
		$V_{CE} = 100$ V, $V_{BE} = -1.5$ V, $T_C = 150°C$			30	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 7$ V, $I_C = 0$			5	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4$ V, $I_C = 4$ A,	See Notes 3 and 4	20	70	
		$V_{CE} = 4$ V, $I_C = 10$ A,	See Notes 3 and 4	5		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4$ V, $I_C = 4$ A,	See Notes 3 and 4		1.8	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 400$ mA, $I_C = 4$ A,	See Notes 3 and 4		1.1	V
		$I_B = 3.3$ A, $I_C = 10$ A,	See Notes 3 and 6		3	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4$ V, $I_C = 1$ A, $f = 1$ kHz		15	120	
f_{hfe}	Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = 4$ V, $I_C = 1$ A,	See Note 5	20		kHz

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	1.52	deg/W

NOTES: 3. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle $\leq 2\%$.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

5. f_{hfe} is the frequency at which the magnitude of the small-signal forward current transfer ratio is 0.707 of its low-frequency value. For this device, the reference measurement is made at 1 kHz.

Figure 8-2. Data sheet for high power transistor. (Courtesy of Texas Instruments, Inc.)

usually followed by mechanical data in the form of an illustration showing the package shape and dimensions, as well as indicating which leads are collector, base, and emitter.

The absolute maximum ratings of the transistor at a temperature of 25°C are listed next. These are the maximum voltages, currents, etc., that the device can take without breaking down. It is very important that these ratings never be exceeded; otherwise, failure of the device is quite possible. For reliability, the maximum ratings should not even be approached. Also, the maximum ratings must be adjusted downward for operation at temperatures greater than 25°C. Following the absolute maximum ratings, there is normally a complete list of electrical characteristics for the device. Again, these are specified at 25°C, and allowances are necessary for variations of temperature. A complete understanding of all the quantities specified on a data sheet will not be achieved until circuit design is studied. Some of the most important quantities are defined below. It is important to note that the ratings of a given transistor are stated for specified circuit conditions. If these conditions change, the ratings are no longer valid.

BV_{CBO}	Collector–base breakdown voltage—dc breakdown voltage for reverse-biased collector–base junction.
BV_{CEO}	Collector–emitter breakdown voltage—collector to emitter dc breakdown voltage with base open circuited.
BV_{EBO}	Emitter–base breakdown voltage—emitter to base reverse-bias dc breakdown voltage.
V_{BE}	Base–emitter voltage—dc voltage drop across forward-biased base–emitter junction.
$V_{CE(sat)}$	Collector–emitter saturation voltage—collector to emitter voltage with device in saturation.
I_{CBO} or I_{CO}	Collector cutoff current—dc collector current with collector–base junction reverse biased and emitter open circuited.
I_{CES}	Collector cutoff current—dc collector current with collector–base junction reverse biased and base short circuited to emitter.
I_{CEO}	Collector cutoff current—dc collector current with collector–base junction reverse biased and base open circuited.
I_{EBO} or I_{EO}	Emitter cutoff current—reverse-biased emitter–base dc current with collector open circuited.
h_{FE}	Static forward current transfer ratio—common emitter ratio of dc collector current and base current, $h_{FE} = I_C / I_B$.
C_{ob}	Common base output capacitance—measured between collector and base.

$\underline{C_{oe}}$ Common emitter output capacitance—measured between collector and emitter.

$\underline{NF}$ Noise figure—ratio of total noise output to total noise input expressed as a decibel (dB) ratio (Section 8-4) for a specified bandwidth and bias conditions. Defines the amount of noise added by the device.

$\underline{f_{h_{f_e}}}$ or f_{α_e} Common emitter cutoff frequency—common emitter operating frequency at which the device current gain falls to 0.707 of its normal (mid-frequency) value.

$\underline{f_{h_{f_b}}}$ or f_{α_b} Common base cutoff frequency—as above for common base.

Maximum Power Dissipation. Consider the data sheet for the 2N3903 and 2N3904 transistors, Fig. 8-1. The absolute maximum ratings at 25°C free air temperature show that the collector–emitter voltage should not exceed 40 V, and that the collector current should not exceed 200 mA. The total device dissipation of 310 mW at a maximum free air temperature of 25°C means that ($V_{CE} \times I_C$) must not exceed 310 mW. For example, if the maximum I_C of 200 mA is to be employed, then maximum V_{CE} should be $(310 \text{ mW})/(200 \text{ mA}) = 1.55$ V. It is important to note that if the free air temperature is greater than 25°C, then the device maximum power dissipation must be reduced.

8-3
Power
Dissipation

A 2N3904 transistor is employed in a circuit in which its V_{CE} will be 20 V. The circuit is to be operated at a free air temperature of 125°C. Determine the maximum value of I_C that can be used.

Example 8-1

solution

From the data sheet for the 2N3904, the 310 mW maximum power dissipation must be derated linearly at 2.81 mW/°C for temperatures greater than 25° C.

Free air temperature for circuit = 125°C.
° C in excess of 25°C = 125 − 25 = 100°C.
Device must be derated by $(2.81 \text{ mW}/° \text{ C}) \times (100°\text{C}) = 281$ mW.
Maximum device dissipation at 125°C,

$$P = 310 \text{ mW} - 281 \text{ mW} = 29 \text{ mW}$$

The device dissipation is $V_{CE} \times I_C$. Thus,

$$20 \ V \times I_{C(\max)} = 29 \text{ mW}$$

$$I_{C(\max)} = \frac{29 \text{ mW}}{20 \text{ V}} = 1.45 \text{ mA}$$

Maximum Power-Dissipation Curve. For power transistors it is sometimes necessary to draw a *maximum power-dissipation curve* on the output characteristics. To draw this curve, the greatest power that may be dissipated at the highest temperature at which the device is to be operated is first calculated. Then using convenient collector–emitter voltage levels, the corresponding collector current levels are calculated for the maximum power dissipation. Using these current and voltage levels, the curve is plotted on the device characteristics.

Example 8-2

Assuming that the device characteristics given in Fig. 8-3 are for a 2N3055 transistor, plot a maximum power-dissipation curve for a case temperature of 78°C.

solution

Case temperature for device = 78°C.

° C in excess of 25°C = 78 − 25 = 53°C.

Device must be derated by 0.66 W/° C × 53°C = 35 W.

Maximum device dissipation at 78°C = 115 W − 35 W = 80 W.

$$P_D = V_{CE} \times I_C$$
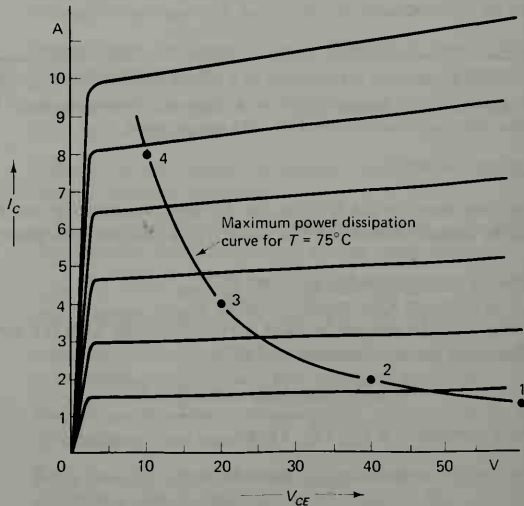
Figure 8-3. Transistor maximum power-dissipation curve.

or

$$I_C = \frac{P_D}{V_{CE}}$$

When $V_{CE} = 60$ V, $I_C = 80$ W$/60$ V $= 1.3$ A.
Plot point 1 on the characteristics at $V_{CE} = 60$ V, $I_C = 1.3$ A.

When $V_{CE} = 40$ V, $\quad I_C = \dfrac{80}{40} = 2$ A $\qquad$ Point 2

When $V_{CE} = 20$ V, $\quad I_C = \dfrac{80}{20} = 4$ A $\qquad$ Point 3

When $V_{CE} = 10$ V, $\quad I_C = \dfrac{80}{10} = 8$ A $\qquad$ Point 4

Now draw a curve through the above points to obtain the maximum power-dissipation curve. The transistor voltage and current conditions must at all times be maintained in the portion of the characteristics below the maximum power-dissipation curve.

Decibels. When the output power of an amplifier changes from P_1 to P_2, the power change is expressed as the log of their ratio:

$$\text{Power change} = \log_{10}\left(\frac{P_2}{P_1} \right) \quad \text{(bels)}$$

$$= 10 \ \log_{10}\left(\frac{P_2}{P_1} \right) \quad \text{decibels (dB)} \qquad (8\text{-}1)$$

Thus, the decibel is a unit of power *change*.
The output power dissipated in a load resistance is

$$P_o = \frac{V_o^2}{R_L}$$

$$\text{Power change} = 10 \ \log_{10}\left[\frac{V_2^2 / R_L}{V_1^2 / R_L} \right] \text{dB}$$

$$= 10 \log_{10}\left[\frac{V_2}{V_1} \right]^2 \text{dB}$$

$$= 20 \log\left[\frac{V_2}{V_1} \right] \text{dB} \qquad (8\text{-}2)$$

Also,

$$P_o = I_o^2 R_L$$

$$\text{Power change} = 10 \log_{10}\left[\frac{I_2^2 R_L}{I_1^2 R_L}\right] \text{dB}$$

$$= 20 \log_{10}\left[\frac{I_2}{I_1}\right] \text{dB} \qquad (8\text{-}3)$$

By means of Eqs. (8-2) and (8-3), power changes can be calculated in decibels using either voltage ratios or current ratios.

Example 8-3   The output power from an amplifier is 50 mW when the signal frequency is 5 kHz. When the frequency is increased to 20 kHz, the output power falls to 25 mW. Calculate the decibel change in output power.

solution

From Eq. (8-1),

$$\text{Power change} = 10 \log_{10}\left[\frac{P_2}{P_1}\right] \text{dB}$$

$$= 10 \log_{10}\left[\frac{25 \text{ mW}}{50 \text{ mW}}\right]$$

$$= 10 \log_{10}\left[0.5\right]$$

$$= -10 \log_{10}\left[2\right]$$

$$= -10(0.3) = -3 \text{ dB}$$

Example 8-4   The output voltage of an amplifier is measured as 1 V at 5 kHz and 0.707 V at 20 kHz. Calculate the decibel change in output power.

solution

From Eq. (8-2),

$$\text{Power change} = 20 \log_{10}\left[\frac{V_2}{V_1}\right] \text{dB}$$

$$= 20 \log_{10}\left[\frac{0.707}{1}\right]$$

$$= -20 \log_{10}\left[\frac{1}{0.707}\right]$$

$$= -20 \log_{10}\left[1.414\right]$$

$$= -20(0.15) = -3 \text{ dB}$$

It is seen from Examples 8-3 and 8-4 that the output power of an amplifier is reduced by 3 dB when the measured power falls to half its normal level, or when the measured voltage falls to 0.707 of its normal level.

Frequency Response. Figure 8-4 shows a typical graph of amplifier output voltage or power plotted versus frequency. It is found that the output normally remains constant over a *middle range* of frequencies and falls off at low and high frequencies, due to the effects explained below. The gain over this middle range is termed the *mid-frequency gain*. The low frequency and high frequency at which the gain falls by 3 dB are designated f_1 and f_2, respectively. This is normally considered the useful range of operating frequency for the amplifier, and the frequency difference $(f_2 - f_1)$ is termed the amplifier *bandwidth* (B).

Frequencies f_1 and f_2 are sometimes termed the *half-power* or *3-dB points*. This is because, as shown in Example 8-3, the power output is -3 dB from its normal level when P_2 is half P_1. When the amplifier output is expressed as a voltage on the graph of frequency response, the 3-dB points (f_1 and f_2) occur when V_2 is 0.707 V_1. This is shown in Example 8-4.

The fall off in amplifier gain at low frequency is due to the effect of coupling and bypass capacitors. Recall that the impedance of a capacitor is $X_c = 1/(2\pi fC)$. At medium and high frequencies, the factor f makes X_c very small, so that all coupling and bypass capacitors behave as short circuits. At low frequencies, X_c increases and some of the signal voltage is potentially divided across the capacitors [see Fig. 8-5(a)]. As the signal frequency gets lower, the capacitor impedances increase and the circuit gain continues to fall.

All transistors have capacitances between their terminals (Section 4-8). As shown in Fig. 8-5(b), there are also *stray capacitances* (C_s), which are the capacitances between connecting wires and ground. All these capacitances are very small, so that at low and medium frequencies their impedances are very high. As frequency increases, the impedance of the stray capacitances falls. When these impedances become small enough, they begin to shunt
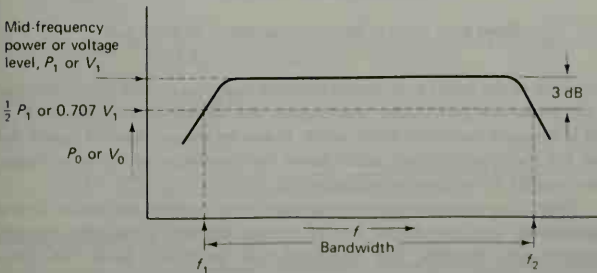
Figure 8-4. Typical amplifier frequency response.
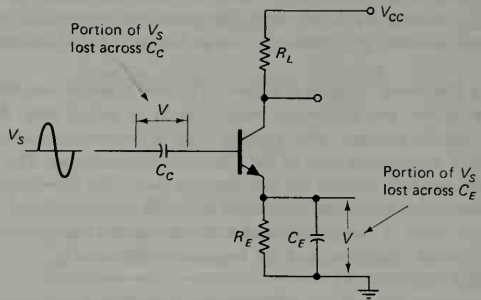
(a) Loss of signal voltage across coupling
and bypass capacitors at low frequency
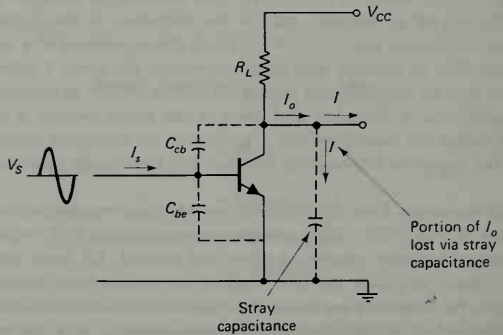
(b) Loss of output current via stray
capacitance at high frequency

Figure 8-5. Effect of stray capacitances on amplifier gain.

away some of the input and output currents and thus reduce the circuit gain. As the frequency gets higher and higher, the circuit gain continues to fall until it becomes too small to be useful. It can be shown that the upper 3-dB point for the amplifier can occur when the reactance of the stray capacitance is equal to the load resistance value.

Even if no external stray capacitances were present, the device internal capacitances, and the *transit time* of charge carriers across the transistor junctions and through the semiconductor material, limit the circuit

frequency response. This limitation is expressed as a *cutoff frequency* f_α, which is the frequency at which the transistor current gain falls to 0.707 of its gain at low and medium frequencies. The cutoff frequency can be expressed in two ways, the *common emitter cutoff frequency* (f_{α_e}) or the *common base cutoff frequency* (f_{α_b}). f_{α_e} is the frequency at which the common emitter current gain (h_{fe}) falls to $0.707 \times$ (mid-frequency h_{fe}). f_{α_b} is the frequency at which the common base current gain (h_{fb}) falls to $0.707 \times$ (mid-frequency h_{fb}). It can be shown that

$$f_{\alpha_b} \approx h_{fe} f_{\alpha_e} \tag{8-4}$$

For maximum bandwidth the stray capacitance should be kept to a minimum. Also f_α should be several times greater than the signal frequency (f_s) at which the reactance of the stray capacitance equals the amplifier load resistance.

Example 8-5

A transistor with $f_{\alpha_b} = 5$ MHz and $h_{fe} = 50$ is employed in a common emitter amplifier. The stray capacitance at the output terminal is measured as 100 pF. Determine the upper 3-dB point (a) when $R_L = 10$ kΩ and (b) when $R_L = 100$ kΩ.

solution

(a) $R_L = 10$ kΩ. From Eq. (8-4),

$$f_{\alpha_b} \approx h_{fe} f_{\alpha_e}$$
$$f_{\alpha_e} \approx \frac{f_{\alpha_b}}{h_{fe}} = \frac{5 \text{ MHz}}{50} = 100 \text{ kHz}$$

The stray capacitance reduces the amplifier gain by 3 dB when

$$\frac{1}{2\pi f_s C_s} = R_L = 10 \text{ kΩ}$$

$$f_s = \frac{1}{2\pi C_s R_L} = \frac{1}{2\pi \times 100 \times 10^{-12} \times 10 \times 10^3} = 159 \text{ kHz}$$

Since $f_{\alpha_e} < f_s, f_2 = f_{\alpha_e} = 100$ kHz.
(b) $R_L = 100$ kΩ.

$$f_s = \frac{1}{2\pi C_s R_L} = \frac{1}{2\pi \times 100 \times 10^{-12} \times 100 \times 10^3} = 15.9 \text{ kHz}$$

Since $f_s < f_{\alpha_e}, f_2 = f_s = 15.9$ kHz.

In Example 8-5 it is assumed that the transistor internal capacitances are very much smaller than the (external) stray capacitance. The internal capacitances can be very important, however, and, as will be shown, they tend to have their greatest effect at the input terminals of the transistor.

Figure 8-5(b) shows that a collector–base capacitance (C_{cb}) and a base–emitter capacitance (C_{be}) exist between the transistor terminals. Assume that an input signal ($+V_i$) is applied to the base of the transistor shown in Fig. 8-5(b). If the circuit voltage amplification is A_v, then the collector voltage change is

$$\Delta V_c = -A_v \times V_i$$

Note that because of the phase shift between input and output, the collector voltage is *reduced* by ($A_v \times V_i$) when the base voltage is *increased* by V_i. This results in a total collector–base voltage reduction of

$$\Delta V_{CB} = V_i + A_v V_i$$
$$= V_i(1 + A_v)$$

Since C_{cb} is the capacitance between collector and base, the voltage across C_{cb} is also changed by ΔV_{CB}. Using the formula $Q = C \times \Delta V$, it is found that the charge supplied to the input of the circuit is

$$Q = C_{cb} \times V_i(1 + A)$$

or

$$Q = (1 + A_v)C_{cb} \times V_i$$

Thus, the collector–base capacitance appears to be $(1 + A_v)C_{cb}$; i.e., the capacitance is *amplified* by a factor of $(1 + A_v)$. This is known as the *Miller effect*.

The total input capacitance (C_{in}) to the transistor is $(1 + A_v)C_{cb}$ in parallel with C_{be}:

$$C_{\text{in}} = C_{be} + (1 + A_v)C_{cb} \qquad (8\text{-}5)$$

At high frequencies, the value of C_{in} reduces the input impedance of the circuit and affects the frequency response.

Example 8-6

A transistor used in a common emitter circuit has $h_{fe} = 75$, $h_{ie} = 2$ kΩ, $C_{cb} = 4$ pF, and $C_{be} = 10$ pF. If the circuit load resistance is 5 kΩ, calculate the value of C_{in}.

From Eq. (6-6),

$$A_v \approx \frac{h_{fe}R_L}{h_{ie}} = \frac{75 \times 5 \text{ k}\Omega}{2 \text{ k}\Omega} \approx 188$$

From Eq. (8-5),

$$C_{in} = 10 \text{ pF} + (1 + 188)4 \text{ pF}$$
$$= 10 \text{ pF} + 756 \text{ pF} = 766 \text{ pF}$$

Unwanted signals at the output of an electronics system are termed *noise*. The noise amplitude may be large enough to swamp the wanted signals; consequently, the noise level dictates the minimum signal amplitude that can be handled. Noise originates as *atmospheric noise* from outside the system and as *circuit noise* generated within resistors and devices.

Consider a conductive material at room temperature. The motion of free electrons drifting around within the material constitutes a flow of many tiny random electric currents. These currents cause minute voltage drops, which appear across the ends (or terminals) of the material. Because the number of free electrons available and the random motion of the electrons are both increased as temperature rises, the generated voltage amplitude is proportional to temperature. This unwanted, randomly varying voltage is termed *thermal noise*.

Thermal noise is generated within resistors, and when the resistors are at the input stage of an amplifier, the noise is amplified and produced as an output. Noise from other resistors is not amplified as much as that from the resistors right at the input; consequently, only the input stage resistors need be considered in noise calculations.

Noise is also generated within a transistor, and again the input stage transistor is the most important because its noise is amplified more than that from any other stage.

Since thermal noise is an alternating quantity, its rms output level from any amplifier is dependant upon the bandwidth of the amplifier. It can be shown that the rms noise voltage generated in a resistance is

$$e_n = \sqrt{4 \, kTBR} \tag{8-6}$$

where k = Boltzmann's constant = 1.374×10^{-23} J/K

(i.e., joules per degree Kelvin)

T = absolute temperature

R = resistance in ohms

B = circuit bandwidth

**8-6
Transistor
Circuit
Noise**

Consider the circuit of Fig. 8-6(a). R_1 and R_2 are bias resistances; e_s is a signal voltage with source resistance R_s. The total noise generating resistance in parallel with the amplifier input terminal is

$$R_G = R_S \| (R_1 \| R_2)$$

In the noise equivalent circuit, Fig. 8-6(b), e_n is the noise voltage generated by R_G. It is also seen from Fig. 8-6(b) that if the amplifier input resistance is R_i then the noise voltage is potentially divided, so that

$$e_{ni} = e_n \times \frac{R_i}{R_i + R_G} \tag{8-7}$$

If the amplifier voltage gain is A_v, the output noise due to R_G is

$$e_{no} = A_v e_{ni} \tag{8-8}$$
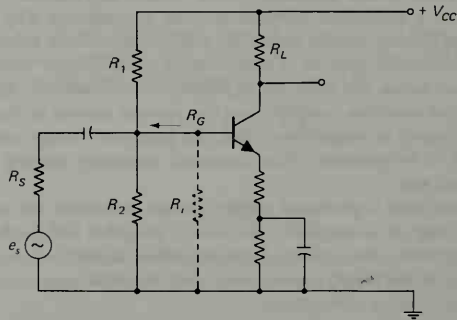
(a) Amplifier
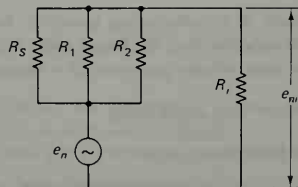
(b) ac equivalent input
circuit for noise

Figure 8-6. Amplifier and equivalent input circuit for noise.

And for a load resistance R_L, the noise output power due to R_G is

$$P_n = \frac{e_{no}^2}{R_L} \qquad (8\text{-}9)$$

To specify the amount of noise produced by a transistor, manufacturers usually quote a *noise figure* (*NF*). To arrive at this figure, the transistor noise output is measured under specified bias conditions, and with a specified source resistor, temperature, and noise bandwidth.

The noise figure defines the amount of noise added by the transistor to the noise generated by the specified resistance (R_G) at the input. Note that R_G is the combined bias and signal source resistances, as seen from the amplifier input.

The noise for a 2N4104 transistor is specified as follows:
At 25°C free air temperature

Parameter	Test Conditions	Min	Max
NF spot noise figure	$V_{CE} = 5$ V, $I_C = 30$ μA, $R_G = 10$ kΩ, $f = 10$ Hz		15 dB
	$V_{CE} = 5$ V, $I_C = 30$ μA, $R_G = 10$ kΩ, $f = 100$ Hz		4 dB
	$V_{CE} = 5$ V, $I_C = 5$ μA, $R_G = 50$ kΩ, $f = 1$ kHz		1 dB
	$V_{CE} = 5$ V, $I_C = 5$ μA, $R_G = 50$ kΩ, $f = 10$ kHz		1 dB

The fact that *NF* is defined as a *spot noise figure* means that the noise has been measured for a bandwidth of 1 Hz. The bias conditions are specified because the transistor noise can be affected by V_{CE} and I_C.

The *noise factor*, *F*, is the total circuit noise power output divided by noise output power from source resistor. The noise figure *NF* is the decibel value of *F*.

$$NF = 10 \log_{10} F \qquad (8\text{-}10)$$

If the transistor were completely noiseless,

total noise output power = noise output power due to R_G

or

$$NF = 10 \log_{10} \frac{\text{noise power from source resistor}}{\text{noise power from source resistor}} = 0 \, \text{dB}$$

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Obviously, the smallest possible noise figure is the most desirable. If the circuit in which the transistor is employed does not have the value of source resistance and the bias conditions specified, then the specified noise figure does not apply. In this case the noise figures can still be used to compare transistors, but for accurate estimations of noise a new measurement of noise figure must be made.

The total noise output power due to R_G and the input transistor is

$$P_N = (\text{noise factor} \times P_n)$$

$$= F \times \frac{e_{no}^2}{R_L} \tag{8-11}$$

Example 8-7

An amplifier with $B = 1$ to 10 kHz, $R_i = 25$ kΩ, and $R_G = 50$ kΩ uses a 2N4104 as the input transistor. The transistor bias conditions are $I_C = 5$ μA and $V_{CE} = 5$ V, and the amplifier has a voltage gain of 30. Calculate the output noise amplitude at 25°C.

solution

From the 2N4104 specification, for $V_{CE} = 5$ V, $I_C = 5$ μA, $R_G = 50$ kΩ, and $f = 1$ to 10 kHz, $NF = 1$ dB.

From Eq. (8-10), $NF = 10 \log_{10} F$:

$$\text{Noise factor } F = \text{antilog } \frac{NF}{10}$$

$$= \text{antilog } \frac{1 \text{ dB}}{10}$$

$$= 1.26$$

From Eq. (8-6),

$$e_n = \sqrt{4kTBR_G}$$

$k = 1.37 \times 10^{-23}$
$T = 25°C = (273 + 25)$ K [i.e., 298 K (degrees Kelvin)]
$B = 1$ to 10 kHz $= 9$ kHz
$R_G = 50$ kΩ

$$e_n = \sqrt{4 \times 1.37 \times 10^{-23} \times 298 \times 9 \times 10^3 \times 50 \times 10^3}$$

$$= 2.7 \text{ μV}$$

From Eq. (8-7),

$$e_{ni} = e_n \times \frac{R_i}{R_i + R_G}$$

$$= 2.7 \text{ μV} \times \frac{25 \text{ kΩ}}{25 \text{ kΩ} + 50 \text{ kΩ}}$$

$$= 0.9 \text{ μV}$$

From Eq. (8-8),

$$e_{no} = A_v \times e_{ni} = 30 \times 0.9 \ \mu V = 27 \ \mu V$$

From Eq. (8-11),

$$P_N = F \times \frac{e_{no}^2}{R_L} = 1.26 \times \frac{(27 \ \mu V)^2}{R_L}$$

and $P_N = V_n^2 / R_L$, where $V_n =$ total rms noise output voltage:

$$\frac{V_n^2}{R_L} = 1.26 \times \frac{(27 \ \mu V)^2}{R_L}$$

$$V_n = \sqrt{1.26 \times (27 \ \mu V)^2} = 30.3 \ \mu V$$

Transistor as a Switch. When a transistor is used as a switch, it is either biased off or biased on to its maximum possible collector current level. Figure 8-7 illustrates the two conditions. In Fig. 8-7(a) the base input voltage polarity is such that the transistor is biased off. In this case, the only current flowing is the *collector base leakage current* I_{CO} (sometimes designated I_{CBO}).

**8-7
Transistor
Switching**

$$V_{CE} = V_{CC} - I_C R_L$$

At cutoff

$$V_{CE} = V_{CC} - I_{CO} R_L \approx V_{CC}$$

In Fig. 8-7(b), V_B biases the transistor *on* to the maximum possible I_C level. I_C is limited only by V_{CC}, R_L, and the minimum possible voltage across the transistor.

(a) *off*-biased transistor   (b) *on*-biased transistor
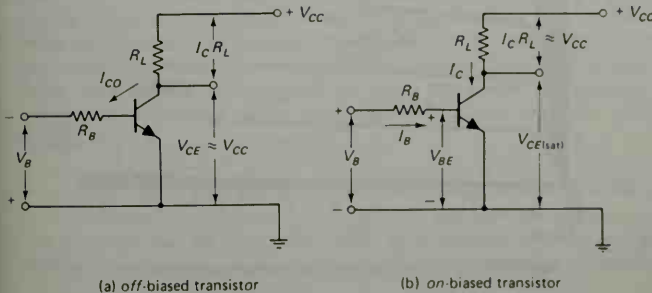
Figure 8-7. Transistor switching circuit.

$$I_C R_L \approx V_{CC}$$

and

$$V_{CE} = V_{CC} - I_C R_L$$

Therefore,

$$V_{CE} \approx 0 \text{ V}$$

Now consider the output characteristics and dc load line for the circuit of Fig. 8-7. This is shown in Fig. 8-8 and is drawn by the usual process of plotting point A at $I_C = 0$ and $V_{CE} = V_{CC}$, and point B at $V_{CE} = 0$ and $I_C = V_{CC}/R_L$. When $I_B = 0$, $I_C = I_{CO}$, and the transistor is said to be cut off. The region of the characteristics below $I_B = 0$ is termed the *cutoff region*. When I_B is a maximum, $V_{CE} = V_{CE(sat)}$, and the transistor is said to be *saturated*. The region of the characteristics to the left of $V_{CE(sat)}$ is termed the *saturation region*. The region between saturation and cutoff is the *active region* in which a transistor is biased for amplification. $V_{CE(sat)}$ is the minimum possible collector–emitter voltage for the device, and is referred to as the transistor *saturation voltage*. It is seen that $V_{CE(sat)}$ is dependent upon the I_C level. For the 2-kΩ load line shown as the broken line in Fig. 8-8, $V_{CE(sat)}$ is smaller than for $R_L = 1$ kΩ.
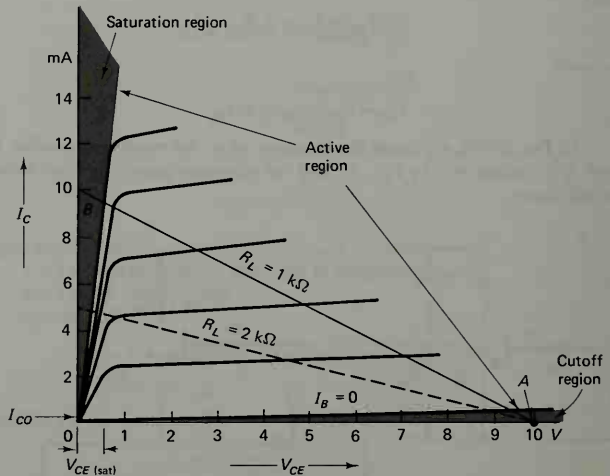
Figure 8-8. Characteristics and load line for transistor switch.

and $R_L = 1$ kΩ. Determine the value of V_{CE} when the transistor is (a) cut off
and (b) saturated.

solution

(a) *At cut-off* $I_C = I_{CO}$. From the *Off Characteristics* section of the 2N3904 data
sheet in Fig. 8-1, the collector cutoff current is $I_{CO} = I_{CEX} = 50$ nA maximum.
(*Note that I_{CEX} is the collector cutoff current for a specified bias and supply voltage.*)

$$V_{CE} = V_{CC} - I_{CO}R_L$$
$$= 10 \text{ V} - (50 \text{ nA} \times 1 \text{ kΩ})$$
$$= 10 \text{ V} - 50 \text{ μV} = 9.99995 \text{ V}$$

(b) *At saturation*

$$V_{CE} \approx 0$$
$$0 \approx V_{CC} - I_C R_L$$

and

$$I_C \approx \frac{V_{CC}}{R_L} \approx \frac{10 \text{ V}}{1 \text{ kΩ}} = 10 \text{ mA}$$

From the 2N3904 data sheet $V_{CE(\text{sat})} = 0.2$ V max at $I_C = 10$ mA.

$$V_{CE} \leqslant 0.2 \text{ V}$$

$V_{CE(\text{sat})}$ is typically around 0.2 V for a silicon transistor, while V_{BE} is
typically 0.7 V. Consider the circuit in Fig. 8-7(b) once again. If $V_{BE} = 0.7$ V
and $V_{CE} = 0.2$ V, then the transistor base is 0.5 V more positive than the
collector. This means that the collector–base junction, which is usually
reverse biased, is in fact forward biased when the transistor is in saturation.
With the collector–base junction forward biased, fewer charge carriers from
the emitter are drawn across to the collector, and the device current gain is
lower than normal. For saturation to occur, the transistor must have a
certain minimum value of h_{FE}, which depends upon the particular circuit
conditions.

the minimum h_{FE} for saturation. (b) If V_B is changed to 1 V, and the
transistor minimum h_{FE} is specified as 50, will the transistor be saturated?

solution (a)

I_C has already been calculated as 10 mA.

The voltage across R_B is $(V_B - V_{BE})$:

$$I_B = \frac{V_B - V_{BE}}{R_B} = \frac{2 \text{ V} - 0.7 \text{ V}}{2.7 \text{ k}\Omega} = 0.481 \text{ mA}$$

$$h_{FE} = \frac{I_C}{I_B} = \frac{10 \text{ mA}}{0.482 \text{ mA}} = 20.8$$

Thus, $h_{FE(\text{min})}$ for the transistor must be at least 20.8 for saturation to occur.

solution (b)

$$I_B = \frac{V_B - V_{BE}}{R_B} = \frac{1 - 0.7}{2.7 \text{ k}\Omega} = 0.111 \text{ mA}$$

$$I_C = h_{FE} \, I_B = 50 \times 0.111 \text{ mA} = 5.55 \text{ mA}$$

Since I_C is required to be 10 mA for saturation, the device will *not* be saturated.

Switching Speed. Another important characteristic of a switching transistor is its operating speed. Consider Fig. 8-9. When the base input current is applied, the transistor does not switch on immediately. This is because of the junction capacitance and the transit time of electrons across the junctions. The time between the application of the input pulse and the commencement of collector current flow is termed the *delay time* (t_d) (Fig. 8-9). Even when the transistor begins to switch on, a finite time elapses before I_C reaches its maximum level. This quantity is known as the *rise time* (t_r). The rise time is specified as the time required for I_C to go from 10% to 90% of its maximum level. The *turn-on time* (t_{on}) is the sum of t_r and t_d. (See Fig. 8-9.) Similarly, when the input pulse is removed, I_C does not go to zero until after a *turn-off time* (t_{off}), made up of a *storage time* (t_s) and a *fall time* (t_f).

The fall time is specified as the time required for I_C to go from 90% to 10% of its maximum level. The storage time is the result of charge carriers being trapped in the depletion region when a junction polarity is reversed. When a transistor is in saturation, both the collector–base and emitter–base junctions are forward biased. At switchoff, both junctions are reverse biased, and before I_C begins to fall the stored charge carriers must be withdrawn or made to recombine with opposite-type charge carriers. For a fast-switching transistor, t_{on} and t_{off} must be of the order of nanoseconds.

Glossary of Important Terms

Decibel (dB). Unit of power change: power change $= 10 \log(P_1/P_2)$ dB.

Half-power points (f_1 and f_2). Low and high frequencies at which an amplifier output power is half its mid-frequency output power. Also,
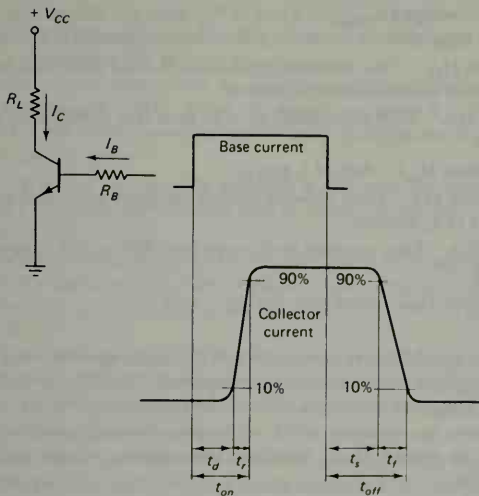
Figure 8-9. Transistor switching times.

the frequencies at which an amplifier output voltage is 0.707 of its mid-frequency output voltage.

Bandwidth (B). Difference between half-power points. $B = (f_2 - f_1)$.

Common emitter cutoff frequency ($f_{h_{fe}}$ or f_{α_e}). The high frequency at which a transistor h_{fe} falls to $0.707 \times$ (mid-frequency h_{fe}).

Common base cutoff frequency ($f_{h_{fb}}$ or f_{α_b}). The high frequency at which a transistor h_{fb} falls to $0.707 \times$ (mid-frequency h_{fb}).

Miller effect. Amplification of device input capacitance.

Noise. Unwanted signals at the output of an electronic system.

Thermal noise. Temperature-dependent noise generated within resistances and semiconductor bulk material.

Noise factor (F). (Total noise output power)/(noise output power from source resistance).

Noise figure (NF). Decibel value of noise factor.

Cutoff region. Region of transistor common emitter characteristics below $I_B = 0$.

Saturation region. Region of transistor common emitter characteristics between $V_{CE} = V_{CE(\text{sat})}$ and $V_{CE} = 0$.

Active region. Region of transistor characteristics between saturation and cutoff.

Saturation voltage ($V_{CE(\text{sat})}$). Level of V_{CE} when the voltage drop across R_L is so large that the transistor collector–base junction is forward biased.

Delay time (t_d). Time between application of input pulse and commencement of transistor collector current.

Rise time (t_r). Time required for I_C to go from 10% to 90% of its maximum level.

Turn-on time (t_{on}). Sum of t_r and t_d.

Storage time (t_s). Time between removal of input pulse and commencement of I_C decrease.

Fall time (t_f). Time required for I_C to go from 90% to 10% of its maximum level.

Turn-off time (t_{off}). Sum of t_s and t_f.

Review Questions

8-1. List and define the most important quantities specified on a transistor data sheet for (a) small-signal transistors, (b) high-power transistors, (c) switching transistors, (d) high-frequency transistors.

8-2. Derive the equations which are employed to calculate power change at the output of an amplifier, using power, voltage, and current ratios.

8-3. Explain why the output power of an amplifier falls at low and high frequencies. Sketch the typical graph of amplifier frequency response, and identify the important points on the graph.

8-4. Discuss *Miller effect* and derive an equation for amplifier input capacitance.

8-5. Explain *thermal noise*, and discuss the various sources of noise which occur within a transistor circuit. Identify the most important noise sources, and explain why they are important. Define *noise figure* and *noise factor* for a transistor.

8-6. Sketch typical output characteristics and dc load line for a transistor used as a switch. Identify the various regions of the characteristics, and briefly explain. Explain the importance of I_{CO} and $V_{CE(\text{sat})}$.

8-7. Sketch the waveforms of input and output currents for a switching transistor. Show the various switching times involved and explain the origin of each.

Problems

8-1.(a) A 2N3904 transistor is required to dissipate 200 mW of power. Calculate the maximum free air temperature at which it can operate.

  (b) If the device is to be operated at a maximum free air temperature of 80°C and is to have a collector current of 2 mA, determine the minimum level of V_{CE} that may be employed.

8-2.(a) A 2N3055 transistor is to be operated at a maximum case temperature of 125°C. Using the output characteristics in Fig. 8-2, draw the maximum power dissipation curve for the device at this temperature.

(b) For the $T = 78°C$ curve shown on Fig. 8-3, draw the dc load line for the smallest possible value of R_L when the circuit supply voltage is 50 V. Determine the value of $R_{L(min)}$.

8-3. The output power from an amplifier is 100 mW when the signal frequency is 1 kHz. When the signal frequency is increased to 25 kHz, the output power falls to 75 mW. Calculate the decibel change in output power.

8-4. The output voltage of an amplifier is 2 V when the signal frequency is 1 kHz. Calculate the new level of output voltage when it has fallen by 4 dB.

8-5. A transistor employed in an amplifier has $h_{fe} = 75$ and $f_{\alpha_e} = 12$ MHz. Stray capacitance at the amplifier output terminal is 100 pF. Determine the upper 3-dB point (a) when $R_L = 5$ kΩ, (b) when $R_L = 20$ kΩ.

8-6. The transistor referred to in Problem 8-5 is connected as an amplifier with $R_L = 15$ kΩ. The upper 3-dB frequency of the amplifier is found to be $f_2 = 75$ kHz. Calculate the value of stray capacitance at the transistor collector terminal.

8-7. The input capacitance of a common emitter circuit is measured as 800 pF. The load resistance of the circuit is 7 kΩ, and the transistor parameters are $h_{fe} = 60$, $h_{ie} = 1.5$ kΩ. If the base–emitter capacitance is 15 pF, calculate the value of collector–base capacitance.

8-8. A transistor with $h_{fe} = 100$, $h_{ie} = 2.2$ kΩ, $C_{cb} = 3$ pF, and $C_{be} = 8$ pF is connected as an amplifier with $R_L = 6.8$ kΩ. Calculate the value of the amplifier input capacitance C_{in}. Also calculate the new value of C_{in} when a 100-pF capacitor is connected (a) between emitter and base, (b) between collector and base, (c) between collector and emitter.

8-9. An amplifier which uses a 2N4104 transistor at the input has lower and upper 3-dB points at 2 kHz and 10 kHz, respectively. The transistor bias conditions are $V_{CE} = 5$ V and $I_C = 5$ μA, and the amplifier voltage gain is 40. Calculate the noise output voltage at 25°C if $R_G = 50$ kΩ and $R_i = 10$ kΩ.

8-10. A transistor amplifier with $A_v = 100$, $B = 15\text{kH}_Z$ and $R_i = 12\text{k}\Omega$ has input bias resistors equivalent to $R_G = 33$ kΩ. If the maximum noise voltage at the output is not to exceed 100 μV rms, determine the largest noise figure for the input transistor.

8-11. A 2N3904 transistor employed as a switch has $V_{CC} = 25$ V and $R_L = 2.7$ kΩ. Calculate the value of V_{CE} when the transistor is (a) cut off, (b) saturated.

8-12. A transistor switching circuit arranged as in Fig. 8-7 has $R_L = 2.7$ kΩ, $V_{CC} = 25$ V, $R_B = 4.7$ kΩ, $V_B = 1.6$ V, and $V_{BE} = 0.3$ V. (a) Calculate the minimum transistor h_{FE} for saturation. (b) If R_L is changed to 1 kΩ and h_{FE} is specified as 40 minimum, will the transistor be saturated?

Basic Multistage and Integrated Circuit Amplifiers

An amplifier may be classified according to the function it performs, the frequency range over which it operates, the coupling method between stages, or how the output transistors are biased.

A *small-signal amplifier*, also known as a *preamplifier*, performs the function of amplifying small voltage signals. A *power amplifier*, or *large signal amplifier*, accepts relatively large input voltages, and drives an output current through a low-impedance load. *Audio frequency*, *intermediate frequency*, *high frequency*, *radio frequency*, and *video* are prefixes employed to identify amplifiers designed for a particular frequency range.

A *dc amplifier* can amplify dc or steady-state input voltages. Most integrated circuit amplifiers are dc amplifiers; they also generally have *differential amplifier* input stages. The differential amplifier has two input terminals and does not employ any bypass capacitors.

Many IC amplifiers are known as *operational amplifiers*. This means that they have very high internal gain, high input impedance, low output impedance, two input terminals, and one output terminal.

Amplifiers may be described as *direct coupled*, *capacitor coupled*, or *transformer coupled*, indicating the interstage coupling method.

Audio power amplifiers are classified as class A (output transistors biased to give $V_{CE} \approx \frac{1}{2} V_{CC}$), class B, (output transistors biased at cutoff), and class AB, (output transistors partially biased *on*). Circuit efficiency and lack of output distortion are prime considerations with audio power amplifiers.

In Section 6-8 a capacitor-coupled two-stage amplifier is ac analyzed to determine the circuit gains and impedances. Each stage of that circuit is a simple fixed-current bias common-emitter arrangement. Figure 9-1 shows two capacitor-coupled emitter-current biased stages. This circuit functions in the same way as the circuit in Fig. 6-15; an ac input signal is amplified by the first stage, and then further amplified by the second stage. The procedure for ac analysis of the circuit is similar to that in example 6-6.

Design Approach. When designing any amplifier, it is necessary to work to a specification which might state supply voltage, amplifier gain, frequency response, signal source impedance, and load impedance.

Obviously, each stage of the amplifier must be designed to operate satisfactorily from the available supply voltage. Designing for a particular value of voltage gain normally requires the use of *negative feedback* to stabilize the gain. The use of an unbypassed emitter resistor, as discussed in Section 6-3, is one method of providing negative feedback. Equation (6-7) shows that, in this case, the stage gain is stabilized at $A_v \approx (-R_L)/R_E$. The circuit in Fig. 9-1 has no provision for negative feedback; thus, it is designed to achieve the largest possible voltage gain.
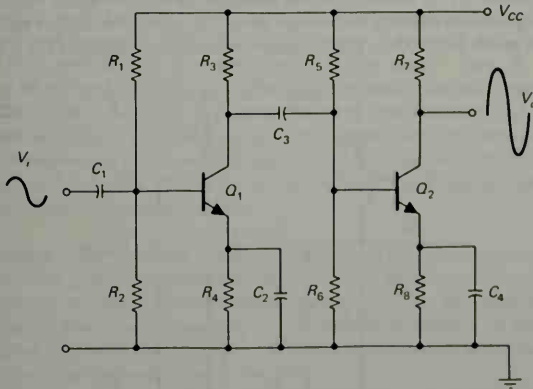
Figure 9-1. Two-stage capacitor-coupled amplifier.

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The simplest approach to the design of a two-stage amplifier (such as in Fig. 9-1) is to make each stage identical. Then, when stage 2 has been designed, the stage 1 components are selected as $R_1 = R_5$, $R_2 = R_6$, $R_3 = R_7$, $R_4 = R_8$, $C_2 = C_4$, and $C_1 = C_3$.

R_L and R_E Selection. From Eq. (6-6), the voltage gain of each stage is

$$A_v = \frac{-h_{fe}R_L}{h_{ie}}$$

Since $A_v \propto R_L$, designing for the largest voltage gain normally requires the selection of the largest possible values of R_L (i.e., R_3 and R_7 in Fig. 9-1).

The collector current for each transistor might be selected to give the greatest h_{fe} value, again to achieve greatest A_v. However, a large collector current results in a small value of R_L (for a given value of V_{RL}), and so a large value of I_C may actually give a lower voltage gain, even though h_{fe} may be relatively large.

For a given level of I_C, the largest possible voltage drop V_{RL} (in Fig. 9-2) gives the greatest value of collector load resistor:

$$R_L = \frac{V_{RL}}{I_C}$$

Therefore, to make V_{RL} large, V_E and V_{CE} should be held to a minimum. The collector–emitter voltage should typically be at least 3 V to ensure that the device is operating in its active region. This allows a maximum output swing of about ± 1 V, which is usually adequate for a small-signal amplifier.

For good bias stability the voltage drop (V_E) across the emitter resistors should be much larger than the transistor base–emitter voltage (V_{BE}). That
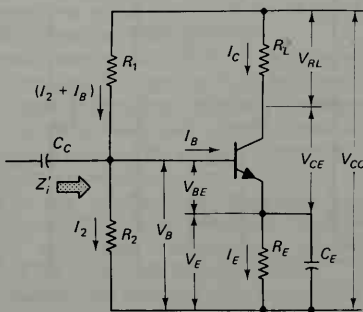
Figure 9-2. Currents and voltages in common emitter circuit.

is,

$$V_E \gg V_{BE}$$

This is because $V_E = V_B - V_{BE}$ (see Fig. 9-2), and when $V_E \gg V_{BE}$, any variation in V_{BE} (due to temperature change or other effects) has only a slight effect upon V_E. Thus, the emitter current and collector current remain fairly stable at

$$I_C \approx I_E = \frac{V_E}{R_E}$$

Once V_E and V_{CE} are decided, V_{RL} can be determined:

$$V_{RL} = V_{CC} - V_{CE} - V_E$$

Then R_L and R_E are calculated:

$$R_L = \frac{V_{RL}}{I_C} \quad \text{and} \quad R_E \approx \frac{V_E}{I_C}$$

Bias Resistors. In Section 5-5 it is explained that the potential divider resistors (R_1 and R_2 in Fig. 9-2) should be made as small as possible for good bias stability. The rule-of-thumb suggested there was to let the potential divider current (I_2 in Fig. 9-2) be equal to the transistor collector current. However, in the circuit in Fig. 9-1, the second-stage bias resistors R_5 and R_6 also affect the input impedance of stage 2 and constitute a load capacitor coupled to stage 1. This reduces the total load resistance at the collector of stage 1, and because $A_v \propto R_L$, the gain of stage 1 is reduced.

It is seen that, to give the largest possible stage 1 gain, R_5 and R_6 should be selected as large as possible. The two conflicting requirements are (1) bias resistors as small as possible for good bias stability, and (2) bias resistors as large as possible for high input impedance and good first-stage gain. A reasonable compromise is achieved by selecting the potential divider current as $I_2 \approx I_C/10$. This keeps $I_2 \gg I_B$ while also resulting in fairly large values of potential divider resistors.

Capacitors. The coupling and bypass capacitors should be chosen to have the smallest possible capacitance value. This is both for economy (large capacitance values are more expensive) and to minimize the physical size of the circuit. Since each capacitor has its highest impedance at the lowest operating frequency, the capacitor values are calculated at the lowest signal frequency that the circuit has to amplify.

The circuit low 3-dB frequency (f_1) is determined by the bypass capacitors (C_2 and C_4 in Fig. 9-1). Using Eqs. (6-6) and (6-7), it can be shown that the low 3-dB frequency for each stage occurs when the bypass

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capacitor has a value of

$$X_c = h_{ib}$$

or

$$X_c = \frac{h_{ie}}{1 + h_{fe}}$$

Substituting

$$X_c = 1(2\pi f C),$$

$$C_E = \frac{1 + h_{fe}}{2\pi f_1 h_{ie}} \tag{9-1}$$

When Eq. (9-1) is employed to calculate C_2 and C_4 in Fig. 9-1, it is found that at f_1 *each stage gain* is 3 dB below its mid-frequency gain. This means that at f_1 the overall amplifier gain is 6 dB below its mid-frequency value. For a 3-dB reduction in overall gain at f_1, the bypass capacitors must be calculated to give a 1.5-dB reduction in each stage gain. The equation for the bypass capacitors now becomes

$$C_E = \frac{1 + h_{fe}}{2\pi(0.65f_1)h_{ie}} \tag{9-2}$$

The coupling capacitors should have very little effect on the overall amplifier gain at the lowest signal frequency. To achieve this, the impedance of each coupling capacitor is made equal to one tenth of the load impedance in series with it:

$$X_c = \frac{Z_i'}{10}$$

or

$$\frac{1}{2\pi f_1 C} = \frac{Z_i'}{10}$$

giving

$$C_c = \frac{10}{2\pi f_1 Z_1'} \tag{9-3}$$

Example 9-1   Design a two-stage, capacitor-coupled, small-signal amplifier (as in Fig. 9-1) to meet the following specification. Supply voltage $V_{CC} = 18$ V, lowest operating frequency $f_1 = 100$ Hz, and voltage gain A_v is as large as possible. Use 2N3904 transistors (data sheet in Fig. 8-1), and make $I_C = 1$ mA.

solution

Design stage 2 first and refer to the components as numbered in Fig. 9-1.

For good bias stability,

$$V_{R8} \gg (V_{BE} = 0.7 \text{ V})$$

Take $V_{R8} = 5$ V.

For maximum V_{RL}, let $V_{CE} = 3$ V:

$$V_{R7} = 18 \text{ V} - 5 \text{ V} - 3 \text{ V}$$

$$= 10 \text{ V}$$

$$R_7 = \frac{V_{R7}}{I_C} = \frac{10 \text{ V}}{1 \text{ mA}}$$

$$= 10 \text{ k}\Omega \qquad \text{(this is a standard resistor value;}$$
$$\text{see Appendix 1)}$$

$$R_8 \approx \frac{V_{R8}}{I_C} = \frac{5 \text{ V}}{1 \text{ mA}}$$

$$= 5 \text{ k}\Omega \quad \text{(use a 4.7-k}\Omega \text{ standard value)}$$

V_{R8} now becomes

$$I_C \times R_8 = 1 \text{ mA} \times 4.7 \text{ k}\Omega = 4.7 \text{ V}$$

and

$$V_B = V_{BE} + V_{R8} = 0.7 \text{ V} + 4.7 \text{ V} = 5.4 \text{ V}$$

Let

$$I_6 = \frac{I_C}{10} = \frac{1 \text{ mA}}{10} = 100 \ \mu\text{A}$$

$$R_6 = \frac{V_B}{I_C} = \frac{5.4 \text{ V}}{100 \ \mu\text{A}}$$

$$= 54 \text{ k}\Omega \quad \text{(use a 47-k}\Omega \text{ standard value)}$$

I_6 now becomes

$$\frac{V_B}{R_6} = \frac{5.4 \text{ V}}{47 \text{ k}\Omega} = 115 \ \mu\text{A}$$

Referring to the 2N3904 data sheet in Fig. 8-1:
At $I_C = 1$ mA, $h_{FE(min)} = 70$ and

$$I_{B(max)} = \frac{I_C}{h_{FE(min)}}$$

$$= \frac{1 \text{ mA}}{70} \approx 14 \ \mu\text{A}$$

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$V_{R5} = V_{CC} - V_{R6} = 18\text{ V} - 5.4\text{ V} = 12.6\text{ V}$

and

$$R_5 = \frac{V_{R5}}{I_6 + I_B} = \frac{12.6\text{ V}}{115\ \mu\text{A} + 14\ \mu\text{A}}$$

$$\approx 98\text{ k}\Omega \quad (\text{use } 100\text{ k}\Omega, \text{ the next higher standard value})$$

From Eq. (9-2),

$$C_4 = \frac{1 + h_{fe}}{2\pi(0.65 f_1)h_{ie}}$$

From the 2N3904 data sheet,

$$h_{fe} = 100 \quad \text{and} \quad h_{ie} = 1\text{ k}\Omega$$

$$C_4 = \frac{1 + 100}{2\pi(0.65 \times 100\text{ Hz})1\text{ k}\Omega}$$

$$= 247\ \mu\text{F} \quad (\text{use } 250\text{-}\mu\text{F standard value; see Appendix 2})$$

$$Z_i' = R_5 \| R_6 \| h_{ie} = 100\text{ k}\Omega \| 56\text{ k}\Omega \| 1\text{ k}\Omega = 973\ \Omega$$

From Eq. (9-3),

$$C_3 = \frac{10}{2\pi f_1 \times Z_i'}$$

$$= \frac{10}{2\pi \times 100\text{ Hz} \times 973\ \Omega}$$

$$= 16\ \mu\text{F} \quad (\text{use } 18\text{-}\mu\text{F standard value})$$

For the first stage, $R_1 = R_5 = 100$ kΩ, $R_2 = R_6 = 56$ kΩ, $R_3 = R_7 = 6.8$ kΩ, $R_4 = R_8 = 4.7$ kΩ, $C_2 = C_4 = 250\ \mu$F, and $C_1 = C_3 = 18\ \mu$F.

9-3
Direct-
Coupled
Two-Stage
Circuit

The two-stage amplifier shown in Fig. 9-3 is known as a *dc feedback pair*. The base of Q_2 is directly connected to the collector of Q_1, and Q_1 is biased via R_3 to the emitter of Q_2. Comparing this circuit to the capacitor-coupled two-stage amplifier in Fig. 9-1 shows a considerable savings in components. The bias resistors (R_1, R_2, R_5, and R_6) in Fig. 9-1 are eliminated in Fig. 9-3, and only a single resistor (R_2) is employed in biasing. As well, the emitter resistor and bypass capacitor are eliminated from the first stage, as is the coupling capacitor between stages.
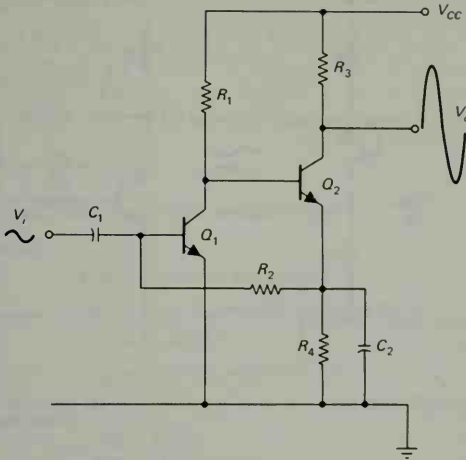
Figure 9-3. DC feedback pair.

The redrawn circuit in Fig. 9-4 shows that Q_1 is biased from its own collector, via transistor Q_2, which behaves as an emitter follower (as far as the biasing of Q_1 is concerned). The biasing arrangement for Q_1 is, in fact, a variation of the collector-to-base bias circuit discussed in Section 5-4. Q_2 is emitter current biased, with emitter resistor R_4 stabilizing the emitter current. Q_2 base voltage is derived from Q_1 collector; consequently, Q_2 bias stability is only as good as Q_1 stability.

Because collector-to-base bias is not as stable as emitter-current bias, the bias conditions in this circuit (when h_{FE} and/or temperature varies) will not remain as constant as those in the circuit of Fig. 9-1. However, the stability is adequate for many purposes, and the saving in components (and space) is frequently a major advantage.

The circuit derives its name (DC feedback pair) from the fact that the first and second stage are direct coupled (DC), and also because there is voltage feedback from the collector of Q_1 to its base. As explained in Section 5-4, when the level of I_{C1} is larger than intended, the (increased) voltage drop across R_1 results in a lower than intended collector voltage V_{C1}. This, in turn, reduces the voltage drop across bias resistor R_2, and consequently cuts down on the level of base current to Q_1. Since $I_C \approx h_{FE} I_B$, the lower base current reduces the collector current level. Thus, there is feedback, which tends to stabilize I_C.

The negative feedback results in ac degeneration (see Section 5-8) if its effect on the (ac) signal is not eliminated. Capacitor C_2 shorts the ac

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(a) DC feedback pair

(b) Collector-
to-base bias
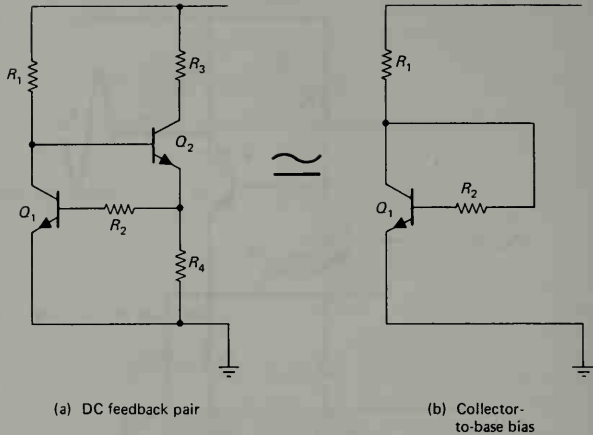
Figure 9-4. The bias circuit for Q_1 in a DC feedback pair is similar to a collector-to-base bias circuit.

feedback to ground and eliminates ac degeneration on stage 1. C_2 also eliminates the ac degeneration on stage 2 by making R_4 look like an ac short circuit to ground (again see Section 5-8).

The design approach to the dc feedback pair is fairly similar to that taken in designing the two-stage capacitor-coupled amplifier. Only one capacitor (C_2) determines the low-frequency cutoff point for the circuit. Equation (9-1) applies. The input impedance is $R_2 \| h_{ie1}$, and C_1 is calculated to have an impedance equal to one tenth of this value at frequency f_1, using Equation (9-3).

Example 9-2   Design a DC feedback pair (as in Fig. 9-3) to operate from a supply of $V_{CC} = 12$ V. Take $I_C = 2$ mA, and assume that the transistors have $h_{FE} = 100$, $h_{fe} = 100$, and $h_{ie} = 2$ kΩ. The low 3-dB frequency for the circuit is to be $f_1 = 150$ Hz.

solution

As in Example 9-1, make V_{R1} and V_{R4} as large as possible for good gain. Take $V_{CE(min)} = 3$ V.

For $V_E \gg V_{BE}$, let $V_{R4} \approx 5$ V.

$$V_{R3} = V_{CC} - V_{CE} - V_{R4} = 12 \text{ V} - 3 \text{ V} - 5 \text{ V} = 4 \text{ V}$$

$$R_3 = \frac{V_{R3}}{I_C} = \frac{4 \text{ V}}{2 \text{ mA}}$$

$$= 2 \text{ k}\Omega \quad (\text{use } 1.8\text{-k}\Omega \text{ standard value; see Appendix 1})$$

$$R_4 \approx \frac{V_{R4}}{I_C} = \frac{5 \text{ V}}{2 \text{ mA}}$$

$$= 2.5 \text{ k}\Omega \quad (\text{use } 2.2\text{-k}\Omega \text{ standard value})$$

V_{R4} now becomes

$$I_C R_4 = 2 \text{ mA} \times 2.2 \text{ k}\Omega = 4.4 \text{ V}$$

$$V_{B2} = V_{R4} + V_{BE} = 4.4 + 0.7 \text{ V} = 5.1 \text{ V}$$

$$V_{C1} = V_{B2} = 5.1 \text{ V}$$

$$V_{R1} = V_{CC} - V_{C1} = 12 \text{ V} - 5.1 \text{ V}$$

$$= 6.9 \text{ V}$$

$$I_{B2} = \frac{I_{C2}}{h_{FE}} = \frac{2 \text{ mA}}{100}$$

$$= 20 \text{ }\mu\text{A}$$

$$I_{R1} = I_{C1} + I_{B2} = 2 \text{ mA} + 20 \text{ }\mu\text{A}$$

$$= 2.02 \text{ mA}$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{6.9 \text{ V}}{2.02 \text{ mA}}$$

$$= 3.4 \text{ k}\Omega \quad (\text{use } 3.3\text{-k}\Omega \text{ standard value})$$

$$V_{R2} = V_{R4} - V_{BE1} = 4.4 \text{ V} - 0.7 \text{ V}$$

$$= 3.7 \text{ V}$$

$$I_{B1} = \frac{I_{C1}}{h_{FE}} = \frac{2 \text{ mA}}{100}$$

$$= 20 \text{ }\mu\text{A}$$

$$R_2 = \frac{V_{R2}}{I_{B1}} = \frac{3.7 \text{ V}}{20 \text{ }\mu\text{A}}$$

$$= 185 \text{ k}\Omega \quad (\text{use } 180\text{-k}\Omega \text{ standard value})$$

From Eq. (9-1),

$$C_2 = \frac{1 + h_{fe}}{2\pi f_1 h_{ie}} = \frac{1 + 100}{2\pi \times 150 \text{ Hz} \times 2 \text{ k}\Omega}$$

$$= 54 \text{ }\mu\text{F} \quad (\text{use } 56\text{-}\mu\text{F standard value; see}$$

$$\text{Appendix 2})$$

$$Z_{in} = h_{ie1} \| R_2 = 2 \text{ k}\Omega \| 180 \text{ k}\Omega = 1.98 \text{ k}\Omega$$

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From Eq. (9-3),

$$C_1 = \frac{10}{2\pi f_1 Z_{in}} = \frac{10}{2\pi \times 150 \text{ Hz} \times 1.98 \text{ k}\Omega}$$

$$= 5.4 \ \mu\text{F} \quad (\text{use } 5.6\text{-}\mu\text{F standard value})$$

9-4
The Differential Amplifier

9-4.1
Basic Circuit

The differential amplifier is widely applied in integrated circuitry because it has both good bias stability and good gain without requiring large bypass capacitors.

Figure 9-5 shows the basic differential amplifier circuit. If transistors Q_1 and Q_2 are assumed to be identical in all respects and have equal base voltages, then

$$I_{E1} = I_{E2}$$

The total emitter current

$$I_E = I_{E1} + I_{E2}$$

and

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

I_E remains virtually constant no matter what the h_{FE} value of the transistors.
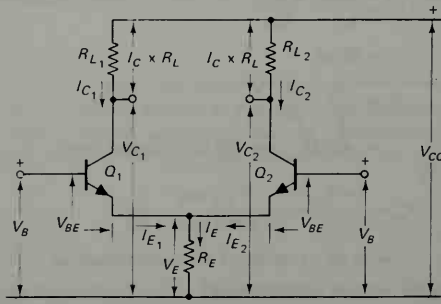
Figure 9-5. Basic differential amplifier.

Since $I_{C1} \approx I_{E1}$, and $I_{C2} \approx I_{E2}$, the collector currents also remain constant, and $I_{C1} \approx I_{C2}$.

In addition, $V_{C1} = V_{C2} = (V_{CC} - I_C R_L)$, assuming $R_{L1} = R_{L2}$.

Since I_E is independent of transistor h_{FE} variations, I_C and V_C are also substantially independent of h_{FE}, and it is seen that *the differential amplifier has excellent bias stability*.

Recall from Eq. (6-7) that the voltage gain of the single-stage common emitter amplifier in Fig. 9-6(a) is

$$A_V = \frac{-h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_E}$$

where R_E is an external resistance in series with the transistor emitter terminal.

Looking from Q_1 emitter toward Q_2 in Fig. 9-6(b), the resistance "seen" is the Z_i to a CB circuit; i.e., $R = h_{ib_2}$. Therefore, for a signal applied at the base of Q_1, Q_2 may be replaced with h_{ib_2} to give the single-stage equivalent circuit of Fig. 9-6(c). Now applying the equation for single-stage gain, and neglecting R_E since it is typically much larger than h_{ib_2}, the gain of the circuit in Fig. 9-6(c) is

$$A_V = \frac{-h_{fe} R_L}{h_{ie_1} + (1 + h_{fe_1}) h_{ib_2}}$$

It can be shown that

$$h_{ib_2} = \frac{h_{ie_2}}{1 + h_{fe_2}}$$

Therefore,

$$A_V = \frac{-h_{fe} R_L}{h_{ie_1} + (1 + h_{fe_1}) h_{ie_2} / (1 + h_{fe_2})}$$

If the transistors are matched, as is usually the case in differential amplifiers, then $h_{fe_1} = h_{fe_2}$ and $h_{ie_1} = h_{ie_2}$ and

$$A_V = \frac{-h_{fe} R_L}{2 h_{ie}} \tag{9-4}$$

This is the voltage gain from one input to one output of a differential amplifier. It is also half the gain available from a similar single transistor stage with R_E bypassed; but note that *for the differential amplifier no bypass capacitor is required*.

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$$A_V = \frac{-h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_E}$$

(a) Showing voltage
gain of single stage
CE amplifier

(b) Showing that the resistance "seen"
looking into Q_{2e} is h_{ib_2}

$$A_V = \frac{-h_{fe} R_L}{h_{ie_1} + (1 + h_{fe_1}) h_{ib_2}}$$

(c) Single-stage representation
of one side of differential
amplifier
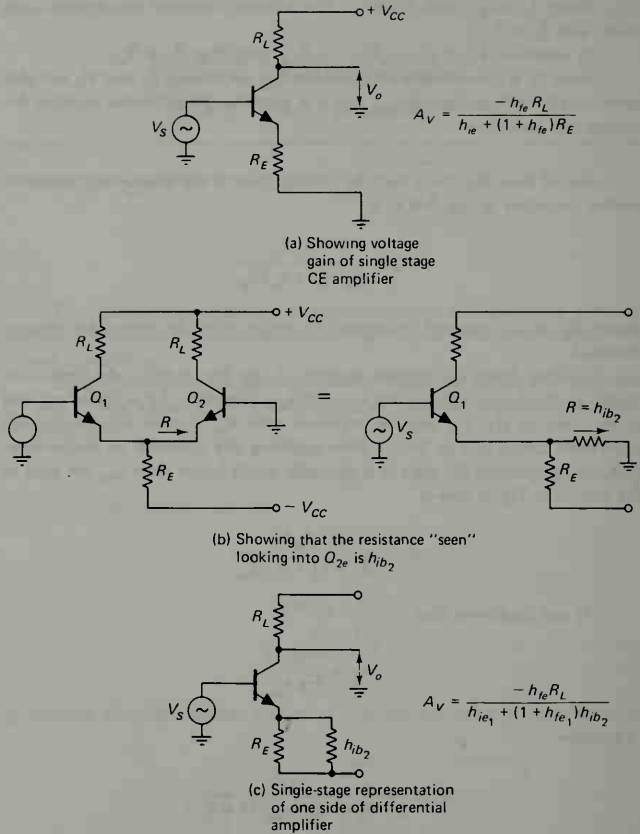
Figure 9-6. Comparing the voltage gain of a differential amplifier to a single-stage common emitter amplifier.

Another way to consider the voltage gain of this circuit is to think of the signal voltage (V_S) being equally divided across h_{ie_1} and h_{ie_2}, as shown in Fig. 9-7(a). Therefore, when the input is positive, the signal voltage developed across the base–emitter of Q_1 is $V_S/2$, *positive on the base*. Across the base–emitter of Q_2, $V_S/2$ appears *positive on the emitter*. This is illustrated in Fig. 9-7(b). Q_1 receives the signal at its base and behaves as a *common emitter* amplifier, while Q_2 receives the signal at its emitter (its base voltage
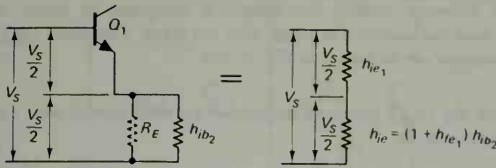
(a) Showing that V_S is equally divided between V_{be_1} and V_{be_2}
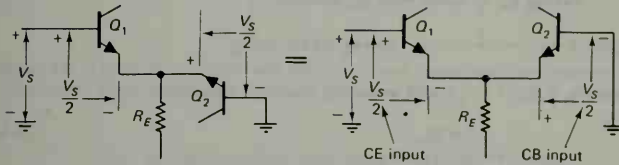
(b) Showing that V_S causes $\dfrac{V_S}{2}$ to be applied as a CE
input to Q_1 and $\dfrac{V_S}{2}$ as a CB input to Q_2
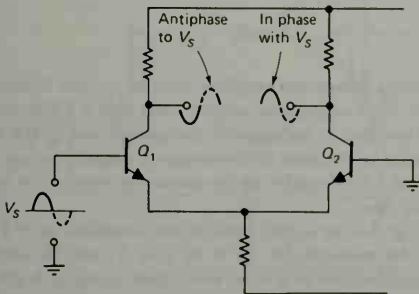
(c) Showing output signals at Q_1 and Q_2 collectors
for input to Q_1 base

Figure 9-7. Showing how an input to Q_1 produces outputs from Q_1 and Q_2.

remaining constant) and behaves as a *common base* amplifier. Since common
emitter and common base voltage gains are equal,

$$\text{Output at } Q_{1C} = \frac{-V_S}{2} \times \frac{h_{fe} R_L}{h_{ie}}$$

and

$$\text{Output at } Q_{2C} = \frac{+V_S}{2} \times \frac{h_{fe} R_L}{h_{ie}}$$

For common emitter the output is antiphase to input, while for common base the output is in phase with the input. Therefore, the input and output voltages are as shown in Fig. 9-7(c).

From Eq. (6-2), the input impedance for a CE circuit with an external emitter resistance is

$$Z_i = h_{ie} + (1 + h_{fe})R_E$$

From Fig. 9-7(a), the external resistance connected to the emitter of Q_1 is $R_E \| h_{ib_2}$. Since $R_E \gg h_{ib_2}$ (usually), R_E can be neglected.

Taking h_{ib_2} in series with Q_1 emitter,

$$Z_i = h_{ie_1} + (1 + h_{fe})h_{ib_2}$$

Since $h_{ib} = h_{ie}/(1 + h_{fe})$, and assuming matched transistors,

$$Z_i = 2h_{ie} \tag{9-5}$$

or $\qquad Z_i = 2 \times (Z_i$ for a single-stage CE circuit)

As was the case for CE and CB circuits, the (circuit) output impedance at the transistor collectors is

$$Z_O' \approx R_L \tag{9-6}$$

Figure 9-8 shows a differential amplifier with an emitter follower (Q_3) connected to provide a low-impedance output. Note that if a positive-going input is provided at terminal 1, the output is also positive going. If a positive going input is provided at terminal 2, the output is negative going. In this circumstance, terminal 1 is referred to as the *noninverting input*, while terminal 2 is called the *inverting input*.

Note that in Fig. 9-8 the supply voltages are identified as $+ V_{CC}$ and $- V_{CC}$. They could, for example, be ± 9 V or ± 12 V, and the input and output terminals could be close to ground level when no signal is present.

If in-phase signals are applied to terminals 1 and 2 at the same time, the input is referred to as a *common mode* input. In this case the transistors are operating in parallel, and the emitter current change is

$$\Delta I_E \approx \frac{V_S}{R_E} \quad (\text{Fig. 9-9})$$

$$\Delta I_{E1} \approx \Delta I_{E2} = \frac{1}{2} \Delta I_E = \frac{V_S}{2R_E}$$

and $\qquad \Delta I_C \approx \Delta I_E$

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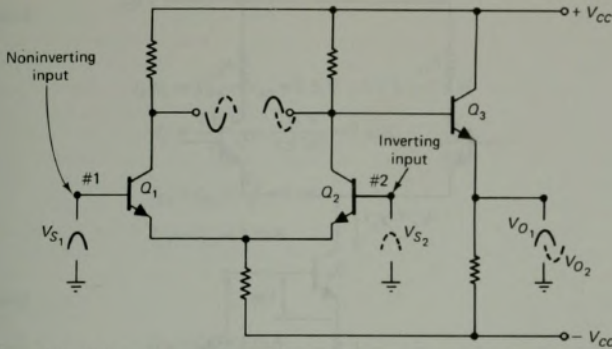
Figure 9-8. Differential amplifier with emitter follower output, showing inverting and noninverting inputs.
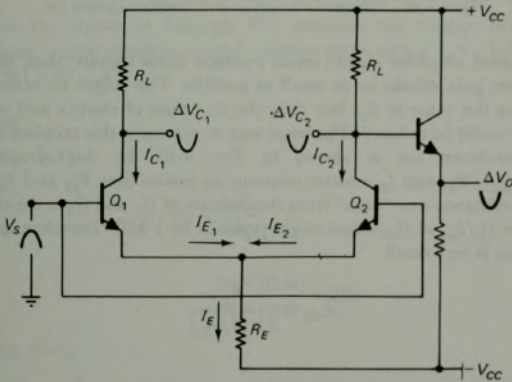
Figure 9-9. Showing common mode input signal producing in-phase outputs.

The voltage change at transistor collectors is ΔV_C, where $\Delta V_C = -\Delta I_C R_L = (-V_S R_L)/(2R_E)$, and $\Delta V_O = \Delta V_C$ because Q_3 is an emitter follower.

The common mode gain is

$$A_{CM} = \frac{\Delta V_C}{V_S} = \frac{-R_L}{2R_E} \qquad (9\text{-}7)$$

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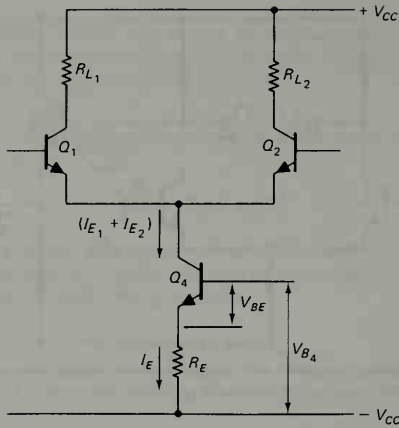
Figure 9-10. Differential amplifier with constant-current tail.

A good amplifier should reject common mode signals; thus, the common mode gain should be as small as possible. This might be achieved by increasing the value of R_E, but then the dc values of emitter and collector currents would be reduced. The usual way to overcome this problem is to use a *constant-current tail* as shown in Fig. 9-10. In this circuit $I_E = (V_{B4} - V_{BE})/R_E$, and I_E remains constant no matter how V_{B1} and V_{B2} vary. The ac resistance now "seen" from the emitters of Q_1 and Q_2 is the collector resistance $(1/h_{oe})$ of Q_4, which might typically be 1 MΩ. Therefore, common mode gain is very small.

$$A_{CM} = \frac{R_L}{2 \times (1/h_{oe})} \qquad (9\text{-}8)$$

Example 9-3

The differential amplifier shown in Fig. 9-10 has $R_{L1} = R_{L2} = 10$ kΩ and $R_E = 3.9$ kΩ. The supply voltage is ±12 V, and the voltage at the base of Q_4 is −3.5 V. If Q_1 and Q_2 bases are grounded, calculate the voltage at the Q_1 and Q_2 collectors. Assume Q_1 and Q_2 are perfectly matched and that for each transistor $V_{BE} = 0.7$ V.

solution

$$V_{B4} = (Q_4 \text{ base voltage with respect to ground}) - (-V_{CC})$$
$$= -3.5 \text{ V} + 12 \text{ V} = 8.5 \text{ V}$$

$$I_E R_E = V_{B4} - V_{BE} = 8.5 \text{ V} - 0.7 \text{ V} = 7.8 \text{ V}$$

$$I_E = \frac{7.8 \text{ V}}{R_E} = \frac{7.8 \text{ V}}{3.9 \text{ k}\Omega} = 2 \text{ mA}$$

$$I_{E1} = I_{E2} = \frac{I_E}{2} = 1 \text{ mA}$$

$$I_{C1} \approx I_{E1} = 1 \text{ mA}$$

and

$$I_{C2} \approx I_{E2} = 1 \text{ mA}$$

$$V_{C1} = V_{C2} = V_{CC} - I_C R_L = 12 \text{ V} - (1 \text{ mA} \times 10 \text{ k}\Omega) = 2 \text{ V}$$

For the circuit of Example 9-3, calculate the voltage gain, input impedance, output impedance, and common mode gain if $h_{ie} = 1$ kΩ, $h_{fe} = 50$, and $h_{oe} = 1 \times 10^{-6}$ S.

Example 9-4

solution

From Eq. (9-4),

$$A_V = \frac{h_{fe} R_L}{2 h_{ie}}$$

$$= \frac{50 \times 10 \text{ k}\Omega}{2 \times 1 \text{ k}\Omega} = 250$$

From Eq. (9-5),

$$Z_i = 2 h_{ie} = 2 \text{ k}\Omega$$

From Eq. (9-6),

$$Z_o' \approx R_L = 10 \text{ k}\Omega$$

From Eq. (9-8),

$$A_{CM} = \frac{R_L}{2 \times (1/h_{oe})} = \frac{10 \text{ k}\Omega}{2 \times 1 \times 10^6} = 5 \times 10^{-3}$$

Figure 9-11 shows the circuit of a CA3002 integrated circuit amplifier manufactured by RCA. Transistors Q_5 and Q_6 are emitter followers providing high input resistance. Q_1 and Q_2 are the main differential amplifier transistors of the circuit. Q_1 has no load resistor because no output is taken from its collector. R_3 and R_4 are small resistances which help to match the emitter currents of Q_1 and Q_2. Resistors R_7, R_8, and R_{10} provide bias to constant current transistor Q_4, and diodes D_1 and D_2 compensate for temperature variations in the base–emitter voltage of Q_4. Q_3 is an emitter follower for low output resistance.

It is important to note that the component tolerance is not critical for the differential amplifier. For example, R_{L_1} and R_{L_2} in Fig. 9-5 could be 10 k$\Omega \pm 20\%$ so long as they are closely matched to each other. Also, the absolute current gain values for Q_1 and Q_2 are not important, so long as h_{FE_1} is closely matched to h_{FE_2}.

In monolithic integrated circuit fabrication, all transistor parts are diffused at the same instant; therefore, all transistors have similar perfor-
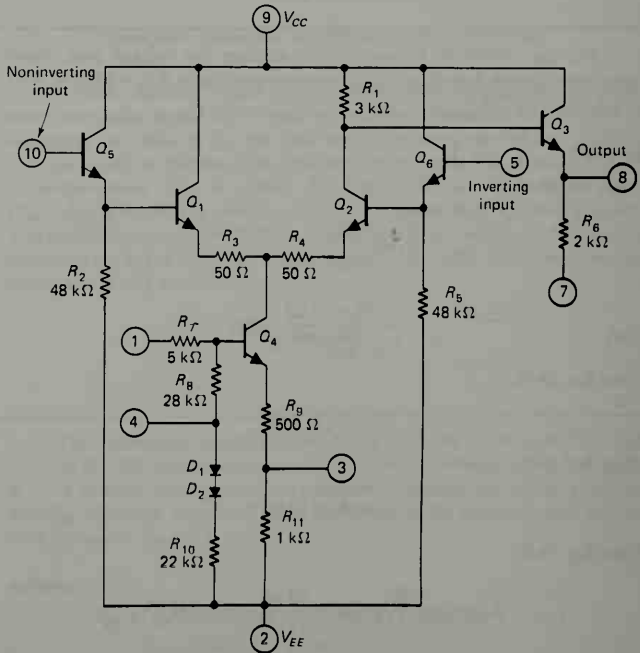
Figure 9-11. Circuit of CA3002 integrated circuit amplifier. (Courtesy of RCA Corp.)

mance. Similarly, all resistors are diffused at the same instant, and thus all resistors having the same nominal value tend to match each other closely. These facts, and the lack of a requirement for large bypass capacitors, make the differential amplifier ideal for application to integrated circuits.

In Figs. 9-12 and 9-13, condensed specifications are presented for CA3002 and μA741 IC amplifiers, respectively. There are significant differences in the performances of these two circuits, so it is important to note that the CA3002 is designed to operate over a wide frequency range, while the μA741 is intended to be a general-purpose *operational amplifier*. An *operational amplifier* is essentially a high input impedance, low output impedance high-gain circuit, with inverting and noninverting input terminals.

CA3002   IF AMPLIFIER

General-purpose amplifier used in video amplifier, product and AM detector applicatons. 10-lead JEDEC MO-006-AF package;

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10	V
Negative DC Supply Voltage	V^-	−10	V
Input Signal Voltage (Single-ended)		±3.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$, $V^- = -6V$)

Static Characteristics			
Input Unbalance Voltage	V_{IC}	2.2	mV
Input Unbalance Current	I_{IU}	2.2typ; 10 max	µA
Input Bias Current	I_I	20 typ; 36 max	µA
Quiescent Operating Voltage:			
Terminal 2 connected to V^-, terminal 4 not connected		2.8	V
Terminals 2 and 4 connected to V^-		3.9	V
Device Dissipation	P_T	55	mW
Dynamic Characteristics			
Differential Voltage Gain (Single-Ended Input and Output, $f = 1.75$ MHz)	A_{DIFF}	19 min; 24 typ	dB
−3-dB Bandwidth	BW	11	MHz
Maximum Output Voltage Swing	V_{out}(P-P)	5.5	V
Noise Figure $(R_s = 1$ kΩ, $f = 1.75$ MHz)	NF	4 typ; 8 max	dB
Parallel Input Resistance $(f = 1.75$ MHz)	R_{Ie}	100	kΩ
Parallen Input Capacitance $(f = 1.75$ MHz)	C_{Ie}	4	pF
Output Resistance $(f = 1.75$ MHz)	R_{out}	70	Ω
3rd Harmonic Intermodulation Distortion	IMD	−30 min; −40 typ	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff, $f = 1.75$ MHz)	AGC	60 min; 80 typ	dB

Figure 9-12. Condensed specification for RCA CA3002 IC amplifier. (Courtesy of RCA Corp.)

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FAIRCHILD LINEAR INTEGRATED CIRCUITS μA741

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V
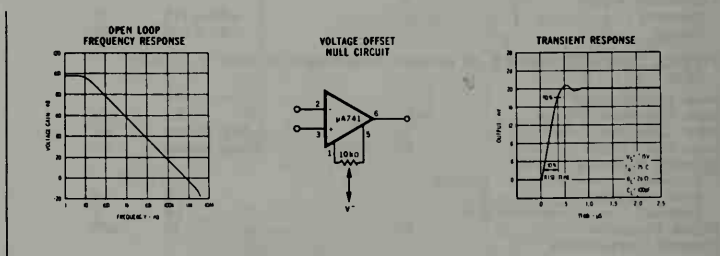
Figure 9-13. Condensed specification for μA741 IC amplifier. (Courtesy of Fairchild Semiconductors)

Some of the most important terms used in the specifications are defined as follows:

Open-loop voltage gain.   The ratio of output voltage to input voltage, i.e., the circuit internal gain.

Differential voltage gain (single-ended input and output).   The ratio of output voltage to input voltage at either one of the two inputs, i.e., same as the *open-loop gain*.

Common-mode rejection ratio.   The ratio of the amplifier open-loop gain to its common mode gain.

Input bias current. The base current to the input transistors.

Input offset current. The difference between the base currents of the input transistors.

Input unbalance current. Same as *input offset current*.

Input offset voltage. The necessary difference between bias voltages at the input transistors to obtain zero output voltage.

Input unbalance voltage. Same as *input offset voltage*.

Input resistance. The ratio of input voltage change to input current change, measured at one input terminal.

Output resistance. The ratio of output voltage change to output current change.

Slew rate. Rate of change of output voltage, expressed in volts per microsecond.

The specified 24-dB typical gain for the CA3002 is a voltage gain of approximately 16, while the typical voltage gain for the μA741 is specified as 200,000. However, the bandwidth of the CA3002 is 11 MHz, while that of the μA741 is less than 100 kHz *when the gain is reduced to approximately* 24 *dB* (see the open-loop frequency response graph).

The circuit symbol employed for IC amplifiers is shown in Fig. 9-14, together with a typical μA741 dual-in-line package and a terminal numbering diagram. The output terminal is always at the point of the triangle as shown, and the input terminals are at the opposite side. The inputs are usually identified by $+$ and $-$, indicating the noninverting input and the inverting input, respectively. Other terminals are used for connecting the positive and negative supplies and in some cases for connection of external components.

Circuit symbol

Dual-in-line package
and numbering diagram
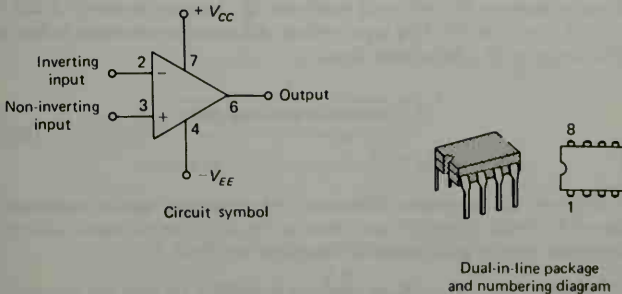
Figure 9-14. Operational amplifier circuit symbol, package, and numbering system.

The IC operational amplifier lends itself to an infinite variety of applications. Perhaps the very simplest application is the *voltage follower* circuit shown in Fig. 9-15(a). The inverting input terminal is connected directly to the output terminal. The noninverting input becomes the single input terminal of the circuit.

The output of the voltage follower follows the input voltage. This is easily seen by examining the basic operational amplifier circuit diagram in Fig. 9-15(b). As in Fig. 9-15(a), the inverting terminal (2) is connected directly to the output terminal (6). If terminal 3 is grounded, terminal 6 (and terminal 2) must also be at ground level.

Note that the bias resistors (R_2 and R_3) at the base of Q_3 potentially divide the collector voltage of Q_2, so that V_o can be lower than V_{C2}.

Suppose terminal 6 were slightly above ground level; then terminal 2 would be more positive than terminal 3, and consequently more collector current would flow in Q_2. This would cause an increased voltage drop across R_1 and thus lower the base voltage of Q_3 and the output voltage. The circuit would settle only when the voltage at terminal 2 is again equal to that at terminal 3, i.e., when $V_o = V_i$. Similarly, any movement of the output in a negative direction would produce a feedback effect which pulls the output back up until the inverting and noninverting input voltages are again equal.

When the input voltage at terminal 3 is increased or decreased, the feedback effect makes the output voltage follow the input faithfully. The actual difference between input and output voltage can be calculated from the output voltage level and the amplifier gain.

Suppose the voltage follower has an input of 5 V. The output should also be 5 V, and to produce this output voltage there must be a voltage difference between the two input terminals, i.e., between terminals 2 and 3 in Fig. 9-15(a) and (b). This input voltage difference is sometimes termed a *differential input*. The differential input is

$$V_{\text{dif}} = \frac{V_o}{\text{amplifier open loop gain}}$$

or
$$V_{\text{dif}} = \frac{V_o}{M}$$

(9-9)

To calculate the maximum differential input voltage, use the minimum value of M. From the μA741 data sheet in Fig. 9-13, the minimum value of large-signal voltage gain is 50,000. Therefore, for $V_o \approx 5$ V,

$$V_{\text{dif}} = \frac{5 \text{ V}}{50,000} = 0.1 \text{ mV}$$

This means that when the input voltage (at terminal 3 in Fig. 9-15) is +5 V,
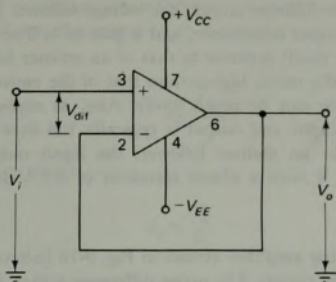
(a) Voltage follower circuit
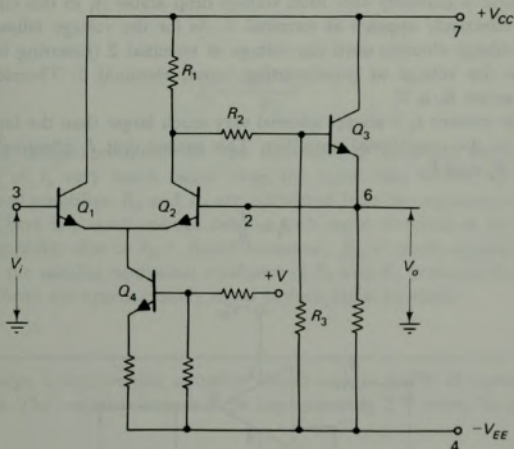
(b) Basic operational amplifier circuit
connected as a voltage follower

Figure 9-15. IC operational amplifier voltage follower.

the output voltage is actually

$$V_o = 5 \text{ V} - 0.1 \text{ mV} = 4.9999 \text{ V}$$

Terminal 2 is then 0.1 mV below the level of terminal 3, and 0.1 mV is the minimum differential input necessary to cause the output to change by approximately 5 V.

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Like an emitter follower circuit, the voltage follower has a high input impedance, a low output impedance, and a gain of 1. The voltage follower performance is very much superior to that of an emitter follower. Its input impedance is normally much higher than that of the emitter follower, and its output impedance can be much lower. Also, as explained above, the difference between input and output is typically less than 0.1 mV with a voltage follower. For an emitter follower, the input–output voltage difference may be 0.7 V with a silicon transistor or 0.3 V for a germanium device.

9-6.2
Noninverting
Amplifier

The noninverting amplifier circuit in Fig. 9-16 behaves very similarly to the voltage follower circuit. The major difference is that, instead of all the output voltage being fed directly back to the inverting input terminal (as in the voltage follower), only a portion of it is fed back. The output voltage is potentially divided by R_2 and R_3 before being applied to terminal 2.

There is normally very little voltage drop across R_1 in this circuit, so that V_i effectively appears at terminal 3. As for the voltage follower, the output voltage changes until the voltage at terminal 2 (inverting input) is equal to the voltage at (noninverting input) terminal 3. Therefore, the voltage across R_3 is V_i.

The current I_2 is always selected very much larger than the input bias current to the operational amplifier. This means that I_2 effectively flows through R_2 and R_3.

$$I_2 = \frac{V_i}{R_3} \tag{9-10}$$
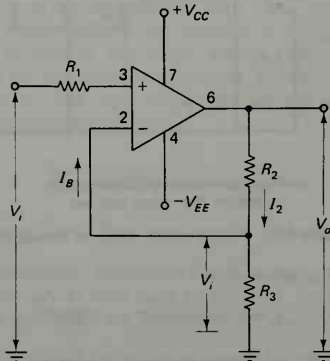
Figure 9-16. Noninverting amplifier.

The output voltage at terminal 6 (V_o) appears at one end of R_3. Since R_2 is grounded, V_o appears across ($R_2 + R_3$), and

$$I_2 = \frac{V_o}{R_2 + R_3} \qquad (9\text{-}11)$$

The circuit voltage gain is

$$A_o = \frac{V_o}{V_i}$$

From Eqs. (9-10) and 9-11,

$$V_i = I_2 R_3 \quad \text{and} \quad V_o = I_2(R_2 + R_3)$$

Therefore,

$$A_v = \frac{R_2 + R_3}{R_3} \qquad (9\text{-}12)$$

The design procedure for the noninverting amplifier begins with selection of I_2 very much larger than the input bias current I_B of the operational amplifier. R_2 and R_3 are calculated from the equations derived above. There is a small voltage drop at each input terminal of the operational amplifier due to $I_B \times$ (bias resistance). R_1 is made approximately equal to the parallel equivalent resistance of R_2 and R_3 to ensure that these voltage drops are approximately equal at each input terminal.

Design a noninverting amplifier circuit using a μA741 IC operational amplifier. The output voltage is to be approximately 2 V when the input is 50 mV.

Example 9-5

solution

$$I_2 \gg I_B$$

For the μA741, $I_{B(\text{max})} = 500$ nA.
Let

$$I_2 = 100 \times I_B = 100 \times 500 \text{ nA}$$

$$= 50 \text{ μA}$$

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From Eq. (9-10),

$$R_3 = \frac{V_i}{I_2}$$

$$= \frac{50 \text{ mv}}{50 \text{ } \mu A}$$

$$= 1 \text{ k}\Omega \quad \text{(standard resistor value)}$$

From Eq. (9-11),

$$R_2 + R_3 = \frac{V_o}{I_2}$$

$$= \frac{2 \text{ V}}{50 \text{ } \mu A}$$

$$= 40 \text{ k}\Omega$$

$$R_2 = 40 \text{ k}\Omega - R_3$$

$$= 40 \text{ k}\Omega - 1 \text{ k}\Omega$$

$$= 39 \text{ k}\Omega \quad \text{(standard resistor value)}$$

$$R_1 = R_2 \| R_3 = 1 \text{ k}\Omega \| 39 \text{ k}\Omega$$

$$\approx 1 \text{ k}\Omega$$

The input impedance of the noninverting amplifier is very high due to the feedback effect of R_2 and R_3. The input impedance can be shown to be

$$Z_i' = R_i + Z_i\left(1 + \frac{M}{A_v}\right) \tag{9-13}$$

where Z_i is the operational amplifier input impedance, M is the internal gain or open-loop gain of the operational amplifier, and A_o is the circuit voltage gain $(R_2 + R_3)/R_3$.

$Z_i = 1 \text{ M}\Omega$ typically for the μA741, and $M = 200,000$ typically. For the circuit designed in Example 9-5,

$$Z_i = 1 \text{ k}\Omega + 1 \text{ M}\Omega\left(1 + \frac{200,000}{40}\right)$$

$$= 5,000 \text{ M}\Omega$$

For obvious reasons, the noninverting amplifier is also known as a *high input impedance amplifier*.

The circuit output impedance is also affected by resistors R_2 and R_3:

$$Z_o' = \frac{Z_o}{1 + M/A_v} \tag{9-14}$$

The μA741 has $Z_o = 70 \ \Omega$ typically. Therefore, for Example 9-5,

$$Z_o' = \frac{70 \ \Omega}{1 + (200,000/40)}$$

$$= 0.014 \ \Omega$$

The name *inverting amplifier* is applied to the circuit of Fig. 9-17 simply because the output goes negative when the input goes positive, and vice versa. Note that terminal 3 is grounded via resistor R_3. Because a very small differential input (less than 1 mV) can cause the output to change by a large amount, the voltage at terminal 2 should remain very close to that at terminal 3. Therefore, terminal 2 voltage is always very close to ground. Because it is not grounded, but remains close to ground potential, the inverting input terminal in this application is sometimes termed a *virtual ground* or *virtual earth*.

If V_i in Fig. 9-17 is $+ 1$ V, the input current can be calculated as

$$I_1 = \frac{V_{R1}}{R_1}$$

Since one end of R_1 is at $V_i = 1$ V, and the other end is at ground level,

$$I_1 = \frac{V_i}{R_1} \tag{9-15}$$

From the μA741 data sheet in Fig. 9-13, the input bias current (i.e., the current flowing into terminals 2 and 3) is a maximum of $I_B = 500$ nA. If I_1 is very much greater than I_B, then effectively all of I_1 must flow through
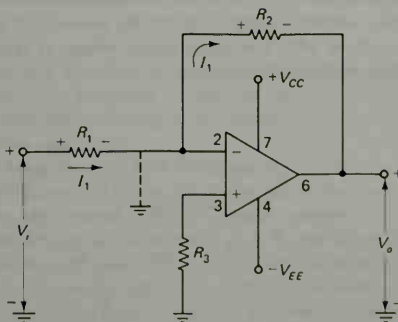
Figure 9-17. Inverting amplifier.

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resistor R_2 (see Fig. 9-17). This means that the voltage drop across R_2 is $I_1 \times R_2$. The left side of R_2 is connected to terminal 2, which, as already discussed, is always at ground potential. Therefore, the right side of R_2 is at $(I_1 \times R_2)$ volts below ground level; i.e.,

$$V_o = -(I_1 \times R_2) \qquad (9\text{-}16)$$

From Eq. (9-15),

$$V_i = I_1 R_1$$

and voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{-I_1 R_2}{I_1 R_1}$$

or

$$A_v = \frac{-R_2}{R_1} \qquad (9\text{-}17)$$

If $V_i = +10$ mV and $R_2/R_1 = 100$, then $V_o = -100 \times 10$ mV $= -1$ V. When the input voltage is negative, the output is positive. A similar kind of feedback effect to that which occurs with the voltage follower and the noninverting amplifier keeps the output voltage exactly equal to $-(R_2/R_1) \times V_i$.

The design of an inverting amplifier is quite simple. A current I_1 is selected so that $I_1 \gg I_B$. R_1 is calculated from Eq. (9-15), and R_2 is determined using either Eq. (9-16) or (9-17). R_3 is made approximately equal to the parallel equivalent resistance of R_1 and R_2.

Example 9-6

An inverting amplifier using a μA741 IC operational amplifier is to have a voltage gain of 144. The input signal voltage is typically 20 mV. Determine suitable resistor values.

solution

For the μA741,

$$I_{B(\text{max})} = 500 \text{ nA}$$

and

$$I_1 \gg I_{B(\text{max})}$$

Let

$$I_1 \approx 100 \times I_{B(\text{max})}$$

$$= 100 \times 500 \text{ nA} = 50 \ \mu\text{A}$$

From Eq. (9-15),

$$R_1 = \frac{V_i}{I_1} = \frac{20 \text{ mV}}{50 \text{ } \mu\text{A}}$$

$$= 400 \text{ } \Omega \quad \text{(use 390-}\Omega\text{ standard value; see Appendix 1)}$$

From Eq. (9-17),

$$R_2 = A_v \times R_1$$
$$= 144 \times 390 \text{ } \Omega$$
$$= 56.2 \text{ k}\Omega \quad \text{(use 56-k}\Omega\text{ standard value)}$$
$$R_3 = R_1 \| R_2 = 56 \text{ k}\Omega \| 390 \text{ } \Omega$$
$$\approx R_1 = 390 \text{ } \Omega$$

The input impedance of the inverting amplifier is

$$Z_i = \frac{V_i}{I_1} = R_1 \qquad (9\text{-}18)$$

For Example 9-6, the circuit input impedance is only 390 Ω, which is very much smaller than that obtained for the noninverting amplifier. It is seen that the inverting amplifier has a relatively low input impedance.

The output impedance of the inverting amplifier is calculated from Eq. (9-14). For the circuit in Example 9-6,

$$Z_o = \frac{70 \text{ } \Omega}{1 + (200,000/144)}$$
$$= 0.05 \text{ } \Omega$$

Like capacitor coupling, a transformer may be used to ac couple amplifier stages while providing dc isolation between stages. The dc resistance of the transformer windings is very small, so that there is no effect on the transistor bias conditions.

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Figure 9-18(a) shows a load resistance R_L transformer coupled to the collector of the transistor. The low (dc) resistance of the transformer primary winding allows any desired level of collector current to flow, while the transformer core couples all variations in I_C to R_L via the secondary winding.

The actual dc load connected in series with the collector and emitter of transistor Q_1 is $(R_{PY} + R_3)$, where R_{PY} is the resistance of the primary winding. The resistance $(R_{PY} + R_3)$ is used to draw the dc load line on the transistor characteristics. The ac load line is a little more complicated. (Note that the dc load line and ac load line for a capacitive coupled circuit are explained in Sections 5-2 and 5-8, respectively.)

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(a) Class A transformer coupled amplifier
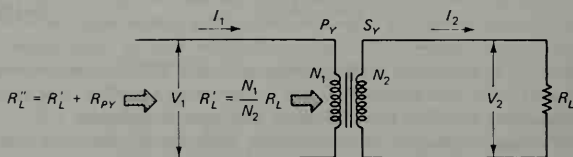
(b) Transformer showing reflected load

Figure 9-18. Class A transformer-coupled amplifier and reflected load.

Consider the transformer illustrated in Fig. 9-18(b). N_1 is the number of turns in the primary winding, and N_2 is the number of secondary turns. V_1 and I_1 are the primary voltage and current, while V_2 and I_2 are the voltage and current for the secondary.

The load resistance R_L could be calculated as

$$R_L = \frac{V_2}{I_2}$$

The ac load resistance that could be measured at the terminals of the primary is designated R_L', which is calculated from

$$R_L' = \frac{V_1}{I_1}$$

From basic transformer theory,

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} \quad \text{and} \quad \frac{I_1}{I_2} = \frac{N_2}{N_1}$$

This gives

$$V_1 = \frac{N_1}{N_2} V_2 \quad \text{and} \quad I_1 = \frac{N_2}{N_1} I_2$$

Substituting for V_1 and I_1 in the equation for R_L',

$$R_L' = \frac{(N_1/N_2)V_2}{(N_2/N_1)I_2}$$

$$= \left[\frac{N_1}{N_2} \right]^2 \frac{V_2}{I_2}$$

or
$$R_L' = \left(\frac{N_1}{N_2} \right)^2 R_L \qquad (9\text{-}19)$$

R_L' is frequently termed the *reflected load*, meaning that R_L is *reflected into* the primary as R_L'. R_L' is also described as the load resistance *referred to the primary*.

The total ac load seen by transistor Q_1 in Fig. 9-18(a) is the sum of R_L' and the dc winding resistance of the transformer primary.

The circuit shown in Fig. 9-18(a) has $V_{CC} = 11$ V, $R_1 = 4.7$ kΩ, $R_2 = 2.2$ kΩ, and $R_3 = 560$ Ω. Transformer T_1 has $R_{PY} = 40$ Ω, $N_1 = 74$, and $N_2 = 14$. The load resistance is $R_L = 56$ Ω. Draw the dc and ac load lines for the circuit on the transistor common emitter characteristics in Fig. 9-19.

Example 9-7

solution

dc load line

$$V_{CC} = I_C(R_{PY} + R_3) + V_{CE}$$

When $I_C = 0$, $V_{CC} = V_{CE}$.
Plot point A on Fig. 9-19 at $I_C = 0$, $V_{CE} = V_{CC} = 11$ V.
Another point on the dc load line (and on the ac load line) is the Q point.

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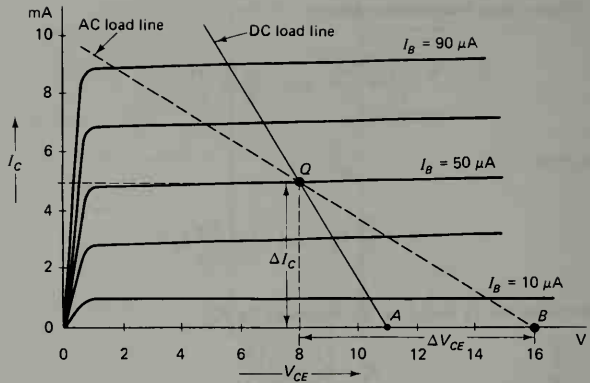
Figure 9-19. DC and ac load lines for a transformer-coupled amplifier.

This defines the dc bias conditions in the circuit.

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2} = 11 \text{ V} \times \frac{2.2 \text{ k}\Omega}{2.2 \text{ k}\Omega + 4.7 \text{ k}\Omega}$$

$$= 3.5 \text{ V}$$

$$V_E = V_B - V_{BE} = 3.5 \text{ V} - 0.7 \text{ V}$$

$$= 2.8 \text{ V}$$

$$I_E = \frac{V_E}{R_3} = \frac{2.8 \text{ V}}{560 \text{ }\Omega}$$

$$= 5 \text{ mA} \approx I_C$$

$$V_{CC} = I_C(R_{PY} + R_3) + V_{CE}$$

When $I_C = 5$ mA,

$$11 \text{ V} = 5 \text{ mA}(40 \text{ }\Omega + 560 \text{ }\Omega) + V_{CE}$$

$$V_{CE} = 8 \text{ V}$$

Plot the Q point on Fig. 9-19 at $I_C = 5$ mA and $V_{CE} = 8$ V. Draw the dc load line through points A and Q.

ac load line
Use Eq. (9-19):

$$R_L' = \left(\frac{N_1}{N_2} \right)^2 R_L$$

$$= \left(\frac{74}{14} \right)^2 \times 56 \text{ }\Omega = 1564 \text{ }\Omega$$

Total ac load,

$$R_L'' = R_{PY} + R_L'$$
$$= 40 \ \Omega + 1564 \ \Omega$$
$$= 1.6 \ k\Omega$$

When the collector current changes by $\Delta I_C = 5$ mA,

$$\Delta V_{CE} = \Delta I_C \times R_L''$$
$$= 5 \ mA \times 1.6 \ k\Omega$$
$$= 8 \ V$$

On Fig. 9-19(b) measure ΔI_C and ΔV_{CE} from the Q point to give point B at $V_{CE} = 16$ V. Draw the ac load line through points Q and B.

The ac load line drawn in Example 9-7 is reproduced in Fig. 9-20, where the effect of an input signal is also illustrated.

When the input signal causes the base current to be increased by $\Delta I_B = 40$ μA, the transistor current and voltage become those at point A' on the ac load line; i.e., $I_C \approx 9$ mA and $V_{CE} \approx 1.6$ V. Similarly, when the base current is decreased by $\Delta I_B = 40$ μA, the current and voltage (at point B') are $I_C \approx 1$ mA and $V_{CE} \approx 14.4$ V.

It is seen that a base current variation of $\Delta I_B = \pm 40$ μA causes the collector current to change by $\Delta I_C = \pm 4$ mA and the collector–emitter voltage to change by $\Delta V_{CE} = \pm 6.4$ V.

This ± 6.4-V variation in V_{CE} appears across the primary winding of transformer T_1, Fig. 9-19(a). The collector current change $\Delta I_C = \pm 4$ mA also flows through the transformer primary winding. The load current can be calculated as

$$\Delta I_L = \frac{N_1}{N_2} (\Delta I_C)$$
$$= \frac{74}{14} \times (\pm 4 \ mA)$$
$$\approx \pm 21 \ mA$$

It is important to note that although the supply voltage to the circuit in Fig. 9-19(a) is only $V_{CC} = 11$ V, the transistor collector–emitter voltage can actually go to $V_{CE} = 16$ V. This is due to the inductive effect of the transformer primary winding. When selecting a transistor for such a circuit, the breakdown voltage of the device should be approximately twice the circuit supply voltage.

The circuit in Fig. 9-18(a) is referred to as a *class A amplifier*. A class A circuit is defined as one in which the Q point is approximately at the center of the ac load line.

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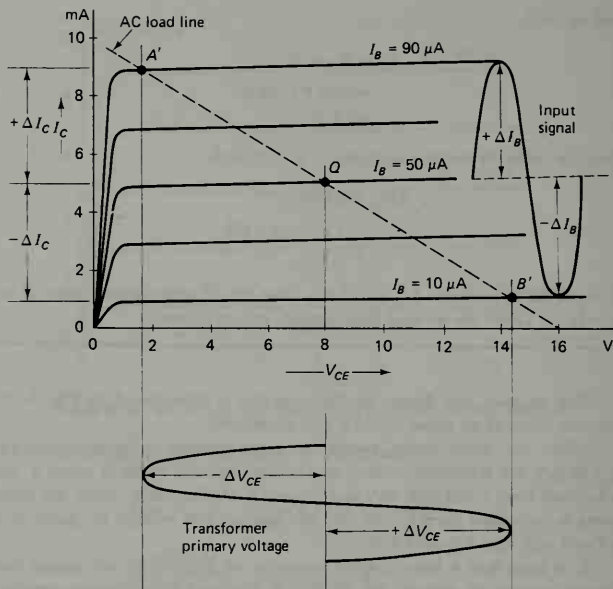
Figure 9-20. Input signal and transformer primary voltage in a transformer-coupled amplifier.

One of the most important considerations in power amplifier design is efficiency. Power dissipated when no signal is present is, of course, wasted power which reduces the efficiency of the circuit. Class A circuits dissipate considerable power due to the transistor bias conditions, and consequently they have low efficiency. In a *class B* amplifier, the transistors are biased at cutoff so that there is no transistor power dissipation when the input signal level is zero.

A basic class B circuit is illustrated in Fig. 9-21(a). Transformer T_1 couples load resistor R_L to the collector circuits of two transistors Q_1 and Q_2. Note that the primary of the transformer has a center tap to which the dc supply voltage V_{CC} is connected. Q_1 and Q_2 have grounded emitters and both are biased *off* via resistors R_1 and R_2, which ground the bases.

The input signals applied to the transistor bases consist of two separate sine waves which are identical, with the exception that they are in anti-phase. When V_1 is going positive, V_2 is going negative, so that Q_2 is being biased further *off* when Q_1 is being biased *on*. As the collector current in Q_1 increases from zero, it produces a half sine wave across the upper half of the

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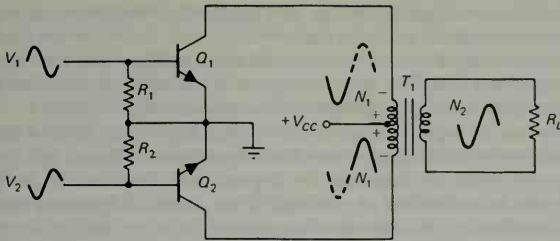
(a) Class B output stage
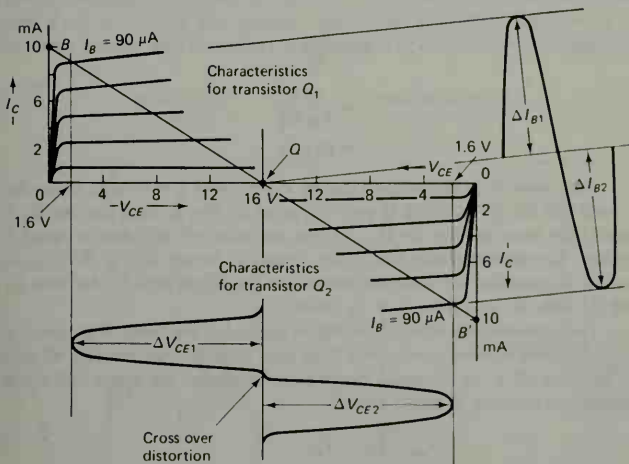
(b) Composite characteristics for class B amplifier

Figure 9-21. Class B amplifier circuit and composite characteristics.

transformer primary, as illustrated. When the positive half-cycle of input signal to Q_1 base begins to go negative, the signal at Q_2 base is commencing to go positive. Thus, as Q_1 becomes biased *off* again, Q_2 is biased *on*, and a half-cycle of waveform is generated across the lower primary winding of the transformer.

The effect of the two half-cycles in separate halves of the transformer primary is to produce a magnetic flux in the transformer core, which flows first in one direction and then in the opposite direction. This flux links with

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the transformer secondary winding and generates a complete sine wave output, which is passed on to the load.

In the class B circuit, the two output transistors are said to be operating in *push–pull*. The push–pull action is best illustrated by drawing the load line on the *composite characteristics*, as shown in Fig. 9-21(b).

Suppose the supply voltage to the circuit in Fig. 9-21(a) is $V_{CC} = 16$ V. Then, when the input signal is zero, both transistors are biased *off*: $I_C = 0$ and $V_{CE} = V_{CC} = 16$ V. Therefore, the Q point is at $I_C = 0$ and $V_{CE} = V_{CC}$. Suppose the ac load offered by each half of the transformer primary to the transistor collectors is 1.6 kΩ (as in Example 9-7).

$$V_{CE} = V_{CC} - I_C R_L''$$

and when $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_L''}$$

$$= \frac{16 \text{ V}}{1.6 \text{ k}\Omega}$$

$$= 10 \text{ mA}$$

Plot point B on the ac load line at $V_{CE} = 0$ and $I_C = 10$ mA. Draw the ac load line for Q_1 from the Q point to point B. The ac load line for Q_2 is exactly the same as that for Q_1. To best see what occurs when a signal is applied, the characteristics for Q_2 are drawn as shown in Fig. 9-21(b), so that the ac load line becomes one continuous line (from B to B') for both Q_1 and Q_2 with the bias point Q at its center.

Now consider the effect of the signal applied to the bases of Q_1 and Q_2. When Q_1 base current is increased from zero to 90 μA, Q_2 remains off and V_{CE1} falls to 1.6 V. At this point the voltage drop across the upper half of the transformer primary in Fig. 9-21(a) is

$$V_{RL} = V_{CC} - V_{CE}$$

$$= 16 \text{ V} - 1.6 \text{ V} = 14.4 \text{ V}$$

When the base current of Q_2 is increased from 0 to 90 μA, Q_1 is *off* and 14.4 V is developed across the lower half of the transformer primary winding.

As explained, a full sine wave is developed at the output of the transformer. When no signal is present, both transistors remain *off* and there is almost zero power dissipation. Some power is dissipated in each transistor only while it is conducting. The wasted power is considerably less with the class B circuit than with a class A circuit.

Actually, the waveform delivered to the transformer primary and the resultant output are not perfectly sinusoidal. *Cross-over distortion* exists, as illustrated in Fig. 9-21(b), due to the fact that the transistors do not begin to

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turn on properly until the input base–emitter voltage is about 0.5 V for a silicon device, or 0.15 V for a germanium transistor. To eliminate this effect, the transistors may be partially biased *on* instead of being biased completely *off*. With this modification, the circuit becomes a *class AB amplifier*.

Figure 9-22 shows a class AB transformer-coupled *output stage* with a class A transformer-coupled *driver stage*.

The output transformer T_2 has a center-tapped primary winding, each half of which forms a load for one of the output transistors, Q_1 and Q_2. Resistors R_4 and R_5 bias Q_1 and Q_2 partially *on*, and resistors R_6 and R_7 limit the emitter (and collector) currents to the desired bias levels. T_1 and Q_3 and the associated components comprise a class A stage. The secondary of T_1 is center tapped to provide the necessary antiphase signals to Q_1 and Q_2.

When the polarity of T_1 output is + at the top, Q_1 base voltage is positive and Q_2 base voltage is negative, as illustrated. At this time Q_1 is *on* and Q_2 is *off*. When the polarity reverses at T_1 output, the base of Q_2 becomes positive and that of Q_1 is negative. The output functions exactly as
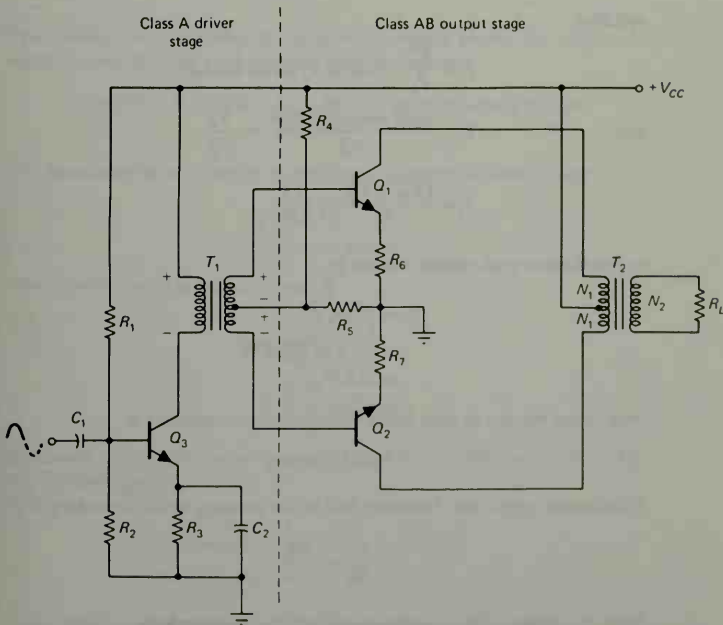
Figure 9-22. Class AB output stage with class A driver.

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for a class B circuit, with the exception that each transistor commences to conduct just before the signal to its base becomes positive. This eliminates the delay in transistor turn on, which creates cross-over distortion in a class B amplifier.

The class A circuit in this case is referred to as a *driver stage*, simply because it provides the input signals to drive the class AB output stage. The input power handled by the driver stage is very much smaller than the circuit output power; therefore, in this case the inefficiency of the class A stage is unimportant.

The design of class B and class AB transformer-coupled circuits consists largely of working out a specification for each of the components involved.

Example 9-8

A class B amplifier is to supply 5 W to a 16-Ω load. The available supply voltage is $V_{CC} = 30$ V. Specify the output transformer and output transistors.

solution

$$P_o = \frac{V_o^2}{R_L} \quad \text{(where } V_o \text{ is rms voltage)}$$

and

$$V_o = \frac{\text{peak output voltage}}{\sqrt{2}} = \frac{V_P}{\sqrt{2}}$$

$$P_o = \frac{\left(V_P/\sqrt{2}\right)^2}{R_L} = \frac{V_P^2}{2R_L}$$

or transformer peak output voltage is

$$V_P = \sqrt{2R_L P_o}$$
$$= \sqrt{2 \times 16\ \Omega \times 5\ \text{W}}$$
$$\approx 12.6\ \text{V}$$

Peak input voltage to each half of the transformer primary is

$$V_P' \approx V_{CC} = 30\ \text{V}$$

Transformer turns ratio from one half of the primary to the secondary is

$$\frac{N_1}{N_2} = \frac{30}{12.6}$$

From the whole primary to the secondary, the turns ratio is

$$\frac{2N_1}{N_2} = \frac{60}{12.6}$$

The ac load resistance appearing at each half of the primary is, using Eq. (9-19),

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$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L$$

$$= \left(\frac{30}{12.6}\right)^2 \times 16 \ \Omega \approx 91 \ \Omega$$

The total load appearing at the terminals of the whole primary is

$$R''_L = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

$$= \left(\frac{60}{12.6}\right)^2 \times 16 \ \Omega \approx 363 \ \Omega$$

The transformer is specified in terms of its output power, the load to be supplied, and the total load reflected into the primary:

$$P_o = 5 \ \text{W}, \quad R_L = 16 \ \Omega, \quad R''_L = 363 \ \Omega, \quad \text{primary center tapped}$$

The transistors have to survive a maximum collector–emitter voltage of

$$V_{CE} = 2 \times V_{CC}$$
$$= 2 \times 30 \ \text{V} = 60 \ \text{V}$$

The transistor peak collector current is

$$I_P = \frac{V_{CC}}{R'_L}$$

$$= \frac{30 \ \text{V}}{91 \ \Omega} \approx 330 \ \text{mA}$$

Maximum power dissipation occurs in the output transistors when $V_{CE} = \frac{1}{2} V_{CC}$ and $I_C = \frac{1}{2} I_P$:

$$P = \frac{V_{CC}}{2} \times \frac{I_P}{2} = \frac{30 \ \text{V}}{2} \times \frac{330 \ \text{mA}}{2}$$

$$\approx 2.5 \ \text{W}$$

The transistors are specified in terms of maximum I_C, V_{CE}, and P:

$$I_{C(\text{max})} = 330 \ \text{mA}, \quad V_{CE(\text{max})} = 60 \ \text{V}, \quad P_{\text{max}} = 2.5 \ \text{W}$$

In some situations where a fairly large output current is to be supplied by an emitter follower, the input current to the emitter follower is so large that it cannot be supplied from the output of most amplifiers. For example, an emitter follower with an emitter current of $I_E = 500$ mA and a current gain of $h_{FE} = 49$ requires a base current of

$$I_B = \frac{I_E}{1 + h_{FE}} = \frac{500 \text{ mA}}{1 + 49}$$

$$= 10 \text{ mA}$$

To further reduce the level of input current, another (emitter follower) transistor is connected as illustrated in Fig. 9-23. This circuit is known as a *Darlington pair*, and it can be made up of *npn* transistors, Fig. 9-23(a), or of *pnp* transistors as shown in Fig. 9-23(b).

Q_2 is the output transistor carrying the load current. Q_1 is the input transistor. The load current is I_{E2}, and the base current to Q_2 is

$$I_{B2} = \frac{I_{E2}}{1 + h_{FE2}}$$

$$= I_{E1}$$

The input current is I_{B1}:

$$I_{B1} = \frac{I_{E1}}{1 + h_{FE1}}$$

$$= \frac{I_{E2}}{(1 + h_{FE1})(1 + h_{FE2})} \tag{9-20}$$
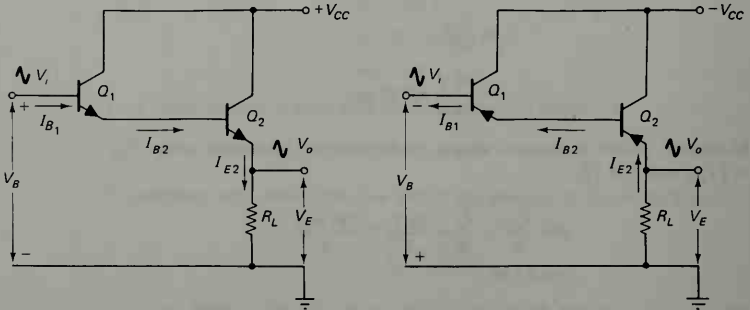
(a) *npn* darlington pair

(b) *pnp* darlington pair

Figure 9-23. Darlington-pair emitter follower.

or
$$I_{B1} \approx \frac{I_{E2}}{h_{FE1} \times h_{FE2}} \qquad (9\text{-}21)$$

Because the h_{FE} (or beta) of the two-transistor combination is ($h_{FE1} \times h_{FE2}$), the Darlington pair is also termed a *superbeta circuit*.

A Darlington pair as in Fig. 9-23 (a) is made up of a 2N3055 for Q_2 and a 2N3904 for Q_1. The load resistance ($R_L = 10\ \Omega$) is to be supplied with 4 V. The circuit supply voltage is $V_{CC} = 10$ V. Calculate the maximum level of input current, the input voltage level, and the power dissipated in each transistor.

Example 9-9

solution

input voltage

$$V_i = V_o + V_{BE1} + V_{BE2}$$

$$= 4\ \text{V} + 0.7\ \text{V} + 0.7\ \text{V}$$

$$= 5.4\ \text{V}$$

output current

$$I_{E2} = \frac{V_o}{R_L} = \frac{4\ \text{V}}{100}$$

$$= 400\ \text{mA}$$

$$I_{B2} = \frac{I_{E2}}{1 + h_{FE2}}$$

From Fig. 8-2, the minimum h_{FE} value listed for the 2N3055 is $h_{FE} = 20$. (Note that this is at $I_C = 4$A. At 400 mA h_{FE} is likely to be greater than 20.)

$$I_{B2(\text{max})} = \frac{400\ \text{mA}}{1 + 20} \approx 19\ \text{mA}$$

$$I_{B1} = \frac{I_{B2}}{1 + h_{FE1}}$$

From Fig. 8-1, the minimum h_{FE} value (at $I_C = 1$ mA) is around 70.

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input current

$$I_{B1(\text{max})} = \frac{19 \text{ mA}}{1+70} \approx 270 \text{ } \mu\text{A}$$

$$P_2 = V_{CE2} \times I_{C2}$$

$$\approx (V_{CC} - V_o) \times I_{E2} = (10 \text{ V} - 4 \text{ V}) \times 400 \text{ mA}$$

$$= 2.4 \text{ W}$$

$$P_1 = V_{CE1} \times I_{C1}$$

$$\approx (V_{CC} - V_{E1}) \times I_{B2} = (10 \text{ V} - 4.7 \text{ V}) \times 19 \text{ mA}$$

$$= 0.1 \text{ W}$$

The input impedance of a Darlington pair is

$$Z_i \approx h_{fe1} \times h_{fe2} \times R_L \tag{9-22}$$

For $h_{fe1} = 70$, $h_{fe2} = 20$, and $R_L = 100$,

$$Z_i \approx 70 \times 20 \times 100 \text{ } \Omega$$

$$\approx 140 \text{ k}\Omega$$

This value is, of course, modified by any bias resistors that might be employed at the input. The output impedance at the emitter of Q_2 is

$$Z_o \approx \frac{R_s}{h_{fe1} \times h_{fe2}} \tag{9-23}$$

where R_s is the impedance of the signal source. For $h_{fe1} = 70$, $h_{fe2} = 20$, and $R_s = 1$ kΩ,

$$Z_o \approx \frac{1 \text{ k}\Omega}{70 \times 20}$$

$$\approx 0.7 \text{ } \Omega$$

This is a very low output impedance, but it is very important to note that in general it applies only for very low frequency operation and for small-signal operation at higher frequencies (i.e., for signals much less than V_{BE}). If the circuit is operated at high frequency with a large input signal, the transistor base–emitter voltage can be reversed when the large fast-moving signal is going in a negative direction. The result is that the output waveform is partially *chopped off* or at least seriously distorted.

The *complementary emitter follower* circuit shown in Fig. 9-24 eliminates the problem discussed above. It is seen that the circuit consists of an *npn* transistor Q_1 connected in series with a *pnp* transistor Q_2. The load resistor R_L is capacitor coupled, but it could be direct coupled if + and − supply voltages are used. Transistor Q_3 and resistors R_3, R_4, and R_5 show one

method of providing bias and input to Q_1 and Q_2. R_4 must have a voltage drop across it of approximately $2 \times V_{BE}$. Capacitor C_1 bypasses R_4 to ensure that the ac input signal is developed equally at the bases of Q_1 and Q_2. Emitter resistors R_1 and R_2 limit the bias current flowing through Q_1 and Q_2.

When the input signal to the bases of Q_1 and Q_2 is large and going positive, Q_2 base–emitter might become reverse biased. This is not important because under these conditions Q_1 base–emitter will be very definitely forward biased. Similarly, when a large input is going in a negative direction, the base–emitter of Q_1 might become reverse biased, but Q_2 base–emitter junction will be forward biased. Thus, the complementary emitter follower provides a low output impedance under all conditions of input signal.
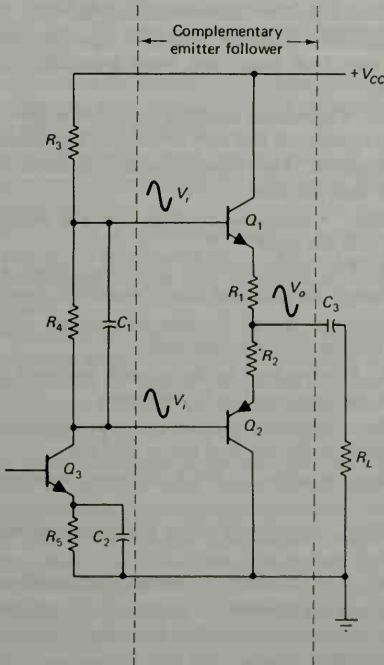
Figure 9-24. Complementary emitter follower.

Capacitor coupling. Signal transference between amplifier stages by means of interconnecting capacitors.

Direct coupling. Direct connection between amplifier stages.

DC feedback pair. Two-stage directly coupled amplifier in which each stage is biased from the other.

Differential amplifier. Amplifier which uses two emitter-coupled transistors.

Inverting input. Input terminal of a differential amplifier which produces an antiphase output when a signal is applied.

Noninverting input. Input terminal of a differential amplifier which produces an in-phase output when a signal is applied.

Common mode gain. Ratio of output voltage to a common signal applied to both inputs of a differential amplifier.

Constant current tail. Additional transistor connected to provide a constant emitter current for a differential amplifier.

Operational amplifier. Amplifier with two input terminals, one output terminal, very high gain, high input impedance, and low output impedance.

Voltage follower. Operational amplifier connected to give a gain of 1, very high input impedance, and very low output impedance.

Noninverting amplifier. Operational amplifier circuit in which the output is in phase with the input.

Inverting amplifier. Operational amplifier circuit in which the output is in antiphase with the input.

Virtual ground. One input terminal of an operational amplifier circuit which although not grounded always remains at ground level.

Transformer coupling. Signal transference between amplifier stages by means of interconnecting transformers.

Reflected load. Effective load at the primary terminals of a transformer due to the load connected to the secondary.

Class A amplifier. Amplifier in which the output transistor's bias point is approximately at the center of the ac load line.

Class B amplifier. Amplifier in which the output transistors are biased at cutoff.

Class AB amplifier. Amplifier in which the output transistors are partially biased *on*.

Darlington pair. Two transistors connected as cascaded emitter followers.

Complementary emitter follower. Two transistors, one *npn*, the other *pnp*, connected to function as emitter followers with common input and output terminals.

Review Questions

9-1. Sketch the complete circuit of two emitter current bias stages using capacitor coupling. Briefly explain the function of every component.

9-2. Discuss the approach to designing a two-stage capacitor-coupled transistor amplifier. Explain the method of calculating each component and the reasoning behind the method.

9-3. Sketch the circuit of a DC feedback pair. Briefly explain the biasing method for each transistor, and discuss the function of each component in the circuit.

9-4. Sketch the circuit of a basic differential amplifier. Briefly explain how the biasing technique affects the component currents and voltage drops.

9-5. For a differential amplifier, show that the gain $A_v = (h_{fe} R_L)/2h_{ie}$. Also derive an expression for common mode gain and show how the common mode gain can be reduced.

9-6. Sketch the circuit of a differential amplifier with an emitter follower output. Identify the inverting and noninverting input terminals.

9-7. Sketch the circuit of a differential amplifier with a constant current tail. Explain how the constant current tail functions and how it affects the circuit.

9-8. Sketch the circuit of the CA3002 IC amplifier. Explain the function of all components. Also explain why the differential amplifier is extensively employed in integrated circuits.

9-9. Define *operational amplifier*. State typical values of open-loop gain, input bias current, input impedance, and output impedance for an IC operational amplifier.

9-10. Sketch the circuit of an operational amplifier employed as a voltage follower. Identify all terminals of the amplifier. Also sketch the basic operational amplifier circuit and explain how it functions as a voltage follower.

9-11. Sketch the circuit of an operational amplifier connected to function as a noninverting amplifier. Identify all terminals of the amplifier. Derive the equation for voltage gain of the noninverting amplifier, and write equations for input and output impedance.

9-12. Repeat Question 9-11 for an inverting amplifier.

9-13. Sketch the circuit of a class A transformer-coupled amplifier. Briefly explain how it functions. Also derive an equation for the load reflected from the secondary winding of transformer into the primary.

9-14. Sketch the basic circuit of a class B transformer-coupled output stage, and briefly explain how it functions. Also explain the advantages of class B operation over class A.

9-15. Sketch the complete circuit of a class AB transformer-coupled amplifier with a class A driver stage. Explain how the circuit operates, and explain the advantage of class AB operation over class B operation.

9-16. Sketch the circuits of *npn* and *pnp* Darlington pairs. Identify all currents, and derive the equation for the current gain of the Darlington pair.

9-17. Sketch the circuit of a complementary emitter follower. Explain how it functions and what its advantages are over an ordinary emitter follower.

Problems

9-1. Design a two-stage capacitor-coupled small-signal amplifier to meet the following specification: supply voltage = 25 V, $f_1 = 75$ Hz, $A_v =$ large as possible. Use 2N3904 transistors and make $I_C = 1.5$ mA.

9-2. A two-stage capacitor-coupled amplifier uses 2N3904 transistors with $I_C = 2$ mA and $V_{CC} = 15$ V. Design the circuit to have the largest possible gain and to have $f_1 = 150$ Hz. Use emitter current bias for each stage.

9-3. Repeat Problem 9-2 using collector-to-base bias for each stage.

9-4. A dc feedback pair is to operate from a supply of 15 V. Using transistors with $h_{FE} = h_{fe} = 75$ and $h_{ie} = 1.5$ kΩ, design the circuit to have $I_C = 0.9$ mA. Make $f_1 = 200$ Hz.

9-5. Using 2N3904 transistors with $V_{CC} = 20$ V and $I_C = 1$ mA, design a dc feedback pair with $f_1 = 250$ Hz.

9-6. The differential amplifier in Fig. 9-5 has $R_{L1} = R_{L2} = 4.7$ kΩ, $R_E = 2.2$ kΩ, $V_{CC} = 20$ V, and $V_B = 8$ V. Taking $V_{BE} = 0.7$ V, calculate V_{C1} and V_{C2}.

9-7. For the circuit described in Problem 9-6, calculate the single-sided voltage gain, common mode gain, input impedance, and output impedance. Take $h_{ie} = 1.5$ kΩ, $h_{fe} = 75$, and $h_{oe} = 1 \times 10^{-6}$ S.

9-8. The CA3002 IC amplifier shown in Fig. 9-11 has its supply and bias voltages connected as follows: V_{CC} (at terminal 9) = +10 V, V_{EE} (at terminal 2) = −10 V, V (at terminal 1) = −5 V, V (at terminal 7) = 0 V, and V (at terminals 5 and 10) = 0 V. Calculate the output voltage at terminal 8.

9-9. An operational amplifier used as a voltage follower has a typical open-loop gain of 200,000. If the maximum input signal voltage is exactly 8 V, calculate the level of maximum output.

9-10. Design a noninverting amplifier using a μA741 operational amplifier. The output voltage from the circuit is to be ±5 V when the input signal is ±75 mV.

9-11. A noninverting amplifier uses an operational amplifier with an input bias current of 750 nA. Design the circuit to have a voltage gain of 120 when $V_{o(max)} = 10$ V.

9-12. An inverting amplifier using a μA741 operational amplifier is to have a voltage gain of 200. The input signal voltage is 45 mV. Calculate suitable resistor values, and determine the circuit input impedance.

9-13. An inverting amplifier is to have an input impedance of 1 kΩ. When the signal voltage is ±100 mV, the output is to be ±3.3 V. Determine suitable resistor values.

9-14. A class A transformer-coupled amplifier, as in Fig. 9-18(a), has $V_{CC} = 20$ V. The bias resistors are $R_1 = 3.9$ kΩ and $R_2 = 1$ kΩ, and the emitter resistor is $R_3 = 68$ Ω. The transformer has a primary winding resistance of $R_{p_1} = 32$ Ω, $N_1 = 80$, and $N_2 = 20$. The load resistance is $R_L = 23$ Ω. Plot the dc load line and ac load line for this circuit on blank characteristics with vertical ordinate as $I_C = (0$ to 100 mA) and horizontal ordinate $V_{CE} = (0$ to 40 V).

9-15. A class B transformer-coupled amplifier, as in Fig. 9-21(a), uses a transformer which has *total* primary turns of $N_1 = 160$ and $N_2 = 20$. The load resistance is $R_L = 23$ Ω, and the *total* primary winding resistance is $R_{p_1} = 64$ Ω. Using blank characteristics with $I_C = (0$ to 100 mA) and $V_{CE} = (0$ to 40 V), plot the *complete* ac load line for the circuit.

9-16. A class B amplifier is to supply 8 W to a 12-Ω load. The supply is $V_{CC} = 25$ V. Specify the output transformer and transistors.

9-17. A class B amplifier uses a transformer with $N_1/N_2 = 5$ (where N_1 is the total number of primary turns on a center-tapped primary). The supply voltage is 45 V, and the load resistance is 8 Ω. Determine the maximum output voltage and power from the circuit, and specify the maximum transistor voltage, current, and power dissipation.

9-18. A Darlington pair has a load resistance of $R_L = 120$ Ω, which is to be supplied with 6 V. The output transistor has $h_{FE} = 25$, and the input transistor has $h_{FE} = 50$. The circuit supply is $V_{CC} = 25$ V. Calculate the input current, input voltage level, and the power dissipated in each transistor.

Basic Sinusoidal Oscillators

10-1
Introduction

A sinusoidal oscillator consists basically of an amplifier and a phase-shifting network. The amplifier receives the output of the phase-shifting network, amplifies it, phase shifts it through 180° and applies it to the input of the network. The network phase shifts the amplifier output through another 180° and attenuates it before applying it back to the amplifier input. When the amplifier gain and phase shift are equal to the network attenuation and phase shift, the circuit is amplifying an input signal to produce an output which is attenuated to become the input signal. The circuit is generating its own input, and a state of oscillation exists.

For oscillation to be sustained certain conditions, known as the *Barkhausen criteria*, must be fulfilled. These are *the loop gain of the circuit must be equal to (or greater than) 1, and the phase shift around the circuit must be zero.*

10-2
Phase-
Shift
Oscillator

In the phase-shift oscillator an external resistor–capacitor (RC) network feeds a portion of the ac output of an amplifier back to the amplifier input. If the amplifier has an internal phase shift of 180° and the

230

network provides a further 180° phase shift, the signal fed back to the input can be amplified to reproduce the output. The circuit is then generating its own input signal, and a state of oscillation is sustained.

Figure 10-1 shows an IC operational amplifier connected as an inverting amplifier (see Section 9-6) to give a 180° phase shift between amplifier input and output. An RC network consisting of three equal-value capacitors and three equal resistors is connected between the amplifier output and input terminals. Each stage of the network provides some phase shift to give a total of 180° from output to input.

The frequency of the oscillator output depends upon the capacitor and resistor values employed. Using basic RC circuit analysis methods, it can be shown that the network phase shift is 180° when the oscillating frequency is

$$f = \frac{1}{2\pi RC\sqrt{6}} \qquad (10\text{-}1)$$
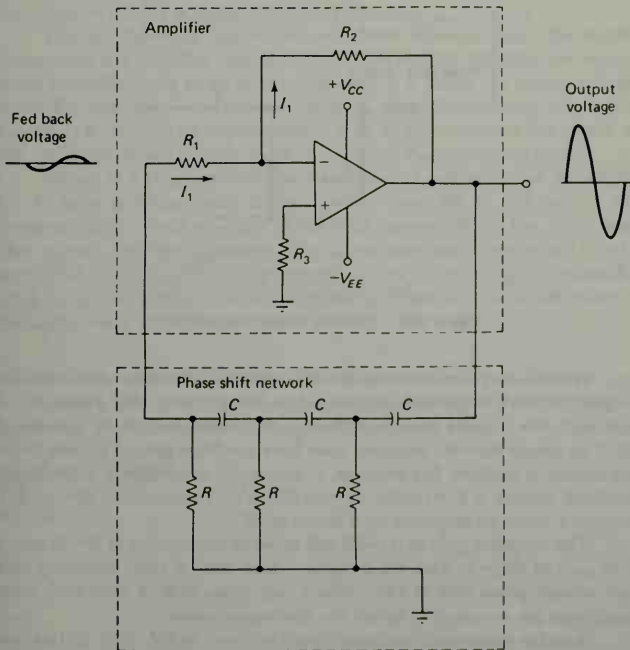
Figure 10-1. Phase-shift oscillator using an IC operational amplifier.
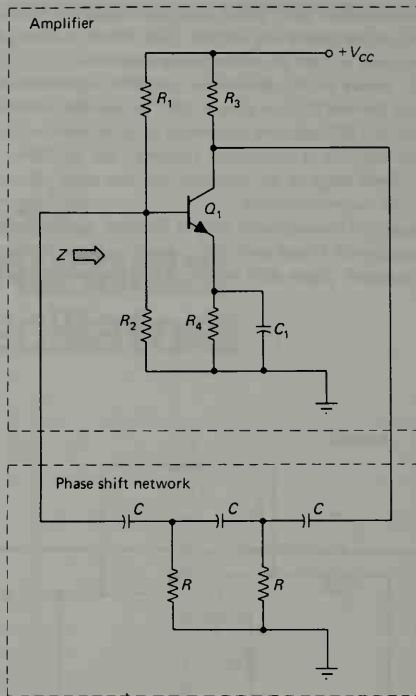
Figure 10-2. Transistor phase-shift oscillator.

As well as phase shifting, the RC network attenuates the amplifier output. Network analysis shows that, when the necessary 180° phase shift is achieved, this network always attenuates the output voltage by a factor of 29. This means that the amplifier must have a voltage gain of at least 29 for the circuit to oscillate. For example, if the output amplitude is ± 2.9 V, the feedback voltage is $V_i = (\pm 2.9/29) = \pm 100$ mV. To reproduce the ± 2.9-V output, V_i must be amplified by a factor of 29.

The amplifier gain of $A_v = 29$ and network attenuation of $\beta = 29$ give a loop gain of $\beta A_v = 1$. Also, the amplifier phase shift of 180° combined with the network phase shift of 180° gives a loop phase shift of zero. Both these conditions are necessary to satisfy the *Barkhausen criteria*.

Another phase-shift oscillator circuit is shown in Fig. 10-2. In this case a single common emitter transistor amplifier stage is employed. The com-

mon emitter circuit has 180° phase shift between input and output, and the RC network phase shifts the output to reproduce the necessary input. Once again the amplifier must have a voltage gain of at least 29. Note that the amplifier input resistance (Z) forms the last resistor of the RC network.

The input impedance of the RC network loads the amplifier, and (especially in the circuit of Fig. 10-2) this affects the amplifier gain. As frequency increases, the capacitor impedances decrease, so that the loading effect is greatest at high frequencies. When the loading effect reduces the amplifier gain below 29, the circuit will not oscillate. It is found that the phase-shift oscillator is most suitable for frequencies ranging up to a maximum of about 100 kHz.

An external load can also reduce the amplifier gain and cause the circuit to cease oscillating. Because the operational amplifier circuit in Fig. 10-1 has a very low output impedance, it is less likely to be affected by overloads than the circuit of Fig. 10-2.

If the amplifier gain is much greater than 29, the oscillator output waveform is likely to be distorted. When the gain is slightly greater than 29, the output is usually a reasonably pure sine wave.

The amplitude of the output waveform depends upon the supply voltage and the amplifier bias conditions. The output voltage of the operational amplifier tends to go to approximately 1 V below the supply voltage levels. For example, if the supply is ± 15 V, then the oscillator output (for Fig. 10-1) is likely to be approximately ± 14 V. In the case of the circuit in Fig. 10-2, the output is likely to be $\pm V_{CE}$ or $\pm V_{R3}$, whichever is least.

Design of a phase-shift oscillator commences with design of the amplifier to have a voltage gain slightly greater than 29. In the case of the transistor circuit, final selection of the load resistor (R_3 in Fig. 10-2) may have to wait until the attenuator input impedance can be estimated to take account of its loading effect. The network resistor value (R) is determined by considering the amplifier input impedance. Then the capacitor value is calculated using Eq. (10-1).

Using a μA741 IC operational amplifier, with $V_{CC} = +10$ V, design a phase-shift oscillator to have an output frequency of 1 kHz.

<div align="right">**Example 10-1**</div>

solution

amplifier

$$I_1 = \frac{V_1}{R_1}$$

and

$$I_1 \gg I_{B(max)}$$

For the μA741, $I_{B(max)} = 500$ nA.
Let

$$I_1 \approx 100 \times I_B$$
$$= 100 \times 50 \text{ nA} = 50 \text{ μA}$$
$$V_O \approx \pm(V_{CC} - 1 \text{ V}) = \pm(10 \text{ V} - 1) = \pm 9 \text{ V}$$
$$V_i \approx \frac{9 \text{ V}}{29}$$

and

$$R_1 = \frac{V_i}{I_1} = \frac{9 \text{ V}}{29 \times 50 \text{ μA}}$$

$$\approx 6.2 \text{ kΩ} \quad \text{(use 5.6-kΩ standard resistor value; see Appendix 1)}$$
$$R_2 = A_v \times R_1 = 29 \times 5.6 \text{ kΩ}$$
$$\approx 162 \text{ kΩ} \quad \text{(use 180-kΩ standard value to give } A_v > 29)$$
$$R_3 = R_1 \| R_2 \approx 5.6 \text{ kΩ}$$

RC network

$$\text{Amplifier } Z_i = R_1 = 5.6 \text{ kΩ}$$

To ensure that R_1 does not load R significantly, make $R < R_1$.
Let $R = R_1/10 = 560$ Ω.
From Eq. (10-1),

$$C = \frac{1}{2\pi R f \sqrt{6}}$$

$$= \frac{1}{2\pi \times 560 \text{ Ω} \times 1 \text{ kHz} \sqrt{6}}$$
$$= 0.116 \text{ μF} \quad \text{(use 0.12-μF standard capacitor value; see Appendix 2)}$$

10-3
Colpitts
Oscillator

The *Colpitts oscillator* circuit shown in Fig. 10-3 uses an *LC* network (C_1, C_2, and L) to provide the necessary phase shift between amplifier output voltage and feedback voltage. In this case the network acts as a filter to pass the desired oscillating frequency and block all other frequencies. The filter circuit resonates at the desired oscillating frequency. For resonance,

$$X_L = X_{CT}$$

where X_{CT} is the reactance of the total capacitance in parallel with the
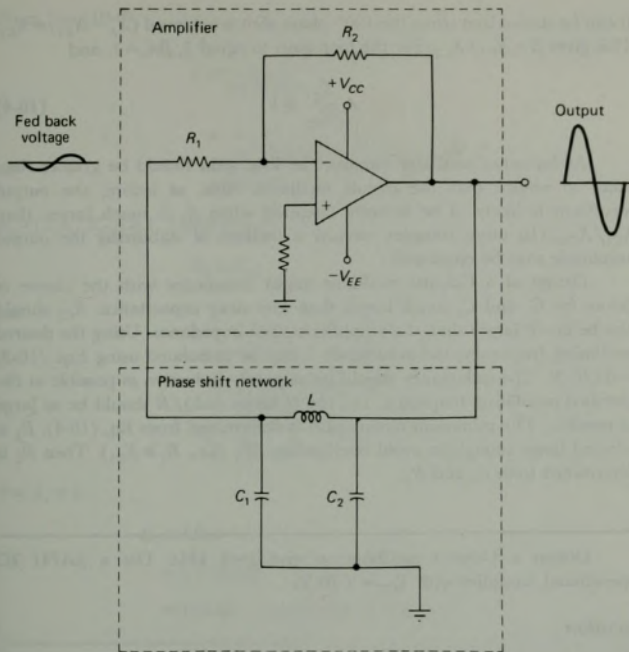
Figure 10-3. Colpitts oscillator using an IC operational amplifier.

inductance. This gives the resonance frequency (and oscillating frequency) as

$$f = \frac{1}{2\pi\sqrt{LC_T}} \qquad (10\text{-}2)$$

where

$$C_T = \frac{C_1 C_2}{C_1 + C_2} \qquad (10\text{-}3)$$

Consideration of the LC network shows that its attenuation (from the amplifier output to input) is

$$\beta = \frac{X_{C1}}{X_L - X_{C1}}$$

It can be shown that when the 180° phase shift is achieved $(X_L - X_{C1}) = X_{C2}$. This gives $\beta = X_{C1}/X_{C2}$. For the loop gain to equal 1, $\beta A_v = 1$, and

$$A_v \frac{X_{C1}}{X_{C2}} \geqslant 1 \qquad (10\text{-}4)$$

As for other oscillator circuits, the loop gain should be greater than unity to ensure that the circuit oscillates. Also, as before, the output waveform is likely to be severely distorted when A_v is much larger than X_{C1}/X_{C2}. (In more complex circuits a method of stabilizing the output amplitude may be employed.)

Design of a Colpitts oscillator might commence with the choice of values for C_1 and C_2 much larger than any stray capacitance. X_{C2} should also be much larger than the amplifier output impedance. Using the desired oscillating frequency, the inductance L can be calculated using Eqs. (10-2) and (10-3). The inductance should be as purely inductive as possible at the specified oscillating frequency; i.e., the Q factor $(\omega L)/R$ should be as large as possible. The minimum circuit gain is determined from Eq. (10-4). R_1 is selected large enough to avoid overloading X_{C1} (i.e., $R_1 \gg X_{C1}$). Then R_2 is determined from A_v and R_1.

Example 10-2

Design a Colpitts oscillator to give $f = 4$ kHz. Use a μA741 IC operational amplifier with $V_{CC} = \pm 10$ V.

solution

$X_{C2} \gg$ than any stray capacitance; take $C_2 = 0.1$ μF and let $C_1 = C_2$. Use Eq. (10-3):

$$C_T = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.1\ \mu\text{F} \times 0.1\ \mu\text{F}}{0.1\ \mu\text{F} + 0.1\ \mu\text{F}}$$

$$= 0.05\ \mu\text{F}$$

At $f = 4$ kHz,

$$X_{C2} = \frac{1}{2\pi \times 4\ \text{kHz} \times 0.1\ \mu\text{F}}$$

$$= 398\ \Omega$$

and the μA741 has $Z_O \approx 70\ \Omega$

$$X_{C2} \gg Z_O$$

From Eq. (10-2),

$$L = \frac{1}{4\pi^2 f^2 C_T}$$

$$= \frac{1}{4\pi^2 \times (4 \text{ kHz})_2 \times 0.05 \ \mu\text{F}}$$

$$\approx 32 \text{ mH}$$

$A_v \geqslant (X_{C1}/X_{C2}) \geqslant 1$. Make $A_v \approx 4$.

$$R_1 > X_{C1}$$

Let

$$R \approx 100 \times X_{C1} = 100 \times 398 \ \Omega$$

$$\approx 39 \text{ k}\Omega \quad \text{(standard value)}$$

$$A_v = \frac{R_2}{R_1}$$

For $A_v = 4$,

$$R_2 = 4R_1$$

$$= 4 \times 39 \text{ k}\Omega$$

$$= 156 \text{ k}\Omega \quad \text{(use 150-k}\Omega \text{ standard value)}$$

A Colpitts oscillator using a single-stage transistor amplifier is shown in Fig. 10-4(a). This is the basic circuit, and its similarity to Fig. 10-3 is fairly obvious. A more practical version of the circuit is shown in Fig. 10-4(b). Here Q_1, R_1, R_2, R_4, and C_3 are unchanged from Fig. 10-4(a). However, in (b) L has replaced the load resistor R_3. A radio frequency choke (RFC) is included in series with V_{CC} and L. This allows direct current I_C to pass, but offers a very high impedance at the oscillating frequency. The upper end of L is ac isolated (by RFC) from V_{CC} and ground. The output of the phase-shifting network is coupled via C_c from the junction of L and C_1 to the amplifier input at Q_1 base. The output voltage V_o is derived from a secondary winding L_2 coupled to the inductance L.

The *Hartley oscillator* circuit is similar to the Colpitts oscillator, except that the phase-shift network consists of two inductors and a capacitor instead of two capacitors and an inductor.
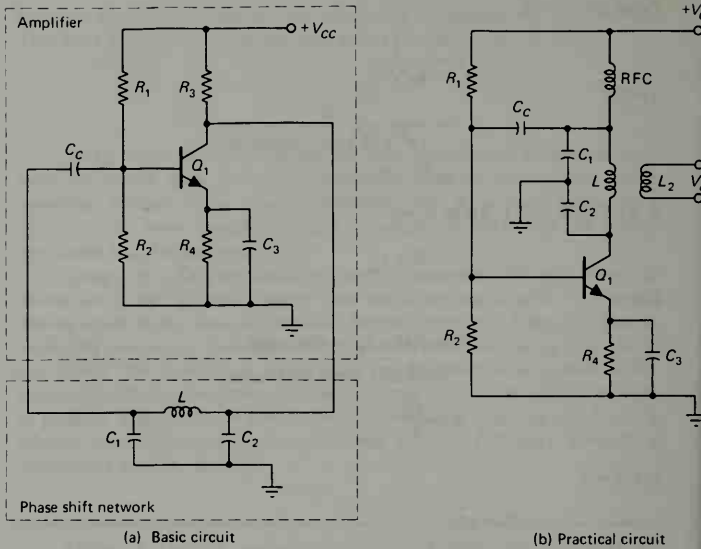
Figure 10-4. Transistor Colpitts oscillator.

Figure 10-5(a) shows the circuit of the Hartley oscillator, and Fig. 10-5(b) illustrates the fact that L_1 and L_2 may be wound on a single core, so that there is mutual inductance between them. In this case the total inductance is given by

$$L_T = L_1 + L_2 + 2M \tag{10-5}$$

where M is the mutual inductance.

As in the case of the Colpitts circuit, the frequency of oscillation is the resonance frequency of the phase-shift network.

$$f = \frac{1}{2\pi\sqrt{CL_T}} \tag{10-6}$$

The attenuation of the phase shift network is

$$\beta = \frac{X_{L1}}{X_{L1} - X_C}$$

Once again, for a 180° phase shift $(X_{L1} - X_C)$ can be shown to equal X_{L2}.
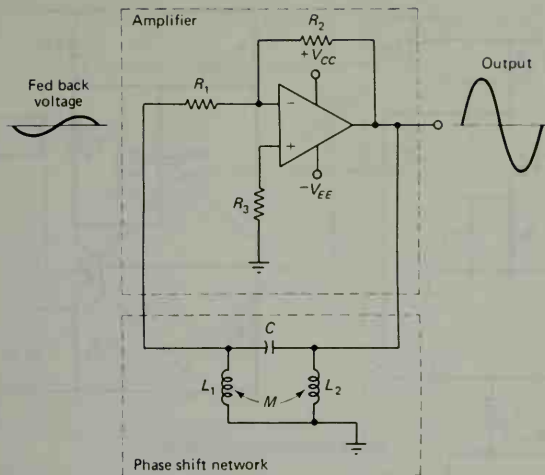
(a) Oscillator circuit
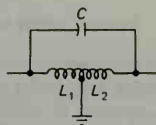
(b) Phase shift network with
L_1 and L_2 wound on a
single core

Figure 10-5. Hartley oscillator using an IC operational amplifier.

For the loop gain to be at least 1,

$$A_v \frac{X_{L1}}{X_{L2}} > 1 \qquad (10\text{-}7)$$

The circuit design procedure for a Hartley oscillator is basically similar to that for the Colpitts circuit.

The circuit of a transistor Hartley oscillator is shown in Fig. 10-6. Figure 10-6(a) gives a basic circuit in which the phase-shift network and amplifier are easily identified as distinct separate stages of the oscillator. In Fig. 10-6(b) a practical circuit is shown. L_1, L_2, and C constitute the phase shift network, and here the inductors are directly connected in place of the
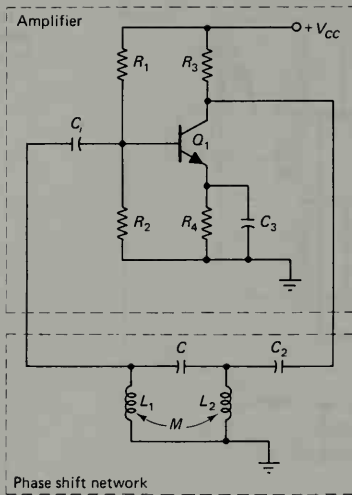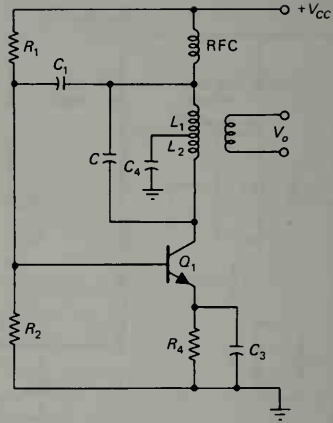
Figure 10-6. Transistor Hartley oscillator.

amplifier load resistance. The radio frequency choke (RFC) passes the direct collector current, but at oscillating frequencies isolates the upper terminal of L_1 from the supply voltage. Capacitor C_1 couples the output of the phase-shift network back to the amplifier input, as in Fig. 10-6(a). Capacitor C_2 in Fig. 10-6 (a) is no longer required in the circuit of Fig. 10-6 (b), because L_2 is directly connected to the amplifier. However, because of the direct connection, the junction of L_1 and L_2 cannot now be directly grounded. Instead, another coupling capacitor C_4 is used.

10-5
Wein
Bridge
Oscillator

      The Wein bridge is an ac bridge in which balance is obtained only at a particular supply frequency. In the *Wein bridge oscillator*, the Wein bridge is used as the feedback network between input and output.

      In Fig. 10-7 (a) the bridge components are R_1, R_2, R_3, R_4, C_1, and C_2. Analysis of the bridge circuit shows that balance is obtained when two equations are fulfilled:

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad (10\text{-}8)$$

$$2\pi f = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \qquad (10\text{-}9)$$

240
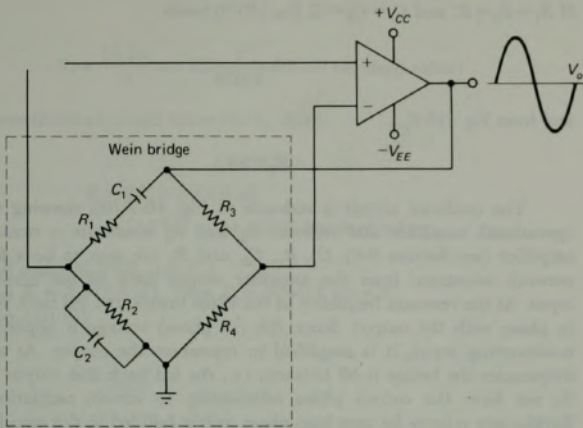
(a) Wein bridge oscillator circuit
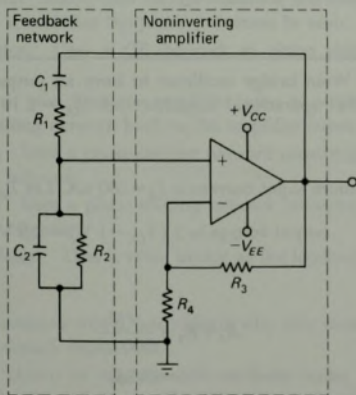
(b) Showing that the circuit consists
of a feedback network and a
noninverting amplifier

Figure 10-7. Wein bridge oscillator.

If $R_1 = R_2 = R$, and $C_1 = C_2 = C$, Eq. (10-9) yields

$$f = \frac{1}{2\pi CR} \qquad (10\text{-}10)$$

and from Eq. (10-8),

$$R_3 = 2R_4 \qquad (10\text{-}11)$$

The oscillator circuit is redrawn in Fig. 10-7 (b), showing that the operational amplifier and resistors R_3 and R_4 constitute a noninverting amplifier (see Section 9-6). C_1, R_1, C_2, and R_2 are seen to be a feedback network connected from the amplifier output back to the noninverting input. At the resonant frequency of the Wein bridge, the fed back voltage is in phase with the output. Since this (in phase) voltage is applied to the noninverting input, it is amplified to reproduce the output. At all other frequencies the bridge is off balance; i.e., the fed back and output voltages do not have the correct phase relationship to sustain oscillations. The Barkhausen criteria for zero loop phase shift is fulfilled in this circuit by the amplifier and feedback network each having zero phase shift.

The design of a Wein bridge oscillator can be approached by first selecting a current level for each bridge arm. This should be much larger than the input bias current to the operational amplifier. $R_3 + R_4$ can then be calculated using an estimated output voltage, and the other circuit components can be determined using Eqs. (10-10) and (10-11).

Example 10-3

Design a Wein bridge oscillator to have an output frequency of 10 kHz. Use a μA741 operational amplifier with $V_{CC} = \pm 10$ V.

solution

Amplifier maximum input current is $I_B = 500$ nA. Let $I_{4(\text{through } R4)} = 500$ μA

$$\text{output voltage} \approx \pm (V_{CC} - 1 \text{ V}) = \pm 9 \text{ V}$$

Then

$$R_3 + R_4 = \frac{9 \text{ V}}{500 \text{ } \mu\text{A}}$$
$$= 18 \text{ k}\Omega$$

Use Eq. (10-11): $R_3 = 2R_4$

$$3R_4 = 18 \text{ k}\Omega$$

and

$$R_4 = \frac{18 \text{ k}\Omega}{3} = 6 \text{ k}\Omega \quad \text{(use 5.6-k}\Omega \text{ standard value)}$$

The lower-than-calculated value for R_4 makes

$$I_4 > 500 \text{ }\mu\text{A}$$
$$R_3 = 2R_4 = 2 \times 5.6 \text{ k}\Omega$$
$$= 11.2 \text{ k}\Omega \quad \text{(use 12-k}\Omega \text{ standard value)}$$

This will make $R_3 > 2R_4$ (and $A_v > 3$).
Let $R_2 = R_4 = 5.6 \text{ k}\Omega$. Then $R_1 = R_2 = 5.6 \text{ k}\Omega = R$.
From Eq. (10-10),

$$C = \frac{1}{2\pi f R}$$

$$C_1 = C_2 = C = \frac{1}{2\pi \times 10 \text{ kHz} \times 5.6 \text{ k}\Omega}$$
$$= 2842 \text{ pF} \quad \text{(use 2700-pF standard capacitor value)}$$

Barkhausen criteria. States that for an oscillator the loop gain must be greater than 1, and that the phase shift must be zero.

Phase-shift oscillator. Uses a CR network to phase shift the amplifier output.

Loop gain. Circuit gain from the amplifier input to output, and through the phase-shifting network back to the amplifier input.

Colpitts oscillator. Uses a phase-shifting network consisting of two capacitors and one inductor.

Hartley oscillator. Uses a phase-shifting network consisting of two inductors and one capacitor.

Wein bridge oscillator. Uses a Wein bridge as the feedback network.

Glossary of Important Terms

10-1. State the *Barkhausen criteria*, and explain why they must be fulfilled for a circuit to sustain oscillations.

10-2. Sketch the circuit of a phase-shift oscillator using an operational amplifier. Briefly explain how the circuit operates and how it fulfills the Barkhausen criteria.

10-3. Sketch the circuit of a phase-shift oscillator using a transistor amplifier circuit. Briefly explain how the circuit operates, and state the equation for oscillating frequency.

Review Questions

10-4. Repeat Question 10-2 for a Colpitts oscillator.

10-5. Repeat Question 10-3 for a Colpitts oscillator.

10-6. Repeat Question 10-2 for a Hartley oscillator.

10-7. Repeat Question 10-3 for a Hartley oscillator.

10-8. Repeat Question 10-2 for a Wein bridge oscillator.

Problems

10-1. Design a phase-shift oscillator to have an output frequency of approximately 3 kHz. Use a μA741 operational amplifier with $V_{CC} = \pm 12$ V.

10-2. A phase-shift oscillator is to use three 0.05-μF capacitors and a μA741 operational amplifier with $V_{CC} = \pm 9$ V. Design the circuit to have $f = 7$ kHz.

10-3. Redesign the circuit of Problem 10-1 to use a single-stage transistor amplifier. Use a 2N3904 transistor with $V_{CC} = 15$ V.

10-4. Repeat Problem 10-1 for a Colpitts oscillator.

10-5. A Colpitts oscillator is to be designed to have $f \approx 5.5$ kHz. An inductor with $L = 20$ mH and a μA741 operational amplifier are to be employed. Using $V_{CC} = \pm 18$ V, complete the circuit design.

10-6. Design a Wein bridge oscillator using a μA741 operational amplifier with $V_{CC} = \pm 14$ V. The output frequency is to be 15 kHz.

10-7. A Wein bridge oscillator is to have an output frequency of 9 kHz. Two 5000-pF capacitors and a μA741 operational amplifier are to be employed. Complete the circuit design using $V_{CC} = \pm 12$ V.

Zener Diodes

When an ordinary silicon junction diode is reverse biased, normally only a very small reverse saturation current (I_S) flows. If the reverse voltage is increased sufficiently, the junction *breaks down* and a large reverse current flows. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown condition. When the reverse bias is reduced below the breakdown voltage, the current returns to its normal I_S level. It is found that for a suitably designed diode, the breakdown voltage is a very stable quantity over a wide range of reverse currents. This quality gives the *breakdown diode* many useful applications as a voltage reference source.

There are two mechanisms by which breakdown can occur at a reverse-biased *pn*-junction. These are *Zener breakdown* and *avalanche breakdown*. Either of the two may occur independently, or they may both occur at once.

Zener breakdown usually occurs in silicon *pn*-junctions at reverse biases of less than 5 V. Under the influence of a high-intensity electric field,

245
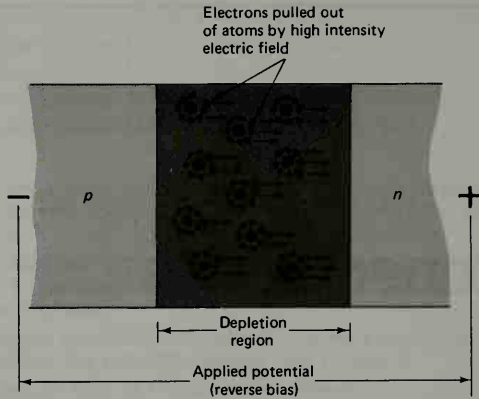
Figure 11-1. Ionization by electric field; Zener breakdown.

large numbers of electrons within the depletion region break the covalent bonds with their atoms (see Fig. 11-1). This is *ionization by an electric field*, and when it occurs the presence of the free electrons converts the depletion region from a material which is almost an insulator into one which is effectively a conductor. Thus, a large (reverse) current can be made to flow across the junction.

Since

$$\text{Electric field strength} = \frac{\text{reverse voltage}}{\text{depletion region width}}$$

a small reverse voltage can produce a very high intensity electric field within a narrow depletion region. Thus, the narrower the depletion region, the smaller the Zener breakdown voltage. The actual intensity of the electric field strength that produces Zener breakdown is estimated as 3×10^5 V/cm.

With lightly doped semiconductor material, some depletion regions are too wide for Zener breakdown to occur even with a 5-V reverse bias. With sufficient increase in reverse bias, Zener breakdown occurs even for relatively wide depletion regions. However, when the reverse bias exceeds approximately 5 V, another form of reverse breakdown occurs before the field intensity becomes great enough to cause electrons to break their bonds.

Recall that the reverse saturation current I_S which flows across a reverse-biased *pn*-junction is made up of minority charge carriers. The velocity of the minority carriers is directly proportional to the applied bias voltage. Hence, when the reverse-bias voltage is increased, the velocity of the minority charge carriers is increased, and consequently their energy content is also increased. When these high-energy charge carriers strike atoms within
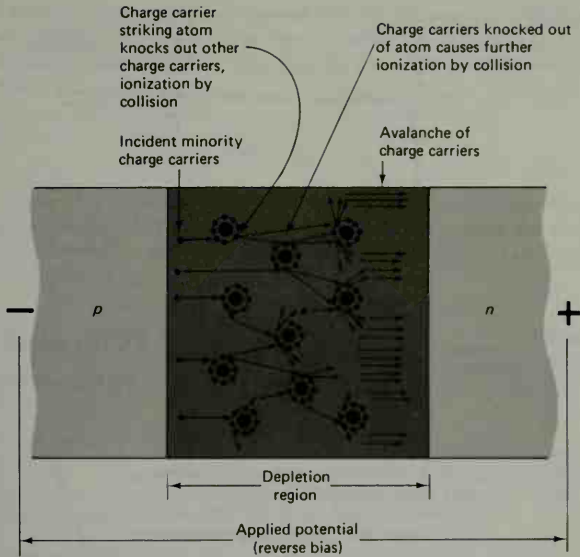
Figure 11-2. Ionization by collision; avalanche breakdown.

the depletion region, they cause other charge carriers to break away from their atoms and join the flow of current across the junction (Fig. 11-2). This effect is termed *ionization by collision*. The additional charge carriers generated in this way are also accelerated to a high energy state and can cause further ionization by collision. The number of charge carriers *avalanches* and the result is *avalanche breakdown*. As in the case of Zener breakdown, the depletion region material is converted from a near insulator into a conductor. Here again a large (reverse) current can be made to flow across the junction.

A typical Zener diode characteristic is shown in Fig. 11-3. The forward characteristic is simply that of an ordinary forward-biased junction diode. The important points on the reverse characteristic are

V_Z = *Zener breakdown voltage*

I_{ZT} = *test current* at which V_Z is measured

I_{ZK} = *Zener current near the knee* of the characteristic; the minimum Zener current necessary to sustain breakdown

I_{ZM} = *maximum Zener current*; limited by the maximum power dissipation

11-3
Zener
Diode
Characteristic
and
Parameters
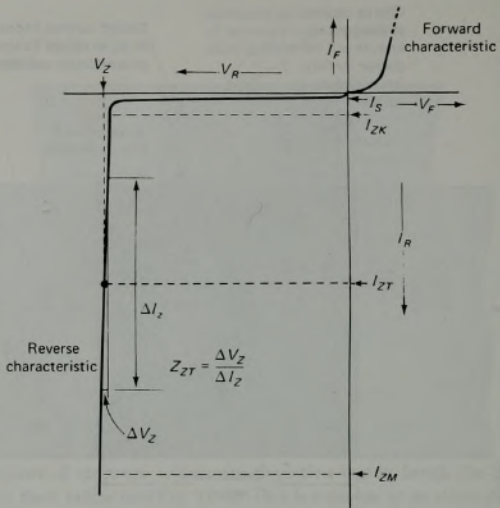
Figure 11-3. Zener diode characteristics.
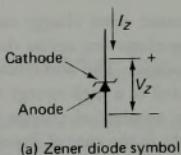
(a) Zener diode symbol
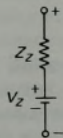
(b) Zener diode equivalent circuit

Figure 11-4. Zener diode symbol and equivalent circuit.

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A very important parameter derived from the characteristic is the *Zener dynamic impedance* (Z_Z), which defines how V_Z varies with change in I_Z. Z_Z is determined by measuring the reciprocal of the slope of the characteristic, as shown in Fig. 11-3:

$$Z_{ZT} = \frac{\Delta V_Z}{\Delta I_Z}$$

Figure 11-4 shows the Zener diode circuit symbol and the equivalent circuit for the device. The equivalent circuit, which represents the diode only in its breakdown condition, is simply a battery of voltage V_Z in series with a resistance of Z_Z.

1N746 thru 1N759

1N4370 thru 1N4372

400 mW
2.4 — 12 V

CASE 51
(DO-7)

Hermetically sealed, all-glass case with all external surfaces corrosion resistant. Cathode end, indicated by color band, will be positive with respect to anode end when operated in the zener region.

MAXIMUM RATINGS

Junction and Storage Temperature: -65°C to +175°C
D-C Power Dissipation: 400 Milliwatts at 50°C Ambient (Derate 3.2 mW/°C Above 50° Ambient)

TOLERANCE DESIGNATION

The type numbers shown have tolerance designations as follows:
1N4370 series: ± 10%, suffix A for ± 5% units.
1N746 series: ± 10%, suffix A for ± 5% units.

ELECTRICAL CHARACTERISTICS (T$_\Lambda$ = 25°C unless otherwise noted)

TYPE NUMBER	NOMINAL ZENER VOLTAGE V_z @ I_{zt} VOLTS	TEST CURRENT I_{zt} mA	MAXIMUM ZENER IMPEDANCE Z_{zt} @ I_{zt} Ohms	MAXIMUM DC ZENER CURRENT I_{zm} mA	REVERSE LEAKAGE CURRENT	
					$T_j = 25°C$ I_R @ $V_R = 1$ V μA	$T_j = 150°C$ I_R @ $V_R = 1$ V μA
1N4370	2.4	20	30	130	100	200
1N4371	2.7	20	30	125	75	150
1N4372	3.0	20	29	120	50	100
1N746	3.3	20	28	110	10	30
1N747	3.6	20	24	100	10	30
1N748	3.9	20	23	95	10	30
1N749	4.3	20	22	85	2	30
1N750	4.7	20	19	75	2	30
1N751	5.1	20	17	70	1	20
1N752	5.6	20	11	65	1	20
1N753	6.2	20	7	60	0.1	20
1N754	6.8	20	5	55	0.1	20
1N755	7.5	20	6	50	0.1	20
1N756	8.2	20	8	45	0.1	20
1N757	9.1	20	10	40	0.1	30
1N758	10.0	20	17	35	0.1	30
1N759	12.0	20	30	30	0.1	20

Figure 11-5. Zener diode specifications. (Courtesy of Motorola, Inc.)

250
Zener
Diodes

1N**3993** thru 1N**4000**

10 W
3.9 — 7.5 V

CASE 56
(DO-4)

Low-voltage, alloy-junction zener diodes in hermetically sealed package with cathode connected to case. Supplied with mounting hardware.

MAXIMUM RATINGS

Junction and Storage Temperature: -65°C to +175°C.
D-C Power Dissipation: 10 Watts.(Derate 83.3 mW/°C above 55°C).

The type numbers shown in the table have a standard tolerance on the nominal zener voltage of ±10%. A standard tolerance of ±5% on individual units is also available and is indicated by suffixing "A" to the standard type number.

ELECTRICAL CHARACTERISTICS (T$_s$ = 30°C ± 3, V$_F$ = 1.5 max @ I$_F$ = 2 amp for all units)

Type No.	Nominal Zener Voltage V$_z$ @ I$_{zr}$ Volts	Test Current I$_{zr}$ mA	Max Zener Impedance		Max DC Zener Current I$_{zm}$ mA	REVERSE LEAKAGE CURRENT	
			Z$_{zr}$ @ I$_{zr}$ Ohms	Z$_{zx}$ @ I$_{zx}$ = 1.0 mA Ohms		I$_L$ (μA)	V$_s$ Volts
1N3993	3.9	640	2	400	2380	100	0.5
1N3994	4.3	580	1.5	400	2130	100	0.5
1N3995	4.7	530	1.2	500	1940	50	1
1N3996	5.1	490	1.1	550	1780	10	1
1N3997	5.6	445	1.0	800	1620	10	1
1N3998	6.2	405	1.1	750	1460	10	2
1N3999	6.8	370	1.2	500	1330	10	2
1N4000	7.5	335	1.3	250	1210	10	3

Figure 11-5. *(cont.)*

Referring to the Zener diode data sheets (Fig. 11-5), it is seen that for low-power devices (IN746 to IN759) typical values of Z_{ZT} range from 5 to 30 Ω. For high-power devices(IN3993 to IN4000), the range of Z_{ZT} is only 1 to 2 Ω. Note that Z_{ZT} is measured at the test current I_{ZT} which is much greater than the current near the knee. The Zener impedence near the knee of the characteristic (Z_{ZK}) is much larger than Z_{ZT}.

Referring again to the data sheets, note that a Zener voltage tolerance of ±5% or ±10% is specified. This means, for example, that the actual Zener voltage of a IN753 is 6.2 V±10%. The value of V_Z will remain stable at whatever voltage it happens to be within its range.

The maximum power dissipation for each type of device is listed on the data sheet for a specified maximum temperature. At higher temperatures the maximum power dissipation must be derated exactly as for transistors (see Section 8-3).
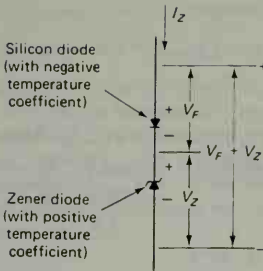
Figure 11-6. Construction of a compensated reference diode.

For Zener breakdown ($V_Z < 5$ V), the *temperature coefficient* (α_Z) of the breakdown voltage is *negative*. For a given value of I_Z, V_Z decreases slightly when the temperature is increased. This is because, as the temperature increases, the valence electrons of the atoms within the depletion region are raised to a higher energy level, and are therefore more easily extracted from their atoms.

In avalanche breakdown, relatively wide depletion regions are involved. Consequently, charge carriers crossing the depletion region experience many collisions with atoms, and as temperature increases the atoms vibrate and impede the progress of the charge carriers. Therefore, to maintain a given current, V_Z must increase slightly when the temperature increases. This effect gives avalanche breakdown a *positive temperature coefficient*.

To produce reference voltages with very small temperature coefficients, compensated reference diodes are constructed as shown in Fig. 11-6. A forward-biased silicon diode is connected in series with a breakdown diode which has a positive temperature coefficient. The negative temperature coefficient of the silicon diode partially cancels the breakdown diode's positive temperature coefficient. With this arrangement, temperature coefficients of better than 0.0005%/° C are possible.

A breakdown diode has $V_Z = 6.2$ V at 25° C, and $\alpha_Z = +0.02\%/°$ C. A silicon diode with $V_F = 0.7$ V and a temperature coefficient of -1.8 mV/° C is connected in series with the breakdown diode. Find the new value of reference voltage and the temperature coefficient of the combination. Also calculate the new value of V_{ref} at a temperature of 50° C.

Example 11-1

solution

$$\alpha_Z = +0.02\% \text{ of } V_Z \text{ for each}°C \text{ temperature change}$$

$$V_Z \text{ change} = +\frac{6.2 \times 0.02}{100} \text{ V/}° \text{ C} = +1.24 \text{ mV/}° \text{ C}$$

Combined V_Z and V_F change is

$$(+1.24 - 1.8) \text{ mV}/°\text{ C} = -0.56 \text{ mV}/°\text{ C}$$

New value of V_{ref} is

$$V_Z + V_F = 6.2 \text{ V} + 0.7 \text{ V} = 6.9 \text{ V}$$

new temperature coefficient $= -0.56 \text{ mV}/°\text{ C}$

$$= \frac{-0.00056 \times 100}{6.9} \%/°\text{ C} = -0.008\%/°\text{ C}$$

The value of V_{ref} at $50°$ C

$$= 6.9 \text{ V} - [0.56 \text{ mV} \times (50°\text{ C} - 25°\text{ C})]$$
$$= 6.9 \text{ V} - 14 \text{ mV} = 6.886 \text{ V}.$$

11-5
Zener
Diode
Voltage
Regulator

11-5.1
Regulator
Design

Figure 11-7 shows the simplest possible form of voltage regulator circuit, a Zener diode connected in series with a resistor R_S. The resistor limits the total current flowing to the diode and the load. The load is connected across the diode, so that

$$V_O = V_Z$$
$$V_R = V_S - V_Z$$
$$I_R = \frac{V_S - V_Z}{R_S}$$

Apart from small variations due to ΔV_Z, I_R will remain constant. Since $I_R = I_Z + I_L$

$$I_Z = I_R - I_L$$
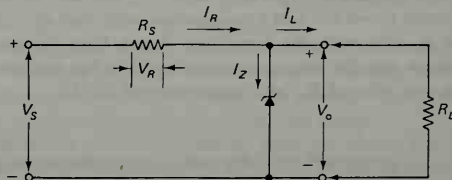
Figure 11-7. Simple Zener diode voltage regulator.

When the load is not connected, $I_L = 0$:

253
Zener
Diode
Voltage
Regulator

$$I_Z = I_R = I_{Z(max)}$$

Therefore, the Zener diode must be capable of passing all the current I_R. Also, for the diode to remain in breakdown, I_Z must not be permitted to fall below a minimum level $I_{Z(min)}$. The maximum value of load current is $I_{L(max)} = I_R - I_{Z(min)}$. $I_{Z(max)}$ can be I_{ZM}, the maximum value of I_Z as limited by maximum power dissipation. $I_{Z(min)}$ could be the value of I_Z near the knee of the characteristic, I_{ZK}. However, Z_Z becomes very large at I_{ZK}, so it is best to keep $I_{Z(min)}$ much larger than I_{ZK}.

Design a simple Zener regulator circuit to supply approximately 6 V from a 15-V source. Calculate the minimum value of load resistor that may be connected across the output terminals. The circuit is to operate at an ambient temperature of 25° C.

Example 11-2

solution

Consulting the Zener diode data sheets (Fig. 11-5), it is seen that a 1N753 has a nominal V_Z of 6.2 V. Therefore, using a 1N753, the voltage across R_S (Fig. 11-7) is

$$V_R = V_S - V_O = 15 \text{ V} - 6.2 \text{ V} = 8.8 \text{ V}$$

From the data sheet,

$$I_{ZM} = 60 \text{ mA}$$
$$V_R = 8.8 \text{ V}$$
$$R_S = \frac{V_R}{I_R} = \frac{8.8 \text{ V}}{60 \text{ mA}} \approx 147 \text{ }\Omega$$

Power dissipation is $R_S = V_R \times I_R = 8.8 \text{ V} \times 60 \text{ mA} = 0.53 \text{ W}$. R_S should be a 1W resistor.

I_{ZK} is not specified for the 1N753, but a typical value of I_{ZK} is 1 mA. $I_{Z(min)}$ should be much greater than I_{ZK}.

Thus, make $I_{Z(min)} = 10 \times I_{ZK} = 10 \text{ mA}$.

$$I_{L(max)} = I_R - I_{Z(min)}$$
$$= 60 \text{ mA} - 10 \text{ mA}$$
$$= 50 \text{ mA}$$

The minimum value of R_L is $R_{L(min)}$, where

$$R_{L(min)} = \frac{V_Z}{I_{L(max)}} = \frac{6.2 \text{ V}}{50 \text{ mA}} \approx 124 \text{ }\Omega$$

Apart from output voltage and maximum load current, the performance of a voltage regulator may be specified in terms of the *stabilization ratio* (S_V) and the *output impedance* (Z_O).

S_V is a measure of how the output voltage varies with changes in input voltage.

$$S_V = \frac{\Delta V_O}{\Delta V_S}$$

The ideal value of S_V is zero.

Z_O defines how V_O varies with variations in load current I_L.

$$Z_O = \frac{\Delta V_O}{\Delta I_L}$$

To calculate S_V and Z_O, consider the ac equivalent circuit for the regulator (Fig. 11-8). The equivalent circuit is drawn simply by replacing the diode with its Zener dynamic impedance (Z_Z).

From Fig. 11-8, when V_S changes by ΔV_S, V_O changes by ΔV_O.

$$\Delta V_O = \frac{Z_Z}{R_S + Z_Z} \times \Delta V_S \tag{11-1}$$

and

$$S_V = \frac{\Delta V_O}{\Delta V_S} = \frac{Z_Z}{R_S + Z_Z} \tag{11-2}$$

The output impedance (also from Fig. 11-8) of the regulator is the impedance "seen" when looking into the output terminals. Since the source resistance of V_S is likely to be much smaller than R_S,

$$Z_O \approx Z_Z \| R_S = \frac{Z_Z \times R_S}{Z_Z + R_S} \tag{11-3}$$
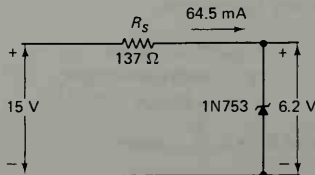
Figure 11-8. AC equivalent circuit for Zener diode voltage regulator.

Example 11-3

Calculate the values of stabilization ratio and output impedance for the regulator designed in Example 11-2.

solution

For the 1N753 diode, $Z_Z = 7\ \Omega$ (Fig. 11-5).
From Eq. (11-2),

$$S_V = \frac{7\ \Omega}{147\ \Omega + 7\ \Omega} = 0.045$$

This means, for example, that if V_S increases or decreases by 1 V, V_O change would be

$$\Delta V_O = S_V \times \Delta V_S = 45\ \text{mV}$$

From Eq. (11-3),

$$Z_O = \frac{7 \times 147}{7 + 147}\ \Omega = 6.7\ \Omega$$

Therefore, when I_L varies by ± 10 mA, for example, V_O will change by

$$\Delta V_O = Z_O \times \Delta I_L = \pm 67\ \text{mV}$$

The regulator performance can also be defined in terms of the *line regulation* and the *load regulation*. The line regulation is just another way of expressing the voltage stabilization ratio, and the load regulation is another method of stating the circuit output impedance.

For a given V_S change (e.g., 10%), the resultant change in V_O is expressed as a percentage of the normal V_O level:

$$line\ regulation = \frac{(\Delta V_O\ \text{for a given}\ \Delta V_S) \times 100\%}{V_O} \qquad (11\text{-}4)$$

For a given change in load current (usually from *no load* to *full load*), ΔV_O is expressed as a percentage of the normal V_O level:

$$load\ regulation = \frac{(\Delta V_O\ \text{for a given}\ \Delta I_L) \times 100\%}{V_O} \qquad (11\text{-}5)$$

Example 11-4

For the regulator referred to in Examples 11-2 and 11-3, determine the line regulation for a 10% change in input voltage. Also determine the load regulation for a load current change from no load to full load.

255

solution

$$\Delta V_S = 10\% \text{ of } V_S = 10\% \text{ of } 15 \text{ V}$$
$$= 1.5 \text{ V}$$
$$\Delta V_O = S_V \times \Delta V_S = 0.045 \times 1.5 \text{ V}$$
$$= 67.5 \text{ mV}$$

From Eq. (11-4),

$$\text{line regulation} = \frac{\Delta V_O}{V_O} \times 100\%$$
$$= \frac{67.5 \text{ mV}}{6.2 \text{ V}} \times 100\%$$
$$\simeq 1.1\%$$

Full load current

$$I_L = 50 \text{ mA}$$
$$\Delta I_L = 50 \text{ mA} - 0 = 50 \text{ mA}$$
$$\Delta V_O = \Delta I_L \times Z_O = 50 \text{ mA} \times 6.7 \text{ }\Omega = 335 \text{ mV}$$

From Eq. (11-5),

$$\text{load regulation} = \frac{\Delta V_O}{V_O} \times 100\%$$
$$= \frac{335 \text{ mV}}{6.2 \text{ V}} \times 100\%$$
$$= 5.4\%$$

11-5.3
Two-Stage
Regulator

To improve the performance of the regulator, designed in Example 11-2, an additional stage may be added giving the circuit shown in Fig. 11-9. With two-stage regulation, the stabilization ratio becomes

$$S_V = \frac{Z_{Z1}}{R_{S1} + Z_{Z1}} \times \frac{Z_{Z2}}{R_{S2} + Z_{Z2}}$$
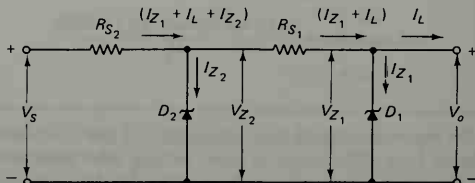
Figure 11-9. Two-stage Zener diode voltage regulator.

(a) Emitter follower voltage regulator

(b) Usual circuit schematic for series regulator
(or emitter follower voltage regulator)
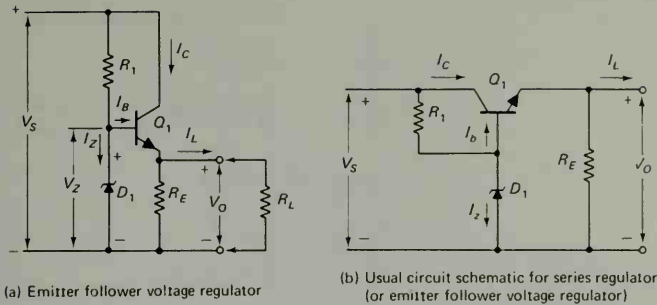
Figure 11-10. Emitter follower or series voltage regulator.

This affords a significant improvement over the stabilization ratio for a single-stage regulator. The regulator output impedance, however, is *not* improved. Z_O remains approximately equal to Z_{Z1} in parallel with R_{S1}.

When a low-power Zener diode is employed in the simple regulator circuit described in Section 11-5, the load current is limited to low values. A high-power Zener used in such a circuit can supply the required load current, but much power is wasted when the load is light. The *emitter follower regulator* shown in Fig. 11-10 is an improvement on the simple regulator circuit, because it draws a large current from the supply only when it is required by the load. In Fig. 11-10(a), the circuit is drawn in the form of the *common collector amplifier* (emitter follower) discussed in Chapter 6. In Fig. 11-10(b), the circuit is shown in a form in which it is usually referred to as a *series regulator*.

V_O from the series regulator is $(V_Z - V_{BE})$, and $I_{L(max)}$ can be the maximum I_E that Q_1 is capable of passing. For a 2N3055 transistor (specification in Fig. 8-2), I_L could approach 15 A. When I_L is zero, the current drawn from the supply is approximately $[I_Z + I_{C(min)}]$. The emitter follower voltage regulator is, therefore, much more efficient than a simple Zener regulator.

11-6
Regulator
with
Reference
Diode

11-7
Other
Zener
Diode
Applications

11-7.1
*Constant
Current
Circuit*

The constant voltage characteristic of a Zener diode can be converted into a constant current characteristic. The constant current circuit is shown in Fig. 11-11. The voltage across R_E is $V_Z - V_{BE}$.

$$I_E = \frac{V_Z - V_{BE}}{R_E} \qquad (11-6)$$
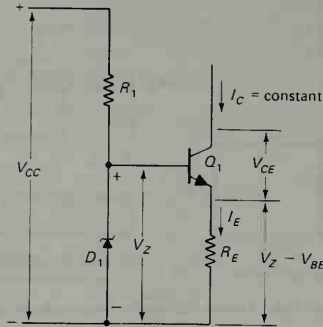
Figure 11-11. Constant current circuit.

Since V_Z and V_{BE} are normally constant quantities, I_E also remains constant, and $I_C \approx I_E$. Therefore, I_C remains substantially constant no matter what the value of the collector voltage.

The only restriction on the circuit is that V_{CE} must remain large enough to keep Q_1 operating in its active region; i.e., Q_1 must not become saturated. The constant current circuit is widely applied.

Example 11-5

The circuit in Fig. 11-11 uses a 1N755 Zener diode, and has $V_{CC} = 12$ V, $R_1 = 220$ Ω, $R_E = 680$ Ω. If Q_1 is a silicon transistor, calculate the transistor collector current and the power dissipation in the Zener diode. Also determine the new value of R_E to give $I_C = 2.5$ mA.

solution

From the Zener diode specifications in Fig. 11-5, the 1N755 has $V_Z = 7.5$ V. From Eq. (11-6),

$$I_E = \frac{V_Z - V_{BE}}{R_E} = \frac{7.5 \text{ V} - 0.7 \text{ V}}{680 \text{ Ω}} = 10 \text{ mA}$$

and

$$I_C \approx I_E = 10 \text{ mA}$$

Neglecting I_B

$$I_Z = \frac{V_{CC} - V_Z}{R_1} = \frac{12 \text{ V} - 7.5 \text{ V}}{220 \text{ Ω}} = 20.45 \text{ mA}$$

Power dissipation in D_1 is

$$P_D = V_Z \times I_Z = 7.5 \text{ V} \times 20.45 \text{ mA} = 153 \text{ mW}$$

For $I_C = 2.5$ mA, $I_E \simeq 2.5$ mA.
From Eq. (11-6),

$$2.5 \text{ mA} = \frac{7.5 \text{ V} - 0.7 \text{ V}}{R_E}$$

$$R_E = \frac{7.5 \text{ V} - 0.7 \text{ V}}{2.5 \text{ mA}} \simeq 2.7 \text{ k}\Omega$$

Zener diodes are used extensively to protect other devices from excessive voltages. In the circuit of Fig. 11-12, for example, the Zener diodes do not operate while the peak input voltage remains below V_Z. When the input peak exceeds V_Z, one diode goes into breakdown while the other is forward biased. Thus, the peak output is limited to $(V_Z + V_F)$.

11-7.2
*Over
Voltage
Protection*

Zener breakdown. Reverse-biased *pn*-junction breakdown produced by high-intensity electric field.

Avalanche breakdown. Reverse-biased *pn*-junction breakdown produced by collision of high-energy charge carriers with atoms.

Ionization by electric field. Removal of charge carriers from atoms by effect of high-intensity electric field.

Ionization by collision. Removal of charge carriers from atoms by other charge carriers colliding with the atoms.

V_Z. Zener breakdown voltage.

I_Z. Test current at V_Z.

I_{ZK}. Zener current near knee of characteristic.

I_{ZM}. Maximum Zener current.

*Glossary of
Important
Terms*
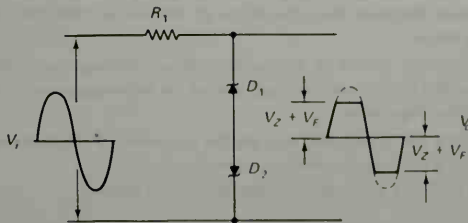
Figure 11-12. Zener diode overvoltage protection circuit.

Z_Z.   Zener dynamic impedance.

Z_{ZT}.   Zener dynamic impedance at I_{ZT}.

Z_{ZK}.   Zener dynamic impedance near knee of characteristic.

α_Z.   Temperature coefficient of V_Z.

Compensated reference diode.   Combination of Zener diode and forward-biased diode to give improved temperature coefficient.

S_V.   Voltage stabilization ratio of regulator.

Z_O.   Output impedance of regulator.

Emitter follower regulator.   Combination of transistor and Zener diode to give improved efficiency regulator circuit.

Series regulator.   Same as *emitter follower regulator*.

Constant current circuit.   Combination of transistor and Zener diode to give constant collector current.

Overvoltage protection circuit.   Zener diode voltage limiter circuit.

Review
Questions

11-1.   Name and explain the two types of breakdown that can occur at a reverse-biased *pn*-junction. Also state the important differences between the performance of breakdown diodes in which different breakdown mechanisms are involved.

11-2.   Sketch the characteristic of a Zener diode. Define and show how the following quantities may be determined from the characteristic: V_Z, I_{ZK}, I_{ZM}, and Z_Z.

11-3.   Sketch the schematic symbol for a Zener diode and show the polarity of V_Z and I_Z. Also sketch and explain the equivalent circuit for a Zener diode.

11-4.   Draw a sketch to show how a compensated reference diode is constructed, and explain how the temperature coefficient is improved.

11-5.   Sketch the circuit of a simple Zener diode voltage regulator. Briefly explain how the circuit operates.

11-6.   Sketch the ac equivalent circuit for the simple Zener diode voltage regulator. Derive the equations for S_V, Z_O, line regulation, and load regulation.

11-7.   Sketch the circuit of a two-stage Zener diode voltage regulator circuit. Explain the advantages of the circuit over the single-stage regulator.

11-8.   Sketch the circuit of an emitter follower voltage regulator. Explain how the circuit operates and discuss its advantages over Zener diode voltage regulators.

11-9.   Sketch the circuit and explain the operation of the following:
(a) A Zener diode constant current circuit.
(b) A Zener diode overvoltage protection circuit.

11-1. A Zener diode has $V_Z = 8.2$ V at 25° C and $\alpha_Z = +0.05\%/°$ C. A silicon diode, which has $V_F = 0.6$ V and a temperature coefficient of -2.2 mV/° C, is to be used with the Zener to construct a compensated reference diode. Calculate the value of V_{ref} at 25° C and at 100° C. Also calculate the value of α_Z for the compensated reference diode.

11-2. Design a simple Zener voltage regulator to supply approximately 5 V from a 12-V source. Calculate the minimum value of load resistance that may be connected across the output terminals if the circuit operates at an ambient temperature of 55° C. Also calculate the values of S_V and Z_O for the regulator.

11-3. Assuming a 10% input voltage change, determine the line regulation of the circuit designed in Problem 11-2. Also calculate the load regulation for a load current change from no load to full load.

11-4. A Zener diode voltage regulator is to have an output of approximately 9 V. The available supply is 25 V, and the load current will not exceed 1 mA. Design a suitable circuit, and calculate the output voltage change when the input drops by 5 V and the load changes from zero to 1 mA at the same time.

11-5. A constant current circuit uses a 1N749 Zener diode in series with a 270-Ω resistance. The supply to the Zener circuit is 10 V, and the transistor is a silicon device. If $R_E = 330$ Ω, calculate the value of the constant collector current. Also determine the new value of R_E to make $I_C \simeq 5.3$ mA.

11-6. The transistor in a constant current circuit is to have a collector current of approximately 2 mA. Design a suitable circuit using a 20-V supply, and calculate the actual collector current level.

Field Effect Transistors

Field effect transistors (FET) are voltage-operated devices. Unlike bipolar transistors, FET's require virtually no input current, and this gives them an extremely high input resistance. There are two major categories of field effect transistors, junction FET's and insulated gate FET's. These are further subdivided into *p*-channel and *n*-channel devices.

The operating principle of the *n-channel junction field effect transistor* (JFET) is illustrated by the block representation in Fig. 12-1. A piece of *n*-type material, referred to as the *channel*, has two smaller pieces of *p*-type attached to its sides, forming *pn*-junctions. The channel's ends are designated the *drain* and the *source*, and the two pieces of *p*-type material are connected together and their terminal is called the *gate*. With the gate terminal not connected, and a potential applied (positive at the drain, negative at the source), a *drain current* (I_D) flows as shown in Fig. 12-1(a). When the gate is biased negative with respect to the source [Fig. 12-1(b)], the *pn*-junctions are reverse biased and depletion regions are formed. The channel is more lightly
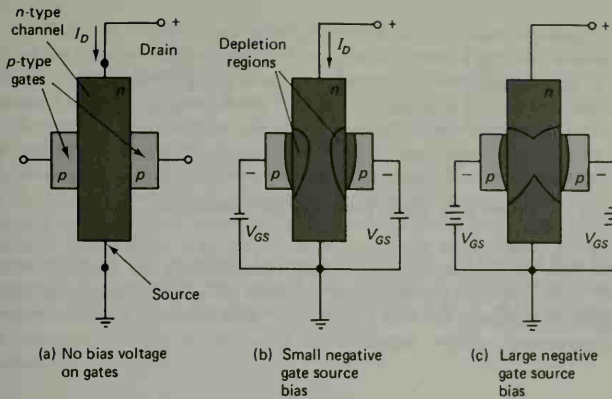
Figure 12-1. Principle of the n-channel JFET.

doped than the p-type gate blocks, so the depletion regions penetrate deeply into the channel. Since a depletion region is a region depleted of charge carriers, it behaves as an insulator. The result is that the channel is narrowed, its resistance is increased, and I_D is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center [Fig. 12-1(c)], and I_D is cut off completely.

When a signal is applied to the gate, the reverse voltage on the junctions is increased as the signal voltage goes negative and decreased as it goes positive. Consequently, as the signal goes negative the depletion regions are widened, the channel resistance is increased, and the drain current reduced. Also, as the signal goes positive the depletion regions recede, the channel resistance is reduced, and the drain current is increased. As will be seen in Chapter 20, the n-channel JFET is comparable to a triode vacuum tube. The drain and source perform the same functions as the plate and cathode, respectively; and, like the grid of a triode, the FET gate controls drain current. As is also the case with a grid, gate current is to be avoided, so the gate–channel junctions are normally never forward biased.

The name *field effect device* comes from the fact that the depletion regions in the channel are the result of the electric field at the reverse-biased gate–channel junctions. The term *unipolar transistor* is sometimes applied to an FET, because unlike a bipolar transistor the drain current consists of only one type of charge carrier, electrons in the n-channel FET and holes in the p-channel device (Section 12-4).

The symbol for the n-channel JFET is shown in Fig. 12-2. As for other types of transistors, the arrowhead always points from p to n. For an n-channel device, the arrowhead points from the p-type gate toward the n-type channel. Some manufacturers use the symbol with the gate terminal opposite the source [Fig. 12-2(a)]; others show the gate centralized between
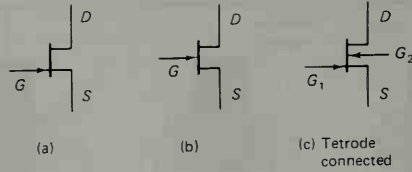
Figure 12-2. Circuit symbols for the *n*-channel JFET.

drain and source [Fig. 12-2(b)]. The symbol shown in Fig. 12-2(c) is used where the terminals of the two gate regions are provided with separate connecting leads. In this case the device is referred to as a *tetrode-connected* FET.

12-3
Characteristics
of *n*-Channel
JFET

12-3.1
*Depletion
Regions*

An *n*-channel JFET is shown in Fig. 12-3 with the gate connected directly to the source terminal. When a drain voltage (V_D) is applied, a drain current I_D flows in the direction shown.
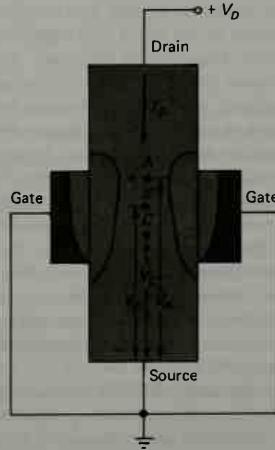
Figure 12-3. *n*-Channel JFET showing internal voltage drops and resulting depletion regions.

Since the n-material is resistive, the drain current causes a voltage drop along the channel. In the portion of the channel between gate and source, I_D causes a voltage drop which biases the gate with respect to that part of the channel close to the gate. Thus, in Fig. 12-3, the gate regions are negative with respect to point A by a voltage V_A. This will cause the depletion regions to penetrate into the channel at point A by an amount proportional to V_A. Between point B and the source terminal the voltage drop along the channel is V_B, which is less than V_A. Therefore, at point B the gate is at $-V_B$ with respect to the channel, and the depletion region penetration is less than at point A. From point C to the source terminal, the voltage drop V_C is less than V_B. Thus, the gate–channel junction reverse bias (at point C) is V_C volts, and penetration by the depletion regions is less than at A or B. This difference in voltage drops along the channel, and the consequent variation in bias, account for the shape of the depletion regions penetrating the n-channel.

When the gate is connected directly to the source (i.e., no external bias), $V_{GS} = 0$. The characteristic for $V_{GS} = 0$ is plotted in Fig. 12-4. When $V_{DS} = 0, I_D = 0$, and the voltage between the gate and all points in the channel is also equal to zero. When V_{DS} is increased by a small amount, a small drain current flows, causing some voltage drop along the channel. This reverse biases the gate–channel junctions by a small amount, causing little depletion region penetration, and having negligible effect on the channel resistance. With further small increases in V_{DS} the drain current increase is nearly linear, and the channel behaves as a resistance of almost constant value.

The channel continues to behave as an almost constant resistance, until the voltage drop along it becomes large enough to cause considerable
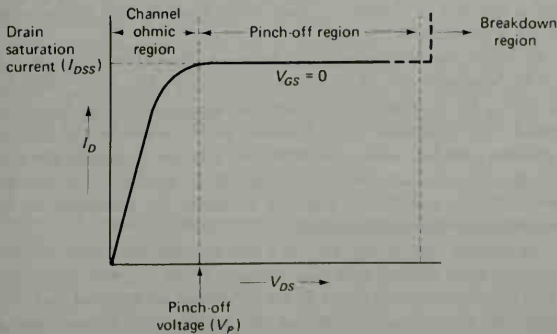
Figure 12-4. Characteristics of n-channel JFET for $V_{GS} = 0$.

penetration by the depletion regions. At this stage the channel resistance is significantly affected by the depletion regions. Further increases in V_{DS} produce smaller increases in I_D, which, in turn, cause increased penetration by the depletion regions and further increase the channel resistance. Because of the rapid increase in channel resistance at this stage (produced by increasing I_D), a *saturation level* of I_D is reached, where further increases in V_{DS} produce only very slight increases in I_D. The drain current at this point, with V_{GS} at zero, is referred to as the *drain–source saturation current I_{DSS}* (see Fig. 12-4). When the drain current saturation level is reached, the shape of the depletion regions is such that they appear to *pinch off* the channel. For this reason, the drain–source voltage at which I_D levels off is designated the *pinch-off voltage (V_P)*, as indicated in Fig. 12-4. The region of the characteristic where I_D is fairly constant is referred to as the *pinch-off region*. The region of the characteristic between $V_{DS} = 0$ and $V_{DS} = V_P$ is termed the *channel ohmic region*, because the channel is behaving as a resistance. With continued increase in V_{DS} a voltage will be reached at which the gate–channel junction breaks down. This is the result of the charge carriers which make up the reverse saturation current at the gate channel junction being accelerated to a high velocity and producing an *avalanche effect* (see Chapter 11). At this point the drain current increases very rapidly, and the device may be destroyed. The normal operating region of the characteristics is the pinch-off region.

When an external bias of, say, -1 V is applied between the gate and source, the gate–channel junctions are reverse biased even when $I_D =$ zero. Therefore, when $V_{DS} = 0$ the depletion regions are already penetrating the channel to some extent. Because of this, a smaller voltage drop along the channel (i.e., smaller than when $V_{GS} = 0$) will increase the depletion regions to the point at which they *pinch off* the current. Consequently, the pinch-off voltage is reached at a lower I_D than when $V_{GS} = 0$. The characteristic for $V_{GS} = -1$ V is shown in Fig. 12-5.

By employing several values of negative external bias voltage, a family of I_D/V_{DS} characteristics is obtained as shown in Fig. 12-5. Note that the value of V_{DS} for breakdown is reduced as the negative gate bias voltage is increased. This is because $-V_{GS}$ is adding to the reverse bias at the junction. If a positive gate bias voltage is employed, a larger I_D can be the result, as shown by the characteristic for $V_{GS} = +0.5$V in Fig. 12-5. In general, however, V_{GS} is maintained negative to avoid the possibility of forward biasing the gate–channel junctions.

The broken line on Fig. 12-5 is a line through the points at which I_D saturates for each level of gate bias voltage. When $V_{GS} = 0$, I_D saturates at I_{DSS}, and the characteristic shows $V_P = 4.5$V. When an external bias of -1 V is applied, the gate–channel junctions still require -4.5 V to achieve pinch off. This means that a 3.5-V drop is now required along the channel instead
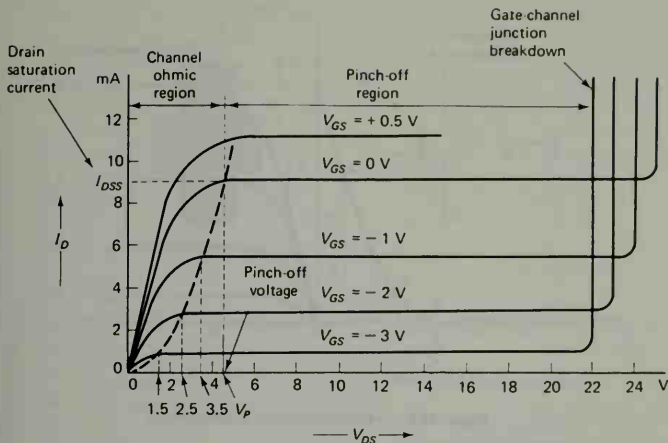
Figure 12-5. n-Channel JFET drain characteristics.

of the previous 4.5 V, and the 3.5 V is achieved with a lower value of I_D. Similarly, when V_{GS} is -2 V and -3 V, pinch off is achieved with 2.5 V and 1.5 V, respectively, along the channel. The 2.5- and 1.5-V drops are, of course, achieved with further reduced values of I_D.

The FET transfer characteristics are experimentally determined by maintaining V_{DS} at a constant level and varying V_{GS} in convenient steps. At each step of V_{GS} the I_D and V_{GS} levels are recorded, and a table of values is obtained from which a graph of I_D is plotted versus V_{GS}. This will give transfer characteristics similar to the transconductance characteristics of a vacuum tube or bipolar transistor (Fig. 12-6). As in the case of other devices, the transfer characteristics may also be derived from the output characteristics by reading off corresponding V_{GS} and I_D levels for a fixed level of V_{DS}.

**12-3.4
Transfer
Characteristics**

Derive the transfer characteristics from the FET drain characteristics in Fig. 12-6.

Example 12-1

solution

Refer to the drain characteristics in Fig. 12-6; when $V_{GS} = 0$, $I_D = 9$mA. Mark point 1 on the transfer characteristics at $I_D = 9$ mA and $V_{GS} = 0$.
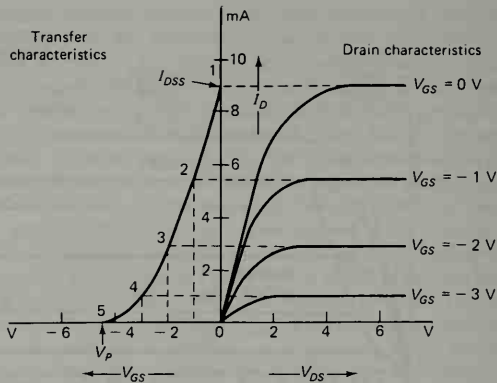
Figure 12-6. n-Channel transfer characteristics.

Point 2 is at $I_D = 5.4$ mA and $V_{GS} = -1$ V

Point 3 is at $I_D = 2.8$ mA and $V_{GS} = -2$ V

Point 4 is at $I_D = 0.9$ mA and $V_{GS} = -3$ V

Point 5 is at $I_D = 0$ mA and $V_{GS} = V_P = -4.5$ V

Draw the transfer characteristic through points 1 to 5.

**12-4
The
p-Channel
JFET**

In this device, the channel is p-type material, and the gate regions are n-type (Fig. 12-7). The drain–source potential is applied, positive to the source, negative to the drain. Thus, a current flows (in the conventional direction) from the source to the drain. To reverse bias the junctions between the gate and the channel, the n-type gate must be made positive with respect to the p-type channel. Therefore, bias voltage is applied, positive on the gate, negative on the source. The voltage drop along the channel is negative at the depletion regions and positive at the source. As in the case of the n-channel device, this voltage drop tends to reverse bias the gate–channel junctions.

Symbols for the p-channel JFET are shown in Fig. 12-7. The arrowhead again points from the p-type material to the n-type material: in this case it points from the p-type channel to the n-type gate. The drain and transconductance characteristics for the p-channel JFET are similar to those of an n-channel device, with the exception that all voltage and current polarities are inverted (Fig. 12-8).
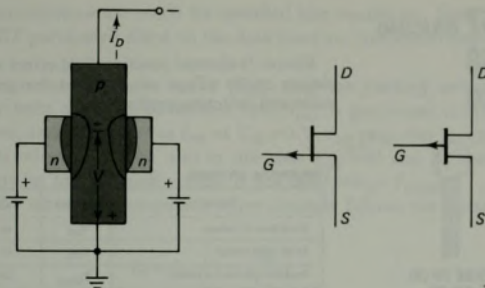
Figure 12-7. Principle of operation and circuit symbols for *p*-channel JFET.
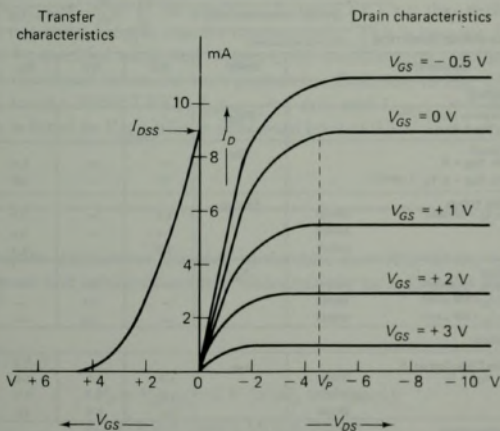
Figure 12-8. *p*-Channel drain and transfer characteristics.

12-5
JFET Data
Sheet and
Parameters

12-5.1
Data
Sheet

A typical FET data sheet is shown in Fig. 12-9. Like the bipolar transistor data sheet, it begins with a device type number and a brief description of the device to indicate the most important applications. These data are followed by the maximum ratings for the FET, and then the

2N**5457** (SILICON)
2N**5458**
2N**5459**

Silicon N-channel junction field-effect transistors depletion mode (Type A) designed for general-purpose audio and switching applications.

CASE 29 (5)
(TO-92)

Drain and source may be interchanged.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D [2]	310 2.82	mW mW/°C
Operating Junction Temperature	T_J [2]	135	°C
Storage Temperature Range	T_{stg} [2]	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($I_G = -10\mu$ Adc, $V_{DS} = 0$)		BV_{GSS}	25	—	—	Vdc
Gate Reverse Current ($V_{GS} = -15$ Vdc, $V_{DS} = 0$) ($V_{GS} = -15$ Vdc, $V_{DS} = 0$, $T_A = 100°C$)		I_{GSS}	— —	— —	1.0 200	nAdc
Gate-Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 10$ nAdc)	2N5457 2N5458 2N5459	$V_{GS(off)}$	0.5 1.0 2.0	— — —	6.0 7.0 6.0	Vdc
Gate-Source Voltage ($V_{DS} = 15$ Vdc, $I_D = 100 \mu$Adc) ($V_{DS} = 15$ Vdc, $I_D = 200 \mu$Adc) ($V_{DS} = 15$ Vdc, $I_D = 400 \mu$Adc)	2N5457 2N5458 2N5459	V_{GS}	— — —	2.5 3.5 4.5	— — —	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current [1] ($V_{DS} = 15$ Vdc, $V_{GS} = 0$)	2N5457 2N5458 2N5459	I_{DSS}	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mAdc
DYNAMIC CHARACTERISTICS						
Forward Transfer Admittance [1] ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 1$ kHz)	2N5457 2N5458 2N5459	$\|y_{fs}\|$	1000 1500 2000	3000 4000 4500	5000 5500 6000	μ mhos
Output Admittance [1] ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 1$ kHz)		$\|y_{os}\|$	—	10	50	μ mhos
Input Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 1$ MHz)		C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 1$ MHz)		C_{rss}	—	1.5	3.0	pF

[1] Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

[2] Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: $P_D = 1.0$ W @ $T_C = 25°C$.
Derate above 25°C – 8.0 mW/°C. $T_J = -65$ to +150°C, $\theta_{JC} = 125°$ C/W.

Figure 12-9. FET data sheet. (Courtesy of Motorola, Inc.)

electrical characteristics are noted for specified bias conditions. Some of the important FET parameters listed on the data sheet are considered below.

The *drain–source saturation current* (I_{DSS}) and the *pinch-off voltage* (V_P) have already been discussed in Section 12-3. I_{DSS} is sometimes termed the *pinch-off current*, and referred to as I_{DP} at $V_{GS} = 0$ V. I_{DP} may also be specified at V_{GS} values other than zero, and in this case V_{GS} will also be specified. Another name for the pinch-off voltage is *gate cutoff voltage* $V_{GS(\text{off})}$.

The FET transfer characteristic approximately follows the equation

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P} \right]^2 \tag{12-1}$$

When I_{DSS} and V_P are known, a table of values of I_D and V_{GS} may be determined from the equation. From this table, the transfer characteristic can be constructed. One of the problems in using FET's is that each device type does not have a single transfer characteristic. This is because I_{DSS} and V_P cannot be specified accurately. Instead, the manufacturer specifies maximum and minimum values for each parameter. Referring to Fig. 12-9, it is seen that, for the 2N5457 FET, $I_{DSS(\text{min})} = 1$ mA, and $I_{DSS(\text{max})} = 5$ mA. Also V_P, which is listed as $V_{GS(\text{off})}$, has a minimum level of 0.5 V and a maximum of 6 V.

Using the information provided on the data sheet (Fig. 12-9), construct the maximum and minimum transfer characteristic for a 2N5459 FET.

Example 12-2

solution

From Fig. 12-9,

$$V_P = V_{GS(\text{off})} = 2 \text{ V (min)}, 8 \text{ V (max)}$$
$$I_{DSS} = 4 \text{ mA (min)}, 16 \text{ mA (max)}$$

To construct the minimum transfer characteristic, the minimum levels of V_P and I_{DSS} are substituted into Eq. (12-1) along with convenient values of V_{GS}.
When $V_{GS} = 0$ V, $I_D = 4$ mA $[1 - 0/2]^2 = 4$ mA.
Plot point 1 of the minimum transfer characteristic at $V_{GS} = 0$ V and $I_D = 4$ mA (Fig. 12-10).

When $V_{GS} = 0.5$ V,	$I_D = 4$ mA $[1 - 0.5/2]^2 = 2.25$ mA	(point 2)
When $V_{GS} = 1$ V,	$I_D = 4$ mA $[1 - 1/2]^2 = 1$ mA	(point 3)
When $V_{GS} = 1.5$ V,	$I_D = 4$ mA $[1 - 1.5/2]^2 = 0.25$ mA	(point 4)
When $V_{GS} = 2$ V,	$I_D = 4$ mA $[1 - 2/2]^2 = 0$ mA	(point 5)
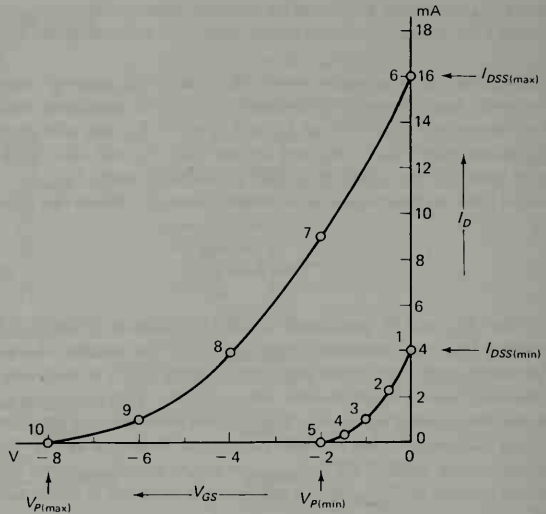
Figure 12-10. Construction of maximum and minimum transfer characteristics for 2N5459.

The minimum transfer characteristic is now drawn through points 1 to 5. For the maximum transfer characteristic the above process is repeated using $I_{DSS} = 16$ mA and $V_P = 8$ V.

When $V_{GS} = 0$ V, $I_D = 16$ mA $[1 - 0/8]^2 = 16$ mA   (point 6)
When $V_{GS} = 2$ V, $I_D = 9$ mA   (point 7)
When $V_{GS} = 4$ V, $I_D = 4$ mA   (point 8)
When $V_{GS} = 6$ V, $I_D = 1$ mA   (point 9)
When $V_{GS} = 8$ V, $I_D = 0$ mA   (point 10)

The maximum transfer characteristic is now drawn through the points as plotted.

12-5.3
Trans-
conductance

It has been shown that I_{DSS} and V_P can readily be determined from the drain and transfer characteristics. Two other quantities that can be determined from the characteristics are the *transconductance* (g_m) and the *drain resistance* (r_d). The transconductance is simply the slope of the transfer

characteristic, and since the slope varies, the value of V_{GS} at which g_m is measured must also be specified. *Forward transfer admittance* or *transadmittance* (Y_{fs}) are other names given to the transconductance (Fig. 12-9). g_m (or Y_{fs}) is usually expressed in *micro Siemens* (μS) [some device manufacturers still use μ *mhos* on their data sheets] and is defined as

$$g_m = \frac{\text{variation in drain current}}{\text{variation in gate–source voltage}}$$

(when drain–source voltage is maintained constant)

$$= \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS}} \qquad (12\text{-}2)$$

From the FET maximum transfer characteristics given in Fig. 12-11, determine g_m at $V_{GS} = -1$ V and $V_{GS} = -4$ V.

Example 12-3
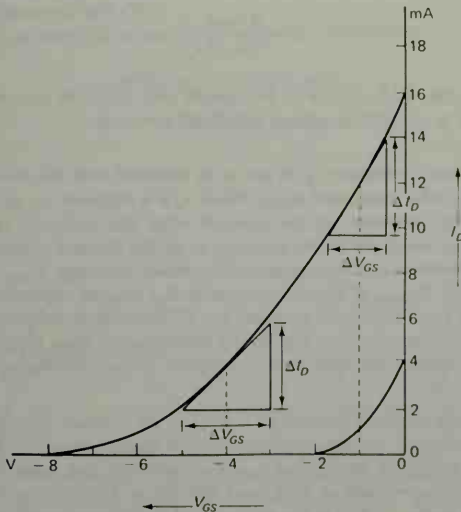
Figure 12-11. Derivation of g_m from transfer characteristics.

solution

From Fig. 12-11 and Eq. (12-2),

$$\text{at } V_{GS} = -1 \text{ V}, \qquad g_m = \frac{4.3 \text{ mA}}{1.25 \text{ V}} = 3.4 \text{ mA/V} = 3400 \mu S$$

$$\text{at } V_{GS} = -4 \text{ V}, \qquad g_m = \frac{3.8 \text{ mA}}{2 \text{ V}} = 1.9 \text{ mA/V} = 1900 \mu S$$

**12-5.4
Drain
Resistance**

    The drain resistance (r_d) is the ac resistance between drain and source terminals when the FET is operating in the pinch-off region. It is also the slope of the drain characteristics in the pinch-off region. Since the characteristics are almost flat, r_d is not easily determined from the characteristics. r_d may also be designated as r_{DSS}, and in each case the units are ohms, kilohms, or megohms. Since r_d is usually the output resistance of the FET, it may also be expressed as an *output admittance*: $|Y_{os}| = 1/r_d$.

    The drain resistance is defined as

$$r_d = \frac{\text{variation in drain–source voltage}}{\text{variation in drain current}}$$

(when the gate–source voltage is maintained constant)

$$= \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}} \tag{12-3}$$

    From Fig. 12-9, $|Y_{os}|$ is 10 μS typical, and 50 μS at maximum. This corresponds to $r_d = 100$ kΩ typical and 20 kΩ minimum.

**12-5.5
Drain–Source
on
Resistance**

    The drain resistance (r_d) is not to be confused with the *drain–source on resistance* R_{DS}, also designated $R_{D(on)}$. While r_d is a dynamic (or ac) quantity, R_{DS} is the dc resistance of the channel when the depletion regions are removed; i.e., when the device is biased *on* in the channel ohmic region of the characteristics. $I_D \times R_{DS}$ gives a *drain–source on voltage* $V_{DS(on)}$ which is similar to the $V_{CE(sat)}$ of bipolar transistors. R_{DS} may be typically 100 Ω or less, and it is an important quantity for FET's used in switching circuits known as *sampling gates*. $I_D \times R_{DS}$ can be much smaller than $V_{CE(sat)}$, making the FET sampling gate superior to the bipolar transistor sampling gates.

**12-5.6
Gate Cutoff
Current
and Input
Resistance**

    The gate–channel junction in a JFET is an ordinary *pn*-junction, and since it is normally reverse biased, a minority charge carrier current flows. This is the *gate–source cutoff current* I_{GSS}, also called the *gate reverse current*. For the 2N5457, $I_{GSS} = 1$ nA at 25°C and 200 nA at 100°C (Fig. 12-9). The device *input resistance* (R_{GS}) is the resistance of the reverse-biased gate–channel junctions, and is inversely proportional to I_{GSS}. Typical values of R_{GS} for a JFET are 10^9 Ω at 25°C and 10^7 Ω at 100°C.

There are several ways in which the FET breakdown voltage may be specified. BV_{DGO} is the *drain-gate breakdown voltage* with the source open circuited. BV_{GSS} is the *gate–source breakdown voltage* with the drain shorted to the source. Typical values for each are in the region of 25 V; they are listed on the 2N5457 data sheet of Fig. 12-9. Both are a measure of the voltage at which the reverse-biased gate–channel junctions break down.

All devices have a temperature-dependent limit to the power that they can dissipate. P_D is normally specified at 25°C, with a derating factor included for operation at higher temperatures. As in the case of bipolar transistors, a maximum power dissipation curve may be drawn upon the FET characteristics.

On the drain characteristics of Fig. 12-12 draw the maximum power dissipation curve for a FET with $P_D = 200$ mW operating at a maximum ambient temperature of 100°C. The derating factor is 2 mW/°C.

solution

$$P_D \text{ at } 25°C = 200 \text{ mW}$$

Derating factor = 2 mW/°C.
Maximum ambient rise above 25°C = 100°C − 25°C = 75°C.

$$P_D \text{ at } 100°C = P_D - (2 \text{ mW} \times 75°C)$$

$$= 200 \text{ mW} - 150 \text{ mW} = 50 \text{ mW}$$
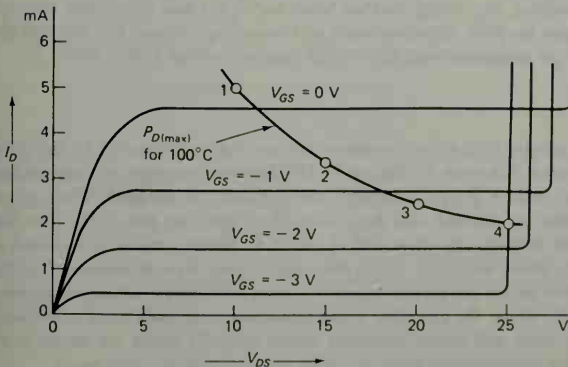
Figure 12-12. Maximum power dissipation curve at 100°C.

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When $V_{DS} = 10$ V, $I_D = P_D/V_{DS} = 50$ mW/10 V = 5 mA.
Plot point 1 on Fig. 12-12 at $V_{DS} = 10$ V, $I_D = 5$ mA.

At $V_{DS} = 15$ V, $I_D = 50$ mW/15 V = 3.3 mA (point 2)

At $V_{DS} = 20$ V, $I_D = 50$ mW/20 V = 2.5 mA (point 3)

At $V_{DS} = 25$ V, $I_D = 50$ mW/25 V = 2 mA (point 4)

Join all the points together as shown to draw the maximum power dissipation curve for $T = 100°C$.

12-5.9
Noise
Figure

One advantage of a FET over a bipolar transistor is that the FET usually has much lower noise. This is because, unlike the bipolar transistor, there are very few charge carriers crossing junction in the FET. As in the case of the bipolar device, the FET *noise figure* (*NF*) is specified as a *spot noise figure* at a particular frequency and bias conditions and for a given value of bias resistance. The figure will vary if any of these conditions are altered. Noise calculations for a FET circuit are performed in the same way as for a bipolar transistor circuit.

12-5.10
Capacitances

Capacitances for FET's may be specified as *gate–drain capacitance* (C_{gd}), *gate–source capacitance* (C_{gs}), and *drain–source capacitance* (C_{ds}). Instead of these quantities, the capacitance is sometimes specified as the *common source input capacitance* (C_{iss}) or (C_{gss}). This is the gate–source capacitance measured with the drain shorted to the source. In this case a *reverse transfer capacitance* (C_{rss}) is also specified, C_{rss} being another term for C_{gd}. These quantities are very important for FET high-frequency and switching circuits. For the 2N5457, C_{iss} is 7 pF maximum and C_{rss} is 3 pF maximum (Fig. 12-9).

12-6
JFET
Construction

Junction field effect transistors are normally constructed by the diffusion process (Chapter 7). Figure 12-13 illustrates one type of construction. Starting with a *p*-type substrate, an *n*-channel is diffused. Then *p*-type impurities are diffused into the *n*-channel to form one side of the gate, the substrate forming the other side of the gate. Finally, metal is deposited in place to make terminals. With this symmetrical type of construction, the drain and source are interchangeable. Other fabrication techniques produce devices in which the geometry is not symmetrical. In such cases interchanging the drain and source terminals would radically affect the device characteristics.
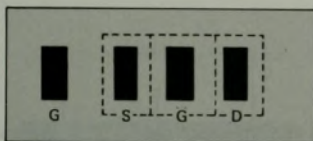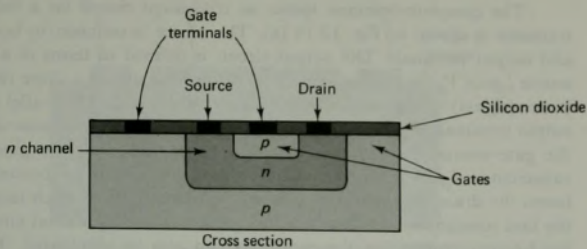
Figure 12-13. *n*-Channel diffused JFET construction.
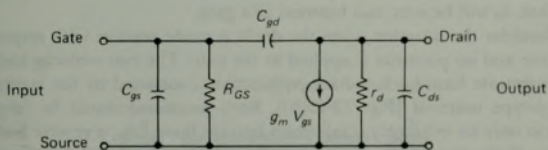
(a) Complete equivalent circuit
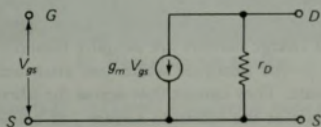
(b) Low frequency ac equivalent circuit

Figure 12-14. Equivalent circuits for junction field effect transistor.

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The complete common source ac equivalent circuit for a field effect transistor is shown in Fig. 12-14 (a). The source is common to both input and output terminals. The output circuit is defined in terms of a current source ($gm \times V_{gs}$) supplying current to drain resistance (r_d). Note that V_{gs} is the ac (signal) voltage applied between gate and source. In parallel with the output terminals is the drain–source capacitance C_{ds}. Input signals will "see" the gate–source leakage resistance R_{GS} in parallel with the gate–source capacitance C_{gs}. The drain–gate capacitance C_{gd} is shown connected between the drain and gate terminals. R_{GS} is normally very much larger than the bias resistances, so it can be eliminated from the equivalent circuit. For low-frequency operation the capacitors can also be eliminated. The simplified low-frequency equivalent circuit is as shown in Fig. 12-14(b).

12-8
The
MOSFET

12-8.1
Enhancement
Mode
MOSFET

Figure 12-15(a) shows the construction of an *insulated gate FET* or *metal oxide semiconductor FET* (MOSFET). Starting with a high-resistive *p*-type substrate, two blocks of heavily doped *n*-type material are diffused into the substrate, and then the surface is coated with a layer of silicon dioxide. Holes are cut through the silicon dioxide to make contact with the *n*-type blocks. Metal is deposited through the holes to form drain and source terminals, and on the surface area between drain and source, a metal plate is deposited. This plate, as will be seen, can function as a gate.

Consider the situation when the drain is made positive with respect to the source and no potential is applied to the gate. The two *n*-blocks and the *p*-type substrate form back-to-back *pn*-junctions connected by the resistance of the *p*-type material [Fig. 12-15(b)]. Both junctions cannot be forward biased, so only an extremely small drain current flows (i.e., a reverse leakage current). If the *p*-substrate is now connected to the source terminal, there is zero voltage across the source–substrate junction, and the drain–substrate junction remains reverse biased. When the gate is made positive with respect to the source and the substrate, negative charge carriers are induced in the substrate as shown in Fig. 12-15(c). As the gate potential is increased, more and more negative charge carriers are induced in the substrate. The induced charge carriers are actually minority charge carriers (electrons) within the *p*-type substrate which are attracted to the positive voltage on the metal plate. They cannot flow across the silicon dioxide to the plate, so they accumulate at the substrate surface just below the plate. The minority charge carriers constitute an *n*-type channel stretching from drain to source. Thus, a drain current flows and its magnitude depends upon the channel resistance, which in turn depends upon the number of charge carriers induced by the positive gate. The gate potential, therefore, controls the drain current. Since the conductivity of the channel is *enhanced* by the

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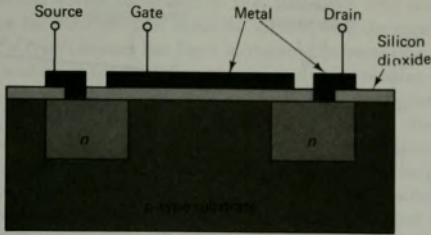
(a) Construction of n-channel enhancement mode MOSFET
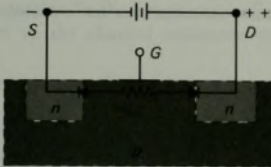
(b) Equivalent circuit when drain-source voltage is applied without any gate bias
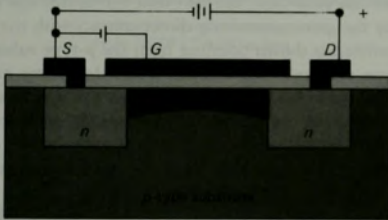
(c) Effect of positive gate bias

Figure 12-15. *n*-Channel enhancement mode MOSFET.

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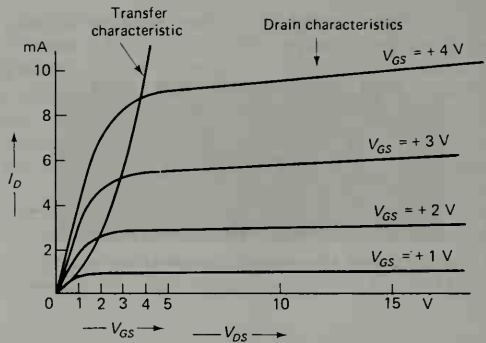
Figure 12-16. Drain and transfer characteristics for *n*-channel enhancement mode MOSFET.

positive bias on the gate, the device is known as an *enhancement mode* MOSFET.

The drain and transfer characteristics of the enhancement mode MOSFET are shown in Fig. 12-16. Note that the drain current increases with positively increasing gate–source bias voltage. Because the gate of the MOSFET is insulated from the channel, there is no leakage current involved. This gives the device a very high input resistance, in some cases 10^{15} Ω or greater. Transconductance values for MOSFETs typically range from 1000 μS to 2000 μS, i.e., from 1 to 2 mA/V.

Two symbols for the enhancement mode *n*-channel MOSFET are shown in Fig. 12-17. In each case, the fact that the device has an insulated gate is indicated by the gate not making direct contact with the channel. In each case the arrowhead is shown pointing from the *p*-type substrate toward the (induced) *n*-type channel. One symbol shows the source and substrate internally connected, while the other symbol shows the substrate connection brought out separately from the source. The line representing the channel is broken into three sections to show that the channel does not exist until a gate voltage is applied, i.e., to show that the device is operated in the *enhancement mode*.

A *p*-channel enhancement mode MOSFET is constructed by starting with an *n*-type substrate and diffusing *p*-type drain and source blocks. All voltage and current polarities are then the reverse of those for the *n*-channel device, and the direction of the arrowhead is reversed in the circuit symbol.
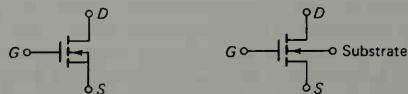
Figure 12-17. Circuit symbols for *n*-channel enhancement mode MOSFET.

Consider the device illustrated in Fig. 12-18 (a). The construction is the same as for the enhancement mode MOSFET, with the exception that a lightly doped n-type channel has been introduced between the two heavily doped source and drain blocks. When the drain is made positive with respect to the source, a drain current will flow, even with zero gate potential. If the gate is made negative with respect to the substrate, positive charge carriers are induced in the n-type channel. These positive charge carriers absorb free negative charge carriers and cause the channel resistance to increase. Drain current is decreased, and the effect is similar to that in the n-channel JFET. Since the action of the negative voltage on the gate is to deplete the channel of free n-type charge carriers, the device is referred to as a *depletion mode* MOSFET.

If the drain characteristics are plotted for various levels of negative gate–source voltage, the curves obtained are very similar to those of an n-channel JFET. Now consider what happens if the gate is made positive with respect to the substrate. In the n-type channel, additional n-type charge carriers are induced, so the channel resistance decreases. Therefore, the
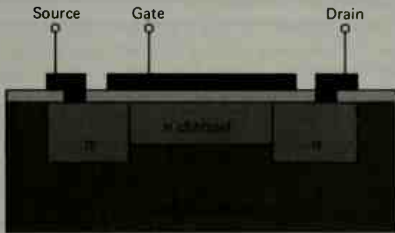
(a) n–channel depletion-enhancement
mode MOSFET with no bias
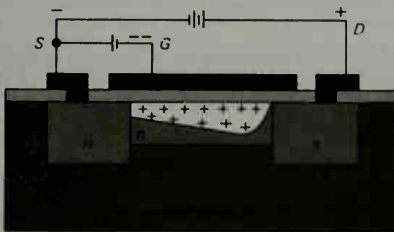
(b) Depletion mode operation

Figure 12-18. n-Channel depletion–enhancement mode MOSFET.
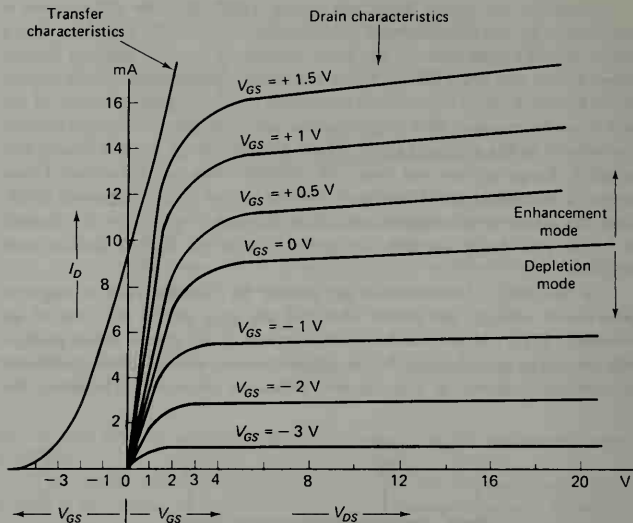
Figure 12-19. Drain and transfer characteristics for *n*-channel depletion–enhancement mode MOSFET.
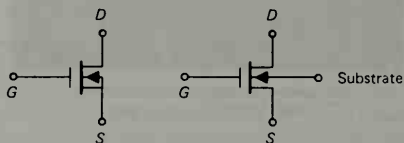
Figure 12-20. Circuit symbols for *n*-channel depletion–enhancement mode MOSFET.

depletion mode MOSFET is capable of being operated in the enhancement mode also. The resultant characteristics are shown in Fig. 12-19.

The symbols for the depletion–enhancement mode MOSFET (Fig. 12-20) are similar to those for the enhancement mode device, with the exception that the line representing the channel is now solid.

12-9
The
V-MOSFET

The construction of the V-MOSFET (or V-FET) is quite different from that of the MOSFET discussed in Section 12-8. The cross section of an *n*-channel V-FET is illustrated in Fig. 12-21. A V-shaped cut penetrates from the surface of the device through n^+, p, and n^- layers almost to the n^+
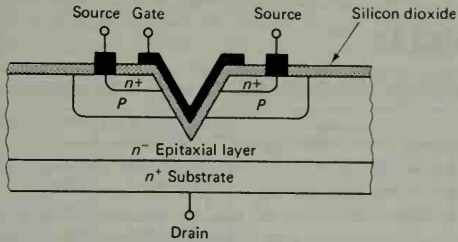
Figure 12-21. Cross section of n-channel enhancement mode V-MOSFET.

substrate. The n^+ layers are heavily doped, low resistive material, while the n^- layers are lightly doped, high resistive regions. The silicon dioxide layer covers both the horizontal surface and the surface of the V-cut. The (insulated) gate is a metal film deposited on the silicon dioxide in the V-cut. Source terminals make contact (through the silicon dioxide) to the upper n^+ and p layers. The n^+ substrate is the drain terminal of the device.

This is an *enhancement mode* FET; no channel exists between the drain and source regions until the gate is made positive with respect to the source. As in the case of the enhancement mode MOSFET described in Section 12-8.1, an n-type channel forms close to the gate when the gate is made positive with respect to the source. In the case of the V-FET, this n-type channel provides a vertical path for charge carrier flow between the n^+ substrate, i.e., the drain, and the n^+ source termination. When the gate–source voltage is zero or negative, no channel exists and no current flow occurs.

The drain characteristics and transfer characteristics for the enhancement mode n-channel V-FET are similar to those for the enchancement mode MOSFET (Fig. 12-16). As the gate is made more and more positive with respect to the source, the channel resistance is reduced and more drain current flows. The gate voltage controls the drain current so that, for a given level of V_{GS}, I_D remains fairly constant over a wide range of V_{DS} levels.

p-Channel VMOS field effect transistors are also available. As for p-channel JFETS and p-channel MOSFETS, the characteristics are similar to those of the n-channel devices, except that the current directions and voltage polarities are reversed. Because the drain terminal of the V-FET is at the bottom of the device, instead of at the top surface, the drain can have a considerably larger area for any given device size. This allows much greater power dissipations than are possible in a MOSFET with both drain and source at the surface.

In the V-FET the channel length is determined by the diffusion process, while in the MOSFET, with a channel parallel to the surface of the semiconductor, the channel length depends upon the dimensions of the photographic masks employed in the diffusion process. By controlling the

VN88AF

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Typ	Max	Unit	Test Conditions
1		BV_{DSS} Drain-Source	80				$V_{GS} = 0, I_D = 10\,\mu A$
2		Breakdown	80			V	$V_{GS} = 0, I_D = 2.5\,mA$
3		$V_{GS(th)}$ Gate Threshold Voltage	0.8		2.0	V	$V_{DS} = V_{GS}, I_D = 1\,mA$
4		I_{GSS} Gate Body Leakage		0.05	100	nA	$V_{GS} = 15\,V, V_{DS} = 0$
5					500		$V_{GS} = 15\,V, V_{DS} = 0, T_A = 125°C$ (Note 2)
6	S T A T I C	I_{DSS} Zero Gate Voltage Drain Current			10	μA	$V_{DS} = $ Max. Rating, $V_{GS} = 0$
7					500		$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0, T_A = 125°C$ (Note 2)
8				100		nA	$V_{DS} = 25\,V, V_{GS} = 0$
9		$I_{D(on)}$ ON State Drain Current (Note 1)	1.0	2		A	$V_{DS} = 25\,V, V_{GS} = 10\,V$
10		$V_{DS(on)}$ Drain-Source Saturation Voltage (Note 1)		0.4		V	$V_{GS} = 5\,V, I_D = 0.1\,A$
11				1.4	1.7		$V_{GS} = 5V, I_D = 0.3\,A$
12				1.3			$V_{GS} = 10\,V, I_D = 0.5\,A$
13				3.0	4.0		$V_{GS} = 10\,V, I_D = 1.0\,A$
14		g_m Forward Transconductance (Note 1)	170	250		m mhos	$V_{DS} = 24\,V, I_D = 0.5\,A$
15		C_{iss} Input Capacitance (Note 2)			50		
16	D Y N A M I C	C_{rss} Reverse Transfer Capacitance (Note 2)			10	pF	$V_{GS} = 0, V_{DS} = 25\,V, f = 1.0\,MHz$
17		C_{oss} Common-Source Output Capacitance (Note 2)			50		
18		$t_{d(on)}$ Turn-ON Delay Time (Note 2)		2	5		
19		t_r Rise Time (Note 2)		2	5	ns	See Switching Time Test Circuit
20		$t_{d(off)}$ Turn-OFF Delay Time (Note 2)		2	5		
21		t_f Fall Time (Note 2)		2	5		

NOTES 1. Pulse test — 80 μs pulse, 1% duty cycle 2. Sample test

Output Characteristics
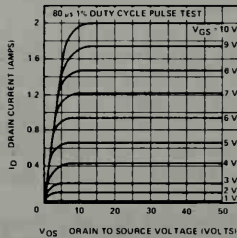
Transfer Characteristic
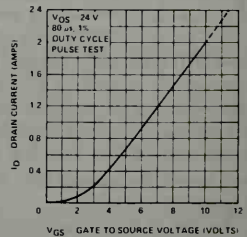
Figure 12-22. Portion of data sheet for V-MOS field effect transistor. (Courtesy of Siliconix, Inc.)

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doping density and the diffusion time, much shorter channels can be created than are possible with mask control of channel length. These shorter channels allow greater current densities, which again contribute to larger power dissipations. The shorter channel length also allows a higher transconductance to be achieved in the V-FET, and very considerably improves the frequency response and switching time of the device.

Another very important factor in V-FET geometry is the presence of the lightly doped n^- epitaxial layer close to the n^+ substrate. When the gate voltage is zero or negative and the drain is positive with respect to the source, the junction between the p-layer and the n-layer is reverse biased. The depletion region at this junction penetrates deep into the n^- layer, and thus avoids *punch through* from drain to source. Because of this, relatively high drain–source voltages can be applied without any danger of device breakdown.

The V-MOSFET can now be described as a high-voltage power transistor capable of high-frequency and fast-switching operation, and having a large transconductance value.

A portion of the manufacturer's data sheet for the SILICONIX VN88AF n-channel enhancement mode V-MOS power FET is shown in Fig. 12-22. The device has a rated maximum power dissipation of 12.5 W, can survive a V_{DS} of 80 V, and can pass a drain current of 2 A. The output characteristics show that, when $V_{GS} = 7$ V, I_D is constant at just over 1.2 A for V_{DS} levels in excess of approximately 8 V.

The transfer characteristic for the VN88AF is almost linear over most of its length. The g_m of the device is typically 250 mS, or 250 mA/V. This compares very favorably with the 6 mA/V (maximum) specified for the 2N5459 JFET (see Fig. 12-9) and with the 20 mA/V maximum usually found in MOSFETs. Since the gain of a FET amplifier is approximately $g_m \times R_L$ (see Section 14-3), V-FET stages obviously have much larger gains than other FET amplifiers.

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n-channel JFET.   Field effect transistor consisting of n-type channel and p-type gate regions, with gates and channel forming pn-junctions.

p-channel JFET.   Field effect transistor consisting of p-type channel and n-type gate regions, with gates and channel forming pn-junctions.

Drain.   FET terminal at one end of channel—most positive terminal for n-channel JFET.

Source.   FET terminal at opposite end of channel from drain—negative channel terminal for n-channel JFET.

Gate.   FET input terminal—controls channel current.

Unipolar transistor. n-channel or p-channel FET.

Drain current, I_D.   Current flowing into or out of the drain terminal.

Source current, I_S.   Current flowing into or out of the source terminal.

Tetrode connected FET. FET with two gate regions, each having separate terminals.

Depletion regions. Regions depleted of charge carriers penetrating into the channel when the gate–channel junctions are reverse biased.

Drain characteristics. Plot of drain current versus drain–source voltage for various levels of gate–source voltage.

Channel ohmic region. Region of drain characteristics in which the FET is behaving like a resistor.

Pinch-off region. Region of drain characteristics in which drain current remains almost constant for a given level of gate–source voltage.

Breakdown region. Region of drain characteristics in which the drain–gate junction breaks down.

Drain saturation current, I_{DSS}. Level of I_D at commencement of saturation region with gate–source voltage at zero.

Pinch-off voltage, V_P. Drain–source voltage at I_{DSS}, the level of V_{GS} at which I_D becomes zero.

Transfer characteristic. Plot of I_D versus V_{GS}.

Transconductance, g_m. Ratio of I_D change to gate–source voltage change for a given level of V_{DS}.

Forward transfer admittance. Same as *transconductance*.

Transadmittance, Y_{fs}. Same as *transconductance*.

Drain resistance, r_d. The drain–source ac resistance when the FET is operating in the pinch-off region. The reciprocal of the slope of the drain characteristics in the pinch-off region.

Output admittance, Y_{os}. The inverse of r_d.

Drain–source on resistance, R_{DS}. The dc drain to source resistance when the FET is biased *on* in the channel ohmic region of the characteristics.

Drain–source on voltage, $V_{DS(on)}$. $I_D \times R_{DS}$.

Gate–source cutoff current, I_{GSS}. Small current which flows across the reverse-biased gate–channel junctions of a JFET.

Gate reverse current. Same as I_{GSS}.

Input resistance, R_{GS}. Resistance of reverse-biased gate–channel junctions.

Drain–gate breakdown voltage, BV_{DGO}. Drain–gate voltage at which gate–channel junctions break down.

Gate–source breakdown voltage, BV_{GSS}. Gate–source voltage at which gate–channel junctions break down.

Common source input capacitance, C_{iss} or C_{gss}. The gate–source capacitance measured with the drain shorted to the source.

Reverse transfer capacitance, C_{rss} or C_{gd}. The drain–gate capacitance.

MOSFET. Metal oxide semiconductor field effect transistor.

Enhancement mode MOSFET. MOSFET which is *off* when $V_{GS} = 0$. Channel conductivity must be enhanced by increasing bias from zero.

Depletion–enhancement MOSFET. MOSFET which conducts when V_{GS} = 0. Channel conductivity can be depleted or enhanced by increasing or decreasing bias.

V-MOSFET. MOSFET in which the gate is V-shaped; high-frequency, high-power device.

12-1. Using illustrations, explain the principle of the n-channel JFET. Show the internal depletion regions, and explain their shape.

12-2. Sketch typical drain characteristics for an n-channel JFET, and explain. Indicate and name the regions of the characteristics. Define and mark I_{DSS} and V_P on the characteristics.

12-3. Sketch a typical transconductance characteristic for an n-channel JFET, and show how g_m may be derived from it.

12-4. Repeat Questions 12-1 and 12-2 for a p-channel JFET.

12-5. Draw the complete equivalent circuit for a JFET. Explain the origin of each component, suggest typical values, and show how the circuit can be simplified for low-frequency operation. Show how some of the parameters involved may be derived from the drain characteristics.

12-6. Draw sketches to show one type of JFET construction. Label all parts and explain.

12-7. Using illustrations, explain the principle of the n-channel enhancement MOSFET. Also sketch the device drain characteristics and explain.

12-8. Repeat Question 12-7 for an n-channel depletion–enhancement MOSFET.

12-9. Sketch the symbols and characteristics for n-channel JFET, p-channel JFET, n-channel enhancement MOSFET, n-channel depletion–enhancement MOSFET, and p-channel depletion–enhancement MOSFET.

12-10. Sketch the cross section of a V-MOSFET and explain how it operates.

12-11. Sketch typical output and transconductance characteristics for a V-FET. Briefly discuss the performance of this device and compare it to other FET's.

12-1. From the drain characteristics in Fig. 12-12, derive the transfer characteristic.

12-2. Using the information provided in the data sheet (Fig. 12-9), construct the maximum and minimum transfer characteristics for a 2N5458 FET.

12-3. From the FET maximum transfer characteristic constructed for Problem 12-2, determine the value of g_m at $V_{GS} = -1$ V and $V_{GS} = -6$ V.

12-4. On the drain characteristics shown in Fig. 12-5, draw the maximum power dissipation curve for a 2N5458 FET operating at a maximum ambient temperature of 125°C.

12-5. From the transfer characteristics for a VN88AF in Fig. 12-22, determine the value of g_m. Using the output characteristics given in Fig. 12-22, draw the transfer characteristic for $V_{DS} = 10$ V. Determine g_m from this characteristic.

FET Biasing

13-1
Introduction

Thermal runaway does not occur with field effect transistors; however, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple bias techniques. To obtain reasonable limits on the quiescent values of drain current, bias techniques similar to those used with vacuum-tube circuits must be employed. For both analysis and design of FET bias circuits, a graphical approach is most convenient. With few exceptions, MOSFET bias circuits are almost identical to those used for JFET's.

13-2
DC Load
Line and
Bias Point

13-2.1
DC Load
Line

The dc load line for a FET circuit is drawn upon the device characteristics in exactly the same way as was done with the bipolar transistor circuit (see Section 5-2). Consider the common source circuit and device character-
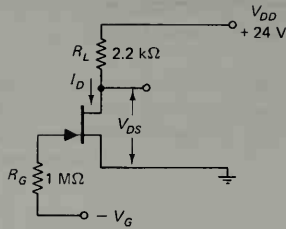
(a) Common
source circuit
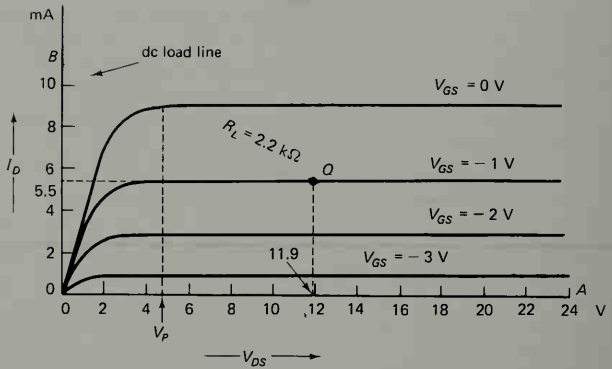
(b) Plotting dc load line

Figure 13-1. DC load line for common source circuit.

istics shown in Fig. 13-1. The drain–source voltage = (supply voltage) − (voltage drop across R_L):

$$V_{DS} = V_{DD} - I_D R_L \qquad (13\text{-}1)$$

By substituting any convenient values of I_D into Eq. (13-1), the corresponding levels of V_{DS} can be calculated. These points are then plotted on the characteristics and the load line is drawn through them.

Example 13-1 Construct the dc load line for the FET common source circuit and characteristics shown in Fig. 13-1.

solution

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Spread of
Characteristics
and Fixed
Bias Circuit

$$V_{DS} = V_{DD} - I_D R_L$$

When $I_D = 0$,

$$V_{DS} = V_{DD} = 24 \text{ V}$$

Plot point A on the characteristics at $I_D = 0$ and $V_{DS} = 24$ V.
When $V_{DS} = 0$,

$$0 = V_{DD} - I_D R_L$$

$$I_D = \frac{V_{DD}}{R_L} = \frac{24 \text{ V}}{2.2 \text{ k}\Omega} = 10.9 \text{ mA}$$

Plot point B on the characteristics at $I_D = 10.9$ mA and $V_{DS} = 0$ V. The dc
load line is now drawn through points A and B.

The dc load line for a FET circuit is a graph of corresponding I_D and
V_{DS} levels for given values of load resistance and supply voltage. The load
line defines all dc values of I_D and V_{DS} that can exist in the circuit. If either
R_L or V_{DS} is changed, a new dc load line must be drawn.

A *dc bias point* or *quiescent point* (Q point) similar to that for bipolar
transistor circuits is selected on the load line. This point defines the dc
conditions that exist in the circuit when no input signal is applied. As
explained in Section 5-2, the bias point may be selected to give maximum
possible equal positive and negative changes in the output voltage from the
circuit. Where maximum possible output voltage variations are not required,
the bias point may be selected at any convenient position on the load line.
For a FET amplifier circuit, however, V_{DS} must not be allowed to fall below
the pinch-off voltage [V_P on Fig. 13-1(b)]. Also, since the gain of a field
effect device is nonlinear, FET amplifiers are usually arranged to give only
small output voltage variations. The Q point for a FET circuit is usually
selected for a convenient value of gate bias voltage. In Fig. 13-1(b) the Q
point is at $V_{GS} = -1$ V, giving $I_D = 5.5$ mA and $V_{DS} = 11.9$ V.

13-2.2
*The Bias
Point*

For a given FET type, typical values of I_{DSS} and V_P are specified on
the device data sheet. These quantities cannot be specified to close toler-
ances, so as explained in Section 12-5, the maximum and minimum values
are also specified. The maximum and minimum values may easily range to
$\pm 50\%$ or more of the typical values. Because of this spread on I_{DSS} and V_P,
there are significant effects on the drain and transfer characteristics. These
are shown in Fig. 12-10 where the maximum and minimum transfer
characteristics are plotted for a 2N5459 FET.

13-3
Spread of
Characteristics
and Fixed
Bias Circuit

The circuit of Fig. 13-1(a) is an example of *fixed bias*. The gate is biased via resistance R_G to a negative voltage V_G. The maximum and minimum levels of I_D for a given bias voltage can be best determined by a graphical technique. A *bias line* is drawn vertically on the transfer characteristics at the fixed level of V_{GS}. $I_{D(max)}$ and $I_{D(min)}$ are then indicated at the intersections of the bias line and the transfer characteristics.

Example 13-2

The maximum and minimum transfer characteristics for the FET in the circuit of Fig. 13-1 (a) are shown in Fig. 13-2. Draw the bias line for $V_G = -1$ V and determine the maximum and minimum levels of I_D and the corresponding V_{DS} levels.
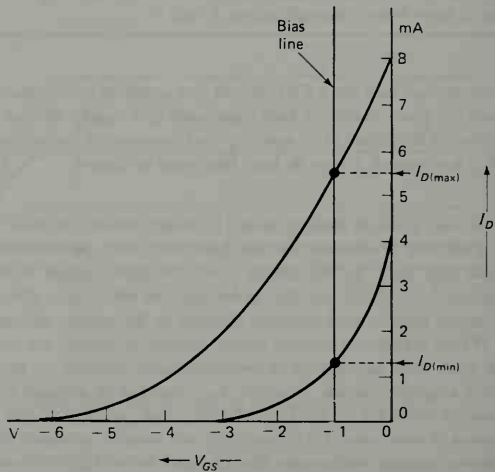
Figure 13-2. $I_{D(max)}$ and $I_{D(min)}$ determination for fixed bias circuit.

solution

$V_{GS} = V_G = -1$ V, V_{GS} being a fixed quantity unaffected by I_D and V_{DS}.
    Draw a *bias line* vertically from $V_{GS} = -1$ V as shown in Fig. 13-2.
    From the points at which the bias line intersects the characteristic, it is seen that $I_{D(max)} = 5.5$ mA and $I_{D(min)} = 1.25$ mA.
    Eq. (13-1)

$$V_{DS} = V_{DD} - I_D R_L$$

For $I_{D(\max)}$,

$$V_{DS} = 24 \text{ V} - (5.5 \text{ mA} \times 2.2 \text{ k}\Omega) = 11.9 \text{ V}$$

For $I_{D(\min)}$,

$$V_{DS} = 24 \text{ V} - (1.25 \text{ mA} \times 2.2 \text{ k}\Omega) = 21.25 \text{ V}$$

Example 13-2 shows that because of the spread in FET characteristics, the fixed bias technique is by no means reliable. It is possible to make such a circuit function satisfactorily by adjusting V_G to give the desired level of V_{DS}. However, this is acceptable only in an experimental situation. For more predictable bias conditions, slightly more complicated circuit techniques must be resorted to.

The process of biasing p-channel FET's is exactly the same as for n-channel devices, with the exception that all voltage polarities are reversed.

13-4
Self-Bias

13-4.1
Bias Line

In the *self-biased circuit* a resistance in series with the source terminal provides the gate bias voltage. Consider the self-biased circuit shown in Fig. 13-3. The voltage drop across R_S is $V_{R_S} = I_D \times R_S$. If $I_D = 1 \text{mA}$ and $R_S = 1$ kΩ, then $V_{R_S} = 1$V. In this case the source terminal is 1V positive with respect to ground or, in other words, ground is 1V negative with respect to the source terminal. Since the gate is grounded via R_G, the gate terminal is also 1V negative with respect to the source terminal; i.e., the gate–source bias is $V_{GS} = -1$V. It is seen that for the self-biased circuit the gate–source bias voltage is

$$V_{GS} = -I_D \times R_S \qquad (13-2)$$

To determine the maximum and minimum values of I_D, it is best to again apply a graphical analysis technique. By selecting convenient values of I_D and calculating the corresponding levels of V_{GS}, a *bias line* may be drawn upon the transfer characteristics. The points where this bias line intersects the transfer characteristics give $I_{D(\max)}$ and $I_{D(\min)}$. Summing the voltage drops across R_L, the transistor, and R_S gives

$$V_{DD} = I_D R_L + V_{DS} + I_D R_S \qquad (13-3)$$

From Eq. (13-3), the maximum and minimum levels of V_{DS} may be calculated once $I_{D(\max)}$ and $I_{D(\min)}$ are determined.
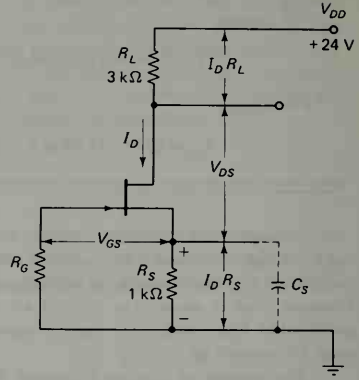
Figure 13-3. Self-biased circuit.

Example 13-3   The circuit of Fig. 13-3 uses a FET with the maximum and minimum transfer characteristics shown in Fig. 13-4. Determine the values of $I_{D(\max)}$ and $I_{D(\min)}$ and the corresponding values of V_{DS}.

solution

From Eq. (13-2),

$$V_{GS} = -I_D R_S$$

When $I_D = 0$, $V_{GS} = 0$. Plot point A on the bias line at $I_D = 0$ and $V_{GS} = 0$.
When $I_D = 5$ mA, $V_{GS} = -5$ mA $\times 1$ kΩ $= -5$ V. Plot point B at $I_D = 5$ mA, $V_{GS} = -5$ V.
The bias line for $R_S = 1$ kΩ is now drawn through points A and B.
Where the bias line cuts the maximum and minimum transfer characteristics, read

$$I_{D(\max)} = 2.5 \text{ mA}$$

and

$$I_{D(\min)} = 1.2 \text{ mA}$$

From Eq. (13-3),

$$V_{DS} = V_{DD} - I_D R_L - I_D R_S$$

$$= V_{DD} - I_D (R_L + R_S)$$
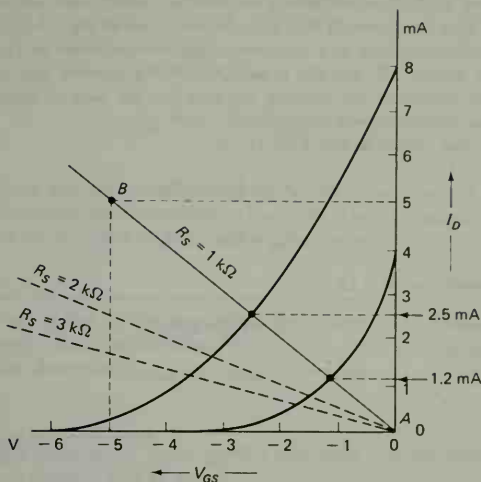
Figure 13-4. $I_{D(max)}$ and $I_{D(min)}$ determination for self-biased circuit.

For $I_{D(max)}$,

$$V_{DS} = 24 \text{ V} - 2.5 \text{ mA}(3 \text{ k}\Omega + 1 \text{ k}\Omega) = 14 \text{ V}$$

For $I_{D(min)}$,

$$V_{DS} = 24 \text{ V} - 1.2 \text{ mA}(3 \text{ k}\Omega + 1 \text{ k}\Omega) = 19.2 \text{ V}$$

It is seen from Example 13-3 that the self-bias technique gives closer limits on I_D, and consequently on V_{DS}, than the fixed-bias circuit. The I_D limits can be even closer if a larger value of R_S is used. The bias lines drawn as broken lines on Fig. 13-4 are for $R_S = 2 \text{ k}\Omega$ and $3 \text{ k}\Omega$, as shown. Although the limits of I_D are closer with large values of R_S, I_D is reduced to quite low levels, and this can be a distinct disadvantage.

As already explained, source resistance R_S is included to stabilize the drain current. R_S will also tend to stabilize I_D against signals applied to the gate; i.e., R_S will reduce the ac voltage gain of the circuit. C_S in Fig. 13-3 is a large capacitor which acts as an ac short circuit across R_S, so that maximum ac gain is achieved. As in the case of bipolar transistor circuits, the total dc load is $(R_L + R_S)$, and the ac load (with R_S bypassed) is R_L. Therefore, an *ac load line* must be drawn to describe the ac performance of the circuit.

**13-4.2
Bypass
Capacitor**

Two methods of employing an external voltage and source resistance for FET bias are shown in Fig. 13-5. In the circuit of Fig. 13-5(a) the source resistance is connected to a negative supply voltage, while in Fig. 13-5(b) a potential divider (R_1 and R_2) is used to derive a positive bias voltage from V_{DD}. The procedure for drawing the bias line for each of these circuits is similar to that for the self-bias circuit.

For the circuit of Fig. 13-5(a),

$$V_{SS} = I_D R_S + V_{GS}$$

$$V_{GS} = V_{SS} - I_D R_S \qquad (13\text{-}4)$$

For the circuit of Fig. 13-5(b).

$$V_G = V_{GS} + I_D R_S$$
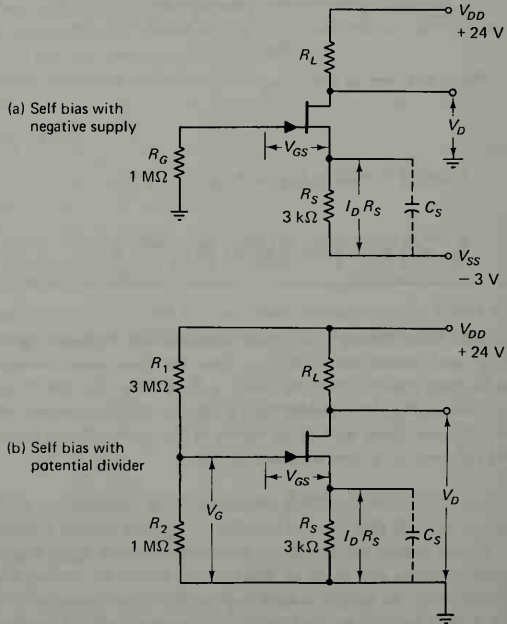
Figure 13-5. Two forms of self-bias with external voltage.

and

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_{GS} = \frac{V_{DD} \times R_2}{R_1 + R_2} - I_D R_S \qquad (13-5)$$

In each case convenient values of I_D can be substituted into the above equations to determine the corresponding V_{GS} levels. These values may then be used to plot the bias lines on the transfer characteristics.

The circuits of Fig. 13-5(a) and (b) use FET's with the maximum and minimum transfer characteristics shown in Fig. 13-6. Draw the bias line for each circuit, and determine $I_{D(max)}$ and $I_{D(min)}$ in each case.

Example 13-4

solution (a)

From Eq. (13-4), when $I_D = 0$, $V_{GS} = V_{SS} = 3$ V. Plot point A on the characteristics (Fig. 13-6) at $I_D = 0$ and $V_{GS} = +3$ V.
When $I_D = 1$ mA, $V_{GS} = 3$ V $- (1$ mA $\times 3$ k$\Omega) = 0$.
Plot point B at $I_D = 1$ mA and $V_{GS} = 0$ V.
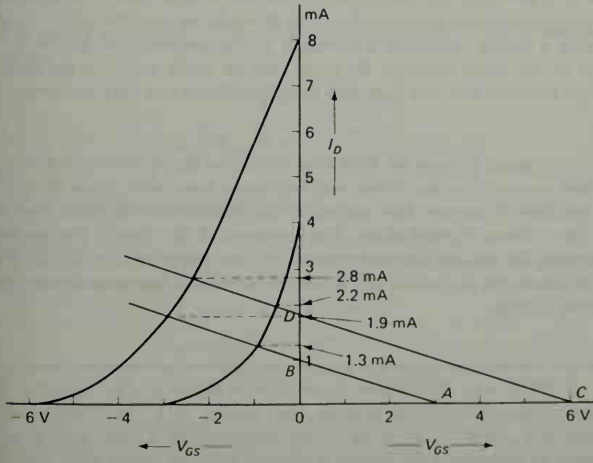
Figure 13-6. $I_{D(max)}$ and $I_{D(min)}$ determination for self-bias circuit with external voltage.

Draw the bias line through points A and B. Where the bias line intersects the transfer characteristics, read $I_{D(\text{max})} = 1.9$ mA and $I_{D(\text{min})} = 1.3$ mA.

solution (b)

From Eq. (13-5), when $I_D = 0$

$$V_{GS} = \frac{24 \text{ V} \times 1 \text{ M}\Omega}{3 \text{ M}\Omega + 1 \text{ M}\Omega}$$
$$= 6 \text{ V}$$

Plot point C on the transfer characteristics at $I_D = 0$ and $V_{GS} = 6$ V. When $I_D = 2$ mA,

$$V_{GS} = \frac{24 \text{ V} \times 1 \text{ M}\Omega}{(3 \text{ M}\Omega + 1 \text{ M}\Omega)} - (2 \text{ mA} \times 3 \text{ k}\Omega) = 0$$

Plot point D at $I_D = 2$ mA and $V_{GS} = 0$ V.
Draw the bias line through points C and D. Where the bias line intersects the transfer characteristics, read $I_{D(\text{max})} = 2.8$ mA and $I_{D(\text{min})} = 2.2$ mA.

It is instructive to compare the results of Example 13-4 to those of Example 13-3. The difference between $I_{D(\text{max})}$ and $I_{D(\text{min})}$ in Example 13-3 is 1.3 mA, while for Example 13-4 the difference is 0.6 mA in each of the two cases. It is seen that the circuits which have an external bias voltage as well as a source resistance maintain I_D within closer limits than the circuit which has only a source resistance. The reason for the improvement is that R_S is larger in the latter example. R_S could also be made larger in the circuit without external bias, but I_D would then be reduced to a very low level.

13-6
Design
of FET Bias
Circuits

The design process for FET bias circuits is simply the reverse of the analysis process. The maximum and minimum acceptable levels of I_D are first specified. These are then marked on the transfer characteristics, and the bias line is drawn through them. The reciprocal of the slope of the bias line determines the value of the source resistance, and the point at which the bias line intersects the horizontal axis of the characteristics indicates the required external voltage.

Example 13-5

A JFET with the transfer characteristics shown in Fig. 13-7 is to be connected in a circuit with a drain load resistor of 4.7 kΩ and a supply voltage of $V_{DD} = 30$ V. V_D is to be approximately 20 V, and is to remain constant to within ±1 V. Design a suitable self-bias circuit with external bias voltage.
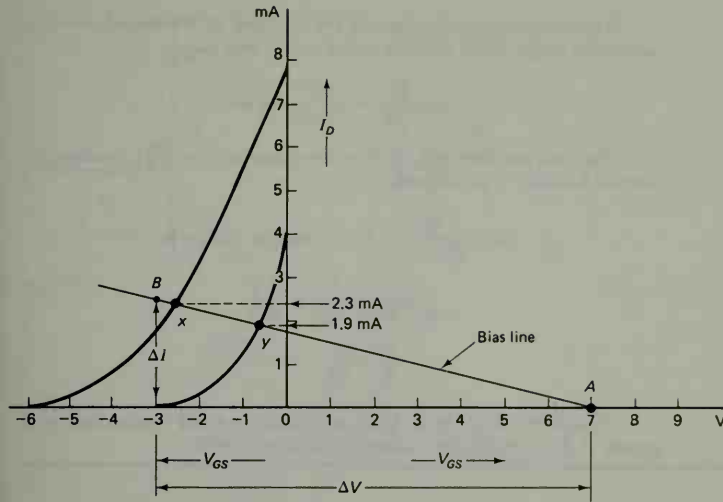
Figure 13-7. Graphical process in bias circuit design.

solution

The circuit is as shown in Fig. 13-5 (b) with different resistance and voltage values.

$$V_D = V_{DD} - I_D R_L$$

$$I_D = \frac{V_{DD} - V_D}{R_L} = \frac{30 \text{ V} - 20 \text{ V}}{4.7 \text{ k}\Omega} \approx 2.1 \text{ mA}$$

For V_D to be constant to within ± 1 V,

$$\Delta I_D = \frac{\pm 1 \text{ V}}{R_L} = \frac{\pm 1 \text{ V}}{4.7 \text{ k}\Omega} \approx \pm 0.2 \text{ mA}$$

$$I_D = (2.1 \pm 0.2) \text{ mA}$$

$$I_{D(\min)} = (2.1 - 0.2) \text{ mA} = 1.9 \text{ mA}$$

$$I_{D(\max)} = (2.1 + 0.2) \text{ mA} = 2.3 \text{ mA}$$

Now mark $I_{D(\max)} = 2.3$ mA (point X) on the maximum transfer characteristic (Fig. 13-7), and $I_{D(\min)} = 1.9$ mA (point Y) on the minimum transfer characteristic. Draw the bias line through these two points, and extend it until it intersects the horizontal axis of the transfer characteristics.

The reciprocal of the slope of the bias line is determined over any convenient range. From points A and B on the bias line,

$$R_S = \frac{\Delta V}{\Delta I} = \frac{10\ \text{V}}{2.5\ \text{mA}} = 4\ \text{k}\Omega$$

The bias line intersects the horizontal axis at $V_G = 7$ V; therefore, an external bias of 7 V is required.

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} \quad \left[\text{see Fig. 13-5(b)}\right]$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_G}{V_{DD}} = \frac{7\ \text{V}}{30\ \text{V}}$$

$$\frac{R_2}{R_1} = \frac{7}{23}$$

R_2 and R_1 should be as large as possible to avoid overloading input signals. If R_2 is 700 kΩ, for example, then $R_1 = 2.3$ MΩ.

**13-7
Biasing
MOSFET'S**

MOSFET biasing is as simple as JFET biasing. In the case of depletion–enhancement devices, the gate–source voltage may be either positive or negative. For enhancement MOSFET's, the gate–source voltage must have the same polarity as the drain supply; i.e., V_{GS} must be positive for an n-channel device and negative for a p-channel FET.

**13-7.1
Fixed Bias
for
MOSFET's**

Consider the two circuits and graphical analysis shown in Fig. 13-8. Both circuits employ a depletion–enhancement device, so V_{GS} may be positive, negative, or zero. The circuit in Fig. 13-8(a) has the device gate grounded via resistor R_G and the source terminal grounded directly. V_{GS} is zero, and the bias line is drawn vertically at $V_{GS} = 0$ on the transfer characteristics in Fig. 13-8(c). $I_{D(\text{max})}$ and $I_{D(\text{min})}$ can be read where the maximum and minimum transfer characteristics cut the bias line.

In the circuit of Fig. 13-8(b), V_{GS} is a positive voltage (V_G) determined by V_{DD} and potential divider R_1 and R_2. To analyze the circuit, a vertical line is drawn on the transfer characteristics at $V_{GS} = V_G$. Again, the maximum and minimum values of I_D are indicated by the intersections of the transfer characteristics and the bias line.

The circuit in Fig. 13-9(a) employs an n-channel enhancement MOSFET. This device must have its gate voltage positive with respect to the source for drain current to flow. Potential divider R_1 and R_2 connected across V_{DD} provides the required V_G. The bias line is drawn vertically on the transfer characteristics [Fig. 13-9(b)] at $V_{GS} = V_G$, and the maximum and minimum levels of I_D are determined as shown.

(a) $V_{GS} = 0$ V

(b) $V_{GS} = +V_G$

(c) Graphical analysis
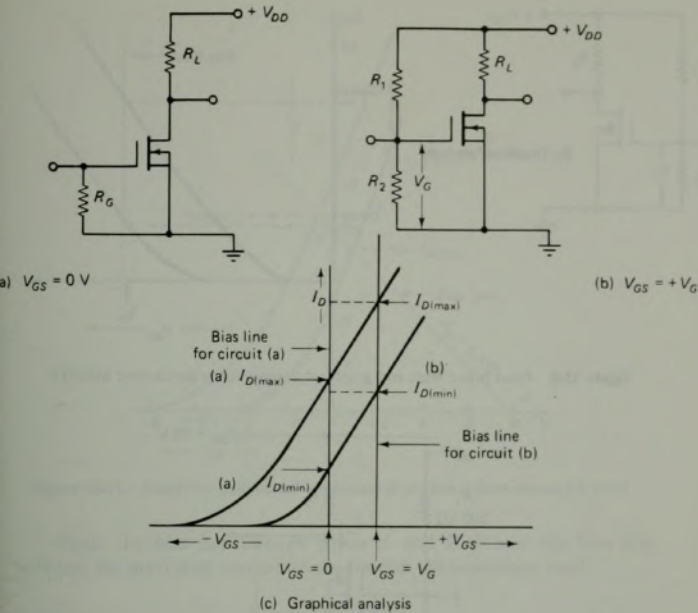
Figure 13-8. Two fixed bias circuits and graphical analysis for depletion-enhancement MOSFET.

The self-bias circuit of Fig. 13-10 is analyzed exactly as was done for the similar JFET circuit.

13-7.2
MOSFET
Self-Bias

The depletion–enhancement MOSFET in the circuit of Fig. 13-10 has the transfer characteristics shown in Fig. 13-11. Determine the maximum and minimum values of I_D for the circuit.

Example 13-6

solution

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$= \frac{20 \text{ V} \times 200 \text{ k}\Omega}{300 \text{ k}\Omega + 200 \text{ k}\Omega} = 8 \text{ V}$$

$$V_{GS} = V_G - I_D R_S$$
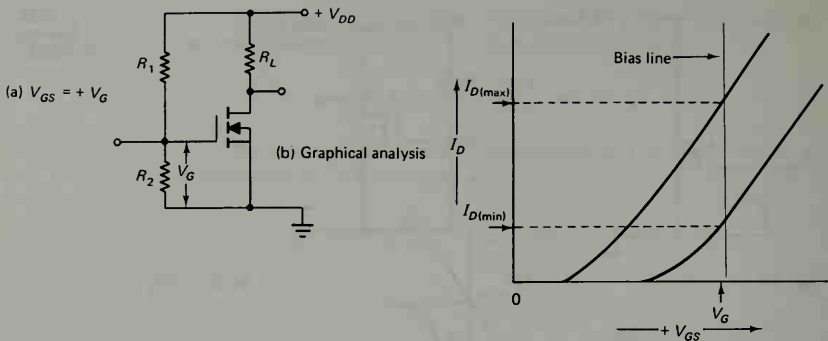
Figure 13-9. Fixed bias circuit and graphical analysis for enhancement MOSFET.
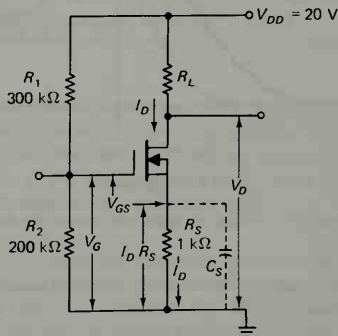
Figure 13-10. Depletion–enhancement MOSFET with self-bias and external bias voltage.

When $I_D = 0$,

$$V_{GS} = 8 \text{ V} - 0 = 8 \text{ V}$$

Plot point A on the transfer characteristics at $I_D = 0$ and $V_{GS} = 8$ V.
When $V_{GS} = 0$

$$0 = 8 \text{ V} - (I_D \times 1 \text{ k}\Omega)$$

$$I_D = \frac{8 \text{ V}}{1 \text{ k}\Omega} = 8 \text{ mA}$$

Plot point B on the characteristics at $V_{GS} = 0$ and $I_D = 8$ mA.

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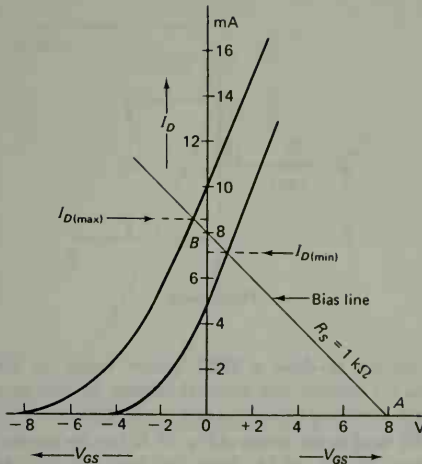
Figure 13-11. Graphical analysis for self-biased depletion–enhancement MOSFET

Draw the bias line through points A and B. Where the bias line intersects the maximum and minimum transfer characteristics, read

$$I_{D(max)} = 8.5 \text{ mA}$$
$$I_{D(min)} = 7.2 \text{ mA}$$

Fixed bias. Circuit in which the source is grounded and a constant bias voltage is applied to the gate.

Self-bias. Circuit in which the gate is grounded via a high resistance, and a resistance is included in series with the source.

Self-bias with external voltage. Circuit with source resistance and a fixed level of gate–source voltage greater than zero.

Bias line. Line drawn upon transfer characteristics to define all possible bias conditions.

Glossary of Important Terms

13-1. A common source amplifier has $V_{DD} = 20$ V and $R_L = 3.9$ kΩ. If the FET used has the drain characteristics shown in Fig. 12-12, draw the dc load line and determine a suitable value of gate bias voltage.

Problems

13-2. The FET used in the circuit of Fig. 13-12 has the maximum and minimum transfer characteristics shown in Fig. 13-11. Draw bias lines for (a) $V_G = -1$ V, and (b) $V_G = +1$ V. In each case determine the levels of $I_{D(max)}$, $I_{D(min)}$, $V_{D(max)}$, and $V_{D(min)}$.
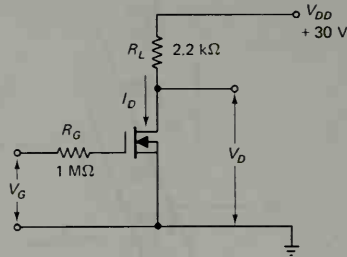
Figure 13-12.

13-3. Draw circuits to show a JFET circuit using (a) fixed bias, (b) self-bias, (c) self-bias with external voltage. In each case include the necessary bypassing capacitors and briefly explain.

13-4. The FET used in the circuit of Fig. 13-13 has the transfer characteristics shown in Fig. 13-14. Draw the bias line and determine the maximum and minimum levels of I_D. Also calculate the maximum and minimum levels of V_D and V_{DS}.

13-5. The circuit in Problem 13-4 is to be redesigned to give I_D within the limits of 1 to 1.3 mA. Draw the new bias line and determine the new value for R_S and the new ratio for R_2/R_1.

13-6. Determine the maximum and minimum values of V_D for the circuit of Fig. 13-15. The FET transfer characteristics are shown in Fig. 13-16.
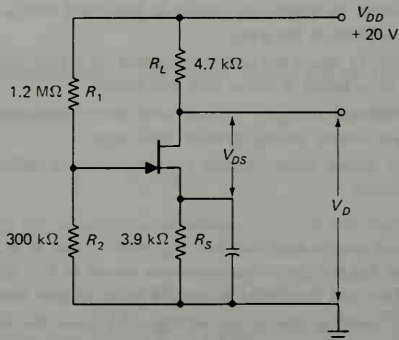
Figure 13-13.
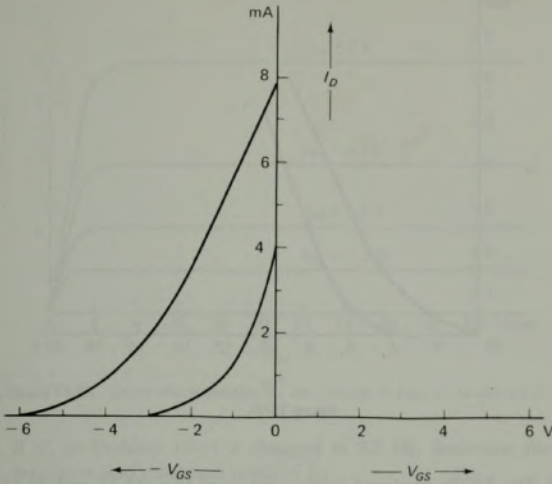
Figure 13-14.

13-7. The FET used in the circuit of Fig. 13-17 has the transfer characteristics shown in Fig. 13-14. Determine maximum and minimum levels of I_D and V_D.

13-8. The self-bias circuit of Fig. 13-3 is to be redesigned to give I_D within the limits of 0.5 to 1.5 mA. If the FET used has the transfer characteristics shown in Fig. 13-14, draw the bias line and determine the new value for R_S.
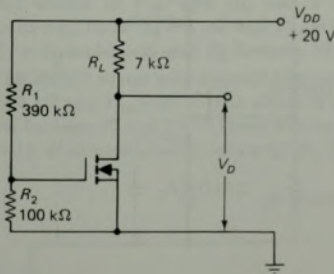
Figure 13-15.
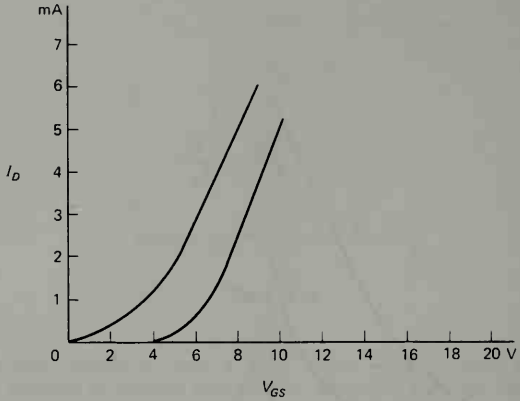
Figure 13-16.

13-9. The FET's employed in the circuits of Figs. 13-13 and 13-17 have typical drain characteristics as shown in Fig. 13-18. Construct the dc load line for each circuit. Note that the total dc load is $R_L + R_S$.

13-10. Determine the maximum and minimum levels of V_{DS} when the gate bias voltage in Example 13-2 is changed to -1.5 V.

13-11. A self-bias circuit uses a JFET with the transfer characteristics shown in Fig. 13-14. If $R_S = 3.9$ kΩ, $R_L = 5.6$ kΩ, and $V_{DD} = 20$ V, determine the maximum and minimum levels of V_D.
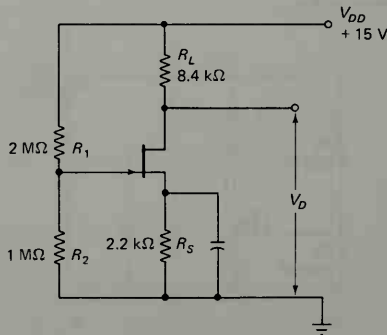
Figure 13-17.
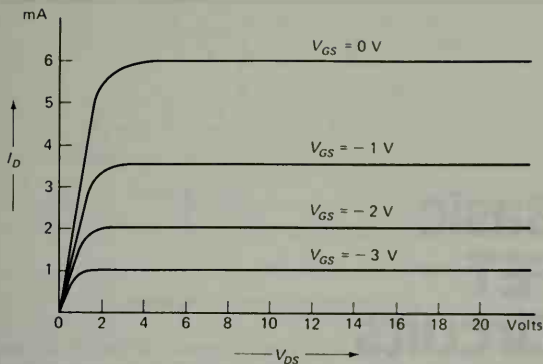
Figure 13-18. Drain characteristics for the circuits in Figs. 13-13 and 13-17.

13-12. If R_S in Problem 13-11 is changed to 2.7 kΩ, determine the new maximum and minimum levels of V_D.

13-13. A FET circuit using self-bias with external voltage (circuit as in Fig. 13-13) has $R_L = 3.3$ kΩ, $R_S = 3.3$ kΩ, $R_1 = 1$ MΩ, $R_2 = 130$ kΩ, and $V_{DD} = 25$ V. The FET transfer characteristics are as shown in Fig. 13-14. Determine the maximum and minimum levels of V_D.

13-14. Determine the new maximum and minimum levels of V_D when the JFET is replaced by a MOSFET with the characteristics in Fig. 13-11, (a) in the circuit of Problem 13-4; (b) in the circuit of Problem 13-7.

13-15. The circuit of Fig. 13-10 is to be redesigned to have V_D between 15 and 18 V. R_L is to be changed to 6 kΩ. Using the transfer characteristics in Fig. 13-14, determine suitable new values for R_1, R_2, and R_S.

13-16. The MOSFET circuit in Fig. 13-8 (b) uses a device with the characteristics in Fig. 13-11. $R_L = 1$ kΩ and $V_{DD} = 24$ V. Determine the ratio of R_2 to R_1 which will give V_D between 10 and 15 V.

13-17. A self-biased MOSFET circuit with external bias (as in Fig. 13-10) is to have $R_L = 3.3$ kΩ and $V_{DD} = 30$ V. The circuit is to be designed to give a V_D level between 20 and 23 V. Using the transfer characteristics in Fig. 13-11, determine suitable values for R_1, R_2, and R_S.

Basic
FET
Circuits

14-1
Introduction

There are three basic FET configurations: *Common source*, *common drain*, and *common gate*. These are similar to the three bipolar transistor circuits. Of the three, the common source circuit is the most frequently used because of its good voltage amplification and high input impedance. The common drain and common gate circuits are applied as buffer amplifiers and high-frequency voltage amplifiers, respectively.

14-2
The Common
Source
Circuit

The *common source circuit* is the FET equivalent of the bipolar transistor common emitter circuit and the vacuum-tube common cathode circuit. Like its transistor and tube equivalents, the common source circuit is used very frequently because of its good voltage amplification. Figure 14-1 shows an n-channel JFET connected as a common source amplifier. The gate is biased negative with respect to the source by voltage $-V_G$ which is connected via the gate resistance R_G. The load resistance R_L is connected in series with the drain and the supply voltage V_{DD}. Input signals are capacitively coupled to
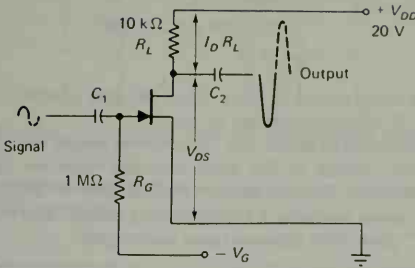
Figure 14-1. Common source amplifier.

the gate via C_1, and the output is taken from the drain via C_2. The source terminal is common to both input and output.

To study the operation of the circuit, assume that the gate bias voltage V_G is such that $I_D = 1$ mA. Also let the transconductance of the FET be

$$g_m = 5000 \ \mu S$$

The voltage drop across $R_L = I_D R_L = 1 \ \text{mA} \times 10 \ \text{k}\Omega = 10 \ \text{V}$, and the drain to source voltage is $V_{DS} = V_{DD} - (I_D R_L) = 20 \ \text{V} - 10 \ \text{V} = 10 \ \text{V}$.

If a $+0.1$ V signal is now applied to the gate, the gate negative bias is decreased by 0.1 V, the depletion region penetration is reduced, and I_D is increased. The new value of I_D is

$$I_D = 1 \ \text{mA} + (g_m \times \Delta V_{GS})$$
$$= 1 \ \text{mA} + (5000 \times 10^{-6} \times 0.1)$$
$$= 1 \ \text{mA} + 0.5 \ \text{mA} = 1.5 \ \text{mA}$$

The new value of drain voltage is

$$V_D = V_{DD} - I_D R_L$$
$$= 20 - (1.5 \ \text{mA} \times 10 \ \text{k}\Omega) = 5 \ \text{V}$$

Thus, an input signal of $+0.1$ V at the gate causes V_D to decrease from 10 V to 5 V; an output change of -5 V.

Similarly, if an input signal of -0.1 V is applied to the gate, the gate negative bias is increased by 0.1 V, the depletion regions penetrate deeper into the channel, and I_D is decreased.

I_D then becomes

$$I_D = 1 \ \text{mA} + (g_m \times \Delta V_G)$$
$$= 1 \ \text{mA} + (5000 \times 10^{-6} \times -0.1)$$
$$= 1 \ \text{mA} - 0.5 \ \text{mA} = 0.5 \ \text{mA}$$

and
$$V_D = V_{DD} - I_D R_L$$
$$= 20 - (0.5 \text{ mA} \times 10 \text{ k}\Omega)$$
$$= 15 \text{ V}$$

Now, an input signal of -0.1 V on the gate caused V_D to increase from 10 to 15 V, an output change of $+5$ V.

The above analysis shows that the common source circuit provides an amplified output voltage at the drain terminal when an input signal is applied to the gate. It also shows, as illustrated in Fig. 14-1, that a positive-going signal produces a negative-going output, and vice versa; i.e., there is a 180° phase shift between input and output.

14-3
AC Analysis
of Common
Source
Circuit

14-3.1
*Equivalent
Circuit*

To draw the ac equivalent circuit for the common source amplifier of Fig. 14-1, the supply voltages and capacitors are replaced with short circuits, and the device is replaced with its own ac equivalent circuit. Using the FET low-frequency equivalent circuit from Fig. 12-14, the common source amplifier equivalent circuit is shown in Fig. 14-2.

14-3.2
*Voltage
Gain*

From Fig. 14-2,

$$\text{Output voltage} = I_d \times (r_d \| R_L)$$
$$= I_d \times \frac{r_d \times R_L}{r_d + R_L}$$
and
$$I_d = -g_m V_i$$
$$V_o = -g_m V_i \times \frac{r_d \times R_L}{r_d + R_L}$$
$$\text{Voltage gain} = A_v = \frac{V_o}{V_i} = \frac{-g_m r_d R_L}{r_d + R_L} \qquad (14\text{-}1)$$

If, as frequently is the case, $r_d \gg R_L$, then $r_d + R_L \approx r_d$, and Eq. (14-1) becomes

$$A_o \approx \frac{-g_m r_d R_L}{r_d}$$
or
$$A_v \approx -g_m R_L \qquad (14\text{-}2)$$
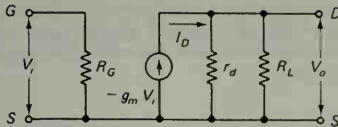
Figure 14-2. AC equivalent circuit for common source amplifier.

This is an approximate expression for common source voltage gain which may be useful occasionally.

The common source amplifier shown in Fig. 14-1 uses a 2N5457 FET. Calculate the typical value of circuit voltage gain.   **Example 14-1**

solution

From Fig. 12-9,

$$r_d = \frac{1}{|Y_{os}|} = \frac{1}{10 \times 10^{-6}} = 100 \text{ k}\Omega$$

$$g_m = |Y_{fs}| = 3000 \ \mu\text{S}$$

From Eq. (14-1),

$$A_v = \frac{-g_m r_d R_L}{r_d + R_L}$$

$$= \frac{-3000 \times 10^{-6} \times 100 \times 10^3 \times 10 \times 10^3}{(100 \times 10^3) + (10 \times 10^3)} = -27.3$$

Using Eq. (14-2),

$$A_v \approx -g_m R_L$$

$$= -3000 \times 10^{-6} \times 10 \times 10^3 = -30$$

At low frequencies, the output impedance is simply   **14-3.3**
                                                                        Output
$$Z_o = R_L \| r_d \approx R_L \qquad (14-3)$$ **Impedance**

At high frequencies, R_L and r_d are shunted by the drain–source capacitance C_{ds}.

Example 14-2   For the circuit of Fig. 14-1, $r_d = 100$ kΩ and $C_{DS} = 3$ pF. Calculate the low-frequency output impedance, and determine the output impedance at a signal frequency of 1 MHz.

solution

Low-frequency output impedance:

$$Z_o = \frac{100 \text{ k}\Omega \times 10 \text{ k}\Omega}{100 \text{ k}\Omega + 10 \text{ k}\Omega} = 9.09 \text{ k}\Omega$$

$$X_c = \frac{1}{2\pi f C_{DS}}$$

At $f = 1$ MHz,

$$X_c = \frac{1}{2\pi \times 1 \times 10^6 \times 3 \times 10^{-12}} = 53 \text{ k}\Omega$$

$$Z_o = R_o \| X_c$$

$$= \frac{R_o \times X_c}{\sqrt{R_o^2 + X_c^2}} \qquad (R_o \text{ is resistive and } X_c \text{ is reactive})$$

$$|Z_o| = \frac{9.09 \text{ k}\Omega \times 53 \text{ k}\Omega}{\left[(9.09 \text{ k}\Omega)^2 + (53 \text{ k}\Omega)^2 \right]^{1/2}} = 8.96 \text{ k}\Omega$$

14-3.4
Input
Impedance

At low frequencies, the input impedance Z_i is the bias resistance R_G. To be strictly correct, $Z_i = R_G \| R_{GS}$, but since R_{GS} is usually very much greater than the bias resistance,

$$Z_i \approx R_G \tag{14-4}$$

At higher frequencies, the input capacitance shunting R_G becomes effective. It is important to note that the actual capacitance presented to an input signal is amplified by the *Miller effect* (see Section 8-5), just as in the case of bipolar transistor and vacuum-tube circuits.

$$C_{in} = C_{gs} + (1 + A_o)C_{gd}$$

where A_v is the circuit voltage gain $g_m(R_L \| r_d)$.

$$C_{in} = C_{gs} + \left[1 + g_m(R_L \| r_d) \right] C_{gd} \tag{14-5}$$

The input resistance is usually much larger than the signal source resistance. Consequently, when the input frequency is increased until $X_{C_{in}}$ is

several times the signal source resistance, the signal is potentially divided across $X_{C_{in}}$ and the signal source resistance, and the overall amplifier gain begins to be reduced.

The common source amplifier in Fig. 14-1 uses a 2N5457 FET. Calculate the typical value of input capacitance for the amplifier.

Example 14-3

solution

Using typical parameters from Fig. 12-9 for the 2N5457 FET,

$$C_{iss} = 4.5 \text{ pF} \quad \text{and} \quad C_{rss} = C_{gd} = 1.5 \text{ pF}$$
$$C_{iss} = C_{rss} + C_{gs}$$
$$C_{gs} = C_{iss} - C_{rss} = 4.5 \text{ pF} - 1.5 \text{ pF} = 3 \text{ pF}$$
$$r_d = \frac{1}{Y_{os}} = \frac{1}{10 \times 10^{-6}} = 100 \text{ k}\Omega$$
$$g_m = |Y_{fs}| = 3000 \text{ } \mu\text{S}$$

From Eq. (14-5),

$$C_{in} = C_{gs} + \left[1 + g_m (R_L \| r_d) \right] C_{gd}$$
$$= 3 \text{ pF} + \left[1 + (3 \times 10^{-3})(10 \text{ k}\Omega \| 100 \text{ k}\Omega) \right] 1.5 \text{ pF}$$
$$= 45.4 \text{ pF}$$

In the *common drain amplifier*, also called the *source follower*, the load resistance (R_L) is in series with the source terminal as shown in Fig. 14-3. This circuit is the FET equivalent of the common collector bipolar transistor circuit and the vacuum-tube common plate circuit. In the circuit of Fig. 14-3, the gate bias voltage V_G is *not* equal to the gate–source voltage V_{GS}. Instead

$$V_G = V_{GS} + V_{R_L} = V_{GS} + I_D R_L$$

Assume that $I_D = 1$ mA, $V_{GS} = -2$ V, and $g_m = 5000$ μS:

$$I_D R_L = 1 \text{ mA} \times 10 \text{ k}\Omega = 10 \text{ V}$$

and

$$V_G = -2 \text{ V} + 10 \text{ V} = 8 \text{ V}$$

Note that the gate is 8 V above ground level, and the source terminal is
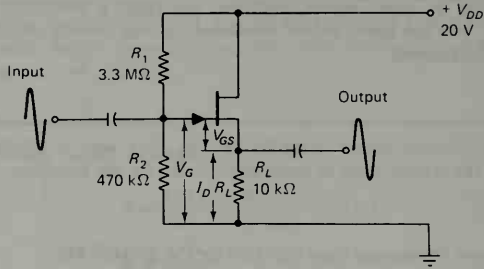
Figure 14-3. Common drain amplifier.

10 V above ground. Consequently, the source is 2 V more positive than the gate; i.e., the gate–source bias is -2 V.

The dc conditions are now established as

$$I_D = 1 \text{ mA}, \qquad V_S = 10 \text{ V}, \qquad V_G = 8 \text{ V}$$

Now calculate the input voltage necessary to produce a $+1$ V change in the output voltage: The new value of voltage at the FET gate is $V_G + V_i$, where V_i is the signal voltage. The new value of V_{R_L} is $(I_D + \Delta I_D) \times 10$ kΩ and $V_{R_L} = 10$ V $+ 1$V $= 11$V. Thus, 11 V $= (I_D + \Delta I_D) \times 10$ kΩ.

$$\Delta I_D = \frac{11 \text{ V}}{10 \text{ k}\Omega} - I_D = 0.1 \text{ mA}$$

and

$$\Delta I_D = g_m \times \Delta V_{GS}$$

$$\Delta V_{GS} = \frac{\Delta I_D}{g_m}$$

$$\Delta V_{GS} = \frac{0.1 \text{ mA}}{5000 \times 10^{-6}} = 0.02 \text{ V}$$

and

$$V_G + V_i = (V_{GS} + \Delta V_{GS}) + (I_D + \Delta I_D) R_L$$

$$8 \text{ V} + V_i = (-2 \text{ V} + 0.02 \text{ V}) + (1 \text{ mA} + 0.1 \text{ mA}) \, 10 \text{ k}\Omega$$

$$V_i = -1.98 \text{ V} + 11 \text{ V} - 8 \text{ V} = +1.02 \text{ V}$$

Therefore, to produce an output change of $+1$ V required an input change of $+1.02$ V. Thus, the common drain amplifier has a voltage gain of approximately 1 and no phase shift between input and output (Fig. 14-3). It can also be said that output voltage changes approximately follow the input voltage changes, hence the name *source follower*.

As in the case of the common source circuit, the ac equivalent circuit for the common drain amplifier is drawn by replacing supply voltages and capacitors with short circuits, and replacing the device with its own ac equivalent circuit. The common drain equivalent circuit is shown in Fig. 14-4. Note that the current generator is $g_m V_{gs}$, where $V_{gs} = V_i - V_o$. Also note that R_G is R_1 in parallel with R_2 (see Fig. 14-3).

From Fig. 14-4,

$$V_o = I_d \times (r_d \| R_L)$$

$$= I_d \times \frac{r_d \times R_L}{r_d + R_L}$$

and

$$I_d = g_m V_{gs} = g_m (V_i - V_o)$$

Therefore,

$$V_o = g_m (V_i - V_o) \frac{r_d \times R_L}{r_d + R_L}$$

Solving for V_o,

$$V_o (r_d + R_L) = g_m V_i r_d R_L - g_m V_o r_d R_L$$

$$V_o (r_d + R_L + g_m r_d R_L) = g_m V_i r_d R_L$$

$$V_o = g_m V_i \frac{r_d R_L}{r_d + R_L + g_m r_d R_L} \qquad (14\text{-}6)$$
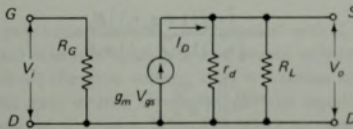
Figure 14-4. AC equivalent circuit for common drain amplifier.

315

The voltage gain is

$$A_v = \frac{V_o}{V_i} = g_m \frac{r_d R_L}{r_d + R_L + g_m r_d R_L} \tag{14-7}$$

If $g_m r_d R_L \gg (r_d + R_L)$, $A_v \approx 1$.

Example 14-4

The common drain amplifier in Fig. 14-3 uses a 2N5457 FET. Calculate the typical value of circuit voltage gain.

solution

From Fig. 12-9,

$$r_d = \frac{1}{|Y_{os}|} = 100 \text{ k}\Omega$$

$$g_m = |Y_{fs}| = 3000 \text{ }\mu\text{S}$$

From Eq. (14-7),

$$A_v = \frac{3000 \times 10^{-6} \times 100 \times 10^3 \times 10 \times 10^3}{(100 \times 10^3) + (10 \times 10^3) + (3000 \times 10^{-6} \times 100 \times 10^3 \times 10 \times 10^3)}$$

$$= 0.965$$

**14-5.3
Output
Impedance**

Consider Eq. (14-6):

$$V_o = g_m V_i \frac{r_d R_L}{r_d + R_L + g_m r_d R_L}$$

$g_m V_i$ is an output current directly proportional to V_i, and $(r_d R_L)/(r_d + R_L + g_m r_d R_L) = $ a resistance, Z_o.

This can be rewritten

$$Z_o = \frac{r_d R_L}{r_d + R_L(1 + g_m r_d)}$$

$$= \frac{\left[r_d/(1 + g_m r_d) \right] R_L}{\left[r_d/(1 + g_m r_d) \right] + R_L}$$

$$= R_L \left\| \frac{r_d}{1 + g_m r_d} \right.$$

$$\approx R_L \left\| \frac{1}{g_m} \right. \tag{14-8}$$
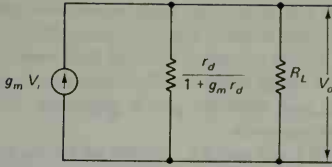
Figure 14-5. Modified equivalent circuit for common drain amplifier.

Using this knowledge, a modified equivalent circuit (Fig. 14-5) can be drawn for the common drain amplifier.

The common drain amplifier of Fig. 14-3 has a FET with $r_d = 100$ kΩ $g_m = 3000$ μS. Calculate the circuit output impedance.

Example 14-5

solution

$$\frac{r_d}{1 + g_m r_d} = \frac{100 \times 10^3}{1 + (3000 \times 10^{-6} \times 100 \times 10^3)} = 332 \ \Omega$$

From Eq. (14-8)

$$Z_o = 10 \text{ k}\Omega \| 332 \ \Omega$$

$$= \frac{10 \text{ k}\Omega \times 332 \ \Omega}{10 \text{ k}\Omega + 332 \ \Omega} = 322 \ \Omega$$

Just as was the case in the common source circuit, the bias resistances constitute the input resistance for a common drain amplifier. For the circuit in Fig. 14-3 the input resistance is

14-5.4
Input
Impedance

$$Z_i = R_1 \| R_2 \qquad (14-9)$$

The drain–gate capacitance C_{gd} is in parallel with Z_i. The gate–source capacitance C_{gs} still exists between gate and source terminals, but since the source voltage follows the gate voltage, only a fraction of the input signal appears across the gate–source terminals. All the signal voltage appears across C_{gd}, however, so C_{gs} has a negligible effect by comparison with C_{gd}. The input capacitance begins to affect the circuit gain when $X_{C_{gd}}$ is reduced to several times the signal source impedance.

In the *common gate circuit*, the input signal is applied to the source terminal, and the output is taken from the drain. The circuit in Fig. 14-6 also shows that the gate is grounded, that the load resistance R_L is in series with the drain, and a source resistance R_S is included. A signal voltage V_i is developed across R_S, and since the gate is grounded, V_i is also developed across the gate source terminals.

Assume an I_D of 1 mA and a g_m of 5000 μS for the circuit of Fig. 14-6. The drain voltage is

$$V_D = V_{DD} - (I_D R_L)$$
$$= 20 \text{ V} - (1 \text{ mA} \times 10 \text{ k}\Omega) = 10 \text{ V}$$

The voltage drop across R_S is

$$V_S = I_D \times R_S$$
$$= 1 \text{ mA} \times 1 \text{ k}\Omega = 1 \text{ V}$$

This means that the source terminal is 1V positive with respect to ground, or to put it another way, ground is -1V with respect to the source terminal. Since the gate is grounded, it is also -1V with respect to the source terminal; i.e., the gate–source voltage $V_{GS} = -1$V.

If an input signal of $+0.1$ V is now applied to the source, the voltage drop across R_S becomes 1.1 V. V_{GS} also becomes -1.1 V; i.e., V_{GS} is changed by -0.1 V. This causes I_D to be reduced. The new value of I_D is

$$I_D = 1 \text{ mA} - (g_m \times \Delta V_{GS})$$
$$= 1 \text{ mA} - (5000 \times 10^{-6} \times 0.1)$$
$$= 1 \text{ mA} - 0.5 \text{ mA}$$
$$= 0.5 \text{ mA}$$
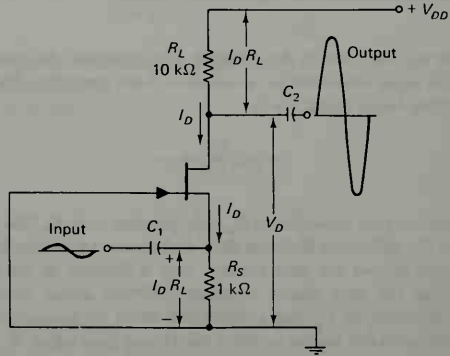
Figure 14-6. Common gate amplifier.

The new value of drain voltage is

$$V_D = V_{DD} - I_D R_L$$
$$= 20 - (0.5 \text{ mA} \times 10 \text{ k}\Omega)$$
$$= 15 \text{ V}$$

Thus, an input signal of $+0.1$ V at the source caused V_D to increase from 10 to 15 V, i.e., a change of $+5$ V. Similarly, it can be shown that an input of -0.1 V will cause the drain voltage to be reduced from 10 to 5 V.

From the above analysis it is seen that the common gate circuit provides voltage amplification, and that the output voltage at the drain is in phase with the input voltage at the source. Another very important point is that since I_D flows through the source as well as the drain, the signal voltage source has to supply the I_D changes. As will be seen, this gives the common gate circuit a very low input impedance.

14-7
AC Analysis
of the
Common
Gate Circuit

Replacing supply voltages and capacitors with short circuits gives the ac equivalent circuit in Fig. 14-7(a). Substituting the device equivalent circuit gives the complete ac equivalent circuit shown in Fig. 14-7(b). Note that the current source ($g_m V_{gs}$) is connected between the drain and the source terminals, as always. However, since the source and the drain are the input and output terminals, respectively, for the common gate circuit, ($g_m V_{gs}$) appears between the input and the output.

14-7.1
*Equivalent
Circuit*

The output voltage is

14-7.2
*Voltage
Gain*

$$V_o = I_d \times (r_d \| R_L)$$
$$= I_d \times \frac{r_d \times R_L}{r_d + R_L}$$

and

$$I_d = g_m V_{gs} = g_m V_i$$

$$V_o = g_m V_i \times \frac{r_d R_L}{r_d + R_L}$$

The voltage gain is

$$A_o = \frac{g_m r_d R_L}{r_d + R_L} \qquad (14\text{-}10)$$
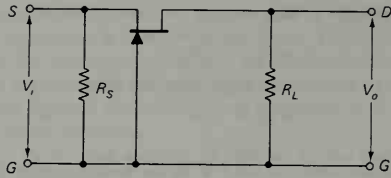
(a) ac equivalent circuit
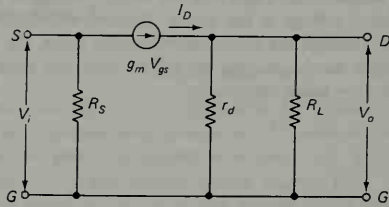
(b) Complete ac equivalent circuit

Figure 14-7. AC equivalent circuits for common gate circuit.

This is the same as the voltage gain equation for the common source amplifier, except that the gain is a positive quantity. The absence of a minus sign from the gain formula indicates that V_o is in phase with V_i, as shown in Fig. 14-6.

Example 14-6

The common gate amplifier in Fig. 14-6 uses a 2N5457 FET. Calculate the typical value of circuit voltage gain.

solution

The calculation is exactly the same as for Example 14-1, except for the sign change.

$$A_v = \frac{g_m r_d R_L}{r_d + R_L} = 27.3 \quad \text{(see Example 14-1)}$$

14-7.3 Output Impedance

Referring to the ac equivalent circuit in Fig. 14-7(b), note that the common gate output impedance is R_L in parallel with r_d.

$$Z_o = R_L \| r_d \approx R_L \tag{14-11}$$

Z_o is, of course, the low-frequency output impedance. At high frequencies, this will be modified by the parallel capacitance C_{gd}.

The ac equivalent circuit of Fig. 14-7(b) shows that, ignoring the current through R_S, the input current is I_d.

$$I_d = g_m V_{gs} = g_m V_i$$

Thus, the input impedance to the device source terminal is $V_i/I_d = V_i/g_m V_i = 1/g_m$.

The circuit input impedance is

$$Z_i = \frac{1}{g_m} \bigg|\bigg| R_S \qquad (14\text{-}12)$$

Actually, R_L and r_d can be shown to be involved in R_i, but the difference is quite negligible.

Calculate the input resistance for the common gate amplifier in Fig. 14-6. Assume that the device is a 2N5457.

Example 14-7

solution

From the data sheet for the 2N5457 (Fig. 12-9),

$$g_m = |Y_{fs}| = 3000 \ \mu S$$

or

$$\frac{1}{g_m} = \frac{1}{3000 \times 10^{-6}} = 333 \ \Omega$$

From Eq. (14-12),

$$Z_i = \frac{1}{g_m} \bigg|\bigg| R_S$$

$$= \frac{333 \times 1 \ k\Omega}{333 + 1 \ k\Omega} = 250 \ \Omega$$

The common gate amplifier has a very low input impedance which requires that the signal have an even lower source impedance. With the common source circuit, the Miller effect amplifies the input capacitance and limits the high-frequency response. Miller effect occurs only where the output voltage is antiphase to the input. Where the output is in phase with the input, as in the common gate circuit, the capacitance between input and

output terminals tends to be reduced instead of amplified. The only input capacitance of any importance is the gate source capacitance C_{gs}. This low input capacitance gives the common gate circuit a much better high-frequency response than the common source circuit.

14-8
BI-FET and BI-MOS Circuits

The major advantage of FET's over bipolar transistors is the very high input resistance of the FET. In the case of JFET's and ordinary MOSFET's, i.e., not V-FETs, the gain of a single stage is considerably less than that of a bipolar single-stage amplifier. For a bipolar stage, $A_v = 200$ to 500, typically. For a FET, $A_v = g_m R_L$. With a typical g_m of 4 mS and $R_L = 10$ kΩ, $A_v = 40$. (For a V-FET, g_m could easily be 100 mS, giving $A_v = 1000$.)

Field effect transistors are frequently combined with bipolar stages to give multistage circuits which have a very high input resistance. Where JFET's are combined with bipolars, the circuits are known as BI-FET circuits. When MOSFET's and bipolars are combined, the name BI-MOS is applied. Several BI-FET and BI-MOS amplifier circuits are illustrated in Figs. 14-8 through 14-10.

Figure 14-8 shows a self-biased JFET stage capacitor coupled to a common emitter stage with emitter current bias. The circuit has a very high input resistance and an overall voltage gain less than that of a two-stage bipolar circuit.
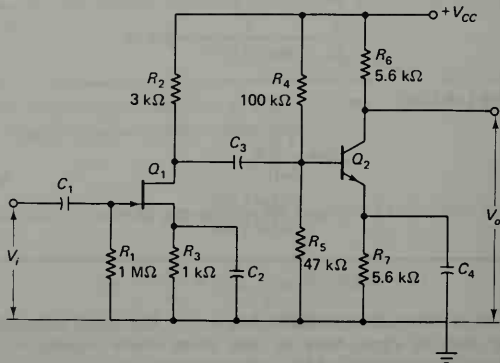
Figure 14-8. Two-stage BI-FET amplifier.
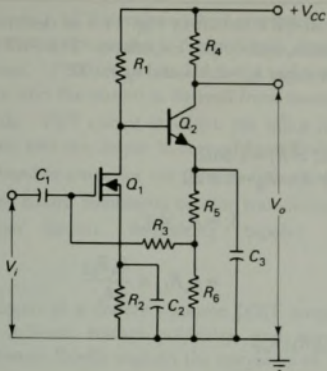
Figure 14-9. BI-MOS DC feedback pair.
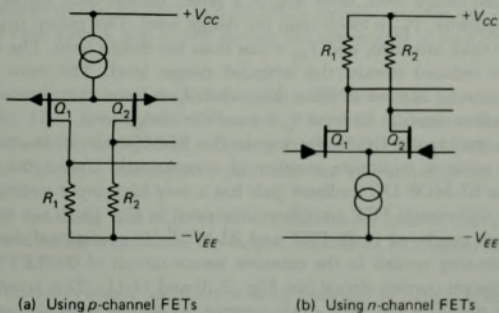
(a) Using p-channel FETs   (b) Using n-channel FETs

Figure 14-10. Differential FET input stages used in BI-FET operational amplifiers.

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Example 14-8

Analyze the BI-FET circuit in Fig. 14-8 to determine overall voltage gain, input impedance, and output impedance. The FET has $g_m = 5$ mS, and the bipolar transistor has $h_{ie} = 2$ kΩ and $h_{fe} = 100$.

solution

Input impedance $Z_i' \simeq R_1 = 1$ MΩ.
Output impedance $Z_o \simeq R_6 = 5.6$ kΩ.

$$A_v = A_{v1} \times A_{v2}$$

$$= g_m R_{L1} \times \frac{h_{fe} R_{L2}}{h_{ie}}$$

where $R_{L1} = R_2 \| R_4 \| R_S \| h_{ie2}$.

$$A_v = 5 \text{ mA/V} [3 \text{ kΩ} \| 100 \text{ kΩ} \| 47 \text{ kΩ} \| 2 \text{ kΩ}] \times \frac{100 \times 5.6 \text{ kΩ}}{2 \text{ kΩ}}$$

$$\simeq 1600$$

The circuit in Fig. 14-9 is a BI-MOS version of the *DC feedback pair* explained in Section 9-3. Q_1 is self-biased with an external gate voltage derived from the emitter resistances (R_5 and R_6) of Q_2. The base of Q_2 is directly connected to the drain terminal of Q_1. If I_{D1} becomes greater than the intended design level, there will be a larger voltage drop across R_1 and R_2. Consequently, V_{B2} is lower than the design level. This means that V_{G1} is also lower than intended, and V_{GS} is less than the design level. The result is that I_D is reduced toward the intended design level. The same line of reasoning can be applied to show that, when I_D is lower than intended, the feedback effect tends to increase I_D toward the design level.

Like the bipolar DC feedback pair, this BI-MOS circuit is a two-stage amplifier using a minimum number of components. Unlike the bipolar circuit, the BI-MOS DC feedback pair has a very high input resistance.

The differential FET amplifiers illustrated in Fig. 14-10 are typical of input stages employed in BI-FET and BI-MOS IC operational amplifiers. The double-ring symbol in the common source circuit of the FET's represents a constant current circuit (see Figs. 9-10 and 11-11). This arrangement internally stabilizes the FET drain current no matter what the gate bias voltage (within limits).

Basically, one of these FET differential circuits is connected as an additional stage preceding a bipolar operational amplifier like that shown in Fig. 9-8. Again, the FET's are employed essentially for the very high input resistance; however, improved slew rates and better frequency responses also result.

Common source circuit. FET circuit in which the input is applied between gate and source, and the output is derived from drain and source.

Common drain circuit. FET circuit in which the input is applied between gate and drain, and the output is derived from source and drain.

Common gate circuit. FET circuit in which the input is applied between source and gate, and the output is derived from drain and gate.

Source follower. Another name for the *common drain amplifier*.

BI-FET. Multistage circuit combining bipolar transistors with JFET's.

BI-MOS. Multistage circuit combining bipolar transistors with MOSFET's.

Glossary of Important Terms

14-1. Sketch the circuit of a common source JFET amplifier. Identify all components, indicate voltage polarities, and show the input and output waveforms. Briefly explain the operation of the circuit.

14-2. Draw the ac equivalent circuit for a common source amplifier, and derive expressions for common source voltage gain and output impedance.

14-3. Repeat Question 14-1 for a common drain amplifier.

14-4. Draw the ac equivalent circuit for a common drain amplifier, and derive expressions for voltage gain and output impedance.

14-5. Repeat Question 14-1 for a common gate amplifier.

14-6. Draw the ac equivalent circuit for a common gate amplifier, and derive expressions for voltage gain, output impedance, and input impedance.

14-7. Sketch typical BI-FET and BI-MOS circuits, explain the operation of each circuit, and briefly discuss the advantages of such circuits.

Review Questions

14-1. A common source amplifier using a 2N5458 FET (specification in Fig. 12-9) has $R_L = 6.8$ kΩ and $R_G = 2.2$ MΩ. Calculate the voltage gain and low-frequency output and input impedances of the circuit.

14-2. (a) Calculate the input capacitance for the amplifier in Problem 14-1.
(b) Assuming that $C_{DS} = 4$ pF for the device used in the circuit of Problem 14-1, calculate the output impedance at a signal frequency of 1 MHz.

14-3. A common source amplifier is to be designed to have a voltage gain of at least 40. If a 2N5459 FET is employed, determine the value of R_L for the circuit. Also calculate the typical and maximum values of circuit voltage gain.

14-4. Calculate the typical and maximum value of input capacitance for the circuit in Problem 14-3.

14-5. A common drain amplifier has $R_L = 6.8$ kΩ, $R_1 = 2.2$ MΩ, and $R_2 = 1$

Problems

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MΩ. The FET employed has $r_d = 120$ kΩ and $g_m = 5000$ μS. Calculate the input impedance, output impedance, and voltage gain.

14-6. A common drain amplifier is to have an output impedance of approximately 200 Ω. Select a suitable FET from the data sheet in Fig. 14-9. If R_L is 1 kΩ, calculate the typical, maximum, and minimum values of Z_o. Also calculate the typical voltage gain for the circuit.

14-7. A common gate amplifier has $R_L = 6.8$ kΩ and $R_S = 870$ Ω. If the FET used in the circuit is a 2N5458, calculate the voltage gain, input resistance, and output resistance.

14-8. A common gate circuit using a 2N5457 FET has a voltage gain of 36. If the FET g_m is the typical value for the device, calculate the value of R_L. Also calculate the maximum and minimum values of A_v.

14-9. The circuit in Fig. 14-10(b) has a 2-mA constant current generator and uses JFET's with the characteristics shown in Fig. 13-6. $R_1 = R_2 = 2.2$ kΩ, $V_{G1} = V_{G2} = -3$ V, $V_{CC} = +12$ V, and $V_{EE} = -12$ V. Determine the maximum and minimum values of drain and source voltages.

14-10. For the circuit described in Problem 14-9, calculate the ac voltage gain from the gate of one FET to its drain terminal. Refer to the bipolar differential amplifier circuit in Chapter 9 for guidance.

The Tunnel Diode

A *tunnel diode* (sometimes called an *Esaki diode* after its inventor, Leo Esaki) is a two-terminal *negative resistance* device which can be employed as an amplifier, an oscillator, or a switch. Because of its very fast response to inputs, it is almost exclusively a high-frequency component. Tunnel diodes require smaller bias voltages and lower load resistances than most other electronic devices.

15-1
Introduction

15-2
Theory of
Operation

Recall from Chapter 2 that the width of the depletion region at a *pn*-junction depends upon the doping density of the semiconductor material. Lightly doped material has a wide depletion region, while heavily doped material has a narrow region. In the case of the tunnel diode, the junction is formed of very heavily doped material, and consequently the depletion region is very narrow.

15-2.1
*Depletion
Region*

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The depletion region is an insulator since it lacks charge carriers, and usually charge carriers can cross it only when the external bias is large enough to overcome the barrier potential. Barrier potentials are approximately 0.7 V for silicon and 0.3 V for germanium. However, because the depletion region in a tunnel diode is extremely narrow, it does not constitute much of a barrier to electron flow. Consequently, a small forward or reverse bias (not large enough to overcome the barrier potential) can give charge carriers sufficient energy to cross the depletion region. When this occurs, the charge carriers are said to be *tunneling* through the barrier.

15-2.2
*Energy Band
Diagrams*

Consider the silicon energy band diagrams shown in Fig. 15-1. If the material is normally doped (either *n*-type or *p*-type), electrons fill all the holes in the valence band of energy levels and the conduction band is empty [Fig. 15-1(a)].
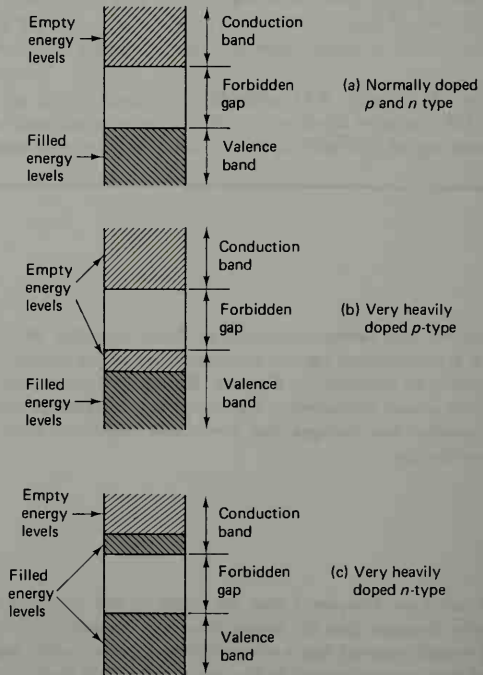
Figure 15-1. Energy band diagrams for normally doped and very heavily doped semiconductor material.

When semiconductor material is very heavily doped with holes (i.e., p-type), there is a shortage of electrons and the valence band cannot be regarded as filled. The result is that at the top of the valence band there is a layer of empty energy levels. This is illustrated in Fig. 15-1(b). With very heavily doped n-type material, there is an abundance of electrons. Consequently, electrons fill the valence band and create a layer of filled energy levels at the bottom of the conduction band [Fig. 15-1(c)].

The energy band diagram for a heavily doped unbiased pn-junction is shown in Fig. 15-2(a). Note that the depletion region is very narrow and that the filled levels on the n-side are exactly opposite those on the p-side. In this condition, no tunneling occurs because there are no empty lower energy levels to which electrons from either side might cross the depletion region. Note also that the conduction and valence bands on the p-side are higher (negatively) than those on the n-side. This is a result of the depletion region and barrier potential being created by electrons crossing from the n-side to the p-side. The n-side lost negative charges and the p-side gained them.

When the junction is reverse biased (negative on the p-side, positive on the n-side), filled energy levels on the p-side are opposite empty energy levels on the n-side. The result is that electrons tunnel through the barrier from the higher-energy levels on the p-side to the lower levels on the n-side [Fig. 15-2(b)]. Despite the fact that the junction is reverse biased, substantial current flows. Figure 15-2(c) shows that with increasing reverse bias more electrons tunnel from the p-side to the n-side and a greater current flows. Therefore, the reverse characteristic of a tunnel diode is linear, just like that of a resistor.

15-2.3
Reverse-
Biased
Tunnel
Diode

When the tunnel diode is forward biased, its initial behavior is similar to when it is reverse biased [Fig. 15-3(a)]. In this case, some of the filled levels on the n-side are raised to a higher energy level than empty levels on the p-side. Electron tunneling now occurs from the n-side to the p-side. When the forward bias is increased, more and more of the electrons on the n-side are raised to a higher level than the empty levels on the p-side. This results in more tunneling of electrons from the n-side to the p-side. Eventually, however, a maximum level of tunneling is reached when the band of filled energy levels at the bottom of the conduction band on the n-side is directly opposite the band of empty energy levels at the top of the valence band on the p-side [Fig. 15-3(b)]. With further increase in forward bias, part of the band of filled levels on the n-side is raised to an energy level corresponding to the forbidden gap on the p-side. Electrons cannot tunnel to a forbidden energy level; thus, as illustrated in Fig. 15-3(c), the current flow due to tunneling is reduced. With continued increase in forward bias, the tunneling continues to be reduced. When all the band of filled levels at the bottom of the conduction band on the n-side is raised to a level corresponding to the forbidden gap on the p-side, Fig. 15-3(d), the current flow due to

15-2.4
Forward-
Biased
Tunnel
Diode

Figure 15-2. Energy band diagrams and characteristic for reverse-biased tunnel diode.

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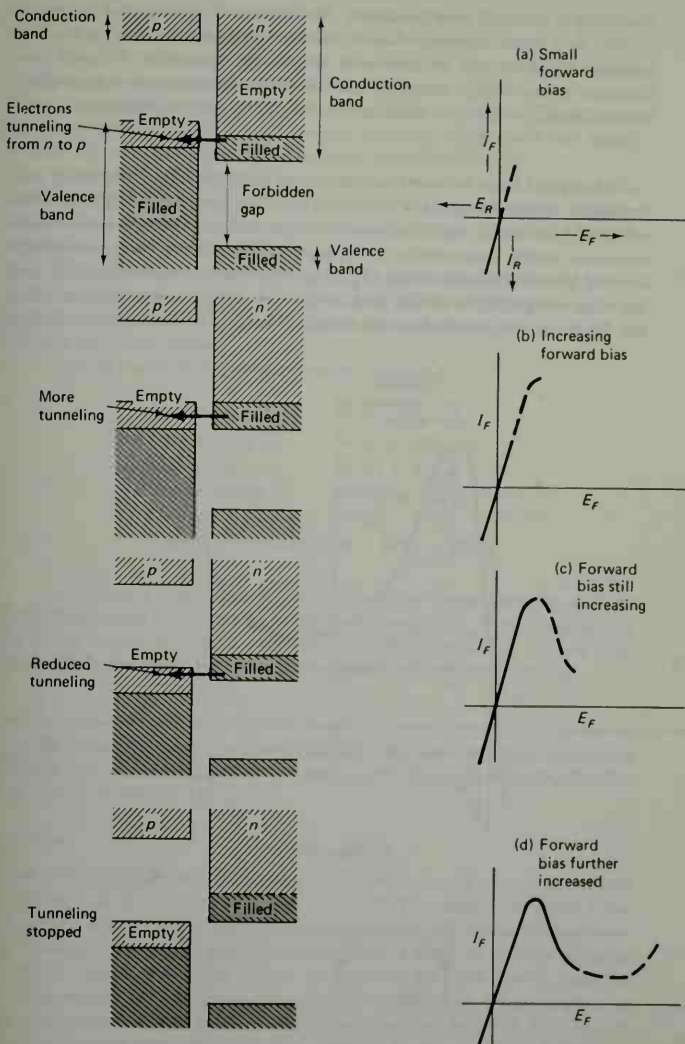
Figure 15-3. Energy band diagrams and characteristic for forward-biased tunnel diode.

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tunneling is reduced to a minimum. Now, however, the normal process of current flow across a forward-biased junction begins to take over, as the bias becomes large enough to overcome the barrier potential. Current now increases as the voltage increases, and the final portion of the tunnel diode forward characteristics is similar to that for an ordinary *pn*-junction.

15-3
Tunnel
Diode
Symbol,
Characteristics,
and
Parameters

A typical tunnel diode characteristic is shown in Fig. 15-4, along with frequently employed symbols for the device. The *peak current* (I_p) and *valley current* (I_v) are easily identified on the characteristic as the maximum and minimum levels, respectively, of I_F prior to the device being completely forward biased. The *peak voltage* (V_p) is the E_D level corresponding to I_p, and the *valley voltage* (V_v) is the E_D level at I_v. V_F is the *forward voltage drop* when the device is completely forward biased. The broken line on Fig. 15-4(a)
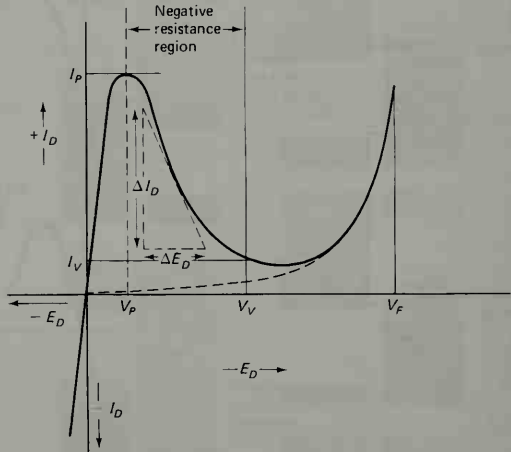
(a) Characteristics
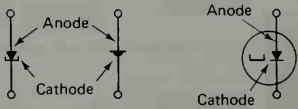
(b) Symbols

Figure 15-4. Tunnel diode characteristics and symbols.

shows the characteristic for an ordinary forward-biased diode. It is seen that this joins the tunnel diode characteristic as V_F is approached.

When a voltage is applied to a resistance, the current normally increases as the applied voltage is increased. Between I_p and I_v on the tunnel diode characteristic, I_D actually *decreases* as E_D is increased. This region of the characteristic is named the *negative resistance region*, and the *negative resistance R_D* of the tunnel diode is its most important property.

The value of the negative resistance may be determined by calculating the reciprocal of the slope of the characteristic in the negative resistance region. From Fig. 15-4(a), the negative resistance $R_D = (\Delta E_D / \Delta I_D)$, and the negative conductance $G_D = (\Delta I_D / \Delta E_D)$.

If R_D is measured at different points on the negative resistance portion of the characteristic, slightly different values will be obtained because the slope is not constant. Therefore, R_D is usually specified at the center of the negative resistance region.

Typical tunnel diode parameters are as follows:

> Peak current I_p = 1 to 100 mA
> Peak voltage V_p = 50 to 200 mV
> Valley current I_v = 0.1 to 5 mA
> Valley voltage V_v = 350 to 500 mV
> Forward voltage V_F = 0.5 to 1 V
> Negative resistance R_D = -10 to $-200\ \Omega$

In Chapter 3 it was shown that a straight-line approximation of diode characteristics can sometimes be conveniently employed. This is true also of the tunnel diode, for which the *piecewise linear characteristics* can be constructed from the data provided by the device manufacturer.

Construct the piecewise linear characteristics and determine R_D for the 1N3712 from the following data: $I_p = 1$mA, $I_v = 0.12$mA, $V_p = 65$mV, $V_v = 350$ mV, and $V_F = 500$ mV (at $I_F = I_P$).

Example 15-1

solution

Refer to Fig. 15-5. Point 1 is first plotted at $I_p = 1$ mA and $V_p = 65$ mV. Point 2 is plotted at $I_v = 0.12$ mA and $V_v = 350$ mV. The origin and point 1 are joined by a straight line to give the initial portion of the forward characteristic. A straight line is now drawn between points 1 and 2 to give the negative resistance region. Point 3 is plotted at $V_F = 500$ mV and $I_F = I_P$, and the forward voltage portion of the characteristic is drawn at the same slope as the line between 0 and point 1. Sometimes a second value of V_F at $\frac{1}{4} I_P$ is given so that the forward region can be plotted more accurately. A horizontal line is then drawn from point 2 to this line to represent the valley region of the characteristic.
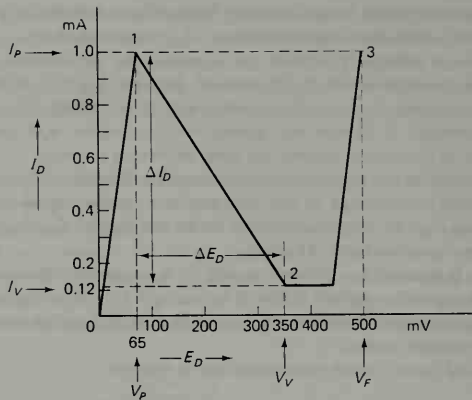
Figure 15-5. Tunnel diode piecewise linear characteristic.

R_D is determined by calculating the reciprocal of the slope of the negative resistance region of the characteristic.

$$R_D = \frac{\Delta E_D}{-\Delta I_D} = \frac{350 \text{ mV} - 65 \text{ mV}}{-(1 \text{ mA} - 0.12 \text{ mA})} = \frac{285 \text{ mV}}{-0.88 \text{ mA}} = -324 \ \Omega$$

15-5
Tunnel
Diode
Equivalent
Circuit

The equivalent circuit shown in Fig. 15-6 is for a tunnel diode biased in the negative resistance region. Therefore, it consists of the negative resistance R_D shunted by the junction capacitance C_D. Values of C_D range from 5 to 100 pF. R_S represents the resistance of the connecting leads and the semiconductor material, and is of the order of 1 Ω. L_S, which is typically 0.5 nH, is the inductance of the connecting leads to the tunnel diode.
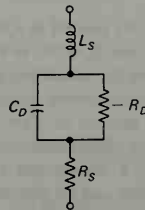
Figure 15-6. Tunnel diode equivalent circuit.

Because of the presence of L_S and C_D in the equivalent circuit, the tunnel diode has a *self-resonance frequency* (f_{xo}), which may range from 700 MHz to 4 GHz. The negative resistance determined from the characteristic does not allow for the effects of C_D shunting R_D at high frequencies. Thus, the *effective negative resistance* becomes progressively smaller as operating frequency increases, and there is a frequency at which the effective R_D becomes zero. This is known as the *resistive cutoff frequency* (f_{ro}). Values of f_{ro} range from 1.6 to about 3.3 GHz.

For operation as an amplifier, a tunnel diode must be biased to the center of its negative resistance region. Figure 15-7(a) shows the basic circuit of a parallel amplifier. The load resistor (R_L) is connected in parallel with the diode (D_1) and supplied with current from battery voltage (E_B) and signal (e_S). Figure 15-7(b) shows the dc conditions of the diode when the signal voltage $e_S = 0$ and when $e_S = \pm 100$ mV. Operation of the circuit is explained by the following example.

15-6
Tunnel
Diode
Parallel
Amplifier
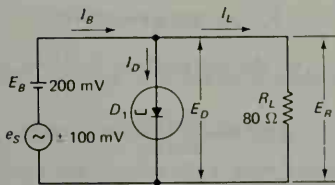
(a) Basic parallel amplifier
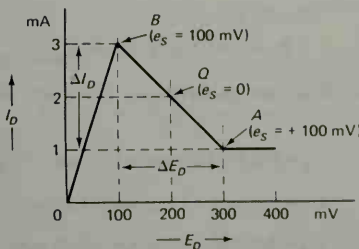
(b) Device current and voltage conditions for $e_S = 0$ and $e_S = \pm 100$ mV

Figure 15-7. Basic circuit of tunnel diode parallel amplifier with device current and voltage conditions.

Example 15-2

Assuming that E_B and e_S have zero source resistance, calculate the current gain, voltage gain, and power gain for the tunnel diode parallel amplifier circuit in Fig. 15-7(a).

solution

When $e_S = 0$,

$$E_B + e_S = E_B = 200 \text{ mV}$$
$$E_D = (E_B + e_S) = 200 \text{ mV}$$

From point Q on the characteristic, $I_D = 2$ mA and $E_R = (E_B + e_S) = 200$ mV.

$$I_L = \frac{E_R}{R_L} = \frac{200 \text{ mV}}{80 \text{ }\Omega} = 2.5 \text{ mA}$$
$$I_B = I_D + I_L = 4.5 \text{ mA}$$

When $e_S = + 100 \text{ } mV$,

$$E_B + e_S = 300 \text{ mV} = E_D = E_R$$

From point A on the characteristic, $I_D = 1$mA and $I_L = 300$ mV/ $80 \text{ }\Omega = 3.75$ mA.

$$I_B = 1 \text{ mA} + 3.75 \text{ mA} = 4.75 \text{ mA}$$

Change in $I_L = \Delta I_L = 3.75 \text{ mA} - 2.5 \text{ mA} = + 1.25 \text{ mA}$

Change in $I_B = \Delta I_B = 4.75 \text{ mA} - 4.5 \text{ mA} = + 0.25 \text{ mA}$

When $e_S = - 100 \text{ } mV$,

$$E_B + e_S = 100 \text{ mV} = E_D = E_R$$

From point B on the characteristic, $I_D = 3$ mA and $I_L = 100$ mV/ $80 \text{ }\Omega = 1.25$ mA.

$$I_B = 3 \text{ mA} + 1.25 \text{ mA} = 4.25 \text{ mA}$$

$$\Delta I_L = 1.25 \text{ mA} - 2.5 \text{ mA} = - 1.25 \text{ mA}$$

$$\Delta I_B = 4.25 \text{ mA} - 4.5 \text{ mA} = - 0.25 \text{ mA}$$

It is seen that, when $e_S = \pm 100$ mV, $\Delta I_L = \pm 1.25$ mA and $\Delta I_B = \pm 0.25$ mA. Also, ΔI_B is an input current (i_s) produced by signal voltage e_S, and ΔI_L is an output current (i_o) through the load resistor R_L.

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Gain
Equation
for a
Parallel
Amplifier

The current gain is

$$A_i = \frac{i_o}{i_s} = \frac{1.25 \text{ mA}}{0.25 \text{ mA}} = 5$$

The output voltage is

$$e_o = \Delta E_R = e_s$$

The voltage gain is

$$A_v = \frac{e_o}{e_s} = 1$$

The power gain is

$$A_p = A_i \times A_v = 5$$

It is seen that a tunnel diode parallel amplifier has current gain and power gain but no voltage gain.

From Fig. 15-7(b), the value of R_D can be determined as

15-7
Gain
Equation
for a
Parallel
Amplifier

$$R_D = \frac{\Delta E_D}{\Delta I_D} = \frac{200 \text{ mV}}{-2 \text{ mA}} = -100 \ \Omega$$

From Example 15-1, when the signal voltage (e_s) changed by $+100$ mV, the diode current (I_D) changed from 2 to 1 mA. Thus,

$$\Delta I_D = -1 \text{ mA} \qquad \text{for } e_s = +100 \text{ mV}$$

ΔI_D can also be calculated as

$$I_D = \frac{e_S}{R_D} = \frac{100 \text{ mV}}{-100 \ \Omega} = -1 \text{ mA}$$

and $i_o = \Delta I_L = e_S / R_L$.

$$i_s = \Delta I_B = \Delta I_L - \Delta I_D$$

$$= \frac{e_S}{R_L} - \frac{e_S}{R_D}$$

$$A_i = \frac{i_o}{i_s} = \frac{e_s/R_L}{(e_s/R_L) - (e_s/R_D)} = \frac{1/R_L}{(1/R_L) - (1/R_D)}$$

For the parallel amplifier

$$A_i = \frac{R_D}{R_D - R_L} \qquad (15\text{-}1)$$

Note that R_D is already taken as negative for this formula, so that only the absolute value of R_D (i.e., no negative sign) should be employed in calculating A_i.

For $R_D = 100\ \Omega$ and $R_L = 80\ \Omega$, as in Example 15-2,

$$A_i = \frac{100}{100 - 80} = 5$$

From the equation for A_i it is seen that

$$\text{When } R_L \ll R_D, \qquad A_i \approx 1$$

and $\qquad\qquad\qquad$ When $R_L \gg R_D, \qquad A_i < 1$

When $R_L = R_D$, $A_i = \infty$, which means that the circuit is likely to oscillate. Therefore, for best gain R_L should be slightly less than R_D.

15-8
Practical
Parallel
Amplifier
Circuit

Figure 15-8 shows the circuit of a practical tunnel diode parallel amplifier. The signal voltage e_S and load resistor R_L are capacitor coupled to the diode, while dc bias is provided by voltage E_B and potential divider R_1 and R_2. Inductor L_1 and capacitor C_1 isolate the bias supply from ac signals. Operation of the amplifier is best understood by drawing the dc and ac equivalent circuits.

Example 15-3

Draw the dc and ac equivalent circuits for the tunnel diode parallel amplifier circuit of Fig. 15-8. Also draw the dc load line on the device characteristic. Determine the circuit bias conditions and calculate the amplifier current gain.
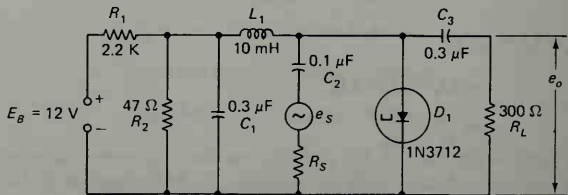
Figure 15-8. Practical tunnel diode parallel amplifier circuit.

solution

dc equivalent circuit

The capacitors are a dc open circuit, and the inductor has a winding resistance R_W. Therefore, the dc equivalent circuit consists of E_B, R_1, R_2, R_W, and D_1 as shown in Fig. 15-9(a).

ac equivalent circuit

For ac signal frequencies, the impedance of L_1 is much higher than that of the diode or R_L. Therefore, L_1 together with E_B, R_1, R_2, and C_1 are all left out of the ac equivalent circuit. C_2 and C_3 are ac short circuits, so the ac equivalent circuit consists of e_S, R_S, D_1, and R_L [Fig. 15-9(b)].

dc load line and bias conditions

E_B, R_1, and R_2 can be replaced by the open-circuit voltage across R_2 and the dc source resistance (R_B) seen when looking toward E_B at R_2 [Fig. 15-9(a)]. This is simply the Thévenin equivalent circuit of E_B, R_1, and R_2.

The open-circuit voltage

$$E_O = \frac{E_B \times R_2}{R_1 + R_2} = \frac{12 \text{ V} \times 47 \text{ }\Omega}{2.2 \text{ k}\Omega + 47 \text{ }\Omega} = 250 \text{ mV}$$

and

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{2.2 \text{ k}\Omega \times 47 \text{ }\Omega}{2.2 \text{ k}\Omega + 47 \text{ }\Omega} = 46 \text{ }\Omega$$

To this must be added R_W, which is typically about 35 Ω.

The simplified dc equivalent circuit is now the diode in series with a bias of 250 mV and a total resistance of approximately 80 Ω. This is shown in Fig. 15-10(a). The dc load line can now be drawn in the usual way.

$$E_D = E_O - (I_D \times R_{L(\text{dc})})$$

where $R_{L(\text{dc})} = R_B + R_W$. When $I_D = 0$, $E_D = E_O - 0 = 250$ mV. Plot point A on the characteristic [Fig. 15-10(b)] at $I_D = 0$ and $E_D = 250$ mV.

(a) dc equivalent circuit

(b) ac equivalent circuit
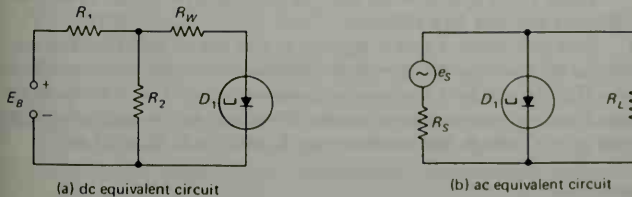
Figure 15-9. DC and AC equivalent circuits for tunnel diode parallel amplifier in Fig. 15-8.
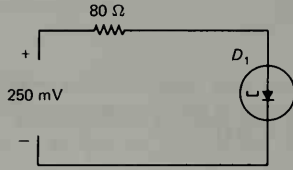
(a) Simplified dc equivalent current
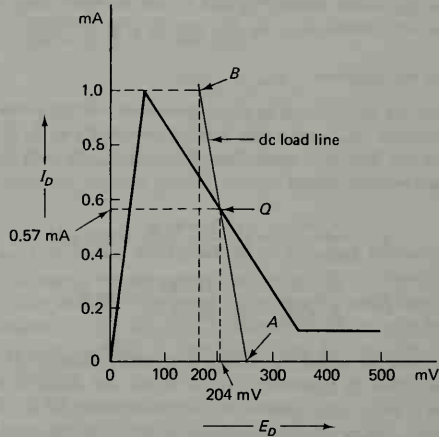
(b) dc load line

Figure 15-10. Simplified DC equivalent circuit and dc load line plotting for tunnel diode parallel amplifier.

When $I_D = 1$ mA, $E_D = 250$ mV $- (1$ mA $\times 80$ $\Omega) = 170$ mV. Plot point B at $I_D = 1$ mA and $E_D = 170$ mV.

Now join points A and B together to give the dc load line. It is seen that the dc load line for $R_L = 80$ Ω intersects the device characteristic at point Q in the middle of the negative resistance region. This is the quiescent point for the circuit, and it defines the dc voltage and current conditions. From point Q, the dc bias conditions are $I_D \simeq 0.57$ mA, $E_D \simeq 204$ mV.

current gain

$$\text{ac load} = R_L = 300 \ \Omega$$

For the IN3712, $R_D = 324\ \Omega$ (see Example 15-1).
From Eq. (15-1),

$$A_t = \frac{R_D}{R_D - R_L} = \frac{324}{324 - 300} = 13.5$$

A tunnel diode *series amplifier* may also be constructed. In this case the device is connected in series with the load, and voltage amplification is obtained instead of current amplification. Oscillators and switching circuits may also be constructed using tunnel diodes.

Heavily doped material. Semiconductor material from which tunnel diodes are manufactured—heavily doped to provide large quantities of p-type or n-type impurities.

Filled energy levels. Semiconductor energy levels which are completely occupied by electrons.

Empty energy levels. Semiconductor energy levels from which electrons are absent—filled with holes.

Forbidden energy levels. Semiconductor energy levels which cannot be occupied by electrons—energy levels in the forbidden gap.

Depletion region. Region at pn-junction depleted of charge carriers—very narrow region in a tunnel diode.

Tunneling. Electrons crossing the depletion region at a pn-junction without being given sufficient energy to overcome the barrier potential are said to be tunneling through the barrier.

Negative resistance region. Region of tunnel diode forward characteristic in which the current decreases as the voltage is increased.

Negative resistance. Reciprocal of the slope of the negative resistance region calculated as (voltage change)/(current change).

Peak current (I_p). Forward current that flows just prior to the negative resistance region.

Peak voltage (V_p). Forward-bias voltage required to produce peak current.

Valley current (I_v). Forward current that flows just after negative resistance region.

Valley voltage (V_v). Forward-bias voltage necessary to produce valley current.

Forward voltage (V_F). Forward-bias voltage necessary to bias the tunnel diode beyond the negative resistance and valley regions.

Piecewise linear characteristic. Straight-line approximation of device characteristic.

Self-resonance frequency. Frequency at which the inductance and capacitance of a tunnel diode will resonate.

Effective negative resistance.   Value of tunnel diode negative resistance at a given high frequency—less than the dc negative resistance value.

Resistive cutoff frequency.   Frequency at which negative resistance goes to zero.

Parallel amplifier.   Current amplifier circuit in which the tunnel diode and load resistor are in parallel.

Series amplifier.   Voltage amplifier in which the tunnel diode and load resistor are in series.

Review Questions

15-1.   Sketch energy band diagrams for (a) normally doped p-type and n-type semiconductor material; (b) very heavily doped p-type; (c) very heavily doped n-type. Briefly explain.

15-2.   Draw typical reverse characteristics for a tunnel diode. Also sketch the energy band diagrams for the tunnel diode, and show the effect of reverse bias. Briefly explain.

15-3.   Make a sketch showing the approximate shape of the forward characteristics for a tunnel diode. Sketch the tunnel diode energy band diagrams, showing the effect of increasing forward bias. Explain the shape of the characteristics in terms of the energy band diagrams.

15-4.   Sketch typical forward characteristics for a tunnel diode, showing realistic voltage and current levels. Label all important points and regions on the characteristics, and show how the most important parameter of the tunnel diode can be derived from the characteristics.

15-5.   Sketch the equivalent circuit for a tunnel diode and explain the origin of every component. State typical values for each component, and define self-resonance frequency, resistive cutoff frequency, and effective negative resistance.

15-6.   Sketch the basic circuit of a tunnel diode parallel amplifier. Briefly explain how it operates.

15-7.   Draw a practical parallel amplifier circuit for a tunnel diode. Explain the function of each component. Also draw the dc and ac equivalent circuits of the parallel amplifier.

Problems

15-1.   A tunnel diode is specified as having $I_p = 6$ mA, $V_p = 50$ mV, $I_v = 0.5$ mA, $V_v = 400$ mV, and $V_F = 550$ mV at $I_F = I_p$. Construct the piecewise linear characteristics, and determine the value of negative resistance for the device.

15-2.   Construct the piecewise linear characteristics and determine R_D for a IN3715 from the following data: $I_p = 2.2$ mA, $I_v = 0.21$ mA, $V_p = 65$ mV, $V_v = 355$ mV, and $V_F = 510$ mV at $I_F = I_p$.

15-3.   A parallel amplifier uses the tunnel diode specified in Problem 15-1 and a load resistance of 47 Ω. Bias voltage is 225 mV from a dc

source having zero resistance. Draw the dc load line for the circuit, and calculate the current gain, voltage gain, and power gain.

15-4. A IN3715 is to be connected as a parallel amplifier. Using the piecewise linear characteristics drawn for Problem 15-2, draw an appropriate dc load line and determine suitable values of R_L, R_B, E_B, and e_s. Calculate the circuit current gain.

15-5. A practical tunnel diode parallel amplifier circuit (Fig. 15-8) has the following components: $E_B = 5$ V, $R_1 = 220$ Ω, $R_2 = 12$ Ω, $C_1 = 0.5$ μF, $R_w = 0.5$ Ω, $L_1 = 20$ mH, $C_2 = 0.2$ μF, $C_3 = 0.5$ μF, and $R_L = 75$ Ω. The tunnel diode used has $I_p = 5$ mA, $E_p = 50$ mV, $I_v = 1$ mA, and $V_v = 400$ mV. Draw the ac and dc equivalent circuits for the amplifier. Construct the piecewise linear characteristics and draw the dc load line. Calculate the circuit current gain.

The Silicon Controlled Rectifier

16-1
Introduction

The silicon controlled rectifier (SCR) can be thought of as an ordinary rectifier with a control element. The current to the control element, which is termed the gate, determines the anode-to-cathode voltage at which the device commences to conduct. The gate bias may keep the device off, or it may permit conduction to commence at any desired point in the forward half-cycle of a sinusoidal input. The SCR is widely applied as an ac power control device. Many other devices, such as the DIAC, TRIAC, etc., are based on the SCR principle. Collectively, SCR-type devices are known as *thyristors*. This term is derived from *thyratron* and *transistor*, the thyratron being a gas-filled tube which behaves like an SCR.

16-2
SCR
Operation

Figure 16-1(a) shows why an SCR is sometimes referred to as a *four-layer device* or *pnpn device*. The SCR consists of four layers of semiconductor material, alternately p-type and n-type. The layers are designated p_1, n_1, p_2, and n_2 in Fig. 16-1(a). Three junctions are produced: J_1, J_2, and J_3, and there are three terminals, *anode* (A), *cathode* (C), and *gate* (G).

344
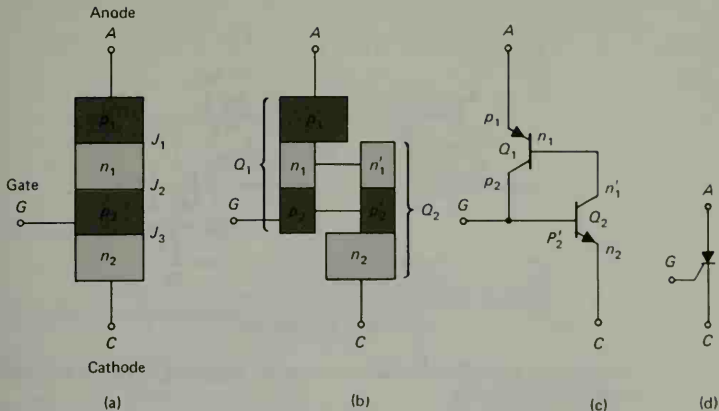
Figure 16-1. (a) and (b) SCR basic construction; (c) two-transistor equivalent circuit; (d) symbol.

To understand the operation of the device, it is necessary to imagine layers n_1 and p_2 split into n_1, n_1', p_2, and p_2', as shown in Fig. 16-1(b). Since n_1 is connected to n_1', and p_2 is connected to p_2', this has not really changed anything. However, it is now possible to think of p_1, n_1, p_2 as a *pnp* transistor, and n_1', p_2', n_2 as an *npn* transistor. Replacing the transistor block representations in Fig. 16-1(b) with the *pnp* and *npn* circuit symbols gives the *two-transistor equivalent circuit* [Fig. 16-1(c)]. It is seen that Q_2 collector is connected to Q_1 base, and the Q_1 collector is commoned with Q_2 base. The Q_1 emitter is the SCR anode terminal, the Q_2 emitter is the cathode, and the gate is the juction of the Q_1 collector and the Q_2 base. The circuit symbol for the SCR is shown in Fig. 16-1(d).

To forward bias the SCR, a voltage is applied as shown in Fig. 16-2(a), positive on the anode, negative on the cathode. If the gate is left unconnected, only small leakage currents flow and both transistors remain cut off. [Reference to Fig. 16-1(a) shows that the leakage currents are the result of junction J_2 being reverse biased when A is positive and C is negative.]

When a negative gate–cathode voltage is applied, the Q_2 base–emitter junction is reverse biased, and only small leakage currents flow, so both transistors remain off. A positive gate–cathode voltage [Fig. 16-2(b)] forward biases the Q_2 base–emitter junction and causes a base current I_{B2} to flow, consequently producing collector current I_{C2}. Since I_{C2} is the same as I_{B1}, Q_1 also switches *on* and I_{C1} flows, providing base current I_{B2}. Each collector current provides much more base current than is needed by the transistors, and even when the gate current (I_G) is cut off the transistors remain *on*, conducting heavily with only a small SCR anode-to-cathode voltage drop.
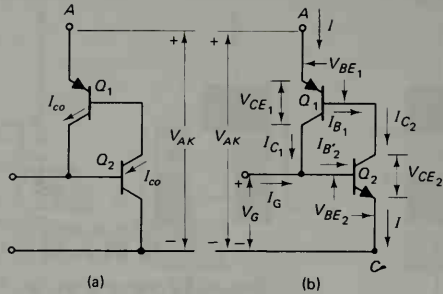
Figure 16-2. SCR operation.

The ability of the SCR to remain *on* when the triggering current is removed is referred to as *latching*.

To switch the SCR on, only a brief pulse of gate current is required. Once switched *on*, the gate has no further control, and the device remains *on* until the anode–cathode voltage is reduced to near zero. The SCR can also be triggered *on* with the gate open circuited, if the anode-to-cathode voltage is made large enough. Consider Fig. 16-1(a) again. With a forward bias (positive on A, negative on C), junctions J_1 and J_3 are forward biased while junction J_2 is reverse biased. When V_F is made large enough, J_2 will break down due to avalanche effect (Chapter 11). The resultant current flow across the junction constitutes collector current in each transistor. Each collector current again feeds base current into the other transistor, and both transistors switch *on*.

16-3
SCR
Characteristics
and
Parameters

Typical forward and reverse characteristics for an SCR are shown in Fig. 16-3. First consider the reverse characteristics, and refer again to Fig. 16-1(a). When a reverse bias is applied (negative on A, positive on C), J_2 is forward biased while J_1 and J_3 are reverse biased. When the reverse voltage $-V_{AK}$ is small, a *reverse* leakage current (I_{RX}) flows (see Fig. 16-3). This is typically around 100 μA and is sometimes referred to as the *reverse blocking current*. As the level of reverse voltage is increased, I_{RX} remains approximately constant until $-V_{AK}$ becomes large enough to cause J_1 and J_3 to break down. As shown in Fig. 16-3, the reverse current increases very rapidly when the *reverse breakdown* voltage is reached, and if I_R is not limited the device would be destroyed. The region of the reverse characteristics before reverse breakdown is termed the *reverse blocking region*.

When the SCR is forward biased with $I_G = 0$, two junctions (J_1 and J_3) are forward biased and J_2 is reverse biased. With small anode-to-cathode voltages ($+V_{AK}$), a small leakage current flows (Fig. 16-3). This *forward*
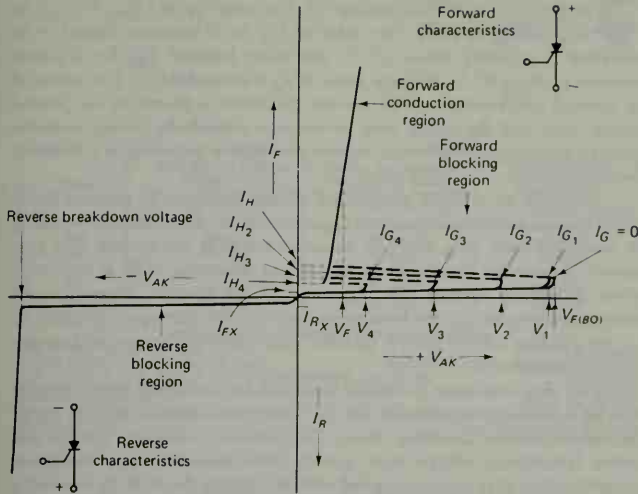
Figure 16-3. SCR forward and reverse characteristics.

leakage current (I_{FX}) is approximately equal to I_{RX} and has a typical value of 100 μA. With I_G at zero, I_F remains at I_{FX} until $+V_{AK}$ is made large enough to cause the reverse-biased J_2 junction to break down. The forward voltage at this point is termed the *forward breakover voltage* $V_{F(BO)}$. When $V_{F(BO)}$ is reached, the two component transistors Q_1 and Q_2 are immediately switched *on* into saturation as already explained, and the anode–cathode voltage falls to the *forward conduction voltage* (V_F).

So far the forward characteristics have been discussed only for the case of $I_G = 0$. Now consider the effect of I_G greater than zero. As already shown, when $+V_{AK}$ is less than $V_{F(BO)}$ and I_G is zero, a small leakage current flows. This is too small to have any effect on the level of $+V_{AK}$ at which switch-on occurs. When I_G is made just slightly larger than the junction leakage currents, it will have a negligible effect on the level of $+V_{AK}$ for switch-on; see I_{G1} in Fig. 16-3. Now consider the opposite extreme. When I_G is made larger than the minimum base current required to switch Q_2 on, the SCR remains off until $+V_{AK}$ is large enough to forward bias the base–emitter junctions of Q_1 and Q_2. This is illustrated in Fig. 16-3 where it is seen that when $I_G = I_{G4}$ switch on occurs when $+V_{AK}$ reaches the relatively low voltage of V_4.

Between I_{G1} and I_{G4} there are gate current levels which permit device switch on at levels of $+V_{AK}$ greater than V_4 but less than $V_{F(BO)}$.

The forward conduction voltage (V_F) is made up of ($V_{BE1} + V_{CE2}$) or ($V_{BE2} + V_{CE1}$) [Fig. 16-2(b)]. The value of V_{CE} for a transistor biased *on* in saturation is typically about 0.2 V, and since forward V_{BE} for a silicon transistor is about 0.7 V, the total value of V_F is around 0.9 V. The region of the forward characteristics before switch on occurs is known as the *forward blocking region*, and the region after switch on is termed the *forward conduction region*. In the forward conduction region, the SCR is behaving as a forward-biased rectifier.

To switch an SCR off, the forward current (I_F) must be reduced below a level known as the *holding current* (I_H) (Fig. 16-3). The holding current is the minimum level of I_F that will maintain the SCR conducting. If a gate current (I_G) greater than zero is maintained while the SCR is on, lower values of holding current (I_{H2}, I_{H3}, or I_{H4}) are possible. Manufacturers usually specify I_H as I_{HO}, the holding current with the gate open circuited, or I_{HX}, the holding current with a specified bias resistance connected between gate and cathode.

Two very important quantities that must be considered in selecting an SCR for a particular application are the voltage and currents that the device can survive without breaking down. The forward breakover voltage and reverse breakdown voltage have already been discussed. The maximum forward voltage that may be applied without causing the SCR to conduct is termed the *forward blocking voltage*. This is designated V_{FOM} or V_{FXM} for an open-circuited gate or a resistance biased gate, respectively. Similarly, the *reverse blocking voltage* is called V_{ROM} or V_{RXM}. The maximum allowable forward current is variously specified as the *average forward current* [$I_{F(av)}$], the *rms forward current* (I_f), or the *peak one-cycle surge current* [$I_{FM(surge)}$]. The first two of these need no explanation; the third is a relatively large nonrepetitive surge current that can be permitted to flow for one cycle.

Part of the available range of SCR's is illustrated by the partial specifications shown in Figs. 16-4 and 16-5. With an rms forward current of 1.6 A and a forward blocking voltage up to 200 V, the C6 range (Fig. 16-4) is relatively low current, low voltage devices. The C6 package is the standard TO-5 transistor-type can. Note that, although the anode-to-cathode voltage can be as high as 300 V (nonrepetitive), the peak reverse gate voltage is only 6 V.

The C35 range (Fig. 16-5) is capable of handling much higher powers than the C6 SCR's. RMS forward current for the C35 devices is 35 A, and peak forward blocking voltages are as high as 800 V repetitive, or 960 V nonrepetitive. The device is bolt mounted for heat dissipation. Even higher voltage and higher current handling are possible with the C500X1, for example. RMS continuous current is 1200 A and forward blocking voltage is 1800 V. To remove the heat dissipated, the device has a water jacket requiring a flow of 1 gal/min ($\approx$4 liters/min) for maximum dissipation.
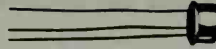
C6

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -40°C$ to $+125°C$ $R_{GK} = 1000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Millisec. $T_J = -40°C$ to $+125°C$
C6U	25 volts	25 volts	40 volts
C6F	50 volts	50 volts	75 volts
C6A	100 volts	100 volts	150 volts
C6G	150 volts	150 volts	225 volts
C6B	200 volts	200 volts	300 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F .... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ .... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ... 10 Amperes
Peak Reverse Gate Voltage, V_{GRM} .... 6 Volts
Operating Temperature T_J .... $-40°C$ to $+125°C$
Forward and Reverse Blocking Current* .... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ .... I_{HX} Typ. 1.0/Max. 5.0 mAdc
Turn-off Time† .... t_{off} Typ. 40 μsec
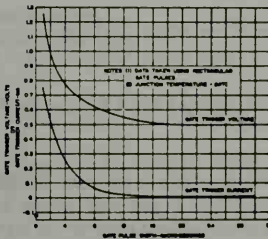
TYPICAL VARIATION OF GATE TRIGGER VOLTAGE AND CURRENT WITH GATE PULSE WIDTH

Figure 16-4. Condensed specification for C6 SCR. (Courtesy of General Electric Semiconductor Products Dept., Syracuse, N.Y.)

16-5
SCR
Control
Circuits

16-5.1
Pulse Control

The simplest of SCR control circuits is shown in Fig. 16-6(a). If SCR_1 were an ordinary rectifier, the ac supply voltage would be half-wave rectified and only the positive half-cycles would appear across the load (R_L). The same would be true if the SCR gate had a continuous bias voltage to keep it

35A RMS SCR UP TO 800V

C35

Type	Peak Forward Blocking Voltage, V_{FOM} $T_C = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage, $V_{ROM}(rep)^*$ $T_C = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec $V_{ROM}(non-rep)^*$ $T_C = -65°C$ to $+125°C$
C35U	25 volts	25 volts	35 volts
C35F	50 volts	50 volts	75 volts
C35A	100 volts	100 volts	150 volts
C35G	150 volts	150 volts	225 volts
C35B	200 volts	200 volts	300 volts
C35H	250 volts	250 volts	350 volts
C35C	300 volts	300 volts	400 volts
C35O	400 volts	400 volts	500 volts
C35E	500 volts	500 volts	600 volts
C35M	600 volts	600 volts	720 volts
C35S	700 volts	700 volts	840 volts
C35N	800 volts	800 volts	960 volts

*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 11°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F . . . . 35 Amperes
Average Forward Current, On-state $I_{F(AV)}$ . . . . . Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) . . . . 150 Amperes
I^2t (for fusing) . . . . 75 Ampere² seconds (for times ≥ 1.5 milliseconds)
Operating Temperature T_J . . . . −65°C to +125°C
Turn-off Time† . . . . t_{off} Max. 75 µsec

Figure 16-5. Condensed specification for C35 SCR. (Courtesy of General Electric Semiconductor Products Dept., Syracuse, N.Y.)

on when the anode–cathode voltage is positive. A trigger pulse applied to the gate can switch the device on at any time during the positive half-cycle of the input voltage. The resultant load waveform is a portion of the positive half-cycle commencing at any instant at which the SCR is triggered [Fig. 16-6(b)]. Resistor R_G holds the gate-cathode voltage at zero when no trigger input is present.

Example 16-1

The circuit of Fig. 16-6(a) has an ac input of 30 V peak, $R_L = 15\ \Omega$, and $R_G = 1\ \text{k}\Omega$. (a) Select a suitable SCR from the specifications in Fig. 16-4. (b) Specify the required trigger current and voltage. (c) Determine the supply voltage at which the SCR will switch off.

solution (a)

For the SCR to remain off until triggered, the forward blocking voltage (V_{FXM}) must be greater than the peak input voltage.

$$V_{FXM} > 30 \text{ V}$$

(a) SCR control circuit

(b) Circuit waveforms
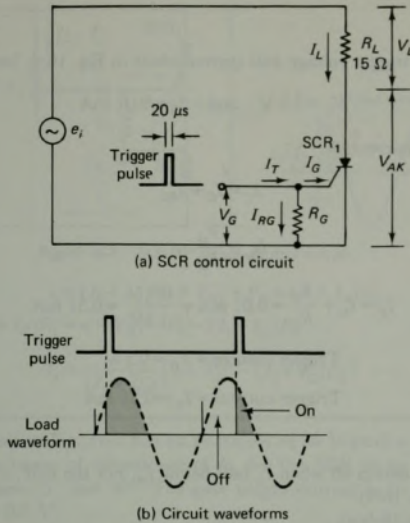
Figure 16-6. Simple SCR control circuit and waveforms.

For the C6U, $V_{FXM} = 25$ V (see Fig. 16-4). Therefore, the C6U is *not* suitable.

For the C6F, $V_{FXM} = 50$ V. The C6F looks like it might be a suitable device. Now consider the peak load current (I_P).

At peak input, voltage across R_L is

$$V_L = e_p - V_{AK}$$

$$I_P = \frac{e_p - V_{AK}}{R_L} \qquad (16\text{-}1)$$

When the SCR is on, a typical V_{AK} is 1 V.

$$I_P = \frac{30 \text{ V} - 1 \text{ V}}{15 \ \Omega} = 1.93 \text{ A}$$

For half-wave rectification, the $_{rms}$ value of I_L is

$$
\begin{aligned}
I_{rms} &= 0.5 \times I_P \\
&= 0.5 \times 1.93 \text{ A} \\
&\approx 0.97 \text{ A}
\end{aligned}
$$

The maximum allowable rms forward current for the C6 range is 1.6 A; therefore, the C6F is a suitable device.

solution (b)

From the gate trigger voltage and current chart in Fig. 16-4, for 20-μs pulse,

$$V_G = 0.5 \text{ V} \quad \text{and} \quad I_G \approx 0.01 \text{ mA}$$

Trigger input current,

$$I_T = I_G + I_{RG}$$

$$I_{R_G} = \frac{V_G}{R_G}$$

$$I_T = I_G + \frac{V_G}{R_G} = 0.01 \text{ mA} + \frac{0.5 \text{ V}}{1 \text{ k}\Omega} = 0.51 \text{ mA}$$

$$\text{Trigger voltage} = V_G = 0.5 \text{ V}$$

$$\text{Trigger current} = I_T = 0.51 \text{ mA}$$

solution (c)

The SCR will switch off when I_L falls below I_H. For the C6F, a typical $I_H = 1$ mA (see Fig. 16-4).

From Fig.16-6(a),

$$e_i = V_{AK} + I_L R_L$$

At $I_L = I_H$,

$$e_i = 1 \text{ V} + (1 \text{ mA} \times 15 \text{ }\Omega) = 1.015 \text{ V}$$

The SCR will switch off when e_i falls below 1.015 V.

**16-5.2
90° Phase
Control**

In the phase-control circuit shown in Fig. 16-7 the gate triggering current is derived from the ac supply via resistance R_1. If R_1 is adjusted to a low resistance value the SCR will trigger almost immediately at the commencement of the positive half-cycle of the input. If R_1 is set to a high resistance, the SCR may not switch on until the peak of the positive half-cycle. For resistances between these two values, the SCR will switch on somewhere between the commencement and the peak of the positive half-cycle, i.e., between 0° and 90°. If I_G is not large enough to trigger the SCR at 90°, then the device will not trigger on at all, because I_G is greatest at the peak of input and falls off as the voltage falls. The purpose of diode D_1 is to protect the SCR gate from the negative voltage that would otherwise be applied to it during the negative half-cycle of the input. R_2 keeps the SCR biased off until triggered. Also, because I_G is not precisely predictable, the presence of R_2 makes the R_1 calculation more reliable.

From Fig. 16-7, it can be seen that at the instant of SCR switch on the current $I_G + I_2$ flows through R_1, D_1, and R_L. Therefore, at the instant of
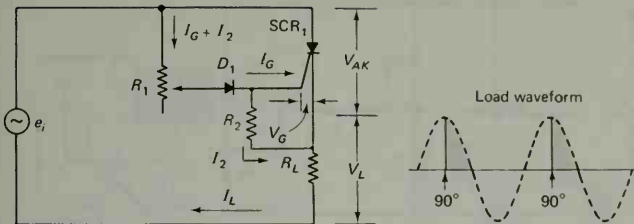
Figure 16-7. SCR 90° phase-control circuit.

switch on
$$e_i = (I_2 + I_G)R_1 + V_{D1} + V_G + (I_2 + I_G)R_L$$

$$(I_2 + I_G)R_1 = e_i - V_{D1} - V_G - (I_2 + I_G)R_L$$

$$R_1 = \frac{1}{(I_2 + I_G)}\left[e_i - V_{D1} - (I_2 + I_G)R_L \right] \qquad (16\text{-}2)$$

The circuit in Fig. 16-7 has an ac supply of 30 V peak and $R_L = 15\ \Omega$. **Example 16-2**
Determine the range of adjustment of R_1 for the SCR to be triggered on
anywhere between 5° and 90°. The gate trigger current is 10 μA and the
gate voltage is 0.5 V.

solution

$$I_2 \gg I_G$$

let
$$I_2 = 90\ \mu A$$

$$R_2 = \frac{0.5\ V}{90\ \mu A} = 5.6\ k\Omega$$

$$I_2 + I_G = 90\ \mu A + 10\ \mu A = 100\ \mu A$$

At 5°, $e_i = 30 \sin 5° = 30 \times 0.0872 = 2.6\ V$.
From Eq. (16-2),

$$R_{1(min)} = \frac{1}{100\ \mu A}\left[2.6\ V - 0.7\ V - 0.5\ V - (100\ \mu A \times 15\ \Omega) \right]$$

$$= \frac{1.4\ V}{100\ \mu A} = 14\ k\Omega$$

At 90°, $e_i = $ peak voltage $= 30$ V.

$$R_{1(max)} = \frac{1}{100\ \mu A}\left[30\ V - 0.7\ V - 0.5\ V - (100\ \mu A \times 15\ \Omega) \right]$$

$$= \frac{30\ V - 1.2015\ V}{100\ \mu A} = \frac{28.8\ V}{100\ \mu A} = 288\ k\Omega$$

R_1 should be adjustable from 14 kΩ to 288 kΩ.
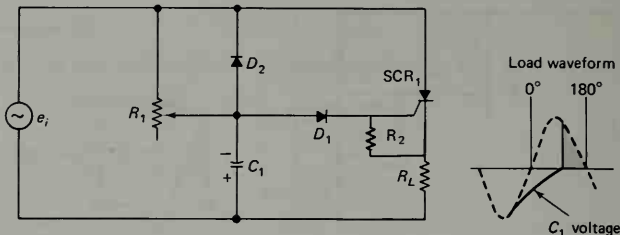
Figure 16-8. SCR 180° phase-control circuit.

The circuit shown in Fig. 16-8 is identical to that in Fig. 16-7, except that diode D_2 and capacitor C_1 have been added. During the negative half-cycle of the input, C_1 is charged negatively as shown in the figure to the peak of the input voltage. When the negative input peak is passed, D_2 is reverse biased, because its anode (connected to C_1) is more negative than its cathode. C_1 then commences to discharge via R_1. Depending upon the values of C_1 and R_1, the capacitor may be almost completely discharged at the commencement of the input voltage positive half-cycle, or it may retain a partially negative charge until almost 180° of positive half-cycle has passed. While C_1 remains negatively charged, D_1 is reverse biased and the gate cannot go positive to trigger on the SCR. Thus, R_1 and/or C_1 may be adjusted to effect SCR triggering anywhere from 0° to 180° of input waveform.

A simple modification of the 180° phase-control circuit is shown in Fig. 16-9. The addition of rectifier D_3 causes the negative half-cycle of the input to appear across the load. Control is available only over the positive half-cycle. Figure 16-10 shows two SCR's and control circuits inverse parallel connected. This affords separate control over positive and negative half-cycles.

The various circuits described above are employed in such applications as light dimmers, battery chargers, etc.

The construction, equivalent circuit and characteristics of a TRIAC are shown in Fig. 16-11. The device amounts to two inverse parallel connected SCR's with a common gate terminal. Section n_1, p_2, n_3, and p_3 in Fig. 16-11(a) form one SCR, which can be represented by transistors Q_1 and Q_2 in Fig. 16-11(b). Similarly, p_1, n_2, p_2, and n_4 form another SCR, which has the transistor equivalent circuit Q_3 and Q_4. P_2 is the layer common to both SCR's, and it functions as a gate for both devices. Because of the inverse parallel connection, the other terminals cannot be identified as anode and cathode; instead they are designated A_1 and A_2. When the gate is made positive with respect to A_1, and A_2 is also made positive with respect to A_1, transistors Q_3 and Q_4 switch on [Fig. 16-11(b)]. In this case A_2 is the anode and A_1 is the cathode. When the gate and A_1 are made positive with respect to A_2, Q_1 and Q_2 switch on. Now A_1 is the anode and A_2 the cathode.
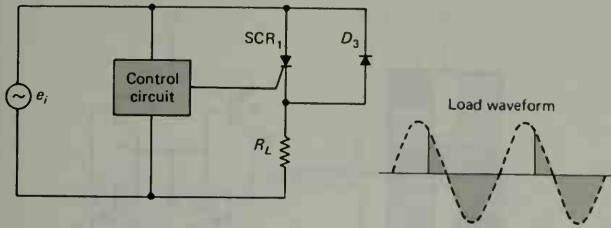
Figure 16-9. Phase-control circuit with rectifier.
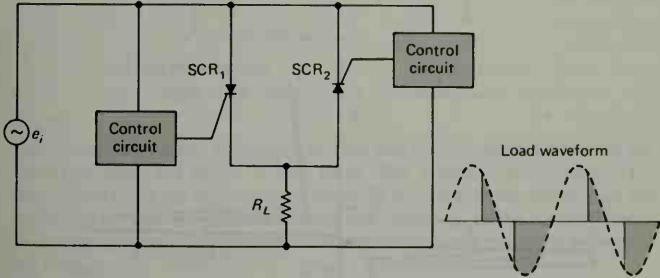
Figure 16-10. Inverse parallel connected SCR's.

It is seen that the TRIAC can be made to conduct in either direction. No matter what the bias polarity, the characteristics for the TRIAC are those of a forward-biased SCR [Fig. 16-11(c)].

A TRIAC control is shown in Fig. 16-12. Note that the circuit symbol is composed of two inverse connected SCR symbols. During the positive half-cycle of the input voltage, diode D_1 is forward biased, D_2 is reverse biased, and the gate terminal is positive with respect to A_1. During the negative half-cycle, D_1 is reverse biased and D_2 is forward biased, so that the gate becomes positive with respect to A_2. Adjustment of R_1 controls the point at which conduction commences.

A DIAC is simply a TRIAC without a gate terminal. Switch on is effected by raising the applied voltage to the breakover voltage. The DIAC characteristics and symbol are shown in Fig. 16-13.

16-7
Other Four-
Layer
Devices

16-7.1
*The Four-
Layer Diode*

The *four-layer diode*, also called the *Shockley* diode after its inventor William Shockley, is essentially a low-current SCR without a gate. To switch the device on, the anode-to-cathode voltage must be increased to the

(a) Construction

(b) Equivalent circuit
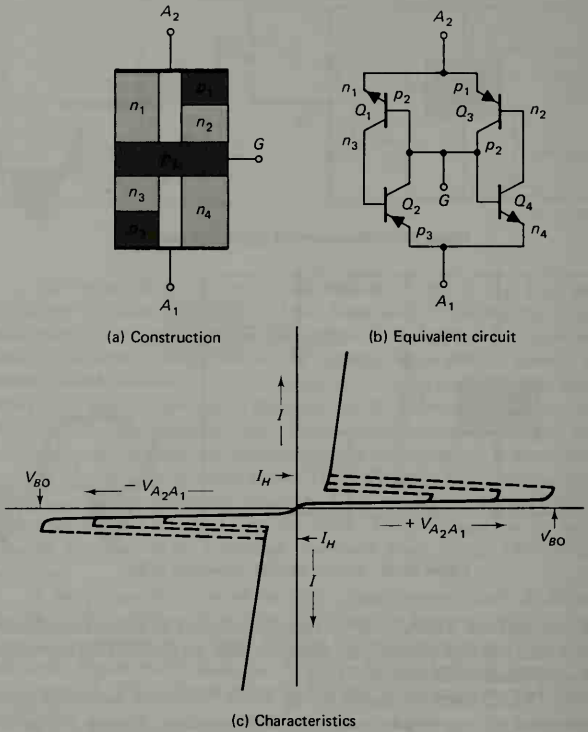
(c) Characteristics

Figure 16-11. TRIAC construction, equivalent circuit, and characteristics.

Load waveform
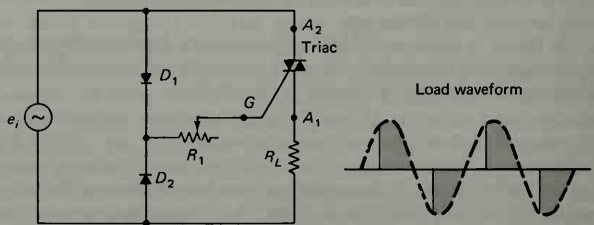
Figure 16-12. TRIAC control circuit.
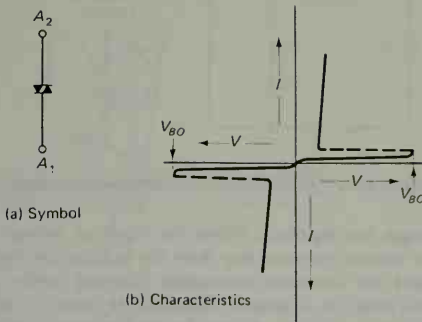
Figure 16-13. DIAC symbol and characteristics.

forward switching voltage. The circuit symbol and typical characteristics for the four-layer diode are shown in Fig. 16-14. The *forward switching voltage* (V_S) [Fig. 16-14(b)] is the equivalent of the SCR *forward breakover voltage*, and the minimum current at which the device will switch on is the *switching current* (I_S). *Holding current* (I_H) and *forward-conduction voltage* (V_F) are as defined for the SCR.

One application for the four-layer diode is the relaxation oscillator circuit shown in Fig. 16-15. In this circuit, capacitor C_1 is charged via resistance R_1 from supply E. Charging continues until the capacitor voltage reaches the diode switching voltage. The diode D_1 then conducts heavily and
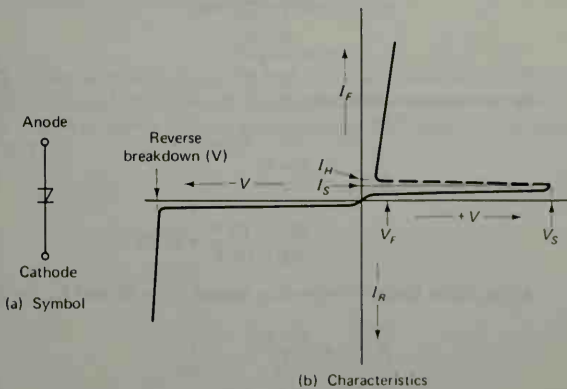
Figure 16-14. Four-layer diode symbol and characteristics.
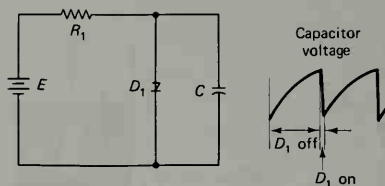
Figure 16-15. Relaxation oscillator using four-layer diode.

rapidly discharges the capacitor. When the capacitor voltage falls so low that the diode current becomes less than the holding current, the diode switches off and the capacitor commences charging again. The output voltage from the circuit is a sawtooth waveform as shown in the figure. For the circuit to function correctly, R_1 must be small enough to allow the diode switching current (I_S) to flow when the four-layer diode switches on. If the current through R_1 is less than I_S, the diode will not switch on. Also, R_1 must be large enough to prevent I_H from flowing when the capacitor is discharged. Otherwise, the four-layer diode will not switch off.

Example 16-3

The four-layer diode employed in the circuit of Fig. 16-15 has $V_S = 10$ V, $V_F = 1$ V, $I_S = 500$ μA, and $I_H = 1.5$ mA. If $E = 30$ V, calculate the minimum and maximum values of R_1 for correct operation of the circuit.

solution

Summing the voltages around the circuit,

$$E = (I \times R_1) + V_C$$

$$R_1 = \frac{E - V_C}{I}$$

At the diode switching voltage,

$$V_C = V_S, \qquad I_{(min)} = I_S$$

$$R_{1(max)} = \frac{E - V_S}{I_S} \tag{16-3}$$

$$= \frac{30\text{ V} - 10\text{ V}}{500 \times 10^{-6}} = 40 \text{ k}\Omega$$

At the diode forward conducting voltage, $V_C = V_F$ and $I_{(max)} = I_H$.

$$R_{1(min)} = \frac{E - V_F}{I_H} \tag{16-4}$$

$$= \frac{30\text{ V} - 1\text{ V}}{1.5\text{ mA}} = 19.3 \text{ k}\Omega$$

(a) Characteristics　　　　　　　　(b) Symbol
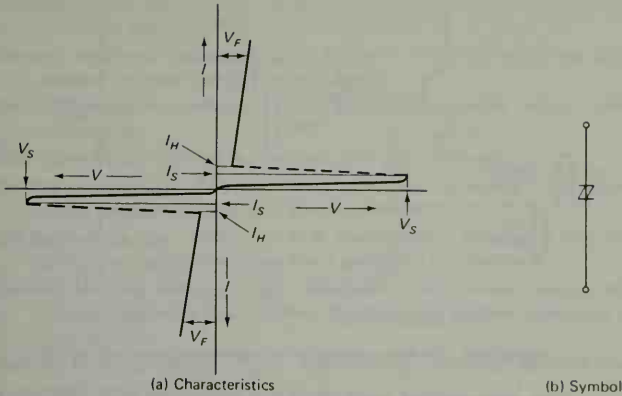
Figure 16-16. Characteristics and symbol for bilateral four-layer diode.

The four-layer diode discussed in Section 16-7.1 is sometimes referred to as a *unilateral four-layer diode*, because it is a one-way device. A *bilateral four-layer diode*, as the name suggests, is a two-way device. In construction, a *bilateral four-layer diode* is simply two inverse parallel connected unilateral four-layer diodes contained in one package. The bilateral device forward and reverse characteristics are each identical to the forward characteristics of the unilateral device [Fig. 16-16(a)]. The circuit symbol used for the bilateral four-layer diode as shown in Fig. 16-16(b) is simply two inverse parallel connected unilateral four-layer diode symbols.

16-7.2
*Bilateral
Four-Layer
Diode*

The *silicon unilateral switch* (SUS) and the *silicon bilateral switch* (SBS) are essentially unilateral and bilateral four-layer diodes, respectively, with the addition of gate terminals. Circuit symbols for the SUS and SBS are shown in Fig. 16-17.

16-7.3
*The SUS
and SBS*
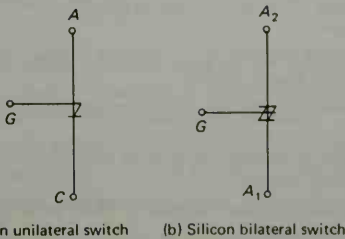
(a) Silicon unilateral switch　　　(b) Silicon bilateral switch

Figure 16-17. Circuit symbols for SUS and SBS.
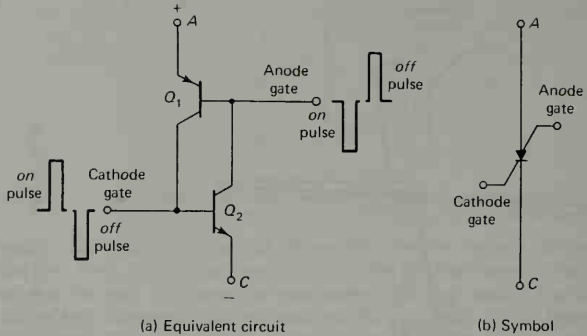
Figure 16-18. Silicon-controlled switch equivalent circuit and symbol.

**16-7.4
The
Silicon-
Controlled
Switch**

The *silicon-controlled switch* (SCS) is a low-current SCR with two gate terminals. An anode gate is provided as well as the cathode gate. In the two-transistor equivalent circuit shown in Fig. 16-18(a), it is seen that a negative pulse at the anode gate causes Q_1 to switch on. Q_1 collector supplies base current to Q_2 and both transistors switch on. Similarly, a positive pulse at the cathode gate can switch the device on. Since only small currents are involved, the SCS may be switched off by an appropriate polarity pulse at one of the gates. At the cathode gate a negative pulse is required for switch off, while at the anode gate a positive pulse is necessary. The SCS circuit symbol is shown in Fig. 16-18(b).

*Glossary of
Important
Terms*

SCR. Silicon controlled rectifier—a rectifier with a control element that determines the anode-to-cathode voltage at which the device commences to conduct.

Gate. Control element on SCR.

Thyristor. Collective name for SCR-type devices.

***pnpn* device.** Another name for SCR-type devices.

Four-layer device. Another name for SCR-type devices.

Latching. The ability of the SCR to remain on after the triggering current is removed.

Reverse blocking current, I_{RX}. A small leakage current that flows when the SCR is reverse biased.

Reverse breakdown voltage. Reverse voltage at which an SCR breaks down.

Reverse blocking region. Region of SCR reverse characteristics before breakdown occurs.

Forward blocking region. Region of SCR forward characteristics before switch on occurs.

Forward leakage current, I_{FX}. A small leakage current that flows before switch on when the SCR is forward biased.

Forward breakover voltage, $V_{F(BO)}$. Forward voltage at which an SCR switches on when the gate current is zero.

Forward conduction voltage, V_F. SCR anode-to-cathode voltage when conducting.

Gate current, I_G. Current flowing into SCR gate terminal.

Holding current, I_{HO}. Minimum SCR anode current required to keep the device conducting when gate is open circuited.

Holding current, I_{HX}. Minimum SCR anode current required to keep the device conducting when gate has a specified bias resistance.

Forward blocking voltage, V_{FOM}. Maximum SCR forward voltage that may be applied without causing the device to conduct when gate is open circuited.

Forward blocking voltage, V_{FXM}. Same as V_{FOM} but with specified bias resistance at gate.

Reverse blocking voltage, V_{ROM}. Maximum SCR reverse voltage that may be applied without causing breakdown when gate is open circuited.

Reverse blocking voltage, V_{RXM}. Same as V_{ROM} but with specified bias resistance at gate.

Average forward current, $I_{F(av)}$. Maximum permissible SCR average forward current.

RMS forward current, I_f. Maximum permissible SCR rms forward current.

Peak one-cycle surge current, $I_{FM(surge)}$. Nonrepetitive forward current that can safely flow for one cycle.

TRIAC. Two inverse parallel connected SCR's with a common gate, contained in one package.

DIAC. Similar to a TRIAC but without a gate terminal.

Four-layer diode. Low-current SCR without gate.

Shockley diode. Same as *four-layer diode*.

Forward switching voltage, V_S. Forward voltage at which four-layer diode commences conduction.

Switching current, I_S. Minimum forward current for four-layer diode to commence conduction.

Unilateral four-layer diode. Another name for the four-layer diode.

Bilateral four-layer diode. Two-way device—two inverse parallel connected unilateral four-layer diodes in one package.

SUS. Silicon unilateral switch—unilateral four-layer diode with a gate.

SBS. Silicon bilateral switch—bilateral four-layer diode with a gate.

SCS. Silicon-controlled switch—low current SCR with anode gate and cathode gate.

16-1. Sketch the construction of a silicon-controlled rectifier. Also sketch the two-transistor equivalent circuit and show how it is derived from the SCR construction. Label all terminals and explain how the device operates.

16-2. Sketch typical SCR forward and reverse characteristics. Identify all regions of the characteristics and all important current and voltage levels. Explain the shape of the characteristics in terms of the SCR two-transistor equivalent circuit.

16-3. Sketch SCR phase control circuits for:
(a) 90° phase control.
(b) 180° phase control.
In each case show the load waveform and explain the circuit operation.

16-4. Show how an additional rectifier (not SCR) may be connected to provide extra load current in the circuits of Question 16-3. Show the effect on the load waveforms and briefly explain.

16-5. Draw an SCR control circuit using two SCR's to provide phase control for positive and negative half-cycles of the supply voltage.

16-6. Draw sketches to show the construction, equivalent circuit, and characteristics of a TRIAC. Identify all important voltage and current levels on the characteristics and explain the operation of the device.

16-7. Sketch a TRIAC control circuit. Show the load waveform and explain the operation of the circuit.

16-8. Sketch the characteristics and circuit symbols and briefly explain the following:
(a) DIAC.
(b) Four-layer diode.
(c) Bilateral four-layer diode.

16-9. (a) Sketch the circuit of a relaxation oscillator using a four-layer diode, and explain its operation.
(b) Sketch the circuit symbols and briefly explain (1) SUS, (2) SBS, and (3) SCS.

16-1. A C6G SCR (data in Fig. 16-4) is employed to switch a 115 V ac supply to a load. Determine the minimum load resistance that may be supplied. If the SCR has a 2.2 kΩ bias resistor at the gate, estimate the required gate trigger voltage and current. Also calculate the instantaneous supply voltage at which the device switches off.

16-2. A load resistance of 33 Ω is supplied from an ac source of 60 V peak. Current to the load is to be switched on and off by an SCR triggered by a 10 μs input pulse.
(a) Sketch the complete circuit.

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(b) Select a suitable SCR from the specifications in Figs. 16-4 and 16-5.

(c) If the gate bias resistance $R_G = 1$ kΩ, specify the required trigger voltage and current.

(d) Determine the supply voltage at which the SCR will switch off.

16-3. An SCR with a 115-V ac supply controls the current through a 150-Ω load resistor. A 90° phase-control circuit is employed to trigger the SCR anywhere between 12° and 90°. The gate trigger current is 50 μA. Calculate the value of the variable resistance, specify the diode required, and select a suitable SCR from the C6 range.

16-4. The circuit in Fig. 16-7 has an ac supply of 30 V rms and $R_L = 20$ Ω. Determine the range of adjustment of R_1 for the SCR to be triggered on anywhere between 7.5° and 90°. The gate trigger current is 500 μA and the gate voltage is 0.6 V.

16-5. For Problem 16-4 the SCR holding current is 1 mA. Calculate the instantaneous input voltage at which it will switch off.

16-6. The four-layer diode employed in the circuit of Fig. 16-15 has $V_S = 8$ V, $I_S = 600$ μA, and $I_H = 1$ mA. If $E = 40$ V, calculate the minimum and maximum values of R_1 for correct operation of the circuit.

16-7. A four-layer diode is used in a relaxation oscillator which has a 25-V supply, a 1-μF capacitor, and a 12-kΩ series resistor, (see Fig. 16-15). The capacitor is to charge up to 15 V, and then discharge to approximately 1 V. Specify the four-layer diode in terms of forward conduction voltage, forward switching voltage, switching current, and holding current.

16-8. Design a 10° to 90° phase-control circuit to control a 1-kW heater. The supply voltage is 120 V. Select a suitable SCR from the specifications in Figs. 16-4 and 16-5.

16-9. A light dimmer uses a TRIAC with a control circuit by means of which the device can be triggered on anywhere between the 5° and 90° points on the input waveform. The supply voltage is 220 V and the total (lighting) load is 750 W. Assuming that the TRIAC gate triggering current is 200 μA, design a suitable circuit and specify all components.

16-10. A TRIAC circuit as in Fig. 16-12 has $e_1 = 150$ V, $R_L = 100$ Ω, and $R_1 = 100$kΩ to 2 kΩ. Determine the minimum points at which the TRIAC can be triggered on. Specify all components.

17

The
Unijunction
Transistor

17-1
Introduction

The operation of a *unijunction transistor* (UJT) is quite different from that of bipolar and field effect transistors although it is a three-terminal device. The device input, called the emitter, has a resistance which rapidly decreases when the input voltage reaches a certain level. This is termed a *negative resistance characteristic*, and it is the characteristic which makes the UJT useful in timing and oscillator circuits.

17-2
Theory of
Operation

Basically, the unijunction transistor (also known as a *double-base diode*) consists of a bar of lightly doped n-type silicon with a small piece of heavily doped p-type material joined to one side. The concept is illustrated in Fig. 17-1(a). The end terminals of the bar are designated *base* 1 (B_1) and *base* 2 (B_2) as shown, and the p-type region is termed the emitter (E). Since the silicon bar is lightly doped it has a high resistance, and it can be represented as two resistors, r_{B1} from B_1 to C and r_{B2} from B_2 to C as shown in Fig. 17-1(b). The sum of r_{B1} and r_{B2} is designated R_{BB}. The p-type emitter forms

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(a) Basic construction   (b) Equivalent circuit
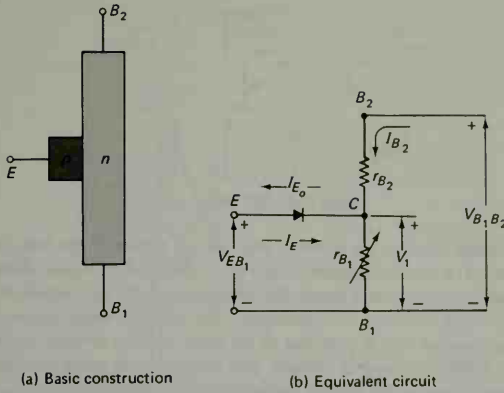
Figure 17-1. Basic construction and equivalent circuit of unijunction transistor.

a pn-junction with the n-type silicon bar, and this is represented by a diode
in the equivalent circuit.

With a voltage V_{B1B2} applied as shown, the voltage at the junction of
r_{B1} and r_{B2} is

$$V_1 = V_{B1B2} \times \frac{r_{B1}}{r_{B1} + r_{B2}}$$

$$= V_{B1B2} \times \frac{r_{B1}}{R_{BB}} \tag{17-1}$$

where $R_{BB} = r_{B1} + r_{B2}$.

V_1 is also the voltage at the cathode of the diode representing the
pn-junction. While the emitter terminal is open circuited, the only current
flowing is

$$I_{B2} = \frac{V_{B1B2}}{R_{BB}} \tag{17-2}$$

If the emitter terminal is grounded, the pn-junction is *reverse* biased and
a small *emitter reverse current* (I_{EO}) flows.

Now consider what happens when the emitter input voltage (V_{EB1}) is
slowly increased from zero. As V_{EB1} becomes equal to V_1, I_{EO} will be reduced
to zero. With equal voltage levels on each side of the diode, no reverse
current or forward current will flow. With a further increase in V_{EB1} the
pn-junction becomes forward biased, and a forward emitter current I_E begins
to flow from the emitter terminal into the n-type silicon bar. When this
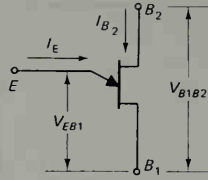
Figure 17-2. UJT circuit symbol.

occurs, charge carriers are injected into the r_{B1} region of the bar. Since the resistance of a semiconductor material is dependent upon doping, the additional charge carriers cause the resistance of the r_{B1} region to rapidly decrease. With decrease in resistance, the voltage drop across r_{B1} also decreases, causing the *pn*-junction to be more heavily forward biased. This results in a greater forward current, and consequently more charge carriers are injected causing still further reduction in the resistance of the r_{B1} region. The input voltage is also "pulled down," and the input current (I_E) is increased to a limit determined by the source resistance. The device remains in this *on* condition until the input is open circuited or until I_E is reduced to a very low level.

The circuit symbol for a UJT is shown in Fig. 17-2. As always, the arrowhead points in the conventional current direction for a forward-biased junction. In this case it points from the *p*-type emitter to the *n*-type bar. The voltage polarities and current directions for operation of the device are also shown.

17-3
UJT
Characteristics

A plot of emitter voltage (V_{EB1}) versus emitter current (I_E) gives the emitter characteristics shown in Fig. 17-3.

When $I_{B2} = 0$, (i.e., $V_{B1B2} = 0$), $V_1 = 0$ and a small increase in V_E forward biases the emitter junction. The resultant plot of V_E and I_E is simply the characteristic of a forward-biased diode with some series resistance. When V_{B1B2} is appriximately 20 V and $V_E = 0$, the emitter junction is reverse biased and the emitter reverse current (I_{EO}) flows as shown at point 1 on the characteristics. Increasing V_{EB1} reduces the emitter junction reverse bias. When $V_E = V_1$ [see Fig. 17-1(b)], there is no reverse or forward bias and $I_E = 0$. This gives point 2 on the characteristic. Increasing V_{EB1} beyond this point begins to forward bias the emitter junction. At the peak point where $V_{EB1} = V_1$ the junction is just forward biased, and a very small forward emitter current is flowing. This is termed the *peak current* I_P. Up until this point, the UJT is said to be operating in the *cutoff region*. When I_E increases beyond I_P the device enters the *negative resistance region*, in which the resistance of r_{B1} falls rapidly and V_E falls to the *valley voltage* V_v. V_v is determined by the forward-biased emitter *diode voltage* V_D and by the *saturation resistance* r_s of r_{B1}. At this point I_E equals the *valley current* (I_v). A further increase of I_E
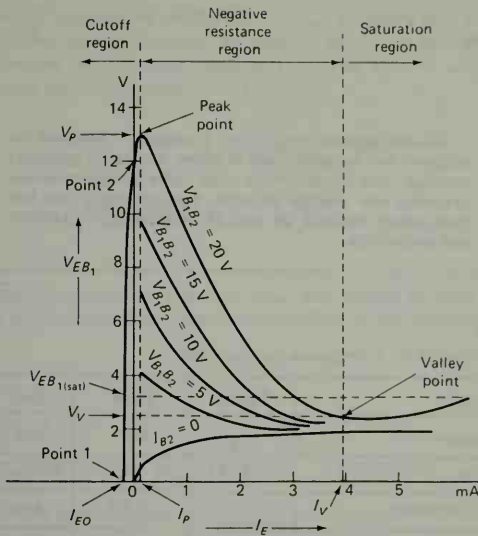
Figure 17-3. UJT emitter characteristics.

causes the device to enter the *saturation region*, where V_E is equal to the sum of V_D and $(I_E \times r_S)$.

When V_{BB} is reduced below 20 V, V_1 will also be reduced and the UJT will switch on at a lower value of V_E. Thus, using various levels of V_{BB}, a family of V_{EB1}/I_E characteristics for a given UJT can be plotted as shown in Fig. 17-3.

17-4
UJT
Parameters
and
Specification

17-4.1
Interbase
Resistance,
R_{BB}

The *interbase resistance* (R_{BB}) is the sum of r_{B1} and r_{B2} when the emitter current is zero. Consider Fig. 17-4 showing a portion of the manufacturer's data sheet for 2N4948 and 2N4949 UJT's. R_{BB} is specified as 7 kΩ typical, 4 kΩ minimum, and 12 kΩ maximum. R_{BB} is very sensitive to temperature variations, and an *interbase resistance temperature coefficient* (αR_{BB}) is usually specified on data sheets. For the 2N4948, αR_{BB} can be as large as 0.9%/°C.

Silicon annular unijunction transistors designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity.

CASE 22A
(TO-18 Modified)
(Lead 3 connected to case)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	360*	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	1.0**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	-65 to +200	°C

* Derate 2.4 mW/°C increase in ambient temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) Note 1 2N4948 2N4949	η	0.55 0.74	- -	0.62 0.86	-
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0) 2N4948, 2N4949	R_{BB}	4.0	7.0	12.0	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65°C to +100°C)	αR_{BB}	0.1	-	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	$V_{EB1(sat)}$	-	2.5	3.0	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	12	15	-	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0) (V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)	I_{EB2O}	- -	5.0 -	10 1.0	nA µA
Peak Point Emitter Current (V_{B2B1} = 25 V) 2N4948 2N4949	I_p	- -	0.6 0.6	2.0 1.0	µA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2 2N4948, 2N4949	I_V	2.0	4.0	- -	mA

Figure 17-4. Portion of UJT data sheet. (Courtesy of Motorola, Inc.)

This is a positive temperature coefficient; i.e., R_{BB} increases with temperature increase. The value of R_{BB} together with the maximum power dissipation P_D determines the maximum value of V_{B1B2} that may be used. With $I_E = 0$, maximum power dissipated in the UJT is

$$P_D = \frac{(V_{B1B2})^2}{R_{BB}}$$

$$\text{maximum } V_{B1B2} = \sqrt{R_{BB} \times P_D} \qquad (17\text{-}3)$$

Determine the maximum value of V_{B1B2} that should be used with a 2N4948 UJT (a) at an ambient temperature of 25°C; (b) for operation up to 100°C.

Example 17-1

solution (a)

From Fig. 17-4, at 25°C,

$$P_D = 360 \text{ mW}, \qquad R_{BB} = 4 \text{ k}\Omega(\text{min}), \qquad 12 \text{ k}\Omega(\text{max})$$

To give the lowest possible value of $V_{B1B2(\text{max})}$ use $R_{BB(\text{min})}$.

$$V_{B1B2(\text{max})} = \sqrt{4 \text{ k}\Omega \times 360 \text{ mW}} \approx 38 \text{ V}$$

This is larger than the *maximum emitter reverse voltage* (V_{B2E}) which is 30 V. Therefore, at 25°C, V_{B1B2} should not exceed 30 V.

solution (b)

at 100°C
First note, from Fig. 17-4, that P_D must be derated linearly at 2.4 mW/°C. The temperature increase from 25°C = (100 − 25)°C = 75°C.

at 75°C

$$P_D = 360 \text{ mW} - (2.4 \times 75) \text{ mW} = 360 - 180 \text{ mW} = 180 \text{ mW}$$

The minimum increase in R_{BB} is 0.1%/°C, from αR_{BB}. For a temperature increase of 75°C this is only a 7.5% increase in R_{BB}, so for calculation of $V_{B1B2(\text{max})}$, ignore the R_{BB} increase.
From Eq. (17-3),

$$V_{B1B2(\text{max})} = \sqrt{4 \text{ k}\Omega \times 180 \text{ mW}} = 26.8 \text{ V}$$

The *intrinsic stand-off ratio*, which is represented by the symbol η (Greek letter eta), simply defines the ratio of r_{B1} to R_{BB}. Together with V_{B1B2} and the emitter junction voltage drop (V_D), η also determines the peak voltage V_P for the UJT.

From Eq. (17-1),

$$V_1 = V_{B1B2} \times \frac{r_{B1}}{r_{B1} + r_{B2}} = \eta V_{B1B2}$$

and the peak voltage is $V_D + V_1$.

$$V_P = V_D + \eta V_{B1B2} \qquad (17\text{-}4)$$

V_D is the forward voltage drop of a silicon diode, typically 0.7 V.

Example 17-2

Determine the minimum and maximum emitter voltages at which a 2N4948 UJT will trigger on (or fire) when $V_{B1B2} = 30$ V.

solution

From Fig. 17-4,

$$\eta = 0.55 \text{ min and } 0.82 \text{ max}$$

From Eq. (17-4)

$$V_{P(\min)} = 0.7 \text{ V} + (0.55 \times 30) = 17.2 \text{ V}$$

and

$$V_{P(\max)} = 0.7 + (0.82 \times 30) = 25.3 \text{ V}$$

Therefore, the device will fire at some emitter voltage between 17.2 and 25.3 V.

$V_{EB1(sat)}$ is the emitter input voltage when the UJT is in its saturation region. Therefore, it is the minimum level to which V_{EB1} falls when the UJT is triggered on. Since $V_{EB1(sat)}$ is affected by I_E and V_{B2B1}, it must be specified at given levels of I_E and V_{B2B1}. From Fig. 17-4, for $V_{B2B1} = 10$ V and $I_E = 50$ mA, $V_{EB1(sat)}$ for a 2N4948 is 2.5 V typical and 3.0 V maximum.

I_P was explained in Section 17-3. It is important as a lower limit to the emitter current. If the source resistance of the input voltage is so high that I_E

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is not greater than I_P, then the UJT will simply not trigger on (see Example 17-4).

This quantity was also explained in Section 17-3. It is important in some circuits as an upper limit to the emitter current. If the source resistance of the input voltage is so low that I_E is equal to or greater than I_V, then the device will remain on when triggered (see Example 17-4).

This is the value of current flowing into B_2 after the device is first fired. The current is said to be modulated by the UJT being fired.

The relaxation oscillator shown in Fig. 17-5 consists of a UJT and a capacitor C_1, which is charged via resistance R_E. When the capacitor voltage reaches V_P, the UJT fires and rapidly discharges C_1 to $V_{EB1(sat)}$. The device then cuts off and the capacitor commences charging again. The cycle is repeated continuously, generating a sawtooth waveform across C_1. The time (t) for the capacitor to charge from $V_{EB1(sat)}$ to V_P may be calculated, and the frequency of the sawtooth determined approximately as $1/t$. The discharge time (t_D) is difficult to calculate because the UJT is in its negative resistance region and its resistance is changing. However, t_D is normally very much less than t, and can be neglected for approximation.

The relaxation oscillator in Fig. 17-5 uses a 2N4948 UJT. Calculate the typical frequency of oscillation.

solution

The general equation for the charging time of a capacitor charged via a
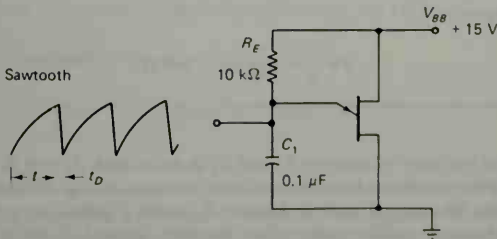
Figure 17-5. UJT relaxation oscillator.

series resistor is

$$t = 2.3\,CR\log\frac{E-E_o}{E-e_c} \tag{17-5}$$

where

C = capacitance in farads

R = resistance in ohms

E = supply voltage

e_c = capacitor voltage at time t

E_o = initial voltage on capacitor

Since the UJT is to fire at time t

$$e_c = V_P$$
$$= V_D + \eta V_{B1B2} \quad \left[\text{from Eq. (17-4)}\right]$$

From the data sheet (Fig. 17-4) a typical value of intrinsic stand-off ratio is $\eta = 0.7$. Also $V_D = 0.7$ V.

$$e_c = 0.7\text{ V} + (0.7 \times 15\text{ V})$$
$$= 0.7\text{ V} + 10.5\text{ V} = 11.2\text{ V}$$

When the UJT fires, the capacitor is discharged to $V_{EB1(\text{sat})}$. This is the capacitor voltage E_o at the start of each charging cycle. For the 2N4948, $V_{EB1(\text{sat})} = 2.5$ V typically.

$$E_o = 2.5\text{ V}$$

From Eq. (17-5),

$$t = 2.3 \times 0.1\ \mu\text{F} \times 10\ \text{k}\Omega \times \log\frac{15-2.5}{15-11.1}$$

$$= 2.3 \times 0.1 \times 10^{-6} \times 10 \times 10^3 \times \log\frac{12.5}{3.9} = 1.16\text{ ms}$$

The frequency is

$$f = \frac{1}{t} = \frac{1}{1.16}\ \text{ms} \approx 860\text{ Hz}$$

The inclusion of resistors R_1 and R_2 in series with B_1 and B_2 provides output *spike* waveforms from the oscillator as shown in Fig. 17-6. When the UJT fires, the surge of current through B_1 causes a voltage drop across R_1 and produces the positive-going spikes. Similarly, at the UJT firing time, the
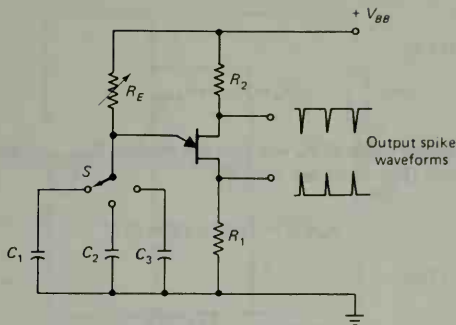
Figure 17-6. Variable frequency UJT relaxation oscillator.

fall of V_{EB1} causes I_{B2} to increase rapidly and generates the negative-going pulse across R_2. In practice, R_1 and R_2 should be much smaller than R_{BB} to avoid altering the UJT firing voltage. Typically, R_1 is selected less than 47 Ω, and R_2 is usually 200 to 300 Ω. A wide range of oscillation frequencies can be achieved by making R_E adjustable and including a switch to select different values of capacitance.

For correct operation of the UJT there is an upper and lower limit to the signal source resistance. For the UJT to fire in the circuit of Fig. 17-6, a minimum current level equal to I_P must flow through R_E when the emitter voltage is V_P.

The upper limit on R_E is

$$R_{E(\max)} = \frac{V_{BB} - V_P}{I_P} \qquad (17\text{-}6)$$

For the relaxation oscillator, R_E must be large enough to prevent the valley current from flowing continuously; otherwise, the UJT will not switch off again.

The lower limit on R_E is

$$R_{E(\min)} = \frac{V_{BB} - V_{EB1(\text{sat})}}{I_V} \qquad (17\text{-}7)$$

The circuit of Fig. 17-6 uses a 2N4948 UJT. If V_{BB} is 15 V, determine the maximum and minimum values for R_E. **Example 17-4**

solution

From Eq. (17-4),

$$V_P = V_D + \eta V_{B1B2}$$

The largest value of V_P will give the smallest $R_{E(\max)}$. Therefore, from the data sheet (Fig. 17-4), use $\eta = 0.82$.

$$V_P = 0.7 + (0.82 \times 15) = 13 \text{ V}$$

From Eq. (17-6),

$$R_{E(\max)} = \frac{V_{BB} - V_P}{I_P}$$

For smallest $R_{E(\max)}$, use maximum I_P. From the data sheet (Fig. 17-4), $I_{P(\max)} = 2 \ \mu A$.

$$R_{E(\max)} = \frac{15 \text{ V} - 13 \text{ V}}{2 \ \mu A} = 1 \text{ M}\Omega$$

From Eq. (17-7)

$$R_{E(\min)} = \frac{V_{BB} - V_{EB1(sat)}}{I_V}$$

For the largest value of $R_{E(\min)}$, use minimum $V_{EB1(sat)}$ and minimum I_V. Deriving these values from the data sheet,

$$R_{E(\min)} = \frac{15 \text{ V} - 2.5 \text{ V}}{2 \text{ mA}} = 6.25 \text{ k}\Omega$$

In practice, R_E should be selected somewhere between the upper and lower limits.

17-6
UJT Control
of SCR

Unijunction transistors are frequently employed for control of SCR's. In the typical circuit, shown in Fig. 17-7(a), the SCR is triggered on by the voltage drop across R_1 when the UJT fires. Diode D_1 allows the positive half-cycle of the supply to charge C_1 via R_E. D_1 also isolates the UJT circuit from the negative half-cycles of the input. By adjusting R_E, the charging rate of C_1, and therefore the UJT firing time, can be selected. The waveforms in Fig. 17-7(b) show that almost 180° of control of SCR triggering is possible.
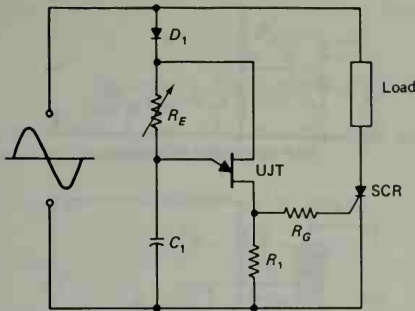
(a) Circuit for UJT control of SCR
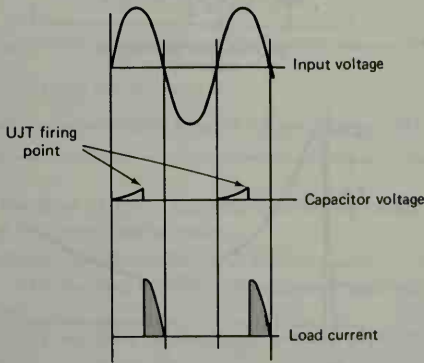
(b) Waveforms

Figure 17-7. Circuit and waveforms for UJT control of SCR.

The *programmable unijunction transistor* (PUT) is not a unijunction transistor at all, but an SCR-type device used in a particular way to simulate a UJT. For the simulated UJT the interbase resistance (R_{BB}) and the intrinsic stand-off ratio (η) may be programmed to any desired values by selecting two resistors. This means that the device firing voltage (the peak voltage V_P) can also be programmed.

Consider Fig. 17-8. The *pnpn* device shown in Fig. 17-8(a) has its gate connected to the junction of resistors R_1 and R_2. The four-layer construction in Fig. 17-8(b) shows that the anode–gate junction is forward biased when the anode becomes positive with respect to V_G. When this occurs the device is triggered on. The anode-to-cathode voltage then drops to a low level, and
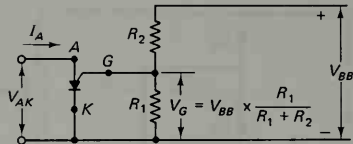
(a) Programmable UJT circuit
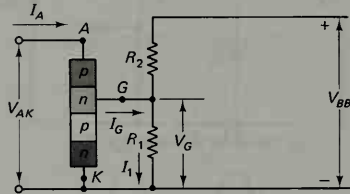
(b) Four-layer construction
of programmable UJT
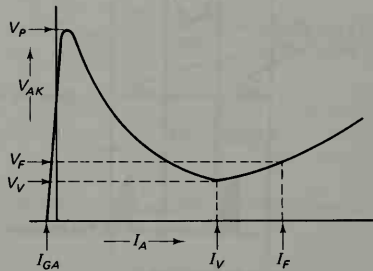
(c) Characteristic of
programmable UJT

Figure 17-8. Circuit, four-layer construction, and characteristic of programmable UJT.

the device conducts heavily until the input voltage becomes too low to sustain conduction. It is seen that this action simulates the performance of a UJT. The anode of the device acts as the UJT emitter, and R_1 and R_2 operate as r_{B1} and r_{B2}, respectively. R_{BB}, η, and V_P are programmed by the selection of R_1 and R_2. The typical characteristic of a programmable UJT is shown in Fig. 17-8(c).

Example 17-5   A programmable UJT has a forward voltage (V_F) of 1 V when on, and requires a gate trigger current (I_G) of 0.1 mA. η is to be programmed to 0.7. Using a 20 V supply, determine R_1 and R_2. Also calculate V_P, V_V, and R_{BB}.

$$\eta = \frac{R_1}{R_1 + R_2} = 0.7$$

$$V_{R_1} = \eta \times V_{BB} = 0.7 \times 20 \text{ V} = 14 \text{ V}$$

If I_1 is too small, V_G may be significantly altered when I_G flows. To ensure a stable V_G level, make $I_1 \geqslant 10 I_G$.

$$I_1 = 10 \times 0.1 \text{ mA} = 1 \text{ mA}$$

$$R_1 = \frac{V_G}{I_1} = \frac{14 \text{ V}}{1 \text{ mA}} = 14 \text{ k}\Omega$$

$$R_2 = \frac{20 \text{ V} - 14 \text{ V}}{1 \text{ mA}} = 6 \text{ k}\Omega$$

$$R_{BB} = R_1 + R_2 = 20 \text{ k}\Omega$$

$V_P = V_D + \eta V_{BB}$, where V_D (anode-to-gate forward voltage drop) is about 0.7 V.

$$V_P = 0.7 + (0.7 \times 20) = 14.7 \text{ V}$$

V_V = anode-to-cathode forward voltage drop $\approx V_F = 1$ V

Unijunction transistor (UJT).   Three-terminal device having one *pn*-junction and an *n*-type resistive region.

Double-base diode.   Another name for a UJT.

Base 1, B_1.   UJT terminal to which the negative terminal of supply is connected.

Base 2, B_2.   UJT terminal to which the positive terminal of supply is connected.

Emitter, E.   UJT input terminal.

r_{B1}.   Resistance of *n*-type region between junction cathode and B_1 of UJT.

r_{B2}.   Resistance of *n*-type region between junction cathode and B_2 of UJT.

Interbase resistance, R_{BB}.   Resistance of UJT measured between B_1 and B_2 —sum of r_{B1} and r_{B2}.

V_{EB1}.   UJT input voltage applied between B_1 and E.

Peak point emitter current, I_P.   UJT emitter current at peak point on characteristic—emitter current at instant of firing.

Valley point current, I_V.   UJT emitter current at valley point on characteristic.

Peak voltage, V_P.   UJT emitter-to-B_1 voltage at instant of firing.

Valley voltage, V_V.   UJT emitter-to-B_1 voltage at valley point on characteristic.

Saturation resistance, r_S.   Resistance of r_{B1} after UJT has fired.

Cutoff region. Region of UJT characteristics before junction becomes forward biased.

Negative resistance region. Region of UJT characteristic between peak point and valley point.

Saturation region. Region of UJT characteristic after device has fired —beyond valley point.

Intrinsic stand-off ratio. Ratio r_{B1}/R_{BB}—determines emitter-to-B_1 voltage at which UJT fires.

Emitter saturation voltage, $V_{EB1(sat)}$. Emitter-to-B_1 voltage of UJT in saturation region.

Modulated interbase current, $I_{B2(mod)}$. Current flowing into B_2 after UJT has fired.

Programmable UJT, PUT. SCR-type device which simulates a UJT.

Review Questions

17-1. Draw sketches to show the basic construction and equivalent circuit of a unijunction transistor. Briefly explain the operation of the UJT.

17-2. Sketch typical UJT emitter characteristics for $I_{B2}=0$, $E_{B1B2}=20$ V, and $E_{B1B2}=5$ V. Identify each region and all important points on the characteristics, and explain their shape.

17-3. Sketch the circuit of a UJT relaxation oscillator with provision for frequency adjustment and spike waveform. Show all waveforms and explain the operation of the circuit.

17-4. Sketch a UJT circuit for control of an SCR. Also sketch input, capacitor, and load waveforms, and briefly explain how the circuit operates.

17-5. Using illustrations explain the operation of a programmable unijunction transistor. Sketch a typical characteristic for the device and explain how the intrinsic stand-off ratio may be programmed.

Problems

17-1. Determine the maximum value of power dissipation for a 2N4948 UJT operating at an ambient termperature of 125°C. Also determine the maximum value of V_{B1B2} that may be used at 125°C. The condensed data sheet for the 2N4948 is shown in Fig. 17-4.

17-2. Calculate the minimum and maximum values of V_{EB1} at which a 2N4948 UJT will trigger on when $V_{B1B2}=20$ V.

17-3. A relaxation oscillator uses a 2N4948 UJT and has $V_{BB}=25$ V. The capacitor employed has a value of 0.5 μF and the charging resistance is 33 kΩ. Calculate the typical oscillation frequency.

17-4. For the circuit of Problem 17-3, calculate the maximum and minimum values of capacitor charging resistance which will sustain oscillations.

17-5. A programmable UJT operating from a 25-V supply has $V_F = 1.5$ V and $I_G = 0.05$ mA. Determine the values of R_1 and R_2 to program η to 0.75. Also calculate V_P, V_V, and R_{BB}.

17-6. A UJT relaxation oscillator to have a frequency of 3 kHz is to operate from a 20-V supply. A 3-μF capacitor is employed, and the maximum and minimum output voltages are to be 7.5 and 1 V, respectively. Determine a suitable value of series resistance, and specify the UJT in terms of intrinsic stand-off ratio and valley voltage.

17-7. A UJT relaxation oscillator has a 30-V dc supply, a 5-μF capacitor, and a 12-kΩ charging resistor. If η ranges from 0.65 to 0.73 and $V_v = 1.5$ V, determine the maximum and minimum values of oscillating frequency and peak output voltage.

17-8. The UJT in Problem 17-3 is to be replaced with a PUT. Determine suitable values for R_1 and R_2, and specify the PUT.

17-9. A programmable UJT has a forward voltage of $V_F \simeq 0.9$ V when on. The gate trigger current is $I_G = 200$ μA. The device is to be programmed to switch on at $V_G = 15$ V when operating from a 24-V supply. Determine suitable values for R_1 and R_2, and calculate V_P, V_v, and R_{BB}.

Optoelectronic Devices

Optoelectronic devices are light-operated devices (photoelectric), light-emitting devices, or devices which modify light.

Photoelectric devices can be categorized as *photoemissive*, *photoconductive*, or *photovoltaic*. In photoemissive devices, radiation falling upon a cathode causes electrons to be emitted from the cathode surface. In photoconductive devices, the resistance of a material is changed when it is illuminated. Photovoltaic cells generate an output voltage proportional to radiation intensity.

Any light source emits energy only over a certain range of frequencies or wavelengths. A graph of energy output plotted versus either frequency or wavelength is termed the *emission spectrum* for the source. An electronic device which is affected by light is sensitive only to a certain range of radiation frequencies. A graph of device current, voltage, or resistance plotted versus radiation frequency is known as its *spectral response*. For a given photosensitive material there is a minimum radiation frequency (or maximum wavelength) that can produce a photoelectric affect; this is known as the *threshold frequency* or *threshold wavelength*.

The total light energy output, or *luminous flux*, from a source can be measured in *milliwatts* (mW) or in *lumens* (lm).

$$1 \text{ lm} = 1.496 \text{ mW}$$

Light intensity is the amount of light that falls on a unit area. Light intensity is expressed in *milliwatts per square centimeter* (mW/cm^2), in *lumens per square meter* (lm/m^2), or in the older unit *lumens per square foot* (lm/ft^2) which is also known as a *foot candle* (fc).

$$1 \text{ fc} = 10.764 \text{ lm}/m^2$$

The light intensity of sunlight on the earth at noon on a clear day is approximately 10,000 fc, or 107,640 lm/m^2. Using 1 lm = 1.496 mW, sunlight intensity becomes 161 W/m^2.

Consider a point source which emits light evenly in all directions. To determine the light intensity at a given distance from the source, it is necessary to consider the surface area of a sphere surrounding the source.

At a distance of 1 m from the source the luminous flux is spread over a total surface area of a sphere with a radius of 1 m.

$$\text{Surface area of sphere} = 4\pi r^2$$

$$\text{Light intensity} = \frac{\text{luminous flux}}{4\pi r^2} \qquad (18\text{-}1)$$

Calculate the light intensity at a distance of 3 m from a lamp which emits 25 W of light energy. Also determine the total luminous flux which strikes an area of 0.25 cm^2 at 3 m from the lamp.

Example 18-1

solution

From Eq. (18-1),

$$\text{Light intensity} = \frac{25 \text{ W}}{4\pi \times (3\text{m})^2}$$

$$= 221 \text{ mW}/m^2 = 221 \times 10^{-4} \text{ mW}/cm^2$$

$$\text{Total flux} = (\text{flux per unit area}) \times (\text{area})$$

$$= (\text{light intensity}) \times (\text{area})$$

$$= (221 \times 10^{-4} \text{ mW}/cm^2) \times (0.25 \text{ cm}^2)$$

$$\simeq 5.5 \text{ mW}$$

Light energy is an electromagnetic radiation; i.e., it is in the form of electromagnetic waves. Therefore, it can be defined in terms of *frequency* or *wavelength* as well as intensity. Wavelength, frequency, and velocity are related by the equation

$$c = f\lambda \qquad (18\text{-}2)$$

where c = velocity

$= 3 \times 10^8$ m/s for electromagnetic waves

f = frequency in Hz

λ = wavelength in meters

Visible light ranges approximately from violet at 380 nm (380 nanometers or 380×10^{-9} m) to red at 720 nm. From Eq. (18-2), the frequency extremes are

and

$$f = \frac{c}{\lambda} = \frac{3 \times 10^8}{380 \times 10^{-9}} \simeq 8 \times 10^{14} \text{ Hz}$$

$$f = \frac{3 \times 10^8}{720 \times 10^{-9}} \simeq 4 \times 10^{14} \text{ Hz}$$

18-3
Photo-
multiplier
Tube

Although many solid-state photoelectric devices are available today, the photomultiplier tube is still widely applied, mainly because it is an extremely sensitive device. A *photomultiplier tube* consists of an evacuated glass envelope containing a *photocathode*, an *anode*, and several additional electrodes termed *dynodes*. Figure 18-1 illustrates the principle of the photomultiplier. Radiation striking the photocathode imparts energy to electrons within the surface material of the cathode. When the radiation frequency exceeds the threshold frequency of the cathode material, electrons are emitted from the surface. The emitted electrons (negative charge carriers) are accelerated toward dynode 1 by the positive potential on that dynode. The dynodes have surfaces which facilitate *secondary emission*. Thus, if the electrons strike the surface of dynode 1 with sufficient energy, *secondary* electrons are knocked out of the surface and are accelerated toward the more positive dynode 2. Each electron which strikes dynode 2 produces more secondary electrons, which are then accelerated to dynode 3, and so on.

The electrons emitted from the dynode surface are termed *secondary electrons* to distinguish them from the *primary* or *incident electrons*. The energy of the incident electrons depends upon the voltage applied to accelerate them, i.e., the dynode voltage. Since there are many more secondary electrons than primary electrons, the original photoemission current is amplified, or, in other words, the number of electrons is multiplied.
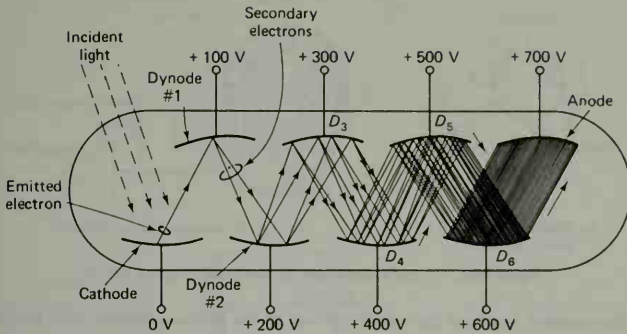
Figure 18-1. Principle of photomultiplier tube.

After moving from dynode 1 to dynode 2 and successive dynodes, the electrons are finally collected at the anode. In this way photoemission currents of the order of microamperes are converted to more useful milli-ampere levels. Current amplifications of up to 10^6 are possible, depending upon the number of dynodes employed.

The characteristics of a typical photomultiplier tube are shown in Fig. 18-2. High voltages are required to operate the device. The anode voltages used with various photomultiplier tubes range from 500 to 5000 V. The *dark current*, which flows when the cathode is not illuminated, results from *thermal emission* and the influence of the high-voltage electrodes. For incident illumination of a given wavelength the number of emitted electrons is directly proportional to the illumination intensity. Thus, for a particular
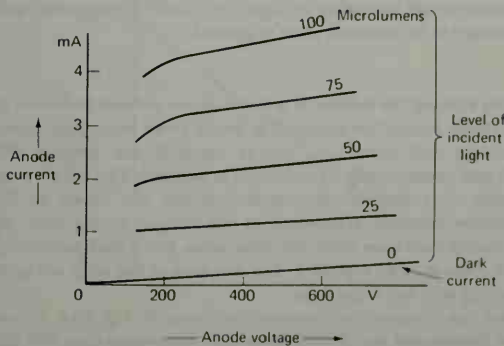
Figure 18-2. Typical characteristics of a photomultiplier tube.
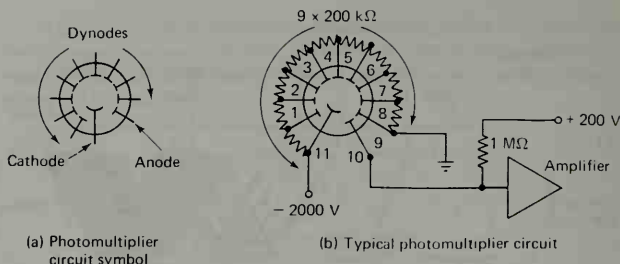
Figure 18-3. Photomultiplier circuit symbol and typical circuit.

illumination intensity the anode current of the photomultiplier tube should tend to remain constant as the anode voltage is increased. However, the dark current always adds to the anode current produced by illumination, and the secondary emission improves with increase in applied voltage; consequently, the anode current tends to increase slightly with increase in anode voltage.

Since the illumination levels indicated on the characteristics are measured in *microlumens*, it is seen that the photomultiplier tube is very sensitive indeed. In fact, the device is so sensitive that destructively large currents could flow if it is exposed to ordinary daylight levels when voltage is applied to its electrodes. Various spectral responses are available in photomultiplier tubes, ranging approximately from 150 to 600 nm, or from 400 to 1000 nm.

The symbol for a photomultiplier tube and a typical circuit arrangement are shown in Fig. 18-3. The cathode is provided with a high negative voltage, and the dynodes are biased via a potential divider arrangement between ground and the negative supply. The anode is connected via a high value of load resistance to a level more positive than ground. Although the device requires high operating voltages, the circuit arrangement enables the output voltage to be relatively close to ground.

**18-4
The
Photo-
conductive
Cell**

Light striking the surface of a material can provide sufficient energy to cause electrons within the material to break away from their atoms. Thus, free electrons and holes (i.e., charge carriers) are created within the material, and consequently its resistance is reduced. The circuit symbol and construction of a typical photoconductive cell are shown in Fig. 18-4. Light-sensitive material is arranged in the form of a long strip, zigzagged across a disc-shaped base with protective sides. For added protection, a glass or plastic cover may be included. The two ends of the strip are brought out to connecting pins below the base.

From the illumination characteristic shown in Fig. 18-5, it is seen that when not illuminated the cell resistance may be greater than 100 kΩ. This is known as the *dark resistance* of the cell. When illuminated, the cell resistance
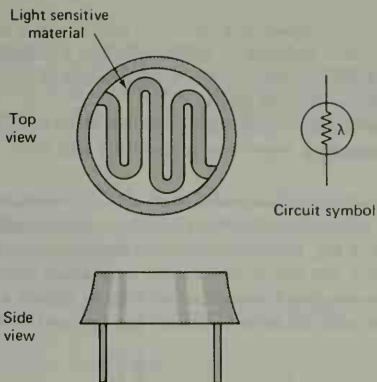
Figure 18-4. Construction and circuit symbol for photoconductive cell.

may fall to a few hundred ohms. Note that the scales on the illumination characteristic are logarithmic. The cell *sensitivity* may be expressed in terms of the cell current for a given voltage and given level of illumination.

The two materials normally employed in photoconductive cells are *cadmium sulfide* (CdS) and *cadmium selenide* (CdSe). Both materials respond rather slowly to changes in light intensity. For cadmium selenide the response time is around 10 ms, while cadmium sulfide may take as long as 100 ms. Another important difference between the two materials is their temperature sensitivity. There is a large change in the resistance of a cadmium selenide cell with changes in ambient temperature, but the cadmium sulfide resistance remains relatively stable. As with all other devices, care must be taken to ensure that the power dissipation is not
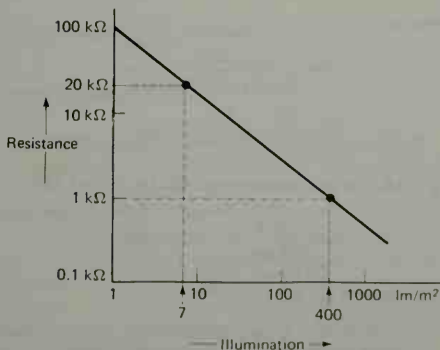
Figure 18-5. Illumination characteristic for photoconductive cell.

excessive. The *spectral response* of a cadmium sulfide cell is similar to that of the human eye; i.e., it responds to visible light. For a cadmium selenide cell, the spectral response is at the longer wavelength end of the visible spectrum and extends into the infrared region.

Two photoconductive cell applications are given in Examples 18-2 and 18-3. Other applications are shown in Figs. 18-8 and 18-9.

Example 18-2

A relay is to be controlled by a photoconductive cell with the characteristics shown in Fig. 18-5. The relay is to be supplied with 10 mA from a 30-V supply when the cell is illuminated with about 400 lm/m², and is required to be de-energized when the cell is dark. Sketch a suitable circuit and calculate the required series resistance and the level of the dark current.

solution

The circuit is shown in Fig. 18-6. A series resistor R_1 is included to limit the current.
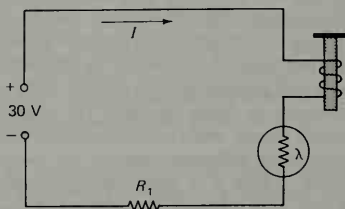
Figure 18-6. Relay control by photoconductive cell.

The current is

$$I = \frac{30 \text{ V}}{R_1 + (\text{cell resistance})}$$

or

$$R_1 = \frac{30}{I} - (\text{cell resistance})$$

From Fig. 18-5, the cell resistance at 400 lm/m² ≈ 1 kΩ:

$$R_1 = \frac{30 \text{ V}}{10 \text{ mA}} - 1 \text{ k}\Omega = 2 \text{ k}\Omega$$

and cell dark resistance ≈ 100 kΩ (from Fig. 18-5).

$$\text{Dark current} \approx \frac{30 \text{ V}}{2 \text{ k}\Omega + 100 \text{ k}\Omega} \approx 0.3 \text{ mA}$$

Example 18-3

An *npn* transistor is to be biased on when a photoconductive cell is dark, and off when it is illuminated. The supply voltage is ± 6 V, and the transistor base current is to be 200 μA when on. If the photoconductive cell has the characteristics shown in Fig. 18-5, design a suitable circuit.

solution

The circuit is as shown in Fig. 18-7. When dark the cell resistance is high, and the transistor base is biased above its grounded emitter. When illuminated, the base voltage is below ground level.
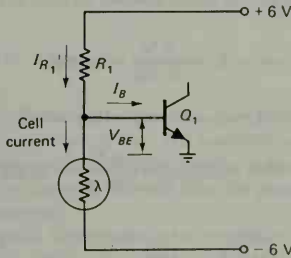
Figure 18-7. Circuit to switch transistor off when photoconductive cell is illuminated.

From Fig. 18-5, the cell dark resistance≈ 100 kΩ.
When the transistor is on,

$$\text{Cell voltage} = 6 \text{ V} + V_{BE} = 6.7 \text{ V} \quad \text{(for a silicon transistor)}$$

$$\text{Cell current} = \frac{6.7 \text{ V}}{100 \text{ k}\Omega} = 67 \text{ } \mu\text{A}$$

The current through R_1 is

$$\text{Cell current} + I_B = 67 \text{ } \mu\text{A} + 200 \text{ } \mu\text{A} = 267 \text{ } \mu\text{A}$$

The voltage across $R_1 = 6$ V $- V_{BE} = 5.3$ V.

$$R_1 = \frac{5.3 \text{ V}}{267 \text{ } \mu\text{A}} \approx 20 \text{ k}\Omega$$

When the transistor is off, the transistor base is at or below zero volts.

$$V_{R_1} \approx 6 \text{ V}$$
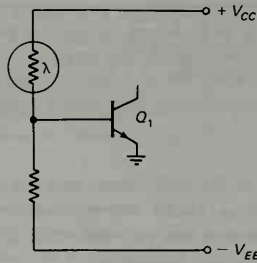
Figure 18-8. Circuit to switch transistor on when cell is illuminated.

and
$$I_{R_1} = \frac{6 \text{ V}}{20 \text{ k}\Omega} = 300 \text{ } \mu\text{A}$$

Since $I_B = 0$, cell current $= I_{R_1}$, and cell voltage ≈ 6 V.

$$\text{Cell resistance} = \frac{6 \text{ V}}{300 \text{ } \mu\text{A}} = 20 \text{ k}\Omega$$
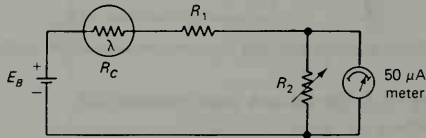
Figure 18-9. Light meter using photoconductive cell.

Therefore, Q_1 will be off when the cell resistance is 20 kΩ or less, i.e., when the illumination level is above approximately 7 lm/m^2 (see characteristics).

**18-5
The
Photodiode**

When a *pn*-junction is reverse biased, a reverse saturation current I_S flows due to thermally generated holes and electrons being swept across the junction as minority carriers. Increasing the junction temperature will generate more hole–electron pairs, and so the minority carrier (reverse) current will be increased. The same effect occurs if the junction is illuminated. Hole–electron pairs are generated by the incident light energy, and minority charge carriers are swept across the junction. Increasing the level of illumination increases the number of charge carriers generated and increases the level of reverse current flowing. Increasing the reverse voltage does not increase the reverse current significantly, because all available
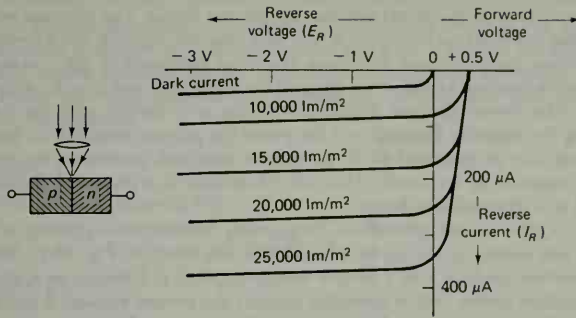
Figure 18-10. Illumination characteristics of photodiode.

charge carriers are already being swept across the junction. Even when the applied external bias is reduced to zero, the available minority carriers are swept across the junction by the junction barrier potential. To reduce the current to zero, it is necessary to forward bias the junction by an amount equal to the barrier potential.

Consider the typical illumination characteristics of a photodiode as shown in Fig. 18-10.

When dark, $I_R \approx 20$ μA at $E_R = 2$ V.

$$\text{Dark resistance} = \frac{E_R}{I_R} \approx \frac{2 \text{ V}}{20 \text{ μA}} = 100 \text{ k}\Omega$$

When illuminated with 25,000 lm/m^2,

$$I_R \approx 375 \text{ μA}$$

and
$$\text{Illuminated resistance} \approx \frac{2 \text{ V}}{375 \text{ μA}} = 5.3 \text{ k}\Omega$$

The resistance has changed by a factor of approximately 20, and it is seen that the photodiode can be employed as a *photoconductive device*.

When the reverse-bias voltage across a photodiode is removed, minority charge carriers will continue to be swept across the junction while the diode is illuminated. This has the effect of increasing the number of holes in the p-side and the number of electrons in the n-side. But the barrier potential is negative on the p-side and positive on the n-side, and was produced by holes flowing from p to n and electrons from n to p. Therefore, the minority carrier flow tends to reduce the barrier potential. When an external circuit is connected across the diode terminals, the minority carriers

will return to their original side via the external circuit. The electrons which crossed the junction from p to n will now flow out through the n-terminal and into the p-terminal. Similarly, the holes generated in the n-material cross the junction and flow out through the p-terminal and into the n-terminal. This means that the device is behaving as a battery with the n-side being the negative terminal and the p-side the positive terminal. In fact, a voltage can be measured at the photodiode terminal, positive on the p-side and negative on the n-side. Thus, the photodiode is a *photovoltaic* device as well as a *photoconductive* device.

Typical silicon photodiode illumination characteristics (plotted in the first and second quadrants for convenience) are shown in Fig. 18-11. When the device operates with a reverse voltage applied, it functions as a photoconductive device. When operating without the reverse voltage, it operates as a photovoltaic device. It is also possible to arrange for a photodiode to change from the photoconductive mode to the photovoltaic mode. The circuit symbol for the device is also shown in Fig. 18-11.

(a) Photodiode symbol

(b) Illumination characteristics
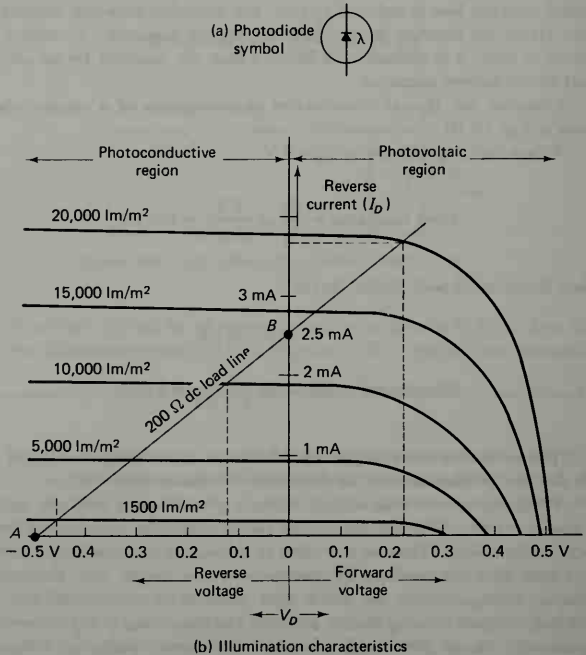
Figure 18-11. Symbol and typical illumination characteristic for silicon photodiode.

Example 18-4

A photodiode with the illumination characteristics shown in Fig. 18-11 is connected in series with a 200-Ω resistance and a 0.5 V supply. The supply polarity reverse biases the device. Draw the dc load line for the circuit and determine the diode currents and voltages at 1500, 10,000, and 20,000 lm/m^2 illumination.

solution

The circuit is as shown in Fig. 18-12.

$$E_S = I_D R_1 + V_D$$

When $I_D = 0$,

$$V_D = E_S = -0.5 \text{ V}$$

Plot point A on Fig. 18-11 at $I_D = 0$ and $V_D = -0.5$ V.
When $V_D = 0$, $V_{R_1} = E_S$.

$$I_D = \frac{V_{R_1}}{R_1} = \frac{-0.5 \text{ V}}{200 \text{ } \Omega} = 2.5 \text{ mA}$$
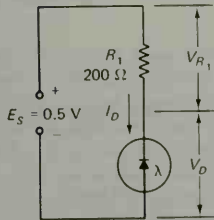
Figure 18-12. Photodiode with load resistance.

Plot point B at $I_D = -2.5$ mA and $V_D = 0$ V.
Draw the dc load line through points A and B.
From the load line,

$$\text{At } 1500 \text{ lm/m}^2, \quad I_D \approx -0.2 \text{ mA} \quad \text{and} \quad V_D \approx -0.45 \text{ V}$$
$$\text{At } 10,000 \text{ lm/m}^2, \quad I_D \approx -1.9 \text{ mA} \quad \text{and} \quad V_D \approx -0.12 \text{ V}$$
$$\text{At } 20,000 \text{ lm/m}^2, \quad I_D \approx -3.6 \text{ mA} \quad \text{and} \quad V_D \approx +0.22 \text{ V}$$

Note that the polarity of V_D changed from negative to positive at the highest level of illumination.

The *solar cell*, or *solar energy converter*, is simply a large photodiode designed to operate solely as a photovoltaic device and to give as much output power as possible. Low-current photodiodes are generally packaged in TO-type cans with an opening or a window on top. Devices for operation as *solar energy converters* require larger surface areas to provide maximum current capacity. The construction and cross section of a typical power solar cell for use as an energy converter are shown in Fig. 18-13. The surface layer of *p*-type material is extremely thin so that light can penetrate to the junction. The nickel-plated ring around the *p*-type material is the positive output terminal, and the plating at the bottom of the *n*-type is the negative output terminal. Power solar cells are also available in flat strip form for
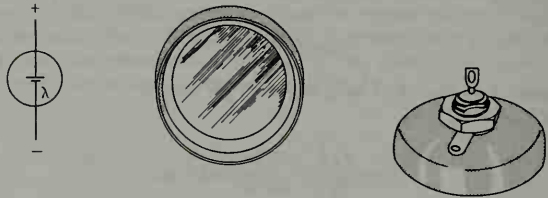
Symbol

(a) Symbol and Construction
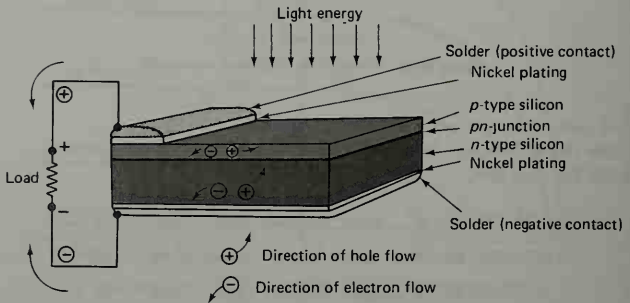
(b) Cross section

Figure 18-13. Symbol, construction, and cross section of a solar cell. (Courtesy of Solar Systems, Inc.)

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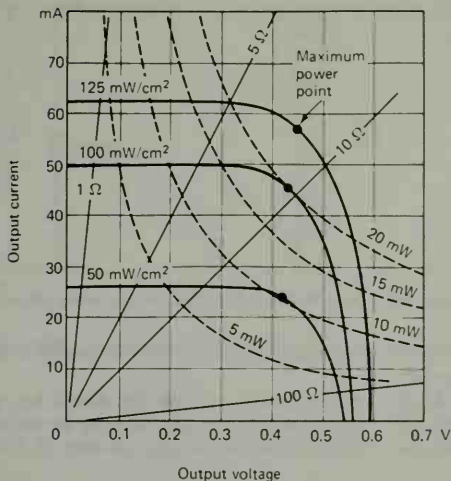
Figure 18-14. Typical output characteristics of power photocell for use as a solar energy converter. (Courtesy of Solar Systems, Inc.)

efficient coverage of available surface areas. The circuit symbol normally used for a photovoltaic device is also shown in Fig. 18-13.

Typical output characteristics of a power photocell are shown in Fig. 18-14. Consider the device characteristic when the incident illumination is 100 mW/cm². If the cell is short circuited, the output current is 50 mA. Since the cell voltage is zero, the output power is zero. If the cell is open circuited, the output current is zero. Therefore, the output power is again zero. For maximum output power the device must be operated on the knee of the characteristic. As in the case of all other devices, the output power must also be derated at high temperatures.

An earth satellite has 12-V batteries which supply a continuous current of 0.5 A. Solar cells with the characteristics shown in Fig. 18-14 are employed to keep the batteries charged. If the illumination from the sun for 12 hours in every 24 is 125 mW/cm², determine approximately the total number of cells required.

Example 18-5

solution

The circuit for the solar cell battery charger is shown in Fig. 18-15. The cells must be connected in series to provide the required output voltage, and
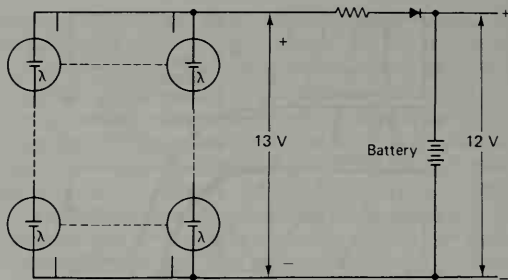
Figure 18-15. Array of solar cells connected as a battery charger.

groups of series-connected cells must be connected in parallel to produce the necessary current.

For maximum output power, each device should be operated at approximately 0.45 V and 57 mA (Fig. 18-14). Allowing for the voltage drop across the rectifier, a maximum output of approximately 13 V is required.

$$\text{Number of series-connected cells} = \frac{\text{output voltage}}{\text{cell voltage}} = \frac{13 \text{ V}}{0.45 \text{ V}} \approx 29$$

The charge taken from the batteries over a 24-hour period is 24 hours × 0.5 A or 12 ampere-hours.

Therefore, the charge delivered by solar cells must be 12 ampere-hours.

The solar cells deliver current only while they are illuminated, i.e., for 12 hours in every 24. Thus, the necessary charging current from the solar cells is 12 ampere-hours/12 hours, or 1 A.

$$\text{Total number of groups of cells in parallel} = \frac{\text{output current}}{\text{cell current}}$$

$$= \frac{1 \text{ A}}{57 \text{ mA}} \approx 18$$

The total number of cells required is (number in parallel) × (number in series) = 18 × 29 = 522

18-7
The Photo-transistor and Photo-darlington

A phototransistor is similar to an ordinary bipolar transistor, except that no base terminal is provided. Instead of a base current, the input to the transistor is provided in the form of light. Consider an ordinary transistor with its base terminal open circuited (Fig. 18-16). The collector–base leakage current (I_{CBO}) will act as a base current.
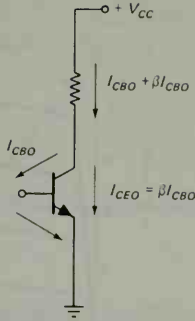
Figure 18-16. Currents in a transistor with its base open circuited.

Since

$$I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO} \qquad (4\text{-}6)$$

and

$$I_B = 0$$
$$I_C = (\beta_{dc} + 1) I_{CBO}$$

In this case, $I_C = I_{CEO}$, the collector–emitter leakage current with the base open circuited.

In the case of the photodiode, it was shown that the reverse saturation current was increased by the light energy incident on the junction. Similarly, in the phototransistor I_{CBO} increases when the collector–base junction is illuminated. When I_{CBO} is increased, the collector current $[(\beta_{dc} + 1) I_{CBO}]$ is also increased. Therefore, for a given amount of illumination on a very small area, the phototransistor provides a much larger output current than that available from a photodiode; i.e., the phototransistor is the more sensitive of the two.

The circuit symbol and typical output characteristics of the phototransistor are shown in Fig. 18-17. Some phototransistors have no base terminal and rely upon the incident illumination to generate a base current. Others have a base connection provided so that an external bias circuit may be connected. The device is usually packaged in a metal can with a lens on top. Clear plastic encapsulated phototransistors are also available.

Arrays of phototransistors and photodiodes are widely applied as *photodetectors* for such applications as punched card and tape *read out*. The phototransistors have the advantage of greater sensitivity than photodiodes. For a given level of illumination a greater output current is produced by a phototransistor than by a photodiode. However, photodiodes are the faster of the two, switching in less than nanoseconds, compared to typical phototransistor switching times of microseconds.
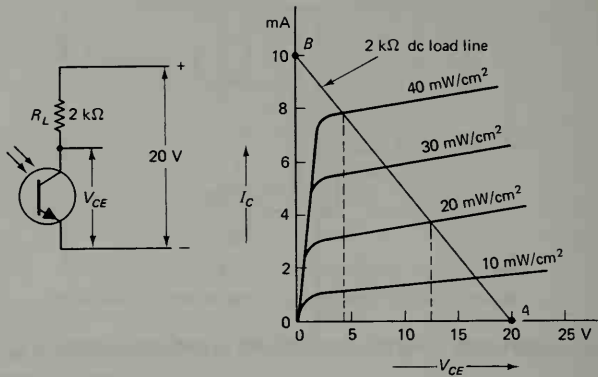
Figure 18-17. Phototransistor circuit and dc load line.

Example 18-6

A phototransistor having the characteristics shown in Fig. 18-17 has a supply of 20 V and a collector load resistance of 2 kΩ. Determine the output voltage when the illumination level is (a) zero, (b) 20 mW/cm², and (c) 40 mW/cm².

solution

The load line is drawn in the usual way.
When $I_C = 0$, $V_{CE} = V_{CC}$.
Plot point A at $I_C = 0$, $V_{CE} = 20$ V.
When $V_{CE} = 0$, $I_C = V_{CC}/R_L = 20$ V/2 kΩ = 10 mA.
Plot point B at $V_{CE} = 0$, $I_C = 10$ mA.
Draw the dc load line through points A and B.

From the intersections of the load line and the characteristics,

At illumination level = 0,   output voltage ≈ V_{CE} = 20 V

At illumination level = 20 mW/cm²,   output ≈ 12.5 V

At illumination level = 40 mW/cm²,   output ≈ 4 V

The *photodarlington* (Fig. 18-18) consists of a phototransistor connected in Darlington arrangement (see Chapter 9) with another transistor. The device is capable of much higher output currents than a phototransistor, and so it has a greater sensitivity to illumination levels than either a phototransistor or a photodiode. With the additional transistor involved, the photodarlington has a considerably longer switching time than a phototransistor.
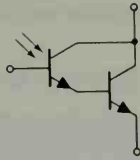
Figure 18-18. The photodarlington.

If a junction field effect transistor has light focused on its gate–channel junction, the light will act as a signal and produce a change in the drain current. Consider the n-channel junction FET and the photoFET in Fig. 18-19. The gate–source leakage current (I_{GSS}) is the *reverse saturation current* at a reverse-biased pn-junction and is temperature dependent. As in the case of the phototransistor, the junction reverse saturation current is also susceptible to light. Illumination on the junction causes more charge carriers to be generated and hence causes I_{GSS} to increase. I_{GSS} flows through bias resistance R_G and causes a voltage drop across R_G with the polarity shown. Thus, if $-V_G$ were just sufficient to bias the device off when dark, then when the junction is sufficiently illuminated the I_{GSS} increase would cause the gate voltage to increase and bias the FET on. A gate bias voltage that partially biases the device on might also be employed, so that increasing and decreasing the light level causes the I_D to increase and decrease. In a photoFET, the light-controlled I_{GSS} is referred to as the *gate current* (λI_g). I_{GSS} then becomes the *dark gate leakage current*. The light-controlled drain current is designated λI_d.

18-8
The
PhotoFET
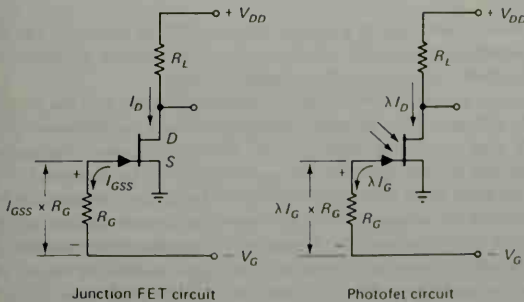
Figure 18-19. Junction FET and photoFET circuits showing effect of leakage currents.

The gate–source voltage changes are proportional to the gate current and the gate bias resistance.

$$\Delta V_{GS} = \lambda I_g \times R_G$$

and

$$\lambda I_d = g_m \times \Delta V_{GS}$$
$$= g_m \lambda I_g R_G$$

The selected value of R_G determines the sensitivity of the photoFET. For $\lambda I_g = 10$ nA, $g_m = 8$ mA/V and $R_G = 1$ MΩ,

$$\lambda I_d = 8 \text{ mA/V} \times 10 \text{ nA} \times 1 \text{ MΩ}$$
$$= 80 \ \mu\text{A}$$

If R_G is increased to 10 MΩ, λI_d becomes 800 μA.

Typical photoFET currents are

$$I_{GSS} = 0.5 \text{ nA}$$
$$\lambda I_g = 50 \text{ nA}/\mu\text{W/cm}^2$$
$$\lambda I_d = 500 \ \mu\text{A}/\mu\text{W/cm}^2$$

18-9
Light-
Emitting
Diodes

Charge carrier recombination takes place at a *pn*-junction as electrons cross from the *n*-side and recombine with holes on the *p*-side. Free electrons are in the conduction band of energy levels while holes are in the valence band. Therefore, electrons are at a higher energy level than holes, and some of this energy is given up in the forms of heat and light when recombination takes place. If the semiconductor material is translucent, the light will be emitted and the junction becomes a light source, i.e., a *light-emitting* diode (LED).

A cross section view of a typical diffused LED is shown in Fig. 18-20. The semiconductor material employed is *gallium arsenide* (GaAs), *gallium arsenide phosphide* (GaAsP), or *gallium phosphide* (GaP).

A *n*-type epitaxial layer is grown upon a substrate, and the *p*-region is created by diffusion. Charge carrier recombinations occur in the *p*-region, so it must be kept uppermost. The *p*-region, therefore, becomes the surface of the device, and the metal film anode connection must be patterned to allow most of the light to be emitted. This is done by making connection to the outside edges of the *p*-type layer, or by depositing a comb–shaped pattern at the center of the *p*-type surface. A gold film is applied to the bottom of the substrate to reflect as much as possible of the light toward the surface of the device and to provide a cathode connection. LED's made from GaAs emit infrared radiation (i.e., it is invisible). GaAsP material provides either red light or yellow light while red or green emission can be produced by using GaP.

http://keralatechnologicaluniversity.blogspot.com
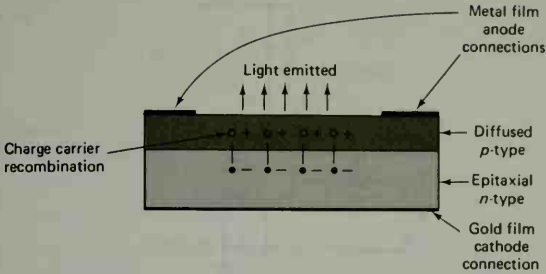
Figure 18-20. Cross section of light-emitting diode.

Figure 18-21 shows the LED circuit symbol (the arrow directions indicate emitted light) and the arrangement of a typical seven-segment LED numerical display. Any desired numeral from 0 to 9 can be displayed by passing current through the appropriate segments. The actual LED device is very small, so to enlarge the lighted surface solid plastic *light pipes* are often employed, as illustrated in Fig. 18-21(c).

(a) Circuit system   (b) Seven-segment arrangement

(c) Construction of seven-segment
LED display
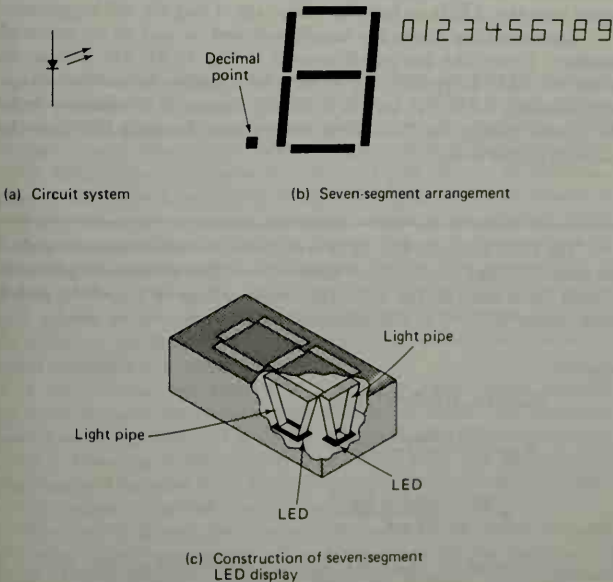
Figure 18-21. Light-emitting diode and seven-segment display.
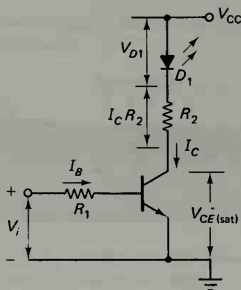
Figure 18-22. LED and transistor switch.

The forward voltage for a LED is typically 1.2 V, and for forward current 20 mA is typical. The relatively large amounts of current consumed by LED's are their major disadvantage. Excluding displays, all the circuitry of an electronic counter might require a total operating current of less than 100 mA. Four seven-segment LED displays could add 500 mA to this requirement, necessitating the inclusion of a much bulkier power supply. Apart from this, LED's do have the advantage of long life and ruggedness.

Light-emitting diodes are usually switched on and off by means of a transistor circuit like the one illustrated in Fig. 18-22. The voltage drop across the LED is typically 1.2 V, and the transistor saturation voltage is approximately 0.2 V (i.e., for low I_C levels). Resistor R_2 is necessary to limit the current through the LED to the desired level. Example 18-7 shows how to design such a circuit.

Example 18-7

The LED shown in Fig. 18-22 is to have a current of approximately 10 mA passed through it when the transistor is on. The transistor employed is a 2N3904 (data sheet in Fig. 8-1). The supply voltage is $V_{CC} = 9$ V, and the input voltage is $V_i = 7$ V. Calculate the required values of R_1 and R_2.

solution

$$V_{CC} = V_{D1} + I_C R_2 + V_{CE(\text{sat})}$$

$$R_2 = \frac{V_{CC} - V_{D1} - V_{CE(\text{sat})}}{I_C}$$

$$= \frac{9 \text{ V} - 1.2 \text{ V} - 0.2 \text{ V}}{10 \text{ mA}}$$

$$= 760 \ \Omega \quad (\text{use } 680\text{-}\Omega \text{ standard value; see Appendix 1})$$

I_C becomes

401
Liquid-
Crystal
Displays
(LCD)

$$\frac{9 \text{ V} - 1.2 \text{ V} - 0.2 \text{ V}}{680 \ \Omega} = 11.2 \text{ mA}$$

$I_B = I_C / h_{FE(min)}$.
From Fig. 8-1, $h_{FE(min)} = 100$ when $I_C \approx 10$ mA.

$$I_B = \frac{11.2 \text{ mA}}{100} = 112 \ \mu\text{A}$$

$$V_i = I_B R_1 + V_{BE}$$

$$R_1 = \frac{V_i - V_{BE}}{I_B} = \frac{7 \text{ V} - 0.7 \text{ V}}{112 \ \mu\text{A}}$$

$$\approx 56 \text{ k}\Omega \quad \text{(standard value)}$$

18-10
Liquid-
Crystal
Displays
(LCD)

18-10.1
*Dynamic
Scattering
LCD*

The molecules in ordinary liquids normally have random orientations. In liquid crystals the molecules are oriented in a definite crystal pattern. When an electric field is applied to the liquid crystal, the molecules, which are approximately cigar shaped, tend to align themselves perpendicular to the field. Charge carriers flowing through the liquid disrupt the molecular alignment and cause a turbulence within the liquid. This is illustrated in Fig. 18-23. When not activated, the liquid crystal is transparent. When activated, the molecular turbulence causes the light to be scattered in all directions so that the activated areas appear bright. This phenomenon is known as *dynamic scattering*. The actual liquid-crystal material may be one of several organic compounds which exhibit the optical properties of a solid while retaining the fluidity of a liquid. Examples of such compunds are *cholesteryl nonanoate* and *p-azoxyanisole*.

A liquid-crystal cell consists of a layer of liquid-crystal material sandwiched between glass sheets with transparent metal film electrodes deposited on the inside faces (Fig. 18-24). With both glass sheets transparent, the cell is known as a *transmittive-type cell*. When only one glass sheet is transparent and the other has a reflective coating, the cell is termed *reflective type*. The application of both types is illustrated in Fig. 18-25.

When not activated, the transmittive-type cell will simply transmit rear or edge lighting through the cell in straight lines. In this condition the cell will not appear bright. When activated, the incident light is diffusely

(a) Molecules in liquid crystal when no current flowing

(b) Charge carrier flow through liquid crystal disturbs molecular alignment and causes turbulence
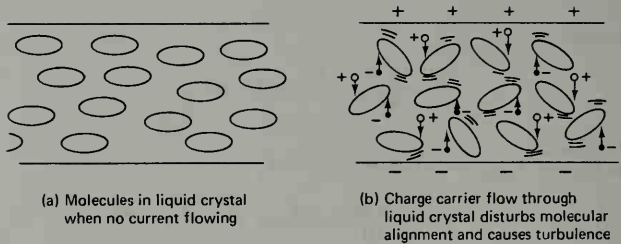
Figure 18-23. Molecules in a liquid crystal and effect of charge carrier flow.
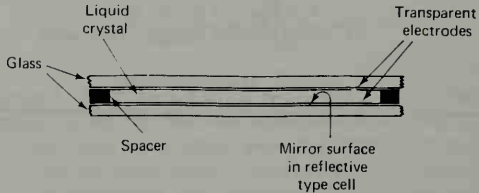
Figure 18-24. Construction of liquid-crystal cell.

scattered forward, as shown in Fig. 18-25(a), and the cell appears quite bright even under high-intensity ambient light conditions. The reflective-type cell operates from light incident on its front surface. When not activated, light is reflected in the usual way from the mirror surface, and the cell does not appear bright. When activated the dynamic scattering phenomenon occurs, and the cell appears quite bright [Fig. 18-25(b)].

18-10.2
Field
Effect
LCD

The field effect LCD is constructed similarly to the dynamic scattering type (Fig. 18-24), with the exception that two thin polarizing optical filters are placed at the surface of each glass sheet. The liquid-crystal material employed is known as *twisted nematic* type, and it actually twists the light passing through when the cell is not energized. This twisting allows the light to pass through the polarizing filters. Thus, in the case of a transmittive-type cell, Fig. 18-25(a), the unenergized cell can appear dark against a bright background. When energized, the cell becomes transparent and *disappears* into the background.

18-10.3
Electrical
Characteristics

Since liquid-crystal cells are light reflectors or transmitters rather than light generators, they consume very small amounts of energy. The only energy required by the cell is that needed to activate the liquid crystal. The total current flow through four small seven-segment displays is typically about 25 μA for dynamic scattering cells and 300 μA for field effect cells. However, the LCD requires an ac voltage supply, either in the form of a sine

(a) Transmittive type

(b) Reflective type
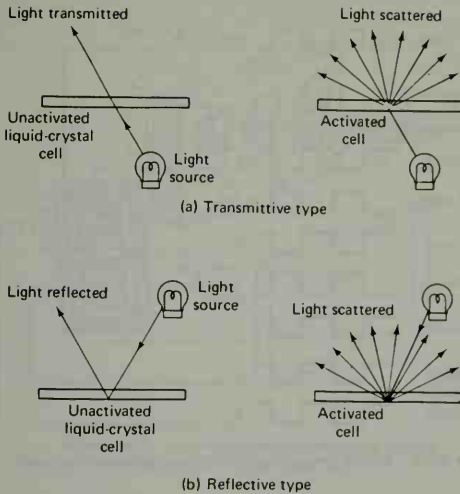
Figure 18-25. Operation of liquid-crystal cells.

wave or a square wave. This is because a continuous direct current flow produces a plating of the cell electrodes, which could damage the device. Repeatedly reversing the current avoids this problem.

A typical supply for a dynamic scattering LCD is a 30 V peak-to-peak square wave with a frequency of 60 Hz. A field effect cell typically uses 8 V peak-to-peak. Figure 18-26 illustrates the square wave drive method for liquid-crystal cells. The *back plane*, which is one terminal common to all cells, is supplied with a square wave. A similar square wave is applied to each of the other terminals. These square waves are either in phase or in antiphase with the back plane square wave. Those cells with waveforms in phase with the back plane waveform (cell e and f in Figure 18-26) have no voltage developed across them (both terminals of the segment are at the same potential); therefore, they are *off*. The cells with square waves in antiphase with the back plane input have an ac voltage developed across them (e.g., positive square waves with 15 V peak effectively produce 30 V peak-to-peak when in antiphase). Therefore, the cells which have square wave inputs in antiphase with the back plane input are energized and appear bright.

Unlike LED displays, which are usually quite small, liquid-crystal displays can be fabricated in almost any convenient size. The maximum power consumed for a typical LCD used in electronics equipment is around 20 μW per segment, or 140 μW per numeral when all seven segments are energized. Comparing this to about 400 mW per numeral for a LED display (including series resistors), the major advantage of liquid-crystal devices is
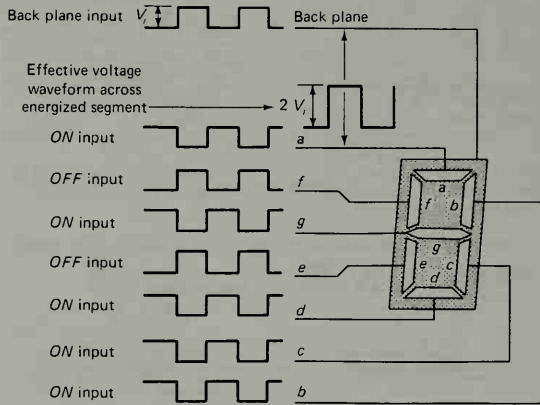
Figure 18-26. Square wave drive method for liquid-crystal display.

obvious. Perhaps the major disadvantage of the LCD is its decay time of 150 ms (or more). This is very slow compared to the rise and fall times of LED's. In fact, the human eye can sometimes observe the fading out of LCD segments switching off. At low temperatures the response time is considerably increased.

18-11
Gas-
Discharge
Displays

The type of seven-segment gas-discharge display illustrated in Fig. 18-27 is widely applied today in electronic calculators. It is actually a gas-filled tube. Separate cathodes in seven-segment format are provided on the base of the device, and the anode (for each seven-segment group) is a transparent metal film deposited on the covering faceplate. Gas is contained in the narrow space between the faceplate and the base.

When a high voltage is provided between the anode (positive polarity here) and one or more of the cathodes, the gas is ionized and causes a glow around each cathode. Thus, any desired numerals can be displayed depending upon the cathodes selected. Neon gas is usually employed, and this gives a red-orange glow; however, other colors are available with different gases.

The supply voltage required for gas-discharge displays is on the order of 140 to 200 V. This is the most serious disadvantage of the device when used with transistor circuits. Offsetting this is the fact that relatively bright displays are possible with current levels of only 200 μA. A 50-μA current
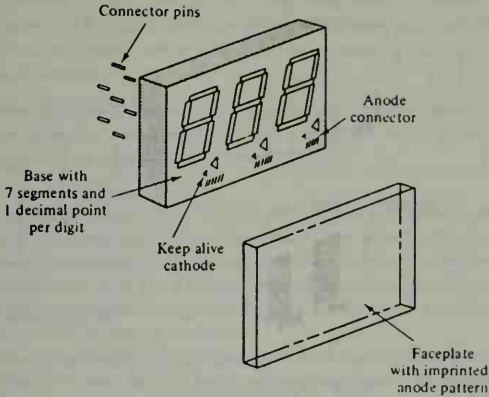
Figure 18-27. Seven-segment gas-discharge display.
(Courtesy of Beckman Instruments, Inc.)

(normally not enough to produce a glow) is usually maintained through the
keep alive cathode (see Fig. 18-27) to ensure that the device switches on rapidly.

An *optoelectronic coupler* (or *optically coupled isolator*) is basically a photo-transistor and a light-emitting diode combined in one package. Figure 18-28 shows the typical circuit and terminal arrangement for one such device contained in a dual-in-line plastic package.

18-12
Opto-
electronic
Couplers

When current flows in the diode, the emitted light is directed to the phototransistor and causes current flow in the transistor. The coupler may be operated as a *switch*, in which case both the LED and phototransistor are normally off. A pulse of current through the LED causes the transistor to be switched on for the duration of the pulse. Since the coupling is optical, there is a high degree of electrical isolation between input and output terminals.

Three additional types of optical couplers are illustrated in Fig. 18-29. They are (a) Darlington output type, (b) SCR output, and (c) TRIAC
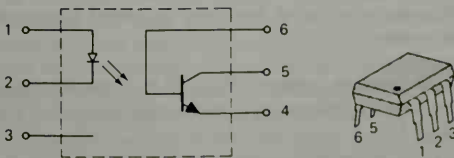
Figure 18-28. Optoelectronic coupler with transistor output.

(a) Darlington output

(b) SCR output

(c) Triac output
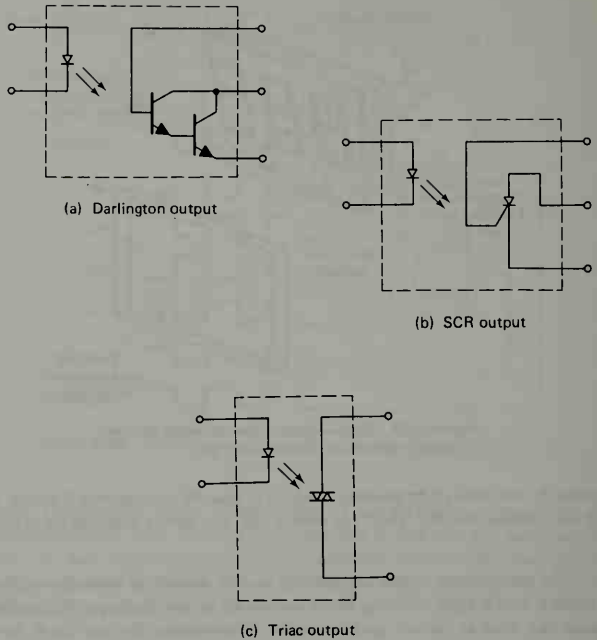
Figure 18-29. Three types of optoelectronic coupler.

output. In (a) the photodarlington output stage provides much higher output current (i.e., for a given LED current) than is possible with a phototransistor output stage. The output stages in (b) and (c) are a light-activated SCR and a light-activated TRIAC, respectively. They are applied in the kind of control circuits discussed in Chapter 16, where an additional requirement is high electrical isolation between triggering current and control device.

The following is a list of the most important parameters for an optoelectronic coupler:

Input to output isolation voltage (V_{iso}). This is the maximum voltage difference that can exist between input and output terminals. Typical values range up to 7500 V.

Current transfer ratio (CTR). The ratio of output (photo transistor) current to input (LED) current, expressed as a percentage. For a phototransistor

output stage CTR values can be anything from 10% to 150%. For a photodarlington, CTR might easily be 500%. CTR does not apply to SCR and TRIAC output stages; instead, the required triggering current (through the LED) is of interest.

Response time. Divided into *rise time* (t_r) and *fall time* (t_f). For phototransistor output stages t_r and t_f are usually around 2 to 5 μs. With a Darlington output, t_r may be 1 μs or less while t_f could be 17 μs.

Laser is the shortened form of *light amplification by stimulated emission of radiation*. A laser emits radiation of essentially one wavelength (or a very narrow band of wavelengths). This means that the light has a single color (is monochromatic); i.e., it is not a combination of several colors. Laser light is referred to as *coherent light* as opposed to light made up of a wide band of wavelengths, which is termed *incoherent*.

The unique property of light generated by a laser is that the emission is in the form of a very narrow beam without significant divergence. The beam of light contains sufficient energy to weld metals or to destroy cancerous growths. It can also be applied to precise measurements, to guidance of industrial machinery, and to optical fiber communication techniques.

Consider the light-emitting diode. The source of light is the energy emitted by electrons which recombine with holes (at a lower energy level). In the case of an LED, the light is incoherent; i.e., it is made up of a wide spectrum of wavelengths.

In a laser the atoms are struck by *photons* (or packets of energy) which are exactly similar to the photons of energy emitted when recombination occurs. This triggers the energy emission and results in two identical photons for each recombination: the incident photon and the emitted photon. The photons produce further emission of similar photons, which in turn creates more similar photons. The result is an emission of energy in the form of a beam of coherent light.

The operating principle of the laser diode is illustrated in Fig. 18-30. A *pn* junction of gallium arsenide (GaAs), or GaAs combined with other materials, is manufactured with a precisely defined length (L) [Fig. 18-30 (a)]. The junction length is related to the wavelength of the light to be emitted. The ends of the junction are each polished to a mirror surface and may have an additional reflective coating. The purpose of this is to reflect internally generated light back into the junction. One end is only partially reflective so that light can pass through when lasing occurs.

Consider the effect of charge carrier *injection* into the depletion region when the junction is forward biased [Fig. 18-30(b)]. As the forward current increases, a growing number of charge carriers enter the depletion region and excite the atoms that they strike. The atoms at first emit photons of energy randomly, as electrons are raised to a high energy level and then fall back to a lower level. Sooner or later several photons strike the reflective
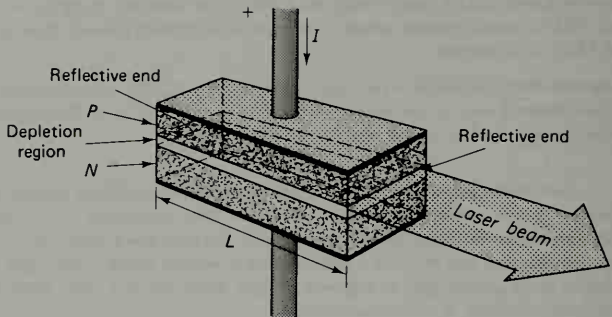
(a) Basic construction of laser diode.
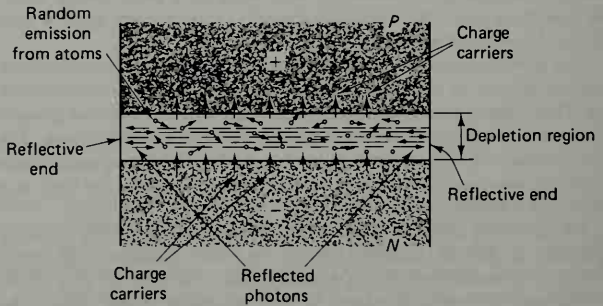
(b) Random emission and laser action within
depletion region.

Figure 18-30. Laser diode construction and operation.

ends of the junction perpendicularly so that they are reflected back along their original (incident) path. These reflected photons are then reflected back again from the other end of the junction. The reflection back and forward continues thousands of times, and the photons increase in number as they cause other similar photons to be emitted from atoms. This activity of reflection and generation of increasing numbers of photons amounts to amplification of the initial reflected photons of light. The beam of laser light emerges through the partially reflective end of the junction.

GaAs laser diodes normally require high forward current levels, anything from about 100 mA up to tens of amperes. At low current levels the device emits light like a LED. Beyond a *threshold current* level the light intensity increases sharply, and its bandwidth decreases as lasing commences. Because of the high-energy density a laser beam can be quite dangerous. *Eye protection must be worn when working with these devices.*

Laser diodes which operate in a pulsed manner are termed *injection laser diodes*. Those which produce a continuous output are referred to as *continuous wave* or *CW laser diodes*. Each type has a threshold input current level, and each emits a particular light wavelength dependent upon the material and dimensions of the junction.

Optoelectronic device. Electronic device which emits light, is operated by light, or modifies light.

Glossary of Important Terms

Photoemissive device. Device in which incident radiation causes electrons to be emitted from a photocathode.

Photoconductive device. Device which changes its resistance when illuminated.

Photovoltaic device. Device which generates a voltage when illuminated.

Spectral response. Plot of device response to illumination versus illumination frequency.

Threshold frequency. Minimum frequency of incident radiation that will produce a photoelectric effect in a given device.

Threshold wavelength. 1/(threshold frequency)—maximum wavelength of incident radiation that will produce a photoelectric effect in a given device.

Lumen. Unit of luminous flux.

Microlumen. 10^{-6} lumens.

Lumen per square meter ($1m/m^2$). Unit of luminous flux density.

Milliwatts/square centimeter (mW/cm^2). Unit of luminous flux density.

Photomultiplier. Electron tube in which incident radiation produces electron emission which is multiplied by secondary emission to produce usable current levels.

Photocathode. Electrode with surface that emits electrons when illuminated.

Dark current. Current which flows in photoelectric device when not illuminated.

Illumination characteristic. Graph showing change of resistance, voltage, and/or current with illumination change.

Cadmium sulfide. Material used in the manufacture of photoconductive device—rise time ≈ 100 ms—spectral response similar to human eye.

Cadmium selenide. Material used in the manufacture of photoconductive device—rise time ≈ 10 ms—spectral response extends into infrared region.

Photodiode. Diode in which the reverse saturation current level changes when the junction is illuminated—photoconductive–photovoltaic device.

Solar cell. Photovoltaic cell—generates a voltage when illuminated.

Phototransistor. Transistor in which I_C changes when the collector–base junction is illuminated.

Photodetector. Phototransistor or photodiode employed to detect presence of light.

Photodarlington. Phototransistor connected in Darlington arrangement with another transistor.

PhotoFET. Junction field effect transistor in which I_D changes when gate–channel junction is illuminated.

Light-emitting diode (LED). Diode in which charge carrier recombination produces light emission.

Liquid-crystal cell. Electronic display device in which liquid-crystal material can be made to appear bright or dark.

Seven-segment display. Arrangement of seven LED's, LCD's, or other light-emitting devices to display numerals from 0 to 9.

Gas-discharge display. Gas-filled tube in which ionized gas displays numerals.

Optoelectronic coupler. Combination of light-emitting diode and phototransistor, photodarlington, light-activated SCR or TRIAC.

Laser. Light amplification by stimulated emission of radiation.

Review Questions

18-1. Using illustrations, explain the operation of a photomultiplier tube. Also sketch typical characteristics for a photomultiplier tube and briefly explain.

18-2. Draw a sketch of a typical photomultiplier circuit. Briefly explain.

18-3. Sketch the symbol, typical construction, and characteristics for a photoconductive cell. Discuss the principle of this type of photocell, and compare the kinds of material usually employed.

18-4. Sketch typical illumination characteristics for a photodiode, and explain the theory of the device.

18-5. Draw circuit diagrams to show how a photoconductive cell may be employed for
   (a) Biasing a *pnp* transistor off when the cell is illuminated.
   (b) Biasing an *npn* transistor on when illuminated.
   (c) Measuring light level.
   (d) Energizing a relay when illuminated.

18-6. Sketch the cross section of a typical solar cell, and briefly explain how it operates.

18-7. Sketch the circuit diagram for an array of solar cells employed as a battery charger. Briefly explain.

18-8. Sketch the circuit symbol and characteristics for a phototransistor. Explain how it operates. Discuss the application of phototransistors, photodarlingtons, and photodiodes as photodetectors.

18-9. Sketch a circuit diagram to show the operation of a photoFET circuit. Briefly explain the principle of the device.

18-10. Using illustrations, explain the construction and operation of light-emitting diodes. Show the circuit symbol for a light-emitting diode, and show how an LED numerical display is arranged. Also discuss the current levels required by LED numerical displays.

18-11. Using illustrations, explain the theory of the liquid-crystal cell. Show how a liquid-crystal cell is constructed, and explain the difference between dynamic scattering and field effect LCD's and between reflective- and transmittive-type cells. Also compare liquid-crystal cells and light-emitting diodes.

18-12. Sketch a seven-segment LCD and show the waveforms involved in controlling the cells. Explain.

18-13. Draw a sketch to show the construction of a seven-segment gas-discharge display. Explain how the device operates and discuss its advantages and disadvantages.

18-14. Using diagrams, explain the various types of optoelectronic couplers. Discuss the most important parameters and the applications of optoelectronic couplers.

18-15. Draw sketches to show the basic construction and operation of a laser diode. Explain how the device operates and compare its performance to that of an LED.

Problems

18-1. A photoconductive cell 2 cm in diameter is to receive 400 1m/m of light energy from a lamp 7 meters distant from the cell. If the lamp emits energy evenly in all directions, determine the required light energy output from the lamp. Also calculate the total luminous flux striking the photocell.

18-2. The total luminous flux striking a surface of a solar cell is measured as 12.5 mW. The light source is 4.5 meters from the solar cell.

Calculate the light energy output from the source if it emits light evenly in all directions. The surface area of the solar cell is 6 cm^2.

18-3. A *pnp* transistor is to be biased on when the level of illumination on a photoconductive cell is greater than 100 lm/m^2 and off when dark. The supply voltage available is ± 5 V, and the transistor collector current is to be 10 mA when on. If the transistor has a h_{FE} of 50 and the photoconductive cell has the characteristics shown in Fig. 18-5, design a suitable circuit.

18-4. The light meter in Fig. 18-9 has the following components: $E_B = 1.5$ V, $R_1 = 13.8$ kΩ, $R_2 = 390$ Ω, and meter resistance $R_m = 390$ Ω. The photoconductive cell has the characteristics in Fig. 18-5. Calculate the meter indication when the illumination level is (a) 400 lm/m^2; (b) 7 lm/m^2.

18-5. A photodiode is connected in series with a resistance and a reverse bias supply of 0.4 V. The diode has the illumination characteristics of Fig. 18-11 and is required to produce an output of $+0.2$ V when illuminated with 20,000 lm/m^2. Calculate the value of the series resistance required, and determine the device voltage and current at 5000 lm/m^2 of illumination.

18-6. A photodiode with the characteristics shown in Fig. 18-11 is connected in series with a 0.4-V supply and a 100-Ω resistance. Determine the resistance offered by the photodiode at 15,000 lm/m^2, 10,000 lm/m^2, and 5000 lm/m^2.

18-7. Two photodiodes are each connected in series with 100-Ω resistors and a 0.5 V supply. A voltmeter is connected to measure the difference in voltage drops across the two diodes. Assuming that each photodiode has the characteristics illustrated in Fig. 18-11, estimate the voltmeter reading when one diode has 10,000 lm/m^2 incident illumination and that on the other diode is 12,500 lm/m^2.

18-8. A rural telephone system uses 6-V rechargeable batteries which supply an average current of 50 mA. The batteries are recharged from an array of solar cells which each have the characteristics shown in Fig. 18-14. The average level of sunshine is 50 mW/cm^2 for 12 hours of each 24-hour period. Calculate the number of solar cells required, and determine how they should be connected.

18-9. The roof of a house has an area of 200 m^2 and is covered with solar cells which are each 2 cm $\times$ 2 cm. If the cells have the output characteristics shown in Fig. 18-14, determine how they should be connected to provide an output voltage of approximately 120 V. Take the average daytime level of illumination as 100 mW/cm^2. If the sun shines for an average of 12 hours in every 24, calculate the kilowatthours generated by the solar cells each day.

18-10. A phototransistor operating from a 25 V supply has the output characteristics shown in Fig. 18-18. If V_{CE} is to be 10 V when the

illumination level is 30 mW/cm², determine the value of load resistance that should be used.

18-11. A phototransistor with the characteristics shown in Fig. 18-17 is connected in series with a relay coil which has a resistance of 1 kΩ. The coil current is to be 8 mA when the illumination level is 40 mW/cm². Determine the required supply voltage level, and estimate the coil current when the illumination falls 10 mW/cm².

18-12. Two light-emitting diodes are connected in series. The current through the diodes is to be controlled by a 2N3903 transistor (see Fig. 8-1), and the supply voltage is $V_{CC} = 12$ V. The diode current is to be approximately 15 mA. Design a suitable circuit.

18-13. A light-emitting diode is to be used to indicate when a 25 V supply is switched on. The LED current is to be 20 mA. Sketch a suitable circuit and make all necessary calculations.

Miscellaneous Devices

19-1
Piezo-
electricity

If a mechanical pressure is applied to a quartz crystal, a voltage proportional to the pressure appears across the crystal. Conversely, when a voltage is applied across the crystal surfaces, the crystal is distorted by an amount proportional to the voltage. All crystals with this property are termed *piezoelectric*. An alternating voltage applied to a crystal causes it to vibrate at its natural resonance frequency. Since this frequency is a very stable quantity, piezoelectric crystals are used to stabilize the frequency of oscillators.

19-2
Piezoelectric
Crystals

19-2.1
*Theory of
Piezo-
electricity*

Consider the flat plan diagram of a piezoelectric crystal structure in Fig. 19–1(a). The broken lines join groups of ions. It is seen that each group consists of three positive ions at the corners of an equilateral triangle and

414
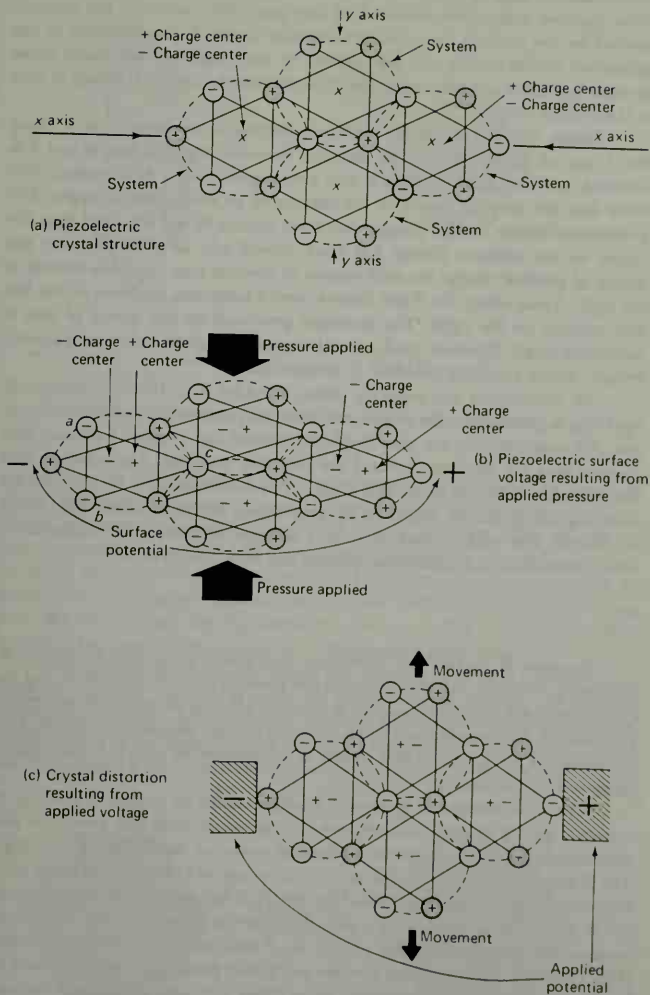
Figure 19-1. Flat plan diagrams of piezoelectric crystal, showing how voltage is generated by applied pressure, and how distortion is produced by applied voltage.

three negative ions at the corners of another triangle. The charge from the three positive ions is concentrated at the geometric center of the triangle formed by the positive ions, and the negative charge is concentrated at the geometric center of the triangle formed by the negative ions. Since these geometric centers are coincident the charges cancel, and each group of ions is electrically neutral.

Figure 19–1(b) shows the result of applying a mechanical force along the Y axis of the structure. The distance between negative ions a and b is reduced, and the distance from a and b to negative ion c is increased. The three ions are now no longer at the corners of an equilateral triangle. The geometrical center of the triangle has been moved to the left, and thus the center of the negative charge has been moved left. In a similar way the center of positive charge for each system of positive ions has been moved to the right. Thus, along the X axis there is now a potential, negative on the left and positive on the right. The potential produced by one group of ions is extremely small. However, each crystal consists of a great many such atomic groups, so the resultant potential is measurable.

To understand the converse effect, consider Fig. 19–1(c). Instead of applying a pressure at the Y axis, an electrical potential is applied at the X axis. All negative ions are now displaced toward the positive terminal, and positive ions are displaced toward the negative terminal. The result is that the crystal is distorted along the Y axis. The distortion may be reversed by reversing the potential. Applying an alternating potential causes the crystal to vibrate. For each crystal there is a natural frequency of resonance at which maximum continuous oscillations can be made to occur.

19-2.2
Manufacture
of Quartz
Crystals

Crystals of *Rochelle salt, tourmaline*, and *quartz* all possess piezoelectric properties. Rochelle salt demonstrates the greatest piezoelectric effect, but its applications are limited because it is strongly affected by moisture and heat. Tourmaline and quartz show approximately similar piezoelectric effects, but tourmaline is semiprecious and quartz is inexpensive, so quartz is universally employed in electronics.

The manufacture of electronic crystals begins by cutting a natural or cultured quartz crystal into sections. In its uncut state the crystal is approximately in the form of the hexagonal prism as shown in Fig. 19–2(a). The Z axis, passing through the ends of the prism, is known as the *optical axis*. No piezoelectric effect is produced by electrical or mechanical stresses along the Z axis. The X axes, which pass through the corners of the hexagonal cross section and are perpendicular to the Z axis, are termed the *electrical axes* [Fig. 19–2(b)]. The *mechanical axes* are the Y axes passing through the faces of the hexagonal prism. Mechanical stress along a Y axis produces a voltage along the perpendicular X axis.

A great variety of *crystal cuts* is possible and each has its own particular characteristics. Figure 19–3 shows an *X-cut* and a *Y-cut*. A mechanical stress
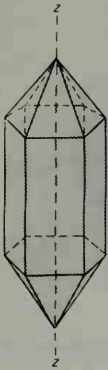
(a) Approximate shape
of natural crystal
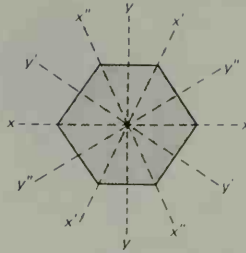
(b) Cross section

Figure 19-2. Approximate shape and cross section of natural quartz crystal.

applied to the edges of an X-cut crystal generates an electrical potential across the flat sides. Similarly, a mechanical stress on the flat sides of a Y-cut crystal generates an electrical potential across its edges. The change of crystal resonant frequency with temperature increase or decrease is termed the *crystal temperature coefficient*. Obviously, for greatest frequency stability of oscillations, the smallest possible temperature coefficient is desirable. Two cuts, the *GT cut* and the *ring-shaped cut*, shown in Fig. 19–4, are widely employed because they have near-zero temperature coefficients.

The sections cut from the crystal are referred to as *blanks*. Each blank must be carefully ground to accurate dimensions to achieve the desired resonance frequency. After grinding, silver or gold electrodes are plated onto opposite sides of the blank to form electrical connections. The crystal is then mounted inside a vacuum-sealed glass envelope or in a hermetically sealed

Section cut
from crystal

y cut

x cut
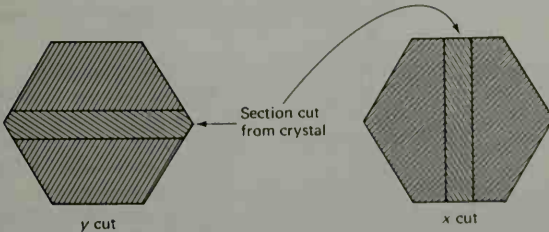
Figure 19-3. X-and Y-cut crystal sections.

(a) GT-cut   (b) Ring-shaped cut
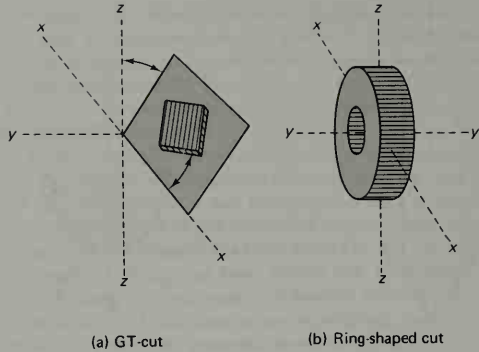
Figure 19-4. *GT*-cut and ring-shaped crystal cut give near-zero temperature coefficient.

metal can. Figure 19–5 shows a ring-shaped crystal mounted on a base and its can-type enclosure.

19-2.3
Crystal
Equivalent
Circuit and
Performance

The electrical equivalent circuit for a crystal is shown in Fig. 19–6(a). The crystal actually behaves as a series *LCR* circuit in parallel with C_m, the capacitance of the mounting electrodes. Because of the presence of C_m, the crystal has two resonance frequencies [Fig. 19–6(b)]. One of these is the *series*
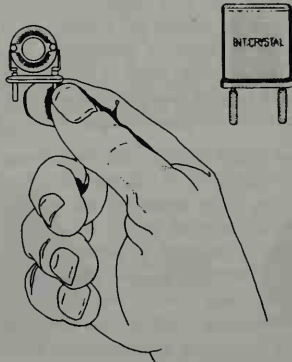
Figure 19-5. Ring-shaped crystal and hermetically sealed metal can. (Courtesy of International Crystal Mfg., Inc.)

(a) Equivalent circuit   (b) Resonance frequencies
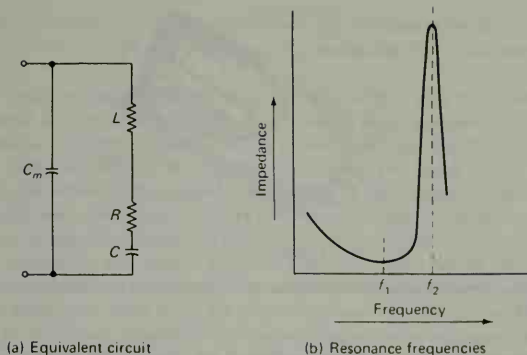
Figure 19-6. Crystal equivalent circuit and resonance frequencies.

resonance frequency (f_1) at which $2\pi fL = 1/(2\pi fC)$. In this case the crystal impedance is very low. The other resonance frequency (f_2) is slightly higher than f_1, and is due to parallel resonance of the capacitance C_m and the reactance of the series circuit. At f_2 the crystal impedance is very high.

When a circuit is operating at its resonance frequency, the capacitive and inductive reactances cancel each other out, and the power supplied to the circuit is dissipated in the resistance. If the resistance is large, the power dissipation can cause drift of the resonance frequency. A measure of the quality of a resonance circuit is the ratio of reactance to resistance. This is termed the *Q factor*. Since the resistive component of the crystal equivalent circuit tends to be very small, crystals have very large Q factors. Crystal Q factors range approximately from 10^4 to 10^6 compared to a maximum of about 400 for an ordinary electrical resonance circuit.

Most crystals will maintain frequency drift to within a few cycles at 25°C. For greater frequency stability, the crystal is often contained in an insulated enclosure termed a *crystal oven*. A typical crystal oven is shown in Fig. 19-7. The temperature is thermostatically controlled. Typical heater power is 4 W and heater voltage is 6 to 24 V.

To stabilize the frequency of an oscillator, a crystal may be operated at either its parallel or series resonance frequency. For very high frequency applications, crystals are often used to control oscillators operating at a multiple of the crystal resonance frequency. In this situation, the crystal is said to be operating in *overtone*.

Figure 19-8 shows an oscillator in which the crystal is operating in parallel resonance; note the circuit symbol for the crystal. Transistor Q_1 combined with R_1, R_2, RFC, and R_E constitutes a common base circuit. Capacitor C_1 provides an ac short circuit across R_2 to ensure that the

**19-2.4
Crystal
Oscillators**
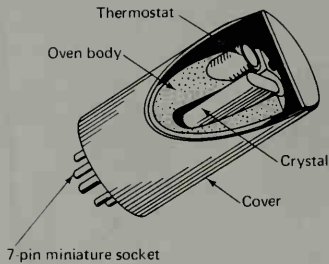
Figure 19-7. Temperature-controlled crystal oven. (Courtesy of Erie Technological Products, Inc.)

transistor base remains at a fixed voltage level. C_2 and C_3 form a capacitive voltage divider which returns a portion of the output voltage to the emitter of Q_1. As the output voltage increases positively, the emitter voltage also increases, and since the base voltage is fixed, the base-emitter voltage is reduced. The reduction in V_{BE} causes I_C to be reduced, and this in turn causes the collector voltage V_C to increase positively. Thus, the circuit is supplying its own input and a state of oscillation exists. The crystal in parallel with C_2 and C_3 permits maximum voltage feedback from collector to emitter when its impedance is very high, i.e., at its parallel resonance frequency. At other frequencies the crystal impedance is low, and the low impedance causes the feedback voltage to be too small to sustain oscillations. The oscillation frequency is stabilized at the parallel resonance frequency of the crystal.

The Colpitts oscillator in Fig. 10–4 is one circuit in which a crystal could be employed in its series resonance mode. The crystal should be
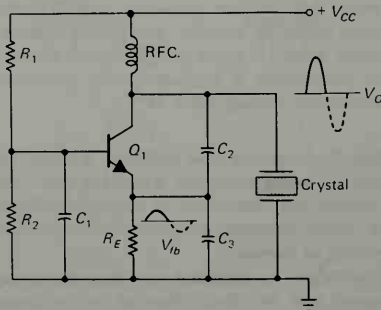
Figure 19-8. Crystal-controlled oscillator with crystal operating in parallel resonance.

substituted in place of coupling capacitor C_C. Maximum feedback occurs when the crystal impedance is a minimum, i.e., at the series resonance frequency.

Crystal oscillators must be designed to provide a load capacitance on the crystal as specified by the manufacturer. This is necessary to obtain oscillation at the specified frequency. It is also important that the power fed to the crystal be held to the specified maximum. Too much crystal power produces distortion in the oscillator waveform. It also causes overheating of the crystal and consequently renders the resonant frequency unstable. More important is that the thin-plated electrodes may be melted off an overdriven crystal, destroying the device. In older types of crystals where more solid plates were employed, the crystal was sometimes shattered by overdriving. Typical maximum drive levels for plated crystals range from 2 to 10 mW.

The maximum allowable drive power limits the ac voltages that may be applied across the crystal, and consequently affects the design of oscillator circuits. Crystal manufacturers usually specify the resistance of each crystal, as well as a maximum drive power. From these two, the maximum crystal ac voltage may be calculated.

A certain crystal is specified as having a resistance of 625 Ω. If the drive power is not to exceed 10 mW, calculate the maximum peak-to-peak ac voltage that may be developed across the crystal.

Example 19-1

solution

$$\text{Power dissipated} = P = \frac{V^2}{R}$$

where V is an rms voltage.

$$V = (PR)^{1/2} = (10 \times 10^{-3} \times 625)^{1/2} = (6.25)^{1/2} = 2.5 \text{ V}$$

and peak-to-peak volts is $2 \times 1.414 \times \text{Vrms} = 7.07\text{V}$.

Piezoelectric crystals cut from quartz and other natural materials are limited to a few shapes. This is a disadvantage because it limits the applications of natural crystals. Synthetic piezoelectric devices can be manufactured in almost any desired shape. Although they are generally unsuitable for such applications as oscillator stabilization, they can be used in other situations where quartz crystals are not appropriate.

The manufacture of synthetic piezoelectric devices involves pressing a ceramic powder, such as *barium titanate*, into required shapes, and then firing it in a high-temperature oven. During the firing process the material is

19-3
Synthetic
Piezoelectric
Devices

(a) Cylindrical transducer   (b) Bimorph
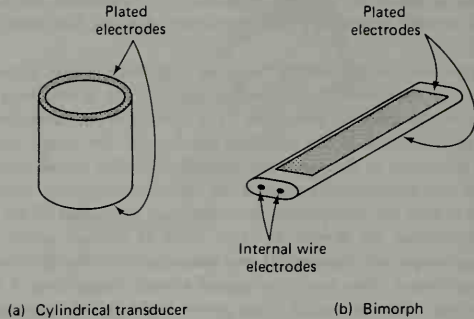
Figure 19-9. Ceramic piezoelectric transducers.

subjected to a high direct voltage. This has the effect of *polarizing* or aligning the atomic groups within the material into a pattern which can produce a piezoelectric effect. The finished devices generate an electrical output when the mechanical faces are distorted, and produce movement at the mechanical faces when an electrical potential is applied.

Two types of synthetic piezoelectric transducers are illustrated in Fig. 19–9. Figure 19–9(a) shows a cylindrical-shaped ceramic device with electrical contacts plated on each end. This kind of transducer is frequently used for listening to sea noises. A preamplifier is inserted inside, the cylinder is sealed at each end, and it is then suspended at the end of a long cable from a buoy or a boat at the surface. Every noise (ship engines and the like) causes a change in pressure on the sides of the transducer. The pressure variations in turn produce electrical signals at the device terminals. These are amplified and fed to the surface for conversion back to audio signals.

Figure 19–9(b) shows a ceramic device known as a *multimorph*. When supported at one end, electrical signals are generated at the internal and external electrodes by vibrations picked up at the other end. This device is basic to a record-player cartridge. The minute vibrations generated as the stylus moves in the record track are converted into electrical signals, and then amplified and fed to speakers.

19-4
Voltage-
Variable
Capacitor
Diodes

Voltage-variable capacitor diodes (VVC's) are also known as *varicaps*, *varactors*, and *epicaps*, as well as by several trade names. Basically, a VVC is simply a reverse-biased diode, and its capacitance is that of the junction depletion region. Recall that the width of the depletion region at a *pn*-junction depends upon the reverse-bias voltage [Fig. 19–10(a)]. A large reverse bias produces a wide depletion region, and with a small reverse bias the

(a) Principle of voltage variable capacitance diode   (b) Circuit symbol
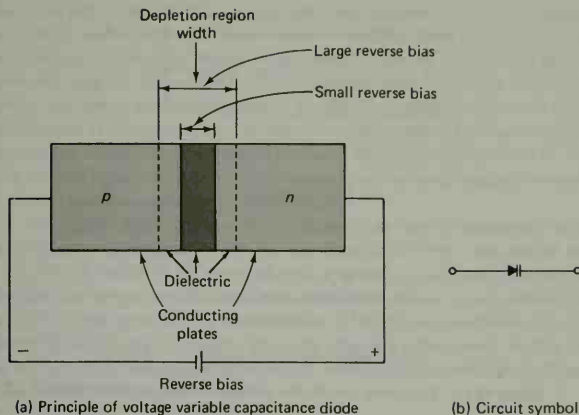
Figure 19-10. Principle of operation and circuit symbol for voltage-variable capacitor diode.

depletion region tends to be very narrow. Since the depletion region acts as a dielectric between two conducting plates, the device has the characteristics of a capacitor. As with all capacitors, the depletion layer capacitance (C_{pn}) is proportional to the junction area and inversely proportional to the width of the depletion region. Since the depletion region width is proportional to the reverse-bias voltage, C_{pn} is inversely proportional to the reverse-bias voltage. This is not a direct proportionality, $C_{pn} \propto 1/V^n$, where V is reverse bias voltage and n depends upon doping density. The circuit symbol for a VVC diode is shown in Fig. 19–10(b).

Figure 19–11(a) shows the equivalent circuit for a VVC diode. C_J is the *junction capacitance* shunted by R_J (the junction reverse leakage resistance). R_s represents the resistance of the semiconductor material, L_s is the package inductance, and C_c is the capacitance of the package. L_s is normally very small and R_J is very large, so for most purposes the equivalent circuit can be simplified to that of Fig. 19–11(b). In this case the diode capacitance is $C_T = C_J + C_C$. *Q factors* for the device can be as high as 600 at a frequency of 50 MHz. However, since the Q varies with bias voltage and frequency, it can be used only as a figure of merit for comparing the performance of different VVC's.

A wide selection of device nominal capacitances is available, ranging from 6 to 550 pF. The *capacitance tuning ratio TR* is the ratio of C_T at a small reverse voltage to C_T at a large reverse voltage. Depending upon the *doping profile* of the device, TR may be as small as 2 or as large as 15. Figure 19–12 shows the doping profiles for an *abrupt junction* diode and for a *hyperabrupt*
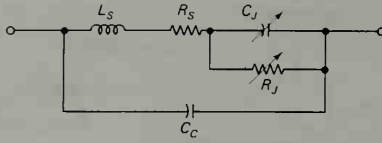
(a) Equivalent circuit
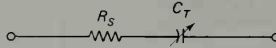
(b) Simplified equivalent circuit

Figure 19-11. Equivalent circuits for voltage-variable capacitor diode.
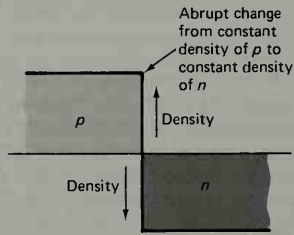
(a) Abrupt junction
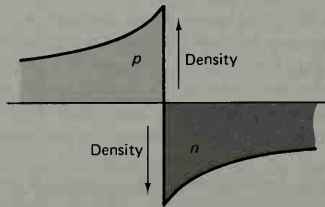
(b) Hyperabrupt junction

Figure 19-12. Doping profile at abrupt and hyperabrupt junction.

junction device. For the abrupt junction doping profile, the semiconductor material is uniformly doped and changes abruptly from *p*-type to *n*-type at the junction. In the case of the hyperabrupt junction, the doping density is increased close to the junction. This increased density makes the depletion region narrower and consequently produces a larger value of junction capacitance. It also causes the depletion region width to be more sensitive to bias voltage variations, and thus it produces the largest values of TR. Figure 19–13 shows typical graphs of diode capacitance plotted against reverse bias for abrupt and hyperabrupt junction devices.

The major application of VVC diodes is as tuning capacitors to adjust the frequency of resonance circuits. An example of this is the circuit shown in Fig.19–14, which is an amplifer with a tuned circuit load. The amplifier produces an output at the resonance frequency of the tuned circuit. Since the VVC diode provides the capacitance of the circuit, and since C_T can be altered by adjusting the diode bias, the resonance frequency of the circuit can be varied. C_c is a coupling capacitor with a value much larger than that of the VVC diode.

Calculate the capacitance tuning ratio (TR) at 1 V and 10 V for the abrupt junction and hyperabrupt junction devices with the characteristics in Fig. 19–13.

Example 19-2
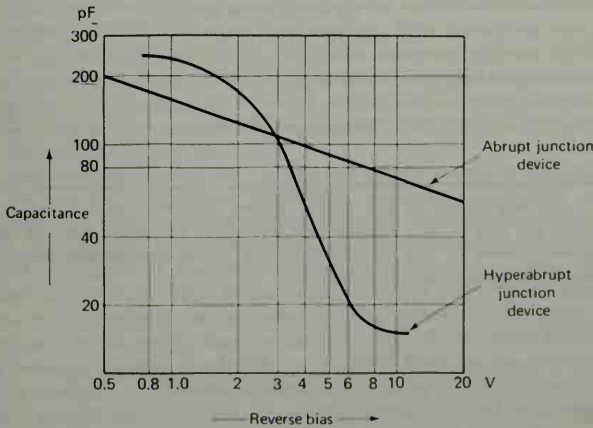
Figure 19-13. Capacitance–voltage characteristics for abrupt and hyperabrupt junction devices.
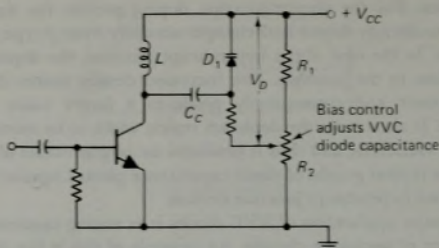
Figure 19-14. Amplifier with VVC diode frequency control.

solution

From the abrupt junction device characteristics in Fig. 19–13,

$$\text{At 1 V,} \quad C \approx 150 \text{ pF}$$
$$\text{At 10 V,} \quad C \approx 60 \text{ pF}$$

For the abrupt junction device,

$$\text{TR}_{(1\text{V}-10\text{v})} = \tfrac{150}{60} = 2.5$$

From the hyperabrupt junction device characteristics in Fig. 19-13,

$$\text{At 1 V}, C \approx 220 \text{ pF}$$
$$\text{At 10 V}, C \approx 15 \text{ pF}$$

For the hyperabrupt junction device,

$$\text{TR}_{(1\text{V}-\text{V})} = \tfrac{220}{15} = 14.6$$

Example 19-3   For the circuit of Fig. 19-14, $V_{CC} = 9$ V, $L = 100$ μH, $R_1 = 4.7$ kΩ, $R_2 = 10$ kΩ, and D_1 is a hyperabrupt junction VVC diode with the characteristic shown in Fig. 19–13. Calculate the maximum and minimum resonance frequency for the circuit.

solution

$$V_{D(\text{min})} = \frac{R_1}{R_1 + R_2} \times V_{CC} = \frac{4.7\text{k}\Omega}{4.7\text{k}\Omega + 10\text{k}\Omega} \times 9 \text{ V} = 2.9 \text{ V}$$

and

$$V_{D(\text{max})} = V_{CC}$$
$$= 9 \text{ V}$$

$$\text{At } V = 2.9 \text{ V} \quad C \approx 100 \text{ pF} \quad \text{At } V = 9 \text{ V}, \quad C \approx 15 \text{ pF}$$

At resonance,

$$2\pi f L = 1/2\pi f C_1$$

$$f = \frac{1}{2\pi (LC)^{1/2}}$$

For $V_{D(\min)}$,

$$f = \frac{1}{2\pi (100 \times 10^{-6} \times 100 \times 10^{-12})^{1/2}} \approx 1.6 \text{ MHz}$$

For $V_{D(\max)}$,

$$f = \frac{1}{2\pi (100 \times 10^{-6} \times 15 \times 10^{-12})^{1/2}} \approx 4.1 \text{ MHz}$$

The resonance frequency range is 1.6 to 4.1 MHz.

The word *thermistor* is a combination of *thermal* and *resistor*. A thermistor is a resistor with definite thermal characteristics. Most thermistors have a *negative temperature coefficient* (NTC), but *positive temperature coefficient* (PTC) devices are also available. Thermistors are widely applied for *temperature compensation*, i.e., canceling the effects of temperature on other electronic devices. They are also employed for measurement and control of temperature, liquid level, gas flow, etc.

19-5
Thermistors

Silicon and germanium are not normally used for thermistor manufacture, because larger and more predictable temperature coefficients are available with metallic oxides. Various mixtures of manganese, nickel, cobalt, copper, iron, and uranium are pressed into desired shapes and sintered (or baked) at high temperature to form thermistors. Electrical connections are made either by including fine wires during the shaping process or by silvering the surfaces after sintering. Thermistors are made in the shape of beads, probes, discs, washers, etc. (Fig. 19–15). Beads may be glass coated or enclosed in evacuated or gas-filled envelopes for protection against corrosion. Washer-shaped thermistors can be bolted together for series or parallel connection. Tiny thin-film thermistors, formed by sintering metal oxide coatings onto a ceramic or foil substrate, are also available.

A typical thermistor resistance–temperature characteristic is shown in Fig. 19–16. It is seen that the device resistance decreases by approximately
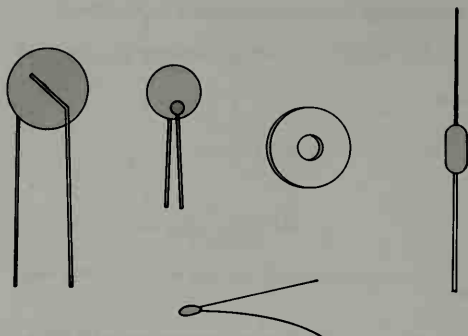
Figure 19-15. Some typical thermistor shapes.

500 times when heated through 150°C. Current through a thermistor causes power dissipation which raises the device temperature. Thus, the device resistance is dependent upon ambient temperature and self-heating. For a fixed ambient temperature the thermistor resistance is dependent upon its own power dissipation. Very small currents have no effect, so that a plot of voltage versus current (Fig. 19–17) shows the device behaving initially as a constant value resistance. As the current increases a peak is reached at which the heating effect of the current begins to significantly change the thermistor resistance. Further increase in current causes a progressive reduction in reistance, and consequently produces a reduction in voltage across the device.

Example 19-4   A thermistor with the resistance–temperature characteristic in Fig. 19–16 is employed in the circuit of Fig. 19–18. The relay coil has a resistance of 5 kΩ at -15°C, and 6.5 kΩ at 50°C. If the relay is energized by a current of 1 mA, calculate the required value of R_1 at -15°C and 50°C(a) with the thermistor and R_2 *not* in circuit; (b) with the thermistor in circuit; (c) with the thermistor and R_2 in the circuit.

solution

(a) Without the thermistor and R_2,

$$I = \frac{E}{R_1 + R_C}$$

$$R_1 = \frac{E}{I} - R_C$$
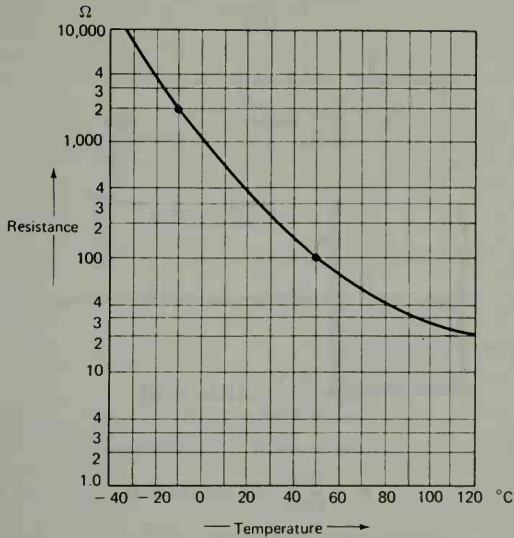
Figure 19-16. Typical resistance–temperature characteristic for thermistor.
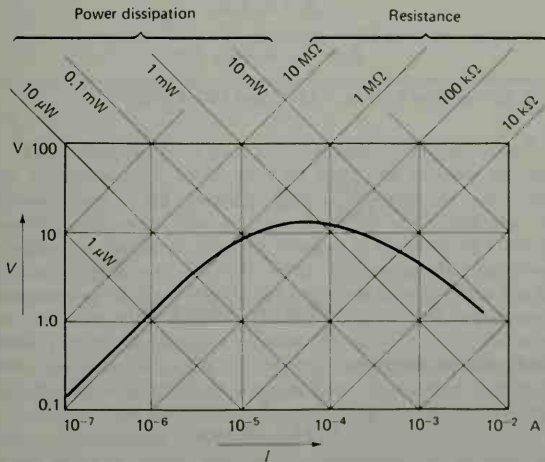
Figure 19-17. Static voltage–current characteristic for thermistor.

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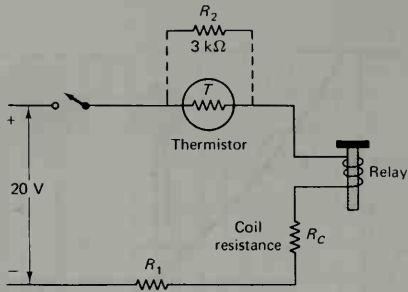
Figure 19-18. Thermistor compensation of relay circuit.

at $-15°C$

$$R_1 = \frac{20\,V}{1\,mA} - 5\,k\Omega = 15\,k\Omega$$

at 50°C

$$R_1 = \frac{20\,V}{1\,mA} - 6.5\,k\Omega = 13.5\,k\Omega$$

(b) With the thermistor,

$$I = \frac{E}{R_1 + R_T + R_C}$$

$$R_1 = \frac{E}{I} - R_T - R_C$$

From Fig. 19-16, $R_T = 3\,k\Omega$ at $-15°C$ and $100\,\Omega$ at $50°C$.

at $-15°C$

$$R_1 = \frac{20\,V}{1\,mA} - 3\,k\Omega - 5\,k\Omega = 12\,k\Omega$$

at 50°C

$$R_1 = \frac{20\,V}{1\,mA} - 100\,\Omega - 6.5\,k\Omega = 13.4\,k\Omega$$

(c) With R_2 and the thermistor,

$$I = \frac{E}{R_1 + (R_T \| R_2) + R_C}$$

$$R_1 = \frac{E}{I} - (R_T \| R_2) - R_C$$
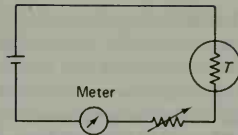
(a) Temperature measurement
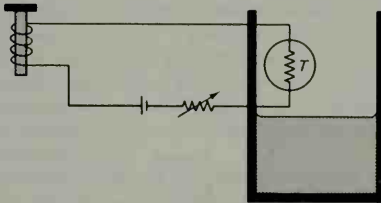
(b) Liquid level detection

Figure 19-19. Other thermistor applications.

at $-15\,^{\circ}C$

$$R_1 = \frac{20\,\text{V}}{1\text{mA}} - (3\,\text{k}\Omega \| 3\,\text{k}\Omega) - 5\,k\Omega = 13.5\,k\Omega$$

at $50\,^{\circ}C$

$$R_1 = \frac{20\,\text{V}}{1\,\text{mA}} - (3\,\text{k}\Omega \| 100\,\Omega) - 6.5\,\text{k}\Omega = 13.4\,\text{k}\Omega$$

From Example 19–4 we see that, without the thermistor in circuit, R_1 must be *reduced* from 15 to 13.5 kΩ when the ambient temperature is increased from $-15°$ to 50°C. This is necessary to allow the 1 mA energizing current to flow through the relay coil. With the unshunted thermistor in circuit, R_1 must be *increased* from 12 to 13.4 kΩ when the temperature goes from $-15°$ to 50°C. This means that the thermistor is *overcompensating* for the change in coil resistance. Finally, when the thermistor and 3 kΩ shunt are included in the circuit, virtually no adjustment of R_1 is necessary at the temperature extremes. Thus, the shunted thermistor completely compensates for the coil resistance change with temperature. Two points should be noted about Example 19-4 . One is that only the temperature extremes were looked at, and obviously the adequacy of compensation between the extremes should be considered. The other point is that the heating effect of current through the thermistor was assumed negligible. Other thermistor applications are illustrated in Fig. 19–19.

The *lambda diode* is a device which has characteristics similar to those of a tunnel diode. However, the typical bias voltage required by a lambda diode is not so inconveniently small as that needed for a tunnel diode.

A lambda diode is simply two complementary FET's connected as shown in Fig. 19–20(a). (*Complementary transistors* are two transistors which have similar parameters but are of different types. For bipolar transistors one would be a *pnp* type and the other an *npn*. For FET's one is an *n*-channel device and the other is a *p*-channel FET.)
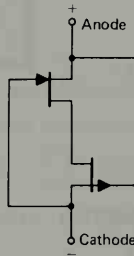
(a) Two FETs connected as a lambda diode
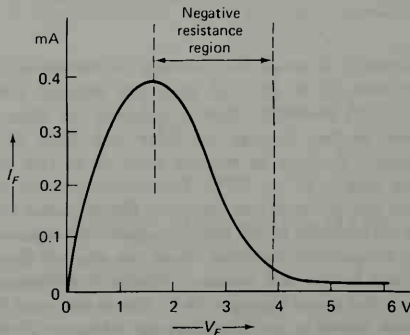
(b) Forward characteristics

Figure 19-20. Circuit and characteristics of a lambda diode.

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Note in Fig. 19–20(a) that the gate of each FET is connected to the source terminal of the other transistor. Note also that the two drain terminals are connected together, and that the source of the n-channel device is the anode of the lambda diode while the source of the p-channel FET is its cathode. Figure 19–20(c) shows typical characteristics for the lambda diode.

To understand the device characteristics, consider the situation when a small voltage (say, 0.5 V) is applied, positive to the anode, negative to the cathode. The gate of Q_1 is -0.5 V with respect to its source. This is *not* a large enough gate–channel reverse bias to turn the device off. Similarly, the gate of Q_2, the p-channel FET, is 0.5 V positive with respect to Q_2's source. Again, this is a reverse bias at the gate–channel junction, but not large enough to bias the FET off. Under these conditions both transistors are conducting. Consequently, when the lambda diode forward-bias voltage is increased from zero through 0.5 V, the current flowing increases in proportion to the applied voltage.

As the forward-bias voltage of the lambda diode is increased, the reverse bias at the gate–channel junction of each FET also increases. Eventually, the reverse-bias voltage becomes large enough to begin to turn each device off (depletion region penetration; see Section 12-2). The point at which the reverse-bias voltage becomes effective is the point on the characteristic at which the current is a peak. As the lambda diode forward voltage is increased beyond this point, the FET channels are narrowed and the current falls steadily to a very low (drain–source leakage) level. With both FET's biased off, further increases in (forward) voltage have no effect. At some high voltage level device breakdown would occur, of course.

When a reverse-bias voltage is applied to the lambda diode, the gate of the n-channel, FET is always positive with respect to its channel, and the p-channel FET always has its gate biased negative with respect to the channel. Consequently, neither FET can become biased off with this voltage polarity. The reverse characteristic is, therefore, that of a resistance equal to the sum of FET channel resistances.

Like the tunnel diode, the negative resistance of the lambda diode allows it to be used as a parallel or series amplifier and in oscillator and switching circuits. The voltage required to bias the lambda diode into its negative resistance region is typically 2 to 3 V, compared to about 200 mV for the tunnel diode. This makes the lambda diode easier to use in a laboratory situation.

Piezoelectric crystal. Crystal which generates a voltage when pressed, and distorts when a voltage is applied to its surface.

Rochelle salt, tourmaline, quartz. Natural materials which have piezoelectric properties.

Optical axis (Z axis). Axis of quartz crystal at which no piezoelectric effect is exhibited.

Electrical axis (X axis). Crystal axis at which a voltage appears when mechanical stress is applied at the mechanical axis.

*Glossary of
Important
Terms*

Mechanical axis (_Y_ axis).   Crystal axis at which a mechanical stress causes a voltage to be generated at the electrical axis.

_X_-cut.   Crystal section cut with its flat sides perpendicular to the electrical axis.

_Y_-cut.   Crystal cut with its flat sides perpendicular to the mechanical axis.

_GT_-cut.   Flat rectangular section cut from crystal at a particular angle to the various axes to give zero temperature coefficient.

Ring-shaped cut.   Crystal cut in ring shape, and at a particular angle to the various axes to give zero temperature coefficient.

Series resonance frequency.   Frequency at which crystal series capacitive reactance and inductive reactance are equal. Frequency at which crystal impedance is a minimum.

Parallel resonance frequency.   Frequency at which the capacitance of the crystal electrodes resonates with reactance of the crystal circuit. Frequency at which crystal impedance is a maximum.

_Q_ factor.   Ratio of reactance to resistance for a resonant circuit.

Overtone operation.   Operation of crystal to control a circuit which is resonating at a frequency which is a multiple of the crystal frequency.

Crystal oven.   Insulated crystal enclosure in which the temperature is thermostatically controlled in order to stabilize the crystal frequency.

Synthetic piezoelectric device.   Ceramic device which exhibits piezo-electric characteristics.

VVC diode.   Variable-voltage capacitance diode. Diode in which junction capacitance is controlled by reverse-bias voltage.

Varicap, varactor, epicap.   Other names for a VVC diode.

Capacitance tuning ratio.   Ratio of VVC diode capacitance at a small reverse voltage to that at a large reverse voltage.

Doping profile.   Graph showing doping density at a _pn_-junction.

Abrupt junction.   _pn_-Junction at which uniform doping density changes abruptly from _p_-type to _n_-type.

Hyperabrupt junction.   _pn_-Junction at which doping density increases near the junction, and changes abruptly from _p_-type to _n_-type.

Thermistor.   Device which exhibits a large resistance change with temperature change.

Lambda diode.   Two field effect transistors connected to simulate the performance of a tunnel diode.

Review Questions

19-1. Sketch a flat plan diagram to show the arrangement of atoms within a piezoelectric crystal. Identify the electrical axis and the mechanical axis, and show how a mechanical stress can cause voltage generation, and how an applied potential can produce crystal distortion.

19-2. (a) Sketch the approximate shape of a natural crystal, and identify each axis by name and symbol. (b) Draw sketches to illustrate X-cut, Y-cut, GT-cut, and ring-shaped crystal cut. Briefly explain.

19-3. (a) Sketch the equivalent circuit of a piezoelectric crystal and explain the origin of each component. (b) Draw a sketch of a typical impedance–frequency graph for a piezoelectric crystal. Identify and explain each of the two resonance frequencies.

19-4. (a) Explain the Q factor and compare the Q factor of a crystal to that of an ordinary electrical resonant circuit. (b) Describe how greatest possible crystal frequency stability is achieved. (c) Define *overtone operation* of a crystal.

19-5. Sketch two crystal-controlled oscillator circuits, one using a crystal in parallel resonance, and the other using a series resonant crystal. Explain the operation of each circuit. Also state two important considerations for using crystals.

19-6. Discuss the manufacture and applications of synthetic piezoelectric devices.

19-7. (a) Using illustrations, explain the operation of a VVC diode.
(b) Sketch the equivalent circuit for a VVC diode. Explain the origin of each component and show how the circuit may be simplified.

19-8. (a) Explain the difference between abrupt and hyperabrupt junction VVC diodes. Draw sketches to illustrate the differences. (b) Sketch typical capacitance–voltage characteristics for abrupt junction and hyperabrupt junction devices. (c) Sketch a circuit to show an application of a VVC diode.

19-9. (a) Describe the performance of a thermistor and explain its construction. (b) Sketch typical resistance–temperature and voltage–current characteristics for a thermistor. Briefly explain.

19-10. Sketch circuit diagrams to show applications of thermistors to (a) compensation of a relay circuit, (b) liquid level detection, (c) temperature measurement. Briefly explain the operation of each circuit. Draw a diagram to show how a NTC thermistor might be used to compensate for V_{BE} variations (due to temperature change) in an emitter current biased transistor circuit.

19-11. Sketch a diagram to show the construction of a lambda diode. Also sketch typical forward characteristics for the device. Explain the operation of the device and the shape of the characteristics. What would the reverse characteristics of this device look like? Briefly explain.

19-1. A crystal with a resistance of 7 kΩ has a specified maximum drive power of 2 mW. Determine the peak-to-peak ac voltage that may be developed across the crystal.

Problems

19-2. Examine each of the oscillator circuits in Figs. 10-1 through 10-6. Describe how piezoelectric crystals might be employed in every circuit to stabilize the output frequency. Also estimate the crystal power dissipation in each case.

19-3. Calculate the capacitance tuning ratio (TR) at 2 V and 8 V for the abrupt junction and hyperabrupt junction devices with the characteristics in Fig. 19-13.

19-4. The frequency-controlled circuit in Fig. 19-14 has $V_{CC} = 20$ V, $L = 80$ μH, $R_1 = 3.3$ kΩ, $R_2 = 20$ kΩ, and D_1 is an abrupt junction device with the characteristics in Fig. 19-13. Determine the maximum and minimum resonance frequencies for the circuit.

19-5. The circuit shown in Fig. 19-19(a) uses a 1.5 V battery and a 1 mA meter. The thermistor used has the resistance–temperature characteristics in Fig. 19-16. Calculate the value of the variable resistance if the meter is to read full scale when the tempeature is 80°C. Assuming that the variable resistance remains unaltered, calculate the meter readings for temperatures of 50°, 20°, and −10°C.

19-6. A relay coil has a resistance of 3.3 kΩ at −15°C and 5 kΩ at 80°C. The relay is energized by a current of 0.5 mA from a 10 V supply in series with a resistance R_1. A thermistor is to be connected in series with the relay and R_1 to provide temperature compensation:
    (a) Sketch the circuit and calculate the required value of R_1 at −15° and at 80°C.
    (b) If the thermistor is included and has the characteristic shown in Fig. 19-16, calculate the new values for R_1 at −15° and 80°C.
    (c) With the thermistor shunted by a 4.1 kΩ resistance, again calculate the required values of R_1 at −15° and 80°C.

Electron Tubes

Electrons can be made to travel through a metallic crystal. They can also be made to travel through a vacuum. In the *vacuum diode*, two electrodes are contained in a glass envelope from which the air has been evacuated. One of the electrodes, termed the *cathode*, is heated electrically, so that it emits electrons. The other electrode, known as the *plate* or *anode*, is maintained at a positive potential with respect to the cathode. Since electrons are negatively charged they are attracted toward the plate, so that a current flows (in the conventional direction) from the positive plate to the negative cathode. If the plate potential is reduced to zero or reversed, the current is cut off. Additional electrodes introduced between the plate and cathode afford control over the plate current and create a wide range of multielectrode tubes.

Vacuum diodes are usually constructed with the *plate* in the form of a cylinder and with the cathode at the center of the plate (Fig. 20-1). The cathode may be a simple filament of *tungsten* or *thoriated tungsten*. Alternatively, it may be a nickel tube coated with *barium oxide* or *strontium oxide*, and heated by an insulated *filament*. The greatest emission efficiencies are available with oxide-coated cathodes, but filament cathodes are toughest.

In low power tubes the plate is usually nickel or iron. For high-power tubes, *tantalum*, *molybdenum*, or *graphite* may be used, because they do not deteriorate as rapidly as iron or nickel at high temperatures. For high-voltage tubes, the plate voltage limit is determined by the insulation resistance between electrodes, rather than by the tube dissipation. For this reason, the plate terminal is frequently at the opposite end of the tube from the other terminals.

Typical vacuum diode characteristics are shown plotted in Fig. 20-2. When the *plate voltage* (E_p) is zero, very few of the electrons emitted from the cathode are attracted to the plate. Hence the *plate current* (I_p) is near zero. When E_p is increased positively from zero, the plate attracts electrons from the cathode. Initially only a small quantity of the electrons flows from cathode to plate. As the plate voltage increases, more and more electrons flow to it until there is almost a linear increase of plate current with increase
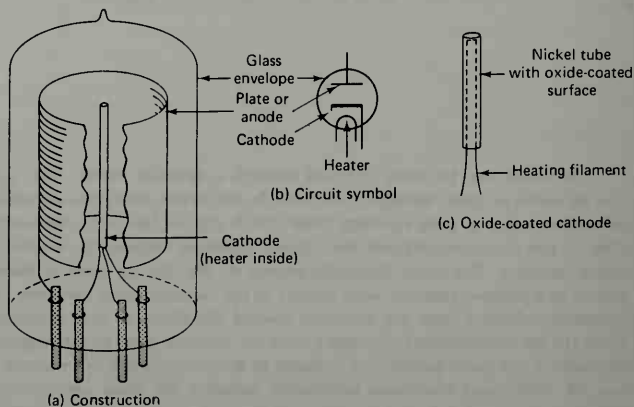
Figure 20-1. Vacuum diode construction and circuit symbol.

flow to it until there is almost a linear increase of plate current with increase in plate voltage. With a continued increase in plate voltage, the plate current eventually reaches a *saturation* level. At this point all available electrons from the cathode are being drawn to the plate. Further increase in E_p produces only a slight increase in I_p. If the cathode temperature is increased, more electrons are emitted and I_p is raised to a new saturation level, (T_2 in Fig. 20-2).

There are two major regions of the diode characteristics, the *space-charge limited region*, and the *temperature-limited region*. The diode is operating in its space-charge limited region when more electrons are being produced at the cathode than are being drawn to the plate. In this condition the plate current is dependent on the plate-to-cathode voltage. In the temperature-limited region, the plate potential is so great that all the electrons produced at the cathode are being drawn to the plate.

In the space-charge limited region, there is always a *cloud* of emitted electrons around the cathode (because more electrons are emitted than are drawn to the anode). *Positive ions*, which are formed by electron collision with gas molecules, are accelerated toward the cathode, but enter the electron cloud and become neutralized by recombining with electrons. When operating in the temperature-limited region, there is no protective cloud of electrons around the cathode, so positive ions can strike the cathode and seriously damage the oxide coating. For this reason, electron tubes are normally operated in the space-charge limited region.
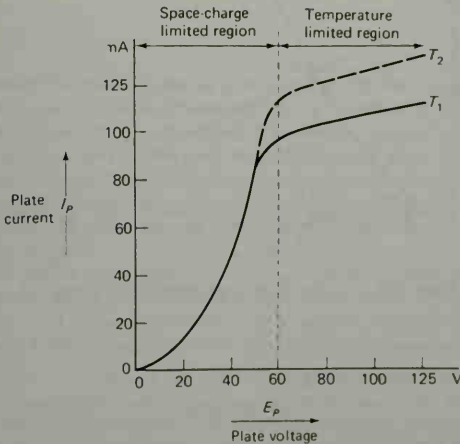
Figure 20-2. Vacuum diode characteristics.

Like the semiconductor diode, the vacuum diode is a one-way device. Therefore, its applications are essentially the same as the semiconductor diode applications described in Chapter 3. The vacuum diode has the disadvantage that its operating plate-to-cathode voltage is typically 5 to 30 V (or greater). The semiconductor diode, by contrast, has an approximately 1 V drop across it when operating. Also, the vacuum diode requires an additional supply for the cathode heater. When the added disadvantage of the vacuum diode's greater physical size is considered, it is seen that there is no vacuum diode function that cannot be more conveniently performed by a semiconductor diode.

Example 20-1

A vacuum diode with the characteristic shown in Fig. 20-3 is connected in series with a supply of 100 V and a load resistance of 4 kΩ. Draw the dc load line for the circuit and determine the value of plate current and plate voltage.
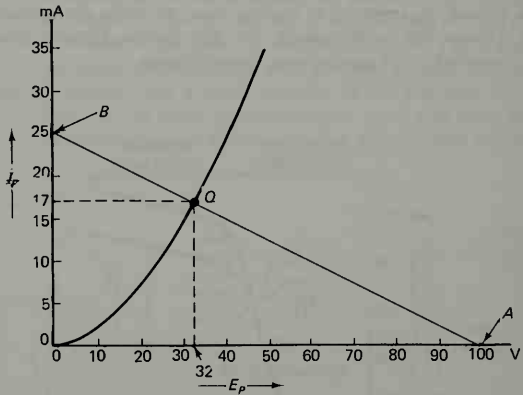
Figure 20-3. Vacuum diode characteristics and dc load line.

solution

The circuit is as shown in Fig. 20-4. From the circuit,

$$E = E_p + I_p R_L$$

When $I_p = 0$, $E = E_p + 0$.

$$E_p = 100 \text{ V}$$
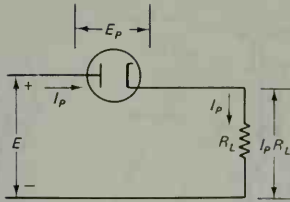
Figure 20-4. Vacuum diode with series load.

Plot point A on the characteristic at $I_p = 0$, $E_p = 100$ V.
When $E_p = 0$, $E = 0 + I_p R_L$.

$$I_p = \frac{E}{R_L} = \frac{100}{4 \text{ k}\Omega} = 25 \text{ mA}$$

Plot point B at $E_p = 0$, $I_p = 25$ mA.
Draw the dc load line between points A and B.
From the intersection of the load line and the characteristic at point Q, read
$I_p = 17$ mA and $E_p = 32$ V.

20-3
The Vacuum
Triode

20-3.1
Grid Effect

Consider the effect of placing a wire grid in the electron tube between the cathode and the plate. When the grid is biased to a large negative voltage with respect to the cathode, all electrons are repelled by it so that no electrons are permitted to pass from the cathode to the plate. When the grid is made only slightly negative with respect to the cathode, many electrons are able to pass through the grid wires to the plate. Thus, by varying the grid potential the plate current is increased, decreased, or switched off completely.

If the grid is made positive with respect to the cathode, electrons are attracted to it, and a grid current will flow. Since this is a condition to be avoided, the grid is always maintained at a negative voltage with respect to the cathode. With the addition of the grid the tube becomes a *vacuum triode*.

The construction and the schematic symbol employed for a vacuum triode are illustrated in Fig. 20-5. The cathode and plate are normally of the same type of construction as for a diode tube. The grid is usually a nickel wire, spiral wound around two support posts. In some modern miniature

20-3.2
Construction

(a) Construction
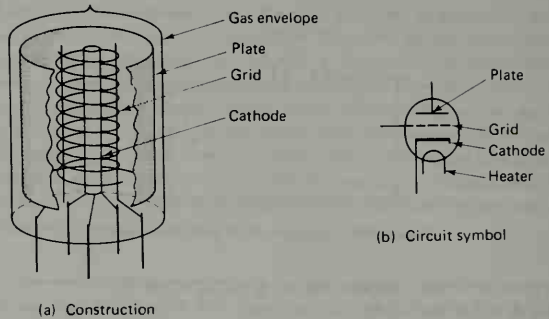
(b) Circuit symbol

Figure 20-5. Triode construction and circuit symbol.

tubes, the grid is a self-supporting wire mesh. The connections for grid, plate, cathode, and cathode heaters are usually brought out at the base of the tube.

20-4
Triode
Characteristics

20-4.1
Plate
Characteristics

When the grid of a triode is maintained at the same potential as the cathode, the triode plate characteristics are similar to those of a diode. Thus, in Fig. 20-6 the triode I_p/E_p characteristic for $E_g = 0$ is exactly as would be expected from a diode tube operating in the space-charge limited region. If E_p is increased further, the temperature-limited region will eventually be reached.

When the grid is made 1 V negative with respect to the cathode ($E_g = -1$ V), then the I_p/E_p characteristic is significantly altered from that for $E_g = 0$. This is because the grid at -1 V constitutes a large negative barrier for electrons to cross before they can pass from cathode to plate. Therefore, the plate current does *not* commence when E_p is around zero volts; instead, E_p has to be made substantially greater than zero before any plate current will flow. Also, at each subsequent level of E_p, the plate current is less than when $E_g = 0$. The effect is that of the $E_g = 0$ characteristic being moved to the right. This is illustrated by the $E_g = -1$ V characteristic in Fig. 20-6.

When the negative bias on the grid is greater than 1 V, the plate characteristic is moved even farther to the right. Thus, using various values of grid voltage, a *family* of I_p/E_p characteristics can be obtained as shown in the figure. If the grid is made positive with respect to the cathode, the
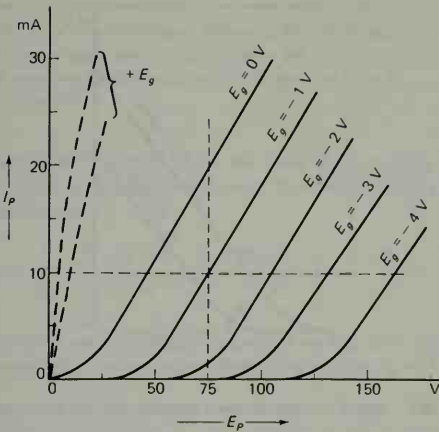
Figure 20-6. Typical plate characteristics for a vacuum triode.

characteristics are as shown by the broken lines in Fig. 20-6. In this case, electrons are being collected by the positive grid, and grid current is flowing. This is a condition normally avoided.

We have already seen that the plate current can be controlled by variation of the grid voltage. If the plate voltage is held constant and the plate current values are recorded for each setting of grid voltage, the *transconductance characteristic* or *transfer characteristic* is obtained (Fig. 20-7).

Referring to Fig. 20-7, it is seen that, for $E_p = 100$ V and $E_g = 0$ V, $I_p = 28$ mA. If E_p is held constant at 100 V and E_g is altered to -1 V, I_p will be reduced because the negative grid will retard the flow of electrons from cathode to plate. A further alteration of E_g to more negative levels (with E_p maintained at 100 V) will further decrease I_p. Using a new constant value of E_p, new levels of I_p are obtained for each $-E_g$ setting. Thus, using different E_p voltages a family of transconductance characteristics can be plotted.

These characteristics are obtained by keeping I_p at a fixed level, and plotting grid voltage (E_g) versus plate voltage (E_p) (Fig. 20-8).

From any one set of characteristics the other two may be derived. Consider the plate characteristics shown on Fig. 20-6. If a horizontal line is drawn at $I_p = 10$ mA, then at the intersection of the line and each E_p/I_p

20-4.2
*Trans-
conductance
Characteristics*

20-4.3
*Constant
Current
Characteristics*

20-4.4
*Relationships
Between
Characteristics*
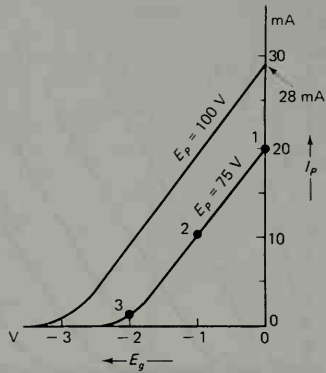
Figure 20-7. Typical transconductance characteristics for a vacuum triode.

graph the corresponding values of E_g and E_p can be read. Hence, the grid voltage values can be plotted against the plate voltage values to obtain the constant current characteristic for $I_p = 10$ mA.

Similarly, if a vertical line is drawn representing a constant value of plate voltage, then the corresponding values of E_g and I_p can be read where the line cuts each graph (see Fig. 20-6). From these readings the transconductance characteristics can be plotted for the plate voltage selected. By a similar method, either of the other two sets of characteristics may be used to produce all three sets of characteristics.
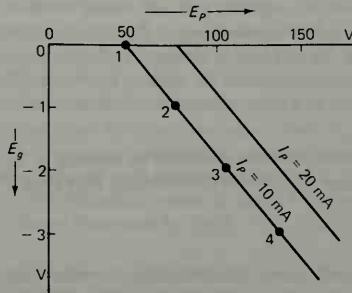
Figure 20-8. Typical constant current characteristics for vacuum triode.

From the plate characteristics shown in Fig. 20-6 derive

Example 20-2

(a) The transconductance characteristic for $E_p = 75$ V.

(b) The constant current characteristic for $I_p = 10$ mA.

solution (a)

Draw a vertical line at $E_p = 75$ V on the plate characteristics (Fig. 20-6). Where the line cuts each characteristic, read the corresponding plate current and grid voltage values:

I_p	20 mA	10 mA	2 mA
E_g	0 V	-1 V	-2 V

Plot the above values at points 1, 2, and 3 on Fig. 20-7. Join the points together to draw the transconductance characteristic for $E_p = 75$ V.

solution (b)

Draw a horizontal line at $I_p = 10$ mA on the plate characteristics (Fig. 20-6). Where the line cuts each characteristic, read the corresponding plate voltage and grid voltage values:

E_g	0 V	-1 V	-2 V	-3 V
E_p	45 V	75 V	105 V	132 V

Plot the above values at points 1, 2, 3, and 4 on Fig. 20-8. Join the points together to draw the constant current characteristic for $I_p = 10$ mA.

20-5
Triode
Parameters

Consider the plate characteristics shown in Fig. 20-9(a). The reciprocal of the slope of the $E_g = 0$ characteristic at $E_p = 75$ V is

20-5.1
Plate
Resistance
(r_p)

$$\frac{\Delta E_p}{\Delta I_p} = (\text{a resistance}) = r_p \qquad (20\text{-}1)$$

From the characteristic

$$r_p = \frac{30 \text{ V}}{10 \text{ mA}} = 3 \text{ k}\Omega$$

The *plate resistance* is the resistance offered by the vacuum tube to plate voltage variations when the grid voltage is held constant. Thus, if E_g is held
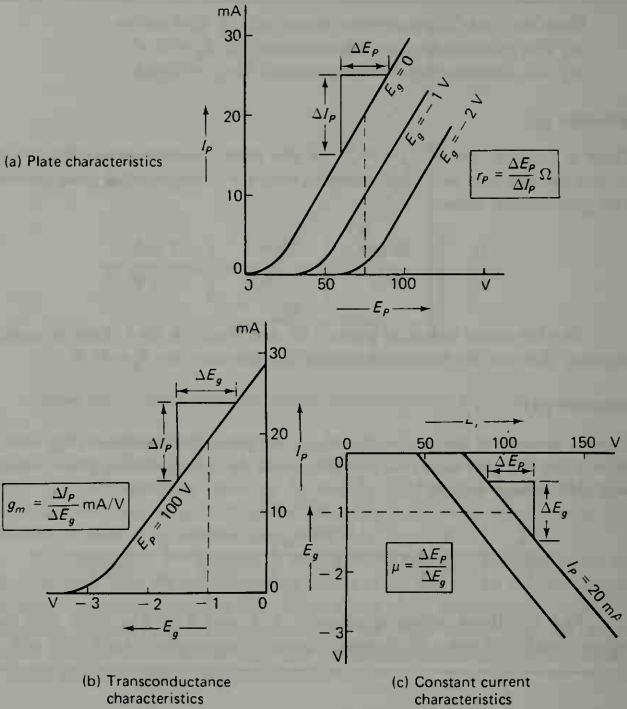
Figure 20-9. Derivation of parameters from triode characteristics.

constant at 0 V and E_p is varied by 30 V, I_p would be altered by $\Delta E_p / r_p = 30\text{V}/3\text{ k}\Omega = 10$ mA. Typical values of r_p range from 250 Ω to 70 kΩ.

20-5.2
*Transcon-
ductance (g_m)*

From the transconductance characteristics on Fig. 20-9(b) the slope of the $E_p = 100$ V characteristic at $E_g = 1$ V is

$$\frac{\Delta I_p}{\Delta E_g} = (\text{a conductance}) = g_m \qquad (20\text{-}2)$$

From the characteristic, $g_m = (10 \times 10^{-3})/1 = 0.01$ S, or $g_m = 10$ mA/V.

The *transconductance* (g_m) is a measure of the grid voltage control over plate current when the plate voltage is held constant. For the g_m value

calculated above, each 1 V variation in E_g will cause I_p to be altered by 10 mA. Typical values of g_m range from 1 to 10 mA/V.

Electron emission from the cathode of a vacuum tube decreases as the tube approaches the end of its useful life. This causes a decrease in the value of g_m for the tube. Thus g_m is useful as an indication of how good a vacuum tube is (i.e., it is a figure of merit).

From the constant current characteristics of Fig. 20-9(c), the slope of the $I_p = 20$ mA characteristic at $E_g = -1$ V is

$$\frac{\Delta E_p}{\Delta E_g} = (\text{a ratio}) = \mu \tag{20-3}$$

From the characteristic

$$\mu = \frac{30 \text{ V}}{1 \text{ V}} = 30$$

The *amplification factor* (μ) is a measure of the relative effectiveness of plate voltage and grid voltage as controllers of the plate current. From the characteristics it is seen that a variation in E_g of 1 V will change I_p by 10 mA when E_p remains constant. To achieve the same variation in I_p with E_g held constant requires E_p to be changed by 30 V. Thus, E_g is μ times as effective as E_p in controlling I_p ($\mu = 30$ in this case). Typical values of μ range from 2.5 to 100.

The following formula manipulation shows the relationship between μ, g_m, and r_p. The expression for μ is multiplied by $\Delta I_p / \Delta I_p$, which is the same as multiplying by 1.

$$\mu = \frac{\Delta E_p}{\Delta E_g} = \frac{\Delta E_p}{\Delta E_g} \times \frac{\Delta I_p}{\Delta I_p} = \frac{\Delta E_p}{\Delta I_p} \times \frac{\Delta I_p}{\Delta E_g}$$

$$\mu = r_p \times g_m$$

$$g_m = \frac{\mu}{r_p}$$

$$r_p = \frac{\mu}{g_m} \quad \text{where } g_m \text{ is in } A/V, \text{ not mA/V}$$

The three major circuit configurations that may be used with electron tubes are *common cathode*, *common plate*, and *common grid*. The common cathode circuit is shown schematically in Fig. 20-10.
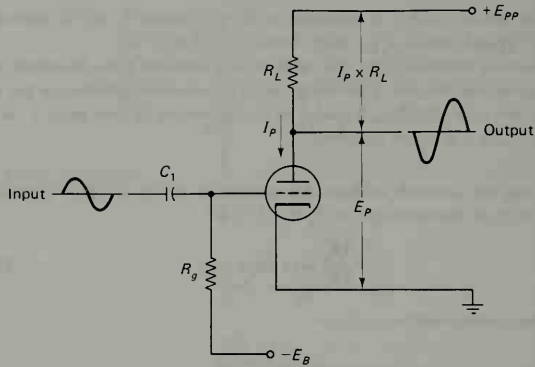
Figure 20-10. Common cathode amplifier.

It can be seen from the circuit that the grid of the triode is biased negatively with respect to the cathode. The resistance R_g is referred to as the *grid leak*, and its function is to connect the bias voltage to the grid so that input signals are not short circuited by E_g. Since no grid current flows, the signal "sees" an input resistance equal to R_g. R_g is typically 1 MΩ, and if it is made too large electrons may accumulate on the grid and alter the bias voltage. Therefore, another function of R_g is to "leak" electrons off the grid. The input signal is applied via C_1 to the grid, and the output voltage is developed across the load R_L. The plate current flows through the load resistor R_L, so that

$$E_p = E_{PP} - I_p R_L$$

**20-6.2
DC Load
Line**

Using the above equation, the dc load line may be drawn on the plate characteristics. Take $R_L = 10$ kΩ and $E_{pp} = 200$ V. When $I_p = 0$,

$$E_p = E_{pp} - 0 = 200 \text{ V}$$

$I_p = 0$ and $E_p = 200$ V are plotted to obtain one point on the dc load line, point A on Fig. 20-11. When $E_p = 0$,

$$I_p = \frac{E_p}{R_L} = \frac{200 \text{ V}}{10 \text{ kΩ}} = 20 \text{ mA}$$

$E_p = 0$ and $I_p = 20$ mA are plotted to obtain point B on the characteristics. The dc load line is drawn by joining these two points together as shown. This is the load line for $R_L = 10$ kΩ and $E_{pp} = 200$ V. If either R_L or E_{pp} is altered, a new load line must be drawn.
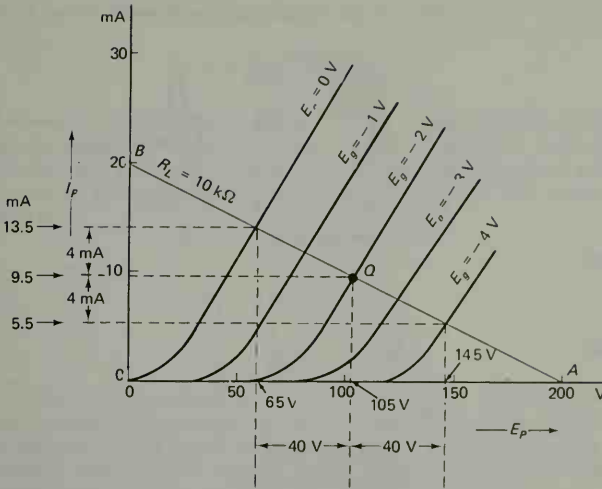
Figure 20-11. DC load line for triode amplifier.

Let the circuit be biased to point Q on the dc load line. At point Q, $E_g = -2$ V, $I_p \simeq 9.5$ mA, and $E_p = 105$. If E_g is now altered to zero volts, I_p becomes 13.5 mA and E_p becomes 65 V. Therefore, a change of $+2$ V at the grid has produced a $+4$ mA change in I_p and a -40 V change in E_p. Similarly, when E_g is changed from -2 to -4V, I_p changes from 9.5 to 5.5 mA and E_p changes from 105 to 145 V. Thus, a -2 V change in E_g produces a -4 mA change in I_p and a $+40$ V change in E_p. Therefore, a signal of ± 2 V produces an output voltage of ± 40 V, so that a voltage gain in this case equal to 20 is obtained. Also, I_p increases when E_g is increased (positively) and decreases when E_g is decreased. So I_p changes in phase with the grid signal voltage. E_p, on the other hand, decreases when E_g is increased (positively), and increases when E_g decreases. Therefore, the output voltage of the common cathode amplifier is antiphase to the input voltage.

The grid voltage variations discussed above could be produced by an ac signal coupled via capacitor C_1 in Fig. 20-10. From the point of view of the ac performance of the circuit, the actual dc bias and supply voltages can be regarded as short circuits. Redrawing the circuit to include the signal voltage e_s, and with E_g and E_{pp} shorted out, gives the ac equivalent circuit shown in Fig. 20-12(a). From the ac equivalent circuit it is seen that the input signal e_s is applied between the grid and cathode terminals of the tube.
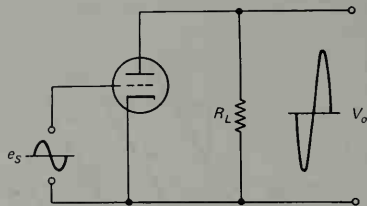
(a) dc voltages become ac short circuits
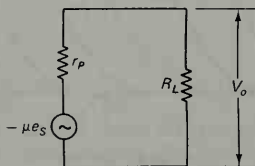
Voltage equivalent circuit

(b) Vacuum tube becomes voltage generator of
voltage $-\mu e_s$ and internal resistance r_p

Figure 20-12. Developing ac equivalent circuit for common cathode amplifier.

Also, the output voltage V_o is derived across the plate and cathode terminals. The cathode terminal is common to both input and output, hence the circuit name *common cathode*.

In the ac equivalent circuit the vacuum tube may be replaced by a voltage source of $-\mu e_s$ volts. The ac internal resistance of the vacuum triode is the plate resistance r_p. Therefore, the voltage source representing the tube must have an internal resistance of r_p. The complete ac equivalent circuit is now the voltage equivalent circuit shown in Fig. 20-12(b).

From the voltage equivalent circuit it is seen that $-\mu e_s$ is potentially divided across r_p and R_L to produce the output voltage V_0. Therefore,

$$V_0 = -\mu e_s \times \frac{R_L}{r_p + R_L}$$

The voltage gain

$$A_v = \frac{V_0}{e_s} = \frac{-\mu R_L}{r_p + R_L} \tag{20-5}$$

Using typical values of $\mu = 30$, $r_p = 5$ kΩ, and $R_L = 10$ kΩ,

$$A_v = \frac{-30 \times 10 \text{ k}\Omega}{5 \text{ k}\Omega + 10 \text{ k}\Omega} = -20$$

"Looking in" to the equivalent circuits from the output terminals, it is seen that the output impedance of a common cathode amplifier is r_p in parallel with R_L. Also, so long as the grid is biased negatively with respect to the cathode, no grid current flows, and the circuit has a high input resistance equal to R_g.

$$Z_o = r_p \| R_L \tag{20-6}$$

and

$$Z_i = R_g \tag{20-7}$$

The common cathode circuit can now be defined as having a high input resistance, an output resistance of R_L in parallel with r_p, substantial voltage gain, and its output voltage antiphase to the input signal. Like its transistor equivalent (the common emitter circuit), the common cathode configuration is the most frequently used of all vacuum-tube circuits.

A vacuum triode used in a common cathode amplifier circuit has the plate characteristics shown in Fig. 20-13. If the load resistance is 7 kΩ, the supply voltage is 175 V, and the grid bias is -2 V, determine I_p and E_p. Calculate the input impedance, output impedance, and voltage gain of the amplifier.

Example 20-3

solution

$$E_{PP} = E_p + I_p R_L$$

when $I_p = 0$, $E_{PP} = E_p + 0$.

$$E_p = 175 \text{ V}$$

Plot point A on the characteristic at $I_p = 0$, $E_p = 175$ V.
    When $E_p = 0$, $E_{PP} = 0 + I_p R_L$.

$$I_p = \frac{E_{PP}}{R_L} = \frac{175 \text{ V}}{7 \text{ k}\Omega} = 25 \text{ mA}$$

Plot point B at $I_p = 25$ mA, $E_p = 0$ V.
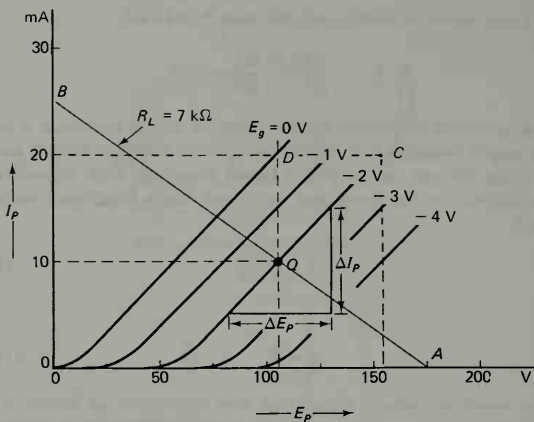
Figure 20-13. Plate characteristics, load line, and parameters for Example 20-3.

Draw the dc load line from point A to B. Where the load line intersects the $E_g = -2$ V characteristic, read

$$I_p = 10 \text{ mA} \quad \text{and} \quad E_p = 105 \text{ V}$$

input impedance
From Eq.(20-7),

$$Z_i = R_g = 1 \text{ M}\Omega \quad \text{typically}$$

output impedance
From Eq. (20-6),

$$Z_o = r_p \| R_L$$

and

$$r_p = \frac{\Delta E_p}{\Delta I_p} = \frac{50 \text{ V}}{10 \text{ mA}} \text{ (from the characteristics)} = 5 \text{ k}\Omega$$

Output impedance $= R_L \| r_p$

$$= \frac{7 \text{ k}\Omega \times 5 \text{ k}\Omega}{7 \text{ k}\Omega + 5 \text{ k}\Omega} = 2.9 \text{ k}\Omega$$

From Eq. (20-5),

$$A_v = \frac{\mu R_L}{r_p + R_L}$$

From Eq. (20-3),

$$\mu = \frac{\Delta E_p}{\Delta E_g}$$

At the bias point, an increase in E_p of 50 V produces a change in I_p of 10 mA when E_g remains at -2 V. At the bias point, a decrease of 2 V in E_g produces a change of 10 mA in I_p if E_p remains at 105 V. Thus,

$$\mu = \frac{50 \text{ V}}{2 \text{ V}} = 25$$

The voltage gain is

$$A_v = \frac{25 \times 7 \text{ k}\Omega}{5 \text{ k}\Omega + 7 \text{ k}\Omega} = 14.6$$

In this circuit (shown in Fig. 20-14) the load resistance R_L is connected in series with the cathode of the tube. The grid bias voltage E_B is now positive, but the grid-to-cathode voltage E_g is *not* equal to the grid bias voltage. Because of the voltage drop across R_L,

20-8
Common
Plate
Circuit

or

$$E_g = E_B - (I_p \times R_L)$$
$$E_B = E_g + (I_p \times R_L)$$
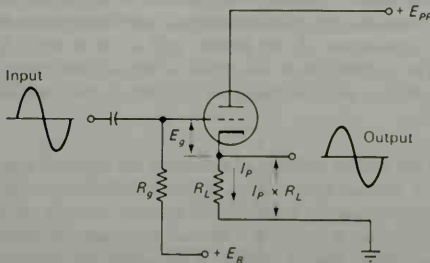
Figure 20-14. Common plate amplifier or cathode follower.

If $R_L = 10$ kΩ, $E_{PP} = 200$ V, and the tube has the characteristics shown in Fig. 20-11, a dc load line can be drawn exactly as for the common cathode circuit. From point Q on the load line,

$$E_g = -2 \text{ V} \quad \text{and} \quad I_p = 9.5 \text{ mA}$$
$$E_B = -2 \text{ V} + (9.5 \text{ mA} \times 10 \text{ kΩ})$$
$$= +93 \text{ V}$$

To achieve the bias conditions at point Q, the grid bias voltge must be $+93$ V. This is a major change from the negative grid bias voltages required with common cathode circuits. Note that the grid is still negative with respect to the cathode.

Now consider the signal required to produce a ± 40 V output. A $+40$ V change across the 10 kΩ load resistance requires a $+4$ mA change in I_p.

I_p becomes $(9.5 \text{ mA} + 4 \text{ mA}) = 13.5$ mA, and to achieve this E_g becomes 0 V (Fig. 20-11).

Now, $I_p \times R_L = 13.5$ mA × 10 kΩ = 135 V, and (bias voltage) + (signal voltage) = $E_B + E_s$, where $(E_B + E_s) = E_g + (I_p \times R_L)$. Since $E_B = +93$ V, the signal voltage is $E_s = 135 - 93$ V = 42 V. Therefore, an output change of $+40$ V requires a signal input of $+42$ V. Similarly, it can be shown that an input of -42 V will produce an output of -40 V. Thus, the common plate circuit has a voltage gain approximately equal to one, and the output is in phase with the signal input. It can also be shown that this circuit has a high input resistance and a very low output resistance. Like the transistor common collector circuit, the common plate circuit (or *cathode follower*) is normally used as a *buffer amplifier*; i.e., it is connected between a low impedance load and a high impedance signal source.

20-9
Common
Grid
Circuit

This is the vacuum-tube equivalent of the transistor common base circuit (Fig. 20-15). Since the input signal is applied to the cathode, the input voltage must supply the plate current changes, and so the circuit has a low input resistance. However, the signal is developed directly across grid and cathode, so a voltage gain is achieved. Like its transistor equivalent, the only major application of the *common grid circuit* is as a high-frequency amplifier. The application of the signal to the cathode means that the grid can be grounded to avoid feedback via the plate-to-grid capacitance.

20-10
Triode
Biasing
Methods

There are several methods of obtaining the required negative grid bias voltage for a vacuum-tube circuit. Figure 20-10 shows that if a suitable negative supply voltage is available the cathode may be grounded and the grid connected via R_g to $-E_b$. By far the most convenient and most frequently employed biasing method is the *cathode bias* technique illustrated on Fig. 20-16. The negative grid voltage is provided by the voltage drop $I_p \times R_k$. Since the grounded end of R_k is negative with respect to the cathode,
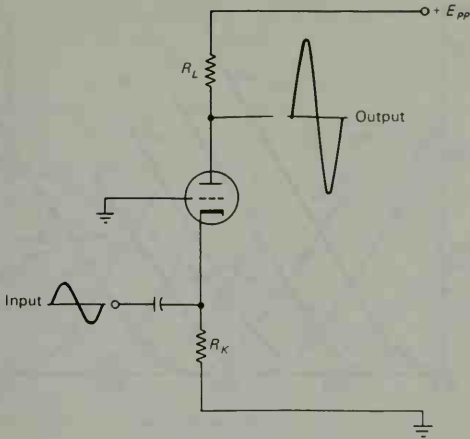
Figure 20-15. Common grid amplifier.

the grid (which is grounded via R_g) is also negative with respect to the cathode. To obtain maximum ac gain, R_k is bypassed by large capacitor C_1, so that R_k is short circuited to alternating current.

With the inclusion of the cathode resistance R_k in the circuit, the total dc load in series with the vacuum tube becomes $(R_L + R_k)$. The dc load line must be drawn for $(R_L + R_k)$. If R_k has a bypass capacitor, the ac load is R_L. The bias point on the dc load line can be determined by drawing a *bias line*.

A common cathode amplifier has $R_L = 9.7$ kΩ, $R_k = 270$ Ω, and $E_{PP} = 200$ V. The triode employed has the plate characteristics shown in Fig. 20-11, and R_k is ac bypassed by a large capacitor. Draw the dc load line and

Example 20-4
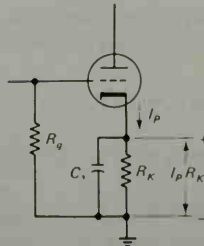
Figure 20-16. Cathode bias or self-bias.
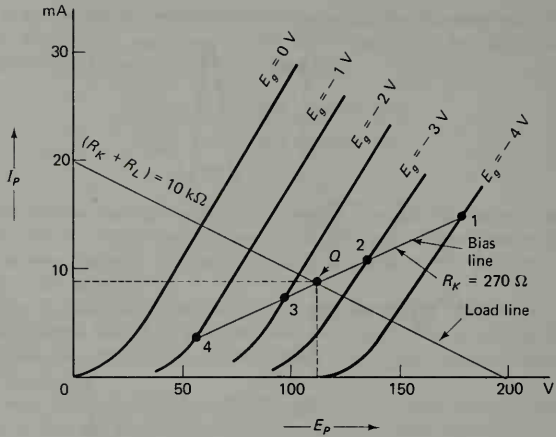
Figure 20-17. Determining Q point for self-biased circuit.

determine the values of E_g, I_p, and E_p. Also draw the ac load line for the circuit.

solution

Total dc load resistance $= R_L + R_k = 9.7 \text{ k}\Omega + 270 \ \Omega \approx 10 \text{ k}\Omega$

The dc load line is drawn exactly as explained in Section 20-6. The grid-to-cathode bias voltage must now be determined by plotting a bias line, as shown in Fig. 20-17. With self-bias,

$$E_g = I_p \times R_k$$

$$I_p = \frac{E_g}{R_k}$$

When $E_g = -4$ V, $I_p = 4 \text{ V}/270 \ \Omega = 14.8 \text{ mA}$.
Plot point 1 on the characteristics at $E_g = -4$ V, $I_p = 14.8$ mA (Fig. 20-17).

$$\text{When } E_g = -3 \text{ V}, \quad I_p = \frac{3 \text{ V}}{270 \ \Omega} = 11.1 \text{ mA} \qquad \text{(point 2)}$$

$$\text{When } E_g = -2 \text{ V}, \quad I_p = \frac{2 \text{ V}}{270 \ \Omega} = 7.4 \text{ mA} \qquad \text{(point 3)}$$

$$\text{When } E_g = -1 \text{ V}, \quad I_p = \frac{1 \text{ V}}{270 \ \Omega} = 3.7 \text{ mA} \qquad \text{(point 4)}$$

Now draw the bias line for $R_k = 270 \ \Omega$ through points 1, 2, 3, and 4.
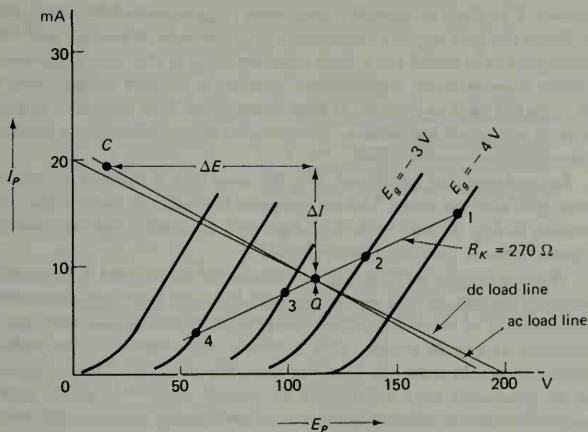
Figure 20-18. AC load line for self-biased circuit.

The bias line intersects the dc load line at point Q, giving $E_g \approx -2.4$ V, $I_p \approx 8.8$ mA, and $E_p = 112$ V. Note that E_p is the tube *plate-to-cathode voltage*. The voltage from ground to plate is $(E_p + I_p R_k)$. Since R_k is bypassed to alternating current, the ac load $= R_L = 9.7$ kΩ.

One point on the ac load line is point Q. When an ac signal causes I_p to change by ΔI_p, E_p will change by $-\Delta I_p \times R_L$.

Let $\Delta I_p = 10$ mA.

$$E_p = -10 \text{ mA} \times 9.7 \text{ k}\Omega = -97 \text{ V}$$

On Fig. 20-18, plot point C on the characteristic by measuring $\Delta I_p = 10$ mA and $\Delta E_p = -97$ V from the Q point.

Draw the ac load line through points C and Q. It is seen that, because the value of ac load is close to the dc load value, the ac and dc load lines are not very different from each other. This is not the case where (ac R_L) $\ll$ (dc R_L).

20-11
The Tetrode Tube

Interelectrode capacitance in a vacuum triode limits the high-frequency performance of the device. The grid-to-cathode capacitance (C_{gk}) appears in parallel with the tube input and is referred to as the *input*

20-11.1
Theory of Operation

capacitance. The plate-to-cathode capacitance (C_{pk}) is termed the *output capaci-tance.* Since the grid-to-plate capacitance (C_{gp}) provides a leakage path from plate to grid, it is called the *leakage capacitance.* C_{gp} is the most important of the three interelectrode capacitances because it permits signals from the plate to be fed back to the grid at high frequencies. This can result in loss of gain or in unwanted oscillations. To eliminate the high-frequency feedback, the tetrode tube was developed.

In the tetrode an additional grid, the *screen grid*, is inserted between the control grid and the plate. The construction is similar to that of the triode illustrated in Fig. 20-5(a), with the screen grid as another fine wire spiral in the space between plate and control grid.

When a tetrode is connected in a circuit the screen grid is grounded to alternating current, so that signals fed back from the plate are channeled to ground instead of reaching the control grid. The screen grid must also be maintained at a high positive (dc) potential with respect to the cathode; otherwise, it would repel the electrons from the cathode. A large capacitor must be connected from screen grid to ground to provide an ac path to ground. The tetrode circuit symbol and the biasing arrangement for the screen grid are shown in Fig. 20-19.

20-11.2
Characteristics
of the
Tetrode

Since the screen grid is held at a fixed high positive potential, it behaves as another plate and collects a portion of the total electron flow from the cathode. The plate collects the remaining portion of the cathode current. The cathode current remains constant, being determined by E_B and R_k. Therefore, $I_k = I_p + I_{sg}$ (see Fig. 20-19).

Consider the plate characteristic for $E_g = 0$ and the screen grid char-acteristic in Fig. 20-20. When the plate voltage is zero, no plate current
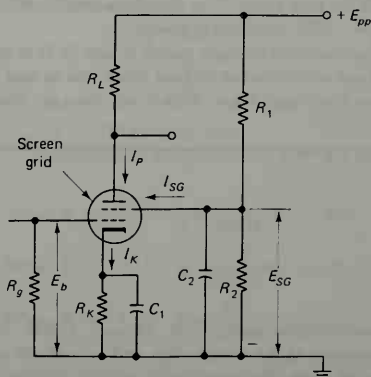
Figure 20-19. Tetrode biasing arrangement.
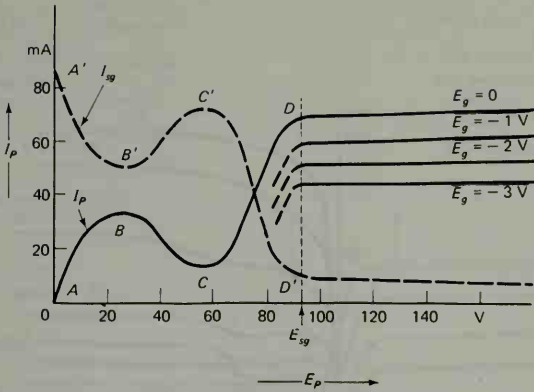
Figure 20-20. Typical tetrode plate characteristics and screen grid characteristic.

flows. Therefore,

$$I_p = 0 \quad \text{and} \quad I_k = 0 + I_{sg}$$

At this time all the cathode current flows via the screen grid. As E_p is increased from zero, I_p increases and consequently I_{sg} decreases. At points B and B', $I_p \approx 35$ mA and $I_{sg} \approx 50$ mA. The cathode current is then $I_k \approx 85$ mA.

When the plate voltage exceeds that at point B, electrons accelerated through the screen grid to the plate strike the plate with sufficient force to cause *secondary emission*. Since the screen grid is more positive than the plate, the secondary electrons are attracted from the plate to the screen grid. This constitutes a decrease in I_p and an increase in I_{sg}, giving parts B to C and parts B' to C' of the characteristics.

As the plate continues to be made more positive, the secondary electrons begin to be attracted back to the plate. I_{sg} now decreases and I_p increases again with E_p increase, giving parts C to D and parts C' to D' of the characteristic. Beyond points D and D', E_p is greater than E_{sg}; therefore, the plate is collecting most of the electrons flowing from the cathode.

The *kink* in the tetrode characteristics is a distinct disadvantage, because only the linear portion (beyond point D) of the characteristics is usable. Several methods have been devised to eliminate the kink. One approach resulted in the *beam tetrode*, which has the circuit symbol and typical characteristics shown in Fig. 20-21. In the beam tetrode, the electrons flowing to the plate are concentrated in dense channels by the negative potential on *beam-forming plates* located between the screen grid and the plate. The result is that secondary emitted electrons are swept back to the plate by the dense channel of electrons flowing toward the plate, and thus the kink is largely eliminated from the characteristic.
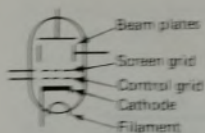
(a) Beam tetrode symbol
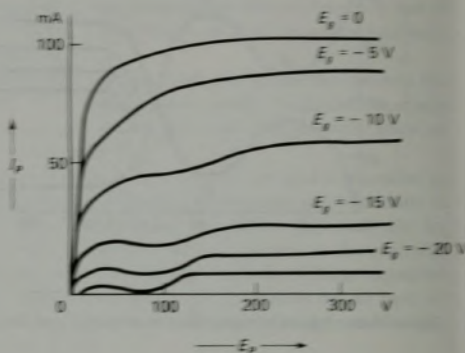
(b) Beam tetrode
characteristics

Figure 20-21. Beam tetrode circuit symbol and characteristics.

20-12
The
Pentode

20-12.1
Theory
of
Operation

Another way of eliminating the secondary emission effects that occur in a tetrode is to introduce a third grid into the tube, making the device into a *pentode*. The third grid, known as the *suppressor grid*, is located between the screen grid and the plate as shown in Fig. 20-22(a). When held at ground potential, the suppressor grid introduces a large negative barrier potential which secondary emitted electrons must cross if they are to travel from the plate back to the screen grid. The suppressor grid has very little effect upon the primary electrons which constitute the plate current. This is because the primary electrons are accelerated to a high velocity as they travel from the cathode. The secondary electrons, however, have low velocity and cannot cross the negative potential barrier set up by the suppressor grid. Secondary emission effects are eliminated, and the pentode characteristics have the wide useful operating range shown in Fig. 20-22(b).

As in the case of the tetrode and beam tetrode, the plate current in a pentode is only slightly affected by plate voltage, i.e., in the useful portion of the characteristics. Consequently, plate resistance (r_p) and amplification factor (μ) are very large by comparison with a triode tube. The transcon-
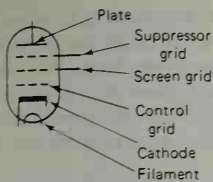
(a) Pentode circuit symbol
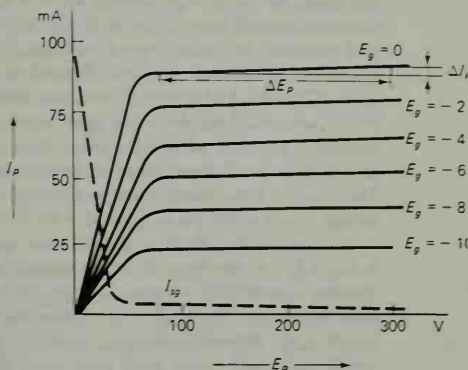
(b) Pentode characteristics

Figure 20-22. Pentode circuit symbol and characteristics.

ductance (g_m) of a pentode remains similar to that of a triode, because the control grid in each case is located close to the cathode. From Fig. 20-22,

$$r_p = \frac{\Delta E_p}{\Delta I_p} \approx \frac{225 \text{ V}}{3 \text{ mA}} = 75 \text{ k}\Omega$$

Typically, r_p is around 1.5 MΩ. Values of 3000 to 10,000 are typical for μ, while g_m remains on the order of 1 to 10 mA/V, as in a triode.

The negative bias for the control grid of a pentode may be obtained by any of the methods employed for a triode. The positive bias for the screen grid is usually provided by the potential divider technique shown in Fig. 20-23. A large capacitor (C_3) must be included to give the potential divider a low output impedance. The suppressor grid is usually connected directly to either the cathode or ground.

20-1?
Pent?
Biasi

20-13
The
Variable-Mu
or Remote
Cutoff
Pentode

The transconductance characteristics for a *sharp cutoff* (i.e., normal) pentode and for a *remote cutoff* pentode are shown in Fig. 20-24. For the sharp cutoff pentode the characteristics are almost completely linear. Also, the plate current is cut off (i.e., goes to zero) at small values of E_g [-11 and -15 V in Fig. 20-24(a)]. For the remote cutoff tube the transconductance characteristics are quite curved, and E_g must go to a large negative level to achieve I_p cutoff.

In a normal pentode, the control grid wires are evenly spaced along the length of the cathode, as they are in a triode (Fig. 20-5). Consequently, electrons emitted from all parts of the cathode are equally affected by the grid potential. In a remote cutoff pentode, the grid wires are either unevenly spaced, or the cathode ends are allowed to project beyond the ends of the grid. With this arrangement, electrons emitted from those cathode areas which are relatively far from grid wires are less affected by the grid potential. To repel electrons emitted from these (farther away) areas, the grid must be made much more negative than it would otherwise need to be. The result is a nonlinear transconductance characteristic and a cutoff grid voltage which might be as large as -60 V.

Consider Fig. 20-24(a) and (b) once again. The transconductance (g_m) is $\Delta I_p / \Delta E_g$, i.e., the slope of the characteristic. For the sharp cutoff device g_m remains substantially constant, but for the remote cutoff tube g_m decreases with increasing values of $-E_g$. Since the tube amplification factor (μ) equals $g_m r_p$, the variation in g_m produces a variation in μ. Therefore, a *variable-mu pentode* circuit has a gain which varies according to the grid bias. This allows specialized applications such as *automatic gain control*.
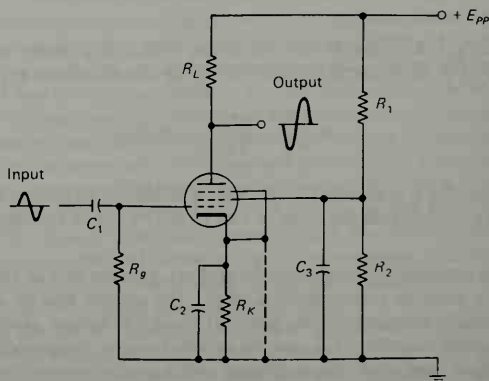
Figure 20-23. Pentode amplifier circuit showing biasing technique for each electrode.

462
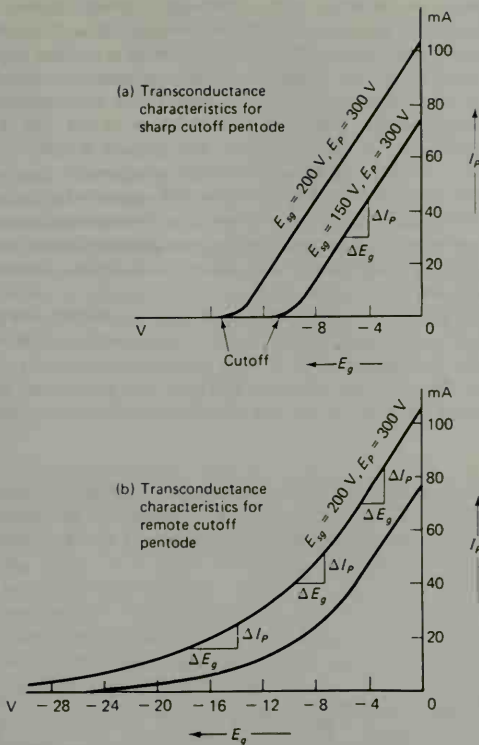
Figure 20-24. Transconductance characteristics for sharp cutoff and remote cutoff pentodes.

20-14
The
Cathode-Ray
Tube

20-14.1
General

The basic construction and biasing of a cathode-ray tube are shown in Fig. 20-25. The system of electrodes is contained in an evacuated glass tube with a viewing screen at one end. A beam of electrons is generated by the cathode and directed to the screen, causing the phosphor coating on the screen to glow where the electrons strike. The electron beam is deflected vertically and horizontally by externally applied voltages.

The triode section of the tube consists of a cathode, a grid, and an anode, which are all substantially different in construction from the usual electrodes in a triode vacuum tube. The grid, which is a nickel cup with a hole in it (see Fig. 20-25), almost completely encloses the cathode. The cathode, also made of nickel, is cylinder shaped with a flat, oxide-coated, electron-emitting surface directed toward the hole in the grid. Cathode heating is provided by an inside filament. The cathode is typically held at approximately -2 kV, and the grid potential is adjustable from approximately -2000 to -2050 V. The grid potential controls the electron flow from the cathode, and thus controls the number of electrons directed to the screen. A large number of electrons striking one point will cause the screen to glow brightly; a small number will produce a dim glow. Therefore, the grid potential control is a *brightness control*.

The first anode (A_1) is cylinder shaped, open at one end, and closed at the other end with a hole at the center of the closed end. Since A_1 is grounded and the cathode is at a high negative potential, A_1 is highly positive with respect to the cathode. Electrons are accelerated from the cathode through the holes in the grid and anode to the focusing section of the tube.

The focusing electrodes A_1, A_2, and A_3 are sometimes referred to as an *electron lens*. Their function is to focus the electrons to a fine point at the screen of the tube. A_1 provides the accelerating field to draw the electrons
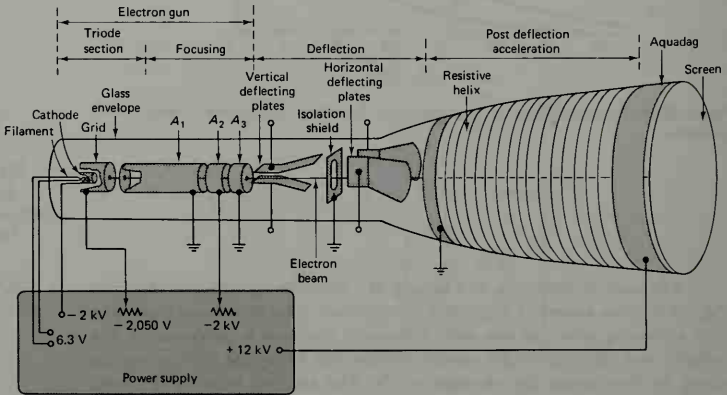
Figure 20-25. Basic construction and biasing of cathode-ray tube.

from the cathode, and the hole in A_1 limits the initial cross section of the electron beam. A_3 and A_1 are held at ground potential while the A_2 potential is adjustable around -2 kV. The result of the potential difference between anodes is that *equipotential lines* are set up as shown in Fig. 20-26. These are lines along which the potential is constant. Line 1, for example, might have a potential of -700 V along its entire length, while the potential of line 2 might be -500 V over its whole length. The electrons enter A_1 as a divergent beam. On crossing the equipotential lines, however, the electrons experience a force which changes their direction of travel toward right angles with respect to the equipotential lines. The shape of the lines within A_1 produces a convergent force on the divergent beam, and those within A_3 produce a divergent force on the beam. The convergent and divergent forces can be altered by adjusting the potential on A_2. This adjusts the point at which the beam is focused. A_2 is sometimes referred to as the *focus ring*.

The negative potential on A_2 tends to slow down the electrons, but they are accelerated again by A_3, so that the beam speed leaving A_3 is the same as when entering A_1. The electrons are traveling at a constant velocity as they pass between the deflecting plates.

Consider the electrostatic deflection illustration in Fig. 20-27. When the potential on each plate is zero, the electrons passing between the plates do not experience any deflecting force. When the upper plate potential is $+E/2$ volts and the lower potential is $-E/2$, the potential difference between the plates is E volts. The (negatively charged) electrons are attracted toward the positive plate and repelled from the negative plate. The electrons are actually accelerated in the direction of the positive plate. However, since they also have a horizontal velocity, the electrons normally never strike a deflecting plate. Instead, the beam is deflected and the electrons strike the screen at a new position.
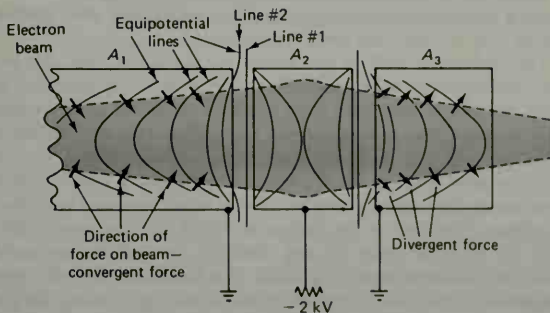
Figure 20-26. Electrostatic focusing.
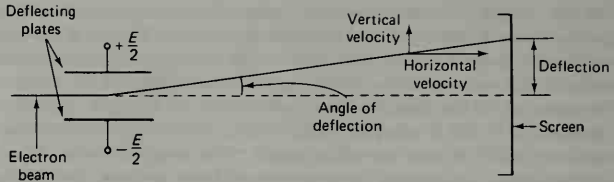
Figure 20-27. Electrostatic deflection.

The beam could be deflected by grounding one plate and applying a positive or negative potential to the other plate. In this case, the potential at the center of the space between the plates would be greater or less than zero volts. This would cause horizontal acceleration or deceleration of the electrons, thus altering the beam speed. Equal positive and negative deflecting voltages would then *not* produce equal deflections. With $+E/2$ volts on one plate and $-E/2$ on the other plate, the center potential in the space between plates is zero volts, and the beam speed is unaffected. The tube sensitivity to deflecting voltages can be expressed in two ways. The voltage required to produce one division of deflection at the screen (V/cm) is referred to as the *deflection factor* of the tube. The deflection produced by one V (cm/V) is termed the *deflection sensitivity*.

The *isolation shield* shown in Fig. 20-25 is designed to keep the deflecting plates isolated from each other's electric fields.

<p style="margin-left:2em">**20-14.5**
The
Screen</p>

The screen of a cathode-ray tube is formed by placing a coating of phosphor materials on the inside of the tube face. When the electron beam strikes the screen, electrons within the screen material are raised to a higher energy level and emit light as they return to their normal levels. The glow may persist for a few milliseconds, for several seconds, or even longer. Depending upon the materials employed, the color of the glow produced at the screen may be blue, red, green, or white.

The phosphors used on the screen are insulators, and, but for secondary emission, the screen would develop a negative potential as the primary electrons accumulate. The negative potential would eventually become so great that it would repel the electron beam. The secondary electrons are collected by a graphite coating termed *aquadag*, around the neck of the tube (see Fig. 20-25), so that the negative potential does not accumulate on the screen. In another type of tube, the screen has a fine film of aluminum deposited on the surface at which the electrons strike. This permits the electron beam to pass through, but collects the secondary electrons and conducts them to ground. The aluminum film also improves the brightness of the glow by reflecting the emitted light toward the glass. A further advantage of the film is that it acts as a heat sink, conducting away heat that might otherwise damage the screen.

As has already been explained, the brightness of the glow produced at the screen is dependent upon the number of electrons making up the beam. Since the grid controls the electron emission from the cathode, the grid voltage control is a brightness control. Brightness also depends upon beam speed; so for maximum brightness the electrons should be accelerated to the greatest possible velocity. However, if the electron velocity is very high when passing through the deflection plates, the deflecting voltages will have a reduced influence, and the deflection sensitivity will be poor. It is for this reason that *postdeflection acceleration* is provided; i.e., the electrons are accelerated again after they pass between the deflecting plates. A helix of resistive material is deposited on the inside of the tube from the deflecting plates to the screen (Fig. 20-25). The potential at the screen end of the helix might be typically +12 kV and at the other end 0 kV. Thus, the electrons leaving the deflecting plates experience a continuous accelerating force all the way to the screen, where they strike with high energy.

When an alternating voltage is applied to the vertical deflecting plates and no input is applied to the horizontal plates, the spot on the tube face will move up and down continuously. If a constantly increasing voltage is also applied to the horizontal deflecting plates, then, as well as moving vertically, the spot on the tube face will move horizontally. Consider Fig. 20-28, in which a sine wave is applied to a vertical deflecting plate and a *sawtooth* is applied to the horizontal plates. If the waveforms are perfectly synchronized, then at time $t = 0$ the vertical deflecting voltage is zero and the horizontal deflecting voltage is -2 V. Therefore, assuming a deflection sensitivity of 2 cm/V, the vertical deflection is zero and the horizontal deflection is 4 cm left from the center of the screen [point 1 on Fig. 20-28(c)]. When $t = 0.5$ ms, the horizontal deflecting voltage has become -1.5 V; therefore, the horizontal deflection is 3 cm left from the screen center. The vertical deflecting voltage has now become $+1.4$ V, and causes a vertical deflection of $+2.8$ cm above the center of the screen. The spot is now 2.8 cm up and 3 cm left from the screen center (point 2). The following is a table of data for other times.

At t	Horizontal	Vertical	Point
1 ms	-1 V	$+2$ V	3
1.5 ms	-0.5 V	$+1.4$ V	Point 4
2 ms	0 V	0 V	Center of screen.
2.5 ms	$+0.5$ V	-1.4 V	Point 6
3 ms	$+1$ V	-2 V	Point 7
3.5 ms	$+1.5$ V	-1.4 V	Point 8
4 ms	$+2$ V	-0 V	Point 9

At point 9 the horizontal deflecting voltage rapidly goes to -2 V again, so the beam returns to the left side of the screen. From here it is ready
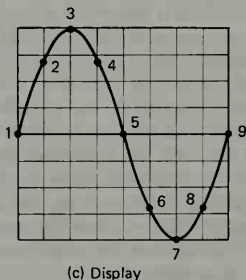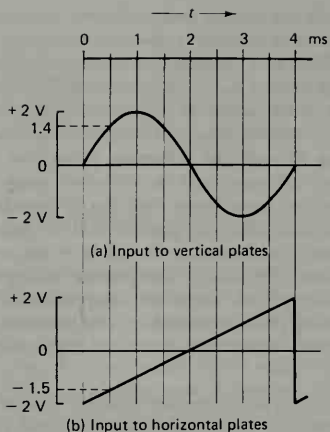
Figure 20-28. Waveform display on cathode-ray tube.

to repeat the waveform trace over again. It is seen that, with a sawtooth applied to the horizontal deflecting plates, any waveform applied to the vertical plates will be displayed on the screen of the cathode-ray tube.

Example 20-5   A 500-Hz triangular wave with a peak amplitude of ±40 V is applied to the vertical deflecting plates of a CRT. A 250 Hz sawtooth wave with a peak amplitude of ±50 V is applied to the horizontal deflecting plates. The CRT has a vertical deflection sensitivity of 0.1 cm/V and a horizontal deflection sensitivity of 0.08 cm/V. Assuming that the two inputs are synchronized, determine the waveform displayed on the screen.

For a triangular wave,

$$T = \frac{1}{f} = \frac{1}{500 \text{ Hz}} = 2 \text{ ms}$$

For a sawtooth wave,

$$T = \frac{1}{250 \text{ Hz}} = 4 \text{ ms}$$

The two waveforms are shown in Fig. 20-29(a) and (b).

at t = 0

Vertical voltage $= 0$

Horizontal voltage $= -50$ V

Horizontal deflection $=$ (voltage) $\times$ (deflection sensitivity)

$= -50 \times 0.08$ cm

$= -4$ cm (i.e., 4 cm left from center)

Point 1 on the CRT screen [Fig. 20-29(c)] is at

Vertical deflection $= 0$

Horizontal deflection $= 4$ cm left of center

at t = 0.5 ms

Vertical voltage $= +40$ V

Horizontal voltage $= -37.5$ V

Therefore, at point 2 on the CRT screen,

Vertical deflection $= +40 \times 0.1$ cm $= +4$ cm

Horizontal deflection $= -37.5 \times 0.08$ cm $= -3$ cm

at t = 1 ms (point 3)

Vertical deflection $= 0$

Horizontal deflection $= -25 \times 0.08$ cm $= -2$ cm

at t = 1.5 ms (point 4)

Vertical deflection $= -40 \times 0.1$ cm $= -4$ cm

Horizontal deflection $= -12.5 \times 0.08$ cm $= -1$ cm
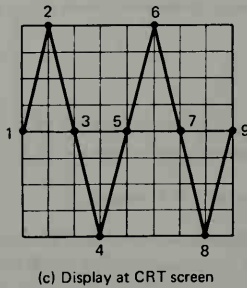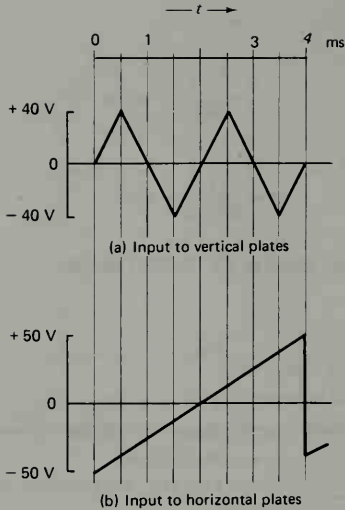
Figure 20-29. Waveforms and display for Example 20-5.

at $t = 2$ *ms* (point 5)

Vertical deflection = 0

Horizontal deflection = 0

t(ms)	2.5	3	3.5	4
Vertical voltage	+ 40 V	0	− 40 V	0
Vertical deflection	+ 40 cm	0	− 4 cm	0

Horizontal voltage	+ 12.4 V	+ 25 V	+ 37.5 V	+ 50 V
Horizontal deflection	+ 1 cm	+ 2 cm	+ 3 cm	+ 4 cm
Point	6	7	8	9

The triode section and focusing section of the tube are together referred to as an *electron gun*. A double-beam tube normally has two *electron guns* used to generate two separate beams. Two separate sets of vertical and horizontal deflecting plates are included. Both beams are made to sweep across the screen together so that the time and phase relationships of separate waveforms can be compared.

Vacuum diode. Two-electrode vacuum tube, contains plate and cathode.

Cathode. Negative terminal of vacuum tube—emits electrons when heated.

Plate. Positive terminal of vacuum tube—collects electrons from cathode.

Anode. Same as *plate*.

Filament. Cathode, or heater for indirectly heated cathode.

Tungsten. Element used in filaments.

Thoriated tungsten. Alloy of tungsten and thorium, used for filament-type cathodes.

Barium oxide. Electron-emitting oxide used on the surface of indirectly heated cathodes.

Plate voltage, E_p. Voltage at plate, or voltage measured from cathode to plate.

Plate current, I_p. Electrons flowing from cathode to plate—conventional direction current from plate to cathode.

Plate characteristics. Graph of I_p values plotted against corresponding values of E_p, for various constant values of grid voltage.

Space-charge limited region. Region of diode plate characteristics during which space charge exists–region in which device is operated.

Temperature-limited region. Region of diode plate characteristics in which all electrons emitted from the cathode are drawn to plate.

Vacuum triode. Three-electrode tube; contains plate, cathode, and grid.

Grid. Wire spiral surrounding the cathode, used to control the plate current.

Transconductance, g_m. Ratio of change in plate current to grid voltage change.

Transconductance characteristic. Graph of I_p values plotted against corresponding grid voltage E_g values, with E_p constant.

Constant current characteristics. Graph of E_p values plotted against corresponding E_g values, with I_p constant.

Plate resistance, r_p. Reciprocal of the slope of plate characteristics—$(\Delta E_p/\Delta I_p)$ ohms.

Amplification factor, μ. Ratio of plate voltage change for a given value of ΔI_p to grid voltage change for same ΔI_p.

Common cathode circuit. Vacuum triode circuit in which input signal is applied between grid and cathode, and output is taken between plate and cathode.

Common plate circuit. Vacuum triode circuit in which input signal is applied between grid and plate, and output is taken between cathode and plate.

Cathode follower. Same as *common plate circuit*.

Common grid circuit. Vacuum triode circuit in which input signal is applied between cathode and grid, and output is taken between plate and grid.

Grid leak. Resistance used to connect grid to bias voltage and to "leak" electrons off the grid.

Cathode bias. Biasing technique using a resistance in series with the cathode.

Self-bias. Same as *cathode bias*.

Leakage capacitance. Plate-to-grid capacitance.

Input capacitance. Grid-to-cathode capacitance.

Output capacitance. Plate-to-cathode capacitance.

Tetrode. Four-electrode tube containing plate, screen grid, control grid, and cathode.

Screen grid. Grid employed to screen the control grid from the effects of plate voltage changes.

Beam tetrode. Tetrode with beam-forming plates to eliminate secondary emission.

Pentode. Five-electrode tube containing plate, suppressor grid, screen grid, control grid, and cathode.

Suppressor grid. Grid employed to suppress secondary emission.

Variable-mu pentode. Pentode in which the transconductance g_m varies according to grid bias voltage. Also requires large negative grid voltage to cut off plate current.

Remote cutoff pentode. Same as *variable-mu pentode*.

Sharp cutoff pentode. Ordinary pentode (i.e., not variable-mu)—requires relatively small negative grid voltage to cut off plate current.

Cathode-ray tube (CRT). Electron tube in which electrons are concentrated into a beam (or ray) which is directed to a display screen.

Electron gun. Cathode, grid, accelerating, and focusing electrodes in cathode-ray tube.

Electron beam. Stream or ray of electrons in a cathode-ray tube.

Brightness control. Voltage control on the grid of a cathode-ray tube.

Focusing system. CRT electrodes which focus the electron beam to a point at the screen of a cathode-ray tube.

Electron lens. Same as *focusing system*.

Equipotential lines. Lines in space between electrodes having a constant potential along their length.

Focus ring. Cylindrical electrode on which the potential is varied to obtain focus of electron beam in CRT.

Vertical deflecting plates. CRT electrodes which deflect the electron beam vertically when a deflecting voltage is applied.

Horizontal deflecting plates. CRT electrodes which deflect the electron beam horizontally when a deflecting voltage is applied.

Isolation shield. Metal plate inserted between CRT horizontal and vertical deflecting plates to isolate their electric fields.

Deflection factor. Voltage required to produce one division of deflection at screen of CRT (V/cm).

Deflection sensitivity. Divisions of deflection at screen of CRT produced by 1 V at deflecting plates (cm/V).

Screen. Flat portion of CRT glass envelope, has inside coating of phosphor materials which glow when struck by electrons.

Aquadag. Graphite coating inside the neck of CRT, collects secondary emitted electrons.

Postdeflection acceleration (PDA). Arrangement to accelerate CRT electron beam after it has been deflected.

Resistive helix. Film of resistive material deposited as helix around the neck of a CRT to facilitate postdeflection acceleration.

Double-beam CRT. CRT with two electrode systems generating separate electron beams.

20-1. Draw sketches to show the circuit symbol and mechanical construction of a vacuum diode. Name each part of the device and briefly explain how it operates.

20-2. (a) Describe the construction of two types of thermionic cathode. State the advantages and disadvantages of each. (b) List the materials used for plates in low-power and high-power vacuum tubes.

20-3. Sketch typical (plate voltage)/(plate current) characteristics for a vacuum diode. Label each region of the characteristics, explain their shape, and show the effects of temperature increase.

20-4. Draw sketches to show the symbol and mechanical construction of a triode vacuum tube. Name each electrode and state its function.

20-5. Sketch typical plate characteristics for a vacuum triode for several

values of negative grid voltage. Also show the effect of positive grid voltage.

20-6. Sketch a practical circuit diagram for
(a) A vacuum triode common cathode amplifier.
(b) A vacuum triode common plate amplifier.
(c) A vacuum triode common grid amplifier.
Indicate supply voltage polarities, current directions, input, and output terminals.

20-7. Draw an ac equivalent circuit for a common cathode amplifier. Draw the voltage equivalent circuit (from the ac equivalent circuit) and derive expressions for voltage gain and output resistance. Also state the input resistance.

20-8. State typical applications for common cathode, common plate, and common grid amplifiers. Explain each application in terms of voltage gain, input and output resistance, etc.

20-9. State the function of, and typical maximum value for, a grid leak resistor. Briefly explain the possible effects of making the grid leak resistor too large.

20-10. Draw sketches to show how the grid of a vacuum triode may be biased to a desired voltage by cathode bias (or self-bias).

20-11. Draw a sketch to show the various capacitances that exist within a triode vacuum tube. Name each of these capacitances, state which is most important, and explain why.

20-12. Explain how the tetrode vacuum tube combats the effects of inter-electrode capacitance. Sketch the circuit symbol for a tetrode and name each electrode and state its function.

20-13. Sketch one plate characteristic and one screen grid characteristic for a tetrode vacuum tube. Carefully explain the shape of the characteristics.

20-14. Explain the origin and operation of a beam tetrode. Sketch the circuit symbol and a typical family of plate characteristics for this device.

20-15. Explain the origin of the pentode vacuum tube. Sketch a typical family of plate characteristics and the circuit symbol for the device.

20-16. State typical values for μ, g_m, and r_p for a pentode. Briefly explain.

20-17. Draw a circuit diagram of a pentode common cathode amplifier with self-bias. Explain the bias arrangements for each electrode.

20-18. Sketch typical transconductance characteristics for (a) a sharp cutoff pentode, (b) a variable-mu pentode. Explain the characteristics, and discuss the mechanical differences between the tubes. State a typical application for a variable-mu tube.

20-19. Sketch the electron-gun section of a cathode-ray tube. Identify each electrode and its function; also indicate typical voltages.

20-20. Draw a sketch to show how an electron lens functions. Briefly explain.

20-21. Sketch the deflection system of a cathode-ray tube and explain how it operates.

20-22. Describe the screen of a cathode-ray tube. Explain the function of the aquadag, and describe another method of performing the function.

20-23. Define *postdeflection acceleration*. Explain why PDA is required and how it is achieved.

Problems

20-1. A vacuum diode with plate characteristics as shown in Fig. 20-3 is connected in series with a load resistance of 3.3 kΩ and a supply of 90 V. Draw the dc load line and determine the values of I_p and E_p.

20-2. A vacuum diode with a series load of 2 kΩ has an I_p of 18 mA. If the plate characteristic for the diode is as shown in Fig. 20-3, draw the dc load line and determine the supply voltage.

20-3. From the triode plate characteristics in Fig. 20-30 derive (a) the transconductance characteristic for $E_p = 80$ V; (b) the constant current characteristic for $I_p = 4$ mA.

20-4. From the plate characteristics in Fig. 20-30 derive r_p, g_m, and μ at $E_p = 60$ V, $E_g = -1$ V.

20-5. A triode used in a common cathode amplifier has the plate characteristics of Fig. 20-30. Supply voltage is 120 V, load resistance is 12 kΩ, and grid bias is -2 V. Draw the dc load line and determine plate current and voltage. Also calculate the output impedance and voltage gain of the amplifier.
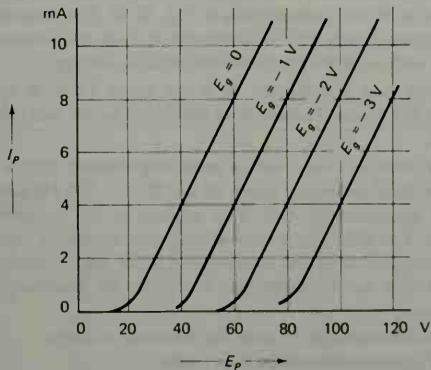
Figure 20-30. Triode plate characteristics for Problems 20-3 through 20-6.

20-6. A common cathode amplifier has $R_L = 13$ kΩ, $R_k = 2$ kΩ, and $E_{PP} = 100$ V. The triode employed has the plate characteristics of Fig. 20-30, and R_k is ac bypassed by a large capacitor. Draw the dc load line and determine the values of E_g, I_p, and E_p. Also draw the ac load line for the circuit.

20-7. A common cathode amplifier uses a triode with the characteristics shown in Fig. 20-11. The supply voltage is $E_{pp} = 150$ V, and the plate voltage is to be $E_p = 100$ V when $E_g = -2$ V. Draw the dc load line; determine the value of R_L and calculate A_v.

20-8. The circuit in Problem 20-7 is to use the cathode bias technique. Determine a suitable value for R_k. Assuming R_k is bypassed by a large capacitor, draw the ac load line for the circuit. Taking $R_g = 100$ kΩ, calculate the input and output impedance of the circuit.

20-9. A common plate circuit with $R_L = 9$ kΩ has a vacuum triode with the characteristics shown in Fig. 20-17. The supply voltage is $E_{pp} = 180$ V, and the cathode voltage is to be $E_k = 80$ V. Draw the dc load line for the circuit and determine the level of I_p. Also calculate the required grid bias voltage level.

20-10. A pentode tube in a common cathode amplifier has the characteristics shown in Fig. 20-22. The supply voltage is $E_{pp} = 300$ V, and E_p is to be 150 V when $I_p = 50$ mA. Draw the dc load line and determine the required value of E_g.

20-11. For the circuit in Problem 20-10 determine a suitable value of cathode resistor R_k to give the required grid bias voltage. Assuming R_k is bypassed by a large capacitor, calculate the circuit voltage gain and output impedance.

20-12. A pentode common plate circuit with $R_L = 4$ kΩ and $E_{pp} = 300$ V uses a tube with the characteristics in Fig. 20-22. The cathode voltage is to be approximately 160 V. Draw the dc load line, determine the level of I_p, and calculate the required grid bias voltage.

20-13. A CRT has a deflection of 5 cm when 75 V is applied to the deflecting plates. Calculate its deflection factor and deflection sensitivity.

20-14. A 1 kHz square wave with a peak amplitude of ± 25 V is applied to the vertical deflecting plates of a CRT. A 500 Hz sawtooth with a peak amplitude of ± 40 V is applied to the horizontal deflecting plates. The CRT has a vertical deflection sensitivity of 0.1 cm/V and a horizontal deflecting sensitivity of 0.075 cm/V. Assuming that the two inputs are synchronized, determine the waveform displayed on the screen.

20-15. Repeat Problem 20-14 with the following changes:
(a) The sawtooth waveform is 1 kHz.
(b) A triangular wave is substituted in place of the square wave.
(c) The square wave is replaced by a pulse waveform with a pulse width of 250 μs and a frequency of 1 kHz.

Appendixes

Ω	Ω	Ω	kΩ	kΩ	kΩ	MΩ	MΩ
—	10	100	1	10	100	1	10
—	12	120	1.2	12	120	1.2	—
—	15	150	1.5	15	150	1.5	15
—	18	180	1.8	18	180	1.8	—
—	22	220	2.2	22	220	2.2	22
2.7	27	270	2.7	27	270	2.7	—
3.3	33	330	3.3	33	330	3.3	—
3.9	39	390	3.9	39	390	3.9	—
4.7	47	470	4.7	47	470	4.7	—
5.6	56	560	5.6	56	560	5.6	—
6.8	68	680	6.8	68	680	6.8	—
—	82	820	8.2	82	820	—	—

Appendix 2
Typical Standard Capacitor Values

pF	pF	pF	pF	µF	µF	µF	µF	µF	µF	µF
5	50	500	5000		0.05	0.5	5	50	500	5000
—	51	510	5100		—	—	—	—	—	—
—	56	560	5600		0.056	0.56	5.6	56	—	5600
—	—	—	6000		0.06	—	6	—	—	6000
—	62	620	6200		—	—	—	—	—	—
—	68	680	6800		0.068	0.68	6.8	—	—	—
—	75	750	7500		—	—	—	75	—	—
—	—	—	8000		—	—	8	80	—	—
—	82	820	8200		0.082	0.82	8.2	82	—	—
—	91	910	9100		—	—	—	—	—	—
10	100	1000		0.01	0.1	1	10	100	1000	10,000
—	110	1100		—	—	—	—	—	—	
12	120	1200		0.012	0.12	1.2	—	—	—	
—	130	1300		—	—	—	—	—	—	
15	150	1500		0.015	0.15	1.5	15	150	1500	
—	160	1600		—	—	—	—	—	—	
18	180	1800		0.018	0.18	1.8	18	180	—	
20	200	2000		0.02	0.2	2	20	200	2000	
22	220	2200		—	0.22	2.2	22	—	—	
24	240	2400		—	—	—	—	240	—	
—	250	2500		—	0.25	—	25	250	2500	
27	270	2700		0.027	0.27	2.7	27	270	—	
30	300	3000		0.03	0.3	3	30	300	3000	
33	330	3300		0.033	0.33	3.3	33	330	3300	
36	360	3600		—	—	—	—	—	—	
39	390	3900		0.039	0.39	3.9	39	—	—	
—	—	4000		0.04	—	4	—	400	—	
43	430	4300		—	—	—	—	—	—	
47	470	4700		0.047	0.47	4.7	47	—	—	

Answers to Problems

Chapter 4	4-1	2.0 mA
	4-2	0.98, 49, 5.355 mA, 0.301 mA
	4-3	2.08 mA, 2.1 mA
	4-4	12.627 mA, 61.5, 0.984, 9.66 mA
	4-5	40 μA, 2.3 mA
	4-7	3 mA, 2.9 mA
	4-8	50
	4-9	0.06×10^{-3}, 53.3
	4-10	2.7 kΩ

Chapter 5	5-1	(0.97 mA 7.7 V), (0.75 mA 6 V)
	5-2	4.5 kΩ
	5-3	(2.325 mA 5.35 V), (1.86 mA 6.28 V), (2.79 mA 4.42 V)
	5-4	± 2.3 V
	5-5	283.2 kΩ, 10 V, 0.134 V
	5-6	251.7 kΩ, 14.91 V, 10.08 V
	5-7	9.58 V, 12.5 V, 7.13 V
	5-8	248 kΩ, 4.94 kΩ, 11.67 V, 8.77 V
	5-9	6.06 V, 6.02 V, 6.008 V
	5-10	10 kΩ, 9.84 kΩ, 19 kΩ, 10.7 kΩ, 9.92 V, 10.2 V
	5-11	5.93 kΩ, 13.1 kΩ, 6.7 kΩ, 8.04 V, 7.97 V
	5-12	61, 59.3, 1.83
	5-13	1 mA, 8 V

Chapter 6	6-1	992 Ω, 3.289 kΩ, -132, 39.7, 5240
	6-2	12.96 kΩ, 3.289 kΩ, -9.08, 35.68, 324
	6-3	18.93 kΩ, 39.47 Ω, 1, 0.945, 0.945
	6-4	48.89 Ω, 3.88 kΩ, 77.22, 0.968, 74.75
	6-5	147.4 Ω, 24.44, 22.57
	6-6	1.4Ω kΩ, 8.2 kΩ, 29387, 5343, 1.59×10^8
	6-7	4029, 1211
	6-8	7.74, 5

Chapter 8	8-1	64.1°C, 155.4 mW
	8-2	8.1 kΩ
	8-3	-1.25 dB
	8-4	1.262 V
	8-5	160 kHz, 125.7 kHz
	8-6	141 pF
	8-7	2.79 pF
	8-8	938 pF, 1038 pF, 31938 pF, 938 pF
	8-9	19.13 μV
	8-10	2.4 dB
	8-11	25 V, 0.65 V to 0.85 V
	8-12	90.4, no

9-1 $R_1 = R_5 = 100$ kΩ, $R_2 = R_6 = 33$ kΩ, $R_3 = R_7 = 10$ kΩ, $R_4 = R_8 = 3.3$ kΩ, $C_2 = C_4 = 330$ μF, $C_1 = C_2 = 22$ μF

9-2 $R_1 = R_5 = 39$ kΩ, $R_2 = R_6 = 22$ kΩ, $R_3 = R_7 = 3.3$ kΩ $R_4 = R_8 = 2.2$ kΩ, $C_2 = C_4 = 180$ μF, $C_1 = C_3 = 15$ μF

9-3 $R_{B1} = R_{B2} = 560$ kΩ, $R_{L1} = R_{L2} = 5.6$ kΩ, $C_1 = C_2 = 15$ μF

9-4 $R_1 = 10$ kΩ, $R_2 = 390$ kΩ, $R_3 = 6.8$ kΩ, $R_4 = 5.6$ kΩ, $C_1 = 5.6$ μF, $C_2 = 47$ μF

9-5 $R_1 = 12$ kΩ, $R_2 = 120$ kΩ, $R_3 = 12$ kΩ, $R_4 = 4.7$ kΩ, $C_1 = 15$ μF, $C_2 = 47$ μF

9-6   12.2 V

9-7   117.5, 3 kΩ, 4.7 kΩ

9-8   5.25 V

9-9   7.9998 V

9-10 $R_1 = 1.5$ kΩ, $R_2 = 100$ kΩ, $R_3 = 1.5$ kΩ

9-11 $R_1 = 1$ kΩ, $R_2 = 120$ kΩ, $R_3 = 1$ kΩ

9-12 $R_1 = 820$ Ω, $R_2 = 180$ kΩ, $R_3 = 180$ kΩ

9-13 $R_1 = 1$ kΩ, $R_2 = 33$ kΩ, $R_3 = 1$ kΩ

9-14   Point A: (20 V, 0 mA), Point Q: (15 V, 49.7 mA), Point B: ($\Delta V = 20$ V, $\Delta I_C = 49.7$ mA)

9-15   Point Q: (40 V, 0 mA), Point B: (0 V, 66.8 mA)

9-16   Transformer: 8 W, $R_L = 12$ Ω, $R_L'' = 155$ Ω ,Transistor: 50 V, 644 mA, 4 W

9-17   18 V, 20 W, Transistors: 90 V, 900 mA, 10 W

9-18   37.6 μA, 7.4 V, 0.95 W, 35 mW

10-1 $R_1 = 6.8$ kΩ, $R_2 = 220$ kΩ, $R_3 = 6.8$ kΩ, $R = 680$ Ω, $C = 0.033$ μF

10-2 $R_1 = 4.7$ kΩ, $R_2 = 150$ kΩ, $R_3 = 4.7$ kΩ, $R = 180$ Ω

10-3 $R_1 = 5.6$ kΩ, $R_2 = 3.3$ kΩ, $R_3 = 1.5$ kΩ, $R_4 = 1.5$ kΩ, $C_1 = 5.6$ μF

10-4 $C_1 = C_2 = 0.1$ μF, $L = 56$ mH, $R_1 = 47$ kΩ, $R_2 = 180$ kΩ

10-5 $C_1 = C_2 = 0.82$ μF, $R_1 = 33$ kΩ, $R_2 = 150$ kΩ

10-6 $C_1 = C_2 = 1300$ pF, $R_1 = R_2 = R_4 = 8.2$ kΩ, $R_3 = 18$ kΩ

10-7 $R_1 = R_2 = R_4 = 3.3$ kΩ, $R_3 = 6.8$ kΩ

11-1   8.8 V, 8.9425 V, 0.002%/°C

11-2   IN751, $R_S = 116$ Ω, $R_L = 103$ Ω, $S_V = 0.128$, $Z_0 = 14.83$ Ω

11-3   3%, 14.7%

11-4   IN757, $R_S = 470$ Ω, 0.115 V

11-5   10.91 mA, 679 Ω

11-6   IN755, $R_E = 3.3$ kΩ, $R_1 = 680$ Ω, 2.06 mA

12-3   2 mA/V, 0.35 mA/V

12-5   259 mA/V

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16-8   C6B, $R_1 = (1.4\ M\Omega$ to $8.5\ M\Omega)$
16-9 $R_1 = (129\ k\Omega$ to $1.55\ M\Omega)$, (V_R for D_1 & D_2) > 311 V
16-10 $1.5°$

17-1   120 mW, 21.9 V
17-2   11.7 V, 17.1 V
17-3   50.8 Hz
17-4   11.3 kΩ, 3.4 MΩ
17-5   33 kΩ, 12 kΩ, 18.95 V, 1.5 V, 45 kΩ
17-6   270 Ω, 0.34, 1 V
17-7   15.6 Hz, 12.4 Hz, 21.2 V
17-8   1.8 kΩ, 820 Ω, $I_G \leqslant 1$ mA, $V_{Ak} \leqslant 2.5$ V
17-9   6.8 kΩ, 3.9 kΩ, 14.6 V, 0.9 V, 10.7 kΩ

Chapter 17

18-1   368 W, 3 mW
18-2   1.18 kW
18-3   6.5 kΩ between base and $+5$ V
18-4   50 μA, 22 μA
18-5   162 Ω, 0.25 V, 0.9 mA
18-6   43 Ω, 116 Ω, 326 Ω
18-7   0.04 V
18-8   70 cells, 5 parallel groups of 14 in series
18-9   1,792 parallel groups of 279 in series, 116kWh
18-10   2.5 kΩ
18-11   1.4 mA
18-12 $R_1 = 27$ kΩ, $R_2 = 680$ Ω with $V_t = V_{CC}$
18-13   1.2 kΩ

Chapter 18

19-1   10.58 V
19-3   1.5, 12
19-4   1.7 MHz, 2.5 MHz
19-5   200 Ω, 3.75 mA, 2.1 mA, 0.65 mA
19-6   (a) 15 kΩ, (b) 13.7 kΩ, 14.96 kΩ, (c) 15 kΩ, 14.96 kΩ

Chapter 19

20-1   17 mA, 34 V
20-2   70 V
20-4   5 kΩ, 4 mA/V, 20
20-5   3.5 mA, 78 V, 3.53 kΩ, 14.1
20-6 -2.6 V, 1.3 mA, 80 V
20-7   6.8 kΩ, 17.3

Chapter 20

20-8   270 Ω, 100 kΩ, 2.1 kΩ
20-9   8.9 mA, 78 V
20-10 −6 V
20-11 120 Ω, 18.75, 3 kΩ
20-12 3.75 mA, −8 V
20-13 15 V/cm, 0.067 cm/V

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