

CST 307	MICROPROCESSORS AND MICROCONTROLLERS	Category	L	T	P	Credit	Year of Introduction
		PCC	3	1	0	4	2019

Preamble: The course enables the learners capable of understanding the fundamental architecture of microprocessors and micro controllers. This course focuses on the architecture, assembly language programming, interrupts, interfacing of microprocessors with peripheral devices and microcontrollers and its programming. It helps the learners to extend the study of latest processors and develop hardware based solutions.

Prerequisite : Sound knowledge in Logic System Design and Computer organization & architecture.

CO#	Course Outcomes
CO1	Illustrate the architecture , modes of operation and addressing modes of microprocessors (Cognitive knowledge: Understand)
CO2	Develop 8086 assembly language programs. (Cognitive Knowledge Level: Apply)
CO3	Demonstrate interrupts, its handling and programming in 8086. (Cognitive Knowledge Level: Apply))
CO4	Illustrate how different peripherals (8255,8254,8257) and memory are interfaced with microprocessors. (Cognitive Knowledge Level: Understand)
CO5	Outline features of microcontrollers and develop low level programs. (Cognitive Knowledge Level: Understand)

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓									✓
CO2	✓	✓	✓	✓								✓
CO3	✓	✓	✓	✓								✓
CO4	✓	✓	✓	✓								✓
CO5	✓	✓	✓	✓								✓

Abstract POs defined by National Board of Accreditation			
PO#	Broad PO	PO#	Broad PO
PO1	Engineering Knowledge	PO7	Environment and Sustainability
PO2	Problem Analysis	PO8	Ethics
PO3	Design/Development of solutions	PO9	Individual and team work
PO4	Conduct investigations of complex problems	PO10	Communication
PO5	Modern tool usage	PO11	Project Management and Finance
PO6	The Engineer and Society	PO12	Life long learning

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination Marks (%)
	Test1 (%)	Test2 (%)	
Remember	20	20	20
Understand	40	40	40
Apply	40	40	40
Analyze			
Evaluate			
Create			

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance	:	10 marks
Continuous Assessment Tests	:	25 marks
Continuous Assessment Assignment	:	15 marks

Internal Examination Pattern:

Each of the two internal examinations has to be conducted out of 50 marks

First Internal Examination shall be preferably conducted after completing the first half of the syllabus and the Second Internal Examination shall be preferably conducted after completing remaining part of the syllabus.

There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly covered module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly covered module), each with 7 marks. Out of the 7 questions in Part B, a student should answer any 5.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

Syllabus**Module-1(Evolution of microprocessors):**

8085 microprocessor (-Basic Architecture only). 8086 microprocessor – Architecture and signals, Physical Memory organization, Minimum and maximum mode of 8086 system and timings. Comparison of 8086 and 8088. Machine language Instruction format.

Module-2 (Addressing modes and instructions):

Addressing Modes of 8086. Instruction set – data copy /transfer instructions, arithmetic instructions, logical instructions, string manipulation instructions, branch instructions, unconditional and conditional branch instruction, flag manipulation and processor control instructions. Assembler Directives and operators. Assembly Language Programming with 8086.

Module- 3 (Stack and interrupts):

Stack structure of 8086, programming using stack- Interrupts - Types of Interrupts and Interrupt Service Routine- Handling Interrupts in 8086- Interrupt programming. -

Programmable Interrupt Controller - 8259, Architecture (Just mention the control word, no need to memorize the control word)- Interfacing Memory with 8086.

Module- 4 (Interfacing chips):

Programmable Peripheral Input/output port 8255 - Architecture and modes of operation- Programmable interval timer 8254-Architecture and modes of operation- DMA controller 8257 Architecture (Just mention the control word, no need to memorize the control word of 8254 and 8257)

Module- 5 (Microcontrollers):

8051 Architecture- Register Organization- Memory and I/O addressing- Interrupts and Stack- 8051 Addressing Modes- Instruction Set- data transfer instructions, arithmetic instructions, logical instructions, Boolean instructions, control transfer instructions- Simple programs.

Text Books

1. Bhurchandi and Ray, Advanced Microprocessors and Peripherals, Third Edition McGraw Hill.
2. Raj Kamal, Microcontrollers: Architecture, Programming, Interfacing and System Design, Pearson Education.
3. Ramesh Gaonkar, Microprocessor Architecture, Programming, and Applications with the 8085, Penram International Publishing Pvt. Ltd.

Reference Books

1. Barry B. Brey, The Intel Microprocessors – Architecture, Programming and Interfacing, Eighth Edition, Pearson Education.
2. A. NagoorKani, Microprocessors and Microcontrollers, Second Edition, Tata McGraw Hill
3. Douglas V. Hall, SSSP Rao, Microprocessors and Interfacing, Third Edition, McGrawHill Education.

Sample Course Level Assessment Questions

Course Outcome1 (CO1):

- 1) Describe how pipelining is implemented in 8086 microprocessor
- 2) Illustrate maximum mode signals in 8086.

Course Outcome 2(CO2):

- 1) Write an 8086 assembly language program for sorting a sequence of N, 8 bit numbers. Describe the modifications that can be done on the above program so that it will sort N, 16 bit numbers. Rewrite the program with those modifications also.

Course Outcome 3 (CO3):

- 1) Design an interface between 8086 CPU and two chips of 16 x 8 EPROM and two chips of 32K x 8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H.
- 2) Give the sequence of instructions for setting the IVT for interrupt type 23H. Assume the Interrupt Service Routine, is present in the code segment named CODE.
- 3) Describe the role of Interrupt Request register and In service register in 8259.

Course Outcome 4(CO4):

- 1) Show how to interface an 8255 with 8086 to work as an I/O port with the following specifications. Initialize port A as output, port B as input and port C as output. Port A address should be 05A0H. Write a program to sense switch positions SW 0 -SW 7 connected to port B. The sensed pattern is to be displayed on port A, to which 8 LED's are attached, while port C lower displays *number of off switches* out of total 8 switches.
- 2) Specify the importance of the DMA address register and Terminal count register in 8257.

Course Outcome 5(CO5):

- 1) Write an 8051 assembly language program to count the number of 1's and 0's in a given 8 bit number
- 2) Write an 8051 assembly language program for computing the square root of an 8 bit number.

Model Question Paper

QP CODE:

Reg No: _____

Name: _____

PAGES : 4

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH. DEGREE EXAMINATION, MONTH & YEAR

Course Code: CST 307

Course Name: Microprocessors and Microcontrollers

Max.Marks:100

Duration: 3 Hours

PART A

Answer All Questions. Each Question Carries 3 Marks

- Describe the functions of following signals in 8086
a)NMI b)ALE
- List any three differences between 8085 and 8086 microprocessors.
- Assume AL register is having the value 7FH. What will be the content of AL after the following instructions are executed
a)ROR AL,01 b)SAR AL,01
- Specify the use of following assembler directives - EQU , EVEN
- Differentiate between maskable and non maskable interrupts?
- Define Interrupt Service Routine? How to find the address of the ISR corresponding to a given interrupt in 8086?
- Give the purposes of the signals DRQ, TC and MARK in 8257?
- How 8254 is used as a square wave generator?
- Differentiate between indirect and indexed addressing modes in 8051.

10. Write the sequence of 8051 instructions to store any two numbers at two consecutive locations 70H and 71H, multiply them and store the result in location 72H. (10x3=30)

Part B

(Answer any one question from each module. Each question carries 14 Marks)

11. (a) Specify the significance of segmentation and how it is implemented in 8086 (5)
 (b) Explain the maximum mode signals in 8086. (9)

OR

12. (a) Write down the differences between 8086 and 8088 processors (4)
 (b) Explain the physical memory organization of 8086 with a neat diagram. How does the 8086 processor access a word from an odd memory location? How many memory cycles does it take? (10)
13. (a) Write an 8086 assembly language program for finding the sum of the squares of first N natural numbers. Calculate the squares of each number using a subroutine SQUARE. (10)
 (b) Describe any four control transfer instructions in 8086. (4)

OR

14. (a) Write an 8086 assembly language program for printing the reverse of a given input string. (5)
 (b) Explain the addressing modes for sequential control flow instructions in 8086. (9)
15. (a) Give the stack structure of 8086. (5)
 (b) Explain the architecture of 8259 with diagram (9)

OR

16. (a) Interface 32Kx8 RAM using four numbers of 8Kx8 memory chips and 16Kx8 ROM using two numbers of 8Kx8 EPROM chips. The address map is given as RAM starts at 00000H and ROM ends at FFFFFH (10)
 (b) Describe the predefined interrupts in 8086 (4)

17. (a) Explain the architecture of 8255 with a neat diagram (10)
- (b) Identify the mode and I/O configuration for ports A, B and C of an 8255 after its control register is loaded with 86 H? (4)

OR

18. (a) Define Direct Memory Access (DMA) and illustrate the role of a DMA controller? Explain the register organization of 8257 and state how these registers are used during DMA transfer operations. (8)
- (b) Explain the architecture of 8254 timer chip (6)
19. (a) Explain the architecture of 8051 microcontroller. (9)
- (b) Write an 8051 assembly language program for adding two matrices whose elements are stored sequentially in some memory location. Assume suitable locations. (5)

OR

20. (a) Explain the internal data memory organization of 8051. (9)
- (b) Describe the control transfer instructions of 8051 microcontroller. (5)

Teaching Plan

No	Contents	No of Lecture Hrs
Module 1 : (Evolution of microprocessors) (9 hours)		
1.1	Overview of 8085 microprocessor	1 hour
1.2	Architecture of 8085	1 hour
1.3	Architecture of 8086	1 hour
1.4	Signals in 8086	1 hour
1.5	Physical Memory organization	1 hour
1.6	Minimum and maximum mode 8086 system and timings(Lecture 1)	1 hour
1.7	Minimum and maximum mode 8086 system and timings(Lecture 2)	1 hour
1.8	Comparison of 8086 and 8088	1 hour
1.9	Machine language Instruction format	1 hour
Module 2 :(programming of 8086) (9 hours)		
2.1	Addressing Modes of 8086	1 hour
2.2	Instruction set – data copy/transfer instructions	1 hour
2.3	arithmetic instructions, logical instructions	1 hour
2.4	string manipulation instructions, branch instructions	1 hour
2.4	unconditional and conditional branch instruction	1 hour
2.5	flag manipulation and processor control instructions	1 hour
2.6	Assembler Directives and operators	1 hour
2.7	Assembly Language Programming with 8086(Lecture 1)	1 hour
2.8	Assembly Language Programming with 8086(Lecture 2)	1 hour
2.9	Assembly Language Programming with 8086(Lecture 3)	1 hour
Module 3 : (stack and Interrupts) (9 hours)		
3.1	Stack structure of 8086, programming using stack.	1 hour
3.2	Types of Interrupts and Interrupt Service Routine.	1 hour
3.3	Handling Interrupts in 8086(Lecture 1)	1 hour
3.4	Handling Interrupts in 8086(Lecture 2)	1 hour

3.5	Interrupt programming.	1 hour
3.6	Programmable Interrupt Controller -8259 (Lecture 1)	1 hour
3.7	Programmable Interrupt Controller -8259 (Lecture 2)	1 hour
3.8	Interfacing Memory with 8086 (Lecture 1)	1 hour
3.9	Interfacing Memory with 8086 (Lecture 2)	1 hour
Module 4 :(Interfacing chips) (7 hours)		
4.1	Programmable Peripheral Input/output port- 8255 (Lecture 1)	1 hour
4.2	Programmable Peripheral Input/output port- 8255 (Lecture 2)	1 hour
4.3	Programmable Peripheral Input/output port- 8255 (Lecture 3)	1 hour
4.4	Programmable interval timer 8254 (Lecture 1)	1 hour
4.5	Programmable interval timer 8254 (Lecture 2)	1 hour
4.6	DMA controller 8257 Architecture (Lecture 1)	1 hour
4.7	DMA controller 8257 Architecture (Lecture 2)	1 hour
Module 5 : (Microcontrollers) (11 hours)		
5.1	8051 Architecture (Lecture 1)	1 hour
5.2	8051 Architecture (Lecture 2)	1 hour
5.3	Register Organization, Memory and I/O addressing	1 hour
5.4	Interrupts and Stack	1 hour
5.5	Addressing Modes	1 hour
5.6	Data transfer instructions, Arithmetic instructions	1 hour
5.7	Logical instructions,	1 hour
5.8	Boolean instructions	1 hour
5.9	Control transfer instructions	1 hour
5.10	Programming of 8051 (Lecture 1)	1 hour
5.11	Programming of 8051(Lecture 2)	1 hour