

Module- 4 (Interfacing chips):

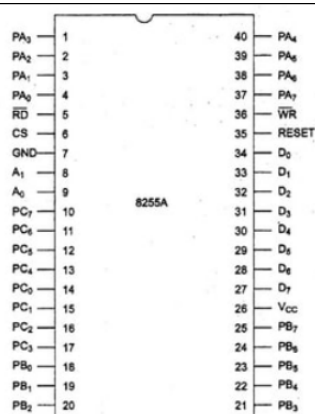
Programmable Peripheral Input/output port 8255 - Architecture and modes of operation- Programmable interval timer 8254-Architecture and modes of operation- DMA controller 8257 Architecture (Just mention the control word, no need to memorize the control word of 8254 and 8257)

I. Programmable Peripheral Input/output port 8255 8255 - Architecture and modes of operation

8255 is a programmable peripheral interface, which means it is a programmable device used to interface I/O devices with the processor. In reality, we are not supposed to connect I/O devices directly with the data bus of the processor, instead there should be some device to which I/O ports should be there to connect I/O devices.

- It has 3 8-bit ports, all ports are bidirectional (Can be used as Input port or output port). They are Port – A (PA) and PB, PC. Port A contains one 8-bit output latch/buffer and one 8-bit input buffer.
- Port B is similar to PORT A.
- Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.



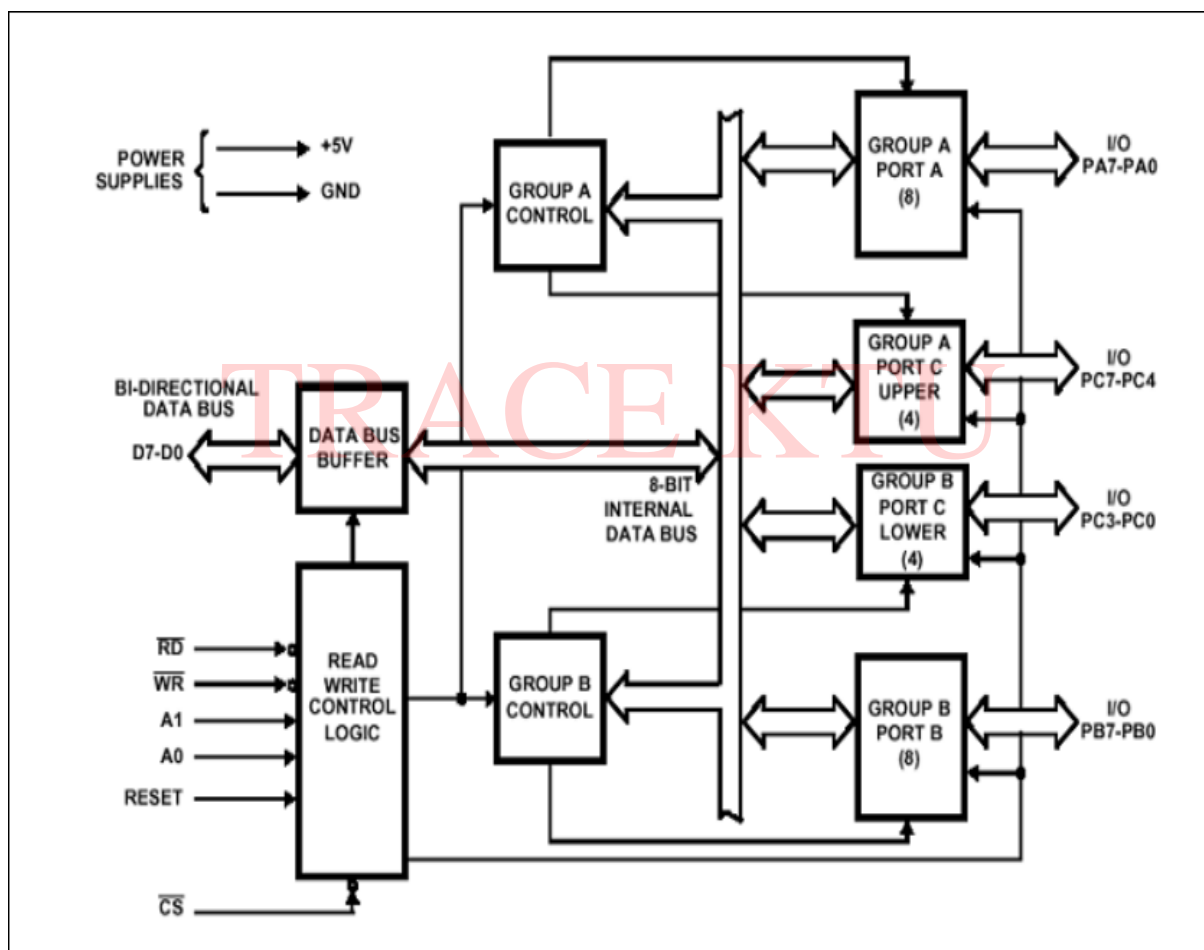
8255 PPI pin out

- Vcc Apply 5 volts to this pin.
- GND Ground this pin
- CS (chip select) A low on this selects the 8255. Now you can use the chip.
- RD (read) A low on this pin indicates that we want to read data from specified port of 8255.
- WR (write) A low on this pin indicates that we want to write to 8255.
- RESET A high on this pin clear all registers and ports.

8255A Pinout

Architecture

It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines. The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port.



Thus, Group A contains an 8-bit port A along with a 4-bit port C upper. The port A lines are identified by symbols PA0-PA7 while the port C lines are identified as PC4-PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0-PC3. The port C upper and port C lower can be used in combination as an 8-bit port C. Both the port C are assigned the same address. Thus, one may have either three 8-bit I/O ports

or two 8-bit and two 4-bit ports from 8255. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR). This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

Functional Descriptions

Data Bus Buffer

It is a tri-state 8-bit buffer, which is used to interface the microprocessor to the system data bus. Data is transmitted or received by the buffer as per the instructions by the CPU. Control words and status information is also transferred using this bus.

Read/Write Control Logic

This block is responsible for controlling the internal/external transfer of data/control/status word. It accepts the input from the CPU address and control buses, and in turn issues command to both the control groups.

CS

It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255A and the CPU. It is connected to the decoded address, and A0 & A1 are connected to the microprocessor address lines.

Their result depends on the following conditions –

CS	A ₁	A ₀	Result
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	Control Register

1 X X No Selection

WR

It stands for write. This control signal enables the write operation. When this signal goes low, the microprocessor writes into a selected I/O port or control register.

RESET

This is an active high signal. It clears the control register and sets all ports in the input mode.

RD

It stands for Read. This control signal enables the Read operation. When the signal is low, the microprocessor reads the data from the selected I/O port of the 8255.

A0 and A1

These input signals work with RD, WR, and one of the control signals. Following is the table showing their various signals with their result.

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A ₁	A ₀	RD	WR	CS	Result
0	0	0	1	0	<u>Input Operation</u> PORT A → Data Bus
0	1	0	1	0	PORT B → Data Bus
1	0	0	1	0	PORT C → Data Bus
0	0	1	0	0	<u>Output Operation</u> Data Bus → PORT A
0	1	1	0	0	Data Bus → PORT A
1	0	1	0	0	Data Bus → PORT B
1	1	1	0	0	Data Bus → PORT D

Modes of Operation

8255A has three different operating modes –

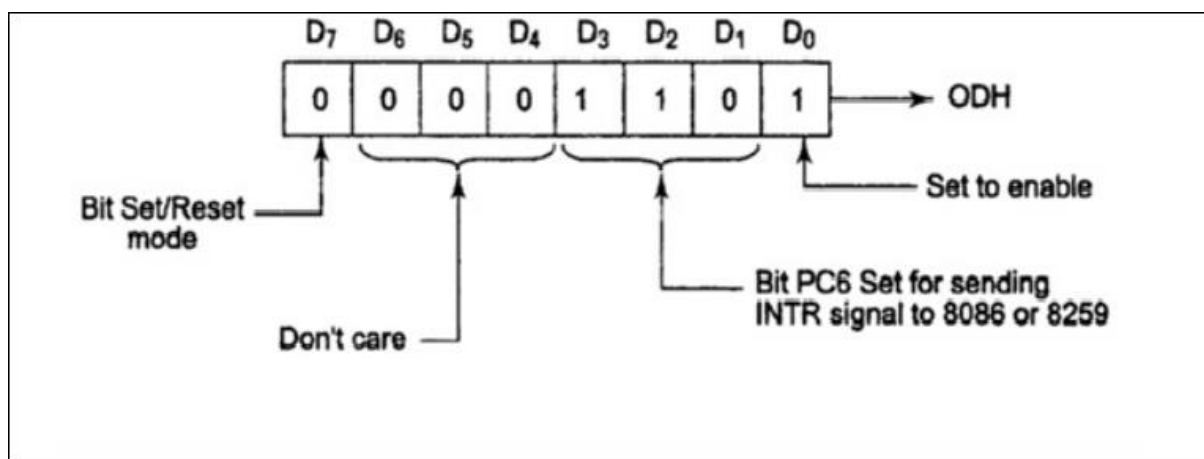
1. INPUT/OUTPUT MODE

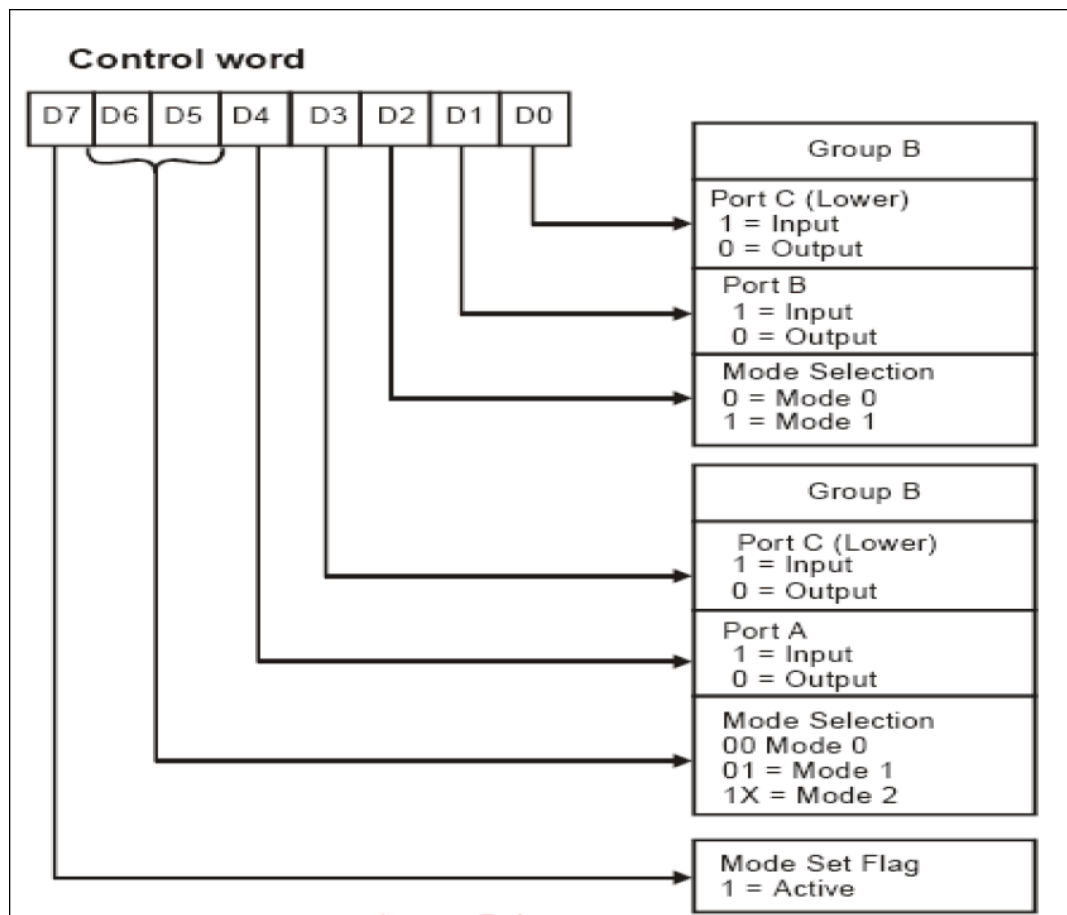
There are three basic modes of operation than can be selected by the system software:

- **Mode 0 -Basic Input/Output**
- **Mode 1 -Strobed Input/Output**
- **Mode 2 -Bi-directional Bus**
- **Mode 0** – In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.

In mode 0 each group can be used as input or output. Port A, port B and Port C can be used as input or output. Port C has the specialty that it can be divided in to two nibbles upper and lower. Both upper and lower can now be programmed to use as input or output. Mode 0 is also known as input/output mode (I/O mode). Question arises how we can do so. Yes, it's simple. Just send a control word to 8255 and it will set itself according to your control word. The control word for mode 0 is like this.

In mode 0 you can also access individual bits of port C. For bit set reset mode D7 will always be 0.



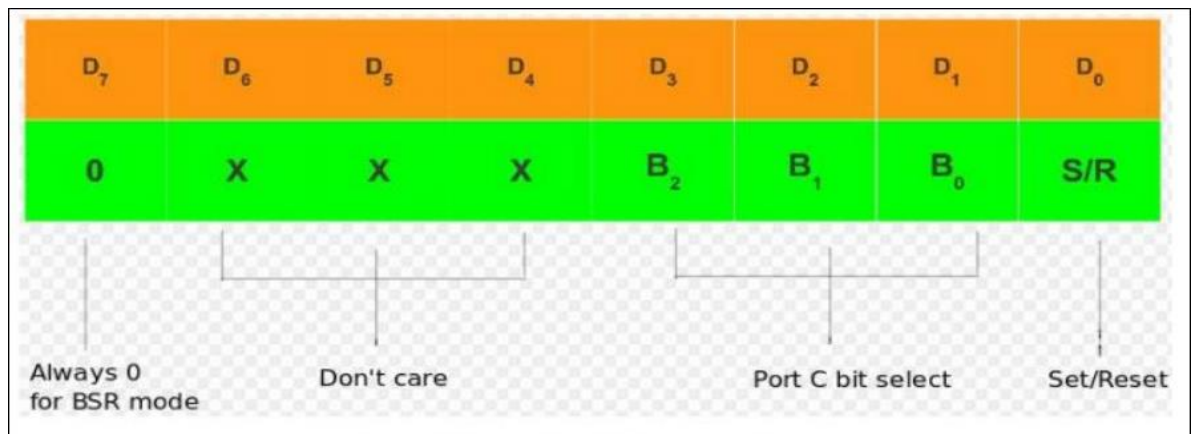


- **Mode 1** - In mode 1 each group can be used as 8-bit input or output data bus and the remaining 4-bits are used as handshaking and interrupt control signals. Port A is used with port c upper three bits and port B is used with port c lower 3 bits. The remaining 2 bits of port C can be used as control signals.
- **Mode 2** – In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

2. BIT SET/RESET (BSR) MODE

In this mode only port b can be used (as an output port). Each line of port C (PC0 - PC7) can be set/reset by suitably loading the command word register. no effect occurs in input-output mode. The individual bits of port c can be set or reset by sending the signal OUT instruction to the control register.

- The figure shows the control word format in BSR mode. This mode is selected by making D7='0'.
- D0 is used for bit set/reset. When D0= '1', the port C bit selected (selection of a port C bit is shown in the next point) is SET, when D0 = '0', the port C bit is RESET.
- D1, D2, D3 are used to select a particular port C bit whose value may be altered using D0 bit as mentioned above.



TRACE KTU

II. Programmable interval timer 8254 - Architecture and modes of operation

The Intel 8253 and 8254 are Programmable Interval Timers (PTIs) designed for microprocessors to perform timing and counting functions using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for “OUT” output. To operate a counter, a 16-bit count is loaded in its register. On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

Difference between 8253 and 8254

The following table differentiates the features of 8253 and 8254 –

8253	8254
<ul style="list-style-type: none">• Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
<ul style="list-style-type: none">• It uses N-MOS technology	It uses H-MOS technology
<ul style="list-style-type: none">• Read-Back command is not available	Read-Back command is available
<ul style="list-style-type: none">• Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.

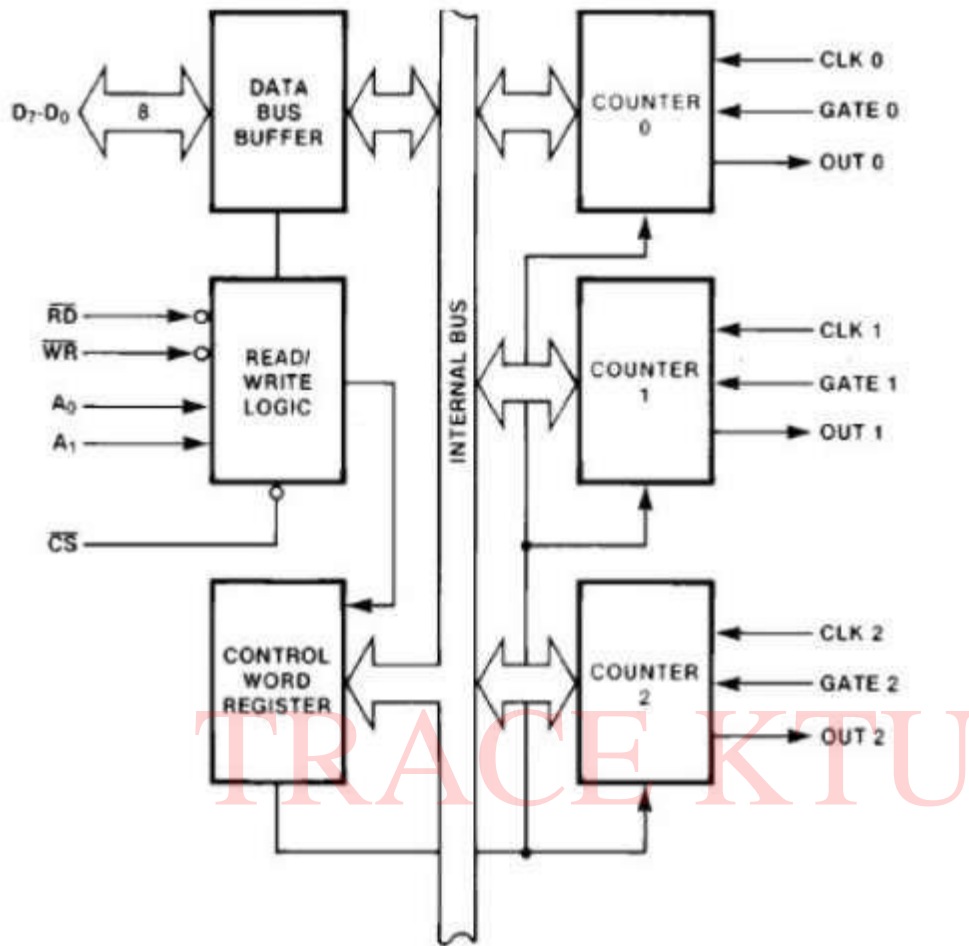
Features of 8253 / 54

The most prominent features of 8253/54 are as follows –

- It has three independent 16-bit down counters.
- It can handle inputs from DC to 10 MHz.
- These three counters can be programmed for either binary or BCD count.
- It is compatible with almost all microprocessors.
- 8254 has a powerful command called READ BACK command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

6.2.1 8254 Architecture

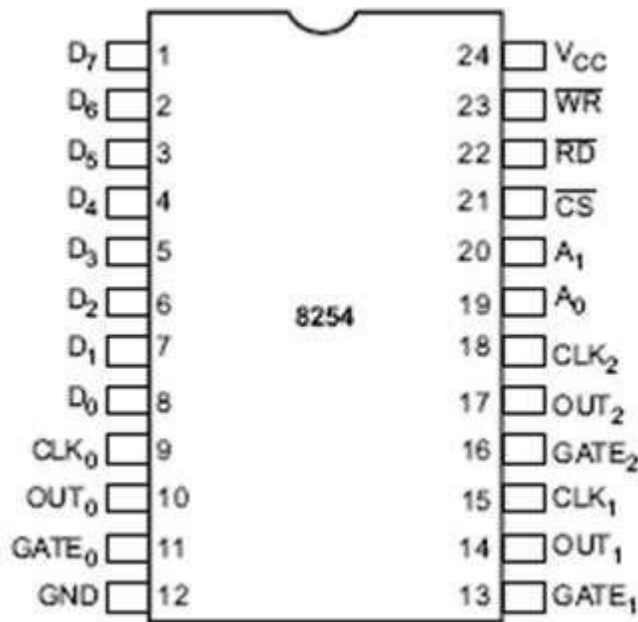
The architecture of 8254 looks as follows –



6.2.2 8254 Pin Description

Here is the pin diagram of 8254 –

In the above figure, there are three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals - CLOCK & GATE, and one output signal - OUT.



Data Bus Buffer

It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has three basic functions –

- Programming the modes of 8253/54.
- Loading the count registers.
- Reading the count values.

Read/Write Logic

It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW. Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

A1	A0	Result
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register
X	X	No Selection

Control Word Register

This register is accessed when lines A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation.

Following table shows the result for various control inputs.

A1	A0	RD	WR	CS	Result
0	0	1	0	0	Write Counter 0
0	1	1	0	0	Write Counter 1
1	0	1	0	0	Write Counter 2
1	1	1	0	0	Write Control Word
0	0	0	1	0	Read Counter 0
0	1	0	1	0	Read Counter 1
1	0	0	1	0	Read Counter 2
1	1	0	1	0	No operation
X	X	1	1	0	No operation
X	X	X	X	1	No operation

Counters

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output are configured by the selection of modes stored in the control Word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

6.2.3 MODES OF OPERATION

8253/54 can be operated in 6 different modes. In this chapter, we will discuss these operational modes.

i. Mode 0 — Interrupt on Terminal Count

It is used to generate an interrupt to the microprocessor after a certain interval. Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.

The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.

The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.

ii. Mode 1 – Programmable One Shot

It can be used as a mono stable multi-vibrator. The gate input is used as a trigger input in this mode. The output remains high until the count is loaded and a trigger is applied.

iii. Mode 2 – Rate Generator

The output is normally high after initialization. Whenever the count becomes zero, another low pulse is generated at the output and the counter will be reloaded.

iv. Mode 3 – Square Wave Generator

This mode is similar to Mode 2 except the output remains low for half of the timer period and high for the other half of the period.

v. Mode 4 – Software Triggered Mode

In this mode, the output will remain high until the timer has counted to zero, at which point the output will pulse low and then go high again. The count is latched when the GATE signal goes LOW. On the terminal count, the output goes low for one clock cycle then goes HIGH. This low pulse can be used as a strobe.

vi. Mode 5 – Hardware Triggered Mode

This mode generates a strobe in response to an externally generated signal. This mode is similar to mode 4 except that the counting is initiated by a signal at the gate input, which means it is hardware triggered instead of software triggered. After it is initialized, the output goes high. When the terminal count is reached, the output goes low for one clock cycle.

III. DMA controller 8257

Suppose any device which is connected to input-output port wants to transfer data to memory, first of all it will send input-output port address and control signal, input-output read to input-output port, then it will send memory address and memory write signal to memory where data has to be transferred. In normal input-output technique the processor becomes busy in checking whether any input-output operation is completed or not for next input-output operation, therefore this technique is slow.

DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

This problem of slow data transfer between input-output port and memory or between two memory is avoided by implementing Direct Memory Access (DMA) technique. This is faster as the microprocessor/computer is bypassed and the control of address bus and data bus is given to the DMA controller.

- HOLD – hold signal
- HLDA – hold acknowledgment
- DREQ – DMA request
- DACK – DMA acknowledgment

How DMA Operations are Performed?

Following is the sequence of operations performed by a DMA –

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.

- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

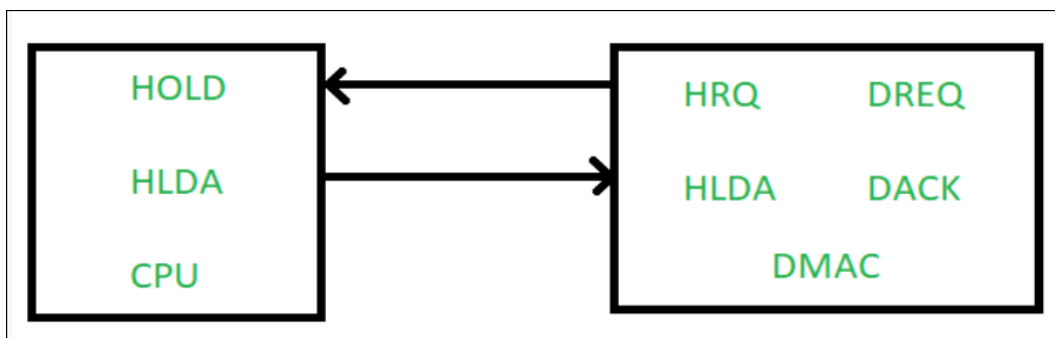
Features of 8257

Here is a list of some of the prominent features of 8257 –

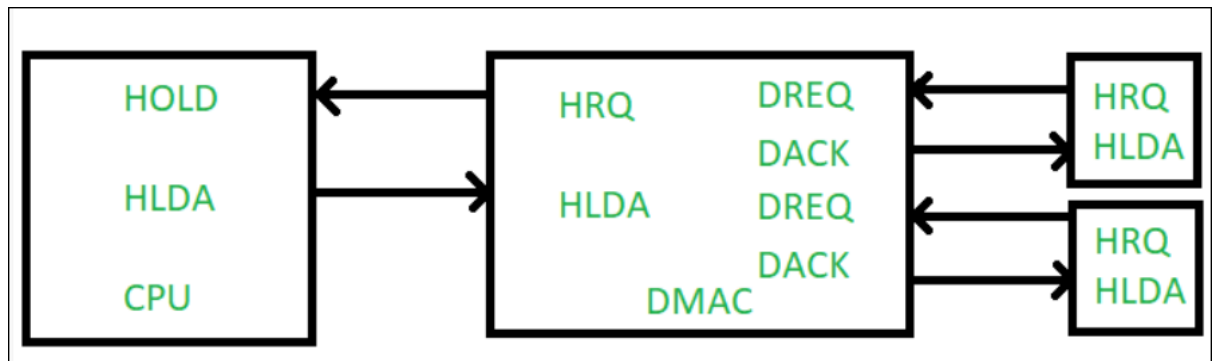
- It has four channels which can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It generates MARK signal to the peripheral device that 128 bytes have been transferred.
- It requires a single-phase clock.
- Its frequency ranges from 250Hz to 3MHz.
- It operates in 2 modes, i.e., Master mode and Slave mode.

Modes of DMAC:

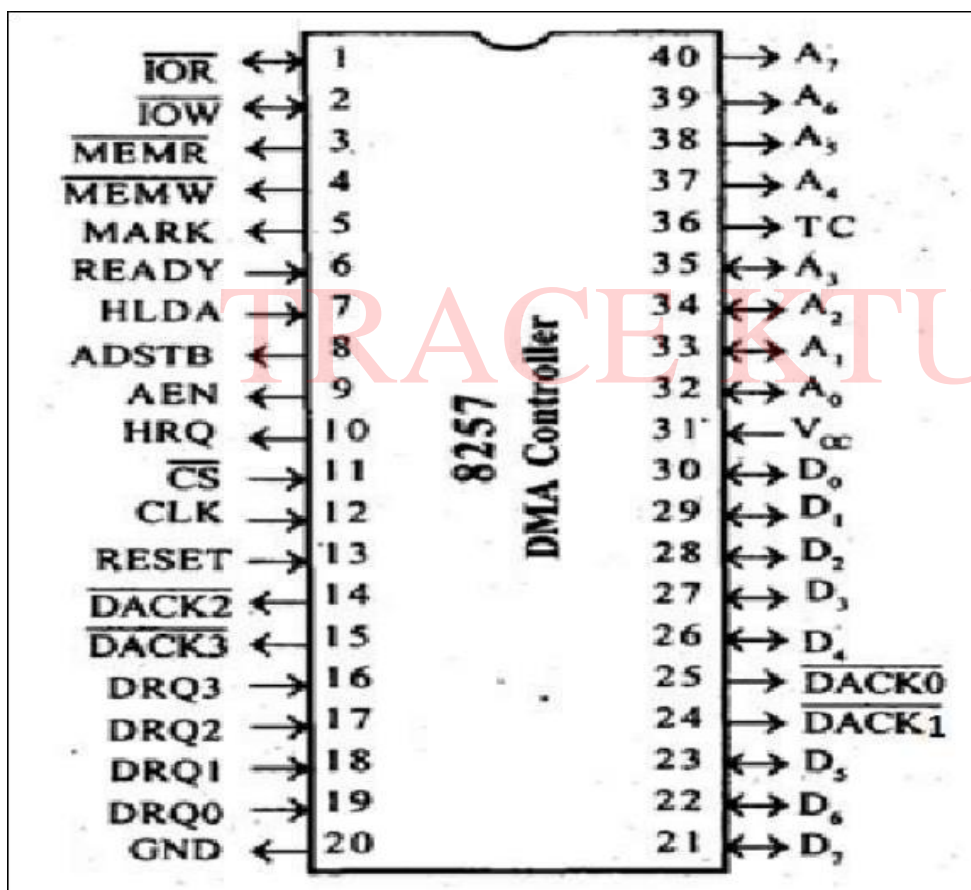
1. Single Mode – In this only one channel is used, means only a single DMAC is connected to the bus system.



2. **Cascade Mode** – In these multiple channels are used, we can further cascade more number of DMACs.



8257 Pin Description



DRQ0–DRQ3

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ_0 has the highest priority and DRQ_3 has the lowest priority among them.

DACK₀ – DACK₃

These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

Do – D7

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

A₀ - A₃

These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

A4 - A7

These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADST

This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

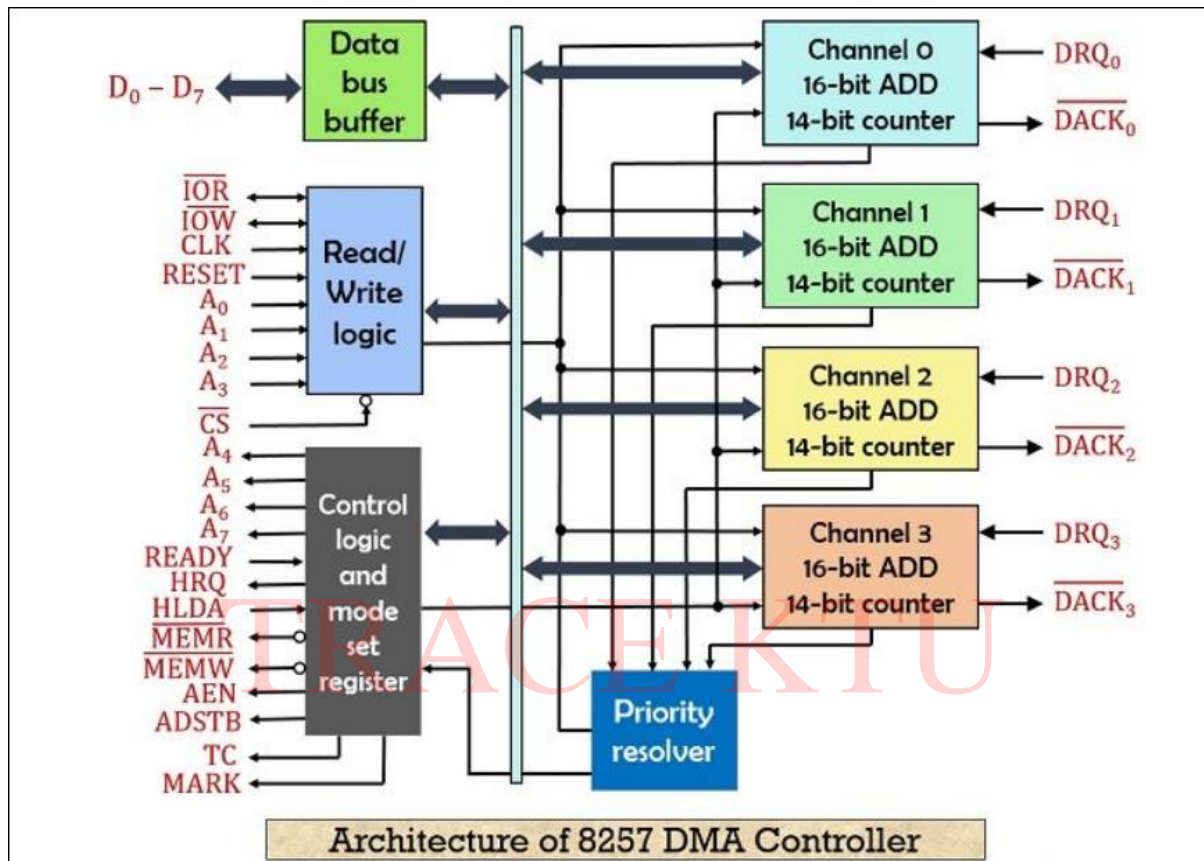
MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc

It is the power signal which is required for the operation of the circuit.

8257 - Architecture



It consists of five functional blocks:

- a) Data bus buffer
- b) Control logic
- c) Read/write logic
- d) Priority Resolver
- e) DMA channels

Data Bus Buffer:

8-bit Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

Read/Write Logic:

In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the A0-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the selected register depending upon whether IOW or IOR signal is activated. In master mode, the read/write logic generates the IOR and IOW signals to control the data flow to or from the selected peripheral.

Control Logic:

The control logic controls the sequences of operations and generates the required control signals like AEN, ADSTB, MEMR, MEMW, TC and MARK along with the address lines A4-A7, in master mode.

Priority Resolver:

The priority resolver resolves the priority of the four DMA channels depending upon whether normal priority or rotating priority is programmed.

Register Organisation of 8257:

The 8257 performs DMA operation over four independent DMA channels with the following Registers.

1. DMA Address Register

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting address stored in the DMA Address Register.

2. Terminal Count Registers

Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.

After each DMA cycle, the terminal count register content will be decremented by one and finally it becomes zero after the required number of DMA cycles are over. The bits 14 and 15 of this register indicate the type of the DMA operation (transfer).

3. Mode Set Register

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation. The bits Do-D3 enable one of the four DMA channels of 8257. If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel. If the TC STOP bit is programmed to be zero, the channel is not disabled, even after the count reaches zero and further request are allowed on the same channel. The auto load bit, if set, enables channel 2 for the repeat block chaining operations, without immediate software intervention between the two successive blocks. The extended write bit, if set to '1', extends the duration of MEMW and IOW signals by activating them earlier, which is useful in interfacing the peripherals with different access times.

4. Status register

The lower order 4-bits of this register contain the terminal count status for the four individual channels. If any of these bits is set, it indicates that the specific channel has reached the terminal count condition. The update flag is not affected by the read operation. This flag can only be cleared by resetting 8257. The update flag is set every time, the channel 2 registers are loaded with contents of the channel 3 registers. It is cleared by the completion of the first DMA cycle of the new block. This register can only read.

DMA TRANSFER & OPERATIONS

The 8257 is able to accomplish three types of operations such as

1. DMA operation
2. Write Operation
3. Read Operation

Operational sequence of 8257 is as follows

- o The 8257 request any one of the 8257 DRQ inputs to transfer single byte.
- o In response to the request, the 8257 sends HRQ signal to CPU at its HLD input and waits for acknowledgement at the HLDA input.
- o If the DMA controller receives the HLDA signal it indicates that the bus is available for the transfer.
- o The DMA controller generate the read and write commands to transfer the

byte from/to the I/O Device.

- o The DACK line of the used channel is pulled down by the DMA controller to I/O device that requested for DMA transfers.
- o The HRQ line is lowered by the DMA controller to indicate the CPU that it may regain the control of the bus.
- o The DRQ must be high until acknowledged.
- o In each s4 state, the DRQ lines are sampled and highest priority request is recognized during next transfer. The HRQ line is maintained active till all the DRQ line go low.

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