APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Scheme for Valuation/Answer Key

Scheme of evaluation (marks in brackets) and answers of problems/key

FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2021

Course Code: CST 307

Course Name: MICROPROCESSORS AND MICROCONTROLLERS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		List any six features -3 marks	3
2		3054 * 10 + 1580 = 31AC0h 3 marks	3
3		Directives 1 marks a) 1 mark b) 1 mark	3
4		Instructions 2 marks and examples 1 marks	3
5		interrupt address resolution steps – 3 marks	3
6		Software vs hardware, maskable vs non-maskable	3
7		Group A(or Port A) mode 0, Port A –output, Port C Upper- Output, Group B(or Port B) mode 1 , Port B –Input , Port C Lower –Output	3
8		8257 features - 3marks	3
9		Minimum 3 difference 3 marks	3
10		IO ports - 3 marks	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Diagram 4 explanation 6	10
	b)	Min 4 differences	4
12	a)	Read Timing diagram - 4.5 marks Write Timing diagram - 4.5 marks	9
	b)	Flag register diagram 2 marks explanation 3 marks	5

Module -2

13	a)	Any six valid addressing modes supported by 8086 with one example for each can be given full marks. 1 mark for Addressing mode, 0.5 marks for example.	9
	b)	Min 4 instruction 4 marks + example 1 marks	5
14	a)		7

Instruction	AX	BX	CX	DX	CF	SF	ZF

ROR AX, 04h	**0003h**	0031h	0032h	0033h	0	0	0
CMP BX, CX	0030h	0031h	0032h	0033h	**1**	**1**	0
XCHG CX, DX	0030h	0031h	**0033h**	**0032h**	0	0	0
AND AX, BX	**0030h**	0031h	0032h	0033h	0	0	0
LOOP Addr	0030h	0031h	**0031h**	0033h	0	0	0
XOR AX, AX	**0000h**	0031h	0032h	0033h	0	0	**1**
STC	**0030h**	0031h	0032h	0033h	**1**	0	0
1 mark for each for correct instruction execution							

b) Proper use of Instruction – 3 , Correct logic - 4 marks 7

Module -3

15 a) Stack structure diagram 2 , marks operations PUSH, POP – 2 marks 4

b) Memory address calculations – 5 marks + interfacing diagram 5 marks 10

16 a) 8259 block diagram 3 marks explanation 5 marks 8

b) IVT 2 marks structure and its operation 3marks diagram 1 mark 6

Module -4

17 a) Block diagram – marks explanation 5 marks mode of operation 4 marks 9

b) Mode of operation 5 marks 5

18 a) 8255 block diagram 3 marks explanation 5 marks 8

b) DMA address reg, Terminal count reg, Mode set reg, status reg 2 marks Explanation 4 marks 6

Module -5

19 a) Internal RAM organization diagram- 4 marks explanation 4 marks 8

b) Addressing modes 1 marks each, examples 0.5 marks each 6

20 a) Diagram 4 marks explanation 5 marks 9

b) Any 5 Special function registers and its use- 5 marks 5

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