A Single Error Correcting and Double Error Detecting Coding Scheme for Computer Memory Systems

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Abstract

This paper proposes a new coding technique for single error correction and double error detection in computer memory systems. The number of 1's in the parity check matrix for the proposed coding is fewer than all currently available codes for this purpose. This results in simplified encoding and decoding circuitry for error detection and correction.

1. Introduction

Single bit error correcting and double-bit error detecting (SEC/DED) codes are extensively used in cache and in main memory systems in computers. An SEC/DED code has a minimum Hamming distance of 4. One such code is the Hsiao code [1]. It uses multiple parity bits to uniquely identify which bit(s) in a code word is erroneous as well as to define the error-free condition. The speed of error detection and correction in a code is largely dependent upon the associated encoder and decoder circuits. The complexity and the speed of such circuits are determined by the number of 1's in the parity check matrix (PCM). The fewer the number of 1's in the PCM the less complex the encoding and decoding circuits are; fewer 1's also enhance the speed of these circuits [2]. Among all the SEC/DED codes the Hsiao code has the minimum number of 1's in the PCM [3].

In Hsiao code the columns corresponding to the information bits are assigned all combinations of 3-out-of-*r* bits, where *r* is the number of check bits; this is followed by all combinations of 5-out-of-*r* bits and then by 7-out-of-*r* bits and so on until all information bits have unique columns. The check bits are assigned 1-out-of-*r* code words. The equations for the check bits in the PCM are derived by taking the linear sum (EX-OR) of all the information bits with 1s in a row in which the check bit is also a 1.

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A single bit error results in a syndrome pattern that matches a column of the PCM. Thus, matching a syndrome pattern to a column in the PCM can identify an erroneous bit. If the column corresponds to a check bit, then no correction is necessary. However for maintenance purposes the error information is logged. Since the Hsiao code uses only odd number of 1's in the columns of its PCM a syndrome pattern corresponding to a single bit error has odd parity. If the syndrome has an even parity, the presence of a double bit error in a code word is indicated.

This paper proposes a coding technique for single bit error correction and double bit error detection that requires fewer 1's in a PCM than that in the Hsiao code. The proposed code differs from the Hsiao code in that columns are assigned m-out-of-r code where $m \leq r$, with all combinations of 2-out-of-4 chosen first followed by increased values of m till all columns get unique code words. It also appends to each column two residue bits that are set to the mod-3 residue of the binary number corresponding to the column. Two columns are also incorporated, one for each residue bit. Each of the these columns is assigned a 1-out-of- (r+2) code word such that together with other assigned check bits they form a identity sub matrix.

2. Code Construction procedure

The PCM for the proposed code is constructed as follows:

i. Assuming r check bits (c_{r-1} , c_{r-2} ,……c_1 , c_0), an r- bit column with a single 1 is assigned to the check bit c_i.

ii. If the length of the information bits is k and ${}^rC_2 \geq k$ then k columns out of ${}^rC_2$ are selected. If ${}^rC_2 = k$, all ${}^rC_2$ columns are selected.

iii. If ${}^rC_2 < k$, all ${}^rC_2$ columns are selected; the remaining columns are selected first from ${}^rC_3$ columns, then from among ${}^rC_4$ columns and so on. This process is continued till all k columns in the PCM have been specified.

iv. Add two additional check bits, m_1 and m_0, to the r-check bits in the PCM. These two check bits are derived as follows. Each column of the PCM is treated as a binary number assuming the top most bit as the least significant bit; the mod-3 residue of the corresponding decimal number is appended as two residue bits to the column.

Let us illustrate the derivation of the PCM for k = 8. The required number of check bits are r = 4. Each check bit is assigned a 4-bit column as shown below:

c_3	c_2	c_1	c_0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0

Since ${}^4C_2 = 6$ is less than 8 (=k), an additional two columns have to be selected from ${}^4C_3$ combinations. Assuming $d_7\ d_6$ ……..d_0 are the information bits, a column assignment is selected which together with the previously assigned check bits form a PCM for the proposed code as shown below:

d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	c_3	c_2	c_1	c_0
0	1	0	1	1	1	0	0	0	0	0	1
1	1	1	0	0	1	1	0	0	0	1	0
1	1	1	0	1	0	0	1	0	1	0	0
1	0	0	1	0	0	1	1	1	0	0	0

The columns for d_7 and d_6 are selected such that the total number of 1's in each row is approximately equal.

The PCM with appended residue check bit columns m_1 and m_0 is shown in Fig.1.

d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	c_3	c_2	c_1	c_0	m_1	m_0
0	1	0	1	1	1	0	0	0	0	0	1	0	0
1	1	1	0	0	1	1	0	0	0	1	0	0	0
1	1	1	0	1	0	0	1	0	1	0	0	0	0
1	0	0	1	0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	1	0

Figure. 1 PCM for the (14, 8) code

The equations for the check bits are derived from the modified PCM:

$$c_0 = d_6 \oplus d_4 \oplus d_3 \oplus + d_2$$
$$c_1 = d_7 \oplus d_6 \oplus d_5 \oplus d_2 \oplus d_1$$
$$c_2 = d_7 \oplus d_6 \oplus d_5 \oplus d_3 \oplus d_0$$
$$c_3 = d_7 \oplus d_4 \oplus d_1 \oplus d_0$$
$$m_0 = d_6 \oplus d_1$$
$$m_1 = d_7 \oplus d_3$$

To illustrate let us assume d_7 d6 d5 d4 d_3 d2 d1 d_0 = 11010010. The corresponding check bits are $c_3\ c_2\ c_1\ c_0\ \ m_1\ m_0$ = 101010. The PCMs for other (n+k+2, n) codes where n is the number of information bits can be derived in a similar manner. For example the PCMs for the (32,24) and (74,64) code are shown in Fig. 2(a) and Fig 2(b) respectively.

```
11111000000000111111111  10000000
10000111100000111100000  01000000
01000100011100010011100  00100000
00100010010011001001 0011  00010000
00010001001010100100 1010  00001000
00001000100101100010 0101  00000100
00000010100001010101 0110  00000010
01010000001000001010 0001  00000001
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Figure. 2(a) PCM for the (32,24) code

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11111110000000000000000000001111111111111111111111000000000000000  1000000000
10000001111110000000000000001111111000000000000000011111111111111  0100000000
01000001000001111100000000001000001111100000000001111100000000000  0010000000
00100000100001000011110000000100001000011110000001000011110000000  0001000000
00010000010000100010001110000010000100010001110000100010001110000  0000100000
00001000001000010001001001100001000010001001001100010001001001100  0000010000
00000100000100001000100101010000100001000100101010001000100101010  0000001000
00000010000010000100010010110000010000100010010110000100010010110  0000000100

00000000101010000001010000101010101010110101011010101000000100000  0000000010
01010100000000101000000100000101010000001010000101010111010101101  0000000001
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Figure. 2(b) PCM for the (74,64) code

The error detection and correction strategy for a single bit error in the proposed code is similar to that in the Hsiao code. A single bit error will produce a syndrome pattern that matches a column in the PCM, the parity of the pattern is not important. The double error detection approach in the proposed code is different than in Hsiao code where a double bit error produces a syndrome pattern that has even parity. In the proposed code the double error detection is based on the following lemmas

Lemma 1: A double bit error composed of two erroneous information bits in a code word will result in the last two syndrome bits to be 11 if one of the corresponding columns in the PCM has 01 as the residue check bits and the other one has 10.

Proof: The residue bits for each column in the PCM are 00,01 or 10. Thus the residue check bits of 11 in a syndrome pattern can result only from the linear sum of two columns corresponding two erroneous single bits if one has 01 as the residue check bits and the other has 10.

Lemma 2: A syndrome pattern with p 1's in the first r bits of a syndrome pattern where p is greater than the highest m in the m-out-of-r code words assigned to each bit in the PCM, indicates a double or a multi bit error in a code word.

Proof: The number of 1's in first r bits of each column in the PCM is 2-out-of-r, 3-out-of-r …m-out-of-r where m ≤ r. A syndrome pattern corresponding to a double or multi bit error is the linear sum of the error patterns of the two or more erroneous bits. Thus the number of 1's in the first r bits of a syndrome pattern can exceed m only due to two more erroneous bits in a code word.

Lemma 3: A syndrome pattern with 00 at the two least significant bits indicates a double bit error if the recomputed mod-3 residue bits of the first *r* bits are not 00.

Proof: The last two bits ($m_0\ m_1$) in a column are 00 only if the mod-3 residue check bits of the first *r* bits is a multiple of 3. The syndrome bits for a double bit error in the proposed scheme as in the Hsiao code, is the linear sum of the two error patterns (columns) in the PCM for the individual erroneous bits. The last two bits in the syndrome pattern will be 00, only if $m_0\ m_1$ bits of the error patterns are identical i.e. 00, 01 or 10. In the absence of a double bit error the residue of the first *r* bits in the syndrome pattern should be 00, and thus be the same as the last two bits of the pattern. If the linear sum of two-error patterns result in a pattern in which the residue bits derived from the first *r* bits do not match the last two bits, the presence of a double bit error is identified. However, in some cases the linear sum of two error patterns may produce a syndrome that can be mistaken as the error pattern of a single bit error.

3. Single Error Correction and Double Error Detection Procedure

A procedure for correcting single bit errors and detecting double bit errors in an encoded word based on the proposed coding technique is given below:

i. Calculate the syndrome s (= $s_0 \ldots s_{r-1}\ m_0\ m_1$)
ii. If $m_0\ m_1 = 11$, there is a double-bit error in the information bits of the word, exit. Else
iii. If $m_0\ m_1 = 00$ and $s_0 \ldots s_{r-1}$ bits contain only a single 1, a check bit identified by the syndrome bits is erroneous, exit. Else
iv. If $m_0\ m_1 = 00$, compute the mod-3 residue of the syndrome bits $s_0 \ldots s_{r-1;}$ identify these as $m'_0\ m'_1$
v. If $m'_0\ m'_1 \neq 00$, there is a double bit error in the code word, exit. Else
vi. If $s_0 \ldots s_{r-1} = 11 \ldots 1$, there is a multi-bit error in the code word, exit. Else
vii. An information bit is erroneous. Decode $s_0 \ldots s_{r-1}$ to identify the erroneous bit

A block diagram of the decoder circuit for the proposed code is shown in Fig.3. The syndrome bits $s_0 \ldots s_{r-1}\ m_0\ m_1$ are calculated by EX-Oring the actual check bits with the check bits recalculated from information bits. The bits $s_0 \ldots s_{r-1}$ of the syndrome pattern feed a mod-3 residue generator circuit.

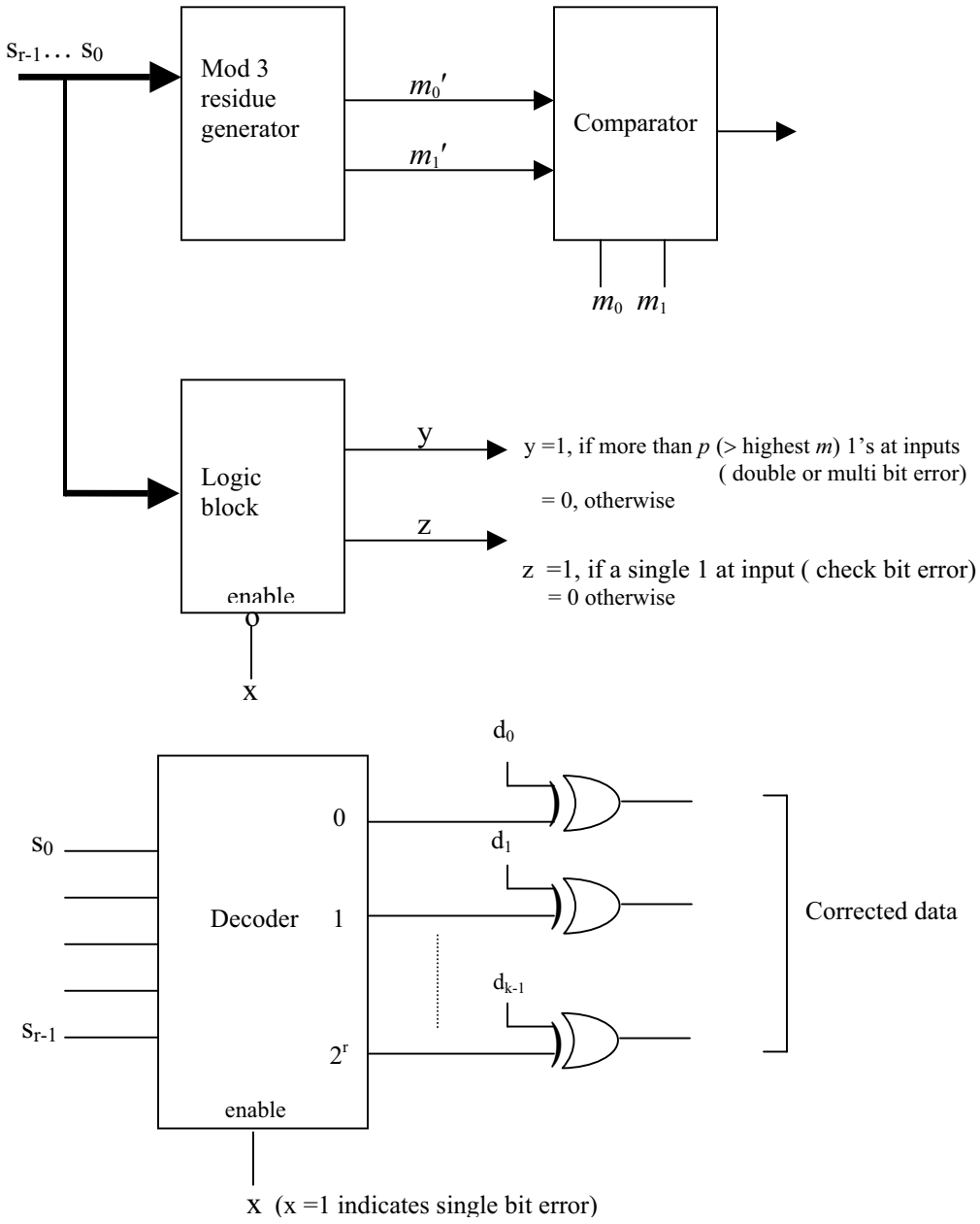

Figure. 3. Error decoding and correcting circuit

The recalculated residue bits m'_0 m'_1 are compared with the last two bits of the syndrome bits i.e. m_0 m_1. The output x of the comparator circuit is 1 if m'_0 $m'_1 = m_0$ m_1 indicating the presence of a single bit error. On the other hand if m_0 $m_1 = 00$ and m'_0 $m'_1 \neq 00$, the presence of a double bit error is indicted and output x is set to 0. The output x of the

comparator drives the enable input of the decoder. If x =1 the syndrome bits are decoded to identify and correct the erroneous bit. It can be seen in Fig.3 that bit s_0 …..s_{r-1} feed a logic block that has two outputs y and z, and an active-low enable input driven by x. hen x = 0, output y produces a 1 if s_0 …..s_{r-1} are all 1's, which indicates a double bit or a multibit error. Note that if m_0 m_1 = 11, they will not be equal to m'_0 m'_1 and y will be set to 1 thereby indicating the presence of a double bit error. A check bit error in a code word identified by a single 1 in a code in syndrome bits s_0 …..$s_{r-1,}$ results in an output of 1 at z.

An advantage of the proposed code is the number of 1's in the PCM is fewer than that in the Hsiao code except when k= 64 in which case the number of 1's are the same as shown in Table 1.

Table. 1 Comparison of the number of 1's in the proposed code and Hsiao code

Information bits	Check bits	#1's in the proposed code	#1's in the Hsiao Code
16	8	48	54
24	8	79	86
32	9	102	103
48	9	164	177
64	10	216	216
128	11	461	481

4. Conclusion

The main feature of the proposed coding technique is the reduced number of 1's in the PCM. This results in simpler encoding and decoding circuits. In addition the decoding of a syndrome pattern to identify the presence of a double bit error is considerably simplified. When the last two bits of a syndrome pattern are 11 a double bit error is immediately identified, no further decoding is necessary. When the last two bits are 00,01 or 10, the decoding circuitry can locate and correct an erroneous bit or indicate the presence of a double/multi-bit error.

5. References

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