Project_Top Project Status (12/11/2021 - 23:33:28)			
Project File:	Project.xise	**Parser Errors:**	No Errors
Module Name:	Project_Top	**Implementation State:**	Programming File Generated
Target Device:	xc7a100t-1fgg676	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	31 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	87	126,800	1%	
Number used as Flip Flops	87			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	149	63,400	1%	
Number used as logic	138	63,400	1%	
Number using O6 output only	60			
Number using O5 output only	45			
Number using O5 and O6	33			
Number used as ROM	0			
Number used as Memory	8	19,000	1%	
Number used as Dual Port RAM	8			
Number using O6 output only	4			
Number using O5 output only	0			
Number using O5 and O6	4			
Number used as Single Port RAM	0			
Number used as Shift Register	0			
Number used exclusively as route-thrus	3			
Number with same-slice register load	0			
Number with same-slice carry load	3			
Number with other load	0			
Number of occupied Slices	61	15,850	1%	
Number of LUT Flip Flop pairs used	152			
Number with an unused Flip Flop	69	152	45%	
Number with an unused LUT	3	152	1%	
Number of fully used LUT-FF pairs	80	152	52%	
Number of unique control sets	15			

Number of slice register sites lost to control set restrictions	61	126,800	1%	
Number of bonded IOBs	42	300	14%	
Number of LOCed IOBs	42	42	100%	
Number of RAMB36E1/FIFO36E1s	0	135	0%	
Number of RAMB18E1/FIFO18E1s	0	270	0%	
Number of BUFG/BUFGCTRLs	4	32	12%	
Number used as BUFGs	4			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYs	0	300	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	0	300	0%	
Number of ODELAYE2/ODELAYE2_FINEDELAYs	0			
Number of OLOGICE2/OLOGICE3/OSERDESE2s	1	300	1%	
Number used as OLOGICE2s	1			
Number used as OLOGICE3s	0			
Number used as OSERDESE2s	0			
Number of PHASER_IN/PHASER_IN_PHYs	0	24	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	24	0%	
Number of BSCANs	0	4	0%	
Number of BUFHCEs	0	96	0%	
Number of BUFRs	0	24	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTs	0	1	0%	
Number of DSP48E1s	0	240	0%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of GTPE2_CHANNELs	0	8	0%	
Number of IBUFDS_GTE2s	0	4	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	6	0%	
Number of IN_FIFOs	0	24	0%	
Number of MMCME2_ADVs	0	6	0%	
Number of OUT_FIFOs	0	24	0%	
Number of PCIE_2_1s	0	1	0%	
Number of PHASER_REFs	0	6	0%	
Number of PHY_CONTROLs	0	6	0%	
Number of PLLE2_ADVs	0	6	0%	
Number of STARTUPs	0	1	0%	
Number of XADCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.52			

Performance Summary [-]

Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Dec 12 12:52:07 2021	0	24 Warnings (0 new)	13 Infos (0 new)
Translation Report	Current	Sun Dec 12 12:52:15 2021	0	0	0
Map Report	Current	Sun Dec 12 12:52:49 2021	0	2 Warnings (0 new)	9 Infos (0 new)
Place and Route Report	Current	Sun Dec 12 12:53:13 2021	0	3 Warnings (0 new)	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Sun Dec 12 12:53:27 2021	0	0	4 Infos (0 new)
Bitgen Report	Current	Sun Dec 12 12:53:56 2021	0	2 Warnings (0 new)	1 Info (0 new)

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	Sun Dec 12 12:53:58 2021	
WebTalk Log File	Current	Sun Dec 12 12:53:59 2021	

Date Generated: 12/13/2021 - 14:11:58