

# Jet™ PLL

Revision 0.9.0-41360

May 6, 2015



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## 20 Jet™PLL

### 20.1 Overview

The JET PLL is a patented hybrid PLL designed for audio applications where in-band phase noise is of concern. The JET PLL is available in a number of chips and as a licensable IP block.

- Jitter attenuation: > 60dB above 100Hz
- Reference event range: 15Hz – 13MHz
- Output frequency range: 15.8MHz – 27.7MHz (typically 512 fs)
- Output frame rate: (30kHz – 54KHz)
- Period jitter: < 50ps RMS
- Baseband Jitter: < 20ps RMS
- Wideband jitter: <200ps RMS
- Configurable operation
- Extended status information

### 20.2 Module Configuration

**Table 20.1 JetPLL module base address**

Base address	Description
0xC4001000	DICE3_JET – Jet™PLL Module

For a detailed description and operating principle, see the “*JET PLL Advanced Parameter Guide*” document.

The tables below enumerate the registers that are implemented in the DICE III, TDC30xx family of chips.

**Table 20.2 JetPLL Control register summary**

Address Offset	Register	Bit	Reset	Dir	Description
0x0000	CAF_ENABLE	1	1	RW	Enables the PLL clock outputs
0x0008	COAST	1	0	RW	Enables Coasting at the last NCO value when 1
0x0018	REF_SEL	5	1	RW	Selects which source reference is used (see below)
0x0028	RDIV	16	0	RW	The clock pre divider (forward)
0x002c	THRTL_R	1	0	RW	Prescale by 32
0x0044	GRAVITY	1	1	RW	Makes the clock gravitate down when unlocked
0x0058	U_THR	8	64	RW	Unlock threshold
0x0060	BW_F	4	4	RW	Loop bandwidth floor. Enforced while the loop is locked.
0x0064	BW_C	4	9	RW	Loop bandwidth ceiling. Acquisition mode.
0x0068	SHP_F	2	2	RW	Acquisition filter shape
0x006c	SHP_V	2	3	RW	Locked state filter shape
0x0070	MAX_SL_F	4	15	RW	Max acquisition state slew rate
0x0074	MAX_SL_V	4	15	RW	Max locked state slew rate
0x0078	DCNT_LIN	3	4	RW	Linear descent rate
0x007c	DCNT_EXP	3	4	RW	Exponential descent rate
0x0088	LSE_THR	8	16	RW	Threshold for 'loose' detection
0x0098	MIN_PER	8	58	RW	Minimum period (highest frequency) to lock to
0x009c	MAX_PER	8	111	RW	Maximum period (lowest frequency) to lock to.
0x00b4	NDIV_E	12	0	RW	Feedback divider (multiplies refEvent)
0x00c0	PHSE_LAG	11	0	RW	Deliberate phase offset between ref. and outputs
0x0110	UNBND_I	1	0	RW	Unbind frame sync.

**Table 20.3 JetPLL Source Reference selections**

Source	Description
0	Use internal JET_CLK/2
1	Use clock controller selection

**Table 20.4 JetPLL Status register summary**

Address Offset	Register	Bit	Reset	Dir	Description
0x0280	FAM_ID	16	"SB"	R	Identifies the family. "Standard Block"
0x0284	FRM_ID	16	"??"	R	Identifies customer form.
0x0288	REV_ID	16	" 0"	R	Identifies revision 0
0x028c	INST_ID	16	0xAA01	R	Identifies this instance.
0x02c0	RES_EX	4	7	W	Resolution of period measurements (see below).
0x02c4	PUNC_MP	1	-*	W	Punctuate a new measurement
0x02cc	MTR_PER	16	-	R	Last detected averaged period of reference.
0x02d0	MAX_MP	16	-	R	Greatest period measured.
0x02d4	MAX_MP_CLR	16	-	R	Greatest period measured. Read will clear.
0x02d8	MIN_MP	16	-	R	Smallest period measured.
0x02dc	MIN_MP_CLR	16	-	R	Smallest period measured. Read will clear.
0x0300	TICK_RATE		-	W	See below.
0x0304	TURN_RATE				
0x0308	MAIN_STAT	16	-	R	Main status bits ( <a href="#">see below</a> )
0x030c	MAIN_STAT_CLR	16	-	R	Main Status bits, read will clear sticky bits which are enabled.
0x0320	DET_RAISE	16	0	W	Sticky bit is set on positive edge.
0x0324	DET_FALL	16	0	W	Sticky bit is set on negative edge.
0x0328	STICK_STAT	16	-	RW*	Sticky bits, write with bit set will clear.
0x032c	STICK_STAT_CLR	16	-	R	Sticky bits, read will clear sticky bits which are enabled.
0x0350	IRQ	16	0	W	Enable sticky bits to generate interrupt.
0x038c	NCO_PER	16	-	R	Current NCO period.
0x0390	MAX_NP	16	-	R	The greatest NCO value since last cleared.
0x0394	MAX_NP_CLR	16	-	R	As greatest_np . Read will clear.
0x0398	MIN_NP	16	-	R	The smallest NCO value since last clear.
0x039c	MIN_NP_CLR	16	-	R	As smallest_np. Read will clear.

**Table 20.5 JetPLL Resolution of Period Measurements**

Value		Description
0	JET_RES_EX_512EVT	Count time for 512 events
1	JET_RES_EX_256EVT	Count time for 256 events
2	JET_RES_EX_128EVT	Count time for 128 events
3	JET_RES_EX_64EVT	Count time for 64 events
4	JET_RES_EX_32EVT	Count time for 32 events
5	JET_RES_EX_16EVT	Count time for 16 events
6	JET_RES_EX_8EVT	Count time for 8 events
7	JET_RES_EX_4EVT	Count time for 4 events
8	JET_RES_EX_2EVT	Count time for 2 events
9	JET_RES_EX_NOAVG	
10	JET_RES_EX_2CLK	Count in steps of $2 \cdot T_{mclk} \sim 40\text{ns}$
11	JET_RES_EX_4CLK	Count in steps of $4 \cdot T_{mclk} \sim 80\text{ns}$
12	JET_RES_EX_8CLK	Count in steps of $8 \cdot T_{mclk} \sim 160\text{ns}$
13	JET_RES_EX_16CLK	Count in steps of $16 \cdot T_{mclk} \sim 320\text{ns}$
14	JET_RES_EX_32CLK	Count in steps of $32 \cdot T_{mclk} \sim 640\text{ns}$
15	JET_RES_EX_64CLK	Count in steps of $64 \cdot T_{mclk} \sim 1280\text{ns}$

When the clock state machine is in acquisition mode, use NOAVG. This will work from 770Hz and up. For slower source rates consider using the multiple clock modes. After the source has determined the range, the clock FSM will choose the appropriate precision.

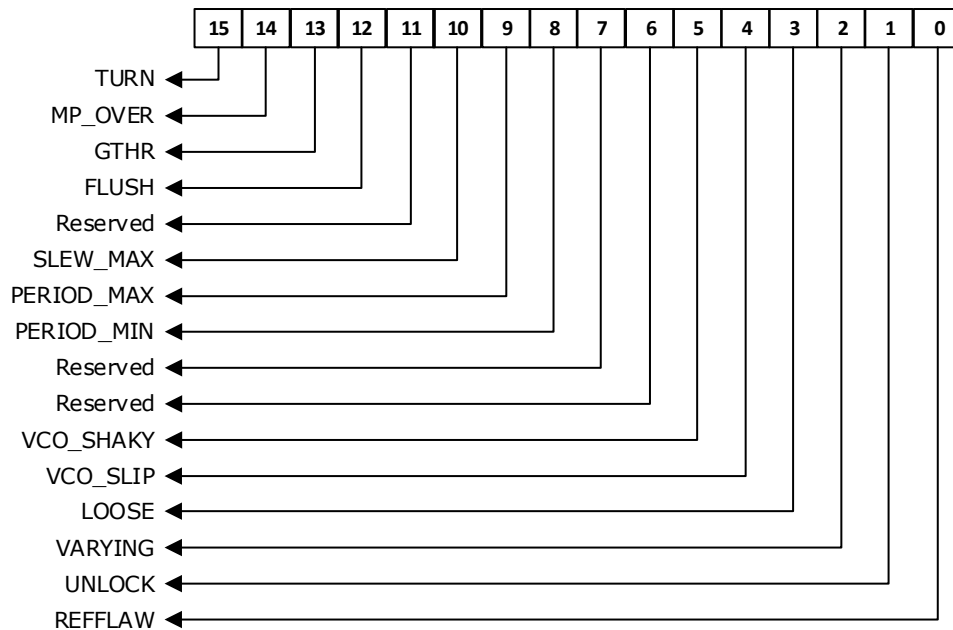


## 20.3 JetPLL Main Status Register – JET\_MAIN\_STAT

Address offset: 0x0308

JET\_MAIN\_STAT

Status bits are described below. These bits are mirrored in the JET\_MAIN\_STAT\_CLR register which is at offset 0x030C, where they are cleared on read.



**Table 20.6 JetPLL Main Status Register bit assignments**

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
STAT_TURN	15	0	R	Pulse every TICK or every 3 TICKS
STAT_MP_OVER	14	0	R	High if measured period overflows, clear when reading JET_MAX_MP_CLR
STAT_GTHR	13	0	R	Goes high if measured min/max period is gathered after punc (~40ms), clear at punc
STAT_FLUSH	12	0	R	Pulses high when a period is gathered after punc, clear at punc
Reserved	11	0	N/A	Reserved
STAT_SLEW_MAX	10	0	R	high when the NCO is at max slew
PERIOD_MAX	9	0	R	high when the NCO is at max end stop
PERIOD_MIN	8	0	R	high when the NCO is at min end stop
Reserved	7	0	R	Reserved
Reserved	6	0	R	Reserved
VCO_SHAKY	5	0	R	The VCO loop hits linearity limit
VCO_SLIP	4	0	R	The VCO loop unlocked

Name	Bit	Reset	Dir	Description
LOOSE	3	0	R	Ref time is off from NCO by loose threshold
VARYING	2	0	R	The Numeric Loop is in acquisition mode.
UNLOCK	1	0	R	If phase wraps or ref time is off from NCO by unlock threshold
REFFLAW	0	0	R	The reference is varying more than +/- 33% from edge to edge, or ref is missing. When using coast or auto coast without GRAVITY: if the ref. is removed, only this signal will indicate that.

## 20.4 Revisions

**Table 20.7 Document revision history**

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication