Remap and Pause Controller

Revision 0.9.0-41360

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10 Remap and Pause Controller

10.1 Overview

The remap and pause controller provides control of the system boot behavior and low-power wait for interrupt mode.

10.2 Programmer's model

The base address of the remap and pause controller memory is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed. ***Table 10.1*** lists the remap and pause controller registers in base offset order.

10.3 Module Configuration

Table 10.1 Remap and Pause register summary

Address	Register	Description
0xC8000000	HAL_DICE3_REMAP_PAUSE	*Pause Register*
0xC8000004	HAL_DICE3_REMAP_REMAP	*Remap Register*
0xC8000008	HAL_DICE3_REMAP_RESET_STATUS	*Reset Status Register*
0xC800000C	HAL_DICE3_TIMER_RESET_STATUS_CLR	*Reset Status Clear Register*

10.3.1 Pause Register – HAL_DICE3_REMAP_PAUSE

Address: 0xC8000000 HAL_DICE3_REMAP_PAUSE

Any write to this location sets the pause output HIGH. The exact effect of writing to this location is not defined, but typically this prevents the processor from fetching further instructions until the receipt of an interrupt of a power-on reset.

10.3.2 Remap Register – HAL_DICE3_REMAP_REMAP

Address: 0xC8000004 HAL_DICE3_REMAP_REMAP

Bit 0 of the HAL_DICE3_REMAP_REMAP register drives the remap output. This is typically used to change the memory map from that required during boot-up to that for normal operation.

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Table 10.2 Remap Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
REMAP	0	0	RW	Set REMAP output.

10.3.3 Reset Status Register – HAL_DICE3_REMAP_RESET_STATUS

Address: 0xC8000008 HAL_DICE3_REMAP_RESET_STATUS

The HAL_DICE3_REMAP_RESET_STATUS register provides the reset status of the system. Only bit 0 is defined in this specification, and provides the **PRESETn** status:

- set HIGH at reset
- set LOW through the HAL_DICE3_TIMER_RESET_STATUS_CLR register.

Table 10.3 Reset Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
ResetStatus	0	**PRESETn**	R	Reset status of the system.

10.3.4 Reset Status Clear Register – HAL_DICE3_TIMER_RESET_STATUS_CLR

Address: 0xC800000C HAL_DICE3_TIMER_RESET_STATUS_CLR

The HAL_DICE3_TIMER_RESET_STATUS_CLR Register location clears bits in the HAL_DICE3_REMAP_RESET_STATUS register.

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10.4 Revisions

Table 10.4 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

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