InS

Receivers and Transmitters

Revision 0.9.0-41360

May 6, 2015

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21 InS Receivers and Transmitters

21.1 Overview

TCD3xxx has one InS Rx and one InS Tx module each having 16 lines, and a total of 128 router channels.

The InS is tightly coupled to the lines in the APORT. These lines are active when the corresponding pins in HAL_DICE3_SYS_CTL_MUXn are configured as InS Audio. The Tx lines go to the even ports and the Rx lines go to the odd ports, i.e. Tx line 0 goes to APORT0, Tx line 1 goes to APORT2, etc. and the Rx signals come from APORT1 for Rx line 0 and APORT3 for Rx line 1, etc.

The way the channels relate to the router map is that they pack so for example if you configure:

Line0 off

Line 1 2 ch

Line 2 4 ch

Line 3 8 ch

Line 4 2 ch

They will pack so:

Router ch 0-1 -> line 1

Router ch 2-5 -> line 2

Router ch 6->13 -> line 3

Router ch 14-15 -> line 4

The biggest configuration is 16 lines of 8 channels which is router ch 0-127

The InS module does not know or care how the APORT mux is programmed so even if a given line is programmed to be something else on the pin the packing will still only depend on how the lines are programmed in the InS.

Limitations:

At low and mid rates the lines can be programmed to 2, 4 or 8 channels per line

At high rates the lines can be programmed to 2 or 4 channels per line.

21.2 InS Receiver

21.2.1 Module Configuration

The InS Receivers are addressed through 1 base address:

Table 21.1 InS Receiver base address

Base address	Description
0xC4000500	DICE3_INS_RX – InS Receivers

Table 21.2 InS Receiver register summary

Address Offset	Register	Description
0x0000	INS_RX_LCR0	*InS Rx Line Control Register 0*
0x0004	INS_RX_LCR1	InS Rx Line Control Register 1
…	…	…
0x003C	INS_RX_LCR15	InS Rx Line Control Register 15

21.2.2 INS Rx Line Control Register 0 – INS_RX_LCR0

Address offset: 0x0000 INS_RX_LCR0

This register is typical of 16 registers, one for each InS Rx line.

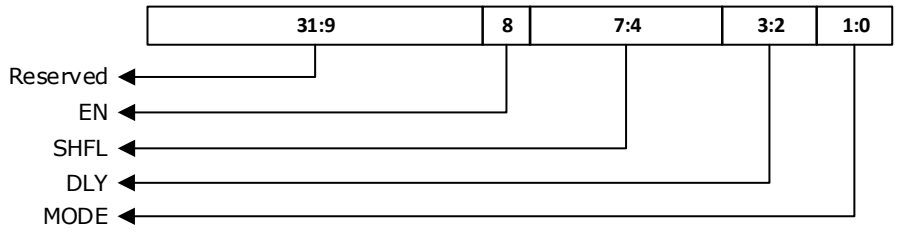

Table 21.3 INS Rx Line Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:9	0	N/A	Reserved
EN	8	0	R/W	This bit enables the operation of the particular Rx instance in the InS module. 0: Rx instance disabled 1: Rx instance enabled

Name	Bit	Reset	Dir	Description
SHFL	7:4	0	R/W	See Data Shuffle table
DLY	3:2	0	R/W	This field selects the delay from the positive edge of sys_1fs to the beginning of data reception. 00: no delay 01: 1 bclk delay 10: 2 bclk delay 11: 3 bclk delay
MODE	1:0	0	R/W	This field selects the mode for the Rx instance. 00: I2S 01: I4S 10: I8S 11: reserved

Table 21.4 Data Shuffle

SHFL values	Order of transmission
0000	data[31:0] -> b31,..,b8, b7,..,b0
0001	data[31:0] -> b31,..,b8, b0,..,b7
0010	data[31:0] -> b8,..,b31, b7,..,b0
0011	data[31:0] -> b8,..,b31, b0,..,b7
0100	data[31:0] -> b7,..,b0, b31,..,b8
0101	data[31:0] -> b7,..,b0, b8,..,b31
0110	data[31:0] -> b0,..,b7, b31,..,b8
0111	data[31:0] -> b0,..,b7, b8,..,b31
1000	data[31:0] -> b31,..,b24, b23,..,b0
1001	data[31:0] -> b31,..,b24, b0,..,b23
1010	data[31:0] -> b24,..,b31, b23,..,b0
1011	data[31:0] -> b24,..,b31, b0,..,b23
1100	data[31:0] -> b23,..,b0, b31,..,b24
1101	data[31:0] -> b23,..,b0, b24,..,b31
1110	data[31:0] -> b0,..,b23, b31,..,b24
1111	data[31:0] -> b0,..,b23, b24,..,b31

21.3 InS Transmitter

21.3.1 Module Configuration

The InS Transmitters are addressed through 1 base address:

Table 21.5 InS Transmitter base address

Base address	Description
0xC4000600	DICE3_INS_TX – InS Transmitters

Table 21.6 InS Register summary

Address Offset	Register	Description
0x0000	INS_TX_LCR0	*InS Tx Line Control Register 0*
0x0004	INS_TX_LCR1	InS Tx Line Control Register 1
…	…	…
0x003C	INS_TX_LCR15	InS Tx Line Control Register 15
0x0040	INS_TX_CCR0	*InS Tx Clock Control Register 0*
0x0044	INS_TX_CCR1	InS Tx Clock Control Register 1
0x0048	INS_TX_CCR2	InS Tx Clock Control Register 2
0x004C	INS_TX_MUTE	*InS Tx Mute Control Register*

21.3.2 INS Tx Line Control Register 0 – INS_TX_LCR0

Address offset: 0x0000 INS_TX_LCR0

This register is typical of 16 registers, one for each InS Tx line.

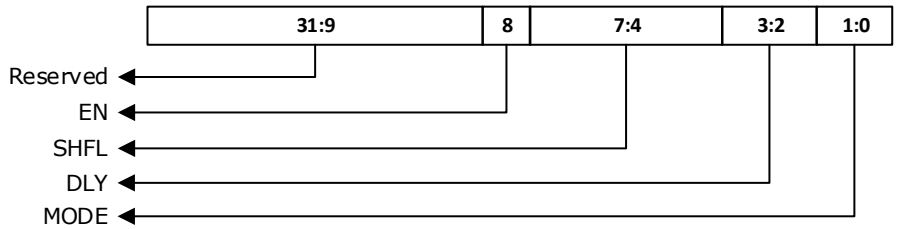

Table 21.7 INS Tx Line Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:9	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
EN	8	0	R/W	This bit enables the operation of the particular Tx instance in the InS module. 0: Tx instance disabled 1: Tx instance enabled
SHFL	7:4	0	R/W	See Data Shuffle table
DLY	3:2	0	R/W	This field selects the delay from the positive edge of sys_1fs to the beginning of data reception. 00: no delay 01: 1 bclk delay 10: 2 bclk delay 11: 3 bclk delay
MODE	1:0	0	R/W	This field selects the mode for the Tx instance. 00: I2S 01: I4S 10: I8S 11: reserved

21.3.3 INS Clock Control Register 0 – INS_TX_CCR0

Address offset: 0x0040, 0x0044, 0x0048 INS_TX_CCR0

This register is typical of 3 registers.

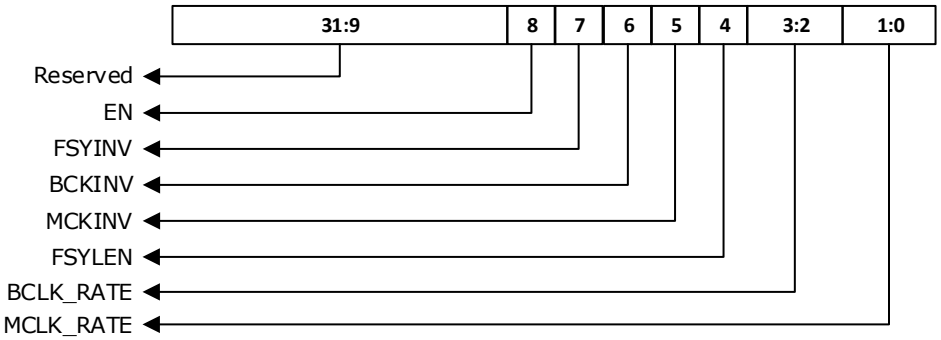

Table 21.8 INS Tx Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:9	0	N/A	Reserved
EN	8	0	R/W	Enables the clock interface. If disabled, all outputs are 0.
FSYINV	7	0	R/W	0: positive edge aligned with 1fs frame 1: negative edge aligned with 1fs frame

Name	Bit	Reset	Dir	Description
BCKINV	6	0	R/W	0: positive edge aligned with 1fs frame 1: negative edge aligned with 1fs frame
MCKINV	5	0	R/W	0: positive edge aligned with 1fs frame 1: negative edge aligned with 1fs frame
FSYLEN	4	0	R/W	0: 1 bclk length 1: 32 bclk length
BCLK_RATE	3:2	0	R/W	0: 64fs 1: 128fs 2: 256fs 3: reserved
MCLK_RATE	1:0	0	R/W	0: 256br 1: 512br 2: 128fs 3: 256fs

21.3.4 INS Mute Control Register – INS_TX_MUTE

Address offset: 0x004C INS_TX_MUTE

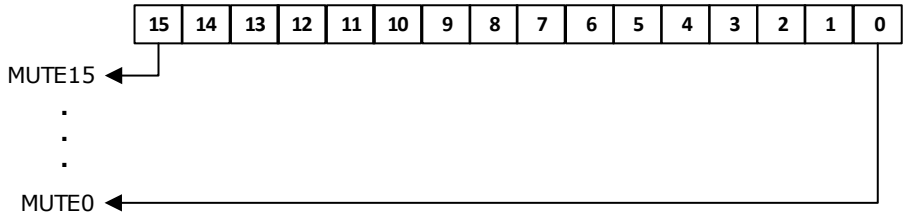

Table 21.9 INS Mute Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
MUTE15	15	0	R/W	0: Tx line 15 not muted 1: Tx line 15 (all channels) muted
. . .				
MUTE0	0	0	R/W	0: Tx line 0 not muted 1: Tx line 0 (all channels) muted

21.4 Revisions

Table 21.10 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

