Timers

Quad Timer Unit

Revision 0.9.0-41360

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11 Quad Timer

11.1 Overview

Two instances of a Dual-Timer module are available. Each dual-timer module consists of two programmable 32/16-bit down counters that can generate interrupts on reaching zero. A Timer module can be programmed for a 32-bit or 16-bit counter size and one of three timer modes using the Control Register.

The operation of each Timer module is identical. It has one of three timer modes:

- **Free-running**

  The counter wraps after reaching its zero value, and continues to count down from the maximum value. This is the default mode.

- **Periodic**

  The counter generates an interrupt at a constant interval, reloading the original value after wrapping past zero.

- **One-shot**

  The counter generates an interrupt once. When the counter reaches zero, it halts until reprogrammed by the user. This can be achieved by either clearing the One Shot Count bit in the control register, in which case the count proceeds according to the selection of Free-running or Periodic mode, or by writing a new value to the Load Value register.

11.2 Operation

Each timer has an identical set of registers as shown in *Table 11.2* The operation of each timer is identical. The timer is loaded by writing to the load register and, if enabled, counts down to zero. When a counter is already running, writing to the load register causes the counter to immediately restart at the new value. Writing to the background load value has no effect on the current count. The counter continues to decrement to zero, and then recommences from the new load value, if in periodic mode, and one shot mode is not selected.

When zero is reached, an interrupt is generated. The interrupt can be cleared by writing to the clear register. If One Shot Mode is selected, the counter halts on reaching zero until One Shot Mode is deselected, or a new Load value is written. Otherwise, after reaching a zero count, if the timer is operating in free-running mode it continues to decrement from its maximum value. If periodic timer mode is selected, the timer reloads the count value from the Load Register and continues to decrement. In this mode the counter effectively generates a periodic interrupt. The mode is selected by a bit in the Control Register. At any point, the current counter value can be read from the Current Value register. The counter is enabled by a bit in the Control Register. At reset, the counter is disabled, the interrupt is cleared, and the load register is set to zero. The mode and prescale values are set to free-running, and clock divide of 1 respectively.

Figure 11.1 shows a block diagram of the free-running timer module.

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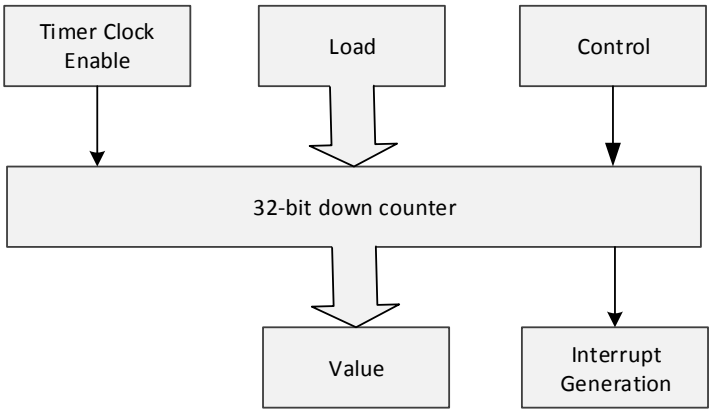

Figure 11.1 Free-running timer block

11.3 Module Configuration

Four logical timers are available as two physical instances of the dual-input timer module. The four timers are organized according to their base addresses as shown in *Table 11.1*.

Table 11.1 Timer base addresses

Base address	Timer number (n)
0xC2000000	0
0xC2000020	1
0xC3000000	2
0xC3000020	3

Logical timer registers are described below by their offsets from their respective base addresses.

Table 11.2 Timer register summary

Address Offset	Register	Description
0x0000	HAL_DICE3_TIMERn_LOAD	*Load Register*
0x0004	HAL_DICE3_TIMERn_VALUE	*Current Value Register*
0x0008	HAL_DICE3_TIMERn_CTRL	*Timer Control Register*
0x000C	HAL_DICE3_TIMERn_INT_CLR	*Interrupt Clear Register*
0x0010	HAL_DICE3_TIMERn_RIS	*Raw Interrupt Status Register*
0x0014	HAL_DICE3_TIMERn_MIS	*Interrupt Status Register*
0x0018	HAL_DICE3_TIMERn_BGL	*Background Load Register*

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11.3.1 Load Register – HAL_DICE3_TIMERn_LOAD

Address offset: 0x0000 HAL_DICE3_TIMERn_LOAD

The HAL_DICE3_TIMERn_LOAD register is a 32-bit register containing the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches zero.

When this register is written to directly, the current count is reset to the new value immediately, or when the timer is enabled if it was not already enabled.

The value in this register is also overwritten if the HAL_DICE3_TIMERn_BGL register is written to, but the current count is not immediately affected.

If values are written to both the HAL_DICE3_TIMERn_LOAD and HAL_DICE3_TIMERn_BGL registers before an enabled rising edge on the timer clock, the following occurs:

- On the next enabled timer clock edge, the value written to the HAL_DICE3_TIMERn_LOAD value replaces the current count value.
- Following this, each time the counter reaches zero, the current count value is reset to the value written to HAL_DICE3_TIMERn_BGL.

Reading from the HAL_DICE3_TIMERn_LOAD register at any time after the two writes have occurred retrieves the value written to HAL_DICE3_TIMERn_BGL. That is, the value read from HAL_DICE3_TIMERn_LOAD is always the value that takes effect for Periodic mode after the next time the counter reaches zero.

11.3.2 Current Value Register – HAL_DICE3_TIMERn_VALUE

Address offset: 0x0004 HAL_DICE3_TIMERn_VALUE

The HAL_DICE3_TIMER_VALUE register gives the current value of the decrementing counter.

11.3.3 Timer Control Register – HAL_DICE3_TIMERn_CTRL

Address offset: 0x0008 HAL_DICE3_TIMERn_CTRL

The HAL_DICE3_TIMERn_CTRL register is a read/write register. The following figures show the register bit assignments.

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Table 11.3 Timer Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
CTRL_EN	7	0	RW	Enable bit. 0: Timer disabled 1: Timer enabled
CTRL_PERIODIC	6	0	RW	Mode bit. 0: Timer is in free-running mode 1: Timer is in periodic mode
CTRL_INTEN	5	1	RW	Interrupt enable bit. 0: Timer Interrupt disabled 1: Timer Interrupt enabled
Reserved	4	0	RW	Reserved bit, do not modify, and ignore on read.
CTRL_PRSCL_MSK	3:2	0	RW	Prescale bits. 00: clock is divided by 1, default 01: clock is divided by 16 10: clock is divided by 256 11: Undefined, do not use
CTRL_32BIT	1	0	RW	Selects 16/32 bit counter operation.. 0: 16-bit counter 1: 32- bit counter
CTRL_ONSHT	0	0	RW	Selects one-shot or wrapping counter mode. 0: wrapping mode 1: one-shot mode

11.3.4 Interrupt Clear Register – HAL_DICE3_TIMERn_INT_CLR

Address offset: 0x000C HAL_DICE3_TIMERn_INT_CLR

Any write to the HAL_DICE3_TIMERn_INT_CLR register clears the interrupt output from the counter.

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11.3.5 Raw Interrupt Status Register – HAL_DICE3_TIMERn_RIS

Address offset: 0010 HAL_DICE3_TIMERn_RIS

This register is read-only. It indicates the raw interrupt status from the counter. This value is ANDed with the timer interrupt enable bit from the Timer Control Register to create the masked interrupt, which is passed to the interrupt output signal. The following figures show the register bit assignments.

Table 11.4 Timer Raw Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	R	Reserved, read undefined, must read as zeros.
Raw Timer Interrupt	0	0	R	Raw Interrupt Status of the counter. 0: Interrupt cleared 1: Interrupt set

11.3.6 Interrupt Status Register – HAL_DICE3_TIMERn_MIS

Address offset: 0x0014 HAL_DICE3_TIMERn_MIS

The HAL_DICE3_TIMERn_MIS register is read-only. It indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the timer interrupt enable bit from the Timer Control Register, and is the same value that is passed to the interrupt output signal. The following figures show the register bit assignments.

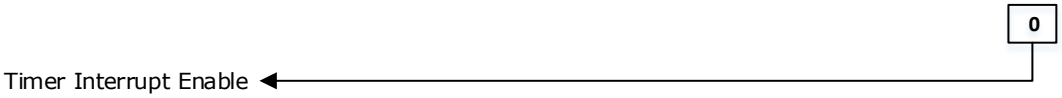

Table 11.5 Timer Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	R	Reserved, read undefined, must read as zeros.
Timer Interrupt Enable	0	0	R	Interrupt Status of the counter. 0: Disabled interrupt status 1**:** Enabled interrupt status from the counter

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11.3.7 Background Load Register – HAL_DICE3_TIMERn_BGL

Address offset: 0x0018 HAL_DICE3_TIMERn_BGL

The HAL_DICE3_TIMERn_BGL register is 32-bits and contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches zero.

This register provides an alternative method of accessing the HAL_DICE3_TIMERn_LOAD Register. The difference is that writes to HAL_DICE3_TIMERn_BGL do not cause the counter to immediately restart from the new value.

Reading from this register returns the same value returned from HAL_DICE3_TIMERn_LOAD. See *Load Register* for more details.

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11.4 Revisions

Table 11.6 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

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