UART

Revision 0.9.0-41360

May 6, 2015

List of Tables

List of Figures

14 UART

14.1 Overview

The UART is similar to an industry-standard 16C650 UART

- Separate 16×8 transmit and 16×12 receive *First-In, First-Out* (FIFO) memory buffers to reduce CPU interrupts.
- Programmable FIFO disabling for 1-byte depth.
- Programmable baud rate generator. This enables division of the reference clock by (1×16) to (65535×16) and generates an internal ×16 clock. The divisor can be a fractional number enabling you to use any clock with a frequency >3.6864MHz as the reference clock.
- Standard asynchronous communication bits (start, stop and parity). These are added prior to transmission and removed on reception.
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts.
- Support for *Direct Memory Access* (DMA).
- False start bit detection.
- Line break generation and detection.
- Fully-programmable serial interface characteristics:
    - data can be 5, 6, 7, or 8 bits
    - even, odd, stick, or no-parity bit generation and detection
    - 1 or 2 stop bit generation
    - baud rate generation, dc up to **UARTCLK**/16

The following key parameters are programmable:

- communication baud rate, integer, and fractional parts
- number of data bits
- number of stop bits
- parity mode
- FIFO enable (16 deep) or disable (1 deep)
- FIFO trigger levels selectable between $^1/_8$, $^1/_4$, $^1/_2$, $^3/_4$, and $^7/_8$

The UART varies from the industry-standard 16C650 UART device as follows:

- receive FIFO trigger levels are $^1/_8$, $^1/_4$, $^1/_2$, $^3/_4$, and $^7/_8$
- transmit FIFO trigger levels are $^1/_8$, $^1/_4$, $^1/_2$, $^3/_4$, and $^7/_8$
- the internal register map address space, and the bit function of each register differ
- the deltas of the modem status signals are not available.
- hardware flow control is not supported. The CTS and RTS signals are not connected to external pins.

The following 16C650 UART features are not supported:

- 1.5 stop bits (1 or 2 stop bits only are supported)
- independent receive clock.

The UART performs:

- serial-to-parallel conversion on data received from a peripheral device
- parallel-to-serial conversion on data transmitted to the peripheral device.

The CPU reads and writes data and control/status information through the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories enabling up to 16-bytes to be stored independently in both transmit and receive modes.

The UART:

- includes a programmable baud rate generator that generates a common transmit and receive internal clock from the UART internal reference clock input, **UARTCLK**
- offers similar functionality to the industry-standard 16C650 UART device
- supports 921600 maximum baud rate

The UART operation and baud rate values are controlled by the *Line Control Register* and the baud rate divisor registers (*Integer Baud Rate Register* and *Fractional Baud Rate Register*).

The UART can generate:

- individually-maskable interrupts from the receive (including timeout), transmit, modem status and error conditions
- a single combined interrupt so that the output is asserted if any of the individual interrupts are asserted, and unmasked
- DMA request signals for interfacing with a *Direct Memory Access* (DMA) controller.

If a framing, parity, or break error occurs during reception, the appropriate error bit is set, and is stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and FIFO data is prevented from being overwritten.

You can program the FIFOs to be 1-byte deep providing a conventional double-buffered UART interface.

14.1.1 UART Block Diagram

Signal names in **bold** in this chapter refer to labels in this diagram.

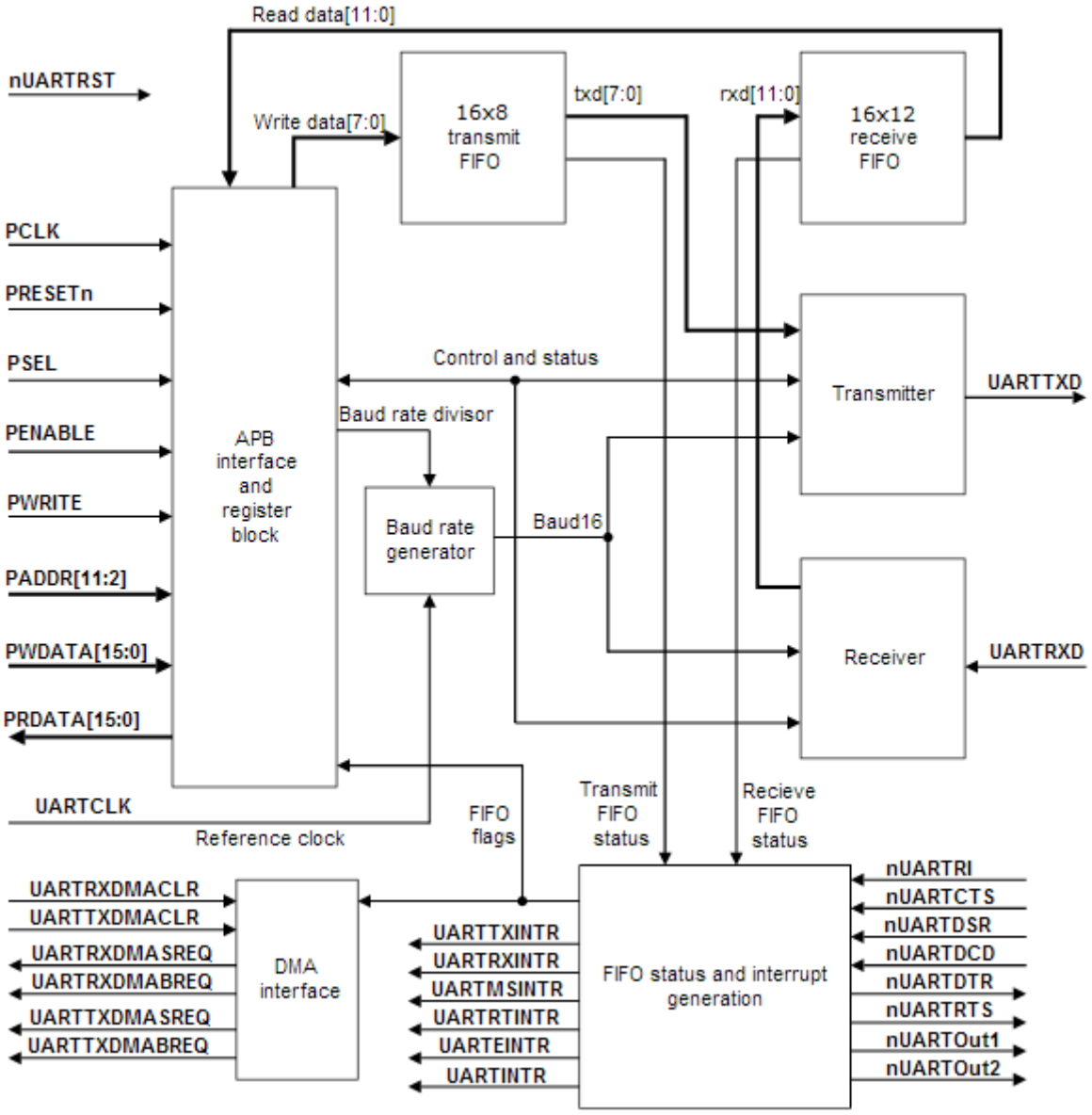

Figure 14.1 UART block diagram

14.1.2 Register block

The register block stores data written, or to be read across the AMBA APB interface.

14.1.3 Baud rate generator

The baud rate generator contains free-running counters that generate the internal ×16 **Baud16** clock. **Baud16** provides timing information for UART transmit and receive control. **Baud16** is a stream of pulses with a width of one **UARTCLK** clock period and a frequency of 16 times the baud rate.

14.1.4 Transmit FIFO

The transmit FIFO is an 8-bit wide, 16 location deep, FIFO memory buffer. CPU data written across the APB interface is stored in the FIFO until read out by the transmit logic. You can disable the transmit FIFO to act like a one-byte holding register.

14.1.5 Receive FIFO

The receive FIFO is a 12-bit wide, 16 location deep, FIFO memory buffer. Received data and corresponding error bits, are stored in the receive FIFO by the receive logic until read out by the CPU across the APB interface. The receive FIFO can be disabled to act like a one-byte holding register.

14.1.6 Transmit logic

The transmit logic performs parallel-to-serial conversion on the data read from the transmit FIFO. Control logic outputs the serial bit stream beginning with a start bit, data bits with the Least Significant Bit (LSB) first, followed by the parity bit, and then the stop bits according to the programmed configuration in control registers.

14.1.7 Receive logic

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Overrun, parity, frame error checking, and line break detection are also performed, and their status accompanies the data that is written to the receive FIFO.

14.1.8 Interrupt generation logic

Individual maskable active HIGH interrupts are generated by the UART. A combined interrupt output is also generated as an OR function of the individual interrupt requests.

You can use the single combined interrupt with a system interrupt controller that provides another level of masking on a per-peripheral basis. This enables you to use modular device drivers that always know where to find the interrupt source control register bits.

You can also use the individual interrupt requests with a system interrupt controller that provides masking for the outputs of each peripheral. In this way, a global interrupt service routine can read the entire set of sources from one wide register in the system interrupt controller. This is attractive where the time to read from the peripheral registers is significant compared to the CPU clock speed in a real-time system.

14.1.9 DMA interface

The UART provides an interface to connect to the DMA controller. This is currently not utilized in support firmware.

14.2 Module Configuration

Each of the two UARTs is independently programmable using duplicate module register sets. The registers are located at the base addresses below.

Table 14.1 UART base addresses

Base address	UART module number
0xC5000000	0
0xC6000000	1

UART registers are described below by their offsets from their respective base addresses.

Table 14.2 UART register summary

Address Offset	Register	Description
0x0000	HAL_DICE3_UART_DR	*UART Data Register*
0x0004	HAL_DICE3_UART_RSR_ECR	*UART Receive Status Register*
0x0018	HAL_DICE3_UART_FR	*UART Flag Register*
0x0024	HAL_DICE3_UART_IBRD	*UART Integer Baud Rate Register*
0x0028	HAL_DICE3_UART_FBRD	*UART Fractional Baud Rate Register*
0x002C	HAL_DICE3_UART_LCR_H	*UART Line Control Register*
0x0030	HAL_DICE3_UART_CR	*UART Control Register*
0x0034	HAL_DICE3_UART_IFLS	*UART Interrupt FIFO Level Select Register*
0x0038	HAL_DICE3_UART_IMSC	*UART Mask Set/Clear Register*
0x003C	HAL_DICE3_UART_RIS	*UART Interrupt Status Register*
0x0040	HAL_DICE3_UART_MIS	*UART Masked Interrupt Status Register*
0x0044	HAL_DICE3_UART_ICR	*UART Interrupt Clear Register*
0x0048	HAL_DICE3_UART_DMACR	*UART DMA Control Register*

14.2.1 UART Data Register – HAL_DICE3_UART_DR

Address offset: 0x0000 HAL_DICE3_UART_DR

The HAL_DICE3_UART_DR register is the data register.

For words to be transmitted:

- if the FIFOs are enabled, data written to this location is pushed onto the transmit FIFO
- if the FIFOs are not enabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO).

The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit (if parity is enabled), and a stop bit. The resultant word is then transmitted.

For received words:

- if the FIFOs are enabled, the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive FIFO
- if the FIFOs are not enabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO).

The received data byte is read by performing reads from the UARTDR Register along with the corresponding status information.

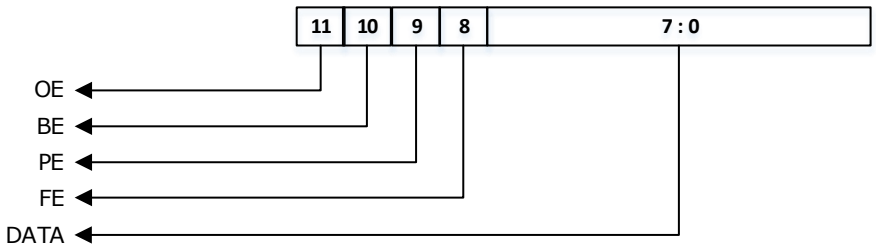

Table 14.3 UART Data Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:12	0	RW	Reserved, read undefined, must read as zeros.
OE	11	0	R	Overrun Error. This bit is set to 1 if data is received and the receive FIFO is already full. This is cleared to 0 once there is an empty space in the FIFO and a new character can be written to it.

Name	Bit	Reset	Dir	Description
BE	10	0	R	Break Error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits). In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state), and the next valid start bit is received.
PE	9	0	R	Parity Error. When set to 1, it indicates that the parity of the received data character does not match the parity that the EPS and SPS bits in the *UART Line Control Register*, HAL_DICE3_UART_LCR_H. In FIFO mode, this error is associated with the character at the top of the FIFO.
FE	8	0	R	Framing Error. When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1). In FIFO mode, this error is associated with the character at the top of the FIFO.
Data	7:0	0	RW	Receive (read) data character. Transmit (write) data character.

Note
You must disable the UART before any of the control registers are reprogrammed. When the UART is disabled in the middle of transmission or reception, it completes the current character before stopping.

14.2.2 UART Receive Status Register/Error Clear Register – HAL_DICE3_UART_ECR

Address offset: 0x0004 HAL_DICE3_UART_RSR_ECR

The HAL_DICE3_UART_RSR_ECR register is the receive status register/error clear register.

Receive status can also be read from the HAL_DICE3_UART_RSR_ECR register. If the status is read from this register, then the status information for break, framing and parity corresponds to the data character read from the *UART Data Register*, HAL_DICE3_UART_DR prior to reading the HAL_DICE3_UART_RSR_ECR Register. The status information for overrun is set immediately when an overrun condition occurs.

A write to the HAL_DICE3_UART_RSR_ECR register clears the framing, parity, break, and overrun errors.

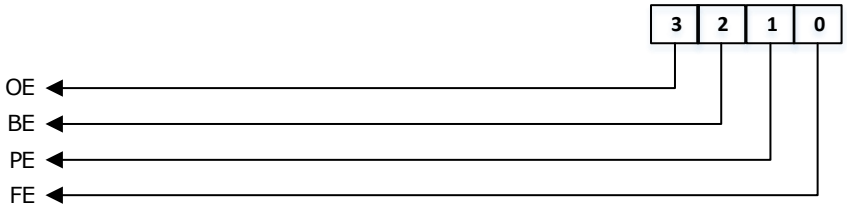

Table 14.4 UART Receive Status Register/Error Clear Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	RW	Reserved, read undefined.
OE	3	0	RW	Overrun error. This bit is set to 1 if data is received and the FIFO is already full. This bit is cleared to 0 by a write to UARTECR. The FIFO contents remain valid because no more data is written when the FIFO is full, only the contents of the shift register are overwritten. The CPU must now read the data, to empty the FIFO.
BE	2	0	RW	Break error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity, and stop bits). This bit is cleared to 0 after a write to UARTECR. In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state) and the next valid start bit is received.
PE	1	0	RW	Parity Error. When set to 1, it indicates that the parity of the received data character does not match the parity that the EPS and SPS bits in the *UART Line Control Register*, HAL_DICE3_UART_LCR_H select. This bit is cleared to 0 by a write to UARTECR. In FIFO mode, this error is associated with the character at the top of the FIFO.
FE	0	0	RW	Framing Error. When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1). This bit is cleared to 0 by a write to UARTECR. In FIFO mode, this error is associated with the character at the top of the FIFO.

Note

The received data character must be read first from the *UART Data Register*, HAL_DICE3_UART_DR before reading the error status associated with that data character from the HAL_DICE3_UART_RSR_ECR register. This read sequence cannot be reversed, because the UARTRSR Register is updated only when a read occurs from the HAL_DICE3_UART_DR register. However, the status information can also be obtained by reading the HAL_DICE3_UART_DR register.

14.2.3 UART Flag Register – HAL_DICE3_UART_FR

Address offset: 0x0018 HAL_DICE3_UART_FR

The HAL_DICE3_UART_FR register is the flag register. After reset FR_TXFF, FR_RXFF, and FR_BUSY are 0, and FR_TXFE and FR_RXFE are 1.

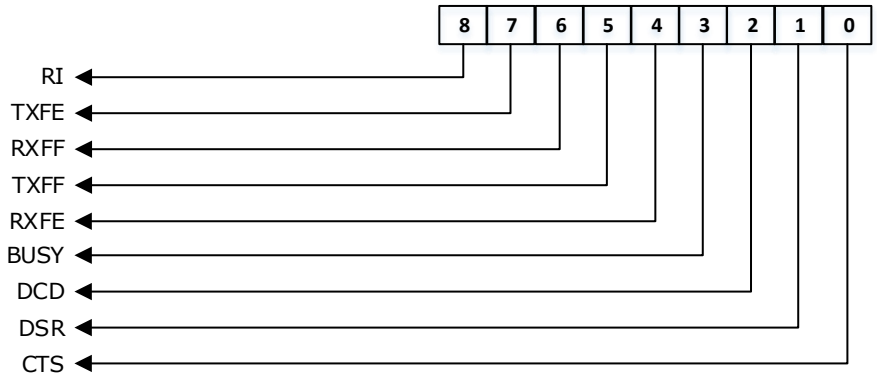

Table 14.5 UART Flag Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:9	0	R	Reserved, do not modify, read as zeros.
RI	8	0	R	Ring Indicator. This bit is the complement of the UART ring indicator, **nUARTRI**, modem status input. That is, the bit is 1 when **nUARTRI** is LOW.
TXFE	7	1	R	Transmit FIFO empty. The meaning of this bit depends on the state of the FEN bit in the *UART Line Control Register*, HAL_DICE3_UART_LCR_H. If the FIFO is disabled, this bit is set when the transmit holding register is empty. If the FIFO is enabled, the TXFE bit is set when the transmit FIFO is empty. This bit does not indicate if there is data in the transmit shift register.

Name	Bit	Reset	Dir	Description
RXFF	6	0	R	Receive FIFO full. The meaning of this bit depends on the state of the FEN bit in the HAL_DICE3_UART_LCR_H register. If the FIFO is disabled, this bit is set when the receive holding register is full. If the FIFO is enabled, the RXFF bit is set when the receive FIFO is full.
TXFF	5	0	R	Transmit FIFO full. The meaning of this bit depends on the state of the FEN bit in the HAL_DICE3_UART_LCR_H register. If the FIFO is disabled, this bit is set when the transmit holding register is full. If the FIFO is enabled, the TXFF bit is set when the transmit FIFO is full.
RXFE	4	1	R	Receive FIFO empty. The meaning of this bit depends on the state of the FEN bit in the HAL_DICE3_UART_LCR_H register. If the FIFO is disabled, this bit is set when the receive holding register is empty. If the FIFO is enabled, the RXFE bit is set when the receive FIFO is empty.
BUSY	3	0	R	UART busy. If this bit is set to 1, the UART is busy transmitting data. This bit remains set until the complete byte, including all the stop bits, has been sent from the shift register. This bit is set as soon as the transmit FIFO becomes non-empty, regardless of whether the UART is enabled or not.
DCD	2	0	R	Data carrier detect. This bit is the complement of the UART data carrier detect, **nUARTDCD**, modem status input. That is, the bit is 1 when **nUARTDCD** is LOW.
DSR	1	0	R	Data set ready. This bit is the complement of the UART data set ready, **nUARTDSR**, modem status input. That is, the bit is 1 when **nUARTDSR** is LOW.
CTS	0	0	R	Clear to send. This bit is the complement of the UART clear to send, **nUARTCTS**, modem status input. That is, the bit is 1 when **nUARTCTS** is LOW. The CTS signal is not connected to external pins, so this function has no effect. Support firmware does not utilize this setting.

14.2.4 UART Integer Baud Rate Register – HAL_DICE3_UART_IBRD

Address offset: 0x0024 HAL_DICE3_UART_IBRD

The HAL_DICE3_UART_IBRD Register is the integer part of the baud rate divisor value.

Table 14.6 UART Integer Baud Rate Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
BAUD_DIVINT	7:0	0	RW	The integer baud rate divisor.

14.2.5 UART Fractional Baud Rate Register – HAL_DICE3_UART_FBRD

Address offset: 0x0028 HAL_DICE3_UART_FBRD

The HAL_DICE3_UART_FBRD register is the fractional part of the baud rate divisor value.

Table 14.7 UART Fractional Baud Rate Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:6	0	RW	Reserved, read undefined, must read as zeros.
BAUD_DIVFRAC	5:0	0	RW	The fractional baud rate divisor.

The baud rate divisor is calculated as follows:

Baud rate divisor BAUDDIV = ($\mathbf{F_{UARTCLK}}$ / (16 × Baud rate))

where $\mathbf{F_{UARTCLK}}$ is the UART reference clock frequency.

The BAUDDIV is comprised of the integer value (BAUD DIVINT) and the fractional value (BAUD DIVFRAC).

Note

- The contents of the HAL_DICE3_UART_IBRD and HAL_DICE3_UART_FBRD registers are not updated until transmission or reception of the current character is complete.

- The minimum divide ratio possible is 1 and the maximum is 65535(2^{16} - 1). That is, HAL_DICE3_UART_IBRD = 0 is invalid and HAL_DICE3_UART_FBRD is ignored when this is the case.
- Similarly, when HAL_DICE3_UART_IBRD = 65535 (that is 0xFFFF), then HAL_DICE3_UART_FBRD must not be greater than zero. If this is exceeded it results in an aborted transmission or reception.

Example Calculating the divisor value

If the required baud rate is 230400 and the **UARTCLK** = 4MHz then:

Baud Rate Divisor = $(4 \times 10^6) / (16 \times 230400) = 1.085$

This means $BRD_I = 1$ and $BRD_F = 0.085$.

Therefore, fractional part, m = integer ($(0.085 \times 64) + 0.5$) = 5

Generated baud rate divider = $1 + {}^{5}/_{64} = 1.078$

Generated baud rate = $(4 \times 10^6) / (16 \times 1.078) = 231911$

Error = $(231911 - 230400) / 230400 \times 100 = 0.656\%$

The maximum error using a 6-bit HAL_DICE3_UART_FBRD register = ${}^{1}/_{64} \times 100 =$ 1.56%. This occurs when m = 1, and the error is cumulative over 64 clock ticks.

Table 14.8 lists some typical bit rates and their corresponding divisors when **UARTCLK** is 7.3728MHz. These values do not use the fractional divider so the value in the HAL_DICE3_UART_FBRD register is zero.

Table 14.8 Typical baud rates and integer divisors when UART clock is 7.3728MHz.

Programmed integer divisor	Bit rate (bps)
0x01	460800
0x02	230400
0x04	115200
0x06	76800
0x08	57600
0x0C	38400
0x18	19200
0x20	14400
0x30	9600

Table 14.9 lists some required bit rates and their corresponding integer and fractional divisor values and generated bit rates when **UARTCLK** is 4MHz.

Table 14.9 Integer and fractional divisors for typical baud rates when UART clock is 4MHz.

Programmed integer divisor	Programmed fractional divisor	Required bit rate (bps)	Generated bit rate (bps)	Error %
0x01	0x05	230400	231911	0.656
0x02	0x0B	115200	115101	0.086
0x03	0x10	76800	76923	0.160
0x06	0x21	38400	38369	0.081
0x11	0x17	14400	14401	0.007
0x68	0x2F	2400	2400	~0

14.2.6 UART Line Control Register – HAL_DICE3_UART_LCR_H

Address offset: 0x002C HAL_DICE3_UART_LCR_H

The HAL_DICE3_UART_LCR_H register is the line control register. This register accesses bits 29 to 22 of the internal UART Line Control Register, UARTLCR.

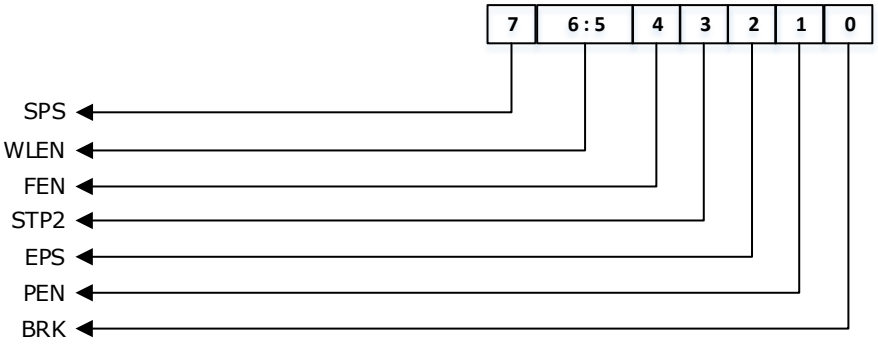

Table 14.10 UART Line Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	15:8	0	RW	Reserved, read as zero.
SPS	7	0	RW	Stick parity select. 0 = stick parity is disabled 1 = either: • if the EPS bit is 0 then the parity bit is transmitted and checked as a 1 • if the EPS bit is 1 then the parity bit is transmitted and checked as a 0. This bit has no effect when the PEN bit disables parity checking and generation. See Table 14.11 for the parity truth table.

Name	Bit	Reset	Dir	Description
WLEN	6:5	0	RW	Word length. These bits indicate the number of data bits transmitted or received in a frame as follows: b11 = 8 bits b10 = 7 bits b01 = 6 bits b00 = 5 bits
FEN	4	0	RW	Enable FIFOs: 0 = FIFOs are disabled (character mode) that is, the FIFOs become 1-byte-deep holding registers 1 = transmit and receive FIFO buffers are enabled (FIFO mode).
STP2	3	0	RW	Two stop bits select. If this bit is set to 1, two stop bits are transmitted at the end of the frame. The receive logic does not check for two stop bits being received.
EPS	2	0	RW	Even parity select. Controls the type of parity the UART uses during transmission and reception: 0 = odd parity. The UART generates or checks for an odd number of 1s in the data and parity bits. 1 = even parity. The UART generates or checks for an even number of 1s in the data and parity bits. This bit has no effect when the PEN bit disables parity checking and generation. See Table 14.11 for the parity truth table.
PEN	1	0	RW	Parity enable: 0 = parity is disabled and no parity bit added to the data frame 1 = parity checking and generation is enabled. See Table 14.11 for the parity truth table.
BRK	0	0	RW	Send break. If this bit is set to 1, a low-level is continually output on the **UARTTXD** output, after completing transmission of the current character. For the proper execution of the break command, the software must set this bit for at least two complete frames. For normal use, this bit must be cleared to 0.

The HAL_DICE3_UART_LCR_H, HAL_DICE3_UART_IBRD, and HAL_DICE3_UART_FBRD registers form the single internal 30-bit wide **UARTLCR** register that is updated on a single write strobe generated by a HAL_DICE3_UART_LCR_H write. So, to internally update the contents of HAL_DICE3_UART_IBRD or HAL_DICE3_UART_FBRD, a HAL_DICE3_UART_LCR_H write must always be performed at the end.

Note

To update the three registers there are two possible sequences:

- UARTIBRD write, UARTFBRD write, and UARTLCR_H write
- UARTFBRD write, UARTIBRD write, and UARTLCR_H write.

To update UARTIBRD or UARTFBRD only:

- UARTIBRD write, or UARTFBRD write, and UARTLCR_H write.

Table 14.11 Parity truth table.

PEN	EPS	SPS	Parity bit (transmitted or checked)
0	x	x	Not transmitted or checked
1	1	0	Even Parity
1	0	0	Odd parity
1	0	1	1
1	1	1	0

Note

- The HAL_DICE3_UART_LCR_H, HAL_DICE3_UART_IBRD, and HAL_DICE3_UART_FBRD registers must not be changed:
  - when the UART is enabled
  - when completing a transmission or a reception when it has been programmed to become disabled.
- The FIFO integrity is not guaranteed under the following conditions:
  - after the BRK bit has been initiated
  - if the software disables the UART in the middle of a transmission with data in the FIFO, and then re-enables it.

14.2.7 UART Control Register – HAL_DICE3_UART_CR

Address offset: 0x0030 HAL_DICE3_UART_CR

The HAL_DICE3_UART_CR Register is the control register.

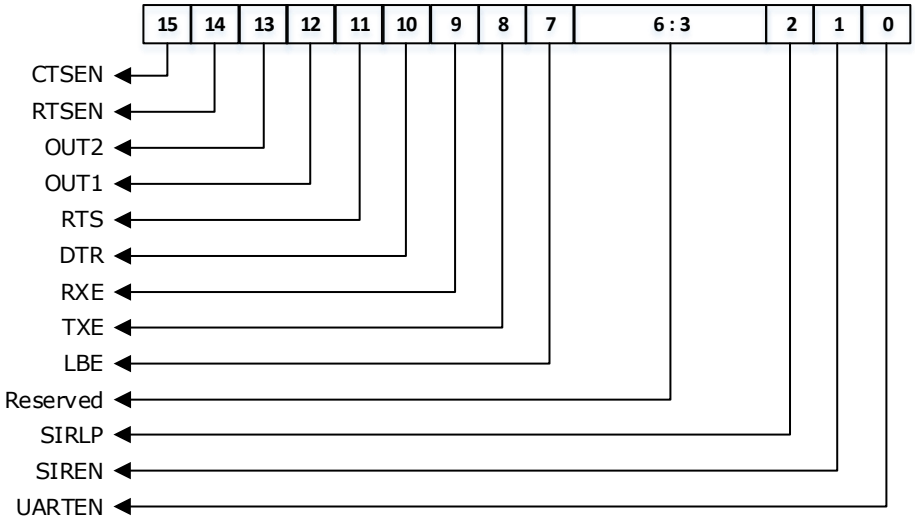

Table 14.12 UART Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	RW	Reserved, do not modify, read as zero.
CTSEn	15	0	RW	CTS hardware flow control enable. If this bit is set to 1, CTS hardware flow control is enabled. Data is only transmitted when the **nUARTCTS** signal is asserted. The CTS signal is not connected to external pins, so this function has no effect. Support firmware does not utilize this setting.
RTSEn	14	0	RW	RTS hardware flow control enable. If this bit is set to 1, RTS hardware flow control is enabled. Data is only requested when there is space in the receive FIFO for it to be received. The RTS signal is not connected to external pins, so this function has no effect. Support firmware does not utilize this setting.
Out2	13	0	RW	This bit is the complement of the UART Out2 modem status output. That is, when the bit is programmed to a 1, the output is 0. For DTE this can be used as *Ring Indicator* (RI).
Out1	12	0	RW	This bit is the complement of the UART Out1 modem status output. That is, when the bit is programmed to a 1 the output is 0. For DTE this can be used as *Data Carrier Detect* (DCD).

Name	Bit	Reset	Dir	Description
RTS	11	0	RW	Request to send. This bit is the complement of the UART request to send, **nUARTRTS**, modem status output. That is, when the bit is programmed to a 1 then **nUARTRTS** is LOW. The RTS signal is not connected to external pins, so this function has no effect. Support firmware does not utilize this setting.
DTR	10	0	RW	Data transmit ready. This bit is the complement of the UART data transmit ready, **nUARTDTR**, modem status output. That is, when the bit is programmed to a 1 then **nUARTDTR** is LOW.
RXE	9	1	RW	Receive enable. If this bit is set to 1, the receive section of the UART is enabled. Data reception occurs for either UART signals or SIR signals depending on the setting of the SIREN bit. When the UART is disabled in the middle of reception, it completes the current character before stopping.
TXE	8	1	RW	Transmit enable. If this bit is set to 1, the transmit section of the UART is enabled. Data transmission occurs for either UART signals, or SIR signals depending on the setting of the SIREN bit. When the UART is disabled in the middle of transmission, it completes the current character before stopping.
LBE	7	0	RW	Not used by support firmware. Loopback enable. If this bit is set to 1 and the SIREN bit is set to 1 and the SIRTEST bit in the *Test Control Register* is set to 1, then the **nSIROUT** path is inverted, and fed through to the **SIRIN** path. The SIRTEST bit in the test register must be set to 1 to override the normal half-duplex SIR operation. This must be the requirement for accessing the test registers during normal operation, and SIRTEST must be cleared to 0 when loopback testing is finished. This feature reduces the amount of external coupling required during system test. If this bit is set to 1, and the SIRTEST bit is set to 0, the **UARTTXD** path is fed through to the **UARTRXD** path. In either SIR mode or UART mode, when this bit is set, the modem outputs are also fed through to the modem inputs. This bit is cleared to 0 on reset, to disable loopback.
Reserved	6:3	0	RW	Reserved, do not modify, read as zero.

Name	Bit	Reset	Dir	Description
SIRLP	2	0	RW	Not used by support firmware. SIR low-power IrDA mode. This bit selects the IrDA encoding mode. If this bit is cleared to 0, low-level bits are transmitted as an active high pulse with a width of 3/16th of the bit period. If this bit is set to 1, low-level bits are transmitted with a pulse width that is 3 times the period of the IrLPBaud16 input signal, regardless of the selected bit rate. Setting this bit uses less power, but might reduce transmission distances.
SIREN	1	0	RW	Not used by support firmware. SIR enable: 0 = IrDA SIR ENDEC is disabled. nSIROUT remains LOW (no light pulse generated), and signal transitions on SIRIN have no effect. 1 = IrDA SIR ENDEC is enabled. Data is transmitted and received on nSIROUT and SIRIN. UARTTXD remains HIGH, in the marking state. Signal transitions on UARTRXD or modem status inputs have no effect. This bit has no effect if the UARTEN bit disables the UART.
UARTEN	0	0	RW	UART enable: 0 = UART is disabled. If the UART is disabled in the middle of transmission or reception, it completes the current character before stopping. 1 = the UART is enabled. Data transmission and reception occurs for either UART signals or SIR signals depending on the setting of the SIREN bit.

Note

To enable transmission, the TXE bit and UARTEN bit must be set to 1. Similarly, to enable reception, the RXE bit and UARTEN bit, must be set to 1.

Note

Program the control registers as follows:

1. Disable the UART.
2. Wait for the end of transmission or reception of the current character.
3. Flush the transmit FIFO by setting the FEN bit to 0 in the *Line Control Register*, HAL_DICE3_UART_LCR_H.
4. Reprogram the UARTCR Register.
5. Enable the UART.

14.2.8 UART Interrupt FIFO Level Select Register – HAL_DICE3_UART_IFLS

Address offset: 0x0034 HAL_DICE3_UART_IFLS

The HAL_DICE3_UART_IFLS Register is the interrupt FIFO level select register. You can use this register to define the FIFO level that triggers the assertion of **UARTTXINTR** and **UARTRXINTR**.

The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level.

The bits are reset so that the trigger level is when the FIFOs are at the half-way mark.

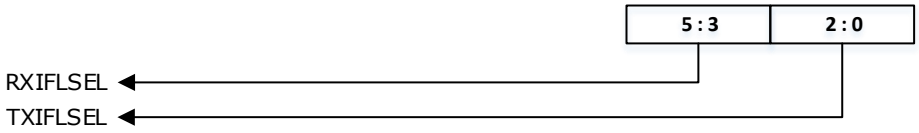

Table 14.13 UART Interrupt FIFO Level Select Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	15:6	0	RW	Reserved, do not modify, read as zero.
RXIFLSEL	5:3	0	RW	Receive interrupt FIFO level select. The trigger points for the receive interrupt are as follows: b000 = Receive FIFO becomes ≥ $^1/_8$ full b001 = Receive FIFO becomes ≥ $^1/_4$ full b010 = Receive FIFO becomes ≥ $^1/_2$ full b011 = Receive FIFO becomes ≥ $^3/_4$ full b100 = Receive FIFO becomes ≥ $^7/_8$ full b101-b111 = reserved.
TXIFLSEL	2:0	0	RW	Transmit interrupt FIFO level select. The trigger points for the transmit interrupt are as follows: b000 = Transmit FIFO becomes ≤ $^1/_8$ full b001 = Transmit FIFO becomes ≤ $^1/_4$ full b010 = Transmit FIFO becomes ≤ $^1/_2$ full b011 = Transmit FIFO becomes ≤ $^3/_4$ full b100 = Transmit FIFO becomes ≤ $^7/_8$ full b101-b111 = reserved.

14.2.9 UART Mask Set/Clear Register – HAL_DICE3_UART_IMSC

Address offset: 0x0038 HAL_DICE3_UART_IMSC

The HAL_DICE3_UART_IMSC register is the interrupt mask set/clear register. It is a read/write register.

On a read this register returns the current value of the mask on the relevant interrupt. On a write of 1 to the particular bit, it sets the corresponding mask of that interrupt. A write of 0 clears the corresponding mask.

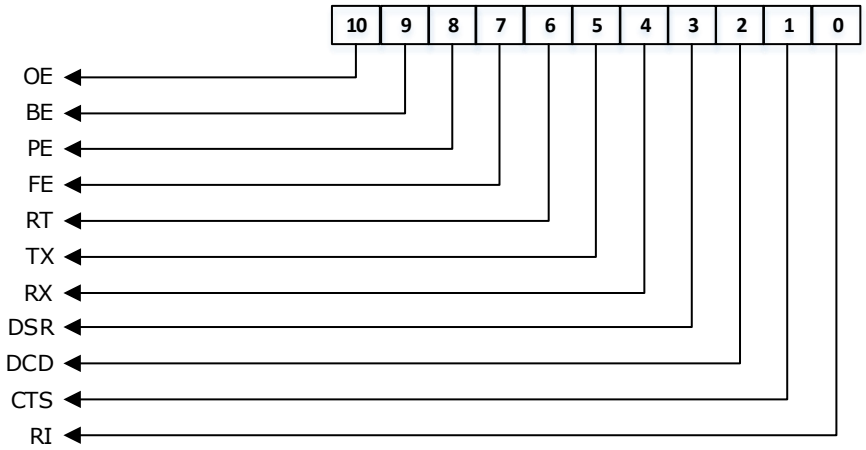

Table 14.14 UART Mask Set/Clear Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	RW	Reserved, do not modify, read as zero.
OE	10	0	RW	Overrun error interrupt mask. A read returns the current mask for the **UARTOEINTR** interrupt. On a write of 1, the mask of the **UARTOEINTR** interrupt is set. A write of 0 clears the mask.
BE	9	0	RW	Break error interrupt mask. A read returns the current mask for the **UARTBEINTR** interrupt. On a write of 1, the mask of the **UARTBEINTR** interrupt is set. A write of 0 clears the mask.
PE	8	0	RW	Parity error interrupt mask. A read returns the current mask for the **UARTPEINTR** interrupt. On a write of 1, the mask of the **UARTPEINTR** interrupt is set. A write of 0 clears the mask.
FE	7	0	RW	Framing error interrupt mask. A read returns the current mask for the **UARTFEINTR** interrupt. On a write of 1, the mask of the **UARTFEINTR** interrupt is set. A write of 0 clears the mask.
RT	6	0	RW	Receive timeout interrupt mask. A read returns the current mask for the **UARTRTINTR** interrupt. On a write of 1, the mask of the **UARTRTINTR** interrupt is set. A write of 0 clears the mask.
TX	5	0	RW	Transmit interrupt mask. A read returns the current mask for the **UARTTXINTR** interrupt. On a write of 1, the mask of the **UARTTXINTR** interrupt is set. A write of 0 clears the mask.

Name	Bit	Reset	Dir	Description
RX	4	0	RW	Receive interrupt mask. A read returns the current mask for the **UARTRXINTR** interrupt. On a write of 1, the mask of the **UARTRXINTR** interrupt is set. A write of 0 clears the mask.
DSR	3	0	RW	**nUARTDSR** modem interrupt mask. A read returns the current mask for the **UARTDSRINTR** interrupt. On a write of 1, the mask of the **UARTDSRINTR** interrupt is set. A write of 0 clears the mask.
DCD	2	0	RW	**nUARTDCD** modem interrupt mask. A read returns the current mask for the **UARTDCDINTR** interrupt. On a write of 1, the mask of the **UARTDCDINTR** interrupt is set. A write of 0 clears the mask.
CTS	1	0	RW	**nUARTCTS** modem interrupt mask. A read returns the current mask for the **UARTCTSINTR** interrupt. On a write of 1, the mask of the **UARTCTSINTR** interrupt is set. A write of 0 clears the mask.
RI	0	0	RW	**nUARTRI** modem interrupt mask. A read returns the current mask for the **UARTRIINTR** interrupt. On a write of 1, the mask of the **UARTRIINTR** interrupt is set. A write of 0 clears the mask.

14.2.10 UART Interrupt Status Register – HAL_DICE3_UART_RIS

Address offset: 0x003C HAL_DICE3_UART_RIS

The HAL_DICE3_UART_RIS Register is the raw interrupt status register. It is a read-only register. This register returns the current raw status value, prior to masking, of the corresponding interrupt. A write has no effect.

Caution

All the bits, except for the modem status interrupt bits (bits 3 to 0), are cleared to 0 when reset. The modem status interrupt bits are undefined after reset.

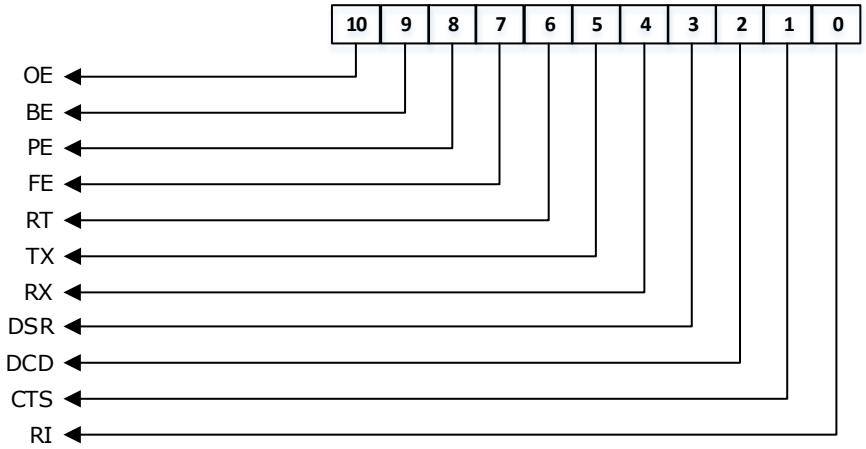

Table 14.15 UART Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	RW	Reserved, do not modify, read as zero.
OE	10	0	RW	Overrun error interrupt status. Returns the raw interrupt state of the **UARTOEINTR** interrupt.
BE	9	0	RW	Break error interrupt status. Returns the raw interrupt state of the **UARTBEINTR** interrupt.
PE	8	0	RW	Parity error interrupt status. Returns the raw interrupt state of the **UARTPEINTR** interrupt.
FE	7	0	RW	Framing error interrupt status. Returns the raw interrupt state of the **UARTFEINTR** interrupt.
RT	6	0	RW	Receive timeout interrupt status. Returns the raw interrupt state of the **UARTRTINTR** interrupt.[1]
TX	5	0	RW	Transmit interrupt status. Returns the raw interrupt state of the **UARTTXINTR** interrupt.
RX	4	0	RW	Receive interrupt status. Returns the raw interrupt state of the **UARTRXINTR** interrupt.
DSR	3	x	RW	**nUARTDSR** modem interrupt status. Returns the raw interrupt state of the **UARTDSRINTR** interrupt.
DCD	2	x	RW	**nUARTDCD** modem interrupt status. Returns the raw interrupt state of the **UARTDCDINTR** interrupt.
CTS	1	x	RW	**nUARTCTS** modem interrupt status. Returns the raw interrupt state of the **UARTCTSINTR** interrupt.
RI	0	x	RW	**nUARTRI** modem interrupt status. Returns the raw interrupt state of the **UARTRIINTR** interrupt.

[1] In this case the raw interrupt cannot be set unless the mask is set, this is because the mask acts as an enable for power saving. That is, the same status can be read from UARTMIS and UARTRIS for the receive timeout interrupt.

14.2.11 UART Masked Interrupt Status Register – HAL_DICE3_UART_MIS

Address offset: 0x0040 HAL_DICE3_UART_MIS

The HAL_DICE3_UART_MIS register is the masked interrupt status register. It is a read-only register. This register returns the current masked status value of the corresponding interrupt. A write has no effect.
All the bits except for the modem status interrupt bits (bits 3 to 0) are cleared to 0 when reset.

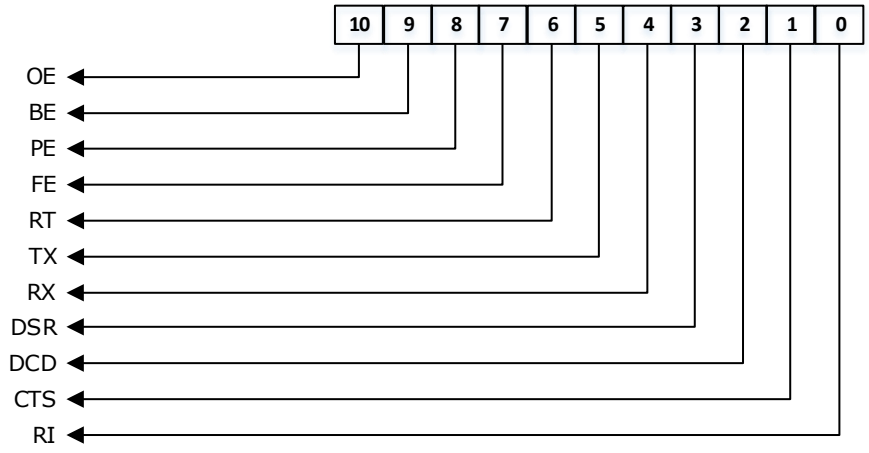

Table 14.16 UART Masked Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	RW	Reserved, do not modify, read as zero.
OE	10	0	RW	Overrun error masked interrupt status. Returns the masked interrupt state of the **UARTOEINTR** interrupt.
BE	9	0	RW	Break error masked interrupt status. Returns the masked interrupt state of the **UARTBEINTR** interrupt.
PE	8	0	RW	Parity error masked interrupt status. Returns the masked interrupt state of the **UARTPEINTR** interrupt.
FE	7	0	RW	Framing error masked interrupt status. Returns the masked interrupt state of the **UARTFEINTR** interrupt.
RT	6	0	RW	Receive timeout masked interrupt status. Returns the masked interrupt state of the **UARTRTINTR** interrupt.

Name	Bit	Reset	Dir	Description
TX	5	0	RW	Transmit masked interrupt status. Returns the masked interrupt state of the **UARTTXINTR** interrupt.
RX	4	0	RW	Receive masked interrupt status. Returns the masked interrupt state of the **UARTRXINTR** interrupt.
DSR	3	x	RW	**nUARTDSR** modem masked interrupt status. Returns the masked interrupt state of the **UARTDSRINTR** interrupt.
DCD	2	x	RW	**nUARTDCD** modem masked interrupt status. Returns the masked interrupt state of the **UARTDCDINTR** interrupt.
CTS	1	x	RW	**nUARTCTS** modem masked interrupt status. Returns the masked interrupt state of the **UARTCTSINTR** interrupt.
RI	0	x	RW	**nUARTRI** modem masked interrupt status. Returns the masked interrupt state of the **UARTRIINTR** interrupt.

14.2.12 UART Interrupt Clear Register – HAL_DICE3_UART_ICR

Address offset: 0x0044 HAL_DICE3_UART_ICR

The HAL_DICE3_UART_ICR register is the interrupt clear register and is write-only. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

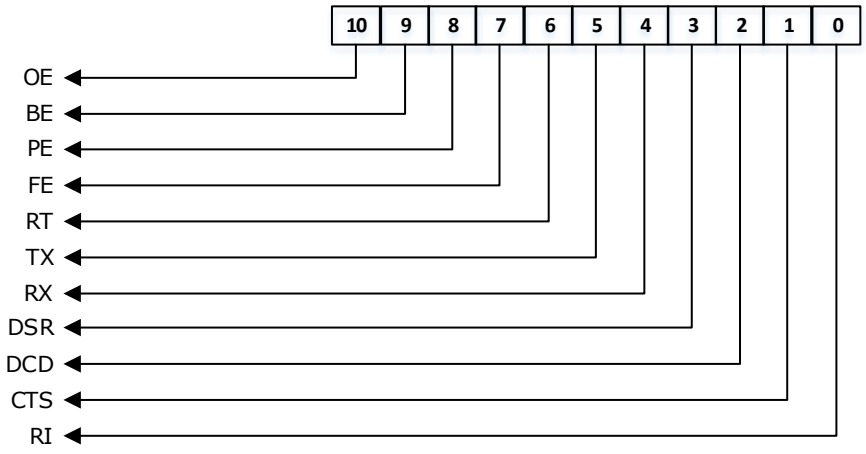

Table 14.17 UART Interrupt Clear Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	W	Reserved, do not modify, read as zero.

Name	Bit	Reset	Dir	Description
OE	10	0	W	Overrun error interrupt clear. Clears the **UARTOEINTR** interrupt.
BE	9	0	W	Break error interrupt clear. Clears the **UARTBEINTR** interrupt.
PE	8	0	W	Parity error interrupt clear. Clears the **UARTPEINTR** interrupt.
FE	7	0	W	Framing error interrupt clear. Clears the **UARTFEINTR** interrupt.
RT	6	0	W	Receive timeout interrupt clear. Clears the **UARTRTINTR** interrupt.
TX	5	0	W	Transmit interrupt clear. Clears the **UARTTXINTR** interrupt.
RX	4	0	W	Receive interrupt clear. Clears the **UARTRXINTR** interrupt.
DSR	3	0	W	**nUARTDSR** modem interrupt clear. Clears the **UARTDSRINTR** interrupt.
DCD	2	0	W	**nUARTDCD** modem interrupt clear. Clears the **UARTDCDINTR** interrupt.
CTS	1	0	W	**nUARTCTS** modem interrupt clear. Clears the **UARTCTSINTR** interrupt.
RI	0	0	W	**nUARTRI** modem interrupt clear. Clears the **UARTRIINTR** interrupt.

14.2.13 UART DMA Control Register – HAL_DICE3_UART_DMACR

Address offset: 0x0048 HAL_DICE3_UART_DMACR

The HAL_DICE3_UART_DMACR register is the DMA control register. It is a read/write register.

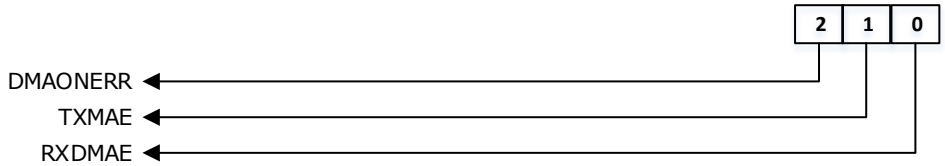

Table 14.18 UART DMA Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	RW	Reserved, do not modify, read as zero.
DMAONERR	2	0	RW	DMA on error. If this bit is set to 1, the DMA receive request outputs, **UARTRXDMASREQ** or **UARTRXDMABREQ**, are disabled when the UART error interrupt is asserted.

Name	Bit	Reset	Dir	Description
TXMAE	1	0	RW	Transmit DMA enable. If this bit is set to 1, DMA for the transmit FIFO is enabled.
RXDMAE	0	0	RW	Receive DMA enable. If this bit is set to 1, DMA for the receive FIFO is enabled.

14.3 Revisions

Table 14.19 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication