ADAT

Receivers and Transmitters

Revision 0.9.0-41360

May 6, 2015

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23 ADAT Receiver and Transmitter

23.1 Overview

The ADAT Receiver module is a dual ADAT conformant receiver supporting SMUX II and SMUX IV.
The ADAT Transmitter module is also a dual ADAT conformant receiver supporting SMUX II and SMUX IV.

These are the main features of the receiver and transmitter:

- Dual stream supporting 16 channels and Normal rates
- SMUX II support for up to 8 channels at Double rates
- SMUX IV support for up to 4 channels at Quad rates
- Sample rates from 32kHz to 192kHz
- Standard DICE Router interface
- User data available through control registers
- Sync signal provided from both ports

23.2 ADAT Receiver

23.2.1 Module Configuration

The ADAT Receiver IS addressed through 1 base address:

Table 23.1 ADAT Receiver base address

Base address	Description
0xC4000900	DICE3_ADAT_RX – Dual ADAT Receiver

Table 23.2 ADAT Receiver register summary

Address Offset	Register	Description
0x0000	ADAT_RX_CSR_0	*ADAT Rx Control Register 0*
0x0004	ADAT_RX_CSR_1	*ADAT Rx Control Register 1*

23.2.2 ADAT Rx Control Register 0 – ADAT_RX_CSR_0

Address offset: 0x0000 ADAT_RX_CSR_0

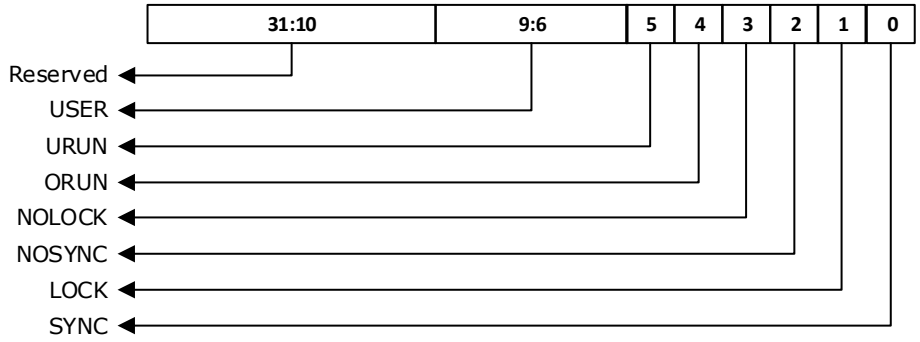

Table 23.3 ADAT Rx Control Register 0 bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:10	0	N/A	Reserved
USER	9:6	0	R	The 4 bits of user data received in the last frame.

Name	Bit	Reset	Dir	Description
URUN	5	0	R	Indicates resampling which typically happens when the system 1FS is faster than 1FS from the master receiver. Can also be due to jitter and phase differences between the router 1FS and 1FS from master receiver. This bit is sticky and will be cleared immediately after a read.
ORUN	4	0	R	Indicates slipped sample which typically happens when the system 1FS is slower than 1FS from the master receiver. Can also be due to jitter and phase differences between router 1FS and 1FS from master receiver. This bit is sticky and will be cleared immediately after a read.
NOLOCK	3	0	R	Indicates that ADAT RX0 is not locked, clear on read.
NOSYNC	2	0	R	No sync was detected by ADAT RX0, clear on read.
LOCK	1	0	R	Indicates that DATA RX0 was locked after 4 consecutive sync patterns.
SYNC	0	0	R	Indicates that ADAT has synchronized for 4 frames.

23.2.3 ADAT Rx Control Register 1 – ADAT_RX_CSR_1

Address offset: 0x0004 ADAT_RX_CSR_1

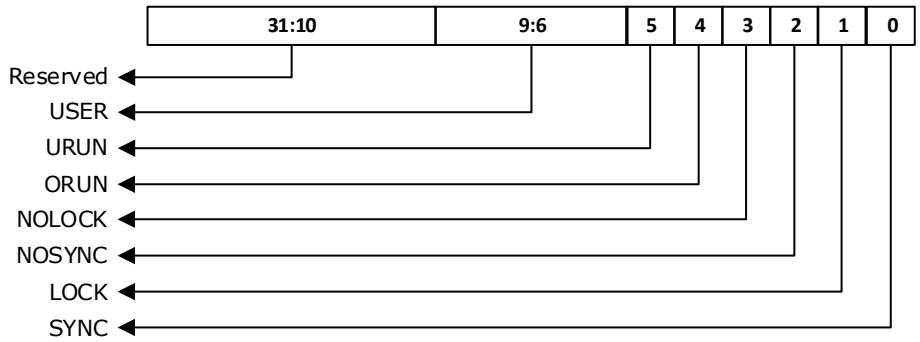

Table 23.4 ADAT Rx Control Register 0 bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:10	0	N/A	Reserved
USER	9:6	0	R	The 4 bits of user data received in the last frame.

Name	Bit	Reset	Dir	Description
URUN	5	0	R	Indicates resampling which typically happens when the system 1FS is faster than 1FS from the master receiver. Can also be due to jitter and phase differences between the router 1FS and 1FS from master receiver. This bit is sticky and will be cleared immediately after a read.
ORUN	4	0	R	Indicates slipped sample which typically happens when the system 1FS is slower than 1FS from the master receiver. Can also be due to jitter and phase differences between router 1FS and 1FS from master receiver. This bit is sticky and will be cleared immediately after a read.
NOLOCK	3	0	R	Indicates that ADAT RX1 is not locked, clear on read.
NOSYNC	2	0	R	No sync was detected by ADAT RX1, clear on read.
LOCK	1	0	R	Indicates that DATA RX1 was locked after 4 consecutive sync patterns.
SYNC	0	0	R	Indicates that ADAT has synchronized for 4 frames.

23.3 ADAT Transmitter

23.3.1 Module Configuration

The ADAT Transmitter is addressed through 1 base address:

Table 23.5 ATAT Transmitter base address

Base address	Description
0xC4000800	DICE3_ADAT_TX – Dual ADAT Transmitter

Table 23.6 ADAT Transmitter register summary

Address Offset	Register	Description
0x0000	ADAT_TX_CSR	*ADAT Tx Control Register*
0x0004	ADAT_TX_MUTE0	ADAT Tx Mute 0 Register
0x0008	ADAT_TX_MUTE1	ADAT Tx Mute 1 Register

23.3.2 ADAT Tx Control Register – ADAT_TX_CSR

Address offset: 0x0000 ADAT_TX_CSR

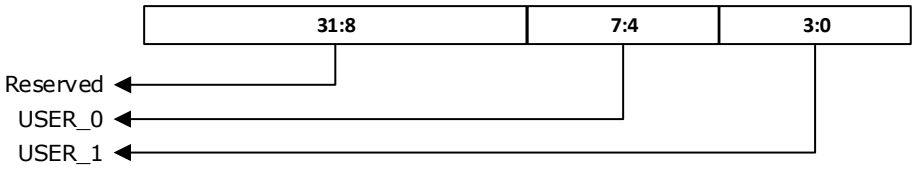

Table 23.7 ADAT Tx Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
USER_0	7:4	0	R/W	Specify user data for ADAT Tx 1
USER_1	3:0	0	R/W	Specify user data for ADAT Tx 0

23.3.3 ADAT Tx Mute Register 0 – ADAT_TX_MUTE0

Address offset: 0x0004 ADAT_TX_MUTE0

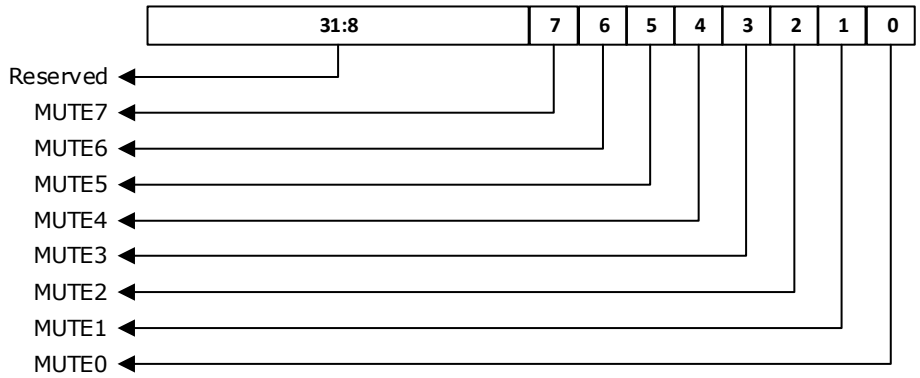

Table 23.8 ADAT Tx Mute 0 Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
MUTE7-0	7:0	0	R/W	Individual Mute of the 8 audio channels in the ADAT TX0 stream.

23.3.4 ADAT Tx Mute Register 1 – ADAT_TX_MUTE1

Address offset: 0x0008 ADAT_TX_MUTE1

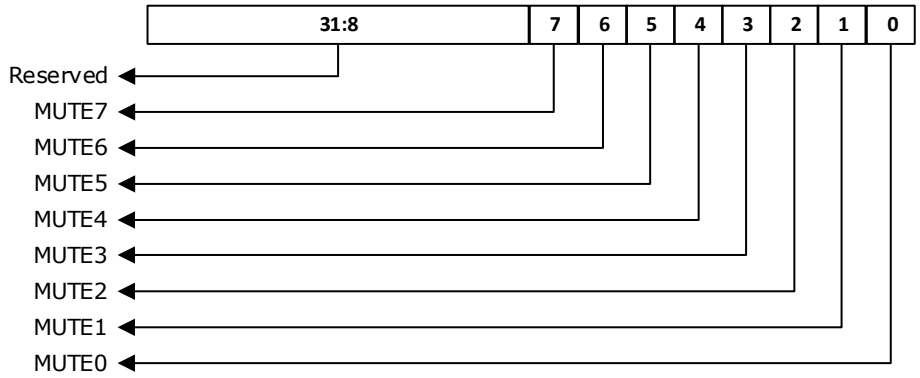

Table 23.9 ADAT Tx Mute 0 Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
MUTE7-0	7:0	0	R/W	Individual Mute of the 8 audio channels in the ADAT TX1 stream.

23.4 Revisions

Table 23.10 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

