ETH

Ethernet MAC with Timestamp Extension

Revision 1.0.0-41582

July 17, 2015

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16 ETH Module

16.1 Module Overview

The ETH module implements an Ethernet Media Access Controller (MAC) with support for 10/100/1000 Mbit/sec Ethernet. The module has extensions for IEEE1588-V2 synchronization and provides a Real-Time Clock (RTC) which can be used for time-stamping of all incoming and outgoing traffic.

ETH module features

- RGMII interface supporting 10/100/1000 Mbit/sec Ethernet frames
- Support for Full Duplex only (no collision detect)
- 2KB RX FIFO with DMA handshake
- 4KB TX FIFO, can be filled from Memory DMA
- 7 perfect DST + ETHTYP filters with 8-byte match and mask
- Hash filter for multicast filtering using 64 bins
- RTC counter with 20 bit fractional ns precision
- Independent PTP packet Rx and Tx FIFO's for 802.1AS implementation
- MDIO interface for communicating with PHY's

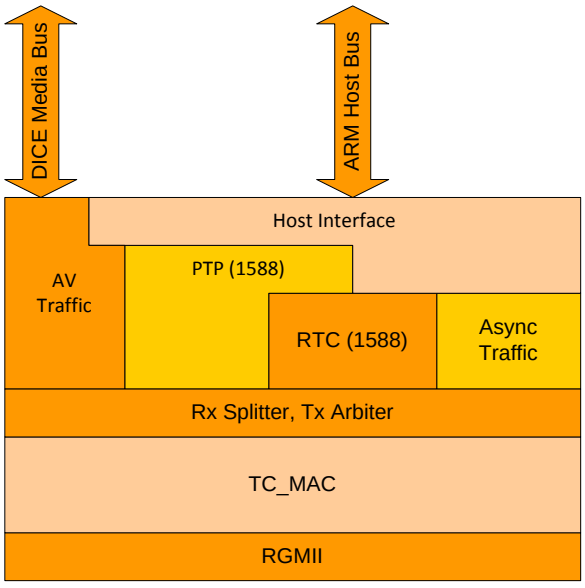


Figure 16.1 ETH Module block diagram

16.2 Module Configuration

Table 16.1 ETH module base addresses

Base address	Base register definition
0x400000000	CYG_HAL_DICE3_ETH

Table 16.2 ETH sub-module base addresses

ETH module registers are described below by their offsets from the base address.

Address offset	Base register definition	Document Section
0x0000	CYG_HAL_DICE3_ETH_RTC_BASE	*Real-Time Clock*
0x0080	CYG_HAL_DICE3_ETH_PTP_RX_BASE	*PTP Module*
0x0100	CYG_HAL_DICE3_ETH_PTP_TX_BASE	*PTP Module*
0x0180	CYG_HAL_DICE3_ETH_RX_BASE	*Legacy Packet Module*
0x0200	CYG_HAL_DICE3_ETH_TX_BASE	*Legacy Packet Module*
0x0280	CYG_HAL_DICE3_ETH_SYS_CFG	*System Configuration*
0x0300	CYG_HAL_DICE3_ETH_MAC_CFG	*MAC Configuration*
0x0380	CYG_HAL_DICE3_ETH_MAC_STAT	*MAC Statistics*

Table 16.3 ETH AVB buffer memory area base addresses

ETH buffer memory areas are described below by their offsets from the base address.

Address offset	Buffer base definition	Document Section
0x0400	CYG_HAL_DICE3_ETH_FKT_BUF	*MAC Filter engine*
0x1000	CYG_HAL_DICE3_ETH_PTP_RX_BUF	*PTP Module*
0x1800	CYG_HAL_DICE3_ETH_PTP_TX_BUF	*PTP Module*
0x4000	CYG_HAL_DICE3_ETH_TX_BUF	*Legacy Packet Module*
0x6000	CYG_HAL_DICE3_ETH_RX_BUF	*Legacy Packet Module*

16.3 Real-Time Clock

The Real-Time Clock module contains a 78 + 20 bit accumulator combining 48 bits of seconds, 30 bits of nanoseconds and 20 bits of fractional nanoseconds. Only the upper 78 bits can be accessed from the firmware.
The 30 bit nanosecond field counts to 2^9-1 and wraps. On every 125MHz clock (8ns) a 26 bit field is added to the accumulator. This field can be written by firmware and allows the accumulator to be tuned to a precision of about 0.1PPM equivalent to a drift of 100ns per second.
In a typical implementation of PTP this counter is free running and is being frequency adjusted based on incoming sync packets. Software will also hold an offset which is the difference between the free running counter and the actual network time.
All Ethernet packets and AIO audio buffers are being time-stamped with the low 32 bits of the RTC (2 bits seconds and 30 bits of nanoseconds). Firmware can handle offset adjustments when those time-stamps are received from the hardware.

16.3.1 The 8KHz pulse

The RTC also creates an 8KHz pulse from the RTC counter. This pulse can be used to drive the JET PLL and it is also used to frame AVB packets in the AVB talker. In order to control the phase of the 8KHz counter an offset register is available. This register should be written by firmware and should contain the firmware offset (nanosecond part only) modulo 125000. As long as the adjustments vary with less than +/- 8192ns the 8KHz pulse train will be continuous. Larger changes will result in resynchronization.
Note that this pulse can drive the JET PLL and therefore sample rates which are aligned to epoc can be synthesized as long as the offset is kept updated using PTP.

16.3.2 The 32 bit nanosecond time stamp

The AVB streaming engine requires a nanosecond timestamp which wraps at 2^{32} ns. The system maintains the correct phase of this counter through another offset register which is written by firmware.
This register should be written with (rtc_offset_sec * 10^9 + rtc_offset_ns) % 2^{32}.
Fortunately due to modulo arithmetic this can be reduced to:

rtc_offset_1722 = (uint32)**rtc_offset_sec** * (uint32)0x3b9aca00 + **rtc_offset_ns**

It is only necessary to update this register if the hardware AVB engine is being used.

16.3.3 Compare Match Engine

In order to generate interrupts or to clock the PLL when certain events are happening, a compare match module can be programmed to generate an interrupt and a JET PLL reference event when the RTC crosses a certain value.

16.3.4 RTC Registers

RTC Module registers are located at 0x40000000, which is the CYG_HAL_DICE3_ETH_RTC_BASE offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.4 RTC Module register summary

Address Offset	Register	Description
0x0000	RTC_RATE	See *RTC Rate Register*
0x0004	RTC_1722_OFS	See *RTC 1722 Offest Register*
0x0008	RTC_8KHZ_OFS	See *RTC 8KHz Offet Register*
0x000c	RTC_FRQ_NS	See *RTC Frequency NS Register*
0x0010	RTC_FRQ_S_LO	See *RTC Frequency S LO Register*
0x0014	RTC_FRQ_S_HI	See *RTC Frequency S HI Register*
0x0018	RTC_CMP_MATCH	See *RTC Compare Match Register*

16.3.4.1 Real-Time Clock Rate Register - RTC_RATE

Address offset: 0x0000 RTC_RATE

This is used for RTC rate corrections.

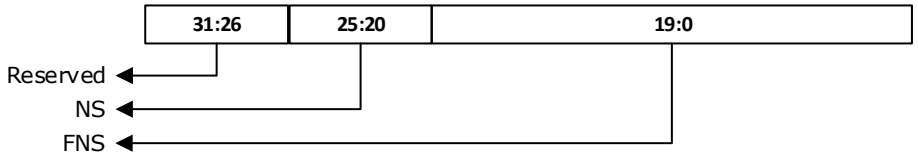


Table 16.5 RTC Clock Rate Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:6	0	N/A	Reserved
NS	25:20	0	R/W	Nanosecond value
FNS	19:0	0	R/W	Fractional nanosecond value

16.3.4.2 Real-Time Clock 1722 Offset Register - RTC_1722_OFS

Address offset: 0x0004 RTC_1722_OFS

This is used for PTP time phase corrections.

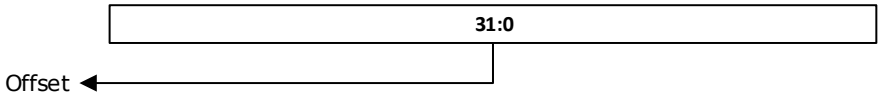


Table 16. RTC 1722 Offset Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:0	0	R/W	Nanosecond value

16.3.4.3 Real-Time Clock 8 KHz Offset Register - RTC_8KHZ_OFS

Address offset: 0x0008 RTC_8HKZ_OFS

This is used for RTC 8 KHz audio clock corrections.

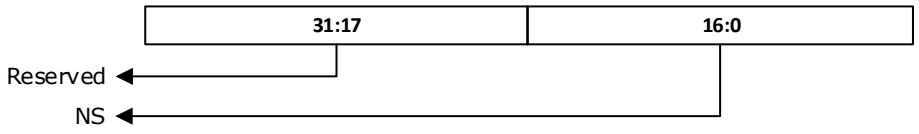


Table 16.6 RTC 8 KHz Offset Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:17	0	N/A	Reserved
NS	16: 0	0	R/W	Offset, nanoseconds % 125000

16.3.4.4 Real-Time Clock Frequency Register - RTC_FRQ_NS

Address offset: 0x000C RTC_FRQ_NS

This is used to read the current RTC nanoseconds value. A read of this register also freezes the current values in the RTC_FRQ_S_LO and RTC_FRQ_S_HI seconds values registers.

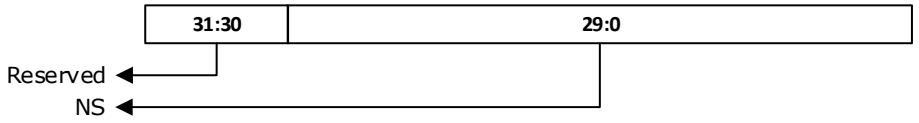


Table 16.7 RTC Frequency Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:30	0	N/A	Reserved
NS	29:0	0	R	Current nanoseconds value

16.3.4.5 Real-Time Clock Frequency S Low Register - RTC_FRQ_S_LO

Address offset: 0x0010 RTC_FRQ_S_LO

This is used to read the current lower 32 bits of the current RTC frequency seconds count. A read to RTC_FRQ_NS should be performed before this value is used.

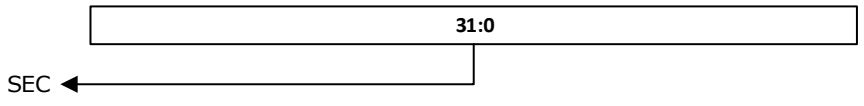


Table 16.8 RTC Frequency S Low Register bit assignments

Name	Bit	Reset	Dir	Description
SEC	31:0	0	R	Value of the lower 32 bits of the seconds value when RTC_FREQ_NS was last read.

16.3.4.6 Real-Time Clock Frequency S High Register - RTC_FRQ_S_HI

Address offset: 0x0014 RTC_FRQ_S_HI

This is used to read the current upper 16 bits of the current RTC frequency seconds count. A read to RTC_FRQ_NS should be performed before this value is used.

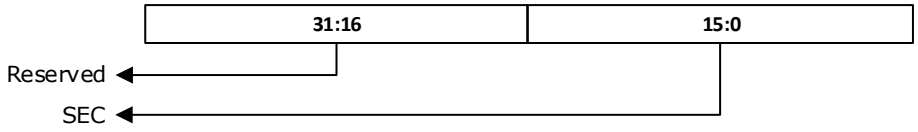


Table 16.9 RTC Frequency S High Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
SEC	15:0	0	R	Value of the upper 16 bits of the seconds value when RTC_FREQ_NS was last read.

16.3.4.7 Real-Time Clock Compare Match Register - RTC_CMP_MATCH

Address offset: 0x0018 RTC_CMP_MATCH

Write a 32 bit compare-match value (i.e. a future time) in the form of 2:30 (seconds:nanoseconds) to start a new compare. When the count reaches the set value, an interrupt occurs and a pulse is sent to the PLL. This allows implementation of entirely firmware-based streaming audio protocols.

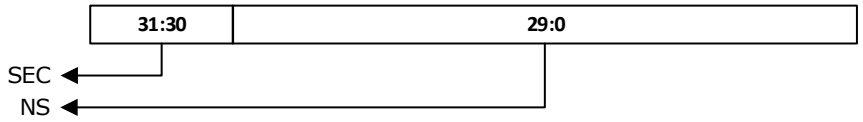


Table 16.10 RTC Compare Match Register bit assignments

Name	Bit	Reset	Dir	Description
SEC	31:30	0	RW	Seconds
NS	29:0	0	RW	Nanoseconds. When reading, if bit 0 is set, it is matched, and the remaining bits read back what was last written.

16.4 PTP Module

While a PTP implementation can be done using the legacy Ethernet packet interface there are some advantages to using a separate system for PTP. This allows quick responses to PTP packets and assures that PTP processing is not postponed while other legacy traffic is being processed.
This engine is designed for processing layer 2 PTP as it only filters on the EtherType field.

16.4.1 PTP Receive FIFO

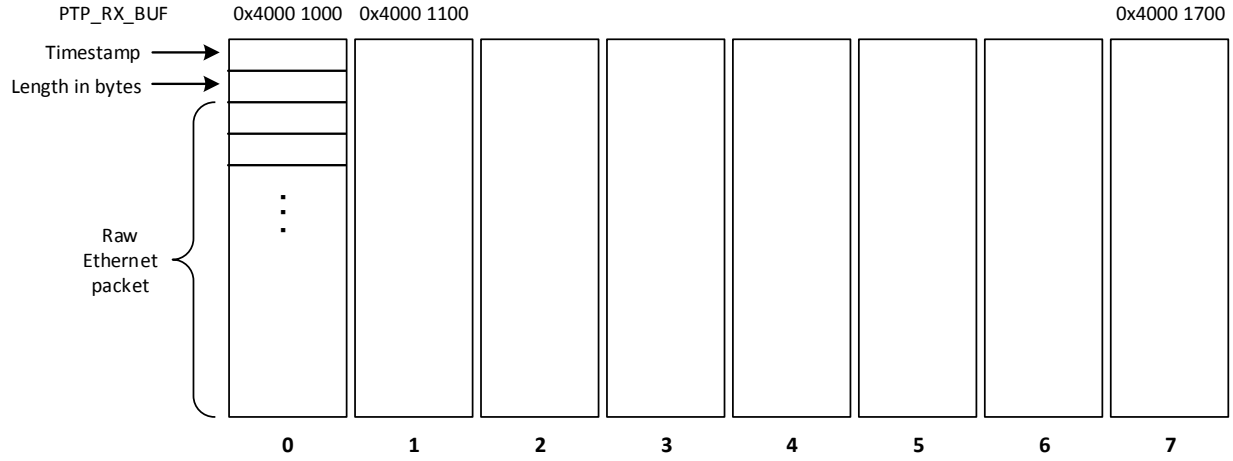
This module is capable of storing 8 incoming messages of each 256 bytes. Messages which are longer will be truncated. Each of the 256 byte buffers (bins) contains a 32-bit word containing a 30-bit timestamp, followed by a 32-bit word containing the length of the raw Ethernet packet in bytes, followed by the raw packet.

The system has a put and a get pointer, which are 3-bit values corresponding to one of the 8 buffers (bins). If the get pointer is different from the put pointer there is at least one message. After reading a message (or messages) the firmware should increase the get pointer modulo 8.

The module contains registers to access the get and put pointers, status and setting of which EtherType used (if other than the default PTP EtherType). An interrupt can be generated when there are packets in the FIFO.

It also contains a flat memory area through which the 8 packet bins can be accessed. The figure below shows how the flat memory area is divided into 8 message bins.

PTP_RX_BUF: 0x40001000 – 0x400017ff



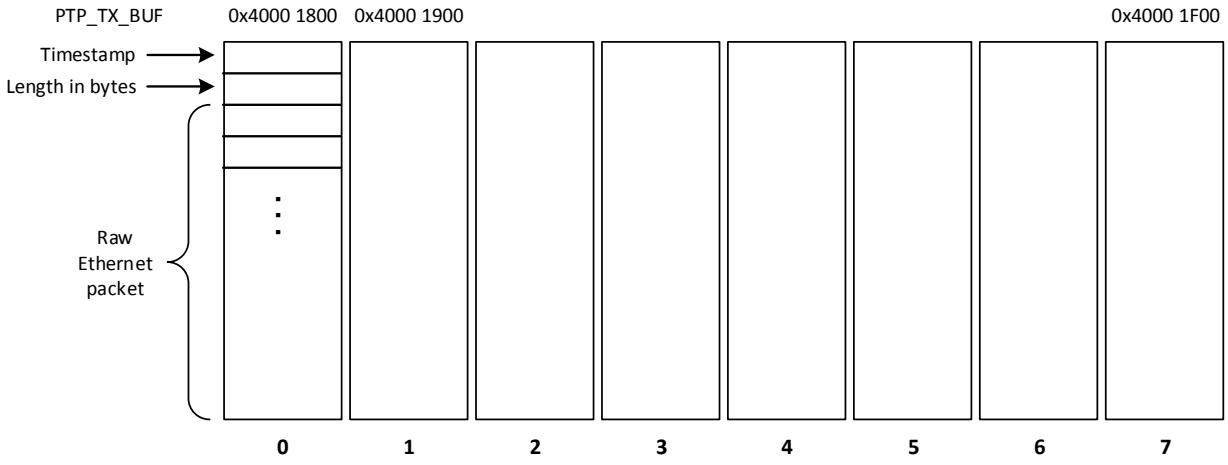
16.4.2 PTP Transmit FIFO

This module is capable of storing 8 outgoing messages of each 256 bytes. This enables the PTP firmware to prepare messages such as pDelay_Req, pDelay_Rsp, pDelay_FollowUp, Sync, FollowUp and Announce.

Each of the 256 byte buffers (bins) contains a 32-bit word containing a 30-bit timestamp (which is added by the transmitter when sent), followed by a 32-bit word containing the length of the raw Ethernet packet in bytes, followed by the raw packet.

Each bin can be enabled for transmission independently and interrupts can be generated when a bin has been sent. The bins are logically addressed with put and get pointers in the same manner as the receive FIFO bins. It also contains a flat memory area through which the 8 packet bins can be accessed. The figure below shows how the flat memory area is divided into 8 message bins.

PTP_TX_BUF: 0x400010800 – 0x40001fff



16.4.3 PTP Registers

16.4.3.1 RX Configuration

PTP Module RX Configuration registers are located at base address 0x40000080, which is the CYG_HAL_DICE3_ETH_PTP_RX_BASE offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.11 PTP Module Receive register summary

Address Offset	Register	Description
0x0000	PTP_RX_GET	See *PTP RX Get Register*
0x0004	PTP_RX_PUT	See *PTP RX Put Register*
0x0008	PTP_RX_STAT	See *PTP RX Status Register*
0x000C	PTP_RX_CTRL	See *PTP RX Control Register*

16.4.3.2 PTP RX Get Register – PTP_RX_GET

Address offset: 0x0000 PTP_RX_GET

Retrieve the current get-pointer in the PTP_RX_BUF. This indicates which of the eight logical buffers is currently ready to read. The logical buffer address is determined by multiplying the get pointer value by 256 and adding the PTP_RX_BASE offset.

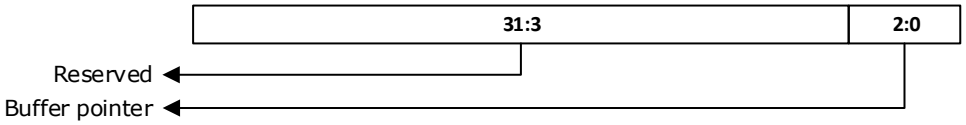


Table 16. PTP RX Get Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	N/A	Reserved
Buffer pointer	2:0	0	R/W	Current RX buffer

16.4.3.3 PTP RX Put Register – PTP_RX_PUT

Address offset: 0x0004 PTP_RX_PUT

Retrieve the current put-pointer in the PTP_TX_BUF. This indicates which of the eight logical buffers is currently ready to read. The logical buffer address is determined by multiplying the put pointer value by 256 and adding the PTP_RX_BASE offset.

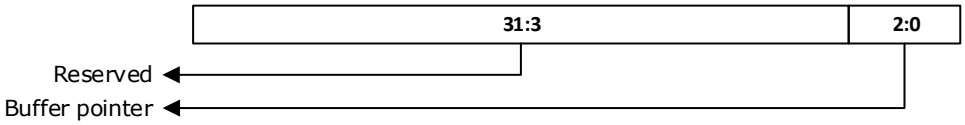


Table 16. PTP RX Put Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	N/A	Reserved
Buffer pointer	2:0	0	R	Current TX buffer

16.4.3.4 PTP RX Status Register – PTP_RX_STAT

Address offset: 0x0008 PTP_RX_STAT

This register is used to determine if any buffers are not empty, and to clear a buffer overrun interrupt.

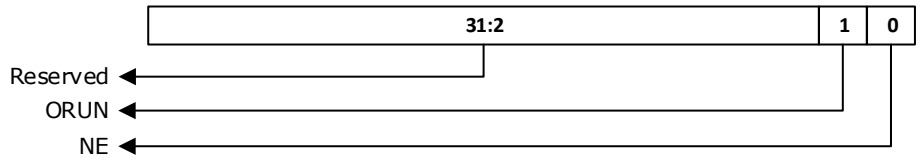


Table 16. PTP RX Stat Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:2	0	N/A	Reserved
ORUN	1	0	R/W	A buffer overrun occurred. Write 1 to clear.
NE	0	0	R/W	Set if buffer is not empty

16.4.3.5 PTP RX Control Register – PTP_RX_CTRL

Address offset: 0x000C PTP_RX_CTRL

This register is used to set the EtherType of the Ethernet frames to receive. This defaults to 0x88F7 on reset, so it is not necessary to set this when using the default PTP protocol EtherType.

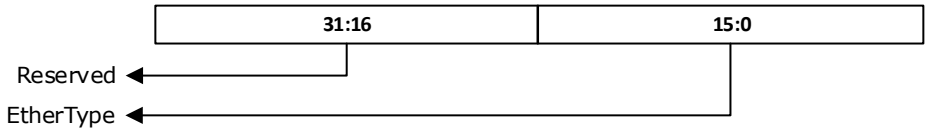


Table 16. PTP RX Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
EtherType	15:0	0x88F7	R/W	EtherType of messages to receive.

16.4.3.6 TX Configuration

PTP Module Transmit registers are located at base address 0x40000100, the CYG_HAL_DICE3_ETH_PTP_TX_BASE offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.12 PTP Module Transmit register summary

Address Offset	Register	Description
0x0000	PTP_TX_PEND	See *PTP TX Pending Register*
0x0004	PTP_TX_STAT	See *PTP TX Status Register*

16.4.3.7 PTP TX Pending Register – PTP_TX_PEND

Address offset: 0x0000 PTP_TX_PEND

Used to indicate a buffer that is ready to send.

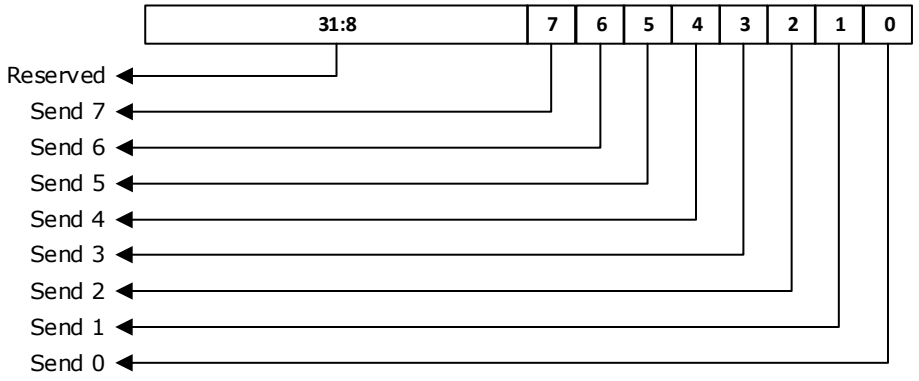


Table 16. PTP TX Pending Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
Send 0-7	7:0	0	R/W	Write a 1 to the bit corresponding to the buffer to send. Read 1 if still pending.

16.4.3.8 PTP TX Status Register – PTP_TX_STAT

Address offset: 0x0004 PTP_TX_STAT

This register is used to clear a TX done interrupt.

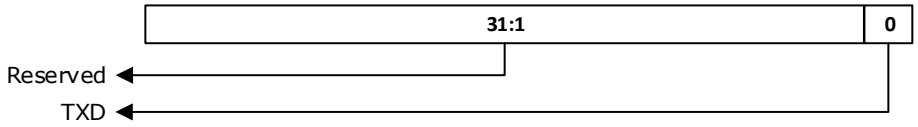


Table 16. PTP RX Get Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
Buffer pointer	0	0	R/W	Set if a buffer was sent. Write 1 to clear.

16.5 Legacy Packet Module

The term 'legacy' refers to all standard Ethernet traffic. This is the module which typically connects to the TCP/IP protocol stack and other stacks.
All packets sent or received will still be time-stamped with the RTC nanosecond value.
This module supports device controlled DMA on the receive side and is compatible with memory to memory DMA on the transmit side.

16.5.1 Packet Receive FIFO

The receive FIFO is 2K bytes (see CYG_HAL_DICE3_ETH_RX_BUF) so it can always contain one maximum size Ethernet packet. The DMA will make sure that packets are transferred out of the FIFO immediately.

The FIFO is accessed in one of two ways:

Non-DMA The FIFO is represented as a linear block of 32 bit words, the PUT and GET pointers are offsets into this memory. The GET pointer should only be moved forward by an integer number of packets after the packet is read or discarded.

DMA The FIFO is represented as a true FIFO and any read from the FIFO memory will pop a 32 bit word. The handshake with the DMA engine assures that a

packet is transferred as a number of DMA block size transfers followed by zero or more single transfers to complete the packet. When one complete packet is transferred the DMA engine is told that the transfer has completed. The DMA must be set up to match the block size of this module and each DMA descriptor must be programmed to handle one full size Ethernet packet including the length and time-stamp fields.

16.5.2 Legacy Packet Module Registers

Legacy Packet Module RX registers are located at 0x40000180, which is the CYG_HAL_DICE3_ETH_RX_BASE offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.13 Legacy Module register summary

Address Offset	Register	Description
0x0000	ETH_RX_GET	See *ETH RX Get Register*
0x0004	ETH_RX_PUT	See *ETH RX Put Register*
0x0008	ETH_RX_STAT	See *ETH RX Status Register*
0x000C	ETH_RX_DMA	See *ETH RX DMA Register*

16.5.2.1 ETH Rx Get Register – ETH_RX_GET

Address offset: 0x0000 ETH_RX_GET

Byte offset into the receive FIFO where the first DWORD (length) of the next packet is to be found. See section 16.4.1.

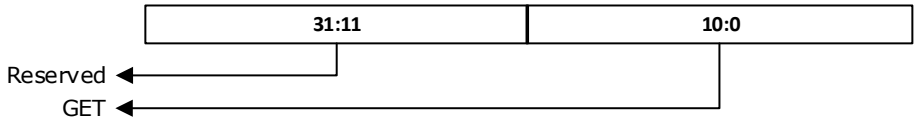


Table 16. ETH RX Get Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
GET	0	0	R/W	Low two bits always zero

16.5.2.2 ETH Rx Put Register – ETH_RX_PUT

Address offset: 0x0004 ETH_RX_PUT

Byte offset right after the last received packet. This is where the next packet will be placed. See section 16.4.2.

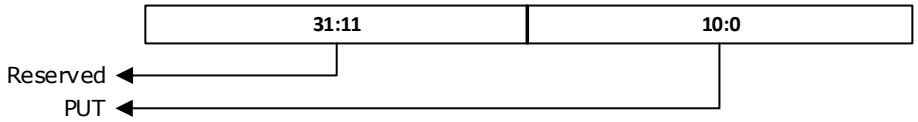


Table 16. ETH RX Put Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
PUT	10:0	0	R	Low two bits always zero

16.5.2.3 ETH RX Status Register – ETH_RX_STATUS

Address offset: 0x0008 ETH_RX_STATUS

This register indicates the status of the receive engine.

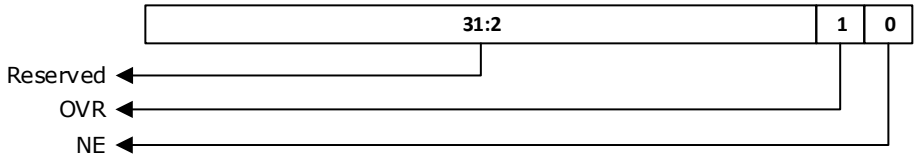


Table 16. ETH RX Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
OVR	1	0	R/W	Set if overrun occurred. Write 1 to clear.
NE	0	0	R/W	Buffer not empty.

16.5.2.4 ETH RX DMA Register – ETH_RX_DMA

Address offset: 0x000C ETH_RX_DMA

This register enables the receive FIFO DMA and set the DMA burst size.

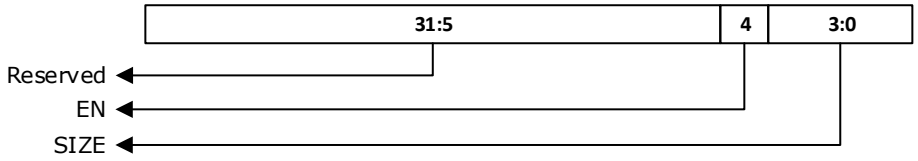


Table 16. ETH RX DMA Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:5	0	N/A	Reserved
EN	4	0	R/W	Set to enable DMA mode
SIZE	3:0	0	R/W	DMA block size in 32-bit words

16.5.2.5 ETH RX Buffer

CYG_HAL_DICE3_ETH_RX_BUF: 0x40006000 – 0x40007fff (see
The memory space is mirrored to enable continuous memory copy operations.
Packets are aligned to 32-bit words. The packet format is as follows:

DWORD 0 Length of packet in bytes
DWORD 1..N Ethernet frame
DWORD N+1 RTC timestamp of time of reception (only 30 bits ns)

N is calculated as (length_bytes + 3)/4

After reading the packet the GET pointer should be moved forward with 4*(N+1) bytes when using non-DMA mode. In DMA mode the GET pointer will automatically be updated when the packet is transferred. The format of the packet in the DMA destination memory is the same as stated above.

16.5.3 Packet Transmit FIFO

The transmit FIFO (see CYG_HAL_DICE3_ETH_TX_BUF) is 4k so a number of Ethernet packets can be moved to the FIFO ahead of time which enables full utilization of the bandwidth.
Because the FIFO is in continuous mirrored memory a simple memory to memory DMA can be used to transfer packets to the FIFO.

Firmware will write one packet into the FIFO starting at the PUT offset, after writing the complete packet the firmware increments the PUT pointer by the size of the packet (frame rounded up to 32 bit word and add one 32 bit word for length field). When the engine completes sending the packet it moves the GET pointer and sets 'tx done'. If the firmware writes more than one outstanding packet it will have to inspect the GET pointer to check when each packet is sent.

Legacy Packet Module TX configuration registers are located at 0x40000200, which is the CYG_HAL_DICE3_ETH_TX_BASE offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.14 Legacy Packet Transmit register summary

Address Offset	Register	Description
0x0000	ETH_TX_GET	See *Ethernet TX Get Register*
0x0004	ETH_TX_PUT	See *Ethernet TX Put Register*
0x0008	ETH_TX_STAT	See *Ethernet TX Status Register*

16.5.3.1 Ethernet TX Get Register – ETH_TX_GET

Address offset: 0x0000 ETH_TX_GET

This register indicates which packet in the FIFO was sent. When the engine has sent a packet it moves the GET pointer to the byte offset right after the packet. When GET equals PUT the FIFO is empty.

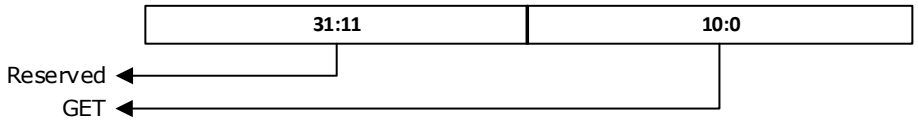


Table 16.15 Ethernet TX Get Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
GET	10:0	0	R	Low two bits always zero

16.5.3.2 Ethernet TX Put Register – ETH_TX_PUT

Address offset: 0x0004 ETH_TX_PUT

This is used determine that a new packet was written to the FIFO. The PUT pointer should be set to the byte offset immediately after the end of the packet just written.

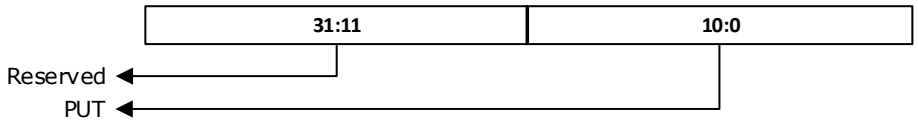


Table 16.16 Ethernet TX Put Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
PUT	10:0	0	R/W	Low two bits always zero

16.5.3.3 Ethernet TX Status Register – ETH_TX_STAT

Address offset: 0x0008 ETH_TX_STAT

This register indicates the status of the transmit engine.

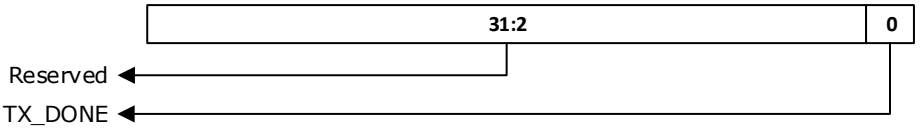


Table 16.17 Ethernet TX Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
TX_DONE	0	0	R/W	Set when the engine has sent one packet and cleared by firmware. Write 1 to clear.

16.5.3.4 ETH TX Buffer

CYG_HAL_DICE3_ETH_RX_BUF: 0x40004000 – 0x40005fff
The memory space is mirrored to enable continuous memory copy operations.
Packets are aligned to 32-bit words, the packet format is as follows:

DWORD 0 Length of packet in bytes
DWORD 1..N Ethernet frame, DWORD 1 overwritten by time-stamp after send

N is calculated as (length_bytes + 3)/4

The time-stamp is written back to the FIFO after the packet is sent so if firmware needs to know the time-stamp it should read it when the GET pointer is updated indicating that the packet is sent and the time-stamp updated.

16.6 System Configuration

This module configures the MAC and handles all interrupt sources from the various modules. System Configuration registers are located at 0x40000280, which is the CYG_HAL_DICE3_ETH_SYS_CFG offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.18 ETH System Configuration register summary

Address Offset	Register	Description
0x0000	ETH_SYS_INT_EN	See *Ethernet System Int Enable Register*
0x0004	ETH_SYS_CTRL	See *Ethernet System Control Register*
0x0008	ETH_SYS_INT_SET	See *Ethernet System Int Set Register*
0x000C	ETH_SYS_INT_CLR	See *Ethernet System Int Clear Register*
0x0010	ETH_SYS_AV_CTRL	See *Ethernet System AV Control Register*

16.6.1.1 ETH System Interrupt Enable Register – ETH_SYS_INT_EN

Address offset: 0x0000 ETH_SYS_INT_EN

This register is used to enable interrupts in the ETH module.

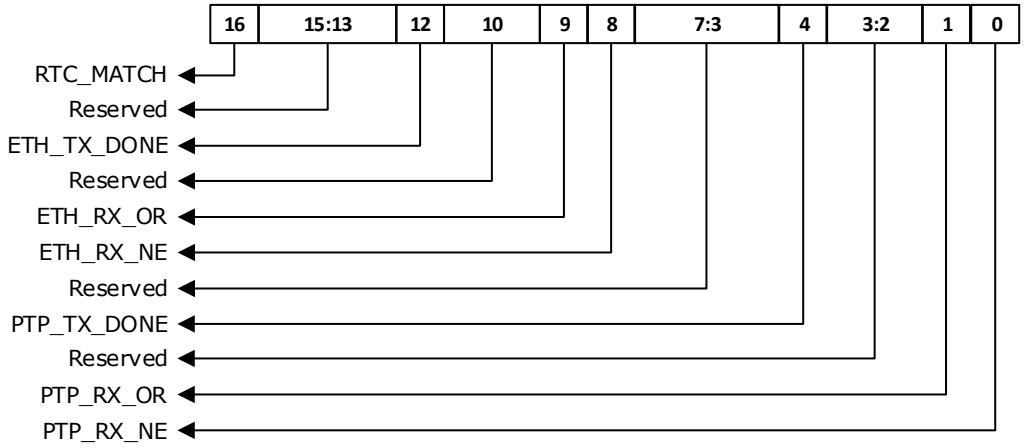


Table 16. ETH System Interrupt Enable Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:17	0	N/A	Reserved
ETH_SYS_INT_RTC_MATCH	16	0	R/W	RTC compare match
Reserved	15:13	0	N/A	Reserved
ETH_SYS_INT_ETH_TX_DONE	12	0	R/W	Packet Tx FIFO, packet sent
Reserved	11:10	0	N/A	Reserved
ETH_SYS_INT_ETH_RX_OR	9	0	R/W	Packet Rx FIFO overrun
ETH_SYS_INT_ETH_RX_NE	8	0	R/W	Packet Rx FIFO is not empty
Reserved	7:5	0	N/A	Reserved
ETH_SYS_INT_PTP_TX_DONE	4	0	R/W	PTP Tx Slot sent
Reserved	3:2	0	N/A	Reserved
ETH_SYS_INT_PTP_RX_OR	1	0	R/W	PTP Rx FIFO overrun
ETH_SYS_INT_PTP_RX_NE	0	0	R/W	PTP Rx FIFO is not empty

16.6.1.2 ETH System Control Register – ETH_SYS_CTRL

Address offset: 0x0004 ETH_SYS_CTRL

This register is used to configure the MAC.

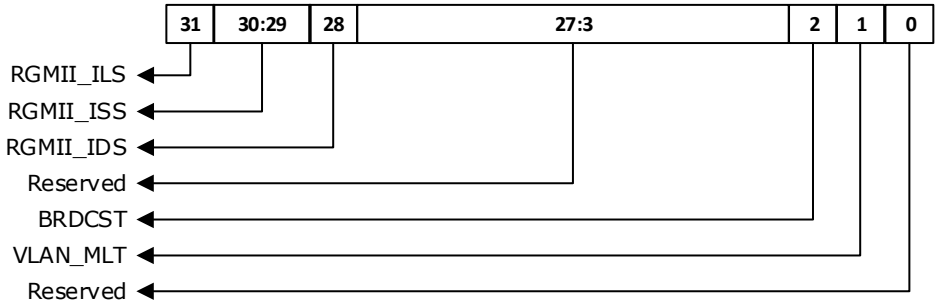


Table 16. ETH System Control Register bit assignments

Name	Bit	Reset	Dir	Description
RGMII_ILS	31	0	R	RGMII inband Link status
RGMII_ISS	30:29	0	R	RGMII inband speed status
RGMII_IDS	28	0	R	RGMII inband duplex status
Reserved	27:3	0	N/A	Reserved
BRDCST_EN	2	0	R/W	Set to allow broadcast to be received
VLAN_MLT_EN	1	0	R/W	Set to allow VLAN multicast to be received
Reserved	0	0	N/A	Reserved

16.6.1.3 ETH System Interrupt Set Register – ETH_SYS_INT_SET

Address offset: 0x0008 ETH_SYS_INT_SET

This register is used to set interrupts in the ETH module. See the ETH_SYS_INT_EN register for bit assignments. Write 1 to the corresponding bit to set an interrupt.

16.6.1.4 ETH System Interrupt Clear Register – ETH_SYS_INT_CLR

Address offset: 0x0004 ETH_SYS_INT_CLR

This register is used to clear interrupts in the ETH module. See the ETH_SYS_INT_EN register for bit assignments. Write 1 to the corresponding bit to clear an interrupt.

16.6.1.5 ETH System AV Control Register – ETH_SYS_AV_CTRL

Address offset: 0x0004 ETH_SYS_AV_CTRL

This register is used to configure the AV Shaper.

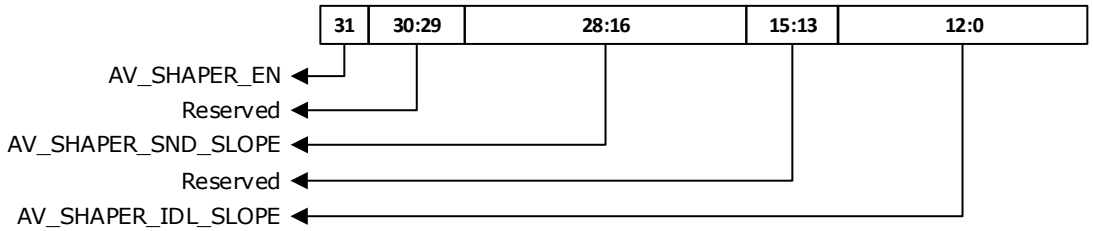


Table 16. ETH System AV Control Register bit assignments

Name	Bit	Reset	Dir	Description
AV_SHAPER_EN	31	0	R/W	AV Shaper enable
Reserved	30:29	0	N/A	Reserved
AV_SHAPER_SND_SLOPE	28:16	0	R/W	AV Shaper Send Slope (AVB engine only)
Reserved	15:13	0	N/A	Reserved
AV_SHAPER_IDL_SLOPE	12:0	0	R/W	AV Shaper Idle Slope (AVB engine only)

The AV shaper is only used by the AVB hardware talker logic and enables shaping as described in 802.1Q.

16.7 MAC Configuration

This module configures the MAC and provides access to the MDIO interface.
MAC Configuration registers are located at 0x40000300, which is the CYG_HAL_DICE3_ETH_MAC_CFG offset from the CYG_HAL_DICE3_ETH module base address.

Table 16.19 ETH MAC Configuration register summary

Address Offset	Register	Description
0x0000	ETH_MAC_IDENT	See *Ethernet MAC Identification Register*
0x0004	ETH_MAC_PHY_CFG	See *Ethernet MAC PHY Config Register*
0x0008	ETH_MAC_PHY_CMD	See *Ethernet MAC PHY Command Register*
0x000C	ETH_MAC_PHY_DATA	See *Ethernet MAC PHY Data Register*
0x0010	ETH_MAC_RX_CFG	See *Ethernet MAC PHY RX Config Register*
0x0020	ETH_MAC_TX_CFG	See *Ethernet MAC PHY TX Config Register*
0x0030	ETH_MAC_SPD_CFG	See *Ethernet MAC SPD Config Register*

16.7.1.1 ETH MAC Identification Register – ETH_MAC_IDENT

Address offset: 0x0000 ETH_MAC_IDENT

This register contains the version number of the ETH MAC module.

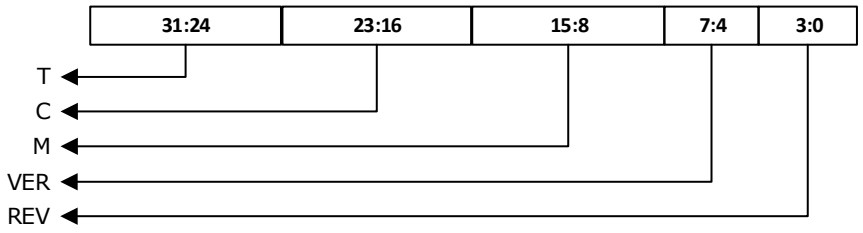


Table 16. ETH MAC Identification Register bit assignments

Name	Bit	Reset	Dir	Description
T	31:24	0x54	R	ASCII 'T'
C	23:16	0x43	R	ASCII 'C'
M	15:8	0x4D	R	ASCII 'M'
VER	7:4	0	R	Version of the module
REV	3:0	1	R	Revision of the module

16.7.1.2 ETH MAC PHY Configuration Register – ETH_MAC_PHY_CONFIG

Address offset: 0x0004 ETH_MAC_PHY_CONFIG

This register is used to enable and set the PRESCALE value.

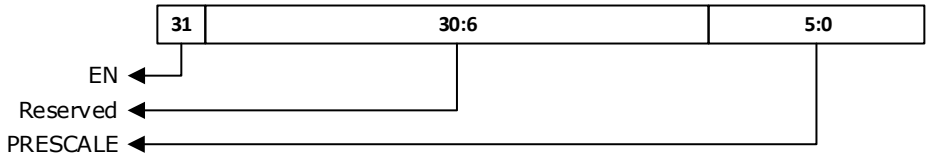


Table 16. ETH MAC PHY Configuration Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	R/W	Set to enable the ETH MAC Module
Reserved	30:6	0	N/A	Reserved
PRESCALE	5:0	0	R/W	Fmdio = Fsys_clk/(PRESCALE+1)

16.7.1.3 ETH MAC PHY Command Register – ETH_MAC_PHY_CMD

Address offset: 0x0008 ETH_MAC_PHY_CMD

This register is used to read or write PHY registers. Writing 1 to EXE will perform a Read or Write operation to the PHY. BUSY will go high in the following cycle and low when the operation is done. If WR is high a write operation is executed and if it is low a read operation is executed. The result will be in PHY_DATA when busy goes low. If RD is low a write operation is executed using data from PHY_DATA.

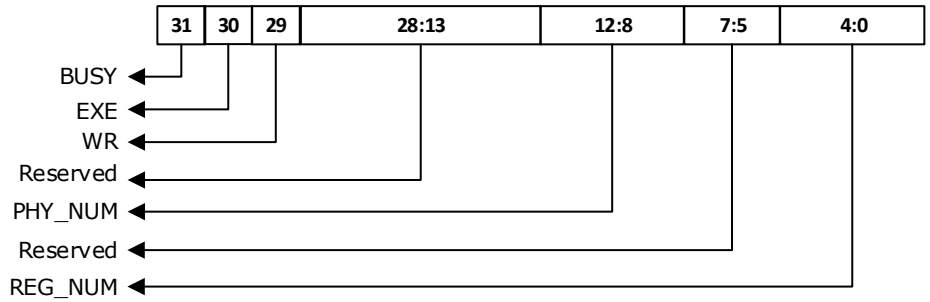


Table 16. ETH MAC PHY Command Register bit assignments

Name	Bit	Reset	Dir	Description
BUSY	31	0	R	Set while operation is in progress.
EXE	30	0	R/W	Writing 1 to EXE will perform a Read or Write operation to the PHY. BUSY will go high in the following cycle and low when the operation is done.
WR	29	0	R/W	Set for write operation, clear for read.
Reserved	28:13	0	N/A	Reserved
PHY_NUM	12:8	0	R/W	The PHY number.
Reserved	7:5	0	N/A	Reserved
REG_NUM	4:0	0	R/W	The register id in the PHY to access.

16.7.1.4 ETH MAC PHY Data Register – ETH_MAC_PHY_DATA

Address offset: 0x000C ETH_MAC_PHY_DATA

This register contains the value to write to a PHY register, or contains the result of a read.

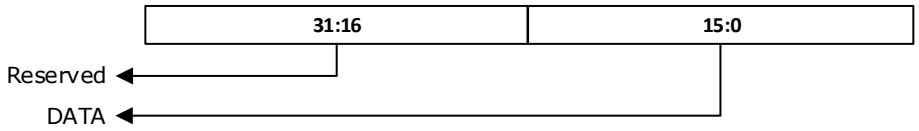


Table 16. ETH MAC PHY Data Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
DATA	0	0	R/W	Write value, or read result.

16.7.1.5 ETH MAC RX Configuration Register – ETH_MAC_RX_CFG

Address offset: 0x0010 ETH_MAC_RX_CFG

This register is used to

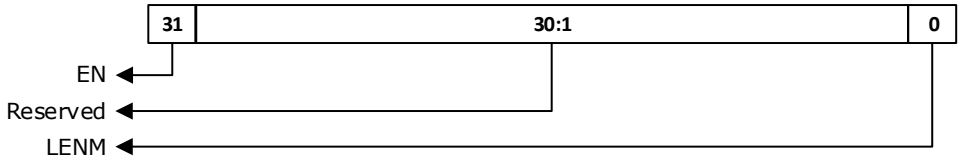


Table 16. ETH MAC RX Configuration Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	R/W	Set to enable the receiver.
Reserved	30:1	0	N/A	Reserved
LENM	0	0	R/W	If set Ethernet frames larger than 1522 bytes are discarded.

16.7.1.6 ETH MAC TX Configuration Register – ETH_MAC_TX_CFG

Address offset: 0x0020 ETH_MAC_TX_CFG

This register is used to enable the transmitter.

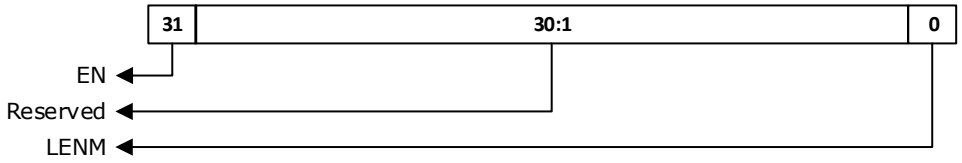


Table 16. ETH MAC TX Configuration Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	R/W	Set to enable the transmitter.
Reserved	30:0	0	N/A	Reserved

16.7.1.7 ETH MAC Speed Configuration Register – ETH_MAC_SPD_CFG

Address offset: 0x0000 ETH_MAC

This register is used to configure the data rate of the MAC.

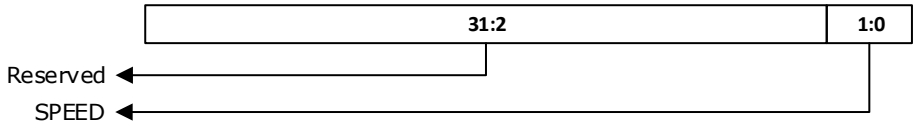


Table 16. ETH MAC Speed Configuration Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:2	0	N/A	Reserved
SPEED	1:0	0	R/W	Set the data rate of the MAC: 0: 10 Mbps 1: 100 Mbps 2: 1000 Mbps

16.8 MAC Statistics

This module keeps statistics of the Ethernet MAC.

The MAC Statistics registers are located at 0x40000380, which is the CYG_HAL_DICE3_ETH_MAC_STAT offset from the CYG_HAL_DICE3_ETH module base address.

The statistics registers maintain 32-bit counts of various events. Writing to any of these registers with bit 0 set will clear all counters.

Register Name	Dir	Offset	Description
ETH_MAC_STAT_RX_FCS	RW	0x0000	Received packets with CRC error
ETH_MAC_STAT_RX_BAD	RW	0x0004	Received packets with any error
ETH_MAC_STAT_RX_GOOD	RW	0x0008	Received packets with no error
ETH_MAC_STAT_TX_GOOD	RW	0x0040	Sent packets

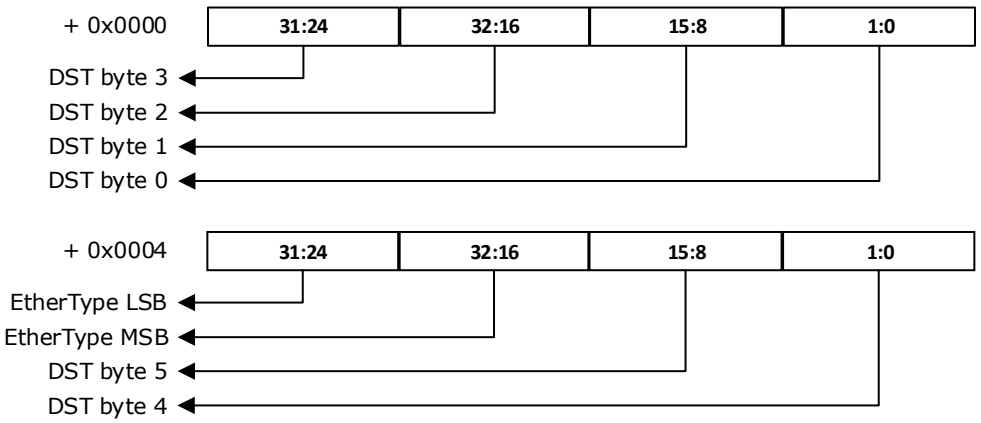
16.9 MAC Filter engine

The filter engine uses the destination address and the EtherType to determine if packets should be transferred to the Packet Receive FIFO. The filter takes load away from the firmware as it can pre-filter packets which are not destined for the device.

A total of 7 perfect filters are available together with a 64 bin multicast hash table.
If any of the filters allow the frame to pass, it will pass.

16.9.1 Perfect filters

Each perfect filter is programmed through 8 bytes of AND mask and 8 bytes of COMPARE mask. The first 6 bytes represent the destination address and the last two the EtherType. Note that the filter registers are Write Only.
It is only possible to write to the filter using 32 bit writes and the format is as follows both for the AND and COMPARE values.



16.9.2 Multicast Hash filter

The multicast hash filter will first create a hash of the destination address. This hash is the upper 6 bits of the CRC-32 of the address.
It will not allow the packet if:

- The least significant bit in the first byte of the address is 0 (not multicast)
- If the frame is VLAN tagged and bit 1 in the ETH_SYS_CTRL is clear.

If it passes the above check the 6 bit hash value is used to look up the programmed hash bit and if that bit is set the frame is allowed.

The register for the hash filter is made up of two 32 bit words, bits 0 to 31 in the first word corresponds to hash bin 0 to 31 and the bits 0 to 31 in the second word corresponds to hash bin 32 to 63.

NOTE: The registers for the perfect filters and the hash bins are not initialized after boot and will contain random values. Firmware must initialize these registers before enabling the MAC Rx function.

16.9.3 Filter registers

Filter Module registers are located at 0x40000400, which is the CYG_HAL_DICE3_ETH_FKT_BUF offset from the CYG_HAL_DICE3_ETH module base address.

Register Name	Dir	Offset	Description
FLT0_AND	W	0x0000	Two 32 bit words of AND mask
FLT0_CMP	W	0x0008	Two 32 bit words of COMPARE mask
FLT1_AND	W	0x0010	Two 32 bit words of AND mask
FLT1_CMP	W	0x0018	Two 32 bit words of COMPARE mask
FLT2_AND	W	0x0020	Two 32 bit words of AND mask
FLT2_CMP	W	0x0028	Two 32 bit words of COMPARE mask
FLT3_AND	W	0x0030	Two 32 bit words of AND mask
FLT3_CMP	W	0x0038	Two 32 bit words of COMPARE mask
FLT4_AND	W	0x0040	Two 32 bit words of AND mask
FLT4_CMP	W	0x0048	Two 32 bit words of COMPARE mask
FLT5_AND	W	0x0050	Two 32 bit words of AND mask
FLT5_CMP	W	0x0058	Two 32 bit words of COMPARE mask
FLT6_AND	W	0x0060	Two 32 bit words of AND mask
FLT6_CMP	W	0x0068	Two 32 bit words of COMPARE mask
MC_HASH	W	0x0070	Two 32 bit words with 64 hash bits

16.10 Revisions

Table 16.20 Document revision history

Date	Rev.	By	Change
July 17, 2015	1.0.0-41582	BK	Initial publication

