TCD3xxx Revision 0 Errata

Document Revision 1.0

November 21, 2014

CONTENTS

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1 Introduction

This document lists the errata in the original Rev0 version of the TCD3XXX (DICE III) chip family. These issues are all addressed in the Rev1 version of the DICE III.

The Rev0 version is identified by reading 0 from the CHIP_ID register in the SYS_CTL module, and Rev1 version may be identified by reading a 1.

Errata	Comment
MPMC – address range	The MPMC is connected such that only 16MB is available to each of the two chip selects
COMMRX/TX	These signals are not connected to the interrupt controller as expected
DMA Arbitration	The BusMatrix prioritizes the ARM CPU over the DMA controller, resulting in blocking the DMA
AVB Talker limit	The AVB Talkers only support 1 stream at the 100Mb Ethernet data rate
Ethernet Multicast Hash	The Ethernet receiver does not have a hash table for multicast reception
PEAK buffer	The Peak detector is using the running buffer instead of the stored buffer
Boot ROM	The boot ROM timeout for X-Modem is insufficiently long for interactive serial terminal use

Table 1, List of errata

2 Errata

2.1 MPMC Address range

Summary of Errata
The chip select scheme allows only 16MB access for each of two chip selects, for a total of 32MB addressable external memory.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	
TCD3020 Rev. 0	
TCD3040 Rev. 0	
TDC3070 Rev. 0	√

Overall Impact
Applications requiring external memories are limited to 2x16MB for a total of 32MB.

Workaround
None.

Course of Action
See below.

Rev 0
The following is implemented in Rev 0 of all versions of the TCD3xx, all affected versions.

SDRAM Address		CPU Address		DMA Address	
0x00000000	0x00FFFFFF	0x35000000	0x35FFFFFF	0x38000000	0x38FFFFFF

Table 2, Rev 0 SDRAM CS0

SDRAM Address		CPU Address		DMA Address	
0x00000000	0x00FFFFFF	0x36000000	0x36FFFFFF	0x3A000000	0x3AFFFFFF

Table 3, Rev 0 SDRAM CS1

Rev 1
The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

The chip select scheme for the MPMC is changed such that each of the two dynamic memory chip selects CS4 (chip CS0) and CS5 (chip CS1) each cover 64MB for a total of 128MB of dynamic memory.

SDRAM Address		CPU Address		DMA Address	
0x00000000	0x00FFFFFF	0x34000000	0x34FFFFFF	0x38000000	0x38FFFFFF
0x01000000	0x01FFFFFF	0x31000000	0x31FFFFFF	0x39000000	0x39FFFFFF
0x02000000	0x02FFFFFF	0x32000000	0x32FFFFFF	0x36000000	0x36FFFFFF
0x03000000	0x03FFFFFF	0x33000000	0x33FFFFFF	0x37000000	0x37FFFFFF

Table 4, Rev 1 SDRAM CS0

SDRAM Address		CPU Address		DMA Address	
0x00000000	0x00FFFFFF	0x38000000	0x38FFFFFF	0x3C000000	0x3CFFFFFF
0x01000000	0x01FFFFFF	0x35000000	0x35FFFFFF	0x3D000000	0x3DFFFFFF
0x02000000	0x02FFFFFF	0x36000000	0x36FFFFFF	0x3A000000	0x3AFFFFFF
0x03000000	0x03FFFFFF	0x37000000	0x37FFFFFF	0x3B000000	0x3BFFFFFF

Table 5, Rev 1 SDRAM CS1

The ranges have a different shuffle form the CPU and DMA point of view. The Virtual to Physical conversion in firmware accommodates this in a transparent manner.

2.2 COMM RX/TX

Summary of Errata
The COMM interrupts are not connected to the interrupt controller.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	√
TCD3020 Rev. 0	√
TCD3040 Rev. 0	√
TDC3070 Rev. 0	√

Overall Impact
This will likely not have any impact. None of the standard debuggers assume that interrupts are implemented for the debug communication interface.

Workaround
Debugging software should not be configured to rely on these interrupts..

Course of Action

The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

These two interrupts from the ARM will be connected to the interrupt controller line 2 and 3.

Signal	Interrupt Line
COMMRX	2
COMMTX	3

2.3 DMA Arbitration

Summary of Errata
The Layer1 bus has fixed priority over the Layer2 bus which means that the DMA's could be blocked when accessing internal memory in cases where the CPU is running code from internal memory.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	√
TCD3020 Rev. 0	√
TCD3040 Rev. 0	√
TDC3070 Rev. 0	√

Detailed Description
The DMAC and the DW_OTG are both DMA masters on the layer 2 bus. They can access peripherals and memory through the BusMatrix.

In the original design the Layer1 bus had fixed priority over the Layer2 bus which meant that the DMA's could be blocked when accessing internal memory in case the CPU was running code from internal memory.

Overall Impact
This means that peripherals and memory should not be accessed with DMA.

Workaround
The DMA can be made to work for devices with no strict latency requirement. Furthermore enabling the instruction cache or making sure that CPU and DMA are not both using the internal memory can mitigate the problem.

Course of Action
The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

The priority for the internal RAM is swapped so the DMA bus has priority.

2.4 AVB Talker Limit

Summary of Errata
AVB implementations that operate at the 100Mb data rate are limited to one talker stream. This limitation does not apply when the device is operating at the 1000Mb data rate where the limit is 16 streams. Reception of streams is not affected by this.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	
TCD3020 Rev. 0	
TCD3040 Rev. 0	√
TDC3070 Rev. 0	√

Detailed Description
When sending multiple streams at 100Mb the packets get concatenated because the FIFO never runs empty.

Overall Impact
AVB implementations that operate at the 100Mb data rate are limited to one talker stream.

Workaround
Only send one stream when the device is connected at 100MB.

Course of Action
The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

The logic has been simplified to fix the problem.

2.5 ETH Multicast Hash

Summary of Errata
The Ethernet MAC does not implement a multicast hashing algorithm for ingress packet filtering.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	
TCD3020 Rev. 0	
TCD3040 Rev. 0	√
TDC3070 Rev. 0	√

Detailed Description
In certain application where a lot of different multicast traffic is to be handled by firmware it is feasible to have a hash table based filter. This is not required for AVB multicast traffic as it is not handled by firmware.
Typical applications where this is feasible are switch management software and software implemented streaming of a large number of streams (AES67 etc.).

Overall Impact
In complex multicast applications the CPU will be burdened with the filtering.

Workaround
Firmware may implement this feature.

Course of Action

The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

The hash system uses a 64 bit bin and also looks at the multicast flag in the MAC address. It is also configurable whether VLAN tagged frames are filtered or not. Additional to the hash system the MAC has 7 perfect filters.

2.6 PEAK Buffer

Summary of Errata
When reading peaks, the peak buffer may not contain the latest peak values.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	√
TCD3020 Rev. 0	√
TCD3040 Rev. 0	√
TDC3070 Rev. 0	√

Detailed Description
The intention of the peak system was for the hardware to make measurements in a background buffer and the firmware read from a foreground buffer. The firmware instructs the hardware to swap the buffers when it requires a new measurement. The swap will result in the new background buffer being cleared.
The errata is concerned the fact that the firmware reads from the background buffer and not the foreground buffer.

Overall Impact
There is a small chance that a peak will be missed in the time from the firmware reading the highest value till the firmware asks to clear it. This will typically only be a few samples in time so for typical musical content the likelihood of being off by more than 1dB is very small.

Workaround
Issuing the peak clear as fast as possible minimizes the issue and the error will be academic for most applications.

Course of Action

The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

The correct buffer is available in the read buffer after a snapshot.

2.7 Boot ROM

Summary of Errata
The timeout for X-Modem firmware loading at boot time is too short for manual interaction.

DICE III variants affected

DICE III version	
TCD3000 Rev. 0	√
TCD3020 Rev. 0	√
TCD3040 Rev. 0	√
TDC3070 Rev. 0	√

Detailed Description
During boot, the DICE III may be booted via X-Modem serial transfer. The boot program waits for an initialization character on UART0, however the boot ROM was not correctly setting the time for timeouts. The timer was set as a 16 bit timer and not 32 bit.

Overall Impact
X-Modem interaction with the Rev 0 DICE III cannot consistently be done via generic serial terminal.

Workaround
X-Modem boot must be implemented using a programmed serial program such as a custom application.

Course of Action

The following is implemented in Rev 1 of all versions of the TCD3xx, all affected versions.

A larger timer is used for the timeout, providing a reasonable interval for manual X-Modem boot operation.

Furthermore the version of the ROM is changed to 1.1.0.2477

2.8 Revisions

Table 2.6 Document revision history

Date	Rev.	By	Change
October 25, 2014	0.1	BK	Initial draft
November 14, 2014	0.2	BK	Edits based on doc review
November 21, 2014	1.0	BK	Rev 1.0

