AES/SPDIF Receiver and Transmitter

AES3/SPDIF RX AND TX

Revision 0.9.0-41360

May 6, 2015

List of Tables

List of Figures

NO TABLE OF FIGURES ENTRIES FOUND.

22 AES Receiver and Transmitter

22.1 AES Receiver

22.1.1 Overview

The DICE AES Receiver is a stereo AES3/SPDIF receiver supporting sampling rates up to 96kHz. It contains two parts; a sync extractor and a data receiver.

The sync extractor uses sys_clk to detect X/Z preambles for feeding to the JET_PLL. In order to detect the sync correctly the system needs to be run through as software state machine. The state machine will constantly try different combinations of MIN_PER, MAX_PER and LONG_THR and look for SYNC_SC being set with no errors.

MIN_PER = sys_clk/(4*(Fs - p%))

MAX_PER = sys_clk/(4*(Fs + p%))

LONG_THR = 2.5*sys_clk/(128Fs) - 1.5

The standard firmware is using the following table.

Table 22.1 Standard firmware setting sets

Sampling Rate	MIN_PER	MAX_PER	LONG_THR
32KHz	346	422	59
44.1KHz	268	307	42
48KHz	230	267	39
88.2KHz	134	153	20
96KHz	115	133	19

The software state machine will try one set at a time, after about 20ms it will check if SYNC_SC is set, and if it is it will clear SERR and go to the check state. If not it will try the next set (round robin).

After about 20ms in the check state it will check SERR again and if not set, the state is synchronized.

In the synchronized state it will look for sync errors and go back to polling if an error is found.

With the 5 possible sets it, will typically take a maximum of 100ms to find the correct rate.

The data extractor assumes that the JET PLL is either locked to the AESSYNC or that the JET PLL is somehow the master of the clock driving the AES signal being received.

22.1.2 Module Configuration

The AES receiver is addressed through 1 base address:

Table 22.2 AES Receiver base address

Base address	Description
0xC4000700	DICE3_AES_RX – AES Receiver

Table 22.3 AES Receiver register summary

Address Offset	Register	Description
0x0000	AES_RX_GCTL0	*AES RX Control0 Register*
0x0004	AES_RX_GCTL1	*AES RX Control1 Register*
0x0008	AES_RX_GSTAT	*AES RX Status Register*
0x0010 – 0x001C	AES_RXn_CSR	*AES RXn CSR Register*
0x0020	AES_RX_CS0_3	*AES RX CS0-3 Register*
0x0024	AES_RX_CS4	*AES RX CS4 Register*

22.1.3 AES Control0 Register – AES_RX_GCTL0

Address offset: 0x0000 AES_RX_GCTL0

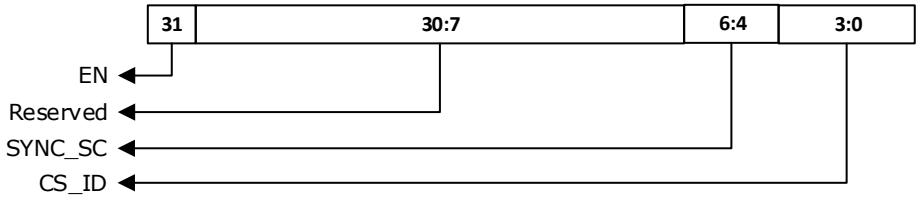

Table 22.4 AES Control0 Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	RW	Enable the receiver device
Reserved	30:7	0	N/A	Reserved
SYNC_SC	6:4	0	RW	device to synchronize from
CS_ID	3:0	0	RW	channel to take channel status from 0=left0, 1=right0, 2=left1, 3=right1 ....

22.1.4 AES Control1 Register – AES_RX_GCTL1

Address offset: 0x0004 AES_RX_GCTL1

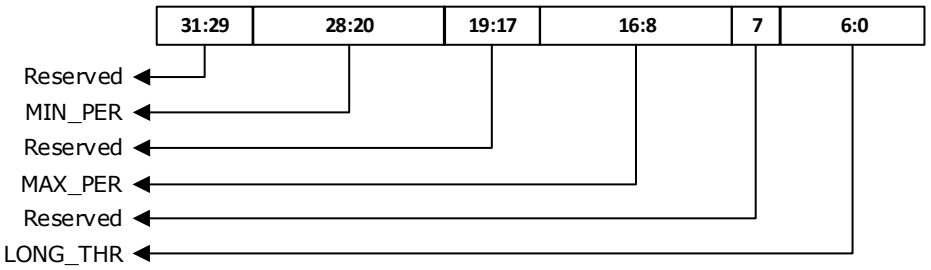

Table 22.5 AES Control1 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:29	0	N/A	Reserved
MIN_PER	28:20	0	RW	minimum frame period in sys_clk/8 counts
Reserved	19:17	0	N/A	Reserved
MAX_PER	16:8	0	RW	maximum frame period in sys_clk/8 counts
Reserved	7	0	N/A	Reserved
LONG_THR	6:0	0	RW	threshold for a long pulse in sys_clk counts

22.1.5 AES Status Register – AES_RX_GSTAT

Address offset: 0x0008 AES_RX_GSTAT

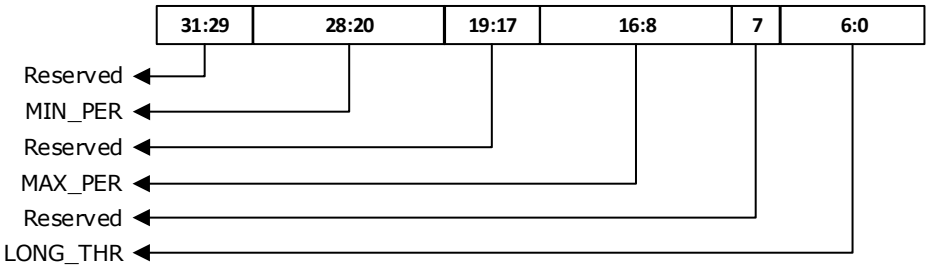

Table 22.6 AES_RX_GSTAT Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:29	0	N/A	Reserved
PERIOD	28:20	0	RW	period
Reserved	19:9	0	N/A	Reserved
CSV	8	0	RW	set to one after two consecutive block sync's, clear by writing 1 (from CS_ID)
Reserved	7:2	0	N/A	Reserved
SYNC	1	0	RW	device is currently synchronized (32 consecutive frames within MIN_PER and MAX_PER)
SERR	0	0	RW	sync error detected, sticky, clear by writing 1

22.1.6 AES_RXn_CSR Register – AES_RXn_CSR

Address offset: 0x00010-0x001C AES_RXn_CSR

This register is typical of five: n=0-4.

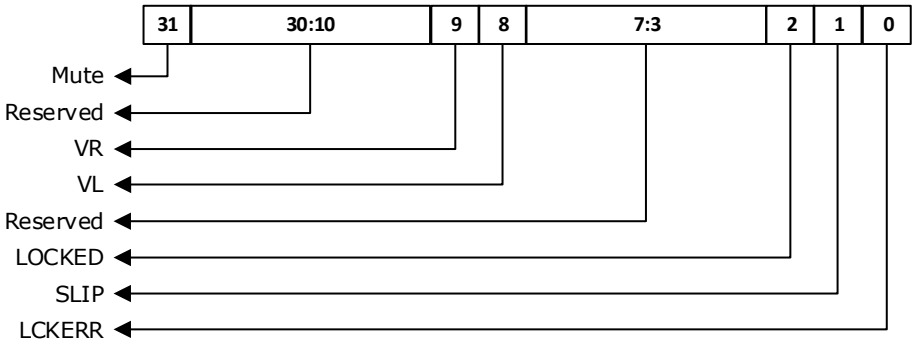

Table 22.7 AES_RXn_CSR Register bit assignments

Name	Bit	Reset	Dir	Description
MUTE	31	0	RW	Set to mute the device
Reserved	30:10	0	N/A	Reserved
VR	9	0	RW	VR
VL	8	0	RW	VL
Reserved	7:3	0	N/A	Reserved
LOCKED	2	0	RW	lock error detected, sticky, clear by writing 1
SLIP	1	0	RW	slip error detected, sticky, clear by writing 1
LCKERR	0	0	RW	device is currently synchronized (16 consecutive frames with no biphase error)

22.1.7 AES_RX_CS0_3 Register – AES_RX_CS0_3

Address offset: 0x0020 AES_RX__CS0_3

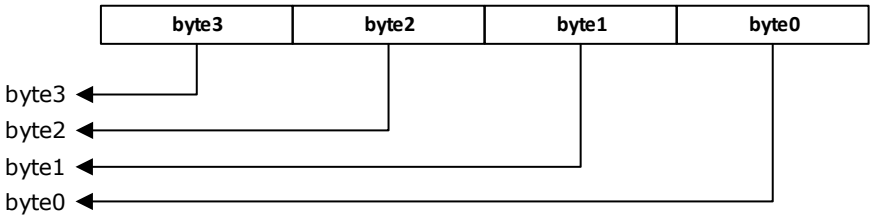

Table 22.8 AES_RX_CS0_3 Register bit assignments

Name	Bit	Reset	Dir	Description
byte3	31:23	0	RW	Byte 3
byte2	22:16	0	RW	Byte 2
byte1	15:8	0	RW	Byte 1
byte0	7:0	0	RW	Byte 0

22.1.8 AES_RX_C4 Register – AES_RX_CS4

Address offset: 0x0024 AES_RX_CS4

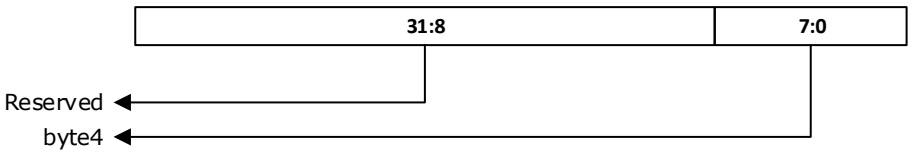

Table 22.9 AES_RX_CS4 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
Byte4	7:0	0	RW	Byte 4

22.2 AES Transmitter

22.2.1 Module Configuration

The AES Transmitter is addressed through 1 base address:

Table 22.10 AES Transmitter base address

Base address	Description
0xC4000800	DICE3_AES_TX – AES Transmitter

Table 22.11 AES Transmitter register summary

Address Offset	Register	Description
0x0000	AES_TX_CTRL	*AES TX Control Register*
0x0004	AES_TX_CS0_3	*AES TX CS0-3 Register*
0x0008	AES_TX_CS4	*AES TX CS4 Register*

22.2.2 AES TX Control Register – AES_TX_CTRL

Address offset: 0x0000 AES_TX_CTRL

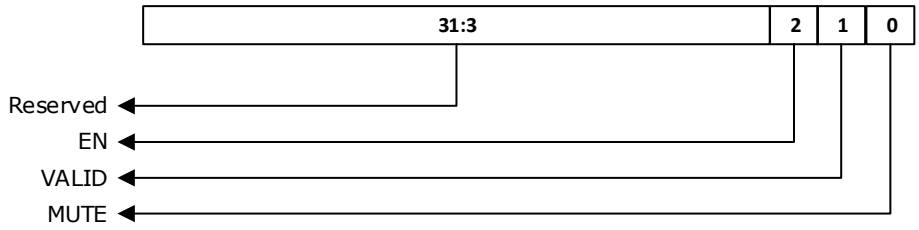

Table 22.12 AES_RX_CS4 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	N/A	Reserved
EN	2	0	RW	Set to enable the device
VALID	1	0	RW	Valid
MUTE	0	0	RW	Set to mute the device

22.2.3 AES_TX_CS0_3 Register – AES_TX_CS0_3

Address offset: 0x0004 AES_TX_CS0_3

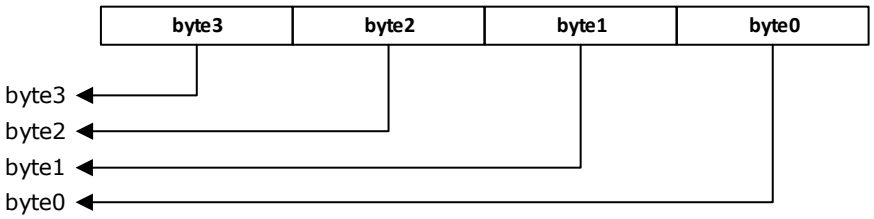

Table 22.13 AES_TX_CS0_3 Register bit assignments

Name	Bit	Reset	Dir	Description
byte3	31:23	0	RW	Byte 3
byte2	22:16	0	RW	Byte 2
byte1	15:8	0	RW	Byte 1
byte0	7:0	0	RW	Byte 0

22.2.4 AES_TX_CS4 Register – AES_RX_CS4

Address offset: 0x0008 AES_TX_CS4

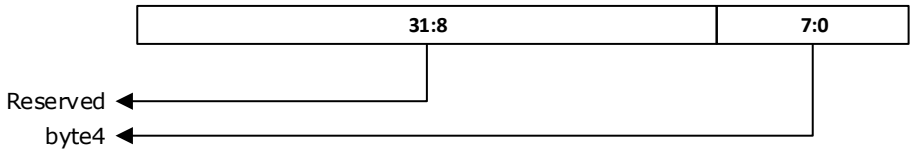

Table 22.14 AES_TX_CS4 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
byte4	7:0	0	RW	Byte 4

22.3 Revisions

Table 22.15 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

