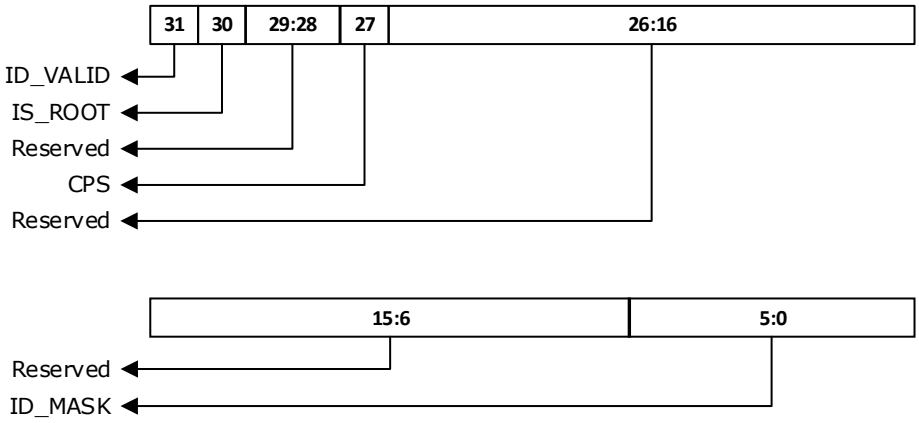
TCAT 1394 LLC

Link Layer Controller

Revision 0.9.0-41360

May 6, 2015

List of Tables



List of Figures

NO TABLE OF FIGURES ENTRIES FOUND.

17 TCAT 1394 LLC

17.1 Overview

The TCAT LLC implements an IEEE1394-2008 compliant Link Layer Controller supporting speeds up to S800. It is using the Beta PHY-link interface.
The LLC supports the following features:

- Beta PHY-link Direct only
- TCAT-SI Host interface Synchronous to PHY clock
- TCAT-SI Memory Interface Asynchronous
- Isochronous Receive port (raw, all Isoc data)
- Isochronous Transmit port, 4 channels

17.2 Module Configuration

Table 17.1 TCAT LLC module base addresses

Base address	Name	Description
0x50000000	DICE3_LLC_BUF	Packet Buffers
0x60000000	DICE3_LLC_REG	Control and Status Registers

Table 17.2 LLC Module Control and Status register summary

Address	Register	Description
0x0000	TC_LLC_IDENT	*LLC Identity Register*
0x0004	TC_LLC_MISC_CTRL_SET	*LLC Misc Control Set Register*
0x0008	TC_LLC_MISC_CTRL_CLR	*LLC Misc Control Clear Register*
0x000C	TC_LLC_NODE_INFO	*LLC Node Info Register*
0x0010	TC_LLC_CYCLE_TIMER	*LLC Cycle Timer Register*
0x0014	TC_LLC_ASYNC_RX_PUT	*LLC Async Rx Put Register*
0x0018	TC_LLC_ASYNC_RX_GET	*LLC Async Rx Get Register*
0x001C	TC_LLC_ASYNC_TX	*LLC Async Tx Register*
0x0020	TC_LLC_INTERRUPT	*LLC Interrupt Register*
0x0024	TC_LLC_INT_MASK_SET	*LLC Interrupt Mask Set Register*
0x0028	TC_LLC_INT_MASK_CLR	*LLC Interrupt Mask Clear Register*
0x002C	TC_LLC_PHY	*LLC PHY Access Register*
0x0030	TC_LLC_ISOC_TX0	*LLC Isochronous Tx 0 Register*
0x0034	TC_LLC_ISOC_TX1	*LLC Isochronous Tx 1 Register*
0x0038	TC_LLC_ISOC_TX2	*LLC Isochronous Tx 2 Register*
0x003C	TC_LLC_ISOC_TX3	*LLC Isochronous Tx 3 Register*

Table 17.3 LLC Module Buffer Memory Map

Address	Register	Description
0x0000-0x07FF	TC_LLC_TX_BUF_OFS	Transmit buffer, 2048bytes
0x0800-0x0FFF	Reserved	Reserved
0x1000-0x17FF	TC_LLC_RX_BUF_OFS	Receive buffer, 2048 bytes
0x1800-0x1FFF	TC_LLC_RX_BUF_OFS	Mirror of receive buffer

17.2.1 Addressing

All registers in the LLC Module are addressed at 32-bit boundaries to remain consistent with the AHB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

17.2.2 LLC Register – TC_LLC_IDENT

Address offset: 0x0000 TC_LLC_IDENT

This register contains the identity and instance version for the module.

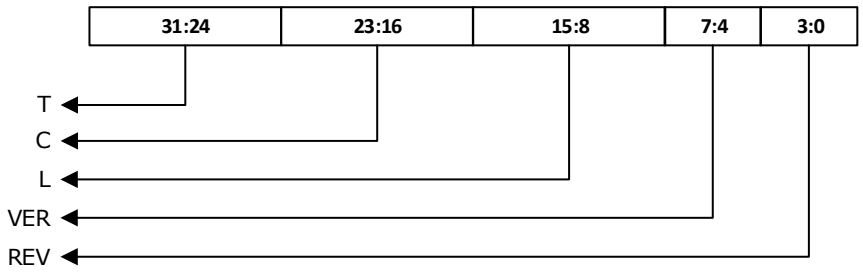


Table 17.4 LLC Identity Register bit assignments

Name	Bit	Reset	Dir	Description
T	31:24	0x54	R	T
C	23:16	0x43	R	C
L	15:8	0x4C	R	L
VER	7:4	1	R	Version
REV	3:0	0	R	Revision

17.2.3 LLC Miscellaneous Control Set Register – TC_LLC_MISC_CTRL_SET

Address offset: 0x0004 TC_LLC_MISC_CTRL_SET

Writing a '1' to a bit in the TC_LLC_MISC_CTRL_SET register will set the bit. Writing a '1' to the TC_LLC_MISC_CTRL_CLR register will clear the bit. Writing '0' will have no effect. Reading either register will return the current setting.

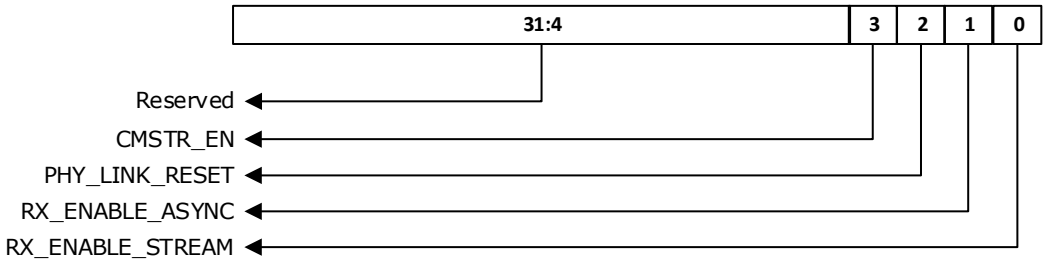


Table 17.5 LLC Miscellaneous Control Set Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	N/A	Reserved
CMSTR_EN	3	0	R/W	If this bit is set the LLC will send cycle starts if it is also the root as indicated by the TC_LLC_NODE_INFO register.
PHY_LINK_RESET	2	0	R/W	Setting this bit will reset the PHY-Link interface using the LPS signal. This bit will read as zero when the reset is complete.
RX_ENABLE_ASYNC	1	0	R/W	0: packets will not be put into the buffer and busy_x will be returned. 1: Asynchronous packets addressed to this node (or broadcast) will be received into the buffer. If the buffer is full busy_x will be acknowledged. If the packet is stored the appropriate acknowledge will be sent.
RX_ENABLE_STREAM	0	0	R/W	If set Asynchronous stream packets will be put into the buffer. Stream packets are never acknowledged.

17.2.4 LLC Miscellaneous Control Clear Register – TC_LLC_MISC_CTRL_CLR

Address offset: 0x0008 TC_LLC_MISC_CTRL_CLR

Writing a '1' to a bit in the TC_LLC_MISC_CTRL_SET register will set the bit. Writing a '1' to the TC_LLC_MISC_CTRL_CLR register will clear the bit. Writing '0' will have no effect. Reading either register will return the current setting.

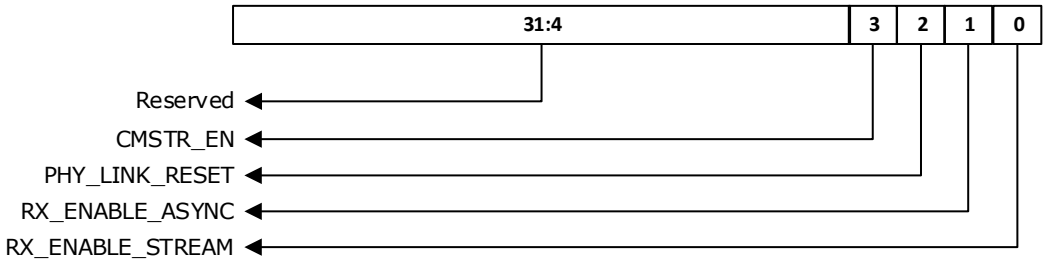


Table 17.6 LLC Miscellaneous Control Set Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	N/A	Reserved
CMSTR_EN	3	0	R/W	If this bit is set the LLC will send cycle starts if it is also the root as indicated by the TC_LLC_NODE_INFO register.
PHY_LINK_RESET	2	0	R/W	Setting this bit will reset the PHY-Link interface using the LPS signal. This bit will read as zero when the reset is complete.
RX_ENABLE_ASYNC	1	0	R/W	0: packets will not be put into the buffer and busy_x will be returned. 1: Asynchronous packets addressed to this node (or broadcast) will be received into the buffer. If the buffer is full busy_x will be acknowledged. If the packet is stored the appropriate acknowledge will be sent.
RX_ENABLE_STREAM	0	0	R/W	If set Asynchronous stream packets will be put into the buffer. Stream packets are never acknowledged.

17.2.5 LLC Node Info Register – TC_LLC_NODE_INFO

Address offset: 0x000C TC_LLC_NODE_INFO

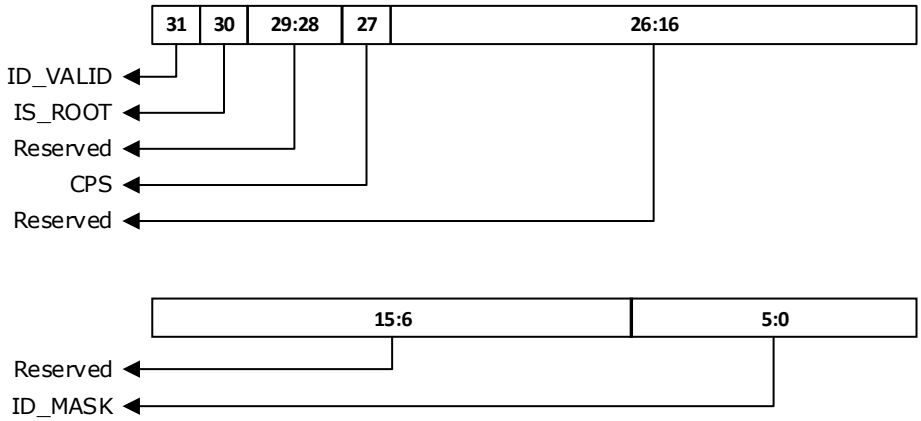


Table 17.7 LLC Node Info Register bit assignments

Name	Bit	Reset	Dir	Description
ID_VALID	31	0	R	Set if the Node ID is valid. Cleared by reset, bus_reset, phy-link init. Set when an unsolicited reg0 read is received from the PHY.
IS_ROOT	30	0	R	Set if the information from the last unsolicited reg0 read indicates that this node is root.
Reserved	29:28	0	N/A	Reserved
CPS	27	0	R	Set according to the CPS field from the last unsolicited reg0 read.
Reserved	26:6	0	N/A	Reserved
ID_MASK	5:0	0	R	Set according to the ID field from the last unsolicited reg0 read.

17.2.6 LLC Cycle Timer Register – TC_LLC_CYCLE_TIMER

Address offset: 0x0010 TC_LLC_CYCLE_TIMER

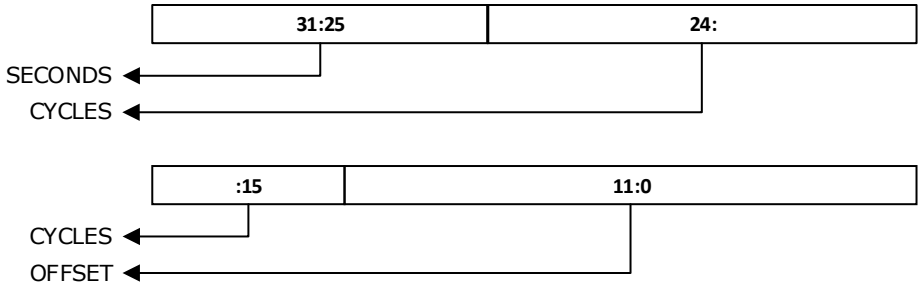


Table 17.8 LLC Cycle Timer Register bit assignments

Name	Bit	Reset	Dir	Description
SECONDS	31:25	0	R/W	Seconds counter of the cycle timer. Wraps every 128 seconds.
CYCLES	24:15	0	R/W	Cycles. Wraps every 8000 cycles.
OFFSET	15:0	0	R/W	Offset, wraps every 3072 counts.

17.2.7 LLC Asynchronous Rx Put Register – TC_LLC_ASYNC_RX_PUT

Address offset: 0x0014 TC_LLC_ASYNC_RX_PUT

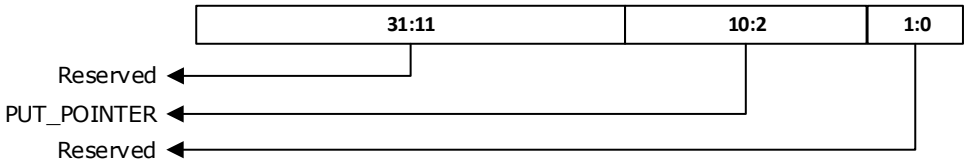


Table 17.9 LLC Asynchronous Rx Put Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
PUT_POINTER	10:2	0	R	Current put pointer in rx buffer. If PUT == GET then the buffer is empty. The buffer is store before increment so the value at buffer[PUT] is not written.
Reserved	1:0	0	N/A	Reserved

17.2.8 LLC Asynchronous Rx Get Register – TC_LLC_ASYNC_RX_GET

Address offset: 0x0018 TC_LLC_ASYNC_RX_GET

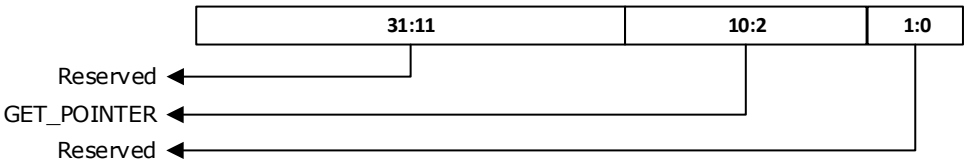


Table 17.10 LLC Asynchronous Rx Get Register bit assignments

Name	Bit	Reset	Dir	Description

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
GET_POINTER	10:2	0	R	Current get pointer in rx buffer. If PUT == GET then the buffer is empty. The application should set the GET pointer to the position immediately after the last quadlet of the last read packet.
Reserved	1:0	0	N/A	Reserved

17.2.9 LLC Asynchronous Transmit Register – TC_LLC_ASYNC_TX

Address offset: 0x001C TC_LLC_ASYNC_TX

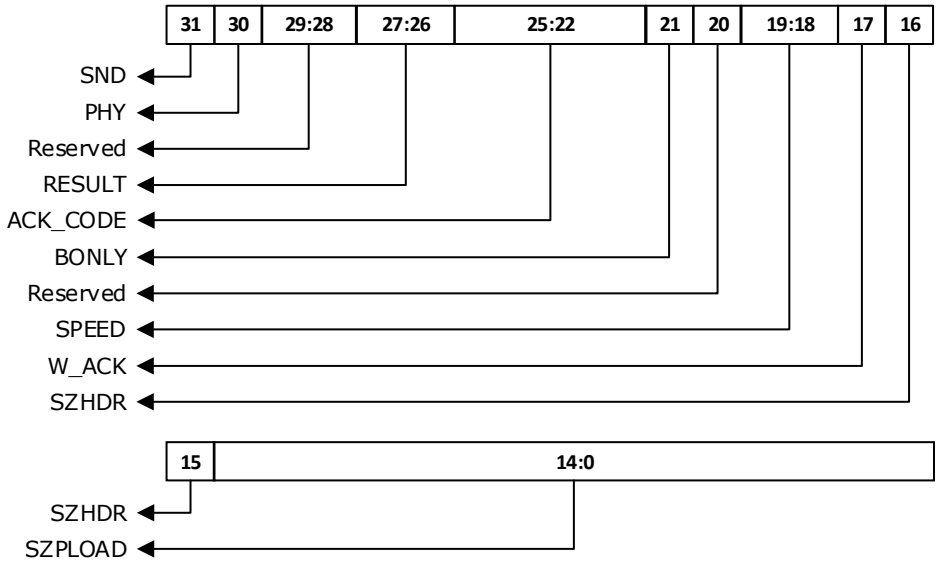


Table 17.11 LLC Asynchronous Transmit Register bit assignments

Name	Bit	Reset	Dir	Description
SND	31	0	R/W	Writing a '1' will start transmission. The bit will clear when the transmission is completed with or without error, or at a bus_reset.
PHY	30	0	R/W	If this bit is set a PHY packet will be sent.
Reserved	29:28	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
RESULT	27:26	0	R	Result of operation (valid when SND is clear) 00: Packet sent, no ACK received 01: Packet sent, ACK received (see ACK_CODE) 10: Packet sent, illegal ACK checksum 11: Packet canceled (bus reset etc.)
ACK_CODE	25:22	0	R	Standard IEEE1394 ACK Codes.
BONLY	21	0	R/W	If set use Beta mode, if clear PHY decides.
Reserved	20	0	N/A	Reserved
SPEED	19:18	0	R/W	Bus speed to use to send packet: 00: S100 01: S200 10: S400 11: S800
W_ACK	17	0	R/W	If set the system will wait for an ACK, if clear it will not.
SZHDR	16:15	0	R/W	The size of the header: 00: Size=1 quadlet (use for PHY) 01: Size=2 10: Size=3 11: Size=4
SZPLOAD	14:0	0	R/W	The size of the payload in bytes.

17.2.10 LLC Interrupt Register – TC_LLC_INTERRUPT

Address offset: 0x0020 TC_LLC_INTERRUPT

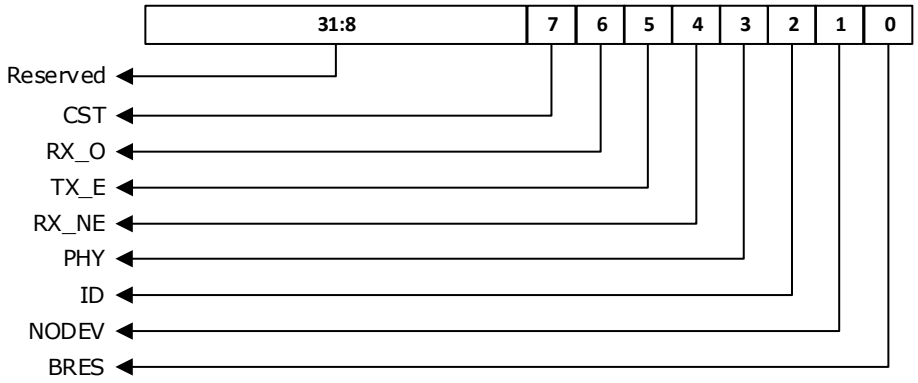


Table 17.12 LLC Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:10	0	N/A	Reserved
CST		0	R/W	Set when a cycle start is received. Cleared by writing 1.
RX_O		0	R/W	Set when a packet is rejected because the buffer is full, cleared by writing 1.
TX_E		1	R	Cleared by starting transmission, set when done, set by init and bus_reset.
RX_NE		0	R	Set when rx buffer is not empty, cleared when rx buffer is empty.
PHY		0	R/W	Set if a PHY interrupt is received, cleared by writing 1.
ID		0	R	Set when ID phase is over, cleared by init and bus_reset.
NODEV		0	R	Set when node ID is valid, cleared by init and bus_reset
BRES		0	R/W	Set at bus reset, cleared by writing 1.

17.2.11 LLC Interrupt Mask Set Register – TC_LLC_INT_MASK_SET

Address offset: 0x0024 TC_LLC_INT_MASK_SET

Writing a '1' to a bit in the TC_LLC_INT_MASK_SET register will set the bit. Writing a '1' to the TC_LLC_INT_MASK_CLR register will clear the bit. Writing '0' will have no effect. Reading either register will return the current setting. The register layout is the same as TC_LLC_INTERRUPT.

17.2.12 LLC Interrupt Mask Clear Register – TC_LLC_INT_MASK_CLR

Address offset: 0x0028 TC_LLC_INT_MASK_CLR

Writing a '1' to a bit in the TC_LLC_INT_MASK_SET register will set the bit. Writing a '1' to the TC_LLC_INT_MASK_CLR register will clear the bit. Writing '0' will have no effect. Reading either register will return the current setting. The register layout is the same as TC_LLC_INTERRUPT.

17.2.13 LLC PHY Access Register – TC_LLC_PHY

Address offset: 0x002C TC_LLC_PHY

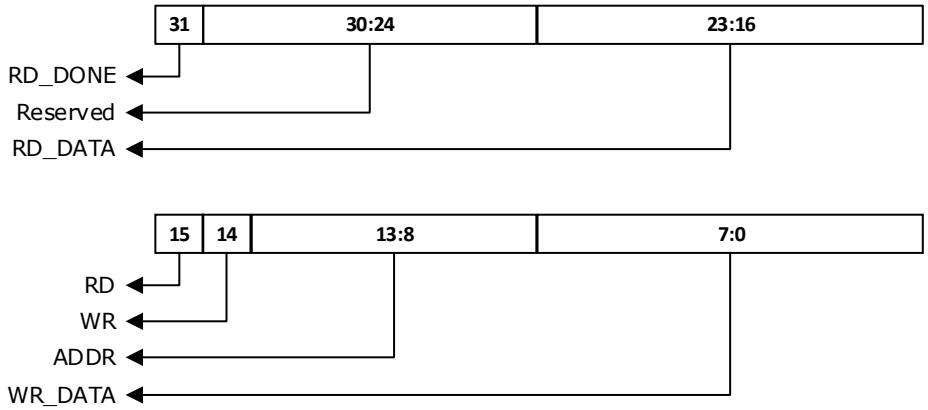


Table 17.13 LLC PHY Access Register bit assignments

Name	Bit	Reset	Dir	Description
RD_DONE	31	0	R	Set when a read operation is complete and data is available. Cleared when a read operation is initiated.
Reserved	30:24	0	N/A	Reserved
RD_DATA	23:16	0	R/W	Result of a read operation. The data is valid when RD_DONE is high.
RD	15	0	R/W	Writing a '1' to this bit will initiate a read operation from the address specified in ADDR. If the WR bit is set at the same time the result is unpredictable. This bit will read as '1' until the operation is completed.
WR	14	0	R/W	Writing a '1' to this bit will initiate a write operation from the address specified in ADDR. If the RD bit is set at the same time the result is unpredictable. This bit will read as '1' until the operation is completed.
ADDR	13:8	0	R/W	The register address to read from or write to.
WR_DATA	7:0	0	R/W	The data to write when a write operation is selected.

17.2.14 LLC Isochronous Transmit n Register – TC_LLC_ISOC_TXn

Address offset: 0x0030-0x003C TC_LLC_ISOC_TXn

Each of the four isochronous transmitters are configured according to the following layout.

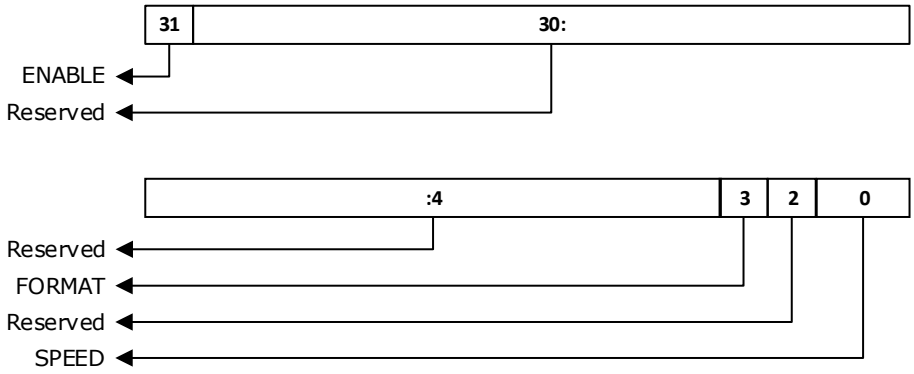


Table 17.14 LLC Isochronous Transmit n Register bit assignments

Name	Bit	Reset	Dir	Description
ENABLE	31	0	R/W	When set this port is enabled. If the corresponding llc_tx_en[n] signal is set an isochronous transfer will be initiated for each isochronous cycle.
Reserved	30:4	0	N/A	Reserved
FORMAT	3	0	R/W	If set use Beta mode, if clear PHY decides.
Reserved	2	0	N/A	Reserved
SPEED	1:0	0	R/W	Bus speed to use to send packet: 00: S100 01: S200 10: S400 11: S800

17.3 Memory Buffer Layout

The TCAT LLC uses two memory spaces, one for packet transmission and one for packer reception.

17.3.1 Receive Buffer

The receive buffer is 512 quadlets (2048 bytes) in size. The two pointers specified in the register definition are used in conjunction with this buffer. If PUT == GET the buffer is empty. If the two pointers are different there are one or more packets in the buffer. The buffer is circular but it is mirrored once to facilitate simple unwrapped copy operations to be performed.

Each packet is preceded by a status quadlet of the following format:

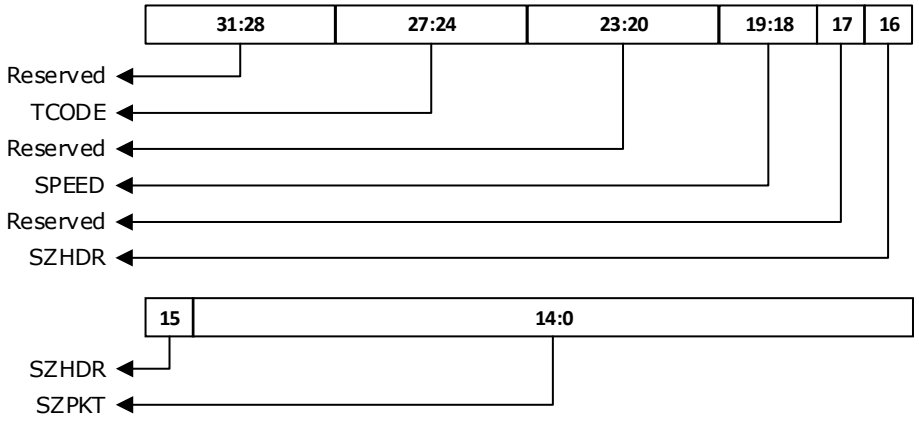


Table 17.15 LLC Isochronous Receive Status Quadlet bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:28	0	N/A	Reserved
TCODE	27:24	0	R	TCODE of the received packet. A special value of 0x0E is used for PHY packets.
Reserved	23:20	0	N/A	Reserved
SPEED	19:18	0	R	Bus speed used for the packet: 00: S100 01: S200 10: S400 11: S800
Reserved	17	0	N/A	Reserved
SZDHR	16:15	0	R	Size of header in quadlets – 1.
SZPKT	14:0	0	R	Size of the complete packet in quadlets not including this status quadlet.

The principle for receiving packets is to look for PUT != GET. Then read the status quadlet from buffer[GET]. Read the packet and set GET=GET+(1+SZPKT)*4.

17.3.2 Transmit Buffer

The transmit buffer only holds one packet. The buffer should not be written while a transmission is pending. The layout of the transmit buffer is simply the IEEE1394 packet not including CRC's. For PHY packets only one quadlet is supplied.

17.4 Revisions

Table 17.16 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

