System Control

Clocking and Power Management

Revision 0.9.0-41360

May 6, 2015

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3.1 Overview

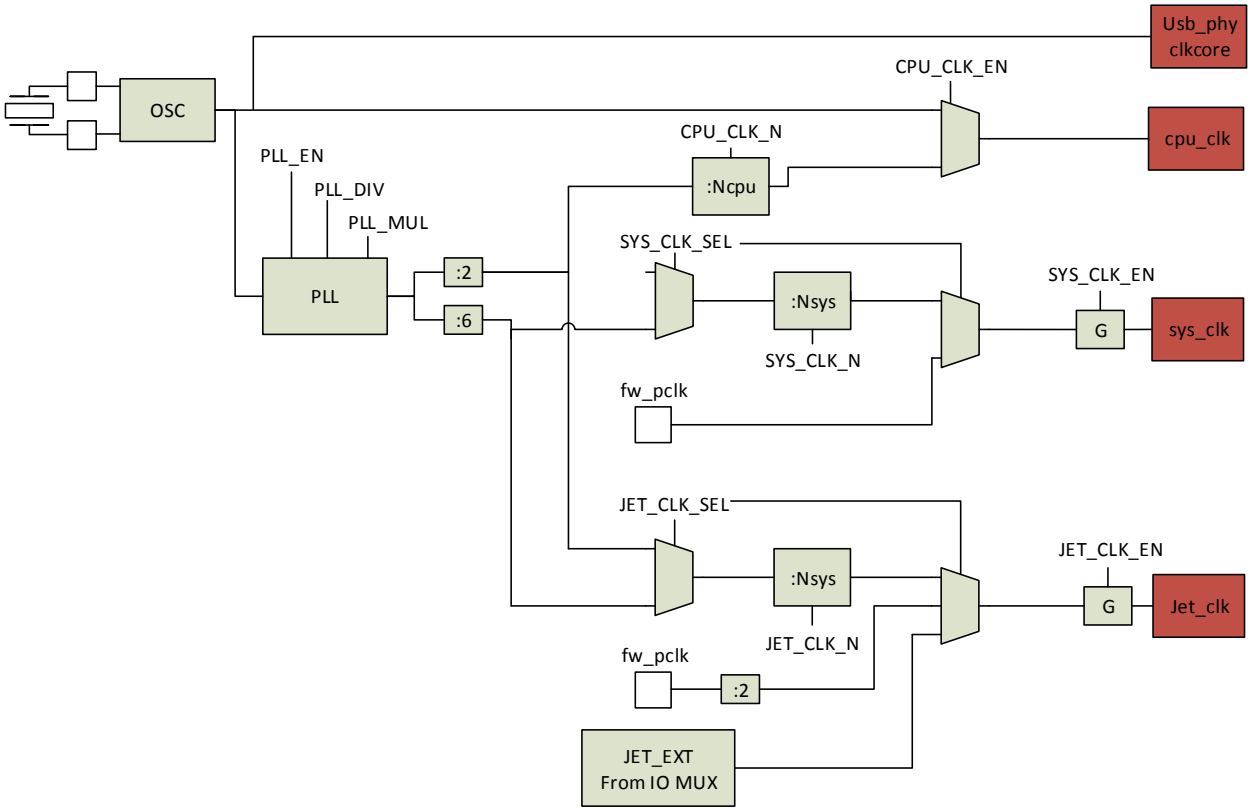

Figure 1, Clocks

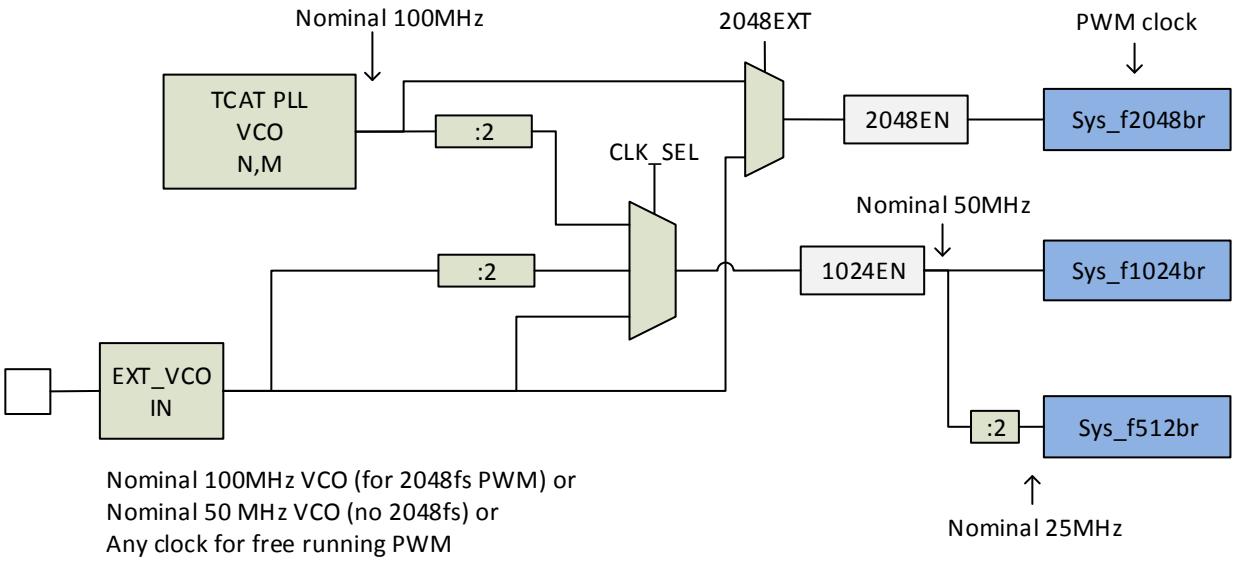

Figure 2, Clocks

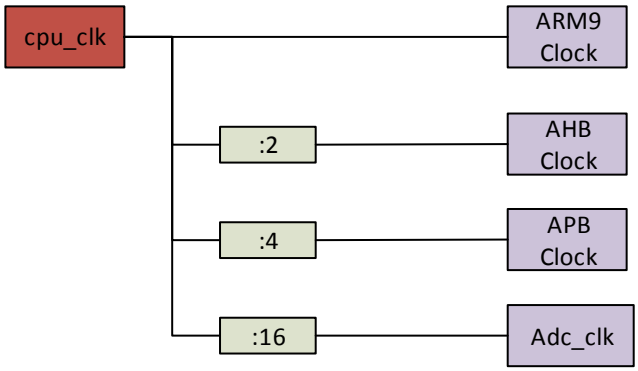

Figure 3, Clocks

3.2 Module Configuration

The System Control module is addressed through 1 base address:

Table 3.1 System Control Module base address

Base address	Description
0xC9000000	HAL_DICE3_SYS_CTL – System Control

Table 3.2 System Control Module register summary

Address Offset	Register	Description
0x0000	HAL_DICE3_SYS_CTL_CPU_PLL	*CPU PLL Control Register*
0x0008	HAL_DICE3_SYS_CTL_SYS_CLK	*System Clock Control Register*
0x000C	HAL_DICE3_SYS_CTL_CPU_CLK	*CPU Clock Control Register*
0x0010	HAL_DICE3_SYS_CTL_SDIO_CLK	*SDIO Clock Control Register*
0x0014	HAL_DICE3_SYS_CTL_ADC_CLK	*ADC Clock Control Register*
0x0018	HAL_DICE3_SYS_CTL_JET_CLK	*JET PLL™ Clock Control Register*
0x001C	HAL_DICE3_SYS_CTL_AUDIO_CLK	*Audio Clock Control Register*
0x0020	HAL_DICE3_SYS_CTL_RESET_SET	*Software Reset Set Register*
0x0024	HAL_DICE3_SYS_CTL_RESET_CLR	*Software Reset Clear Register*
0x0028	HAL_DICE3_SYS_CTL_CHIP_ID	*Chip ID Register*
0x002C	HAL_DICE3_SYS_CTL_BOND_TYPE	*Bond Option Register*
0x0030	HAL_DICE3_SYS_CTL_MUX0	*MUX Control 0 Register*
0x0034	HAL_DICE3_SYS_CTL_MUX1	*MUX Control 1 Register*
0x0038	HAL_DICE3_SYS_CTL_MUX2	*MUX Control 2 Register*
0x003C	HAL_DICE3_SYS_CTL_MUX3	*MUX Control 3 Register*
0x0040	HAL_DICE3_SYS_CTL_INMUX	*Input MUX Control Register*
0x0044	HAL_DICE3_SYS_CTL_AUDIOALT	*Audio Source Input Control Register*
0x0048	HAL_DICE3_SYS_CTL_MPMC_FB	*MPMC Feedback Clock Control Register*
0x0050	HAL_DICE3_SYS_CTL_RST_STAT	*CPU Reset Status Register*
0x0054	HAL_DICE3_SYS_CTL_PUMP_POL	*Pump Polarity Control Register*
0x0058	HAL_DICE3_SYS_CTL_USB_TUNE_SET	*USB Tune Overwrite Register*

3.3 CPU PLL Control Register – HAL_DICE3_SYS_CTL_CPU_PLL

Address: 0xC900_0000 HAL_DICE3_SYS_CTL_CPU_PLL

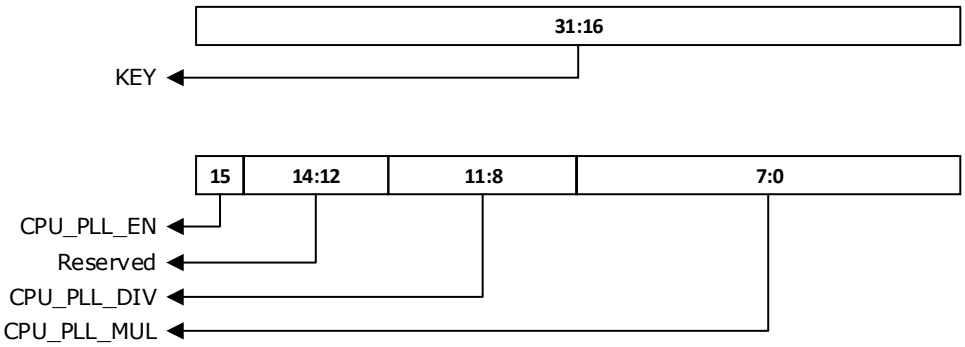

Table 3.3 CPU PLL Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_CPU_PLL register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
PLL_EN	15	0	R/W	0: PLL clock disabled 1: PLL clock enabled
Reserved	14:12	0	N/A	Reserved
PLL_DIV	11:8	0	R/W	Set to achieve the desired frequency
PLL_MUL	7:0	0	R/W	Set to achieve the desired frequency

3.4 System Clock Control Register - HAL_DICE3_SYS_CTL_SYS_CLK

Address: 0xC900_0008 HAL_DICE3_SYS_CTL_SYS_CLK

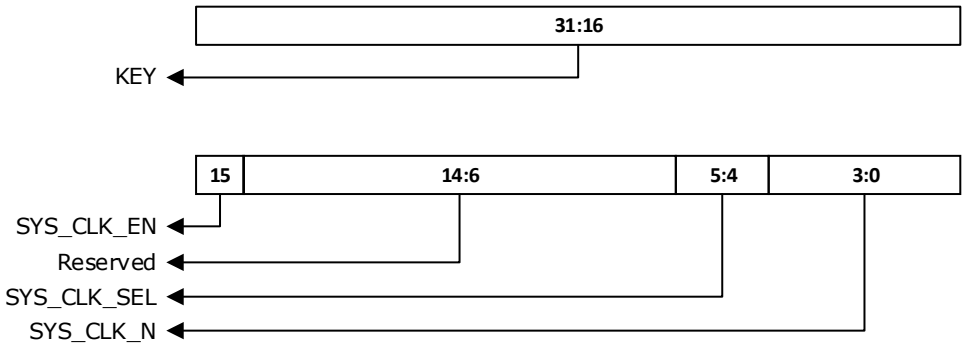

Table 3.4 System Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_SYS_CLK register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
SYS_CLK_EN	15	0	R/W	0: System clock disabled 1: System clock enabled
Reserved	14:6	0	N/A	Reserved
SYS_CLK_SEL	5:4	0	R/W	System clock source select 00: 1394PHY 01: PLLCLKOUT1 10: PLLCLKOUT2 11: Reserved
SYS_CLK_N	3:0	0	R/W	Set to achieve the desired frequency when PLL is selected as a source. Valid values are 0/1/2/4/6/8/10/12/14

3.5 CPU Clock Control Register - HAL_DICE3_SYS_CTL_CPU_CLK

Address: 0xC900_000C HAL_DICE3_SYS_CTL_CPU_CLK

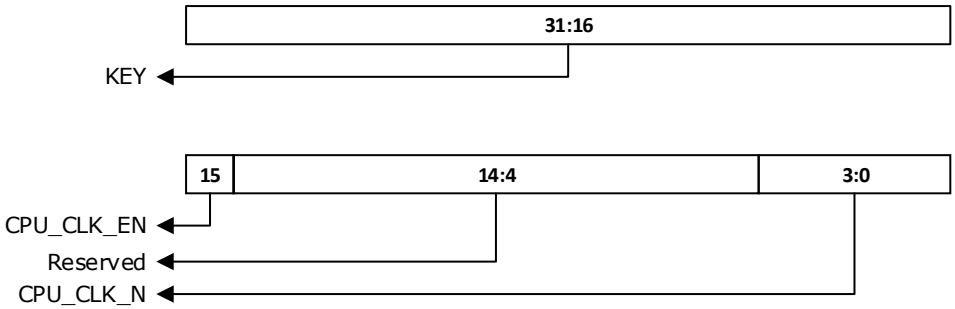

Table 3.5 CPU Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_CPU_CLK register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
CPU_CLK_EN	15	0	R/W	CPU clock source select 0: Oscillator 1: PLL
Reserved	14:4	0	N/A	Reserved
CPU_CLK_N	3:0	0	R/W	Set to achieve the desired frequency when PLL is selected as a source. Valid values are 0/1/2/4/6/8/10/12/14

3.6 SDIO Clock Control Register - HAL_DICE3_SYS_CTL_SDIO_CLK

Address: 0xC900_0010 HAL_DICE3_SYS_CTL_SDIO_CLK

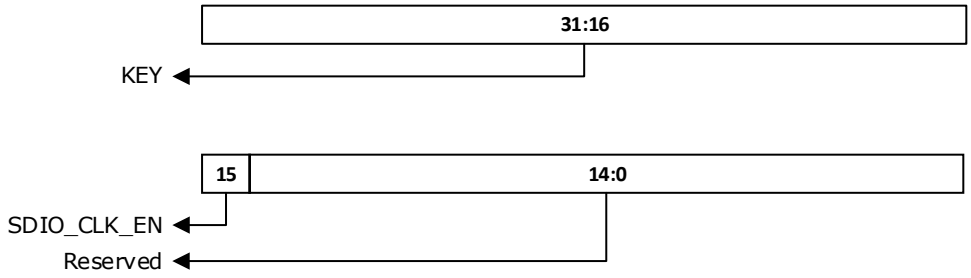

Table 3.6 SDIO Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_SDIO_CLK register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
SDIO_CLK_EN	15	0	R/W	SDIO clock gater 0: SDIO clock gated 1: SDIO clock enabled
Reserved	14:0	0	N/A	Reserved

3.7 ADC Clock Control Register - HAL_DICE3_SYS_CTL_ADC_CLK

Address: 0xC900_0014 HAL_DICE3_SYS_CTL_ADC_CLK

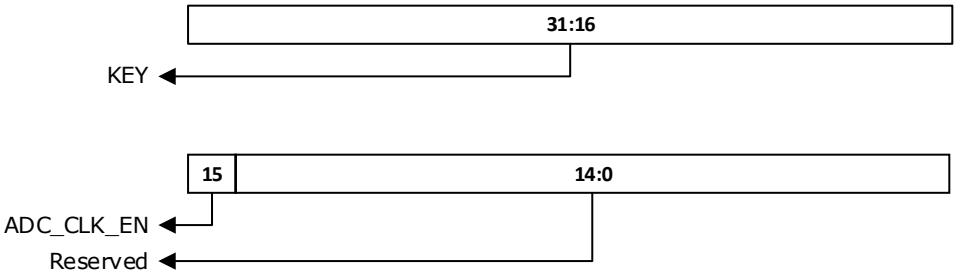

Table 3.7 ADC Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_ADC_CLK register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
ADC_CLK_EN	15	0	R/W	ADC clock gater 0: ADC clock gated 1: ADC clock enabled

Name	Bit	Reset	Dir	Description
Reserved	14:0	0	N/A	Reserved

3.8 Jet PLL™ Clock Control Register - HAL_DICE3_SYS_CTL_JET_CLK

Address: 0xC900_0018 HAL_DICE3_SYS_CTL_JET_CLK

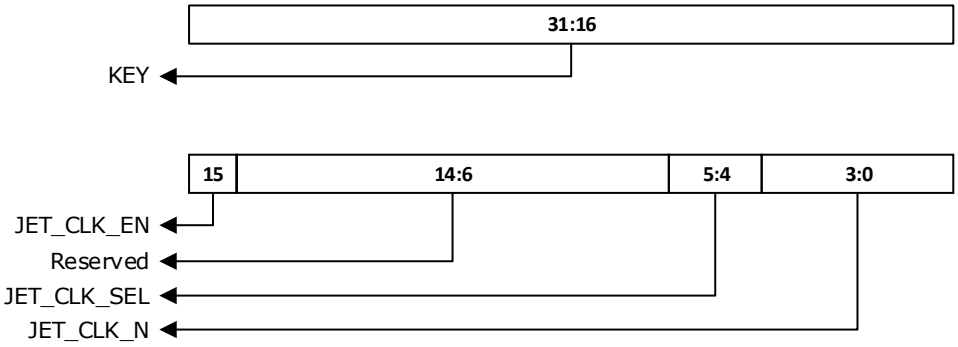

Table 3.8 Jet PLL™ Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_JET_CLK register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
JET_CLK_EN	15	0	R/W	0: clock disabled 1: clock enabled
Reserved	14:6	0	N/A	Reserved
JET_CLK_SEL	5:4	0	R/W	Jet clock source select 0: 1394PCLK 1: PLLCLKOUT1 2: PLLCLKOUT2 3: External Jet
JET_CLK_N	3:0	0	R/W	Set to achieve the desired frequency when PLL is selected as a source. Valid values are 0/1/2/4/6/8/10/12/14

3.9 Audio Clock Control Register - HAL_DICE3_SYS_CTL_AUDIO_CLK

Address: 0xC900_001C HAL_DICE3_SYS_CTL_AUDIO_CLK

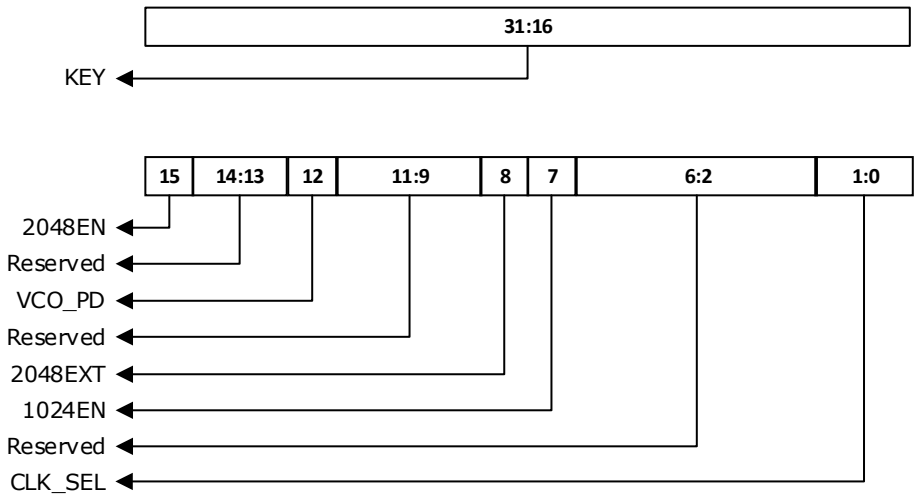

Table 3.9 Audio Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
KEY	31:16	0	R/W	To write to the HAL_DICE3_SYS_CTL_ AUDIO_CLK register, the upper 16 KEY bits must contain 0xabcd. Reads zero.
2048EN	15	0	R/W	0: clock disabled 1: clock enabled
Reserved	14:13	0	N/A	Reserved
VCO_PD	12	0	R/W	Sets Jet PLL™ to sleep if not used to reduce noise. 0: VCO PLL active 1: PLL sleep signal is on (shuts down PLL buffers)
Reserved	11:9	0	N/A	Reserved
2048EXT	8	0	R/W	F2048 Clock source select 0: VCO 1: External
1024EN	7	0	R/W	0: Clock disabled 1: Clock enabled
Reserved	6:2	0	N/A	Reserved
CLK_SEL	1:0	0	R/W	0: VCODiv2 1: External 2: ExternalDiv2 3: Reserved

3.10 Software Reset Set Register - HAL_DICE3_SYS_CTL_RESET_SET

Address: 0xC900_0020 HAL_DICE3_SYS_CTL_RESET_SET

To generate software reset for any of the following blocks, write 1 to the corresponding bit in this register. Writing "0" has no effect on the register content or block operation. To return to normal operation, write "1" to the corresponding bits in the HAL_DICE3_SYS_CTL_RESET_CLR register. Bits return the corresponding current status when read.

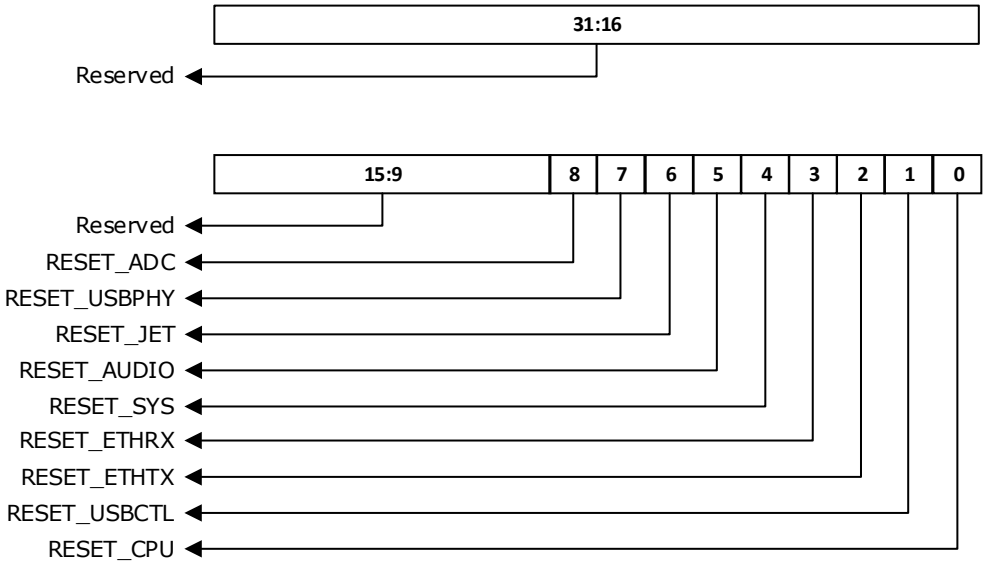

Table 3.10 Software Reset Set Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
Reserved	15:9	0	N/A	Reserved
RESET_ADC	8	1	R/W	ADC block is in reset
RESET_USBPHY	7	1	R/W	Software reset is generated for USB 60MHz domain
RESET_JET	6	1	R/W	Software reset is generated for Jet clock domain
RESET_AUDIO	5	1	R/W	Software reset is generated for Audio clock domain
RESET_SYS	4	1	R/W	Software reset is generated for System clock domain
RESET_ETHRX	3	1	R/W	RGMII is reset by software
RESET_ETHTX	2	1	R/W	Ethernet software reset is generated
RESET_USBCTL	1	1	R/W	Software reset is set for USB 12MHz domain
RESET_CPU	0	0	R/W	Software reset is programmed

3.11 Software Reset Clear Register - HAL_DICE3_SYS_CTL_RESET_CLR

Address: 0xC900_0024 HAL_DICE3_SYS_CTL_RESET_CLR

Bits for each block return the corresponding current status when read.

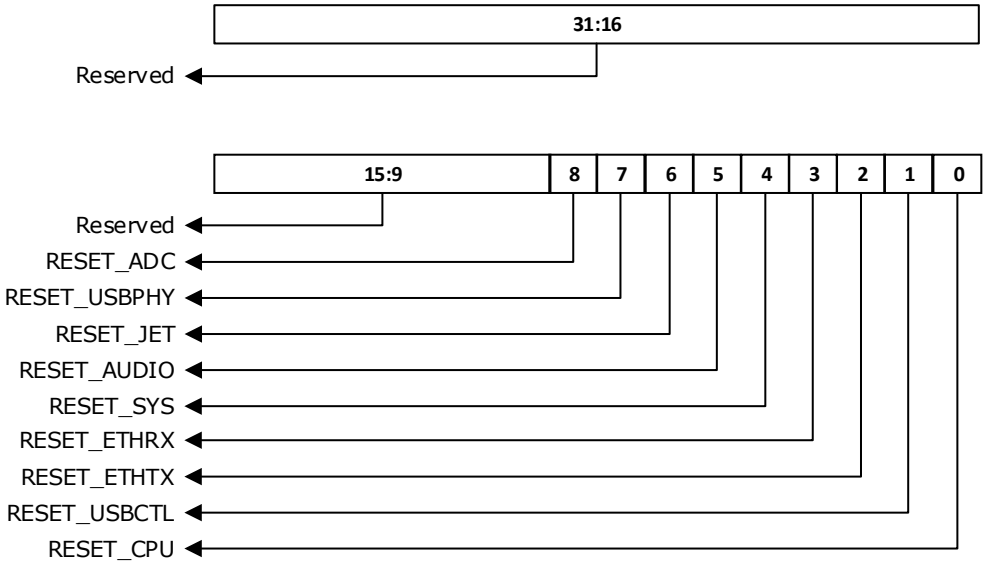

Table 3.11 Software Reset Clear Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:9	0	N/A	Reserved
RESET_ADC	8	1	R/W	ADC block is in reset
RESET_USBPHY	7	1	R/W	Software reset is generated for USB 60MHz domain
RESET_JET	6	1	R/W	Software reset is generated for Jet clock domain
RESET_AUDIO	5	1	R/W	Software reset is generated for Audio clock domain
RESET_SYS	4	1	R/W	Software reset is generated for System clock domain
RESET_ETHRX	3	1	R/W	RGMII is reset by software
RESET_ETHTX	2	1	R/W	Ethernet software reset is generated
RESET_USBCTL	1	1	R/W	Software reset is set for USB 12MHz domain
RESET_CPU	0	0	R/W	Software reset is programmed

3.12 Chip ID Register - HAL_DICE3_SYS_CTL_CHIP_ID

Address: 0xC900_0028 HAL_DICE3_SYS_CTL_CHIP_ID

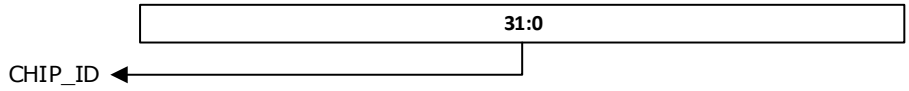

Table 3.12 Chip ID Register bit assignments

Name	Bit	Reset	Dir	Description
CHIP_ID	31:0	0	R	Chip revision

3.13 Bond Option Register - HAL_DICE3_SYS_CTL_BOND_TYPE

Address: 0xC900_002C HAL_DICE3_SYS_CTL_BOND_TYPE

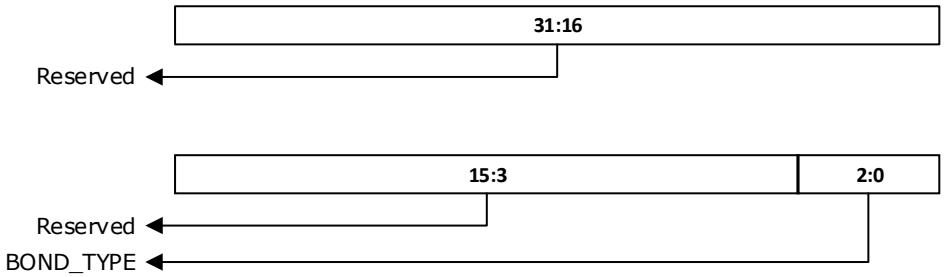

Table 3.13 Bond Option Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	N/A	Reserved
BOND_TYPE	2:0		R	000: TCD3000, DICEIII USB 4x4 001: Reserved 010: TCD3020, DICEIII USB 18x18 011: Reserved 100: TCD3040, DICEIII AVB, USB 18x18 101: Reserved 110: Reserved 111: TCD3070, DICEIII 1394, USB 18x18, AVB

3.14 Mux Control 0 Register - HAL_DICE3_SYS_CTL_MUX0

Address: 0xC900_0030 HAL_DICE3_SYS_CTL_MUX0

The functions of some pins are programmable. The HAL_DICE3_SYS_CTL_MUXn registers are used to configure these multi-function pins.

Table 3.14 Mux Control Port Signal options

Option	Resulting Port Function
0	Either InS in, InS out, or Audio clocks out
1	Always PWM output
2	S/PDIF output, only valid for some ports
3	ADAT0 or ADAT1 output, only valid for some ports
4	GPIO output, all pins are always GPIO inputs
5	UART1 output, only valid for some pins
6	SPI in or out, different function for different pins
7	I^2C in or out, different function for different pins

Table 3.14 is a general reference for assigning functionality for the various multifunction port pins. See the APort MUX Section of the DICEIII TCD30xx_Hardware_Guide for detailed function options for each APort pin.

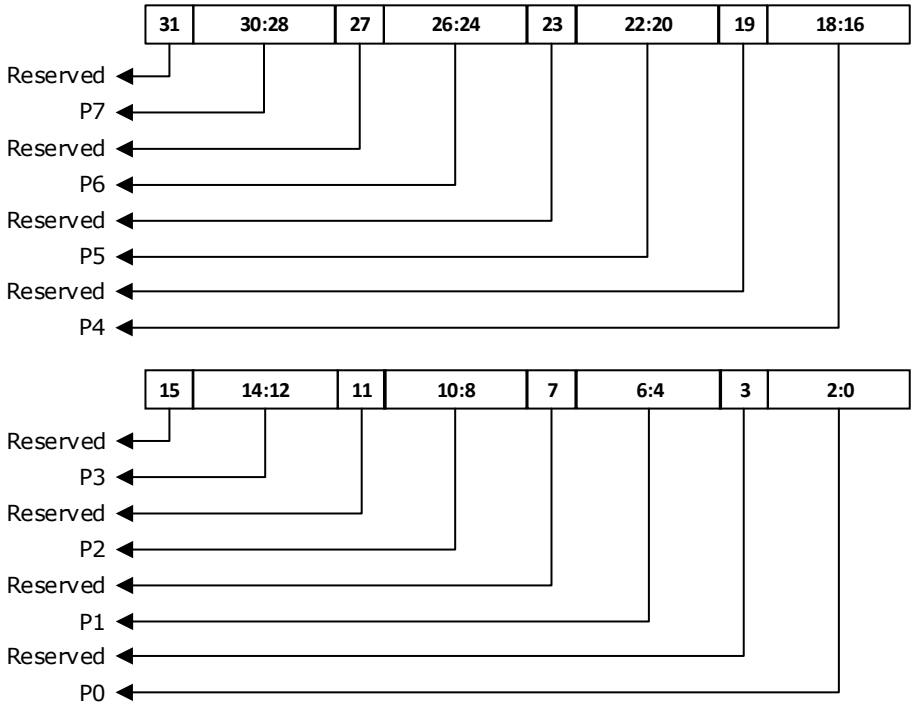

Table 3.15 Mux Control 0 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31	0	N/A	Reserved
P7	30:28	0	R/W	Port 7 pin control
Reserved	27	0	N/A	Reserved
P6	26:24	0	R/W	Port 6 pin control
Reserved	23	0	N/A	Reserved
P5	22:20	0	R/W	Port 5 pin control
Reserved	19	0	N/A	Reserved
P4	18:16	0	R/W	Port 4 pin control
Reserved	15	0	N/A	Reserved
P3	14:12	0	R/W	Port 3 pin control
Reserved	11	0	N/A	Reserved
P2	10:8	0	R/W	Port2 pin control
Reserved	7	0	N/A	Reserved
P1	6:4	0	R/W	Port 1 pin control
Reserved	3	0	N/A	Reserved
P0	2:0	0	R/W	Port 0 pin control

3.15 Mux Control 1 Register - HAL_DICE3_SYS_CTL_MUX1

Address: 0xC900_0034 HAL_DICE3_SYS_CTL_MUX1

The functions of some pins are programmable. The HAL_DICE3_SYS_CTL_MUXn registers are used to configure these multi-function pins. Table 3.14 is a general reference for assigning functionality for the various multifunction port pins. See the APort MUX Section of the DICEIII TCD30xx_Hardware_Guide for detailed function options for each APort pin.

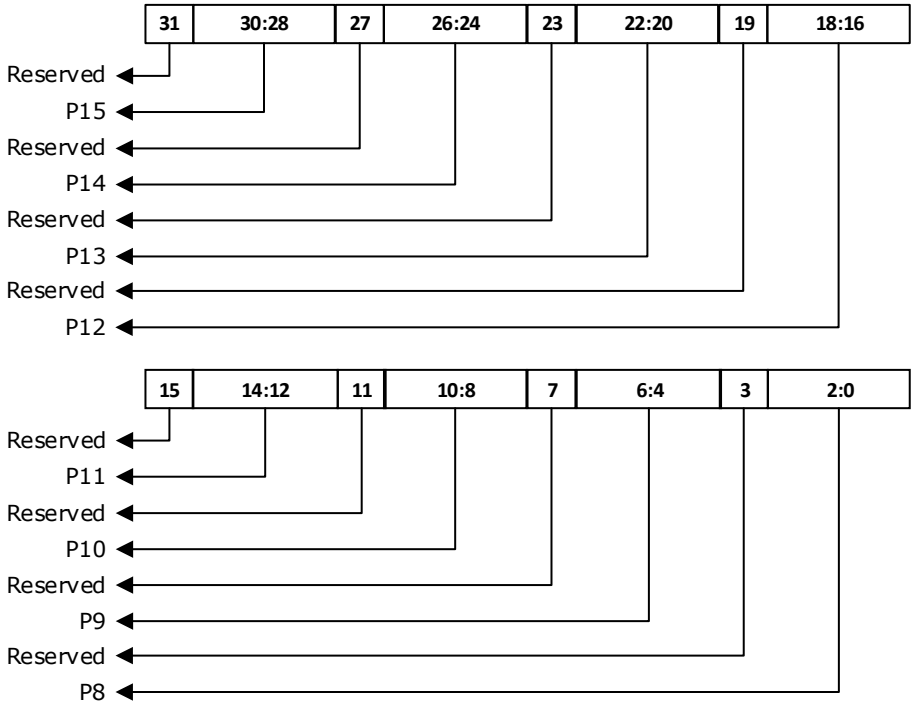

Table 3.16 Mux Control 1 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31	0	N/A	Reserved
P15	30:28	0	R/W	Port 15 pin control
Reserved	27	0	N/A	Reserved
P14	26:24	0	R/W	Port 14 pin control
Reserved	23	0	N/A	Reserved
P13	22:20	0	R/W	Port 13 pin control
Reserved	19	0	N/A	Reserved
P12	18:16	0	R/W	Port 12 pin control
Reserved	15	0	N/A	Reserved
P11	14:12	0	R/W	Port 11 pin control
Reserved	11	0	N/A	Reserved
P10	10:8	0	R/W	Port 10 pin control
Reserved	7	0	N/A	Reserved
P9	6:4	0	R/W	Port 9 pin control
Reserved	3	0	N/A	Reserved
P8	2:0	0	R/W	Port 8 pin control

3.16 Mux Control 2 Register - HAL_DICE3_SYS_CTL_MUX2

Address: 0xC900_0038 HAL_DICE3_SYS_CTL_MUX2

The functions of some pins are programmable. The HAL_DICE3_SYS_CTL_MUXn registers are used to configure these multi-function pins. Table 3.14 is a general reference for assigning functionality for the various multifunction port pins. See the APort MUX Section of the DICEIII TCD30xx_Hardware_Guide for detailed function options for each APort pin.

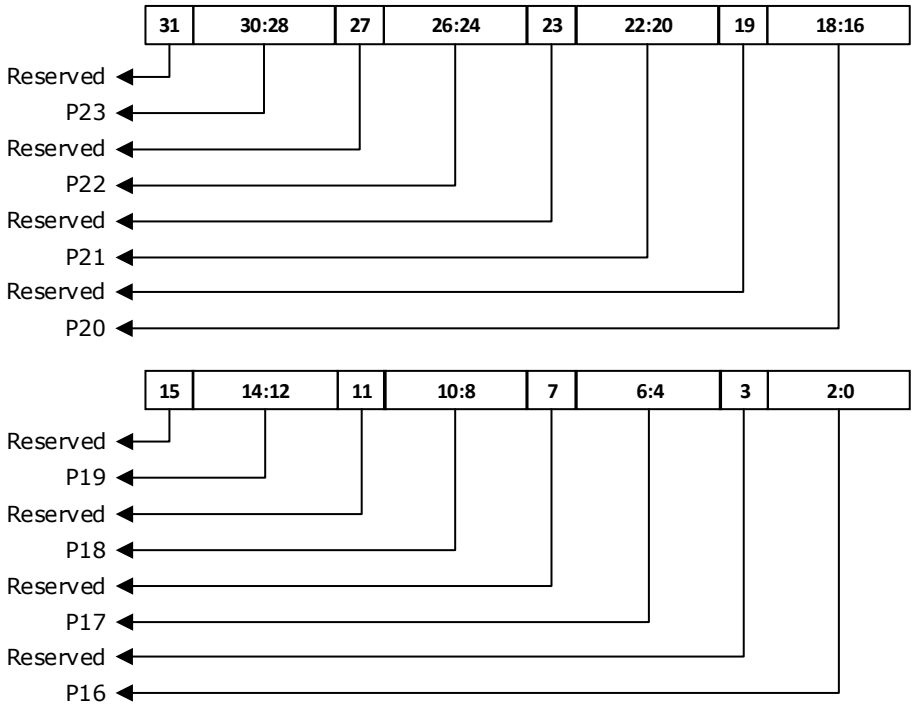

Table 3.17 Mux Control 2 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31	0	N/A	Reserved
P23	30:28	0	R/W	Port 23 pin control
Reserved	27	0	N/A	Reserved
P22	26:24	0	R/W	Port 22 pin control
Reserved	23	0	N/A	Reserved
P21	22:20	0	R/W	Port 21 pin control
Reserved	19	0	N/A	Reserved
P20	18:16	0	R/W	Port 20 pin control
Reserved	15	0	N/A	Reserved
P19	14:12	0	R/W	Port19 pin control
Reserved	11	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
P18	10:8	0	R/W	Port 17 pin control
Reserved	7	0	N/A	Reserved
P17	6:4	0	R/W	Port17 pin control
Reserved	3	0	N/A	Reserved
P16	2:0	0	R/W	Port 16 pin control

3.17 Mux Control 3 Register - HAL_DICE3_SYS_CTL_MUX3

Address: 0xC900_003C HAL_DICE3_SYS_CTL_MUX3

The functions of some pins are programmable. The HAL_DICE3_SYS_CTL_MUXn registers are used to configure these multi-function pins. Table 3.14 is a general reference for assigning functionality for the various multifunction port pins. See the APort MUX Section of the DICEIII TCD30xx_Hardware_Guide for detailed function options for each APort pin.

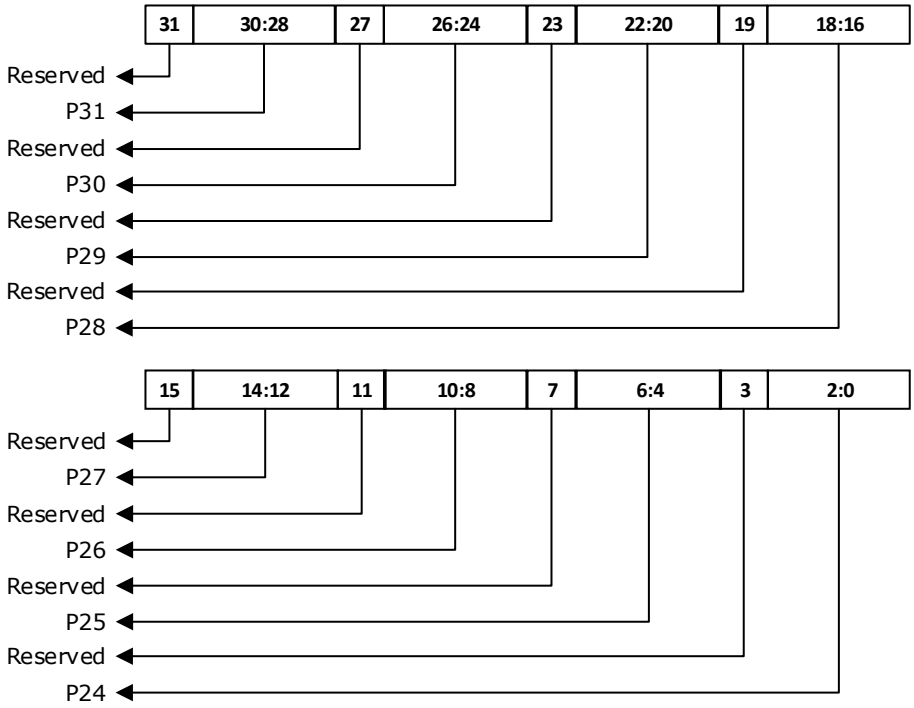

Table 3.18 Mux Control 3 Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31	0	N/A	Reserved
P31	30:28	0	R/W	Port 31 pin control
Reserved	27	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
P30	26:24	0	R/W	Port 30 pin control
Reserved	23	0	N/A	Reserved
P29	22:20	0	R/W	Port 29 pin control
Reserved	19	0	N/A	Reserved
P28	18:16	0	R/W	Port 28 pin control
Reserved	15	0	N/A	Reserved
P27	14:12	0	R/W	Port 27 pin control
Reserved	11	0	N/A	Reserved
P26	10:8	0	R/W	Port 26 pin control
Reserved	7	0	N/A	Reserved
P25	6:4	0	R/W	Port 25 pin control
Reserved	3	0	N/A	Reserved
P24	2:0	0	R/W	Port 24 pin control

3.18 Input Mux Control Register - HAL_DICE3_SYS_CTL_INMUX

Address: 0xC900_0040 HAL_DICE3_SYS_CTL_INMUX

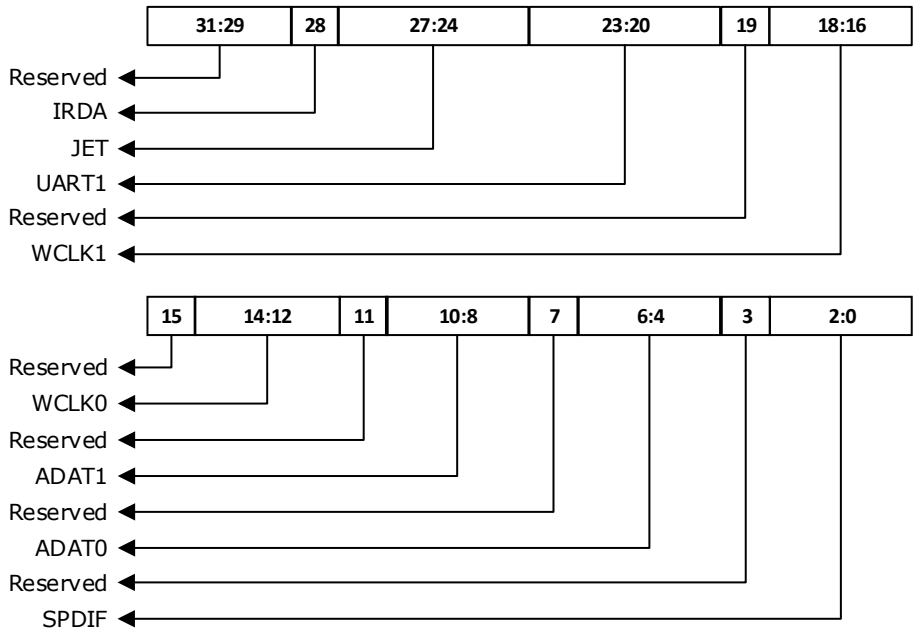

Table 3.19 Input Mux Control Register bit assignments

Name	Bit	Reset	Dir	Description

Name	Bit	Reset	Dir	Description
Reserved	31:29	0	N/A	Reserved
IRDA	28	0	R/W	0: UART1 uses regular signals 1: UART1 uses IRDA signals
JET	27:24	0	R/W	Chose the source of JetExt pins from IO Mux ports
UART1	23:30	0	R/W	The port the signal is taken from is 2* uart1_in_sel +1. This is 1, 3, 5 .. 31
Reserved	19	0	N/A	Reserved
WCLK1	18:16	0	R/W	The port the signal is taken from is 4*wclk1_in_sel+3. This is 3, 7, 11 .. 31.
Reserved	15	0	N/A	Reserved
WCLK0	14:12	0	R/W	The port the signal is taken from is 4*wclk0_in_sel+1. This is 1, 5, 9 .. 29.
Reserved	11	0	N/A	Reserved
ADAT1	10:8	0	R/W	The port the signal is taken from is 4*adat1_in_sel+3. This is 3, 7, 11 .. 31.
Reserved	7	0	N/A	Reserved
ADAT0	6:4	0	R/W	The port the signal is taken from is 4*adat0_in_sel+1. This is 1, 5, 9 .. 29.
Reserved	3	0	N/A	Reserved
SPDIF	2:0	0	R/W	The port the signal is taken from is 2*spdif_in_sel+1. This is 1, 3, 5 .. 31.

3.19 Audio Source Input Control Register - HAL_DICE3_SYS_CTL_AUDIOALT

Address: 0xC900_0044 HAL_DICE3_SYS_CTL_AUDIOALT

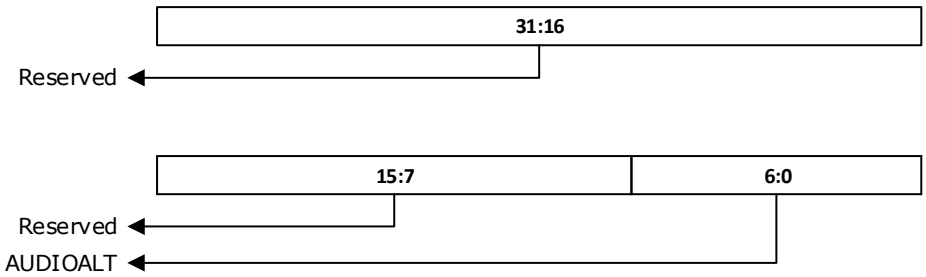

Table 3.20 Audio Source Input Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:7	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
AUDIOALT	6:0	0	R/W	Selects the alternate audio function audio inputs from Port pins. See below.

Table 3.21 Alternate audio function options

Option	Resulting Audio Function
0x00	None
0x01	A0 WCLK
0x02	A16 BCLK1
0x04	A17 MCLK1
0x08	A18 FCLK1
0x10	A24 MCLK2
0x20	A30 WCLK
0x40	A31 CLK2

3.20 MPMC Feedback Clock Control Register - HAL_DICE3_SYS_CTL_MPMC_FB

Address: 0xC900_0048 HAL_DICE3_SYS_CTL_MPMC_FB

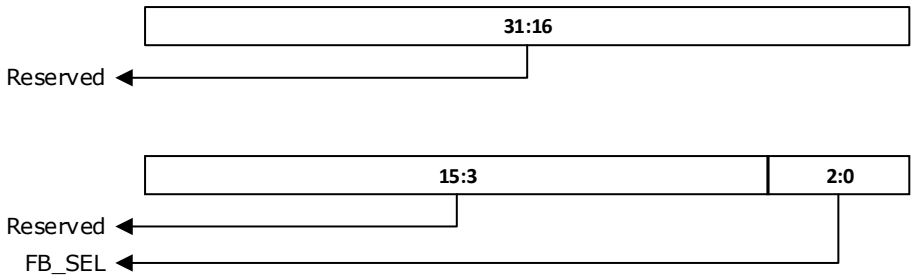

Table 3.22 MPMC Feedback Clock Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	N/A	Reserved
FB_SEL	2:0	0	R/W	Selects source MPMC clock signals 00: clock is fed by EBI input 01: clock is fed by inverted EBI input 10: clock is fed by EBI output 11: clock is fed by inverted EBI output

3.21 CPU Reset Status Register - HAL_DICE3_SYS_CTL_RST_STAT

Address: 0xC900_0050 HAL_DICE3_SYS_CTL_RST_STAT

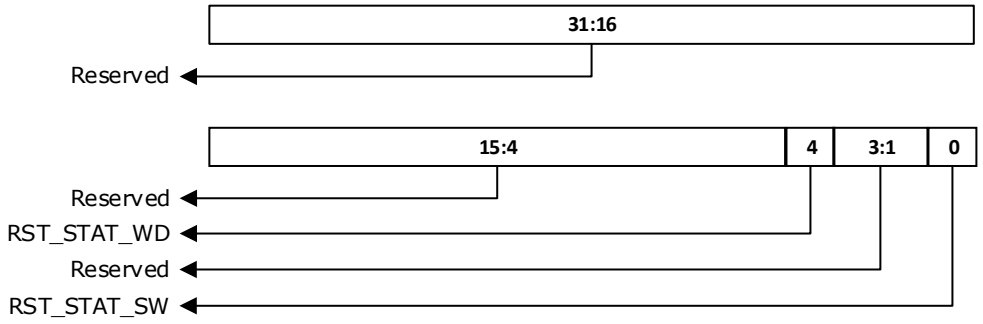

Table 3.23 CPU Reset Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:5	0	N/A	Reserved
RST_STAT_WD	4	0	R/W	System reset was caused by the WatchDog
Reserved	3:1	0	N/A	Reserved
RST_STAT_SW	0	0	R/W	System reset was caused by a CPU software reset

Both bits are reset by PowerOn reset or cleared by software writing "1" to a specific bit. Software should not clear these bits right after set, otherwise the incorrect status will be reflected after reset occurred.

3.22 Pump Polarity Control Register - HAL_DICE3_SYS_CTL_PUMP_POL

Address: 0xC900_0054 HAL_DICE3_SYS_CTL_PUMP_POL

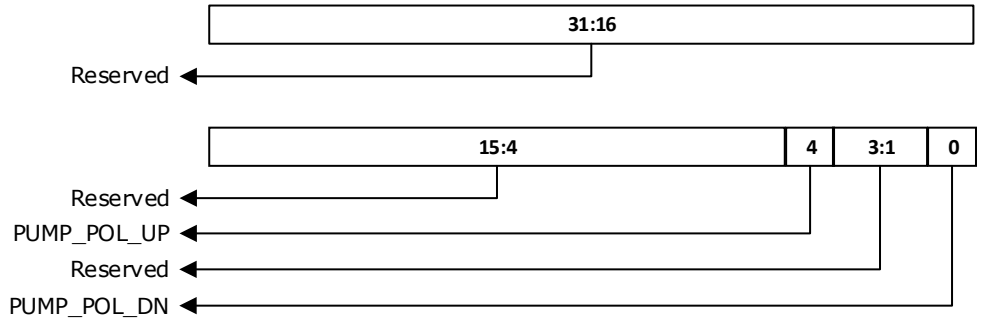

Table 3.24 Pump Polarity Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:5	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
PUMP_POL_UP	4	0	R/W	0: Pump Up signal is active high at VCO PLL input 1: Pump Up signal is active low at VCO PLL input
Reserved	3:1	0	N/A	Reserved
PUMP_POL_DN	0	0	R/W	0: n_pump_down is active low at the VCO PLL input 1: n_pump_down is active high at VCO PLL input

3.23 USB Tune Overwrite Register - HAL_DICE3_SYS_CTL_USB_TUNE_SET

Address: 0xC900_0058 HAL_DICE3_SYS_CTL_USB_TUNE_SET

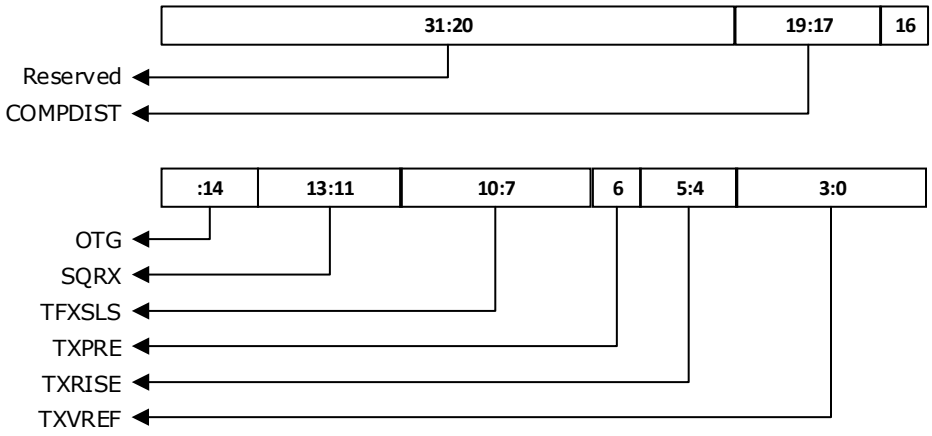

Table 3.25 USB Tune Overwrite Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:20	0	N/A	Reserved
COMPDIST	19:17	3	R/W	See below.
OTG	16:14	3	R/W	"
SQRX	13:11	3	R/W	"
TXFSLS	10:7	4	R/W	"
TXPRE	6	1	R/W	"
TXRISE	5:4	2	R/W	"
TXVREF	3:0	4	R/W	"

Default values after reset are the same as defaults defined in the USB PHY documentation. If software will change these values, it should be done while the USB PHY is held in Reset by

using the corresponding bit in the *HAL_DICE3_SYS_CTL_RESET_SET* register. The USB PHY should be brought out of reset for the values to take effect. These registers are for testing purposes and should be left at reset value.

3.24 Revisions

Table 3.26 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication