PWM

Pule-Width Modulator Module

Revision 0.9.0-41360

May 6, 2015

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29 PWM

29.1 Overview

The Pulse-Width Modulator module supports up to 8 balanced PWM amplifiers for direct connection to a FET H-bridge. They can also be used as 16 normal PWM generators for LED's etc.

29.2 Module Configuration

Table 29.1 PWM base address

Base address	Description
0xC7000000	PWM Module

Table 29.2 PWM register summary

Address Offset	Register	Description
0x0000	HAL_DICE3_PWM_CTL	*PWM Control Register*
0x0004	HAL_DICE3_PWM_STAT	*PWM Status Register*
0x0008	HAL_DICE3_PWM _IE	*PWM Interupt Enable Register*
0x000C	HAL_DICE3_PWM_DREG	*PWM Data Register*

29.2.1 PWM Control Register – HAL_DICE3_PWM_CTL

Address offset: 0x0000 HAL_DICE3_PWM_CTL

This register is used to configure the PWM module.

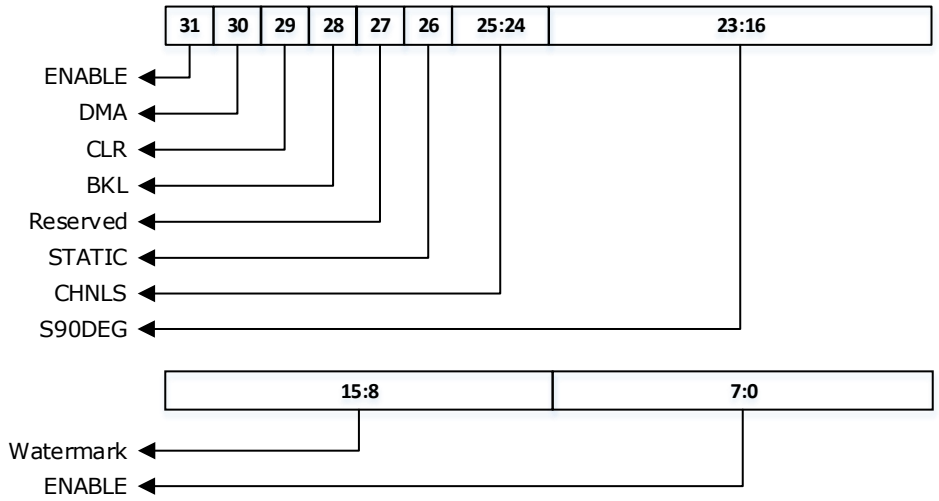


Table 29.3 PWM Control Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	RW	Set to enable the PWM engine
DMA	30	0	RW	Set to enable DMA operation
CLR	29	0	RW	Write1 to clear the FIFO
BLK	28	0	RW	Write 1 to make next data write the first word (automatically set by DMA)
Reserved	27	0	N/A	Reserved, read undefined
STATIC	26	0	RW	If set repeat last word at underrun condition (classic PWM)
CHNLS	25:24	0	RW	00 = 2 channels (1 DWORD) 01 = 4 channels (2 DWORDS) 10 = 8 channels (4 DWORDS)
S90DEG	23:16	0	RW	For each S90DEG bit that is set, the pulses for the corresponding channel are delayed by 128 pulse counts
WATERMARK	15:8	0	RW	The FIFO level which will set the BELOW bit in the Status and Interrupt registers (see below). The bits are set when the FIFO level less than WATERMARK
CH_EN	7:0	0	RW	For each CH_EN bit that is set, the pulses for the corresponding PWM channel is enabled

29.2.2 PWM Status Register – HAL_DICE3_PWM_STAT

Address offset: 0x0004 HAL_DICE3_PWM_STAT

This register is used to monitor the status of the PWM module.

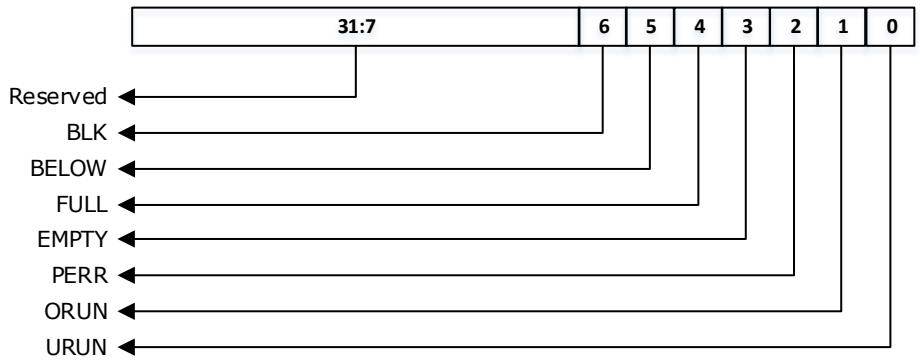


Table 29.4 PWM Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:7	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
BLK	6	0	RW	Set if the next word will be the first of a block, clear when write data
BELOW	5	0	RW	Set if FIFO has less than watermark words in it
FULL	4	0	RW	Set if FIFO is full
EMPTY	3	0	RW	Set if FIFO is empty
PERR	2	0	RW	Sticky phase error flag, write 1 to clear
ORUN	1	0	RW	Sticky overrun flag, write 1 to clear
URUN	0	0	RW	Sticky underrun flag, write 1 to clear

29.2.3 PWM Interrupt Enable Register – HAL_DICE3_PWM_IE

Address offset: 0x0008 HAL_DICE3_PWM_IE

This register is used to enable PWM interrupts.

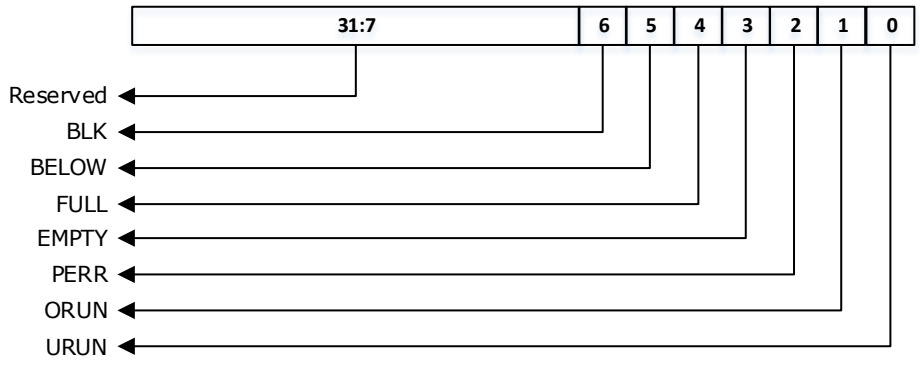


Table 29.5 PWM Interrupt Enable Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:7	0	N/A	Reserved
BLK	6	0	RW	Set to receive an interrupt if the next word will be the first of a block, clear when write data
BELOW	5	0	RW	Set to receive an interrupt if FIFO has less than watermark words in it
FULL	4	0	RW	Set to receive an interrupt if FIFO is full
EMPTY	3	0	RW	Set to receive an interrupt if FIFO is empty
PERR	2	0	RW	Set to receive an interrupt when a phase error occurs
ORUN	1	0	RW	Set to receive an interrupt when an overrun occurs
URUN	0	0	RW	Set to receive an interrupt when an underrun occurs

29.2.4 PWM Data Register – HAL_DICE3_PWM_DREG

Address offset: 0x000C HAL_DICE3_PWM_DREG

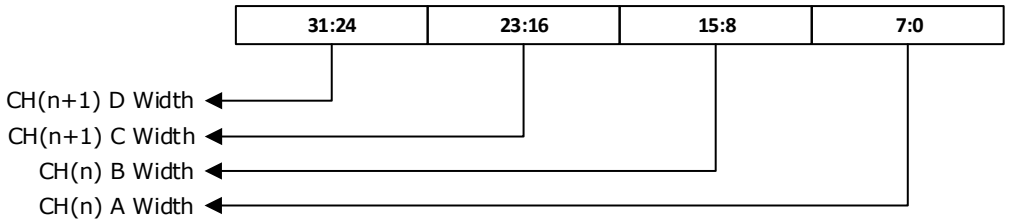
This register is used to write data to the PWM FIFO.

If the Status register BLK flag is set, n=0.

If CHNLS=0 (2 channel mode) n always=0

If CHNLS=1 (4 channel mode) if BLK flag is set n=0, else n=(n+2)%4

If CHNLS=2 (8 channel mode) if BLK flag is set n=0, else n=(n+2)%8



29.3 Revisions

Table 29.6 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication