GPIO

General Purpose I/O

Revision 0.9.0-41360

May 6, 2015

List of Tables

List of Figures

9 GPIO

9.1 Overview

The General Purpose I/O (GPIO) consists of two GPIO module instances with a data width of 8 bits each for a total maximum number of 16 GPIO ports, with the exception of the TCD3000 having a maximum of 8 GPIO ports.

- Each port is configurable as input or output
- Each port is configurable for level or edge sensitive interrupts
- Configurable deglitching logic for each port

The default direction of the GPIO is input.

9.2 Signal Description

Each GPIO is mirrored from 0-15 up to 16-31 in the aport mux. Many pins are shared/multi-purpose. When using the TCD3020 and higher, some GPIO signals can be configured for more than one pin. *Table 9.1* shows the pins that may correspond to the GPIOs for each chip variant.

If two pins are configured for the same GPIO output, then the corresponding GPIO signal being set will be reflected on both output pins. If more than one pin is configured as an input to the same GPIO, then the input signal will only be reflected only the GPIO that corresponds to the lowest aport number.

Support firmware provides macros which implement GPIO port configuration transparently.

Table 9.1 GPIO Signal Description

Signal	aport	TCD3000	TCD3020 TCD3040	TCD3070	Drive (mA)	Description
GPIO0	0	34	A26	R9	8	General Purpose I/O (5V)
GPIO1	1	35	B28	N9	8	General Purpose I/O (5V)
GPIO2	2	40	B34	N11	8	General Purpose I/O (5V)
GPIO3	3	42	B35	R13	8	General Purpose I/O (5V)
GPIO4	4	45	A37	N14	8	General Purpose I/O (5V)
GPIO5	5	46	B40	P15	8	General Purpose I/O (5V)
GPIO6	6	50	B44	M15	8	General Purpose I/O (5V)
GPIO7	7	51	A42	L15	8	General Purpose I/O (5V)
GPIO8	8	-	A24	R8	8	General Purpose I/O (5V)
GPIO9	9	-	B26	N8	8	General Purpose I/O (5V)
GPIO10	10	-	B29	R10	8	General Purpose I/O (5V)
GPIO11	11	-	B30	R11	8	General Purpose I/O (5V)
GPIO12	12	-	B31	N10	8	General Purpose I/O (5V)
GPIO13	13	-	A34	R14	8	General Purpose I/O (5V)
GPIO14	14	-	B36	R15	8	General Purpose I/O (5V)
GPIO15	15	-	B32	M14	8	General Purpose I/O (5V)
GPIO0	16	-	A40	L13	8	General Purpose I/O (5V)
GPIO1	17	-	B47	K15	8	General Purpose I/O (5V)
GPIO2	18	-	B46	K13	8	General Purpose I/O (5V)
GPIO3	19	-	-	K14	8	General Purpose I/O (5V)
GPIO4	20	-	-	P8	8	General Purpose I/O (5V)
GPIO5	21	-	-	P9	8	General Purpose I/O (5V)
GPIO6	22	-	-	P10	8	General Purpose I/O (5V)
GPIO7	23	-	-	R12	8	General Purpose I/O (5V)
GPIO8	24	-	-	P11	8	General Purpose I/O (5V)
GPIO9	25	-	-	P12	8	General Purpose I/O (5V)
GPIO10	26	-	-	P13	8	General Purpose I/O (5V)
GPIO11	27	-	-	N12	8	General Purpose I/O (5V)
GPIO12	28	-	-	P14	8	General Purpose I/O (5V)
GPIO13	29	-	-	M13	8	General Purpose I/O (5V)
GPIO14	30	-	-	N15	8	General Purpose I/O (5V)
GPIO15	31	-	-	L14	8	General Purpose I/O (5V)

9.3 Module Configuration

Table 9.2 GPIO base addresses

Base address	GPIO module number
0xCA000000	0
0xCB000000	1

Table 9.3 GPIO register summary

Address Offset	Register	Description
0x0000 – 0x3FC	HAL_DICE3_GPIO_DATA	*GPIO Data Register*
0x0400	HAL_DICE3_GPIO_DIR	*GPIO Data Direction Register*
0x0404	HAL_DICE3_GPIO_IS	*GPIO Interrupt Sense Register*
0x0408	HAL_DICE3_GPIO_IBE	*GPIO Interrupt Both Edges Register*
0x040C	HAL_DICE3_GPIO_IEV	*GPIOInterrupt Event Register*
0x0410	HAL_DICE3_GPIO_IE	*GPIO Interrupt Mask Register*
0x0414	HAL_DICE3_GPIO_RIS	*GPIO Raw Interrupt Status Register*
0x0418	HAL_DICE3_GPIO_MIS	*GPIO Masked Interrupt Status Register*
0x041C	HAL_DICE3_GPIO_IC	*GPIO Interrupt Clear Register*
0x0420	HAL_DICE3_GPIO_AFSEL	*GPIO Mode Control Select Register*

9.3.1 GPIO Data Register – HAL_DICE3_GPIO_DATA

Address offset: 0x0000 - 0x03FC HAL_DICE3_GPIO_DATA

The same data register appears at 256 locations in the memory map. This allows you to use the address bus [9:2] as an additional bit masking feature. **See *Data Register access* for details.**

The HAL_DICE3_GPIO_DATA register is the data register. In software control mode, values written in the HAL_DICE3_GPIO_DATA register are transferred onto the GPOUT pins if the respective pins have been configured as outputs through the HAL_DICE3_GPIO_DIR register.

In order to write to HAL_DICE3_GPIO_DATA, the corresponding bits in the mask, resulting from the address bus, PADDR[9:2], must be HIGH. Otherwise the bit values remain unchanged by the write.

Similarly, the values read from this register are determined for each bit, by the mask bit derived from the address used to access the data register, PADDR[9:2]. Bits that are 1 in the address mask cause the corresponding bits in HAL_DICE3_GPIO_DATA to be read,

and bits that are 0 in the address mask cause the corresponding bits in HAL_DICE3_GPIO_DATA to be read as 0, regardless of their value.

A read from HAL_DICE3_GPIO_DATA returns the last bit value written if the respective pins are configured as output, or it returns the value on the corresponding input GPIN bit when these are configured as inputs. All bits are cleared by a reset.

Table 9.4 GPIO Data Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Data	7:0	0	R W	Input Data Output Data

9.3.2 GPIO Data Direction Register – HAL_DICE3_GPIO_DIR

Address offset: 0x0400 HAL_DICE3_GPIO_DIR

The HAL_DICE3_GPIO_DIR register is the data direction register. Bits set to HIGH in the HAL_DICE3_GPIO_DIR configure corresponding pin to be an output. Clearing a bit configures the pin to be input. All bits are cleared by a reset. Therefore, the GPIO pins are input by default.

Table 9.5 GPIO Data Direction Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
DataDir	7:0	0	RW	Bits set: pins output Bits cleared: pins input

9.3.3 GPIO Interrupt Sense Register – HAL_DICE3_GPIO_IS

Address offset: 0x0404 HAL_DICE3_GPIO_IS

The HAL_DICE3_GPIO_IS register is the interrupt sense register. Bits set to HIGH in HAL_DICE3_GPIO_IS configure the corresponding pins to detect levels. Clearing a bit configures the pin to detect edges. All bits are cleared by a reset.

Table 9.6 GPIO Interrupt Sense Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Interrupt Sense	7:0	0	RW	Bits clear: edge on corresponding pin is detected Bits set: level on corresponding pin is detected

9.3.4 GPIO Interrupt Both Edges Register – HAL_DICE3_GPIO_IBE

Address offset: 0x0408 HAL_DICE3_GPIO_IBE

The HAL_DICE3_GPIO_IBE register is the interrupt both-edges register. When the corresponding bit in HAL_DICE3_GPIO_IS is set to detect edges, bits set to HIGH in HAL_DICE3_GPIO_IBE configure the corresponding pin to detect both rising and falling edges, regardless of the corresponding bit in the HAL_DICE3_GPIO_IEV (interrupt event register). Clearing a bit configures the pin to be controlled by HAL_DICE3_GPIO_IEV. All bits are cleared by a reset.

Table 9.7 GPIO Interrupt Both Edges Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Interrupt BothEdges	7:0	0	RW	Bits set: both edges on corresponding pin trigger an interrupt. Bits cleared, interrupt generation event is controlled by HAL_DICE3_GPIO_IEV. Single edge: determined by corresponding bit in HAL_DICE3_GPIO_IEV register

9.3.5 GPIO Interrupt Event Register – HAL_DICE3_GPIO_IEV

Address offset: 0x040C HAL_DICE3_GPIO_IEV

The HAL_DICE3_GPIO_IEV register is the interrupt event register. Bits set to HIGH in HAL_DICE3_GPIO_IEV configure the corresponding pin to detect rising edges or high levels, depending on the corresponding bit value in HAL_DICE3_GPIO_IS. Clearing a bit configures the pin to detect falling edges or low levels, depending on the corresponding bit value in HAL_DICE3_GPIO_IS. All bits are cleared by a reset.

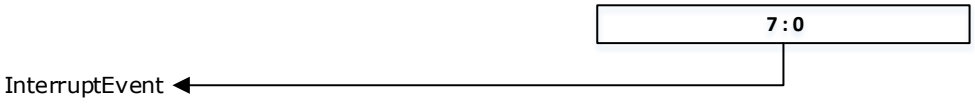

Table 9.8 GPIO Interrupt Event Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Interrupt Event	7:0	0	RW	Bits set: rising edges, or high levels on corresponding pins trigger interrupts. Bits cleared: falling edges, or low levels on corresponding pin trigger interrupts

9.3.6 GPIO Interrupt Mask Register – HAL_DICE3_GPIO_IE

Address offset: 0x0410 HAL_DICE3_GPIO_IE

The HAL_DICE3_GPIO_IE register is the interrupt mask register. Bits set to HIGH in HAL_DICE3_GPIO_IE allow the corresponding pins to trigger their individual interrupts and the combined GPIOINTR line. Clearing a bit disables interrupt triggering on that pin. All bits are cleared by a reset.

Table 9.9 GPIO Interrupt Mask Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Interrupt Mask	7:0	0	RW	Bits set: corresponding pin is not masked. Bits cleared:, corresponding pin interrupt is masked.

9.3.7 GPIO Raw Interrupt Status Register – HAL_DICE3_GPIO_RIS

Address offset: 0x0414 HAL_DICE3_GPIO_RIS

The HAL_DICE3_GPIO_RIS register is the raw interrupt status register. Bits read HIGH in HAL_DICE3_GPIO_RIS reflect the status of interrupts trigger conditions detected (raw, prior to masking), indicating that all the requirements have been met, before they are finally allowed to trigger by HAL_DICE3_GPIO_IE. Bits read as zero indicate that corresponding input pins have not initiated an interrupt. This register is read only, and bits are cleared by a reset.

Table 9.10 GPIO Raw Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Raw Interrupt Status	7:0	0	R	Reflect the status of interrupts trigger conditions detection on pins (raw, prior to masking). Bits set: requirements met by corresponding pins. Bits clear: requirements not met.

9.3.8 GPIO Masked Interrupt Status Register – HAL_DICE3_GPIO_MIS

Address offset: 0x0418 HAL_DICE3_GPIO_MIS

The HAL_DICE3_GPIO_MIS register is the masked interrupt status register. Bits read HIGH in HAL_DICE3_GPIO_MIS reflect the status of input lines triggering an interrupt. Bits read as LOW indicate that either no interrupt has been generated, or the interrupt is

masked. HAL_DICE3_GPIO_MIS is the state of the interrupt after masking. This register is read-only, and all bits are cleared by a reset.

Table 9.11 GPIO Masked Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Masked Interrupt Status	7:0	0	R	Masked value of interrupt due to corresponding pin. Bits clear: GPIO line interrupt not active. Bits set: GPIO line asserting interrupt.

9.3.9 GPIO Interrupt Clear Register – HAL_DICE3_GPIO_IC

Address offset: 0x041C HAL_DICE3_GPIO_IC

The HAL_DICE3_GPIO_IC register is the interrupt clear register. Writing a 1 to a bit in this register clears the corresponding interrupt edge detection logic register. Writing a 0 has no effect. This register is write-only and all bits are cleared by a reset.

Table 9.12 GPIO Interrupt Clear Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Interrupt Clear	7:0	0	W	Bit written as 1: clears edge detection logic. Bit written as 0: has no effect.

9.3.10 GPIO Mode Control Select Register – HAL_DICE3_GPIO_AFSEL

Address offset: 0x0420 HAL_DICE3_GPIO_AFSEL

The HAL_DICE3_GPIO_AFSEL register is the mode control select register. Writing a 1 to any bit in this register selects the hardware control for the corresponding GPIO line. All bits are cleared by a reset, therefore no GPIO line is set to hardware control by default.

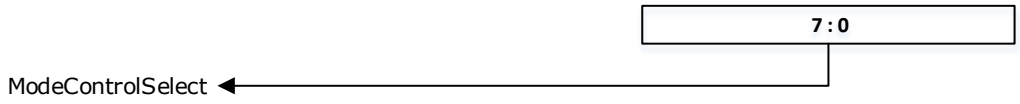

Table 9.13 GPIO Interrupt Clear Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	RW	Reserved, read undefined, must read as zeros.
Mode Control Select	7	0	RW	Bit set: enables hardware control mode. Bit cleared: enables software control mode..

9.4 Data Register access

Each GPIO block comprises eight programmable input/output lines. When the software control mode is enabled, data and control for these lines are provided by a *data register*, HAL_DICE3_GPIO_DATA, and a data direction register. On reads, the data register contains the current status of the GPIO pins, whether they are configured as input or output.

Writing to the data register only affects the pins that are configured as outputs.

So that independent software drivers can set their GPIO bits without affecting any other pins in a single write operation, the address bus is used as a mask on read/write operations.

The following is informative only. Support firmware provides macros which implement this transparently.

The data register effectively covers 256 locations in the address space. The eight address lines used are **PADDR [9: 2]**. During a write, if the address bit associated with that data bit is HIGH, the value of the HAL_DICE3_GPIO_DATA register is altered. If it is LOW, it is left unchanged.

For example:

Writing to address GPIODATA + 0x098 = 0b000010011000

PADDR[9:2] = 0b0000100110. When a value of 0xFB is written to the address 0x098 then:

- bits 5, and 1 of the GPIO pins are set to 1, and bit 2 is set to 0
- the other bits are not changed.

Figure 9.1 shows the above effect of the address value of 0x098 operating on the data value of 0xFB.

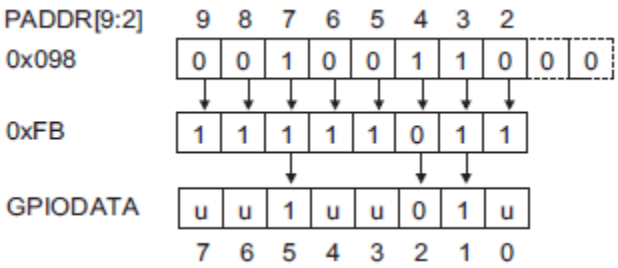

Figure 9.1 Example, write to address 0x098

During a read if an address bit associated with data is HIGH the value is read, if it is LOW it is as zero.

For example:

Read from address GPIODATA + 0x0C4 = 0b000011000100

PADDR[9:2] = 0b0000110001. When reading from 0x0C4 then:

- bits 5, 4, and 0 of the GPIO pins are returned
- the value of bits 7, 6, 3, 2, and 1 are returned as zero, regardless of their state.

Figure 9.2 shows a read from the address 0x0C4 and the output on the **PRDATA[7:0]** lines.

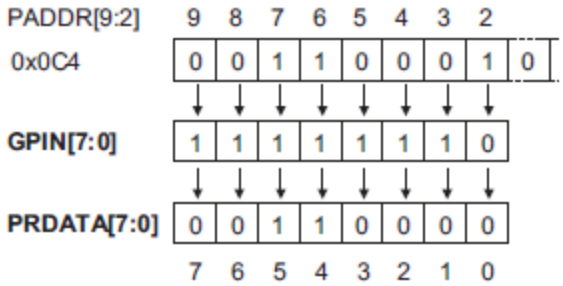

Figure 9.2 Example, read from address 0x0C4

9.5 Revisions

Table 9.14 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication