Interrupt Controller

Revision 0.9.0-41360

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4 Interrupt Controller

4.1 Overview

The interrupt controller provides a software interface to the interrupt system. Two levels of interrupt are available:

- Fast Interrupt Request (FIQ) for fast, low latency interrupt handling
- Interrupt Request (IRQ) for more general interrupts

Only a single FIQ source at a time is generally used in a system, to provide a true low-latency interrupt. This has the following benefits:

- You can execute the interrupt service routine directly without determining the source of the interrupt.
- Interrupt latency is reduced. You can use the banked registers available for FIQ interrupts more efficiently, because a context save is not required.

There are 32 interrupt lines. The interrupt controller uses a bit position for each different interrupt source. The software can control each request line to generate software interrupts.

The nonvectored and daisy-chained IRQ interrupts provide an address for an *Interrupt Service Routine* (ISR). Reading from the vector interrupt address register, ICVectAddr, provides the address of the ISR, and updates the interrupt priority hardware that masks out the current and any lower priority interrupt requests. Writing to the ICVectAddr register indicates to the interrupt priority hardware that the current interrupt is serviced, enabling lower priority interrupts to go active.

The FIQ interrupt has the highest priority, followed by nonvectored IRQ interrupts. Daisy-chained interrupts have the lowest priority. A programmed interrupt request enables you to generate an interrupt under software control. This register is typically used to downgrade an FIQ interrupt to an IRQ interrupt. The interrupt map is shown in *Table 4.2* below.

Note

The priority of the FIQ over IRQ is set by the ARM core. The interrupt controller can raise both an FIQ and an IRQ at the same time.

The IRQ and FIQ request logic has an asynchronous path. This enables interrupts to be asserted when the clock is disabled.

4.2 Programmer's model

The software can control the source interrupt lines to generate software interrupts. These interrupts are generated before interrupt masking, in the same way as external source interrupts. Software interrupts are cleared by writing to the software interrupt clear register, HAL_DICE3_INTCTRL_SWCLR. See *Software Interrupt Clear Register*. This is normally done at the end of the interrupt service routine.

4.2.1 Simple interrupt flow

The following procedure shows how you can use the interrupt controller without using vectored interrupts or the interrupt priority hardware. For example, you can use it for debugging.

1. An interrupt occurs.
2. Branch to IRQ or FIQ exception vector.
3. Branch to the interrupt handler.
4. Interrogate the HAL_DICE3_INTCTRL_IRQSTAT register to determine the source that generated the interrupt, and prioritize the interrupts if there are multiple active interrupt sources. This takes a number of instructions to compute.
5. Branch to the correct ISR.
6. Execute the ISR.
7. Clear the interrupt. If the request was generated by a software interrupt, the HAL_DICE3_INTCTRL_SWCLR register must be written to.
8. Check the HAL_DICE3_INTCTRL_IRQSTAT register to ensure that no other interrupt is active. If there is an active request go to Step 4.
9. Return from the interrupt.

Note

If the above flow is used, you must not read or write to the HAL_DICE3_INTCTRL_VECT register.

Table 4.1 lists the registers in base offset order.

4.3 Module Configuration

Table 4.1 Interrupt Controller register summary

Address	Register	Description
0xF000 0000	HAL_DICE3_INTCTRL_IRQSTAT	*IRQ Status Register*
0xF000 0004	HAL_DICE3_INTCTRL_FIQSTAT	*FIQ Status Register*
0xF000 0008	HAL_DICE3_INTCTRL_RAWSTAT	*Raw Interrupt Status Register*
0xF000 000C	HAL_DICE3_INTCTRL_FIQSEL	*Interrupt Select Register*
0xF000 0010	HAL_DICE3_INTCTRL_ENABLE	*Interrupt Enable Register*
0xF000 0014	HAL_DICE3_INTCTRL_CLEAR	*Interrupt Enable Clear Register*
0xF000 0018	HAL_DICE3_INTCTRL_SWSET	*Software Interrupt Register*
0xF000 001C	HAL_DICE3_INTCTRL_SWCLR	*Software Interrupt Clear Register*
0xF000 0020	HAL_DICE3_INTCTRL_PROT	*Protection Enable Register*
0xF000 0030	HAL_DICE3_INTCTRL_VECT	*Vector Address Register*
0xF000 0034	HAL_DICE3_INTCTRL_DEFVECT	*Default Vector Address Register*

Table 4.2 Interrupt Map

Interrupt number	Description
0	UART 0
1	UART 1
2	COMM RX
3	COMM TX
4	TIMER 1
5	TIMER 2
6	TIMER 11
7	TIMER 12
8	Watchdog
9	Bounced to GPIO0-15
10	DMAC INT C
11	DMAC INT Err
12	ADC
13	I2C
14	USB
15	SDIO
16	SPI 2
17	SPI 1
18	SPI 0
19	-
20	-
21	PWM
22	AUSB Audio
23	AVS Audio
24	LLC
25	AVB Audio
26	Ethernet
27	Jet PLL
28	AIO

4.3.1 IRQ Status Register – HAL_DICE3_INTCTRL_IRQSTAT

Address: 0xF0000000 HAL_DICE3_INTCTRL_IRQSTAT

The HAL_DICE3_INTCTRL_IRQSTAT register is read-only. It provides the status of interrupts [31:0] after IRQ masking. The table below lists the register bit assignments.

Table 4.3 IRQ Status Register bit assignments

Name	Bit	Reset	Dir	Description
IRQStatus	31:0	0	R	Shows the status of the interrupts after masking by the HAL_DICE3_INTCTRL_ENABLE and ICIntSelect registers. A HIGH bit indicates that the interrupt is active, and generates an interrupt to the processor.

4.3.2 FIQ Status Register – HAL_DICE3_INTCTRL_FIQSTAT

Address: 0xF0000004 HAL_DICE3_INTCTRL_FIQSTAT

The HAL_DICE3_INTCTRL_FIQSTAT register is read-only. It provides the status of the interrupts after FIQ masking. The table below lists the register bit assignments.

Table 4.4 FIQ Status Register bit assignments

Name	Bit	Reset	Dir	Description
FIQStatus	31:0	0	R	Shows the status of the interrupts after masking by the HAL_DICE3_INTCTRL_ENABLE and ICIntSelect registers. A HIGH bit indicates that the interrupt is active, and generates an interrupt to the processor.

4.3.3 Raw Interrupt Status Register – HAL_DICE3_INTCTRL_RAWSTAT

Address: 0xF0000008 HAL_DICE3_INTCTRL_RAWSTAT

The HAL_DICE3_INTCTRL_RAWSTAT register is read-only. It provides the status of the source interrupts, and software interrupts, to the interrupt controller. The following table shows the register bit assignments.

Table 4.5 Raw Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
RawInterrupt	31:0	0	R	Shows the status of the interrupts before masking by the enable registers. A HIGH bit indicates that the appropriate interrupt request is active before masking.

4.3.4 Interrupt Select Register– HAL_DICE3_INTCTRL_FIQSEL

Address: 0xF000000C HAL_DICE3_INTCTRL_FIQSEL

The HAL_DICE3_INTCTRL_FIQSEL register is read/write. It selects whether the corresponding interrupt source generates an FIQ or an IRQ interrupt. The following table shows the register bit assignments.

Table 4.6 Interrupt Select Register bit assignments

Name	Bit	Reset	Dir	Description
IntSelect	31:0	0	RW	Selects type of interrupt for interrupt request: 0 = IRQ interrupt 1 = FIQ interrupt

4.3.5 Interrupt Enable Register – HAL_DICE3_INTCTRL_ENABLE

Address: 0xF0000010 HAL_DICE3_INTCTRL_ENABLE

The HAL_DICE3_INTCTRL_ENABLE register is read/write. It enables the interrupt request lines, by masking the interrupt sources for the IRQ interrupt. The following table shows the register bit assignments.

Table 4.7 Interrupt Enable Register bit assignments

Name	Bit	Reset	Dir	Description
IntEnable	31:0	0	RW	Enables the interrupt request lines: 0 = Interrupt disabled. 1 = Interrupt enabled. Enables interrupt request to processor. On reset, all interrupts are disabled. A HIGH bit sets the corresponding bit in the HAL_DICE3_INTCTRL_ENABLE register. A LOW bit has no effect.

4.3.6 Interrupt Enable Clear Register – HAL_DICE3_INTCTRL_CLEAR

Address: 0xF0000014 HAL_DICE3_INTCTRL_CLEAR

The HAL_DICE3_INTCTRL_CLEAR register is write-only. It clears bits in the HAL_DICE3_INTCTRL_ENABLE register. The following table shows the register bit assignments.

Table 4.8 Interrupt Enable Clear Register bit assignments

Name	Bit	Reset	Dir	Description
IntEnable Clear	31:0	0	W	Clears bits in the HAL_DICE3_INTCTRL_ENABLE register. A HIGH bit clears the corresponding bit in the HAL_DICE3_INTCTRL_ENABLE register. A LOW bit has no effect.

4.3.7 Software Interrupt Register – HAL_DICE3_INTCTRL_SWSET

Address: 0xF0000018 HAL_DICE3_INTCTRL_SWSET

The HAL_DICE3_INTCTRL_SWSET register is read/write. It generates software interrupts. The following table shows the register bit assignments.

Table 4.9 Software Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
SoftInt	31:0	0	RW	Setting a bit generates a software interrupt for the specific source interrupt before interrupt masking. A HIGH bit sets the corresponding bit in the HAL_DICE3_INTCTRL_SWSET register. A LOW bit has no effect.

4.3.8 Software Interrupt Clear Register – HAL_DICE3_INTCTRL_SWCLR

Address: 0xF000001C HAL_DICE3_INTCTRL_SWCLR

The HAL_DICE3_INTCTRL_SWCLR register is write-only. It clears bits in the HAL_DICE3_INTCTRL_SWSET register. The following table shows the register bit assignments.

Table 4.10 Software Interrupt Clear Register bit assignments

Name	Bit	Reset	Dir	Description
SoftInt Clear	31:0	0	W	Clears bits in the HAL_DICE3_INTCTRL_SWSET register. A HIGH bit clears the corresponding bit in the HAL_DICE3_INTCTRL_SWSET register. A LOW bit has no effect.

4.3.9 Protection Enable Register – HAL_DICE3_INTCTRL_PROT

Address: 0xF0000020 HAL_DICE3_INTCTRL_PROT

The HAL_DICE3_INTCTRL_PROT register is read/write. It enables or disables protected register access. The following table shows the register bit assignments.

Table 4.11 Protection Enable Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	
Protection	0	0	RW	Enables or disables protected register access. When enabled, only privileged mode accesses, reads and writes, can access the interrupt controller registers. When disabled, both User mode and privileged mode can access the registers. This register is cleared on reset, and can only be accessed in privileged mode.

Note

If the bus master cannot generate accurate protection information, leave this register in its reset state to enable User mode access.

4.3.10 Vector Address Register – HAL_DICE3_INTCTRL_VECT

Address: 0xF0000030 HAL_DICE3_INTCTRL_VECT

The HAL_DICE3_INTCTRL_VECT register is read/write. It contains the *Interrupt Service Routine* (ISR) address of the currently active interrupt. Any writes to this register clear the interrupt. Support software does not require use of this register.

4.3.11 Default Vector Address Register – HAL_DICE3_INTCTRL_DEFVECT

Address: 0xF0000034 HAL_DICE3_INTCTRL_DEFVECT

The HAL_DICE3_INTCTRL_DEFVECT register is read/write. It contains the default ISR address. Support software does not require use of this register.

4.4 Revisions

Table 4.12 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication