I2C

Inter-IC Module

Revision 0.9.0-41360

May 6, 2015

List of Tables

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8.1 I2C Module Interface Diagram

Signal names in **bold** in this chapter refer to labels in this diagram.

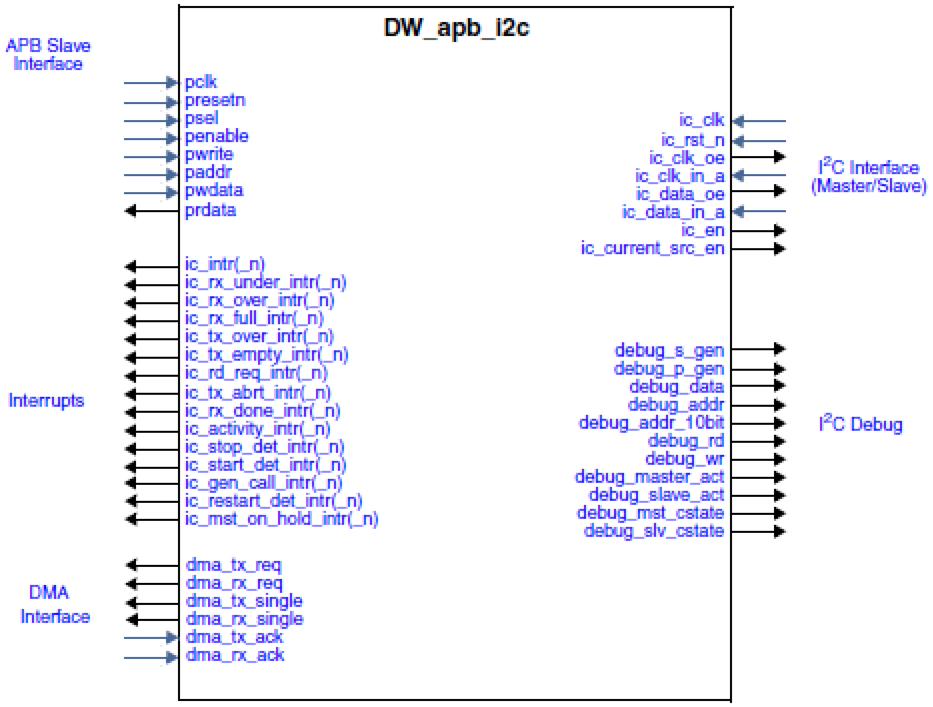

Figure 8.1 I2C Module block diagram

8.2 Module Configuration

Table 8.1 I2C Module register summary

Address	Register	Description
0xCD000000	HAL_DICE3_I2C_CON	I2C Control Register
0xCD000004	HAL_DICE3_I2C_TAR	I2C Target Address Register
0xCD000008	HAL_DICE3_I2C_SAR	I2C Slave Address Register
0xCD000010	HAL_DICE3_I2C_DATA_CMD	I2C Data Buffer and Command Register
0xCD000014	HAL_DICE3_I2C_SS_SCL_HCNT	I2C Standard Speed Clock SCL High Count Register
0xCD000018	HAL_DICE3_I2C_SS_SCL_LCNT	I2C Standard Speed Clock SCL Low Count Register
0xCD00001C	HAL_DICE3_I2C_FS_SCL_HCNT	I2C Fast Mode Clock SCL High Count Register
0xCD000020	HAL_DICE3_I2C_FS_SCL_LCNT	I2C Fast Mode Clock SCL Low Count Register
0xCD00002C	HAL_DICE3_I2C_INTR_STAT	I2C Interrupt Status Register
0xCD000030	HAL_DICE3_I2C_INTR_MASK	I2C Interrupt Mask Register
0xCD000034	HAL_DICE3_I2C_RAW_INTR_STAT	I2C Raw Interrupt Status Register
0xCD000038	HAL_DICE3_I2C_RX_TL	I2C Receive FIFO Threshold Register
0xCD00003C	HAL_DICE3_I2C_TX_TL	I2C Transmit FIFO Threshold Register
0xCD000040	HAL_DICE3_I2C_CLR_INTR	I2C Clear Interrupts Register
0xCD000044	HAL_DICE3_I2C_CLR_RX_UNDER	I2C Clear RX_UNDER Interrupt Register
0xCD000048	HAL_DICE3_I2C_CLR_RX_OVER	I2C Clear RX_OVER Interrupt Register
0xCD00004C	HAL_DICE3_I2C_CLR_TX_OVER	I2C Clear TX_OVER Interrupt Register
0xCD000050	HAL_DICE3_I2C_CLR_RD_REQ	I2C Clear RD_REQ Interrupt Register
0xCD000054	HAL_DICE3_I2C_CLR_TX_ABRT	I2C Clear TX_ABRT Interrupt Register
0xCD000058	HAL_DICE3_I2C_CLR_RX_DONE	I2C Clear RX_DONE Interrupt Register
0xCD00005C	HAL_DICE3_I2C_CLR_ACTIVITY	I2C Clear ACTIVITY Interrupt Register
0xCD000060	HAL_DICE3_I2C_CLR_STOP_DET	I2C Clear STOP_DET Interrupt Register
0xCD000064	HAL_DICE3_I2C_CLR_START_DET	I2C Clear START_DET Interrupt Register
0xCD000068	HAL_DICE3_I2C_CLR_GEN_CALL	I2C Clear GEN_CALL Interrupt Register

Address	Register	Description
0xCD00006C	HAL_DICE3_I2C_ENABLE	*I2C Enable Register*
0xCD000070	HAL_DICE3_I2C_STATUS	*I2C Status Register*
0xCD000074	HAL_DICE3_I2C_TXFLR	*I2C Transmit FIFO Level Register*
0xCD000078	HAL_DICE3_I2C_RXFLR	*I2C Receive FIFO Level Register*
0xCD00007C	HAL_DICE3_I2C_SDA_HOLD	*I2C SDA Hold Time Length Register*
0xCD000080	HAL_DICE3_I2C_TX_ABRT_SOURCE	*I2C Transmit Abort Source Register*
0xCD000084	HAL_DICE3_I2C_SLV_DATA_NACK_ONLY	*I2C Generate SLV_DATA_NACK Register*
0xCD000088	HAL_DICE3_I2C_DMA_CR	*I2C DMA Control Register*
0xCD00008C	HAL_DICE3_I2C_DMA_TDLR	*I2C DMA Transmit Data Level Register*
0xCD000090	HAL_DICE3_I2C_DMA_RDLR	*I2C DMA Receive Data Level Register*
0xCD000094	HAL_DICE3_I2C_SDA_SETUP	*I2C SDA Setup Register*
0xCD000098	HAL_DICE3_I2C_ACK_GENERAL_CALL	*I2C ACK General Call Register*
0xCD00009C	HAL_DICE3_I2C_ENABLE_STATUS	*I2C Enable Status Register*
0xCD0000A0	HAL_DICE3_I2C_FS_SPKLEN	*I2C ISS and FS Spike Suppression Limit Register*
0xCD0000A8	HAL_DICE3_I2C_CLR_RESTART_DET	*I2C Clear RESTART_DET Interrupt Register*
0xCD0000F4	HAL_DICE3_I2C_COMPONENT_PARAM_1	*I2C Component Parameter Register*

8.2.1 Addressing

All registers in the SPI Module are addressed at 32-bit boundaries to remain consistent with the AHB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

8.2.2 Registers

Some registers may be written only when the I2C Module is disabled, programmed by the HAL_DICE3_I2C_ENABLE register. Software should not disable the I2C Module while it is active. If the DW_apb_i2c is in the process of transmitting when it is disabled, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. The slave continues receiving until the remote master aborts the transfer, in which case the I2C Module could be disabled. Registers that cannot be written to when the I2C Module is enabled are indicated in their descriptions.

8.2.3 I2C Control Register – HAL_DICE3_I2C_CON

Address offset: 0xCD000000 HAL_DICE3_I2C_CON

This register can be written only when the I2C Module is disabled, which corresponds to HAL_DICE3_I2C_ENABLE[0] being set to 0. Writes at other times have no effect.

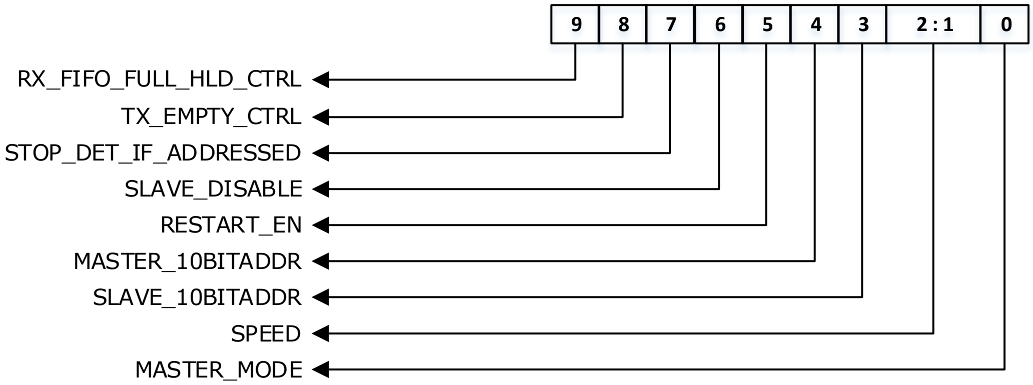

Table 8.2 I2C Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:10	0	N/A	Reserved
RX_FIFO_FULL_HLD_CTRL	9	0	RW	This bit controls whether I2C Module should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the RX_FULL_HLD_BUS_EN parameter.
TX_EMPTY_CTRL	8	0	RW	This bit controls the generation of the TX_EMPTY interrupt, as described in the HAL_DICE3_I2C_RAW_INTR_STAT register.

Name	Bit	Reset	Dir	Description
STOP_DET_IF_ADDRESSED	7	0	RW	In slave mode: **1:** issues the STOP_DET interrupt only when it is addressed. **0:** issues the STOP_DET irrespective of whether it's addressed or not. **Dependencies**: This register bit value is applicable in the slave mode only (MASTER_MODE=1) **Note**: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).
SLAVE_DISABLE	6	1	RW	This bit controls whether I2C has its slave disabled, which means once the **presetn** signal is applied, then this bit takes on the value of 1. If this bit is set (slave is disabled), I2C Module functions only as a master and does not perform any action that requires a slave. **0:** slave is enabled **1:** slave is disabled **Note**: Software should ensure that if this bit is written with '0,' then bit 0 should also be written with a '0'.

Name	Bit	Reset	Dir	Description
RESTART_EN	5	1	RW	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several I2C Module operations. **0:** disable **1:** enable When the RESTART is disabled, the I2C Module master is incapable of performing the following functions: Sending a START BYTE Performing any high-speed mode operation Performing direction changes in combined format mode Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple I2C Module transfers. If the above operations are performed, it will result in setting bit 6 (*TX_ABRT*) of HAL_DICE3_I2C_RAW_INTR_STAT register.
IC_10BITADDR_MASTER	4	1	R	The function of this bit is handled by bit 12 of HAL_DICE3_I2C_TAR register, and becomes a read-only copy. **0:** 7-bit addressing **1:** 10-bit addressing

Name	Bit	Reset	Dir	Description
IC_10BITADDR_SLAVE	3	1	RW	When acting as a slave, this bit controls whether the I2C Module responds to 7- or 10-bit addresses. **0:** 7-bit addressing. The I2C Module ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the SAR register are compared. **1:** 10-bit addressing. The I2C Module responds to only 10-bit addressing transfers that match the full 10 bits of the SAR register.
Note Bits 3 and 4 of this register can be programmed differently and in any combination depending on which format is required for the transfers. For example, master mode can be configured with 10-bit addressing and slave mode can be configured with 7-bit addressing.				
SPEED	2:1	2	RW	These bits control at which speed the I2C Module operates; its setting is relevant only if one is operating the I2C Module in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to 2; otherwise, hardware updates this register with the value of 2. **1:** standard mode (0 to 100 Kb/s) **2:** fast mode (≤ 400 Kb/s) or fast mode plus (≤ 1000 Kb/s)
MASTER_MODE	0	1	RW	This bit controls whether the I2C Module master is enabled. **0:** master disabled **1:** master enabled NOTE: Software should ensure that if this bit is written with '1,' then bit 6 should also be written with a '1'.

Certain combinations of the IC_SLAVE_DISABLE (bit 6) and MASTER_MODE (bit 0) result in a configuration error. Table 6-3 lists the states that result from the combinations of these two bits.

Table 8.3 States for IC_SLAVE_DISABLE (bit 6) and MASTER_MODE (bit 0)

IC_SLAVE_DISABLE (HAL_DICE3_I2C_CON[6])	MASTER_MODE (HAL_DICE3_I2C_CON[0])	State
0	0	Slave Device
0	1	Config Error
1	0	Config Error
1	1	Master Device

Note
Because the I2C Module should only be used either as an I2C master or I2C slave (but not both) at any one time, care should be taken in software that certain combinations of the two bits IC_SLAVE_DISABLE and IC_MASTER_MODE are not programmed into the "HAL_DICE3_I2C_CON" register. In particular, IC_SLAVE_DISABLE and IC_MASTER_MODE must not be set to '0' and '1,' respectively at any given time.

8.2.4 I2C Target Address Register – HAL_DICE3_I2C_TAR

Address offset: 0xCD000004 HAL_DICE3_I2C_TAR

Writes to HAL_DICE3_I2C_TAR succeed when one of the following conditions are true:

- I2C Module is NOT enabled (HAL_DICE3_I2C_ENABLE [0] is set to 0); or
- I2C Module is enabled (HAL_DICE3_I2C_IC_ENABLE[0]=1); AND
- I2C Module is NOT engaged in any Master (tx, rx) operation (HAL_DICE3_I2C_STATUS [5]=0); AND
- I2C Module is enabled to operate in Master mode (HAL_DICE3_I2C_CON[0]=1); AND
- there are NO entries in the Tx FIFO (HAL_DICE3_I2C_STATUS [2]=1).

If the software or application is aware the the I2C Module is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (HAL_DICE3_I2C_STATUS[2]= 0).

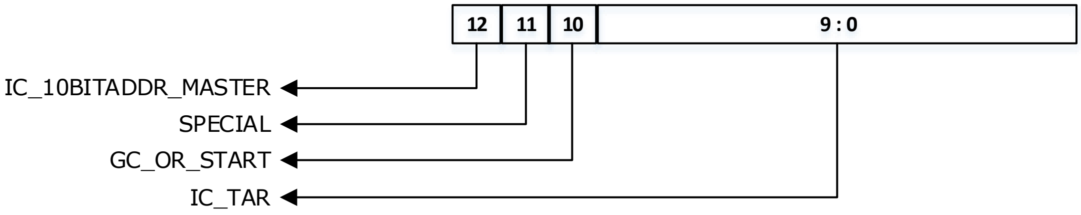

Table 8.4 I2C Target Address Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:13	0	N/A	Reserved
IC_10BITADDR_MASTER	12	0	RW	This bit controls whether the I2C Module starts its transfers in 7-or 10-bit addressing mode when acting as a master. **0:** 7-bit addressing **1:** 10-bit addressing
SPECIAL	11	0	RW	This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally **1:** perform special I2C command as specified in GC_OR_START bit
GC_OR_START	10	0	RW	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C Module. **0:** General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the HAL_DICE3_I2C_INTR_STAT register. The I2C Module remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. **1:** START BYTE
IC_TAR	9:0	0x55	RW	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

Note

It is not necessary to perform any write to this register if I2C Module is enabled as an I2C slave only.

8.2.5 I2C Slave Address Register – HAL_DICE3_I2C_SAR

Address offset: 0xCD000008 HAL_DICE3_I2C_SAR

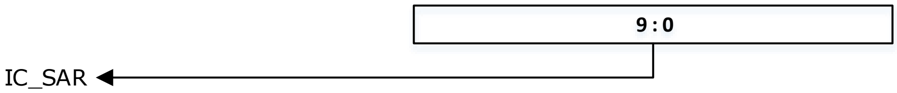

Table 8.5 I2C Slave Address Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:10	0	N/A	Reserved
IC_SAR	9:0	0x55	RW	The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to HAL_DICE3_I2C_ENABLE[0] being set to 0. Writes at other times have no effect. NOTE: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value. Refer to Table bkbk on page 39 for a complete list of these reserved values.

Note

It is not necessary to perform any write to this register if I2C Module is enabled as an I2C master only.

8.2.6 I2C Data Buffer and Command Register – HAL_DICE3_I2C_DATA_CMD

Address offset: 0xCD000010 HAL_DICE3_I2C_DATA_CMD

This is the register the CPU writes to when filling the TX FIFO, and the CPU reads from when retrieving bytes from RX FIFO.

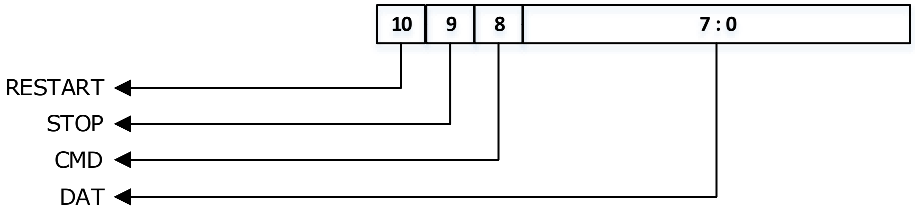

Table 8.6 I2C Data Buffer and Command Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:11	0	N/A	Reserved
RESTART	10	0	W	This bit controls whether a RESTART is issued before the byte is sent or received. **1:** If IC_RESTART_EN (HAL_DICE3_I2C_CON[5]) is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. **0:** If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
STOP	9	0	W	This bit controls whether a STOP is issued after the byte is sent or received. **1:** STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. **0:** STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.

Name	Bit	Reset	Dir	Description
CMD	8	0	W	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C Module acts as a slave. It controls only the direction when it acts as a master. 1 = Read 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a *TX_ABRT* interrupt (HAL_DICE3_I2C_RAW_INTR_STAT[6]), unless bit 11 (*SPECIAL*) in the HAL_DICE3_I2C_TAR register has been cleared. If a "1" is written to this bit after receiving a *RD_REQ* interrupt, then a *TX_ABRT* interrupt occurs.
DAT	7:0	0	RW	This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the I2C Module. However, when you read this register, these bits return the value of data received on the I2C Module interface.

8.2.7 I2C Standard Speed Clock SCL High Count Register – HAL_DICE3_I2C_SS_SCL_HCNT

Address offset: 0xCD000014 HAL_DICE3_I2C_SS_SCL_HCNT

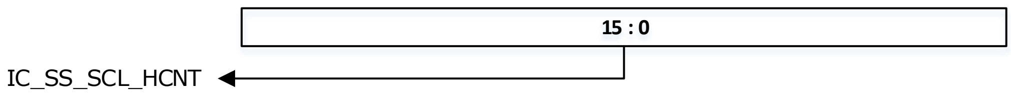

Table 8.7 I2C Standard Speed Clock SCL High Count Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
IC_SS_SCL_HCNT	15:0	0xC8	RW	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to "IC_CLK Frequency Configuration" on page 59 bkbk. This register can be written only when the I2C interface is disabled which corresponds to HAL_DICE3_I2C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. **NOTE:** This register must not be programmed to a value higher than 65525, because I2C Module uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT+10.

8.2.8 I2C Standard Speed Clock SCL Low Count Register – HAL_DICE3_I2C_SS_SCL_LCNT

Address offset: 0xCD000018 HAL_DICE3_I2C_SS_SCL_LCNT

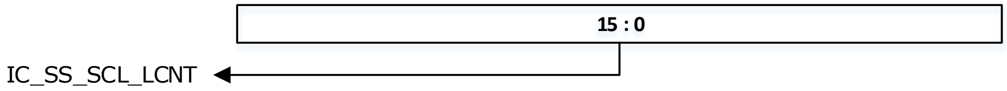

Table 8.8 I2C Standard Speed Clock SCL Low Count Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
IC_SS_SCL_LCNT	15:0	0xEB	RW	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to “IC_CLK Frequency Configuration” on page 59 bkbk. This register can be written only when the I2C interface is disabled which corresponds to HAL_DICE3_I2C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.

8.2.9 I2C Fast Mode Clock SCL High Count Register – HAL_DICE3_I2C_FS_SCL_HCNT

Address offset: 0xCD00001C HAL_DICE3_I2C_FS_SCL_HCNT

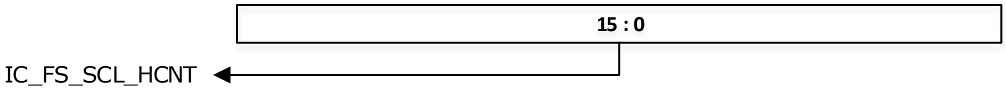

Table 8.9 I2C Fast Mode Clock SCL High Count Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
IC_FS_SCL_HCNT	15:0	0x1E	RW	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to "IC_CLK Frequency Configuration" on page 59 bkbk. This register can be written only when the I2C interface is disabled, which corresponds to HAL_DICE2_I2C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.

8.2.10 I2C Fast Mode Clock SCL Low Count Register – HAL_DICE3_I2C_FS_SCL_LCNT

Address offset: 0xCD000020 HAL_DICE3_I2C_FS_SCL_LCNT

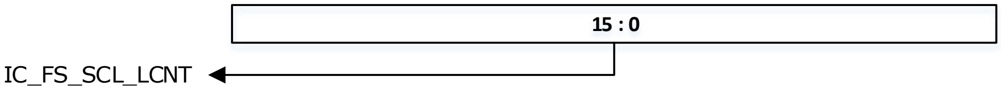

Table 8.10 I2C Fast Mode Clock SCL Low Count Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:16	0	N/A	Reserved
IC_FS_SCL_LCNT	15:0	0x41	RW	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to "IC_CLK Frequency Configuration" on page 59 bkbk. This register can be written only when the I2C interface is disabled, which corresponds to HAL_DICE3_I2C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set.

8.2.11 I2C Interrupt Status Register – HAL_DICE3_I2C_INTR_STAT

Address offset: 0xCD00002C HAL_DICE3_I2C_INTR_STAT

Each bit in this register has a corresponding mask bit in the HAL_DICE3_I2C_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the HAL_DICE3_I2C_RAW_INTR_STAT register.

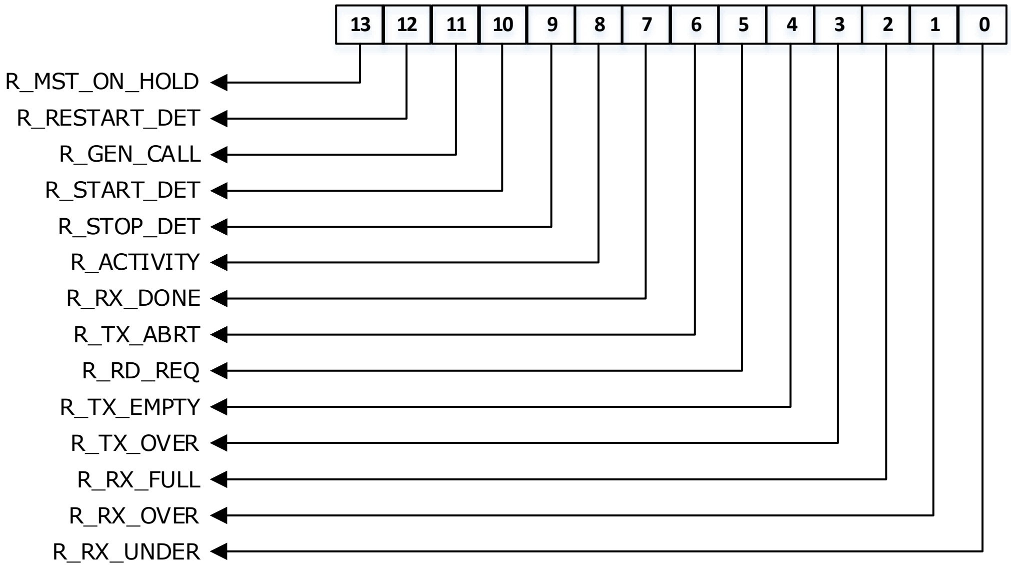

Table 8.11 I2C Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:14	0	N/A	Reserved
R_MST_ON_HOLD	13	0	R	See “IC_RAW_INTR_STAT” on page 128 bkbk for a detailed description of these bits.
R_RESTART_DET	12	0	R	
R_GEN_CALL	11	0	R	
R_START_DET	10	0	R	
R_STOP_DET	9	0	R	
R_ACTIVITY	8	0	R	
R_RX_DONE	7	0	R	
R_TX_ABRT	6	0	R	
R_RD_REQ	5	0	R	
R_TX_EMPTY	4	0	R	
R_TX_OVER	3	0	R	

Name	Bit	Reset	Dir	Description
R_RX_FULL	2	0	R	
R_RX_OVER	1	0	R	
R_RX_UNDER	0	0	R	

8.2.12 I2C Interrupt Mask Register – HAL_DICE3_I2C_INTR_MASK

Address offset: 0xCD000030 HAL_DICE3_I2C_INTR_MASK

These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

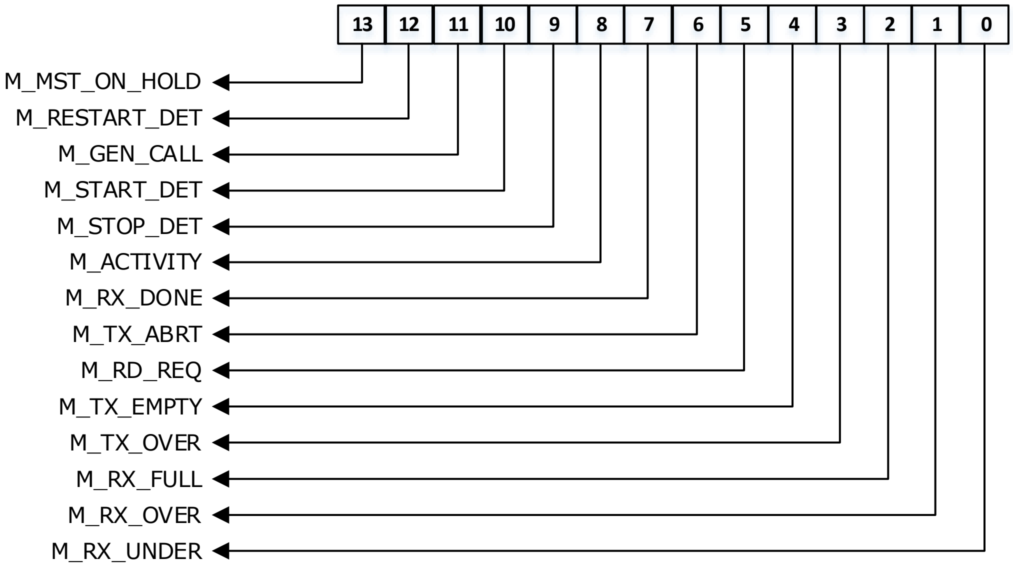

Table 8.12 I2C Interrupt Mask Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:14	0	N/A	Reserved
M_MST_ON_HOLD	13	1	RW	This bit masks the R_MST_ON_HOLD interrupt bit in the HAL_DICE3_I2C_INTR_STAT register.
M_RESTART_DET	12	1	RW	This bit masks the R_RESTART_DET interrupt status bit in the HAL_DICE3_I2C_INTR_STAT register.
M_GEN_CALL	11	1	RW	These bits mask their corresponding interrupt status bits in the HAL_DICE3_I2C_INTR_STAT register.
M_START_DET	10	1	RW	
M_STOP_DET	9	1	RW	
M_ACTIVITY	8	1	RW	

Name	Bit	Reset	Dir	Description
M_RX_DONE	7	1	RW	
M_TX_ABRT	6	1	RW	
M_RD_REQ	5	1	RW	
M_TX_EMPTY	4	1	RW	
M_TX_OVER	3	1	RW	
M_RX_FULL	2	1	RW	
M_RX_OVER	1	1	RW	
M_RX_UNDER	0	1	RW	

8.2.13 I2C Raw Interrupt Status Register – HAL_DICE3_I2C_RAW_INTR_STAT

Address offset: 0xCD000034 HAL_DICE3_I2C_RAW_INTR_STAT

Unlike the HAL_DICE3_I2C_INTR_STAT register, these bits are not masked so they always show the true status of the I2C Module.

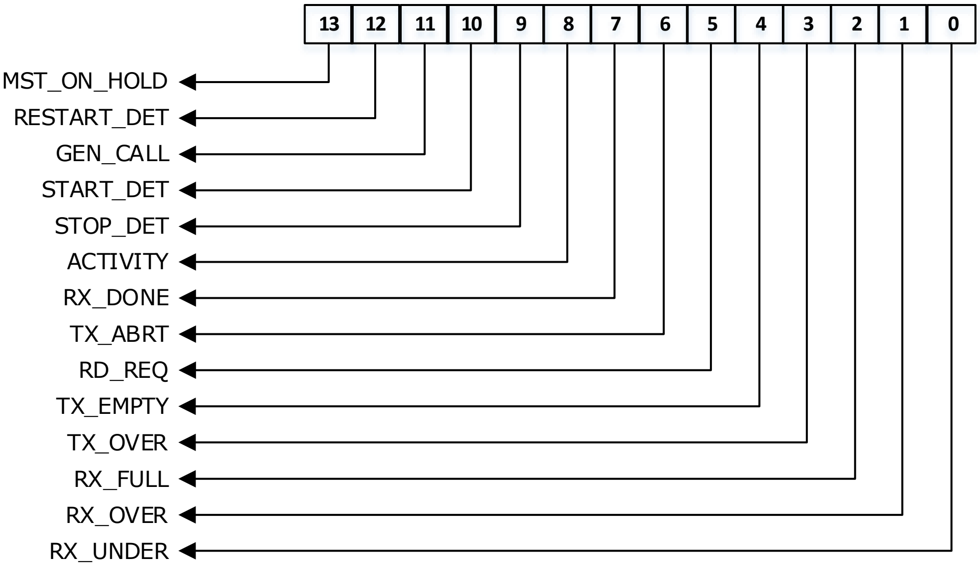

Table 8.13 I2C Raw Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:14	0	N/A	Reserved
MST_ON_HOLD	13	0	R	Indicates whether a master is holding the bus and the Tx FIFO is empty.

Name	Bit	Reset	Dir	Description
RESTART_DET	12	0	R	Indicates whether a RESTART condition has occurred on the I2C interface when I2C Module is operating in slave mode and the slave is the addressed slave.
GEN_CALL	11	0	R	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling I2C Module or when the CPU reads bit 0 of the HAL_DICE3_I2C_CLR_GEN_CALL register. I2C Module stores the received data in the Rx buffer.
START_DET	10	0	R	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether I2C Module is operating in slave or master mode.
STOP_DET	9	0	R	The behavior of the STOP_DET interrupt status differs based on the STOP_DET_IFADDRESSED selection in the IC_CON register • When STOP_DET_IFADDRESSED=0 Indicates whether a STOP condition has occurred on the I2C interface regardless of whether I2C Module is operating in slave or master mode. In slave mode, a STOP_DET interrupt is generated irrespective of whether the slave is addressed or not. • When STOP_DET_IFADDRESSED=1 In Master Mode (MASTER_MODE=1), indicates a STOP condition has occurred on the I2C interface. In Slave Mode (MASTER_MODE=0), a STOP_DET interrupt is generated only if the slave is addressed. **NOTE:** During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IFADDRESSED=1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).

Name	Bit	Reset	Dir	Description
ACTIVITY	8	0	R	This bit captures I2C Module activity and stays set until it is cleared. There are four ways to clear it: • Disabling the I2C Module • Reading the HAL_DICE3_I2C_CLR_ACTIVITY register • Reading the HAL_DICE3_I2C _CLR_INTR register • System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the I2C Module module is idle, this bit remains set until cleared, indicating that there was activity on the bus.
RX_DONE	7	0	R	When the I2C Module is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
TX_ABRT	6	0	R	This bit indicates if I2C Module, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a "transmit abort". When this bit is set to 1, the HAL_DICE3_I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort took place. **NOTE**: The I2C Module flushes/resets/empties both TX_FIFO and RX_FIFO whenever there is a transmit abort caused by any of the events tracked by the IC_TX_ABRT_SOURCE register. The Tx FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface.

Name	Bit	Reset	Dir	Description
RD_REQ	5	0	R	This bit is set to 1 when I2C Module is acting as a slave and another I2C master is attempting to read data from I2C Module. The I2C Module holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the HAL_DICE3_I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the HAL_DICE3_I2C_CLR_RD_REQ register.
TX_EMPTY	4	0	R	The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. • When TX_EMPTY_CTRL=0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. • When TX_EMPTY_CTRL=1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the HAL_DICE3_I2C_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When HAL_DICE3_I2C_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with **ic_en**=0, this bit is set to 0.

Name	Bit	Reset	Dir	Description
TX_OVER	3	0	R	Set during transmit if the transmit buffer is filled to 8 and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and **ic_en** goes to 0, this interrupt is cleared.
RX_FULL	2	0	R	Set when the receive buffer reaches or goes above the RX_TL threshold in the HAL_DICE3_I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (HAL_DICE3_I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once HAL_DICE3_I2C_ENABLE[0] is set to 0, regardless of the activity that continues.
RX_OVER	1	0	R	Set if the receive buffer is completely filled to 8 and an additional byte is received from an external I2C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (HAL_DICE3_I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when **ic_en** goes to 0, this interrupt is cleared. **NOTE:** Due to the component parameter configuration, this interrupt is never set to 1 since the criteria to set it are never met.
RX_UNDER	0	0	R	Set if the processor attempts to read the receive buffer when it is empty by reading from the HAL_DICE3_I2C_DATA_CMD register. If the module is disabled (HAL_DICE3_I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when **ic_en** goes to 0, this interrupt is cleared.

8.2.14 I2C Receive FIFO Threshold Register – HAL_DICE3_I2C_RX_TL

Address offset: 0xCD000038 HAL_DICE3_I2C_RX_TL

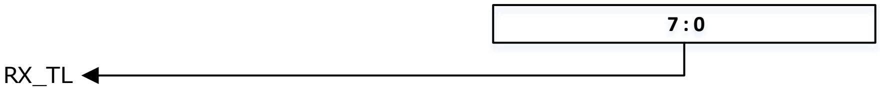

Table 8.14 I2C Receive FIFO Threshold Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
RX_TL	7:0	0	RW	Receive FIFO Threshold Level controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in HAL_DICE3_I2C_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.

8.2.15 I2C Transmit FIFO Threshold Register – HAL_DICE3_I2C_TX_TL

Address offset: 0xCD00003C HAL_DICE3_I2C_TX_TL

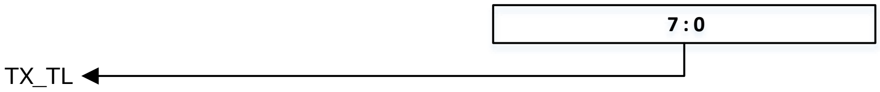

Table 8.15 I2C Transmit FIFO Threshold Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
TX_TL	7:0	0	RW	Transmit FIFO Threshold Level controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in HAL_DICE3_I2C_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

8.2.16 I2C Clear Interrupts Register – HAL_DICE3_I2C_CLR_INTR

Address offset: 0xCD000040 HAL_DICE3_I2C_CLR_INTR

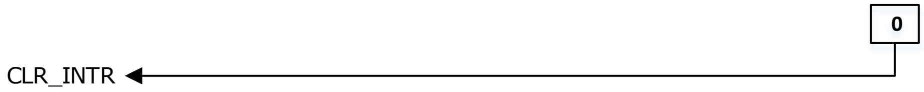

Table 8.16 I2C Clear Interrupts Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_INTR	0	0	R	Read this register to clear the combined interrupt, all individual interrupts, and the HAL_DICE3_I2C_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to bit 9 of the HAL_DICE3_I2C_TX_ABRT_SOURCE register for an exception to clearing HAL_DICE3_I2C_TX_ABRT_SOURCE.

8.2.17 I2C Clear RX_UNDER Interrupt Register – HAL_DICE3_I2C_CLR_RX_UNDER

Address offset: 0xCD000044 HAL_DICE3_I2C_CLR_RX_UNDER

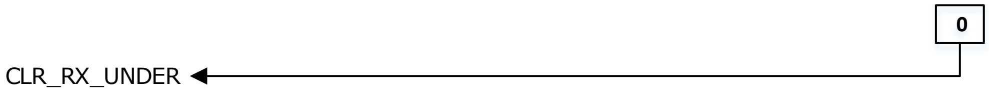

Table 8.17 I2C Clear RX_UNDER Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_RX_UNDER	0	0	R	Read this register to clear the RX_UNDER interrupt (bit 0) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.18 I2C Clear RX_OVER Interrupt Register – HAL_DICE3_I2C_CLR_RX_OVER

Address offset: 0xCD000048

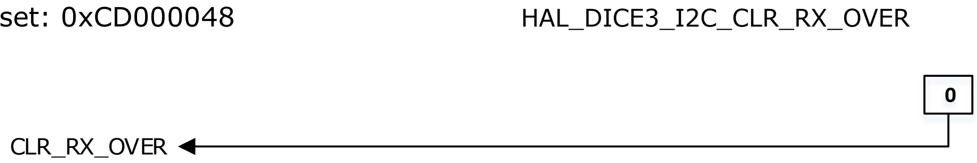

Table 8.18 I2C Clear RX_OVER Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_RX_OVER	0	0	R	Read this register to clear the RX_OVER interrupt (bit 1) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.19 I2C Clear TX_OVER Interrupt Register – HAL_DICE3_I2C_CLR_TX_OVER

Address offset: 0xCD00004C

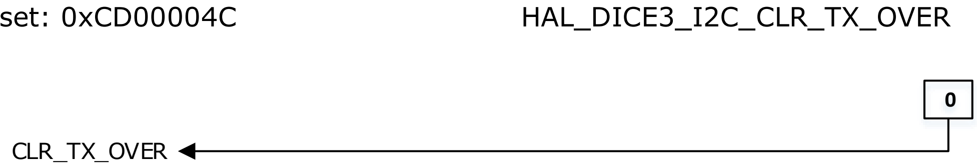

Table 8.19 I2C Clear TX_OVER Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_TX_OVER	0	0	R	Read this register to clear the *TX_OVER* interrupt (bit 3) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.20 I2C Clear RD_REQ Interrupt Register – HAL_DICE3_I2C_CLR_RD_REQ

Address offset: 0xCD000050 HAL_DICE3_I2C_CLR_RD_REQ

Table 8.20 I2C Clear RD_REQ Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_RD_REQ	0	0	R	Read this register to clear the RD_REQ interrupt (bit 5) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.21 I2C Clear TX_ABRT Interrupt Register – HAL_DICE3_I2C_CLR_TX_ABRT

Address offset: 0xCD000054 HAL_DICE3_I2C_CLR_TX_ABRT

Table 8.21 I2C Clear TX_ABRT Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_TX_ABRT	0	0	R	Read this register to clear the TX_ABRT interrupt (bit 6) of the HAL_DICE3_I2C_RAW_INTR_STAT register, and the HAL_DICE3_I2C_TX_ABRT_SOURCE register. This also releases the Tx FIFO from the flushed/reset state, allowing more writes to the Tx FIFO. Refer to Bit 9 of the HAL_DICE3_I2C_TX_ABRT_SOURCE register for an exception to clearing HAL_DICE3_I2C_TX_ABRT_SOURCE.

8.2.22 I2C Clear RX_DONE Interrupt Register – HAL_DICE3_I2C_CLR_RX_DONE

Address offset: 0xCD000058 HAL_DICE3_I2C_CLR_RX_DONE

0
CLR_RX_DONE

Table 8.22 I2C Clear RX_DONE Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_RX_DONE	0	0	R	Read this register to clear the RX_DONE interrupt (bit 7) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.23 I2C Clear ACTIVITY Interrupt Register – HAL_DICE3_I2C_CLR_ACTIVITY

Address offset: 0xCD00005C HAL_DICE3_I2C_CLR_ACTIVITY

0
CLR_ACTIVITY

Table 8.23 I2C Clear ACTIVITY Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_ACTIVITY	0	0	R	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.24 I2C Clear STOP_DET Interrupt Register – HAL_DICE3_I2C_CLR_STOP_DET

Address offset: 0xCD000060 HAL_DICE3_I2C_CLR_STOP_DET

0
CLR_STOP_DET

Table 8.24 I2C Clear STOP_DET Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_STOP_DET	0	0	R	Read this register to clear the STOP_DET interrupt (bit 9) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.25 I2C Clear START_DET Interrupt Register – HAL_DICE3_I2C_CLR_START_DET

Address offset: 0xCD000064 HAL_DICE3_I2C_CLR_START_DET

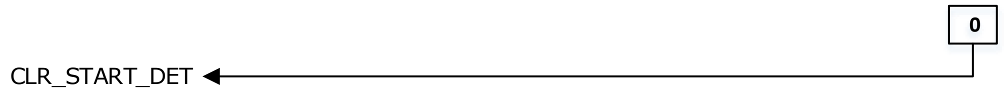

Table 8.25 I2C Clear START_DET Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_START_DET	0	0	R	Read this register to clear the START_DET interrupt (bit 10) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.26 I2C Clear GEN_CALL Interrupt Register – HAL_DICE3_I2C_CLR_GEN_CALL

Address offset: 0xCD000068 HAL_DICE3_I2C_CLR_GEN_CALL

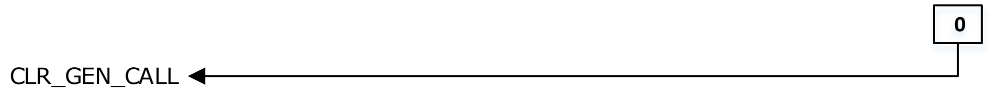

Table 8.26 I2C Clear GEN_CALL Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_GEN_CALL	0	0	R	Read this register to clear the GEN_CALL interrupt (bit 11) of HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.27 I2C Enable Register – HAL_DICE3_I2C_ENABLE

Address offset: 0xCD00006C HAL_DICE3_I2C_ENABLE

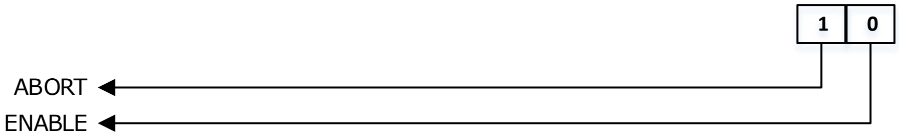

Table 8.27 I2C Enable Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:2	0	N/A	Reserved
ABORT	1	0	RW	When set, the controller initiates the transfer abort. • 0: ABORT not initiated or ABORT done • 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation. For a detailed description on how to abort I2C transfers, refer to “Aborting I2C Transfers” on page 57 bkbk.

Name	Bit	Reset	Dir	Description
ENABLE	0	0	RW	Controls whether the I2C Module is enabled. • 0: Disables I2C Module (TX and RX FIFOs are held in an erased state) • 1: Enables I2C Module Software can disable I2C Module while it is active. However, it is important that care be taken to ensure that I2C Module is disabled properly. A recommended procedure is described in “Disabling I2C Module” on page bkbk. When I2C Module is disabled, the following occurs: • The TX FIFO and RX FIFO get flushed. • Status bits in the IC_INTR_STAT register are still active until I2C Module goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the I2C Module stops the current transfer at the end of the current byte and does not acknowledge the transfer. [bkbk *In systems with asynchronous* ***pclk*** *and* ***ic_clk*** *when IC_CLK_TYPE parameter set to asynchronous (1), there is a two* ***ic_clk*** *delay when enabling or disabling the I2C Module. For a detailed description on how to disable I2C Module, refer to “Disabling I2C Module” on page 57* bkbk.]

8.2.28 I2C Status Register – HAL_DICE3_I2C_STATUS

Address offset: 0xCD000070 HAL_DICE3_I2C_STATUS

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the I2C is disabled by writing 0 in bit 0 of the DICE3_HAL_I2C_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and **ic_en**=0:

- Bits 5 and 6 are set to 0

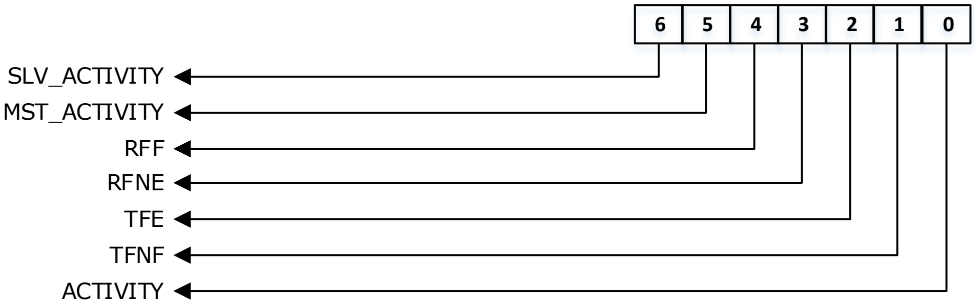

Table 8.28 I2C Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:7	0	N/A	Reserved
SLV_ACTIVITY	6	0	R	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. **0:** Slave FSM is in IDLE state so the Slave part of I2C Module is not Active **1:** Slave FSM is not in IDLE state so the Slave part of I2C Module is Active
MST_ACTIVITY	5	0	R	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. **0:** Master FSM is in IDLE state so the Master part of I2C Module is Not Active **1:** Master FSM is not in IDLE state so the Master part of I2C Module is Active **NOTE**: HAL_DICE3_I2C_STATUS[0] - that is, ACTIVITY bit - is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.
RFF	4	0	R	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. **0:** Receive FIFO is not full **1:** Receive FIFO is full
RFNE	3	0	R	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. **0:** Receive FIFO is empty **1:** Receive FIFO is not empty

Name	Bit	Reset	Dir	Description
TFE	2	1	R	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. **0:** Transmit FIFO is not empty **1:** Transmit FIFO is empty
TFNF	1	1	R	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. **0:** Transmit FIFO is full **1:** Transmit FIFO is not full
ACTIVITY	0	0	R	I2C Activity Status

8.2.29 I2C Transmit FIFO Level Register – HAL_DICE3_I2C_TXFLR

Address offset: 0xCD000074 HAL_DICE3_I2C_TXFLR

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort—that is, TX_ABRT bit is set in the HAL_DICE3_I2C_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

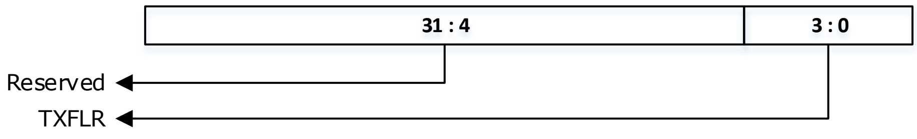

Table 8.29 I2C Transmit FIFO Level Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	N/A	Reserved
TXFLR	3:0	0	R	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

8.2.30 I2C Receive FIFO Level Register – HAL_DICE3_I2C_RXFLR

Address offset: 0xCD000078 HAL_DICE3_I2C_RXFLR

This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in HAL_DICE3_I2C_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

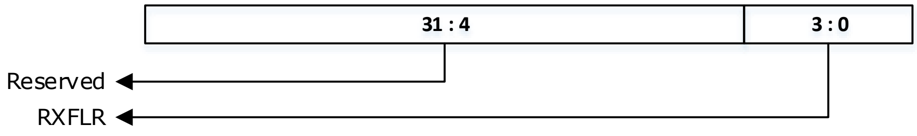

Table 8.30 I2C Receive FIFO Level Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	N/A	Reserved
RXFLR	3:0	0	R	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

8.2.31 I2C SDA Hold Time Length Register – HAL_DICE3_I2C_SDA_HOLD

Address offset: 0xCD00007C HAL_DICE3_I2C_SDA_HOLD

The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW).
The bits [23:16] of this register rare used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode.
Writes to this register succeed only when HAL_DICE3_I2C_ENABLE[0]=0.
The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode - one cycle in master mode, seven cycles in slave mode - for the value to be implemented.
The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

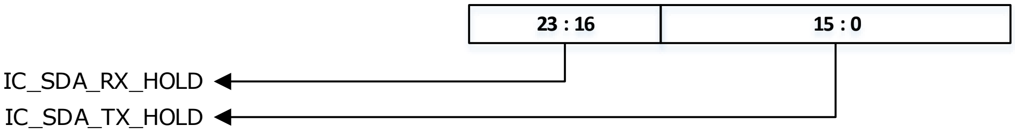

Table 8.31 I2C SDA Hold Time Length Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:24	0	N/A	Reserved
IC_SDA_RX_HOLD	23:16	1	RW	Sets the required SDA hold time in units of **ic_clk** period, when I2C Module acts as a receiver.
IC_SDA_TX_HOLD	15:0	1	RW	Sets the required SDA hold time in units of **ic_clk** period, when I2C Module acts as a transmitter.

8.2.32 I2C Transmit Abort Source Register – HAL_DICE3_I2C_TX_ABRT_SOURCE

Address offset: 0xCD000080 HAL_DICE3_I2C_TX_ABRT_SOURCE

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the HAL_DICE3_I2C_CLR_TX_ABRT register or the HAL_DICE3_I2C_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (HAL_DICE3_I2C_CON[5]=1), the SPECIAL bit must be cleared (HAL_DICE3_I2C_TAR[11]), or the GC_OR_START bit must be cleared (HAL_DICE3_I2C_TAR[10]).
Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

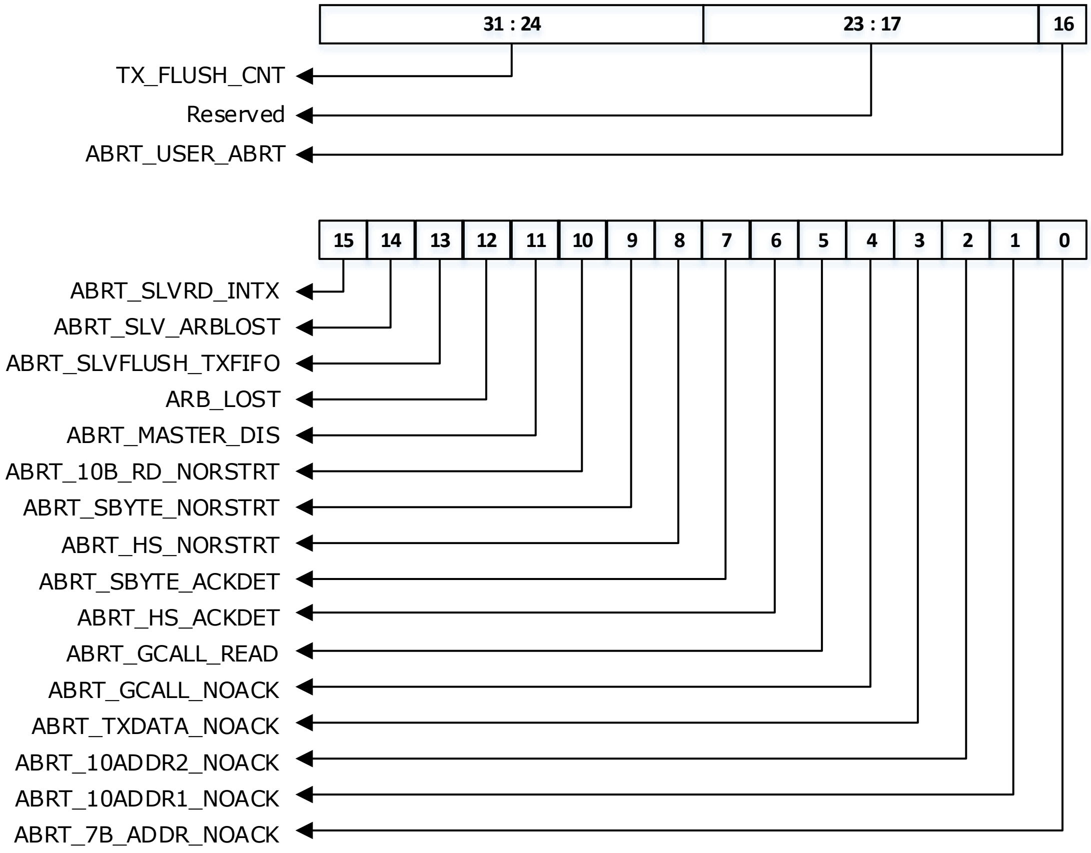

Table 8.32 I2C Transmit Abort Source Register bit assignments

Name	Bit	Reset	Dir	Description
TX_FLUSH_CNT	31:24	0	RW	Master-transmitter or Slave-transmitter: This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I2C is disabled.
Reserved	23:17	0	N/A	Reserved
ABRT_USER_ABRT	16	0	R	Master-transmitter: This is a master-mode-only bit. Master has detected the transfer abort (HAL_DICE3_I2C_ENABLE[1]).
ABRT_SLVRD_INTX	15	0	R	Slave-transmitter: 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of HAL_DICE3_I2C_DATA_CMD register.

Name	Bit	Reset	Dir	Description
ABRT_SLV_ARBLOST	14	0	R	Slave-transmitter: **1:** Slave lost the bus while transmitting data to a remote master. HAL_DICE3_I2C_TX_ABRT_SOURCE[12] is set at the same time. **NOTE**: Even though the slave never "owns" the bus, something could go wrong on the bus. This is a fail-safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then I2C Module no longer own the bus.
ABRT_SLVFLUSH_TXFIFO	13	0	R	Slave-transmitter: **1:** Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
ARB_LOST	12	0	R	Master-transmitter or Slave-transmitter: 1: Master has lost arbitration, or if HAL_DICE3_I2C_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
ABRT_MASTER_DIS	11	0	R	Master-transmitter or Master-receiver: User tries to initiate a Master operation with the Master mode disabled.
ABRT_10B_RD_NORSTRT	10	0	R	Master-receiver: 1: The restart is disabled (IC_RESTART_EN bit (HAL_DICE2_I2C_CON[5])=0) and the master sends a read command in 10-bit addressing mode.

Name	Bit	Reset	Dir	Description
ABRT_SBYTE_NORSTRT	9	0	R	Master: To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (HAL_DICE3_I2C_CON[5]=1), the SPECIAL bit must be cleared (HAL_DICE3_I2C_TAR[11]), or the GC_OR_START bit must be cleared (HAL_DICE3_I2C_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. **1:** The restart is disabled (IC_RESTART_EN bit (HAL_DICE3_I2C_CON[5])=0) and the user is trying to send a START Byte.
ABRT_HS_NORSTRT	8	0	R	[Not used] Master-transmitter or Master-receiver: **1:** The restart is disabled (*IC_RESTART_EN* bit (HAL_DICE3_I2C_CON[5])=0) and the user is trying to use the master to transfer data in High Speed mode.
ABRT_SBYTE_ACKDET	7	0	R	Master: **1:** Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
ABRT_HS_ACKDET	6	0	R	[Not used] Master: **1:** Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
ABRD_GCALL_READ	5	0	R	Master-transmitter: **1:** I2C Module in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (HAL_DICE3_I2C_DATA_CMD[9] is set to 1).
ABRT_GCALL_NOACK	4	0	R	Master-transmitter: **1:** I2C Module in master mode sent a General Call and no slave on the bus acknowledged the General Call.

Name	Bit	Reset	Dir	Description
ABRT_TXDATA_NOACK	3	0	R	Master-transmitter: **1:** This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
ABRT_10ADDR2_NOACK	2	0	R	Master-transmitter or Master-receiver: **1:** Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
ABRT_10ADDR1_NOACK	1	0	R	Master-transmitter or Master-receiver: **1:** Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
ABRT_7B_NOACK	0	0	R	Master-transmitter or Master-receiver: **1:** Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

8.2.33 I2C Generate SLV_DATA_NACK Register – HAL_DICE3_I2C_SLV_DATA_NACK_ONLY

Address offset: 0xCD000084 HAL_DICE3_I2C_SLV_DATA_NACK_ONLY

The register is used to generate a NACK for the data part of a transfer when I2C Module is acting as a slave-receiver. A write can occur on this register if both of the following conditions are met:

- I2C Module is disabled (HAL_DICE3_I2C_ENABLE[0]=0)
- Slave part is inactive (HAL_DICE3_I2C_STATUS[6]=0)

Note

The HAL_DICE3_I2C_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

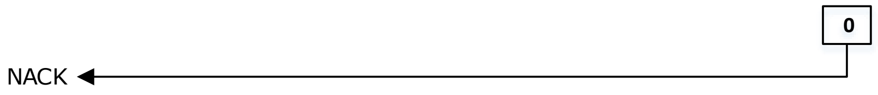

Table 8.33 I2C Generate SLV_DATA_NACK Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
NACK	0	0	RW	Generate NACK. This NACK generation only occurs when I2C Module is a slave-receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. **1:** generate NACK after data byte received **0:** generate NACK/ACK normally

8.2.34 I2C DMA Control Register – HAL_DICE3_I2C_DMA_CR

Address offset: 0xCD000088 HAL_DICE3_I2C_DMA_CR

The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of HAL_DICE3_I2C_ENABLE.

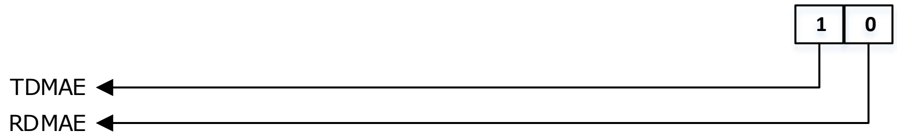

Table 8.34 I2C DMA Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:2	0	N/A	Reserved
TDMAE	1	0	RW	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. **0:** Transmit DMA disabled **1:** Transmit DMA enabled
RDMAE	0	0	RW	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. **0:** Receive DMA disabled **1:** Receive DMA enabled

8.2.35 I2C DMA Transmit Data Level Register – HAL_DICE3_I2C_DMA_TDLR

Address offset: 0xCD00008C HAL_DICE3_I2C_DMA_TDLR

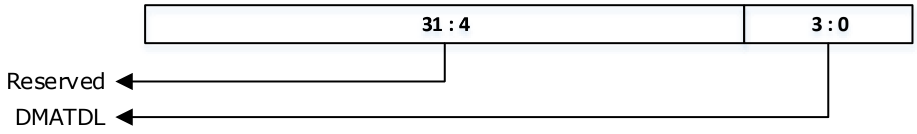

Table 8.35 I2C DMA Transmit Data Level Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	N/A	Reserved
DMATDL	3:0	0	RW	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the **dma_tx_req** signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE=1.

8.2.36 I2C DMA Receive Data Level Register – HAL_DICE3_I2C_DMA_RDLR

Address offset: 0xCD000090 HAL_DICE3_I2C_DMA_RDLR

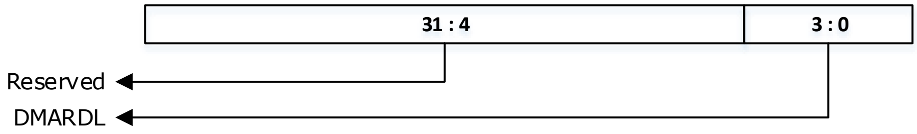

Table 8.36 I2C DMA Receive Data Level Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:4	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
DMARDL	3:0	0	RW	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level=DMARDL+1; that is, **dma_rx_req** is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value+1, and RDMAE=1. For instance, when DMARDL is 0, then **dma_rx_req** is asserted when 1 or more data entries are present in the receive FIFO.

8.2.37 I2C SDA Setup Register – HAL_DICE3_I2C_SDA_SETUP

Address offset: 0xCD000094 HAL_DICE3_I2C_SDA_SETUP

This register controls the amount of time delay (in terms of number of **ic_clk** clock periods) introduced in the rising edge of SCL - relative to SDA changing - by holding SCL low when I2C Module services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.
Writes to this register succeed only when HAL_DICE3_I2C_ENABLE[0]=0.

Note

The length of setup time is calculated using [(IC_SDA_SETUP-1)*(**ic_clk_period**)], so if the user requires 10 **ic_clk** periods of setup time, they should program a value of 11.
The HAL_DICE3_I2C_SDA_SETUP register is only used by the I2C Module when operating as a slave transmitter.

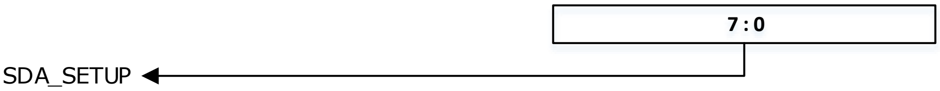

Table 8.37 I2C SDA Setup Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
SDA_SETUP	0	0x64	RW	SDA Setup. It is recommended that if the required delay is 1000ns, then for an **ic_clk** frequency of 10 MHz, SDA_SETUP should be programmed to a value of 11. SDA_SETUP must be programmed with a minimum value of 2.

8.2.38 I2C ACK General Call Register – HAL_DICE3_I2C_ACK_GENERAL_CALL

Address offset: 0xCD000098 HAL_DICE3_I2C_ACK_GENERAL_CALL

The register controls whether I2C Module responds with an ACK or NACK when it receives an I2C General Call address. This register is applicable only when the I2C Module is in the slave mode.

0
ACK_GEN_CALL

Table 8.38 I2C ACK General Call Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
ACK_GEN_CALL	0	1	RW	ACK General Call. When set to 1, I2C Module responds with a ACK (by asserting **ic_data_oe**) when it receives a General Call. When set to 0, the I2C Module does not generate General Call interrupts.

8.2.39 I2C Enable Status Register – HAL_DICE3_I2C_ENABLE_STATUS

Address offset: 0xCD00009C HAL_DICE3_I2C_ENABLE_STATUS

The register is used to report the I2C Module hardware status when HAL_DICE3_I2C_ENABLE[0] is set from 1 to 0; that is, when I2C Module is disabled.
If HAL_DICE3_I2C_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
If HAL_DICE3_I2C_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.

Note

When HAL_DICE3_I2C_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the I2C Module depends on I2C bus activities.

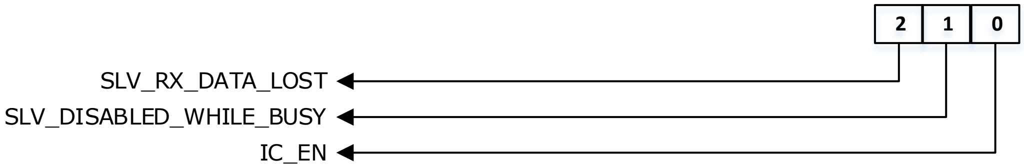

Table 8.39 I2C Enable Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:3	0	N/A	Reserved
SLV_RX_DATA_LOST	2	0	R	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to setting HAL_DICE3_I2C_ENABLE[0] from 1 to 0. When read as 1, I2C Module is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. **NOTE:** If the remote I2C master terminates the transfer with a STOP condition before the I2C Module has a chance to NACK a transfer, and HAL_DICE3_I2C_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, I2C Module is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. **NOTE:** The CPU can safely read this bit when IC_EN (bit 0) is read as 0.

Name	Bit	Reset	Dir	Description
SLV_DISABLED_WHILE_BUSY	1	0	R	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to bit 0 of HAL_DICE3_I2C_ENABLE while: (a) I2C Module is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, I2C Module is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in I2C Module (IC_SAR register) OR if the transfer is completed before bit 0 of IC_ENABLE is set to 0, but has not taken effect. **NOTE:** If the remote I2C master terminates the transfer with a STOP condition before the I2C Module has a chance to NACK a transfer, and bit 0 of IC_ENABLE has been set to 0, then this bit will also be set to 1. When read as 0, I2C Module is deemed to have been disabled when there is master activity, or when the I2C bus is idle. **NOTE:** The CPU can safely read this bit when IC_EN (bit 0) is read as 0.
IC_EN	0	0	R	**ic_en** Status. This bit always reflects the value driven on the output port **ic_en**. • When read as 1, I2C Module is deemed to be in an enabled state. • When read as 0, I2C Module is deemed completely inactive. **NOTE:** The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read *SLV_RX_DATA_LOST* (bit 2) and *SLV_DISABLED_WHILE_BUSY* (bit 1).

8.2.40 I2C ISS and FS Spike Suppression Limit Register – HAL_DICE3_I2C_FS_SPKLEN

Address offset: 0xCD0000A0 HAL_DICE3_I2C_FS_SPKLEN

This register is used to store the duration, measured in **ic_clk** cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in standard mode, fast mode, or fast mode plus. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

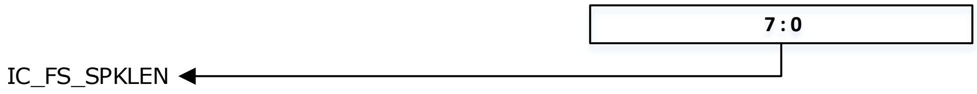

Table 8.40 I2C ISS and FS Spike Suppression Limit Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:8	0	N/A	Reserved
IC_FS_SPKLEN	7:0	3	RW	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in **ic_clk** cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to “Spike Suppression” on page bkbk 57. This register can be written only when the I2C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.

8.2.41 I2C Clear RESTART_DET Interrupt Register – HAL_DICE3_I2C_CLR_RESTART_DET

Address offset: 0xCD0000A8 HAL_DICE3_I2C_CLR_RESTART_DET

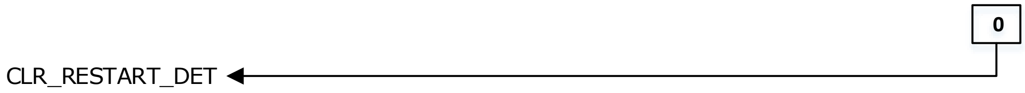

Table 8.41 I2C Clear RESTART_DET Interrupt Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	N/A	Reserved
CLR_RESTART_DET	0	0	R	Read this register to clear the RESTART_DET interrupt (bit 12) of the HAL_DICE3_I2C_RAW_INTR_STAT register.

8.2.42 I2C Component Parameter Register – HAL_DICE3_I2C_COMPONENT_PARAM_1

Address offset: 0xCD0000F4 HAL_DICE3_I2C_COMPONENT_PARAM_1

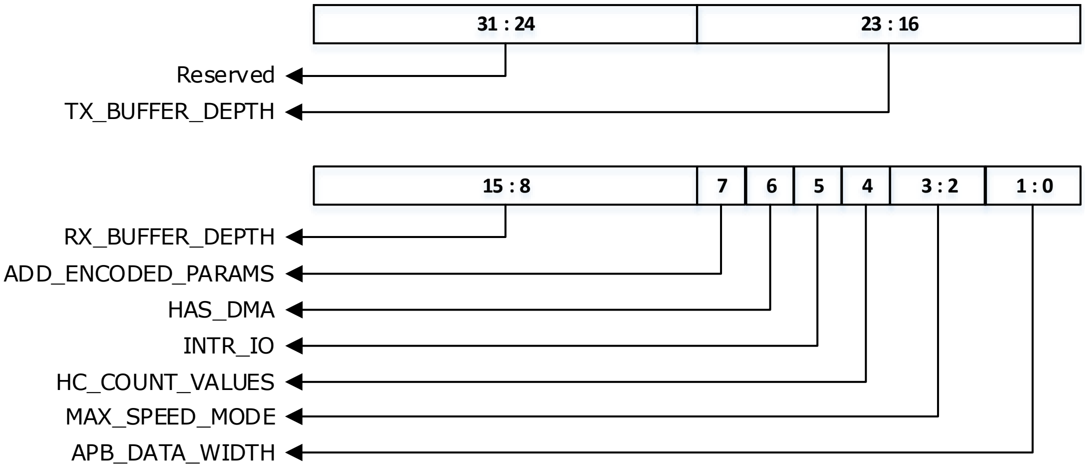

Table 8.42 I2C Component Parameter Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:24	0	N/A	Reserved
TX_BUFFER_DEPTH	23:16	8	R	I2C Module parameters
RX_BUFFER_DEPTH	15:8	8	R	
ADD_ENCODED_PARAMS	7	1	R	
HAS_DMA	6	1	R	
INTR_IO	5	1	R	
HC_COUNT_VALUES	4	0	R	
MAX_SPEED_MODE	3:2	2	R	
APB_DATA_WIDTH	1:0	32	R	

8.3 Revisions

Table 8.43 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication