ADC

Analog to Digital Converter

Revision 1.0.0-41542

June 15, 2015

31 ADC

31.1 Overview

This module is a simple successive approximation type AD with a selectable analog mux in front. The precision is 10 bits. This interface is primarily for reading pots, temperature sensors, etc. and is not intended for audio.

The successive approximation takes 16 F_{adc} clocks to complete. The clock provided is $F_{cpu}/16$. For a typical configuration F_{cpu} is 200MHz giving an F_{adc} of 12.5MHz and a conversion time of $16/F_{adc}$ = 1.28µs.

31.2 Module Configuration

Table 31.1 ADC base addresses

Base address		Description
0xC0000000	CYGHWR_HAL_DICE3_ADC	ADC module

Table 31.2 ADC register summary

Address Offset	Register	Description
0x0000	HAL_DICE3_ADC_CSR	*ADC CSR Register*
0x0004	HAL_DICE3_ADC_DATA	*ADC Data Register*

31.2.1 ADC CSR Register – HAL_DICE3_ADC_CSR

Address offset: 0x0000 HAL_DICE3_ADC_CSR

Control and status register.

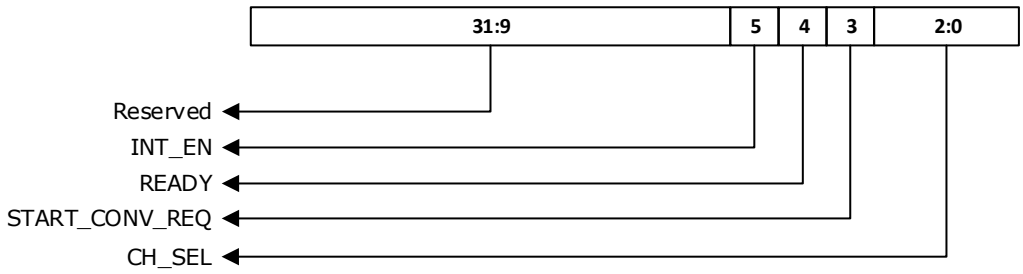

Table 31.3 ADC CSR Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:6	0	N/A	Reserved, read undefined, must read as zeros.
INT_EN	5	0	RW	When set, interrupt is enabled. Interrupt is generated when Ready set.
READY	4	0	R	When set, indicates that the conversion data is ready and stable. This is a sticky bit, and is cleared when 1 is written to this bit or the START_CONV_REQ bit.
START_CONV_REQ	3	0	W	Writing a 1 to this will generate the SOC pulse to start conversion. Also the READY bit is cleared if set when 1 is written. This bit has to be de-asserted before the next request is active.
CH_SEL	2:0	0	RW	Set these bits to select appropriate 0 to 7 channels

31.2.2 ADC Data Register – HAL_DICE3_ADC_DATA

Address offset: 0x0004 HAL_DICE3_ADC_DATA

Data register.

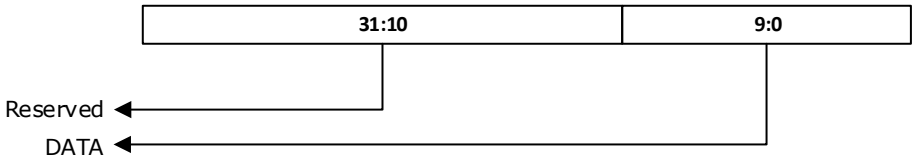

Table 31.4 ADC Data Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:10	0	N/A	Reserved, read undefined, must read as zeros.
DATA	9:0	0	RW	Current conversion data value.

31.3 Revisions

Table 31.5 Document revision history

Date	Rev.	By	Change
June 15, 2015	1.0.0-41542	BK	Initial publication