Float/Fix

Float/Fix Converter

Revision 0.9.0-41360

May 6, 2015

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30 Float/Fix

30.1 Float/Fix (fltfix) Engine

The fltfix engine is configured as a router device, which has 64 source channels and 64 destination channels. The first 64 channels are used to compute 32-bit float to 24-bit fixed-point conversions, and the last 64 channels are for 24-bit fixed to 32-bit floating-point conversions.

The floating point mapping is [-1.0;1.0[=> [0x800000;0x7fffff] with saturation. Only numbers from -1.0 inclusive to +1.0 non-inclusive are used. Numbers outside that range in float-2-fix will saturate and in fix-2-float will not be generated.

The 24 bit fix-point system with the decimal point being left of the most significant bit not including sign will represent [-1.0;1.0[as [-2^{23} ; 2^{23}-1], which can also be calculated as $N/2^{23}$ where N is the 24 bit signed integer representation of the fixed-point value. In other words, the Q notation for the 24-bit fixed point audio representation is Q0.23, i.e. the scaling factor for conversion is $2^{23.}$

30.1.1 Router Float/Fix Control Register – HAL_DICE3_FLOATFIX_CSR

Address: 0xC4000200 HAL_DICE3_FLOATFIX_CSR

The float/fix module is addressed through 1 base address, which represents a control register that is used to enable or disable the module.

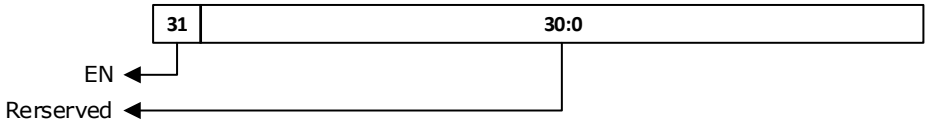

Table 30.1 Router Float/Fix Control Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	RW	Set to enable the fltfix engine.
Reserved	30:0	0	N/A	Reserved

30.2 Revisions

Table 30.2 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

