TCD3xxx
Rev1 Re-spin

Revision 0.1

October 1, 2014

1 Introduction

This document lists the changes done to the Rev1 version of the chip compared to the original. It includes details for the TCAT related changes and an overview of eSilicon changes to the ARM Sub System.

Change	Resp.	Comment
MPMC – address range	eSilicon	The MPMC was connected such that only 16MB was available to each of the two chip selects.
COMMRX/TX	eSilicon	These signals were not hooked up to the interrupt controller as expected.
DMA Arbitration	eSilicon	The BusMatrix would always prioritize CPU over DMA resulting in blocking the DMA
AVB Talker limit	TCAT	The AVB Talkers would only support 1 stream at 100Mb.
ETH Multicast Hash	TCAT	The Ethernet receiver did not have a hash table for multicast reception.
PEAK buffer	TCAT	The Peak detector was using the running buffer instead of the stored buffer.
Boot ROM	TCAT	The boot ROM uses too short timeouts for X-Modem.
ChipRev register	TCAT	The chip revision register should be changed to enable software to check revision.

Table 1, List of changes

2 Changes ARM SS (eSilicon)

The following changes are performed by eSilicon.

2.1 MPMC Address range

The chip select scheme for the MPMC is changed such that each of the two dynamic memory chip selects CS4 (chip CS0) and CS5 (chip CS1) cover 64MB.

SDRAM Address		CPU Address		DMA Address	
0x00000000	0x00FFFFFF	0x34000000	0x34FFFFFF	0x38000000	0x38FFFFFF
0x01000000	0x01FFFFFF	0x31000000	0x31FFFFFF	0x39000000	0x39FFFFFF
0x02000000	0x02FFFFFF	0x32000000	0x32FFFFFF	0x36000000	0x36FFFFFF
0x03000000	0x03FFFFFF	0x33000000	0x33FFFFFF	0x37000000	0x37FFFFFF

Table 2, SDRAM CS0

SDRAM Address		CPU Address		DMA Address	
0x00000000	0x00FFFFFF	0x38000000	0x38FFFFFF	0x3C000000	0x3CFFFFFF
0x01000000	0x01FFFFFF	0x35000000	0x35FFFFFF	0x3D000000	0x3DFFFFFF
0x02000000	0x02FFFFFF	0x36000000	0x36FFFFFF	0x3A000000	0x3AFFFFFF
0x03000000	0x03FFFFFF	0x37000000	0x37FFFFFF	0x3B000000	0x3BFFFFFF

Table 3, SDRAM CS1

The ranges have a different shuffle form the CPU and DMA point of view. The Virtual to Physical conversion in firmware will take care of that.

2.2 COMM RX/TX

These two interrupts from the ARM will be connected to the interrupt controller line 2 and 3.

Signal	Interrupt Line
COMMRX	2
COMMTX	3

2.3 DMA Arbitration

The DMAC and the DW_OTG are both DMA masters on the layer 2 bus. They can access peripherals and memory through the BusMatrix.
In the original design the Layer1 bus had fixed priority over the Layer2 bus which meant that the DMA's could be blocked when accessing internal memory in case the CPU was running code from internal memory.

The fix is to swap the priority for the internal ram so the DMA bus has priority.

3 Changes to DICE (TCAT)

The following changes are done to the DICE system:

3.1 AVB Talker Limit

When sending multiple streams at 100Mb the packets get concatenated because the FIFO never runs empty.
The logic has been simplified to fix that problem.

File: **avb_av_tx.v**
Line: 254
Changing

```
assign fifo_in_data = {mbus_req[cur_grant],mbus_data};
```

To

```
assign fifo_in_data = {mbus_den,mbus_data};
```

This change should not have any significant consequences as the old signal and the new signal both comes from the same clock domain (tx_clk) and the depth of logic is comparable.

3.2 ETH Multicast Hash

A hash scheme was added to the Ethernet receiver. It utilizes a CRC operation which is already existing in the code.

3.2.1 Register upper 6 bits of CRC from MAC receiver

File: **client_rx.v**
Line: 297

Add 6 registers registering the upper 6 bits of *crc_result_inv*
Enable logic is a simple compare of 14 existing registers to a constant.

Line: 51
Add port for the new hash register.

File: **tc_mac_top.v**
Just adding port for the hash register

File: **tc_mac_top_rgmii.v**
Just adding port for the hash register

3.2.2 Add two config register bits for vlan and bcast

File: **avb_host_generic_tcmac.v**

The two registers ethrx_mcvlan and ethrx_bcast are registering data bus. Enable logic already exist for mac_nreset so no new enable logic needed.

Also add reading of these bits, two constants replaced by Q from new registers.

Adding registers to module port

3.2.3 Signal routing

File: **avb_top_generic_tcmac.v**
The hash, mcvlan and bcast ports are connected between modules. No logic.

3.2.4 The hash filter system

File: **avb_mac_fltr_dst_etyp.v**

Select logic for register compAcc changed, added a 3 bit compare.

Select logic for regisrer rx_filtered changed, added 50 bit compare reg to const.

Add register hashflt and select logic. 32 bit select mux and some simple logic.

3.3 PEAK Buffer

Invert one address bit for ram.
File: **peaker.v**
Line: 163
Insert inverter.

3.4 Boot ROM

The boot ROM was not correctly setting the time for timeouts. The timer was set as a 16 bit timer and not 32 bit.

Furthermore the version of the ROM is changed to 1.1.0.2477

3.5 Chip Revision

File: **clock_pm_apb_if.v**
Line: 116

Simple change of the revision number readable by the ARM from 4'b0000 to 4'b0001.

3.6 Other change (do not implement)

This change is not required to fix. It was just found by inspection that latches were used instead of registers.

File: **aes_rx_auxbits.v**
Line: 117

Blocking assignments replaced by non-blocking. This will just make timing closure easier and is not a bug. Please don't include this change.