Watchdog Unit

Revision 0.9.0-41360

May 6, 2015

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8 Watchdog Unit

8.1 Overview

The Watchdog module is based around a 32-bit down counter that is initialized from the Reload Register, HAL_DICE3_WDG_LOAD. The watchdog clock generates a regular interrupt, depending on a programmed value. The counter decrements by one on each positive clock edge of the input clock when the clock enable is HIGH. The watchdog monitors the interrupt and asserts a reset WDOGRES signal, when the counter reaches zero, and the counter is stopped. On the next enabled clock edge the counter is reloaded from the HAL_DICE3_WDG_LOAD Register and the countdown sequence continues. If the interrupt is not cleared by the time that the counter next reaches zero then the Watchdog module reasserts the reset signal. The Watchdog module is intended to be used to apply a reset to a system in the event of a software failure, providing a way of recovering from software crashes. You can enable or disable the watchdog unit as required.

Table 8.1 lists the watchdog registers.

8.2 Module Configuration

Table 8.1 Watchdog unit register summary

Address	Register	Description
0xC1000000	HAL_DICE3_WDG_LOAD	*Watchdog Load Register*
0xC1000004	HAL_DICE3_WDG_VALUE	*Watchdog Value Register*
0xC1000008	HAL_DICE3_WDG_CTRL	*Watchdog Control Register*
0xC100000C	HAL_DICE3_WDG_INTCLR	*Watchdog Interrupt Clear Register*
0xC1000010	HAL_DICE3_WDG_RIS	*Watchdog Raw Interrupt Status Register*
0xC1000014	HAL_DICE3_WDG_MIS	*Watchdog Interrupt Status Register*
0xC1000C00	HAL_DICE3_WDG_LOCK	*Watchdog Lock Register*

8.2.1 Watchdog Load Register – HAL_ HAL_DICE3_WDG_LOAD

Address: 0xC1000000 HAL_DICE3_WDG_LOAD

The HAL_DICE3_WDG_LOAD Register is a 32-bit register containing the value from which the counter is to decrement. When this register is written to, the count is immediately restarted from the new value. The minimum valid value for HAL_DICE3_WDG_LOAD is 1.

8.2.2 Watchdog Value Register – HAL_DICE3_ WDG _VALUE

Address: 0xC1000004 HAL_DICE3_WDG_VALUE

The HAL_DICE3_ WDG_VALUE register gives the current 32-bit value of the decrementing counter.

8.2.3 Watchdog Control Register – HAL_DICE3_ WDG _CTRL

Address: 0xC1000008 HAL_DICE3_WDG_CTRL

The WDOGCONTROL Register is a read/write register that enables the software to control the watchdog unit. The table below shows the register bit assignments.

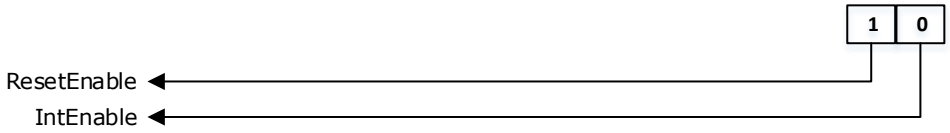

Table 8.2 Watchdog Control Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:2	0	R	Reserved, read undefined, must read as zeros.
ResetEnable	1	0	R	Enable Watchdog reset output. Acts as a mask for the reset output. Set HIGH to enable the reset, and LOW to disable the reset.
IntEnable	0	0	R	Enable the interrupt event. Set HIGH to enable the counter and the interrupt, and set LOW to disable the counter and interrupt. Reloads the counter from the value in HAL_DICE3_WDG_LOAD when the interrupt is enabled, and was previously disabled.

8.2.4 Watchdog Interrupt Clear Register – HAL_DICE3_WDG_INTCLR

Address: 0xC100000C HAL_DICE3_WDG_INTCLR

A write of any value to the HAL_DICE3_ WDG _INTCLR register clears the watchdog interrupt, and reloads the counter from the value in HAL_DICE3_WDG_LOAD.

8.2.5 Watchdog Raw Interrupt Status Register – HAL_DICE3_WDG _RIS

Address: 0xC1000010 HAL_DICE3_WDG_RIS

The HAL_DICE3_WDG_RIS Register is read-only. It indicates the raw interrupt status from the counter. This value is ANDed with the interrupt enable bit from the control register to create the masked interrupt, which is passed to the interrupt output pin. The table below shows the register bit assignments.

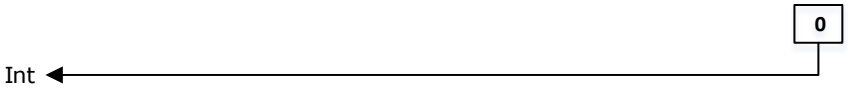

Table 8.3 Watchdog Raw Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	R	Reserved, read undefined, must read as zeros.
Int	0	0	R	Raw interrupt status from the counter

8.2.6 *Watchdog Interrupt Status Register* – HAL_DICE3_WDG_MIS

Address: 0xC1000014 HAL_DICE3_WDG_MIS

The HAL_DICE3_WDG_MIS register is read-only. It indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the IntEnable bit from the control register, and is the same value that is passed to the interrupt output pin. The figure below shows the register bit assignments.

Table 8.4 Watchdog Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Reserved	31:1	0	R	Reserved, read undefined, must read as zeros.
Int	0	0	R	Enabled interrupt status from the counter

8.2.7 Watchdog Lock Register – HAL_DICE3_ WDG _LOCK

Address: 0xC1000C00 HAL_DICE3_WDG_LOCK

The HAL_DICE3_WDG_LOCK register is write-only. Use of this register causes write-access to all other registers to be disabled. This is to prevent rogue software from disabling the watchdog functionality. Writing a value of0x1ACCE551 enables write access to all other registers. Writing any other value disables write accesses. A read from this register returns only the bottom bit:

- 0 indicates that write access is enabled, not locked
- 1 indicates that write access is disabled, locked.

Table 8.5 Watchdog Interrupt Status Register bit assignments

Name	Bit	Reset	Dir	Description
Enable register writes	31:1	0	W	Enable write access to all other registers by writing 0x1ACCE551. Disable write access by writing any other value.
Register write enable status	0	0	RW	Enabled interrupt status from the counter

8.3 Revisions

Table 8.6 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

