AIO

CPU Audio IO Module

Revision 0.9.0-41360

May 6, 2015

LIST OF TABLES **28-3**

LIST OF FIGURES **28-4**

28 AIO MODULE **28-5**

28.1 MODULE OVERVIEW 28-5

28.1.1 Router AIO CSR Register – HAL_DICE3_AIO_CSR *28-6*

28.1.2 Router AIO Clear Register – HAL_DICE3_AIO_CLR *28-8*

28.1.3 Router AIO Time Register – HAL_DICE3_AIO_TIME *28-9*

28.2 REVISIONS 28-10

List of Tables

TABLE 28.1 AIO BASE ADDRESSES 28-5
TABLE 28.2 AIO BUFFER OFFSETS SUMMARY 28-5
TABLE 28.3 AIO REGISTER SUMMARY 28-6
TABLE 28.4 ROUTER AIO CSR REGISTER BIT ASSIGNMENTS 28-6
TABLE 28.5 DPT EXAMPLE - CHANNELS VS. NUMBER OF SAMPLES 28-7
TABLE 28.6 ROUTER AIO CLEAR REGISTER BIT ASSIGNMENTS 28-8
TABLE 28.7 ROUTER AIO TIME REGISTER BIT ASSIGNMENTS 28-9
TABLE 28.8 DOCUMENT REVISION HISTORY 28-10

List of Figures

NO TABLE OF FIGURES ENTRIES FOUND.

28 AIO Module

28.1 Module Overview

The AIO module enables routing of up to 64 channels of audio to and from the ARM sub-system. The ARM can then process those samples in an interrupt routine.

The module is a DICE router module which can be configured to route up 64 rx and 64 tx channels.

The maximum buffer size supported by the DICE III implementation is 128 words, and the system can be configured for a trade-off between sample depth and channels.

Principle of operation:
Ping/pong scheme with N samples in each buffer. N is variable.
Each buffer contains a number of channels M. M is variable.
Each of the two buffers hold 128 elements. (2**CPU_WBUF elements, CPU_WBUF is a constant and is 7 for DICE III).
This means that M+N must be less than or equal to 128. See *Table 28.5* below for channel/sample configurations.

From the router point-of-view, a pointer which goes from 0 to N-1 counts the sample events. When this counter wraps the internal ping/pong flag is and the IRDY flag is raised. If the IRDY flag was already set, a computation the ERR overflow flag is set.
When the ARM is done processing the incoming data and has written the outgoing data it writes to the IRDY bit in the AIO_CLR register.

Processing time available:
Buffers are posted based on the sample rate and depth. If Fs is the rate then the time between events will be depth/Fs less synchronization time which is insignificant.

The AIO is addressed through 2 base addresses:

Table 28.1 AIO base addresses

Base address	Register name	Description
0xC4000400	DICE3_AIO_REG	AIO Registers
0x50009000	DICE3_AIO_BUF	AIO Audio Buffers

Table 28.2 AIO Buffer offsets summary

Base address	Register name	Description
0x0000	DICE3_AIO_RX_BUF	ARM CPU Reads
0x0200	DICE3_AIO_TX_BUF	ARM CPU Writes

Table 28.3 AIO Register summary

Address Offset	Register	Description
0x0000	HAL_DICE3_AIO_CSR	*AIO CSR Register*
0x0004	HAL_DICE3_AIO_CLR	*AIO CLR Register*
0x0008	HAL_DICE3_AIO_TIME	*AIO Time Register*

28.1.1 Router AIO CSR Register – HAL_DICE3_AIO_CSR

Address offset: 0x0000 HAL_DICE3_AIO_CSR

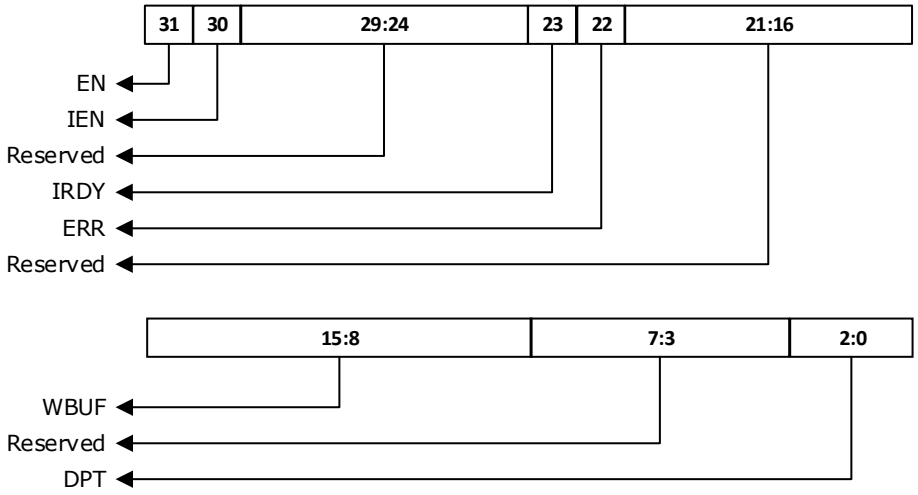

Table 28.4 Router AIO CSR Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	RW	Set to enable the engine. Enable the engine, when disabled no interrupt is generated and no RAM access is performed.
IEN	30	0	RW	Enable interrupt on IRDY status.
Reserved	29:24	0	N/A	Reserved

Name	Bit	Reset	Dir	Description
IRDY	23	0	R	Read only. A new buffer set is available. The ARM CPU must process and clear IRDY before the next buffer is posted including clock domain crossing time. Clear this status bit using the AIO CLR register.
ERR	22	0	R	Set if a new buffer is ready before the previous has been acknowledged by the CPU. Clear this status bit using the AIO CLR register.
Reserved	21:16	0	N/A	Reserved
WBUF	15:8	0	R	Read only. The constant used for this IP Core instantiation, enables firmware to adapt.
Reserved	7:3	0	N/A	Reserved
DPT	2:0	0	RW	This is encoded as 0=2, 1=4, 2=8, 3=16, 4=32 all other values are reserved.

28.1.1.1 DPT Example: WBUF = 7

Table 28.5 DPT Example - channels vs. number of samples

DPT	depth	channels	elements / buf	RAM (Rx and Tx)
0	2	64	128	256
1	4	32	128	256
2	8	16	128	256
3	16	8	128	256
4	32	4	128	256

28.1.2 Router AIO Clear Register – HAL_DICE3_AIO_CLR

Address offset: 0x0004 HAL_DICE3_AIO_CLR

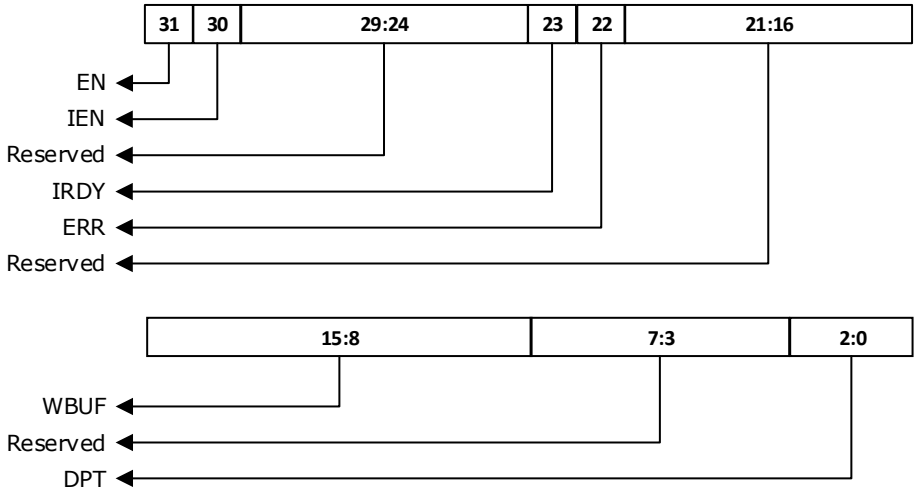

Table 28.6 Router AIO Clear Register bit assignments

Name	Bit	Reset	Dir	Description
EN	31	0	R	Read only. Set if the engine is enabled.
IEN	30	0	R	Read only. Set if interrupt on IRDY is enabled.
Reserved	29:24	0	N/A	Reserved
IRDY	23	0	W	Write 1 to clear the corresponding status bit in the AIO CSR register.
ERR	22	0	W	Write 1 to clear the corresponding status bit in the AIO CSR register
Reserved	21:16	0	N/A	Reserved
WBUF	15:8	0	R	Read only. The constant used for this IP Core instantiation, enables firmware to adapt.
Reserved	7:3	0	N/A	Reserved
DPT	2:0	0	R	Read only.

28.1.3 Router AIO Time Register – HAL_DICE3_AIO_TIME

Address offset: 0x0008 HAL_DICE3_AIO_TIME

This register contains the RTC time of the first sample in the buffer. The RTC is part of the AVB sub system.

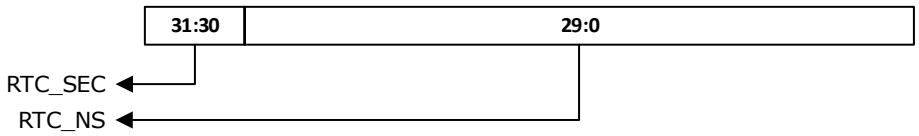

Table 28.7 Router AIO Time Register bit assignments

Name	Bit	Reset	Dir	Description
RTC_SEC	31:30	0	R	Real time counter seconds
RTC_NS	20:0	0	R	Real time counter nanoseconds

28.2 Revisions

Table 28.8 Document revision history

Date	Rev.	By	Change
May 6, 2015	0.9.0-41360	BK	Initial publication

