Bharatiya Vidya Bhavan's
**Sardar Patel Institute of Technology**
Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058-India
(Autonomous College Affiliated to University of Mumbai)

**Academic Year:** 2020-2021

# OCULUS-2021 SHORT CIRCUIT EVENT

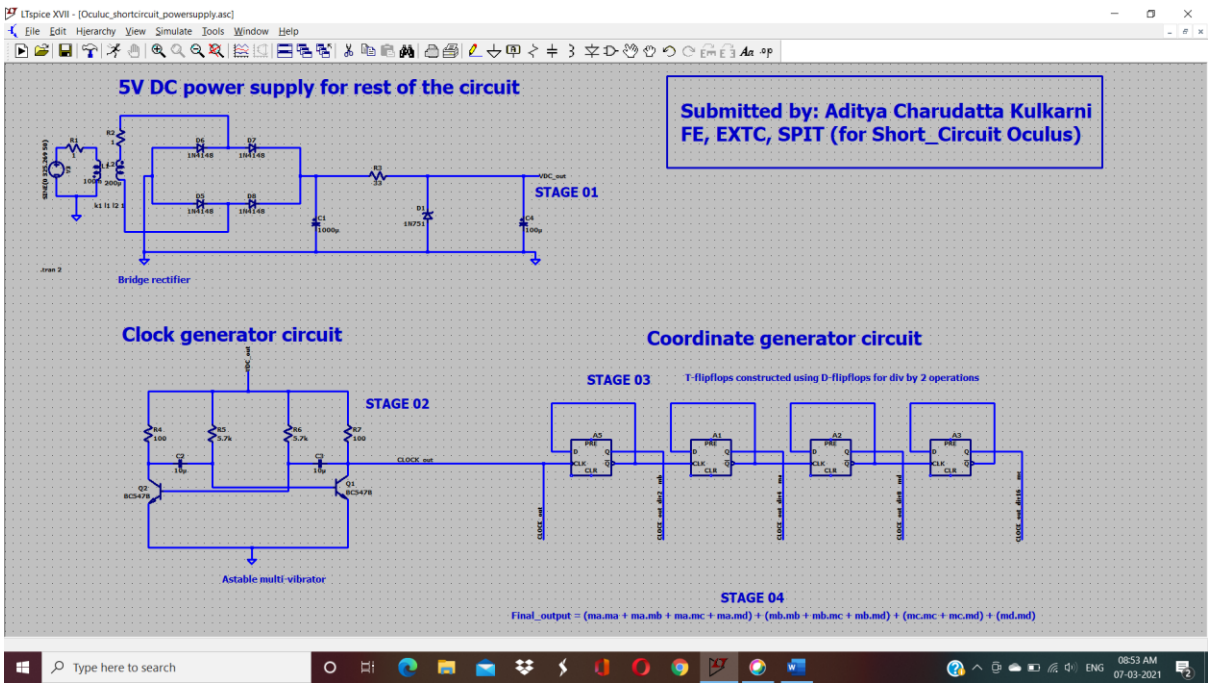
**Team name** : **Aditya Kulkarni (Solo participation)**
**Submitted by** : **Aditya Charudatta Kulkarni**
**UCID** : **2020200037**
**Class** : **FE**
**Branch** : **EXTC**

## Problem Statement:

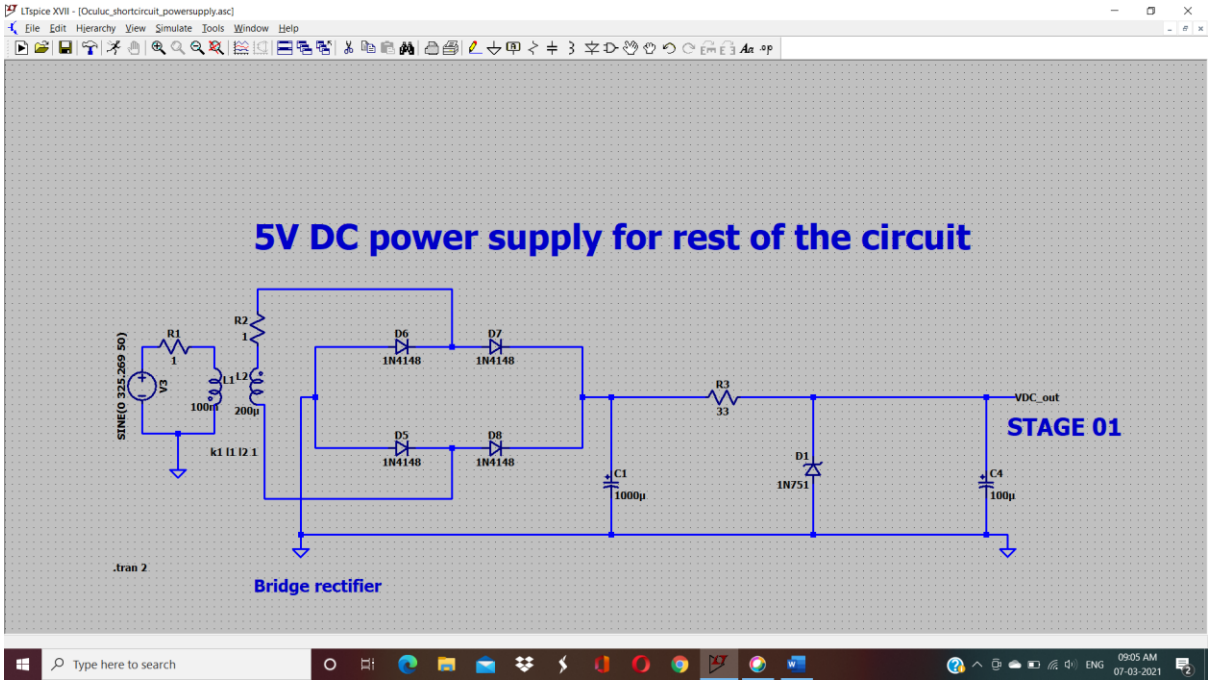
Mr. Arnab is a huge fan of mathematics, especially matrices. He believes that Upper Triangular Matrices can generate interesting results. He decides to test his theory using some electronic components. Help Arnab to design a circuit such that the final output remains high when the input co-ordinates are a part of a 4x4 upper triangular matrix.

**Circuit development:**

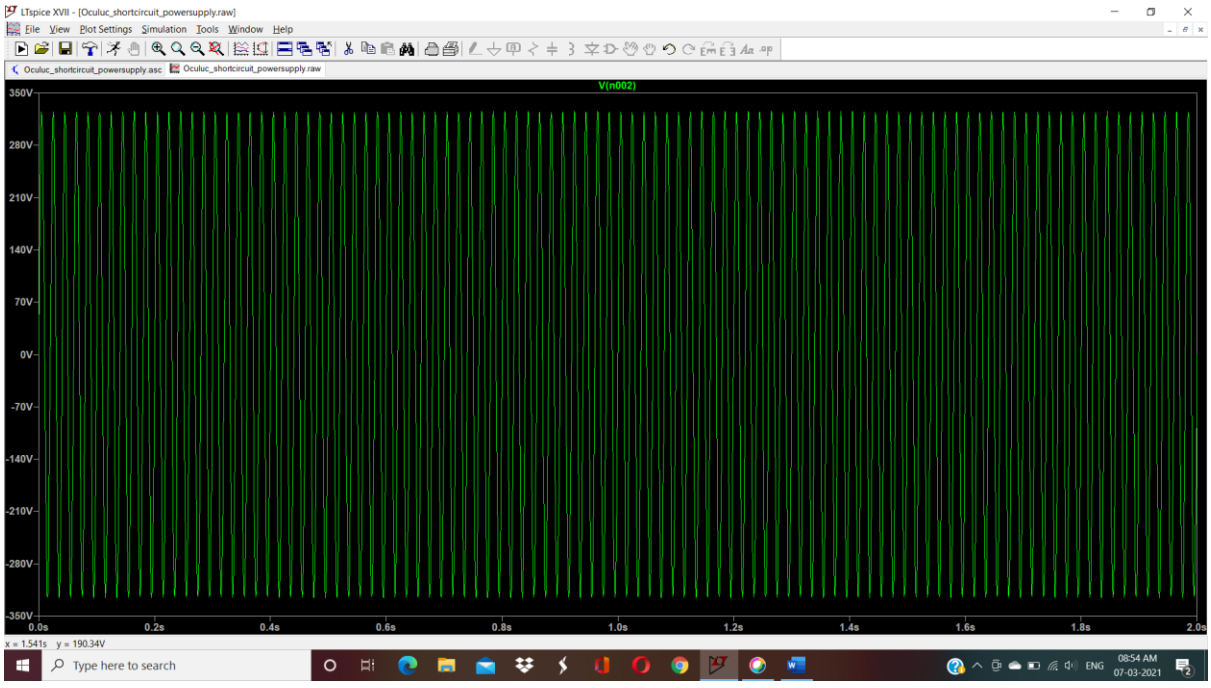
I have prepared the circuit using LTSpice package as following:



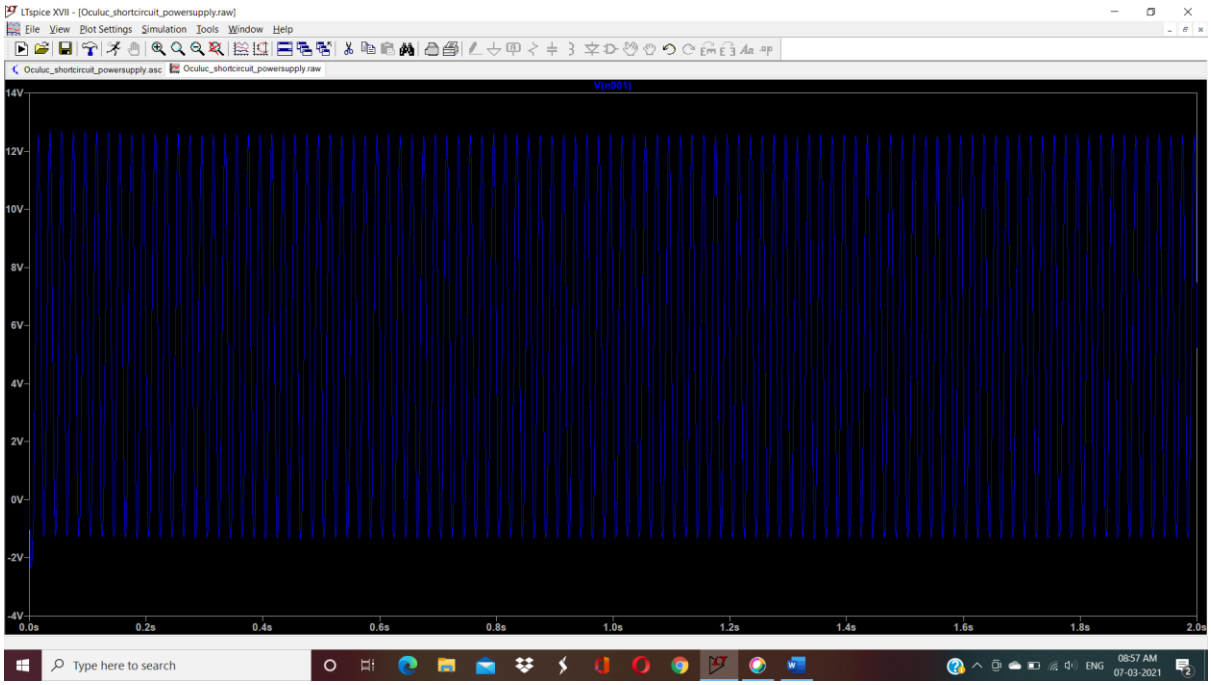
## STAGE-01: (AC-DC)



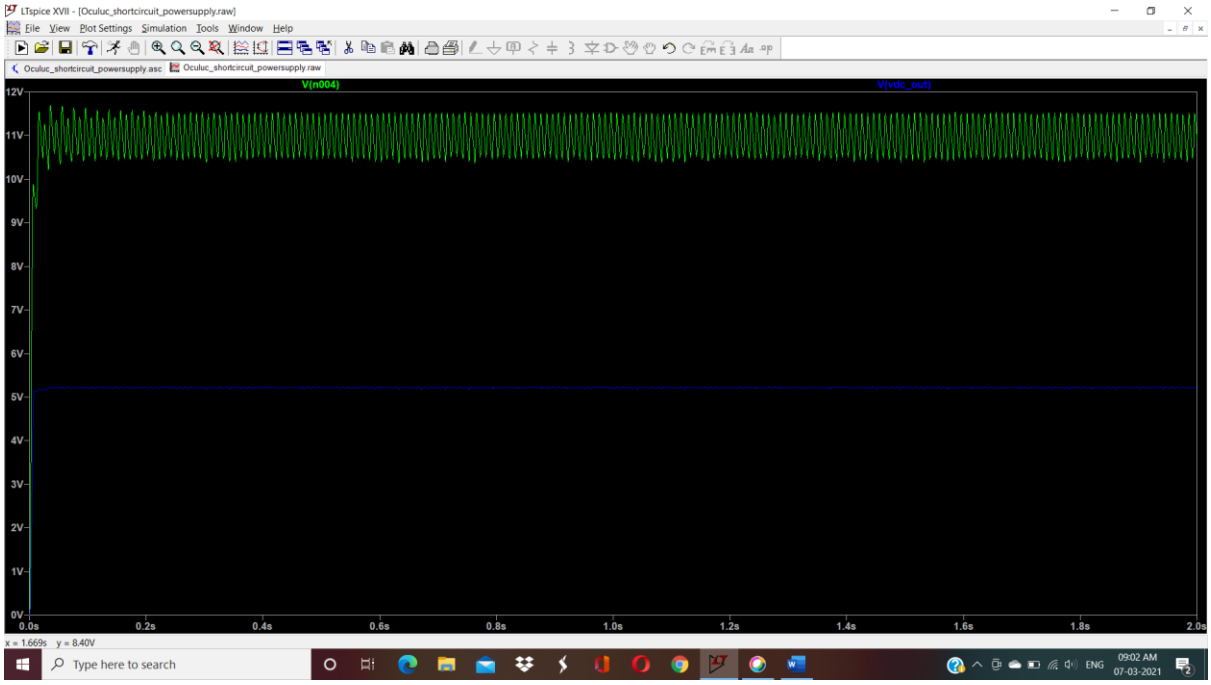

Mains 230Vrms AC supply input:



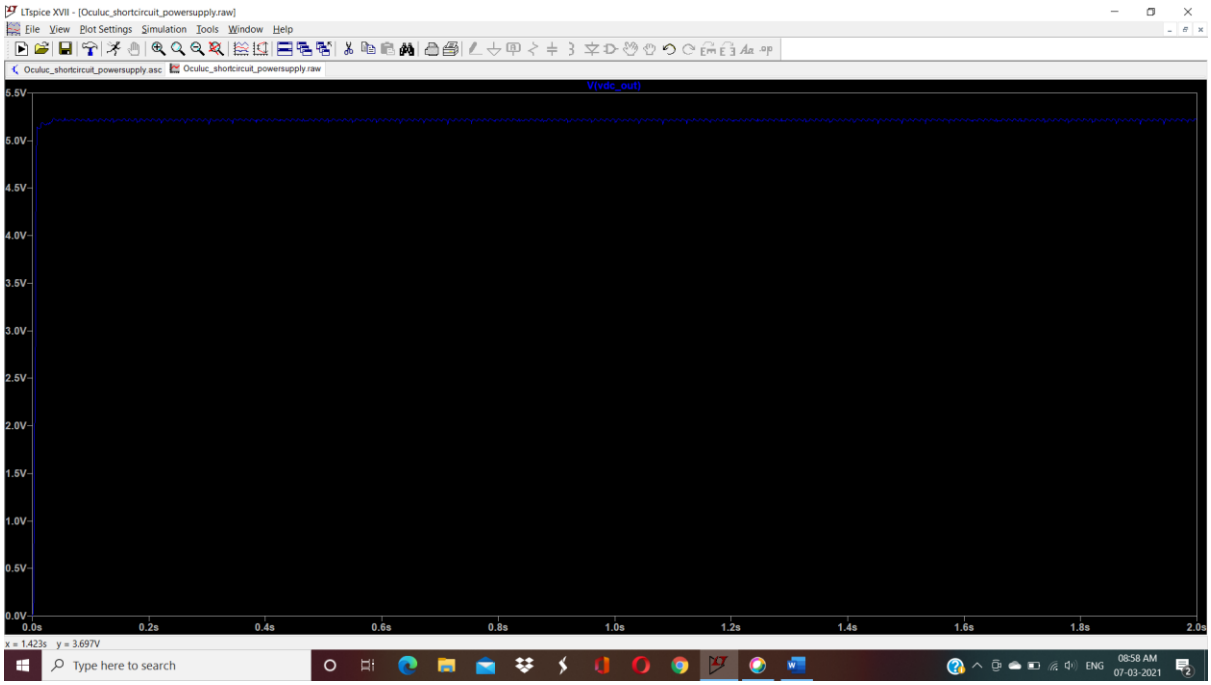
9Vrms AC output after step-down transformer:



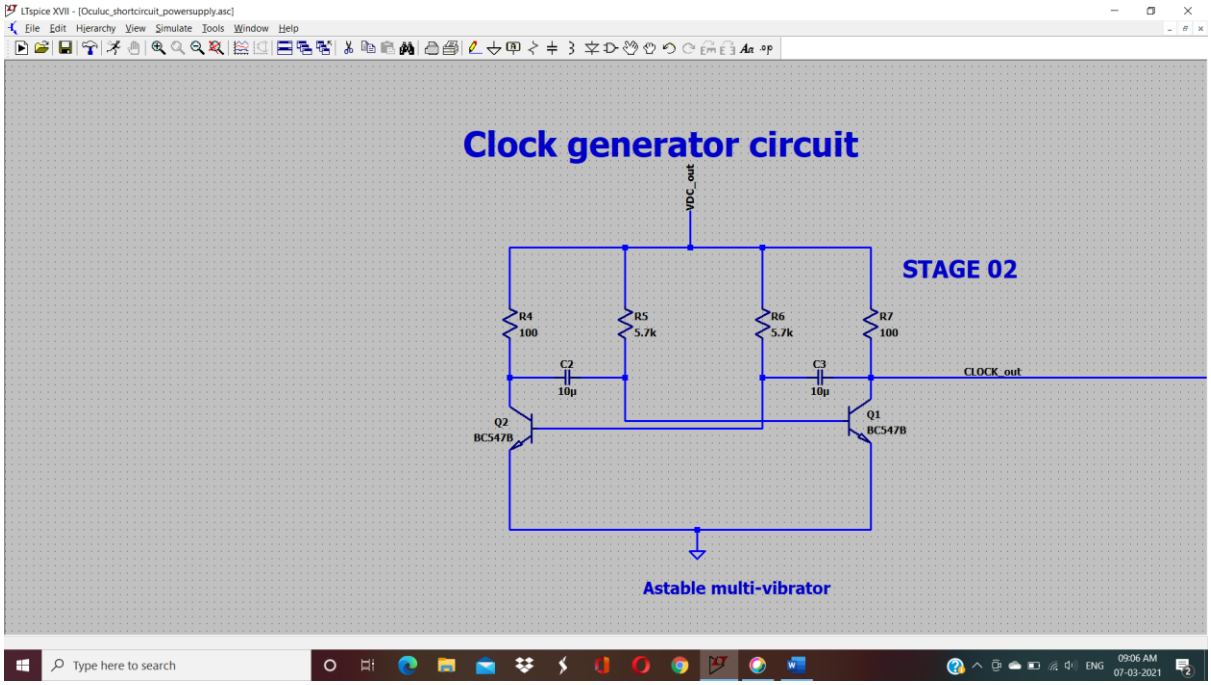

5VDC output after rectification, filter and regulation using zener diode:



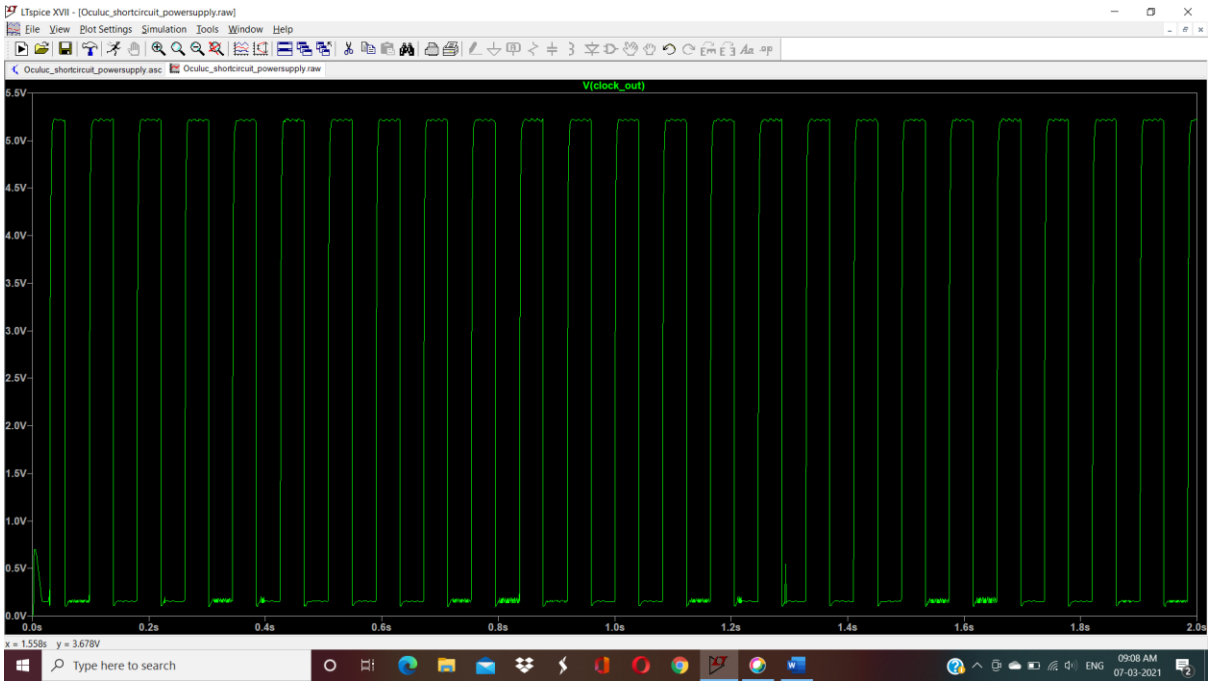
Stage-01 Final output:



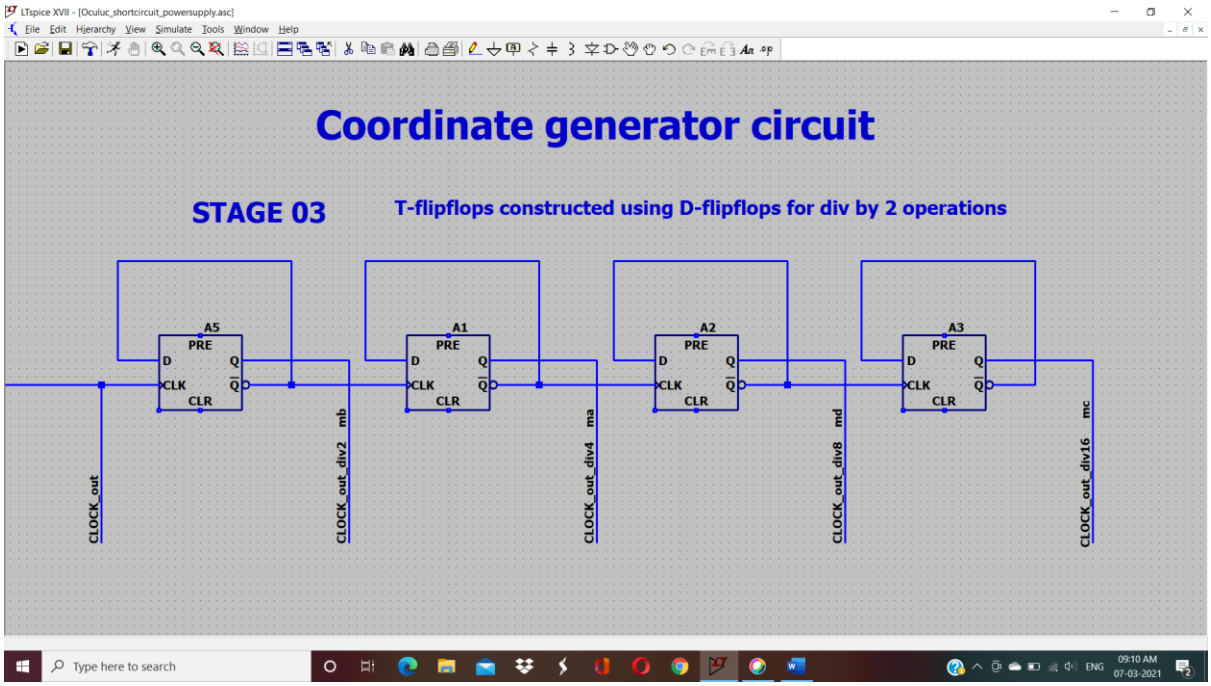

## STAGE-02: (Clock generator)



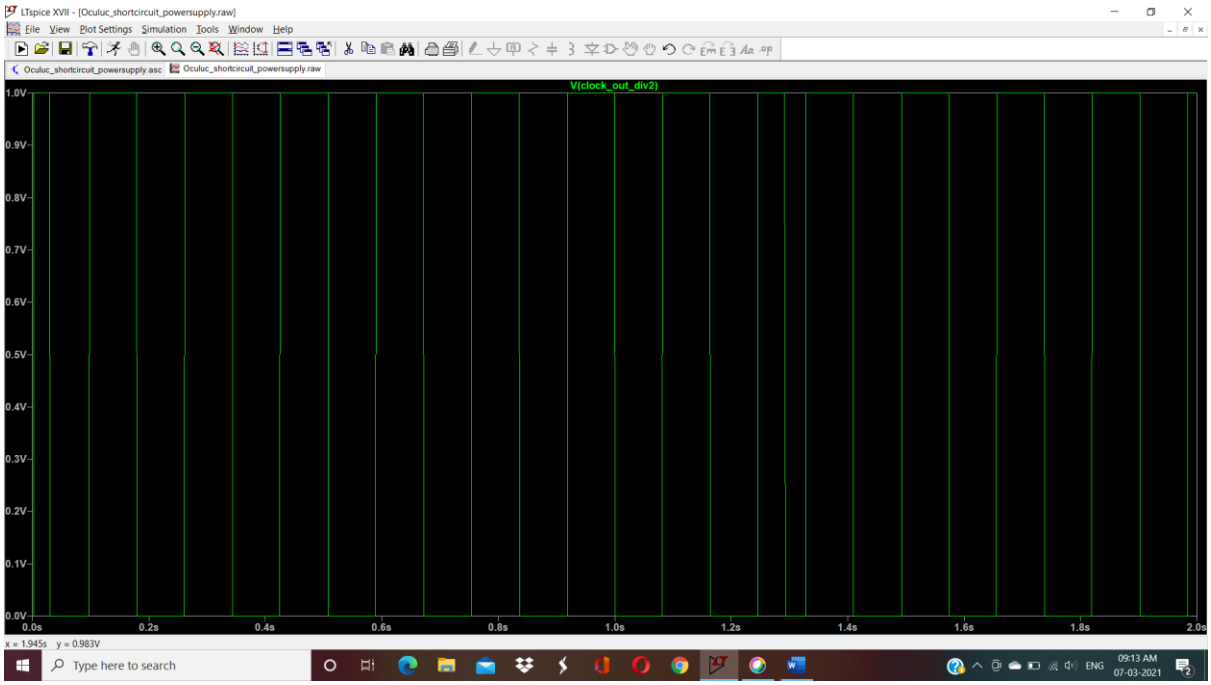
Stage-02 Final output: (CLOCK_out)



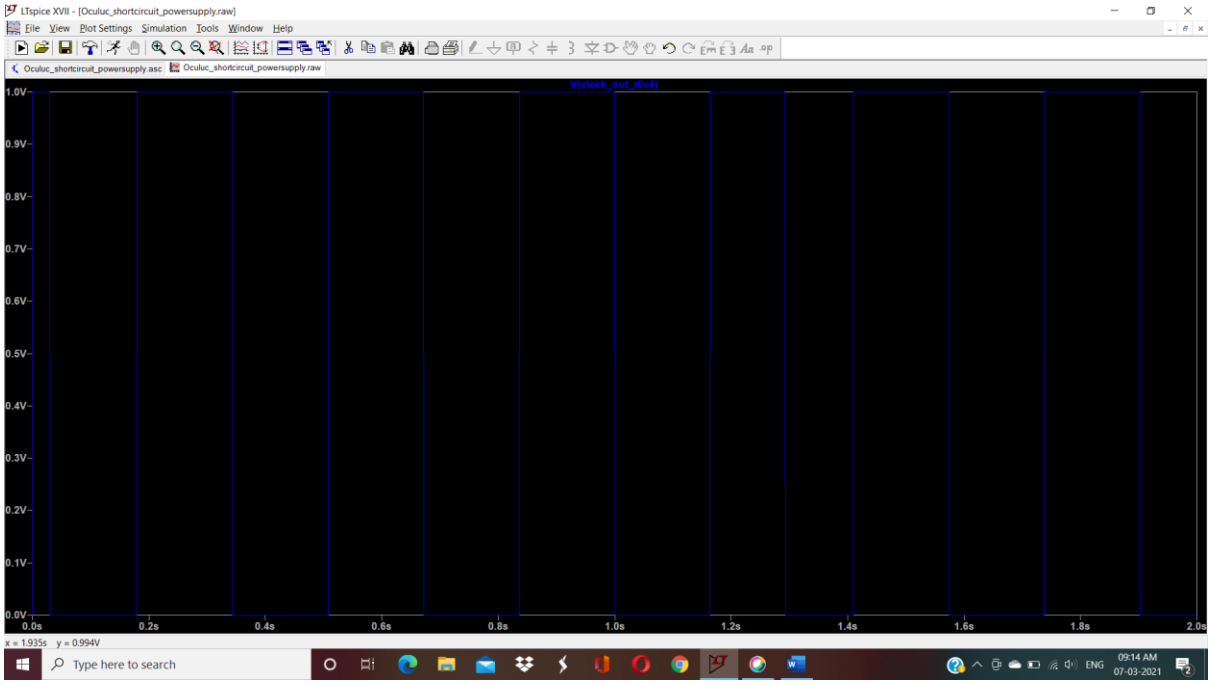

## STAGE-03: (Co-ordinate generator)



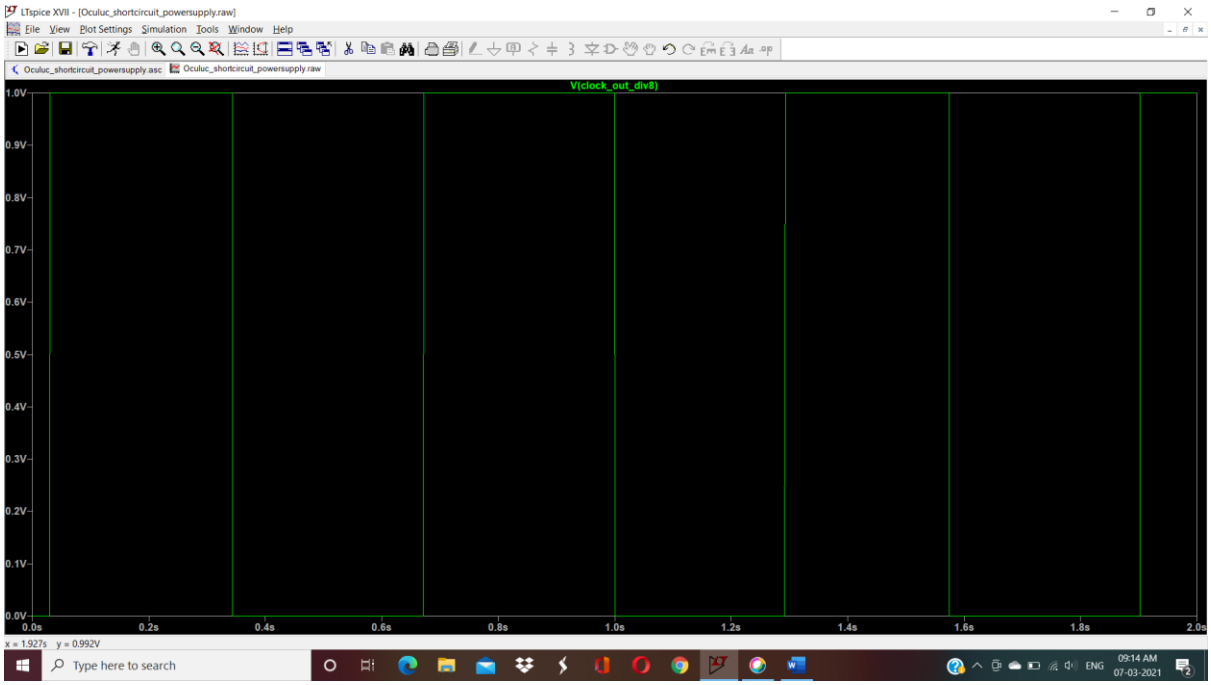
Stage-03  output: (CLOCK_out_div2, also named as mb)



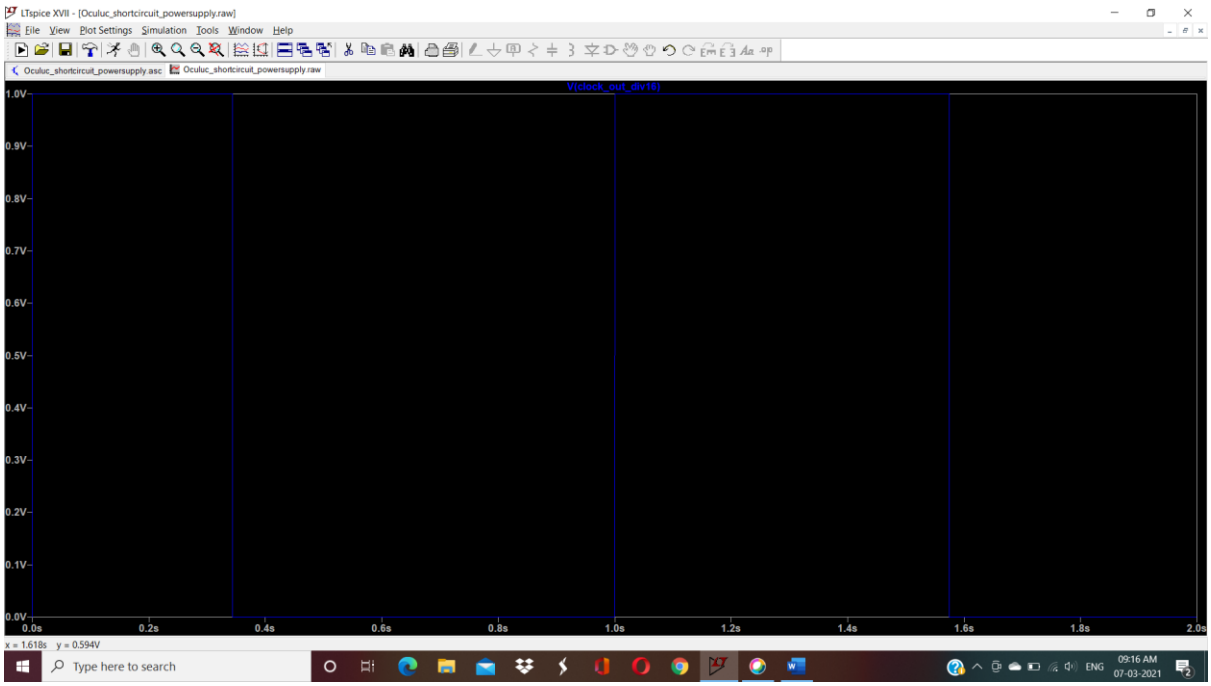

Stage-03  output: (CLOCK_out_div4, also named as ma)



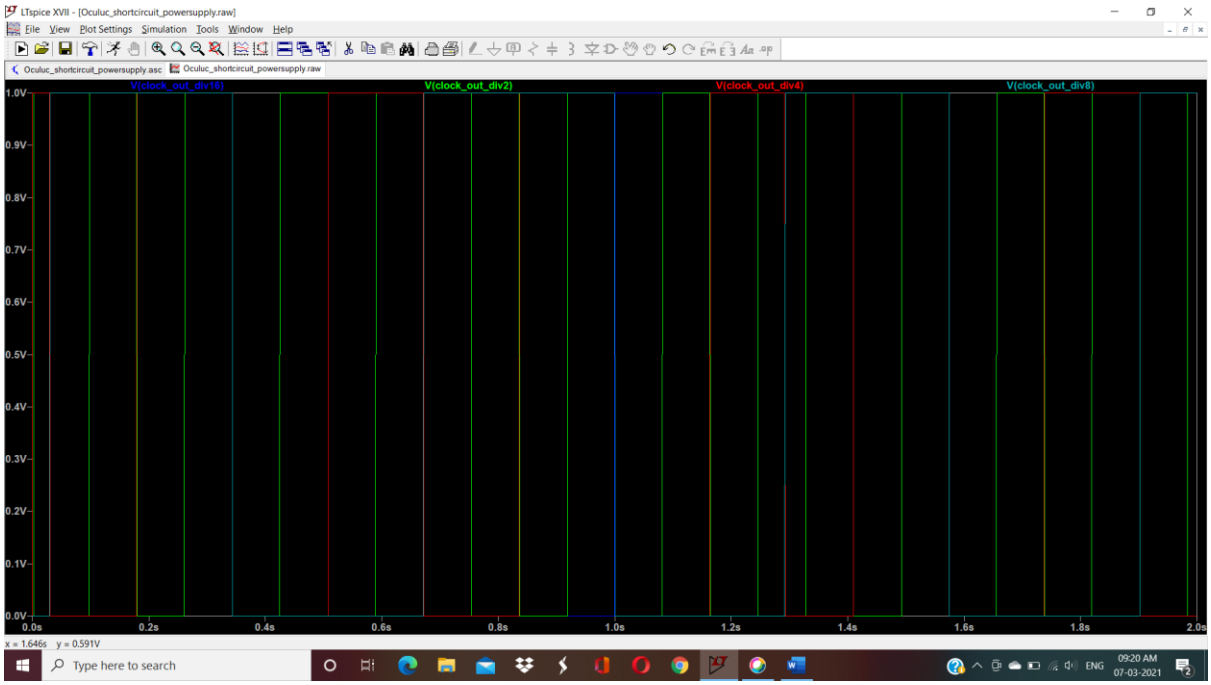
Stage-03  output: (CLOCK_out_div8, also named as md)



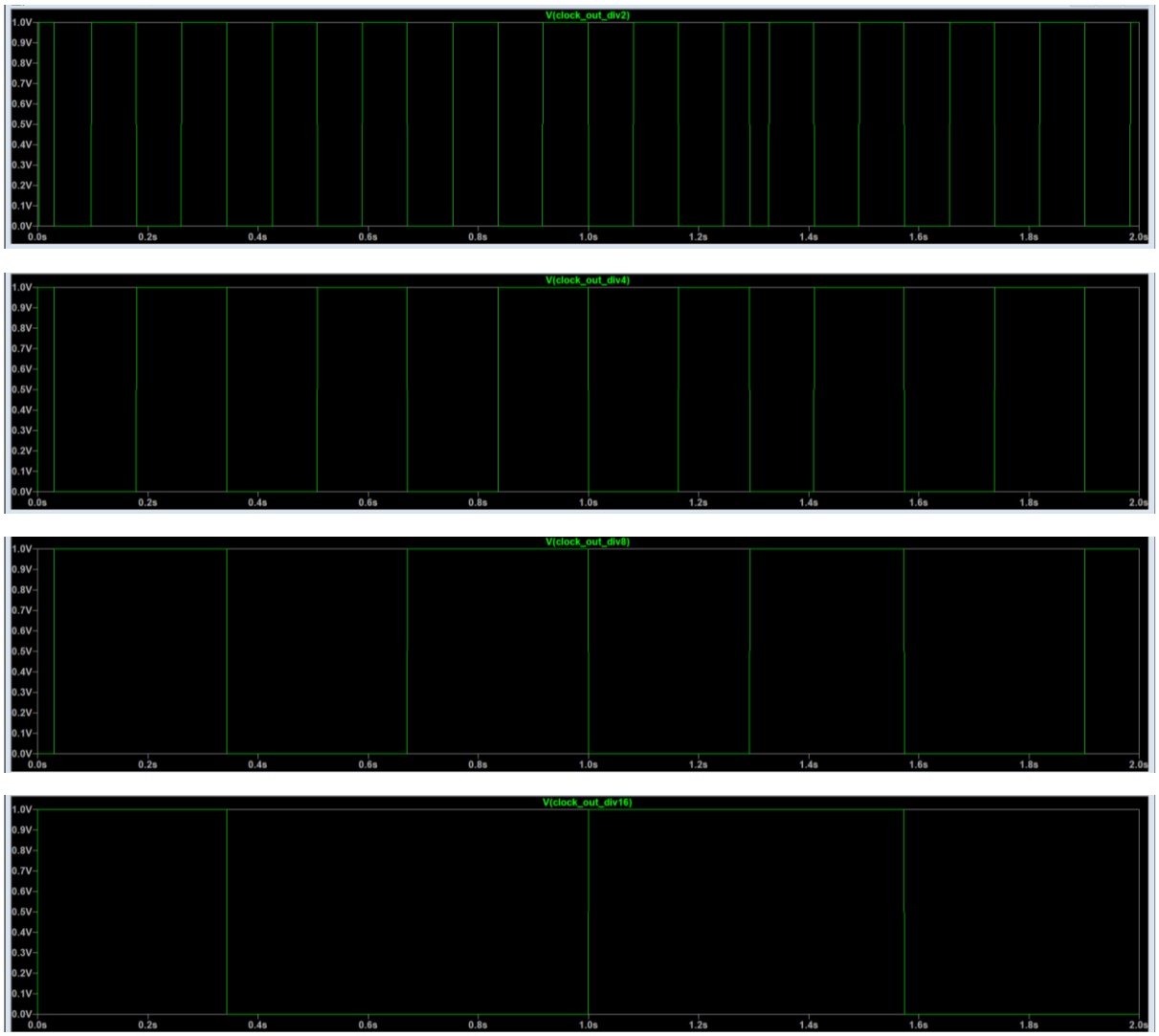

Stage-03  output: (CLOCK_out_div16, also named as mc)



Stage-03 Combined outputs: (mb, ma, md, mc as per the sequence given in problem data)

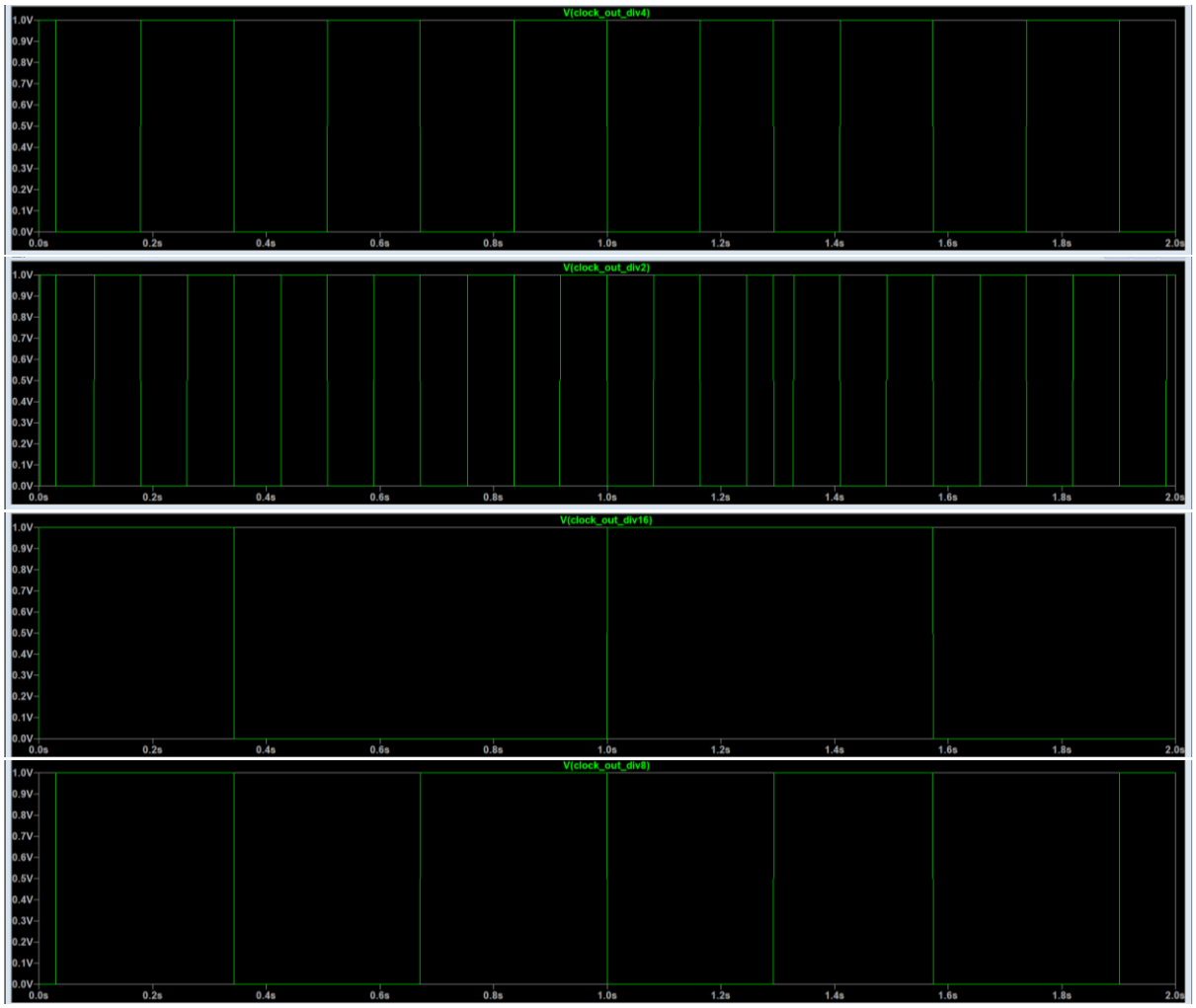


Stage-03 Combined view of 4 outputs: (as per the natural sequence)




Below is Stage-03 Combined view of 4 outputs: (**as per the sequence given in problem data**)

# FINAL OUTPUTS



**Calculations:**

1. Selection of transformer:

N1/N2 = ~ 23 such that input is 230 Vac to output as 10Vac

(N1/N2) ^2 = L1/L2 = V1/V2 = I2/I1

Primary L1 is 100 mH and secondary L2 is 200uH

2. Selection of filter capacitor:

C = I/(2 x f x Vpp)

To get min ripple, 1000uF capacitor is selected

3. Selection of zener:

Available 5V Zener is used.

Rs = (Vin – Vz) / (Iz + IL) = (12 - 5) / (100 + 50) = ~33 ohm

4. Selection of astable multivibrator timing:

T = 0.69RC

So C=10 uF and R=5.7K selected. R = 4.7K + 1K as available in component available.

T = ~ 40ms on time.

So 2T = ~80 ms

Thus 80 ms timing wave as per problem image is generated.

5. Selection of frequency divider stages:

Available DFF is used to create Toggle FF and 4 such stages made.

This give div_by_2, div_by_4, div_by_8, and div_by_16 waveforms

Final output 4x4 upper triangular matrix output was not created. However an equation is written as per my best understanding.

## Learnings from the problem statement:

1. Learned to use LTSpice in detail

2. To design transformer

3. To design rectifier

4. To design Zener regulator

5. To design astable mv clock generator

6. To make DFF to TFF for clock division

7. To analyze waveforms

8. General interactions and auctions etc.

I thank all the organizers of short circuit theme and Oculus program.

# THANKS…