

KCU116 PCIe Design Creation

May 2019



XTP462

Revision History

Date	Version	Description
05/29/19	8.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	7.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	6.0	Updated for 2018.2.
04/09/18	5.0	Updated for 2018.1.
12/20/17	4.0	Updated for 2017.4.
10/26/17	3.0	Updated for 2017.3.1.
06/20/17	2.0	Updated for 2017.2.
04/19/17	1.0	Initial version.

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- > Kintex UltraScale PCIe x8 Gen 3 Capability
- > Xilinx KCU116 Board
- > KCU116 Software Install and Board Setup
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- > Generate x8 Gen 3 PCIe Core
 - » Modify PCIe Core
 - » Compile Example Design
 - » Generate PCIe MCS File
 - » Program SPI Flash with PCIe Design
- > Running the PCIe x8 Gen 3 Design
- > References

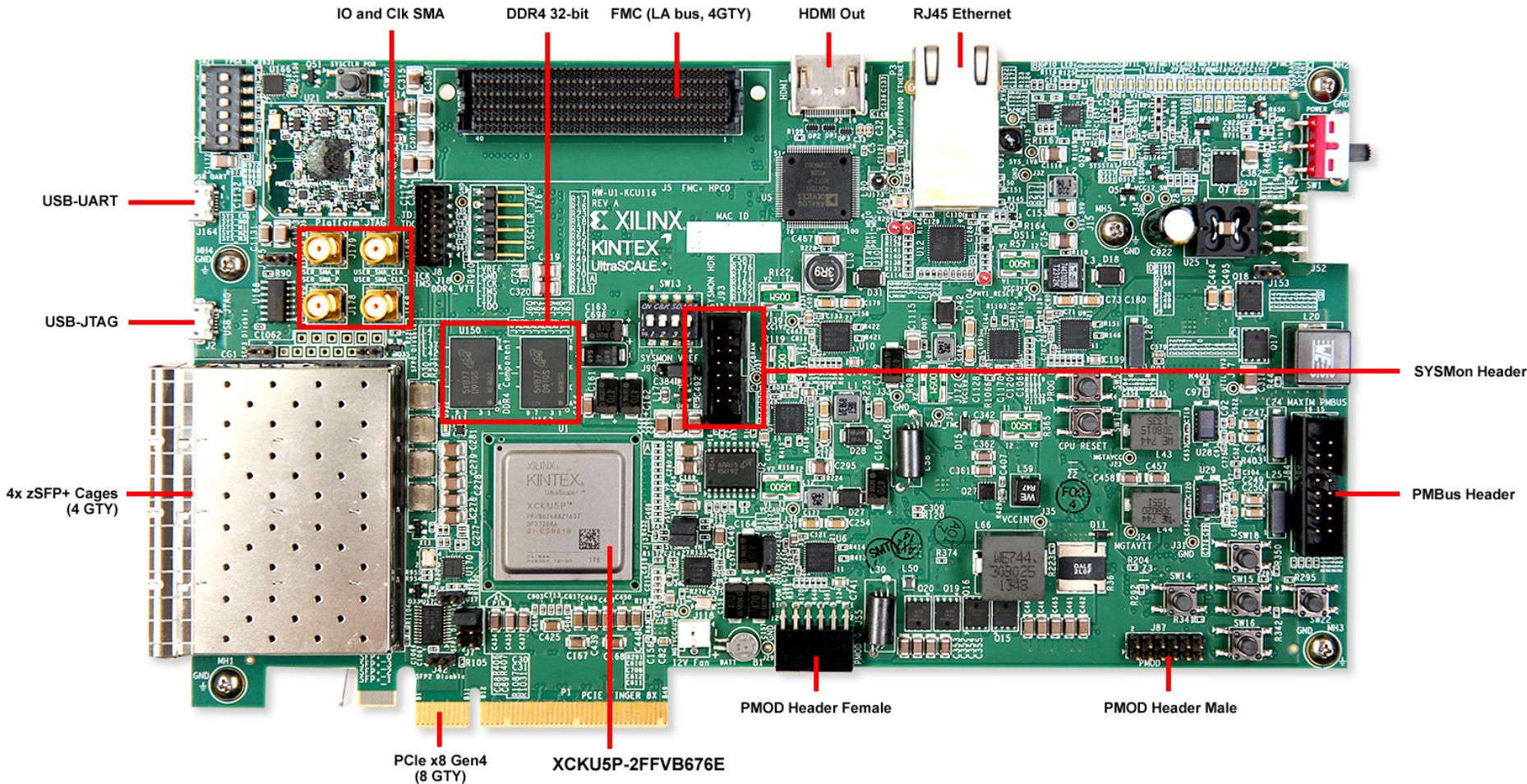
Kintex UltraScale PCIe x8 Gen 3 Capability

- > **KCU116 Supports PCIe Gen 1, Gen 2, and Gen 3 Capability**
 - » x8, x4, x2, or x1 in Gen 1, Gen 2, and Gen 3 lane widths
 - » See [DS922](#) for details
- > **LogiCORE PIO Example Design**
 - » RDF0412 - KCU116 PCIe Design Files (2019.1 C) ZIP file
- > **UltraScale Integrated Block for PCI Express**
 - » See [PG213](#) for details

Kintex UltraScale PCIe x8 Gen 3 Capability

- > **Integrated Block for PCI Express**
 - » PCI Express 3.0 Specification
- > **Configurable for Endpoint or Root Port Applications**
 - » KCU116 configured for Endpoint Applications
- > **GTH Transceivers implement a fully compliant PHY**
- > **Large range of maximum payload size**
 - » 128 / 256 / 512 / 1024 bytes
- > **Configurable BAR spaces**
 - » Up to 6 x 32 bit, 3 x 64 bit, or a combination
 - » Memory or IO
 - » BAR and ID filtering
- > **Management and Statistics Interface**

Xilinx KCU116 Board



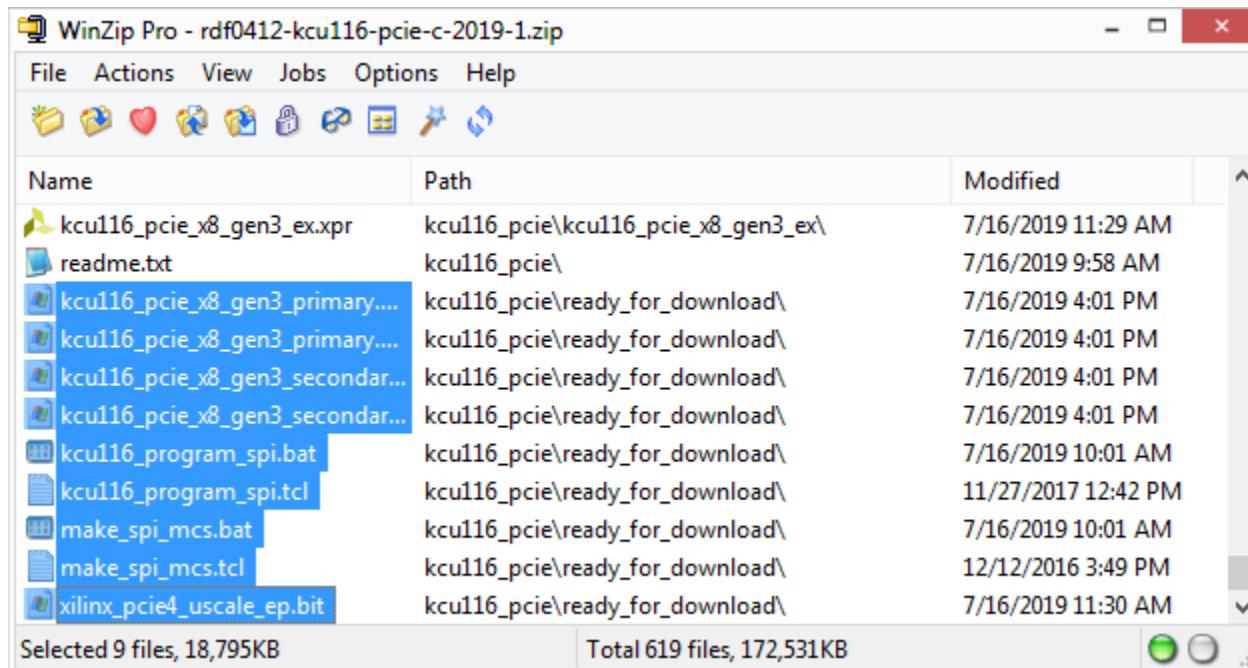
KCU116 Software Install and Board Setup

- > Refer to XTP464 – KCU116 Software Install and Board Setup for details on:
 - » Software Requirements
 - » KCU116 Board Setup



Files needed for PCIe design

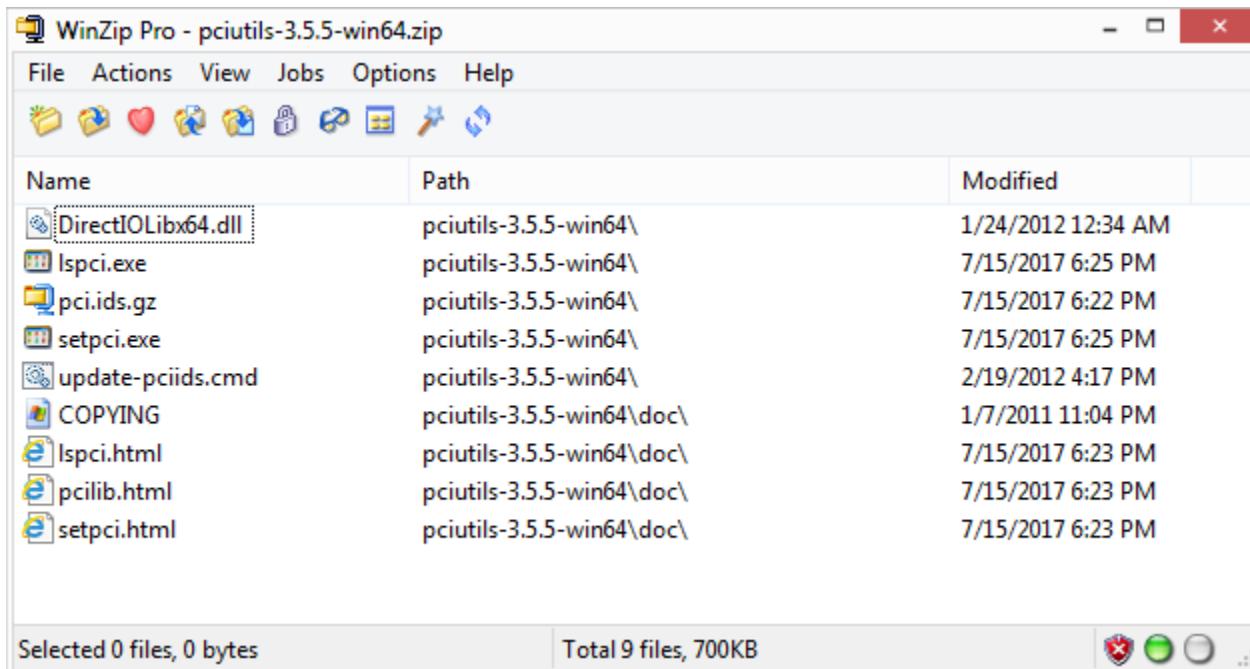
- > Open the KCU116 PCIe Design Files (2019.1 C) ZIP file, and extract these files to your C:\ drive:
 - » kcu116_PCIE\ready_for_download*



Ispci Software Requirement

> Ispci for Windows

- » Free [download](#)
- » Unzip to the C:\ drive of the test PC



Generate x8 Gen 3 PCIe Core

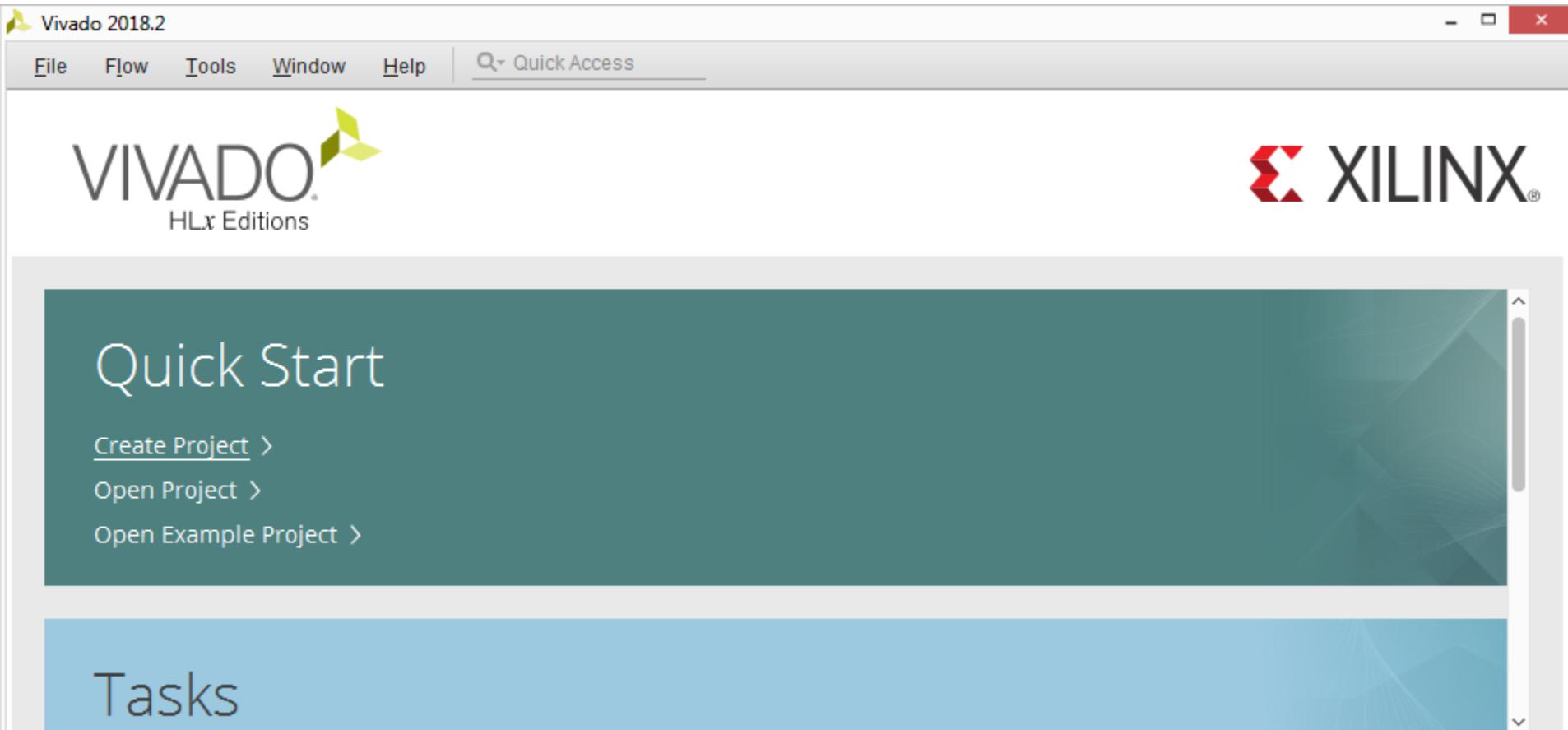


Generate x8 Gen 3 PCIe Core

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Create Project



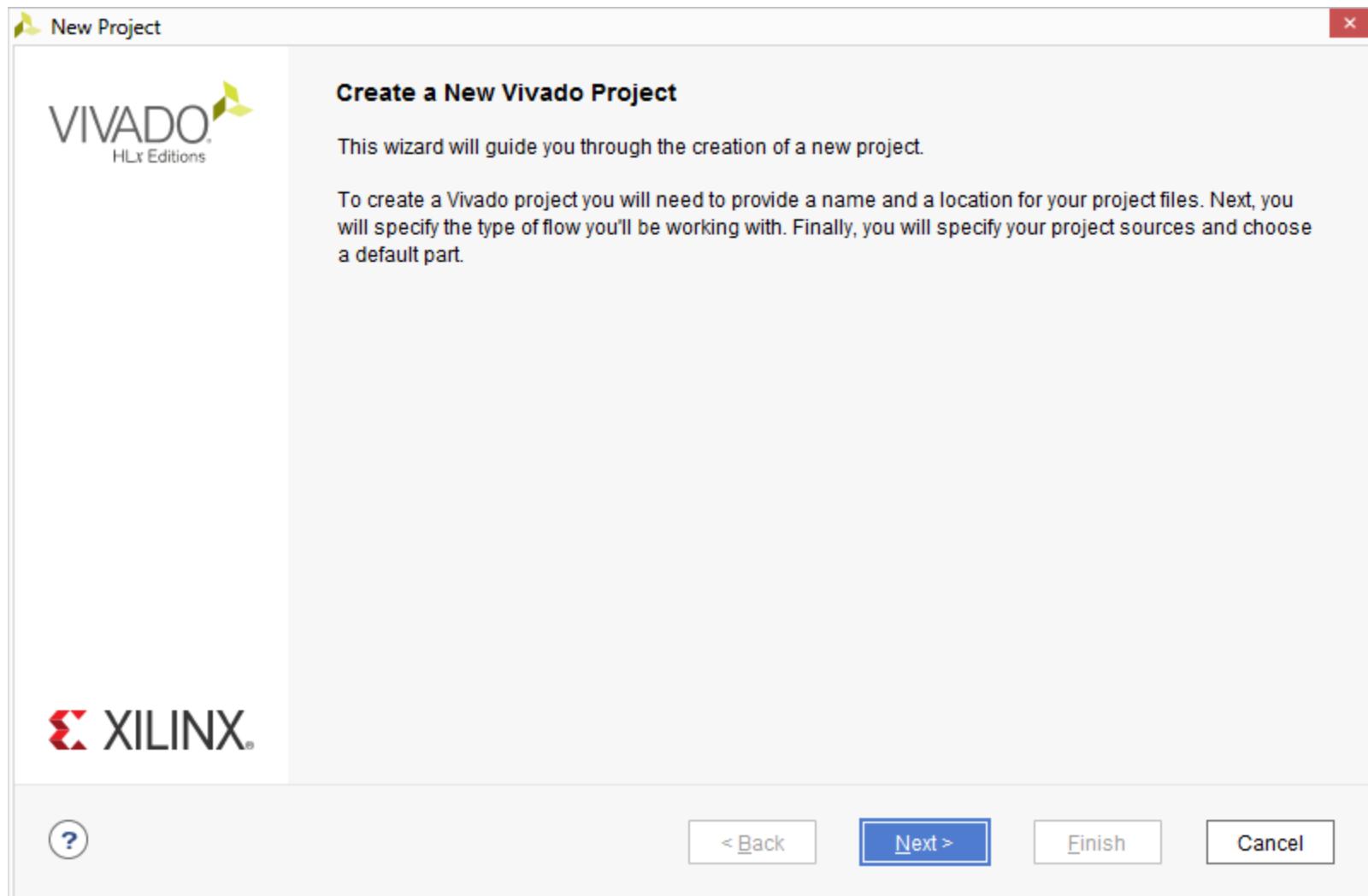
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the KCU116

XILINX

Generate x8 Gen 3 PCIe Core

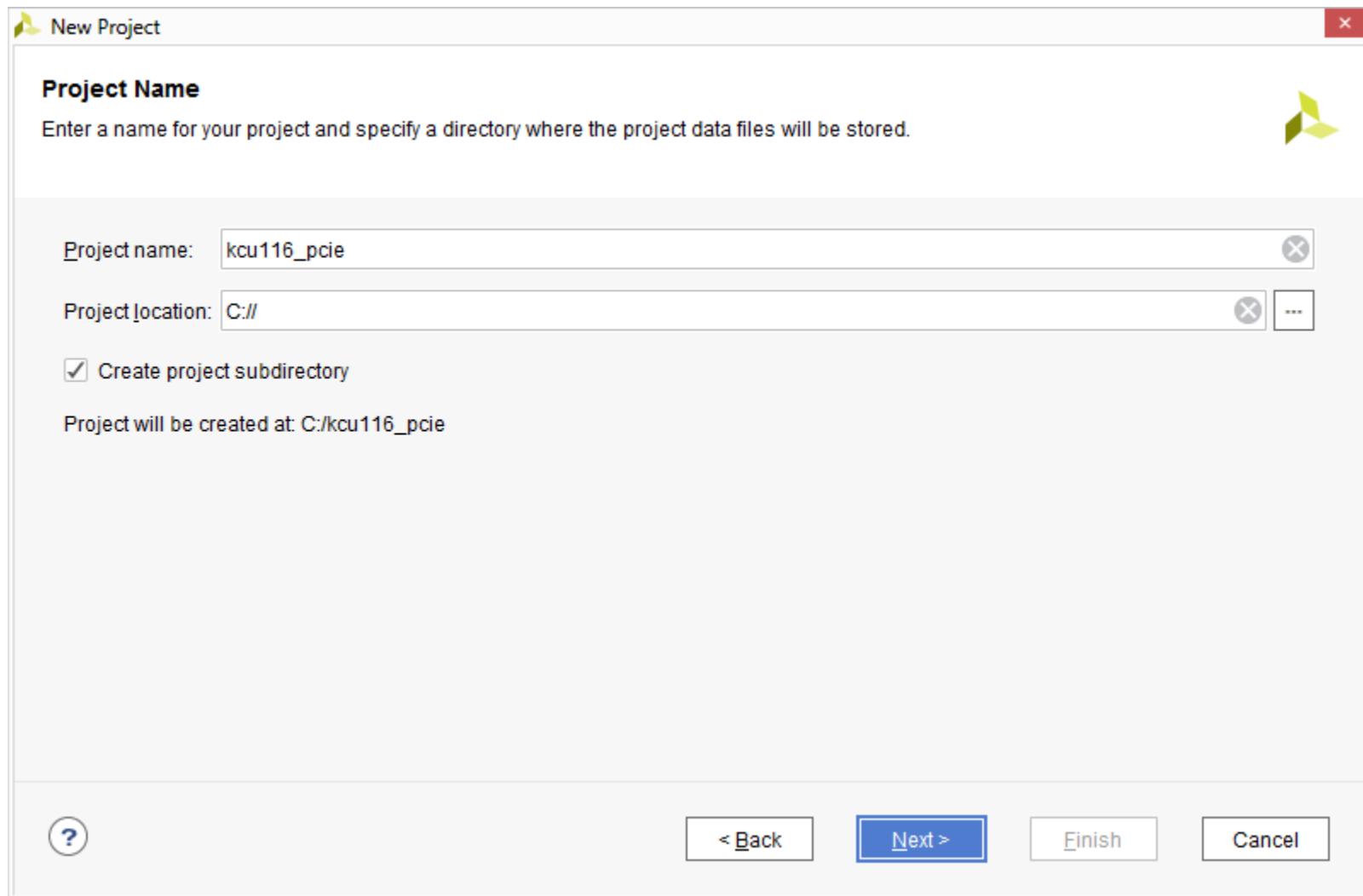
> Click Next



Generate x8 Gen 3 PCIe Core

- > Set the Project name and location to kcu116_PCIE and C:/

- » Check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Generate x8 Gen 3 PCIe Core

> Select RTL Project

» Select Do not specify sources at this time

New Project X

Project Type
Specify the type of project to create.

RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Generate x8 Gen 3 PCIe Core

> Select the KCU116 Evaluation Platform

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	F
Kintex UltraScale+ KCU116 Evaluation Platform Add Daughter Card Connections		xilinx.com	1
Kintex UltraScale KCU1500 Acceleration Development Board		xilinx.com	1

< >

?

< Back

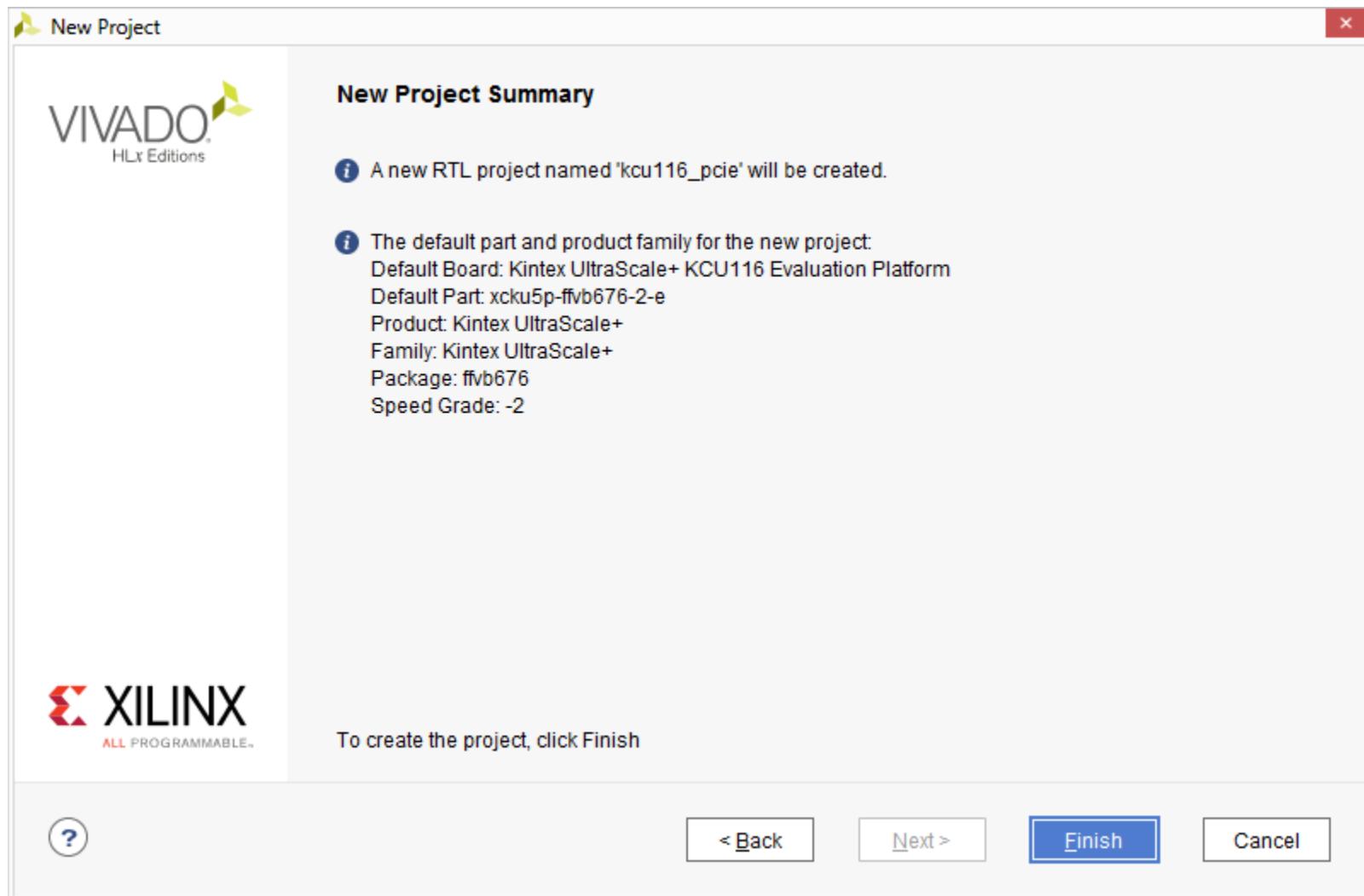
Next >

Finish

Cancel

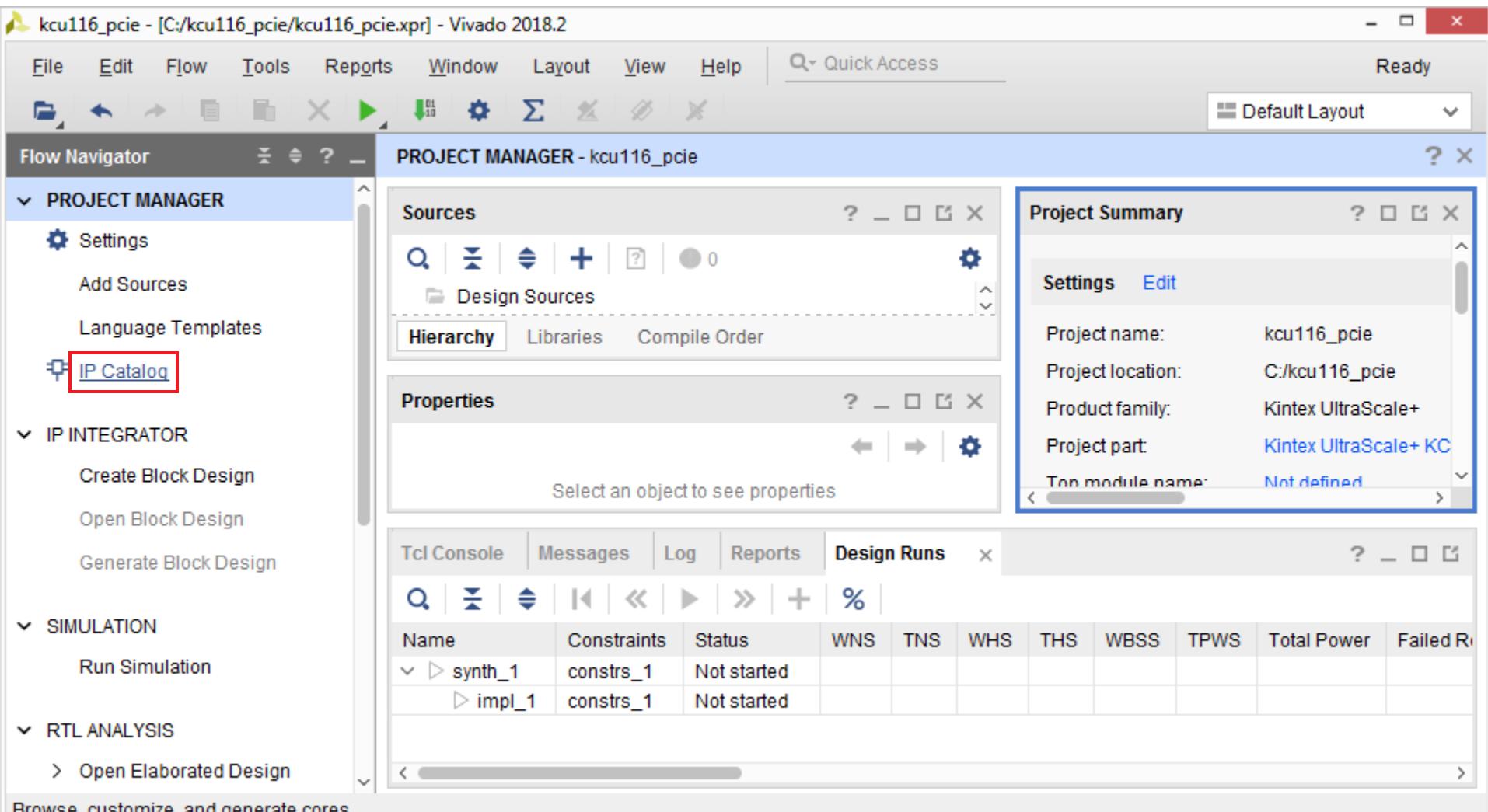
Generate x8 Gen 3 PCIe Core

> Click Finish



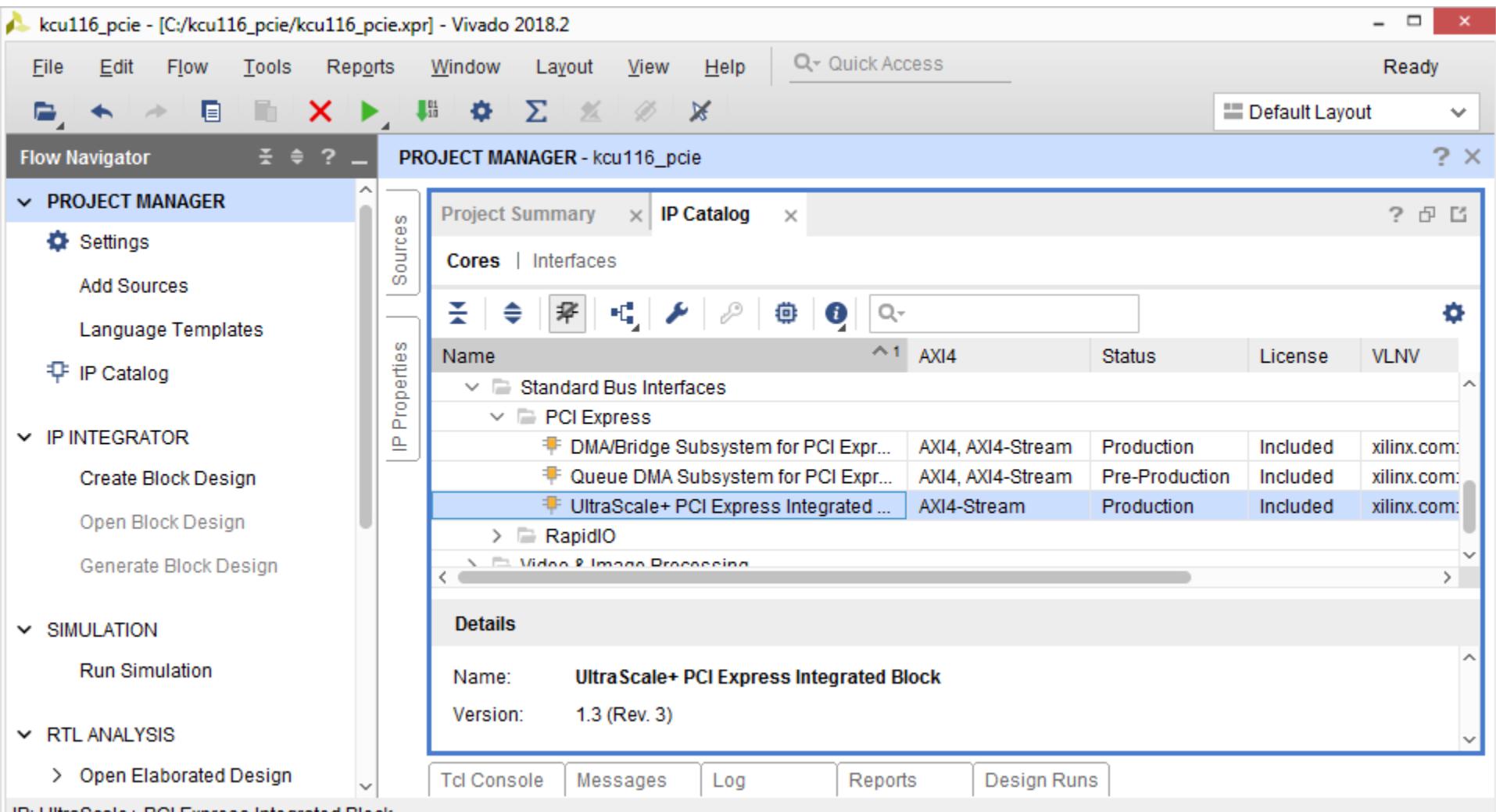
Generate x8 Gen 3 PCIe Core

> Click on IP Catalog



Generate x8 Gen 3 PCIe Core

- > Select UltraScale+ PCI Express Integrated Block, v1.3 under Standard Bus Interfaces

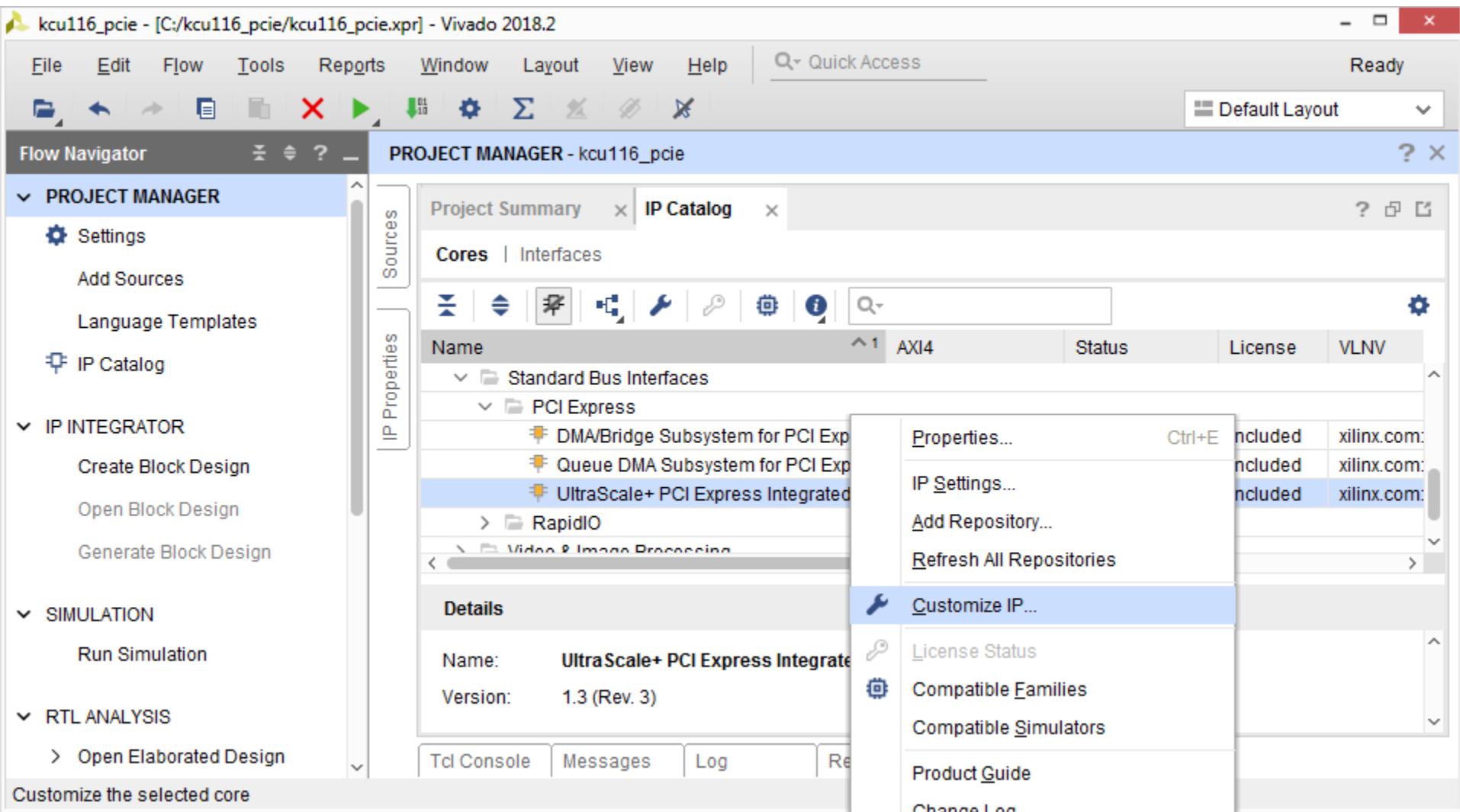


Note: Presentation applies to the KCU116

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Generate x8 Gen 3 PCIe Core

- > Right click on UltraScale+ PCI Express Integrated Block and select Customize IP...

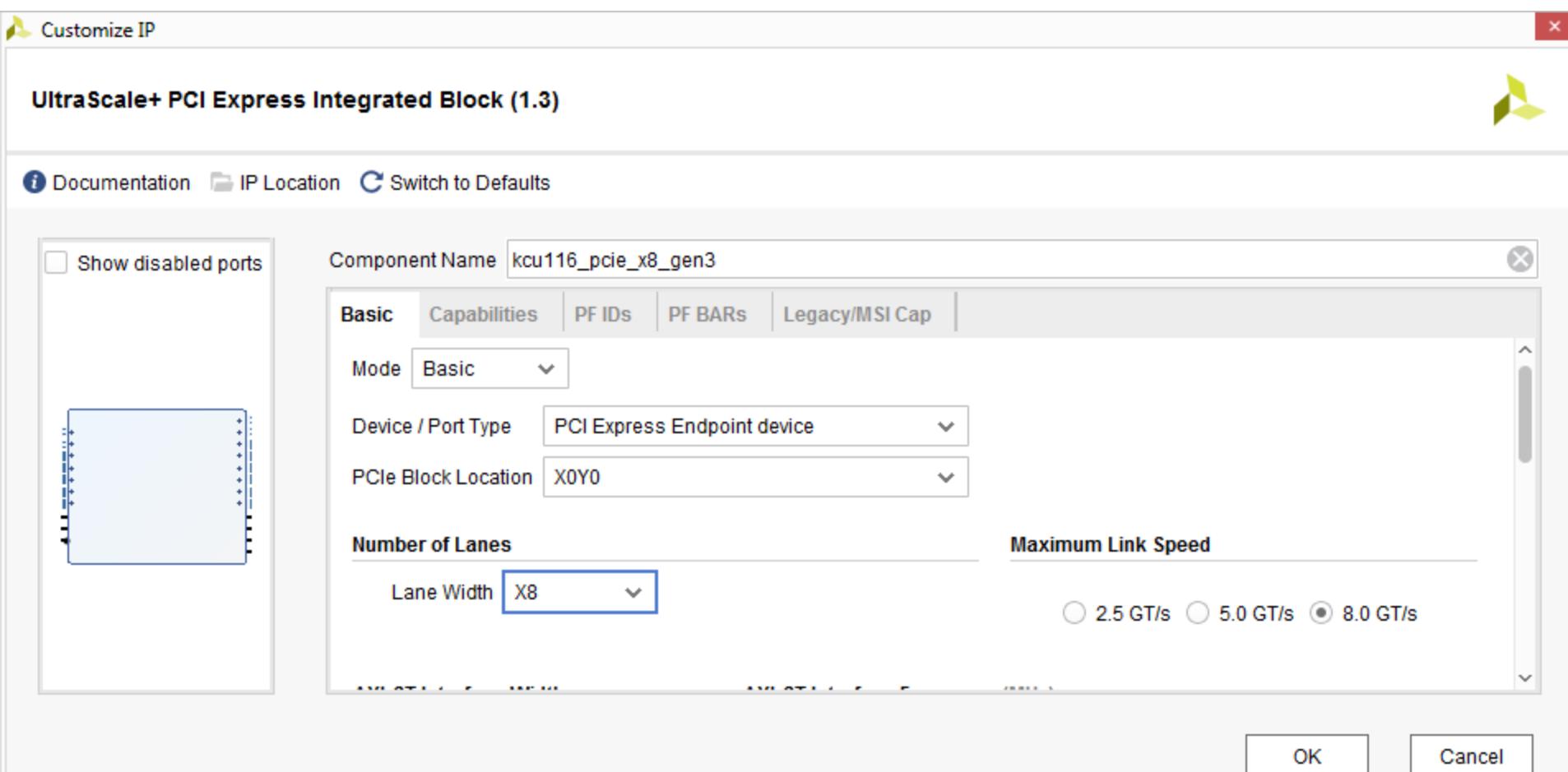


Note: Presentation applies to the KCU116

Generate x8 Gen 3 PCIe Core

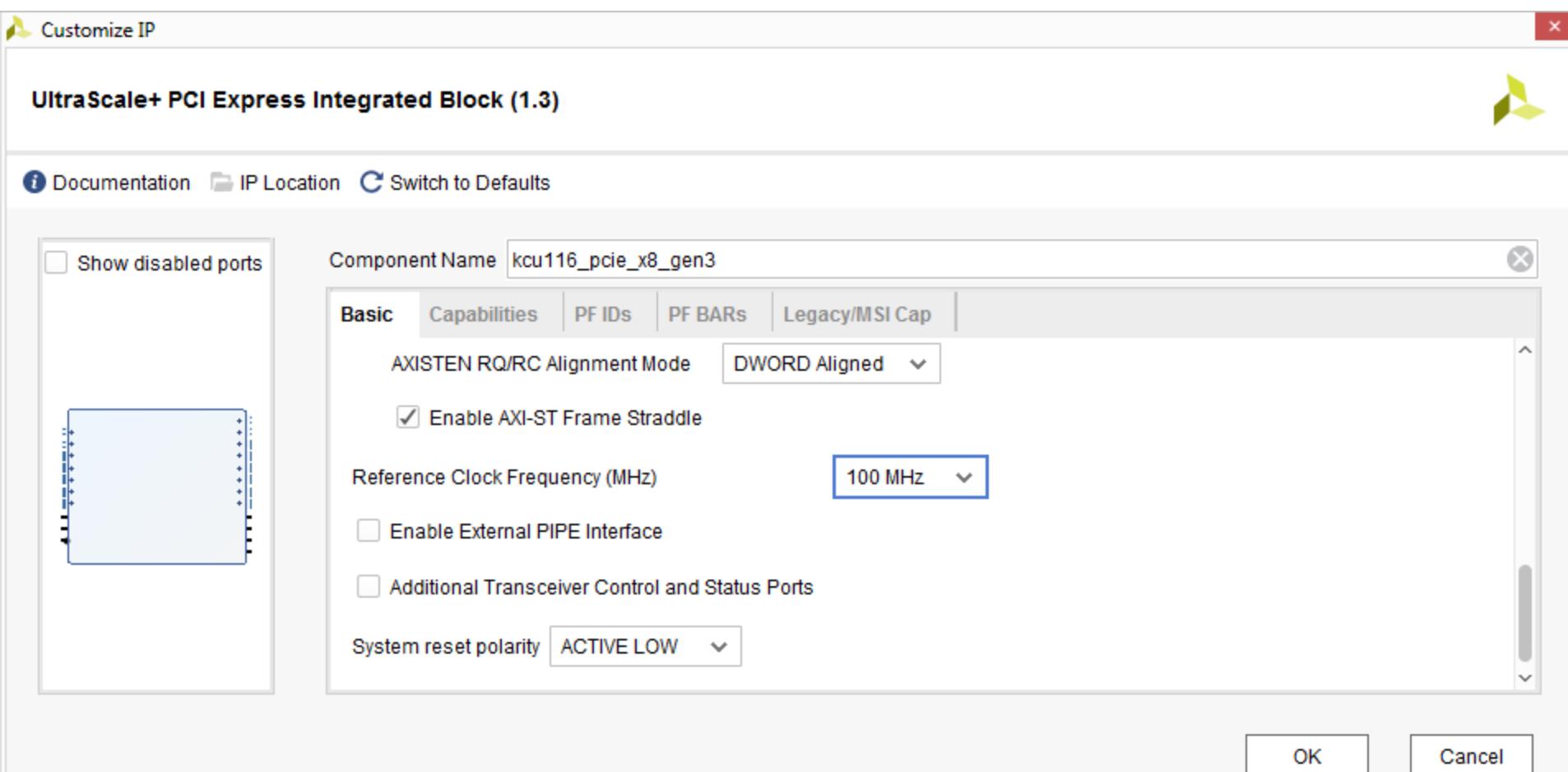
> Under the Basic tab,

- » Set Component Name to **kcu116_pcie_x8_gen3**
- » Set the Max Link Speed to **8.0 GT/s**
- » Set the Lane Width to **X8**



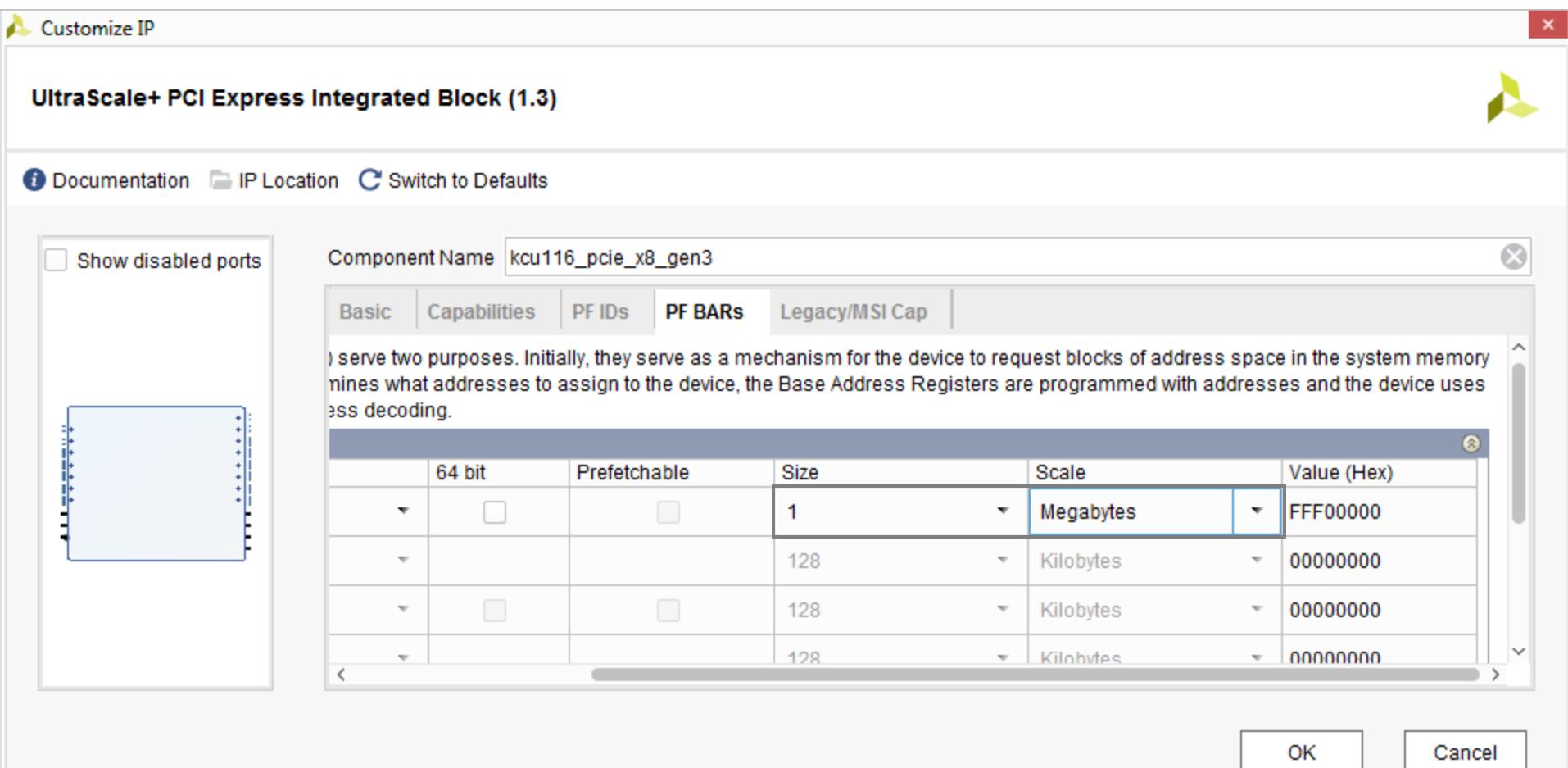
Generate x8 Gen 3 PCIe Core

- > Under the Basic tab,
 - » Set the Ref Clock to 100 MHz



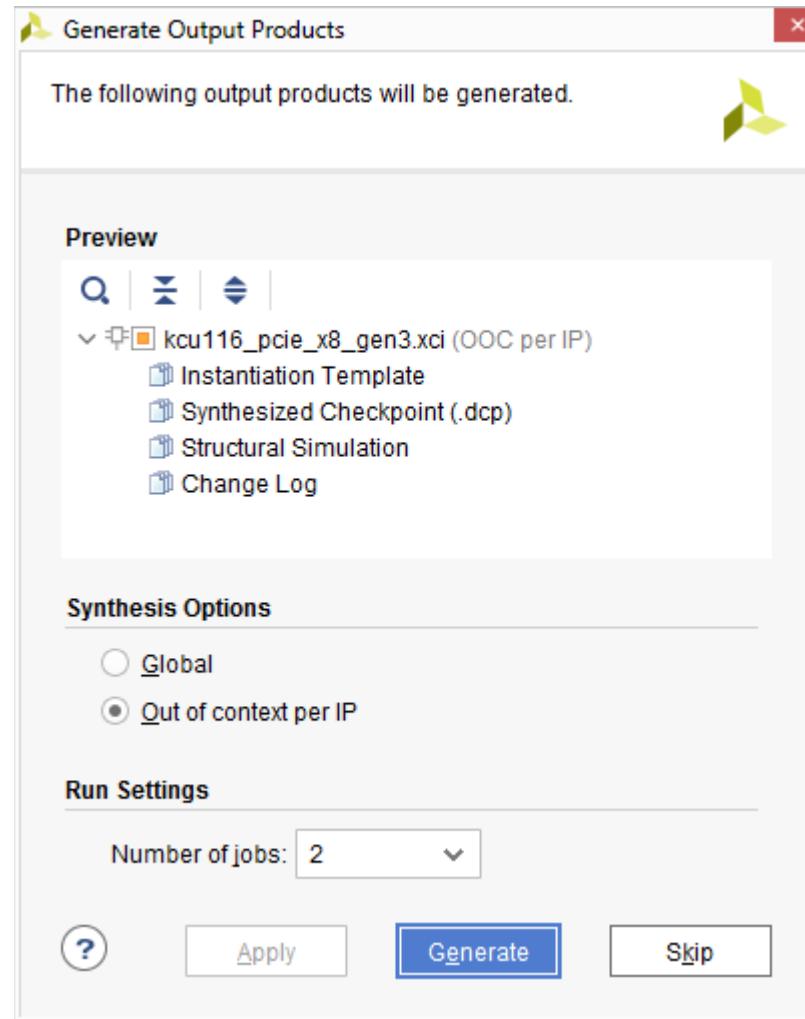
Generate x8 Gen 3 PCIe Core

- > Under the PF0 BAR tab, set BAR 0
 - » Set to 1 Megabytes
- > Click OK



Generate x8 Gen 3 PCIe Core

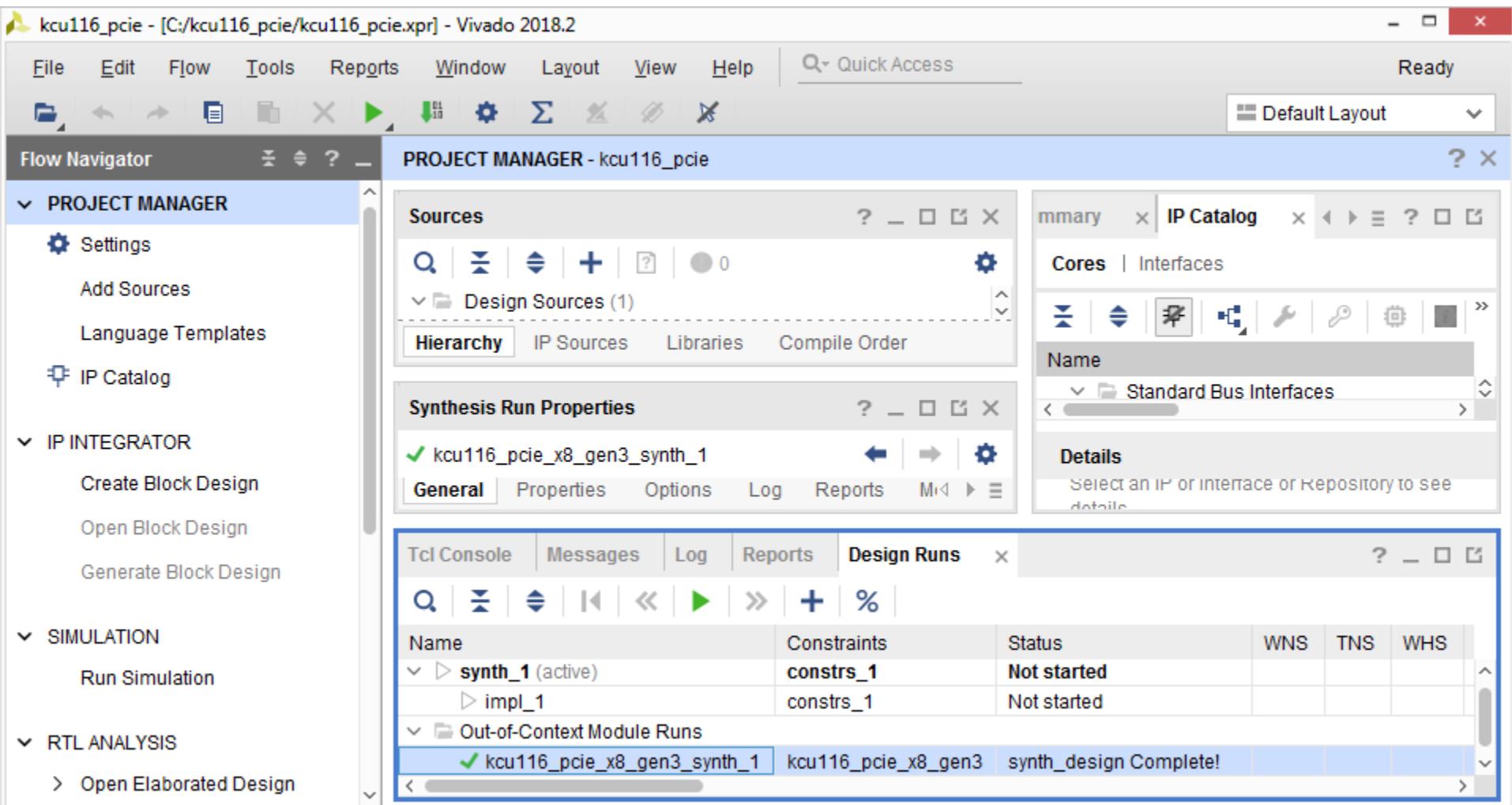
> Click Generate



Generate x8 Gen 3 PCIe Core

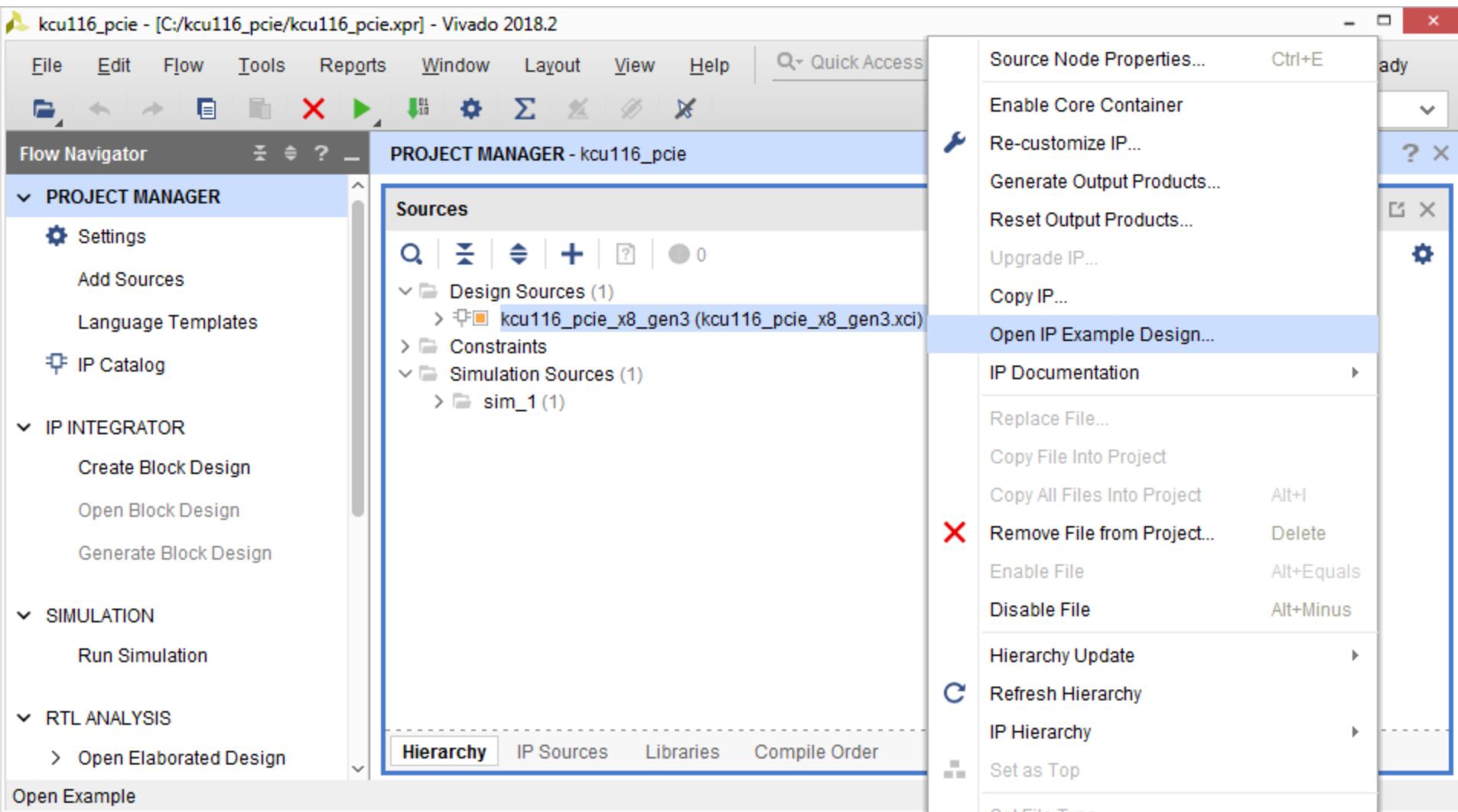
> PCIe design appears in Design Sources

- » Wait until checkmark appears on kcu116_PCIE_x8_gen3_synth_1



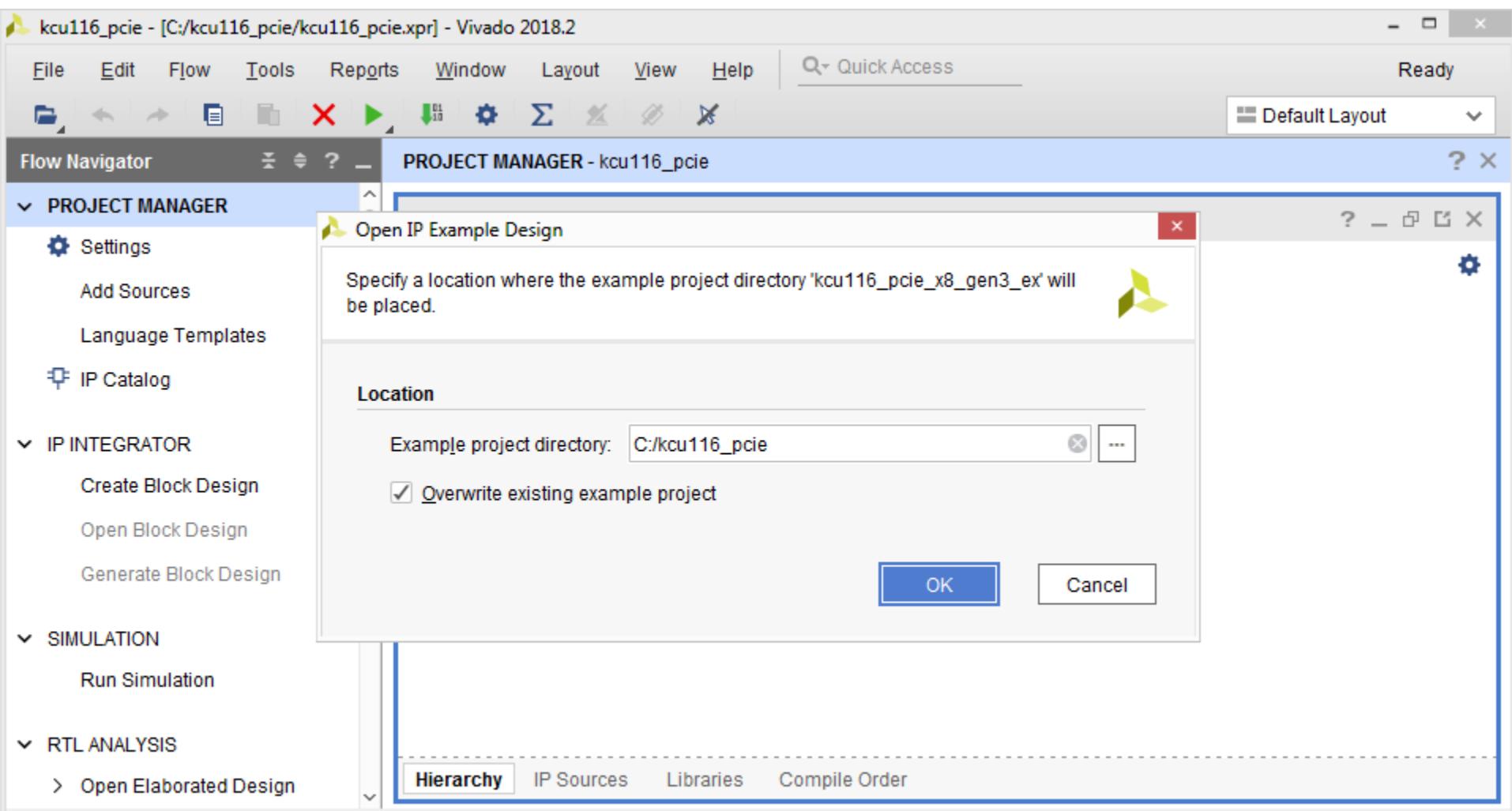
Generate x8 Gen 3 PCIe Core

- > Right-click on kcu116_pcie_x8_gen3 and select Open IP Example Design...



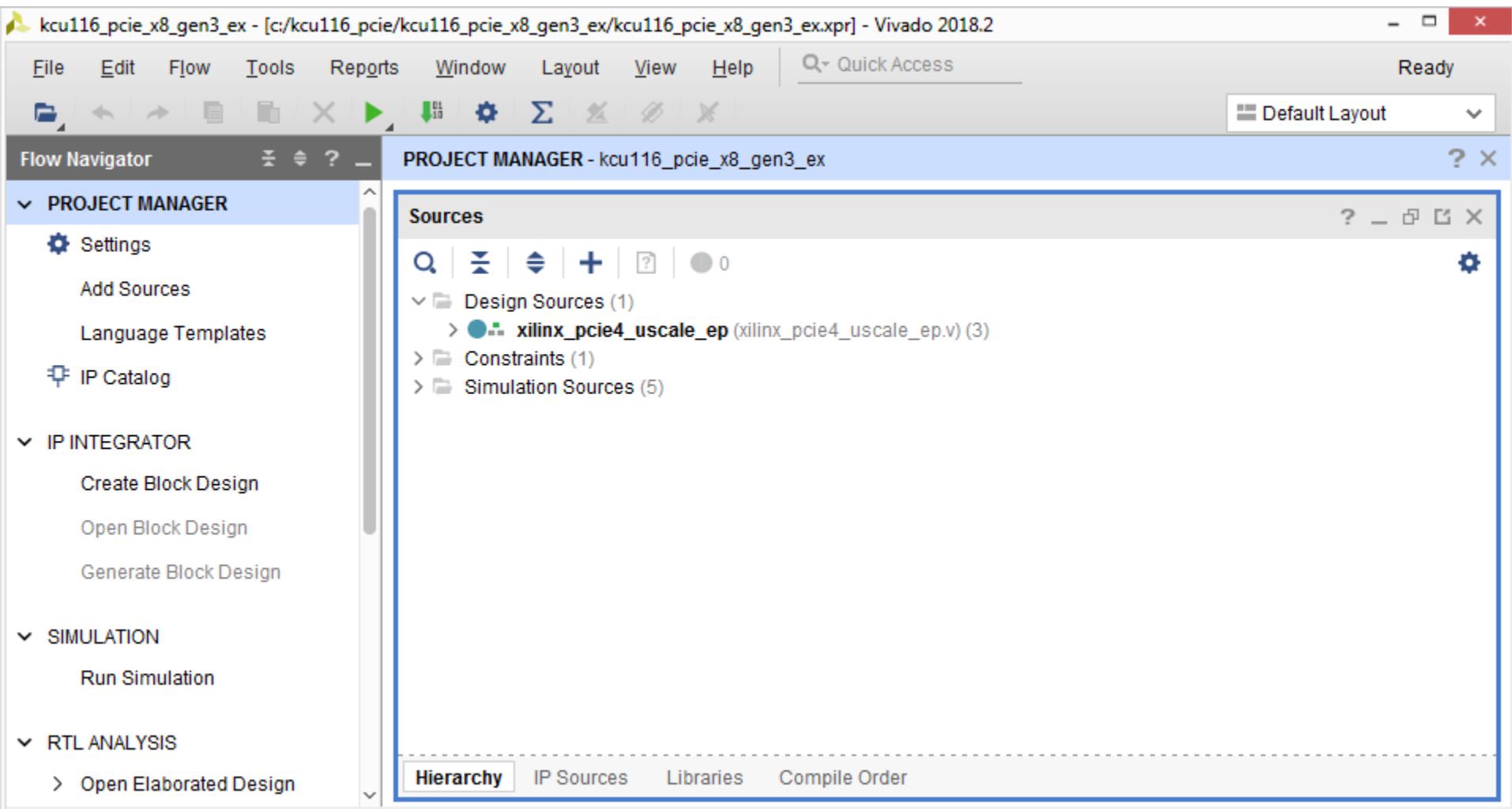
Generate x8 Gen 3 PCIe Core

- > Set the location to C:/kcu116_PCIE and click OK



Generate x8 Gen 3 PCIe Core

- > A new project is created under <design path>/
kcu116_pcie_x8_gen3_example



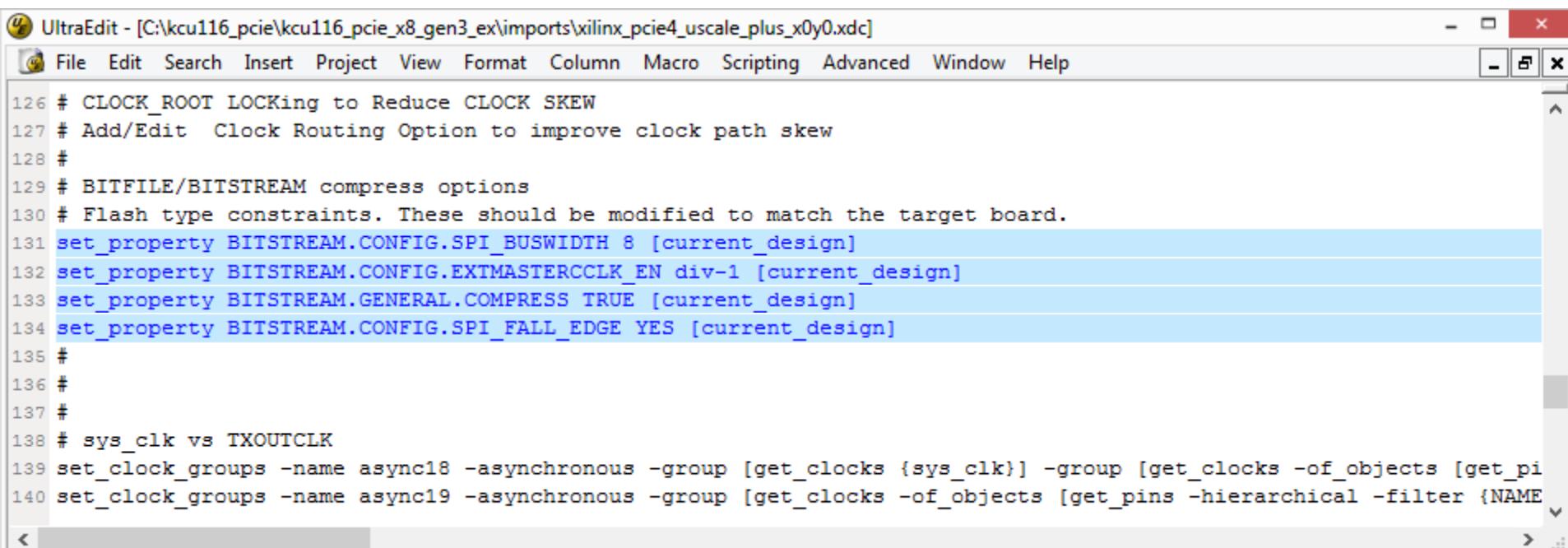
Note: The original project window can be closed

Modify PCIe Core

- > As per [UG570](#), [UG949](#), and [MT25QU01G Flash](#) specifications

- » In the XDC file, xilinx_pcie3_uscale_ep_x8g3.xdc, add these lines:

```
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
```



The screenshot shows a Windows application window titled "UltraEdit - [C:\kcu116_pcie\kcu116_pcie_x8_gen3_ex\imports\xilinx_pcie4_uscale_plus_x0y0.xdc]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The main text area displays an XDC script. Lines 131 through 140 are highlighted in blue, indicating they are the new configuration properties added to the file. The script also contains comments and other standard XDC constraints.

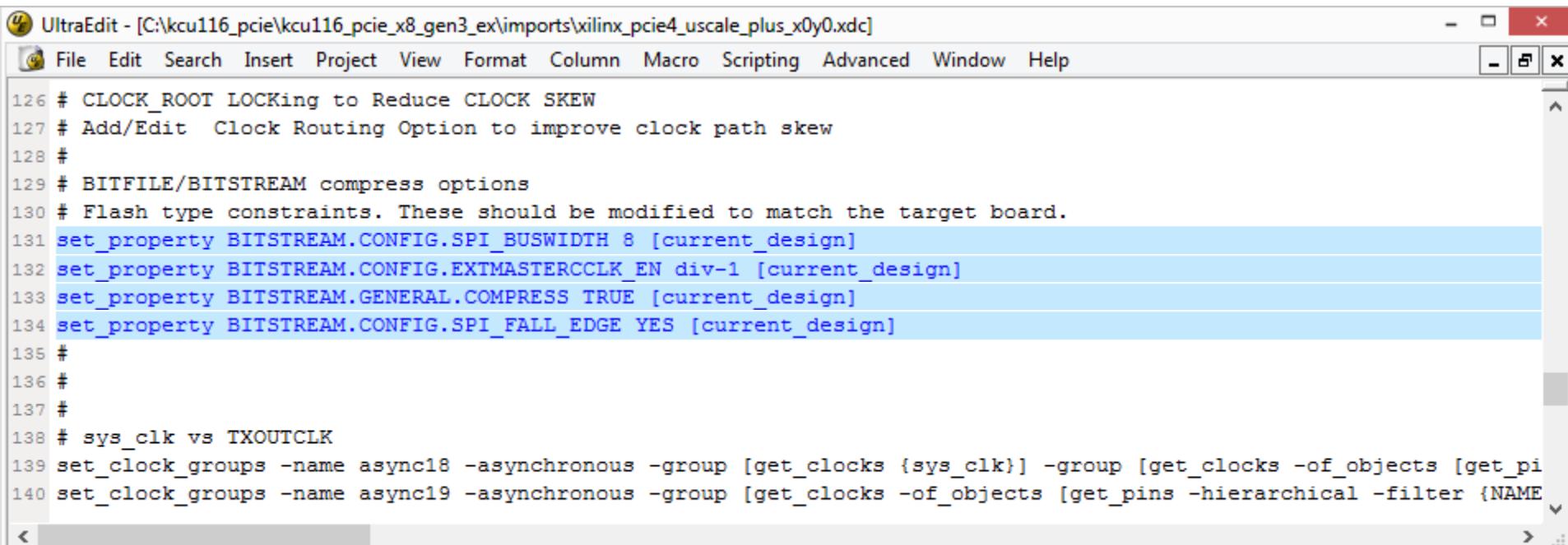
```
126 # CLOCK_ROOT LOCKING to Reduce CLOCK SKEW
127 # Add/Edit Clock Routing Option to improve clock path skew
128 #
129 # BITFILE/BITSTREAM compress options
130 # Flash type constraints. These should be modified to match the target board.
131 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
132 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
133 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
134 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
135 #
136 #
137 #
138 # sys_clk vs TXOUTCLK
139 set_clock_groups -name async18 -asynchronous -group [get_clocks {sys_clk}] -group [get_clocks -of_objects [get_pins -hierarchical -filter {NAME
```

Note: Do this after creating the example design

Modify PCIe Core

> Details on the XDC constraints :

- » MT25QU01G Maximum Frequency: 108 MHz; KCU116 EMCCLK Freq: 90 MHz
- » BITSTREAM.CONFIG.SPI_BUSWIDTH 8: For Dual Quad SPI
- BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1: Sets the EMCCLK in the FPGA to divide by 1
- » BITSTREAM.GENERAL.COMPRESS TRUE: Shrinks the bitstream
- » BITSTREAM.CONFIG.SPI_FALL_EDGE YES: Improves SPI loading speed

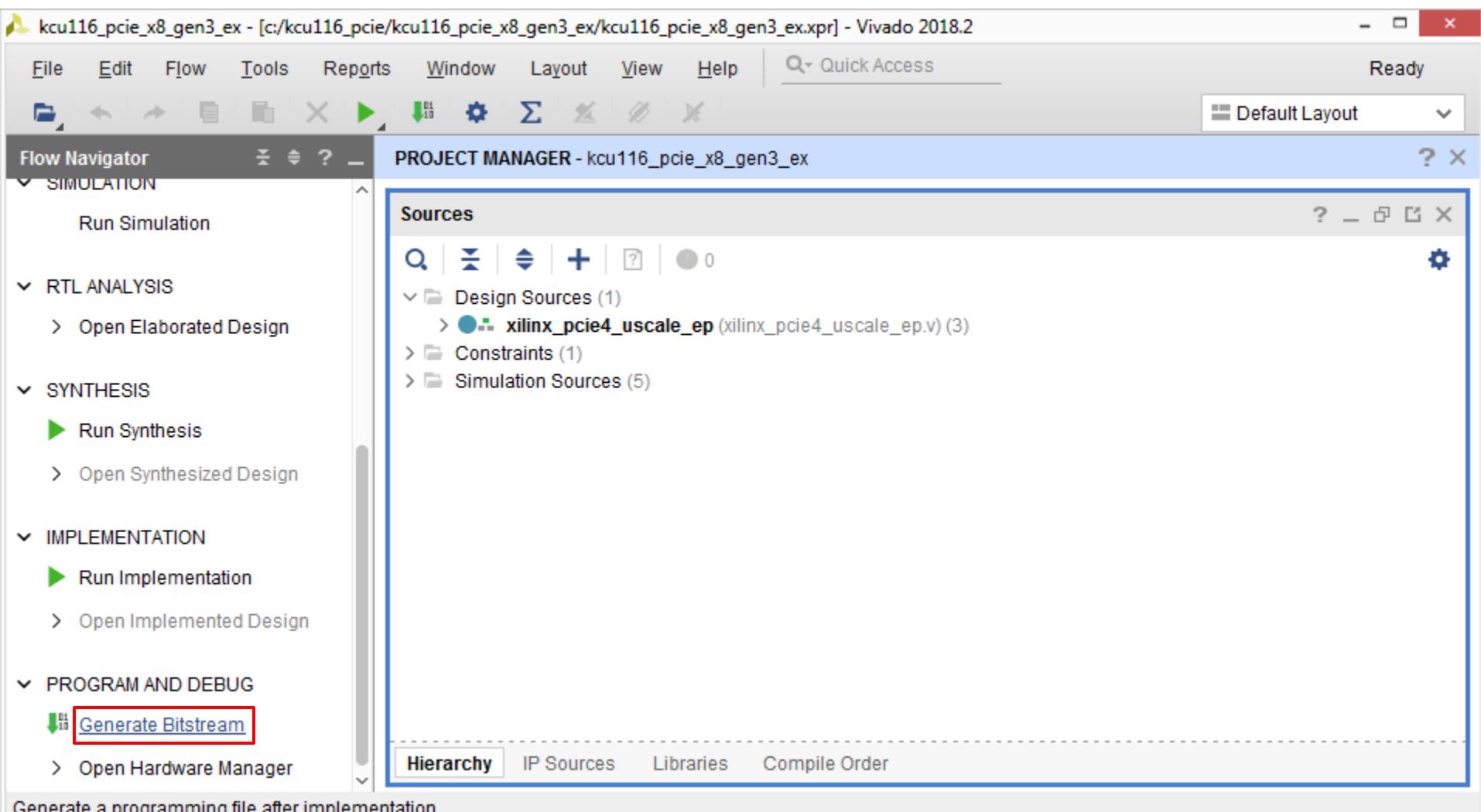


The screenshot shows a window titled "UltraEdit - [C:\kcu116_pcie\kcu116_pcie_x8_gen3_ex\imports\xilinx_pcie4_uscale_plus_x0y0.xdc]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The code area displays the following XDC constraints:

```
126 # CLOCK_ROOT LOCKING to Reduce CLOCK SKEW
127 # Add/Edit Clock Routing Option to improve clock path skew
128 #
129 # BITFILE/BITSTREAM compress options
130 # Flash type constraints. These should be modified to match the target board.
131 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
132 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
133 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
134 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
135 #
136 #
137 #
138 # sys_clk vs TXOUTCLK
139 set_clock_groups -name async18 -asynchronous -group [get_clocks {sys_clk}] -group [get_clocks -of_objects [get_pins -hierarchical -filter {NAME
```

Compile Example Design

- > Click on Generate Bitstream



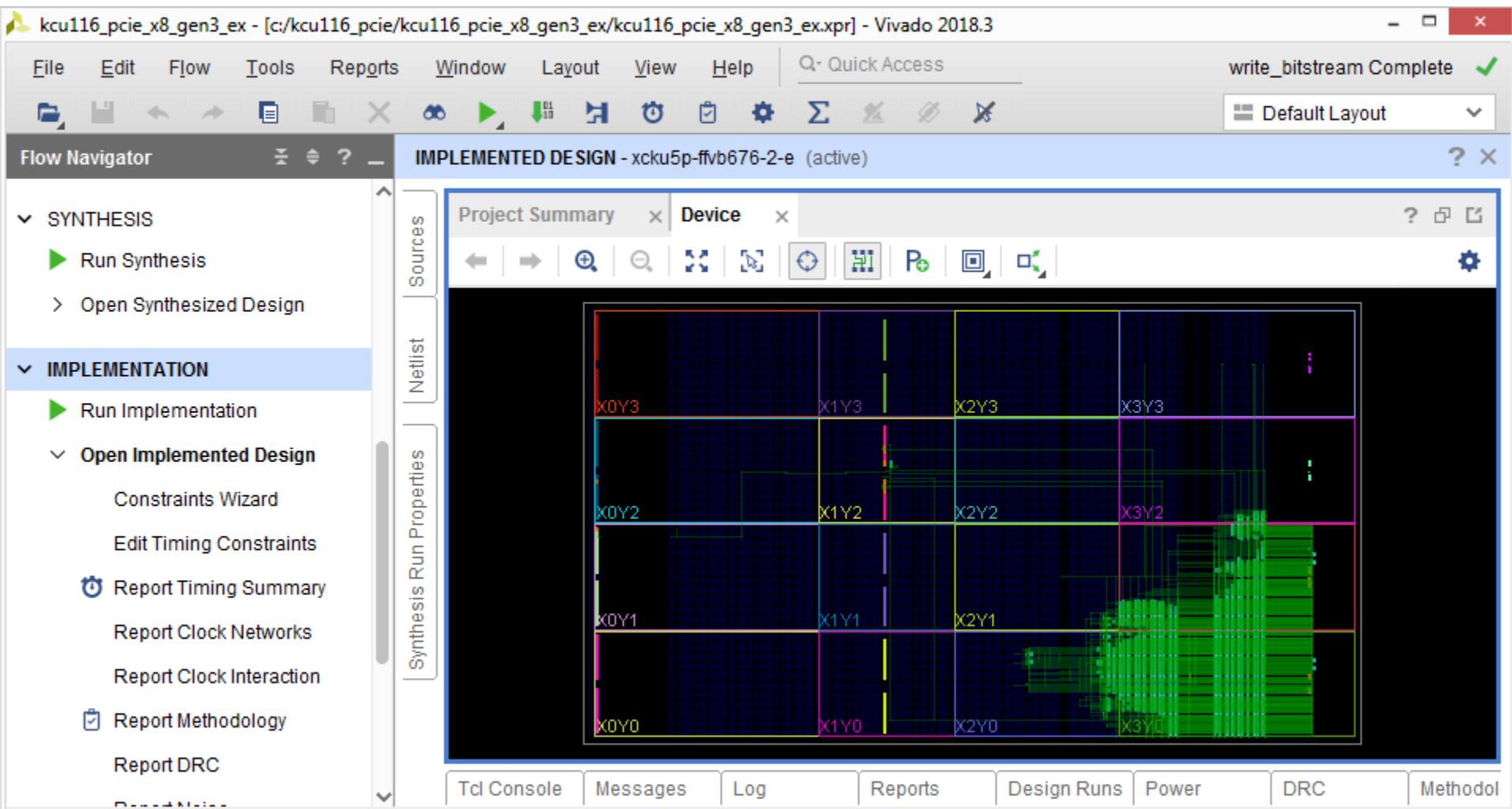
Generate a programming file after implementation

Note: Presentation applies to the KCU116

 XILINX

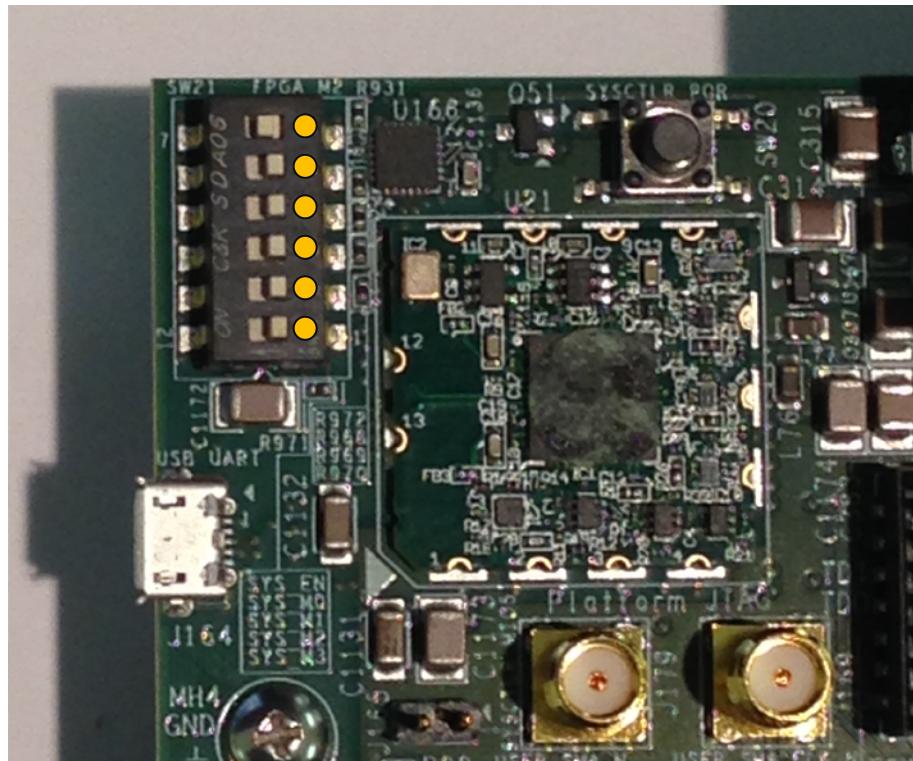
Compile Example Design

- > Open and view the Implemented Design



Programming the Dual MT25QU01G QSPI Flash

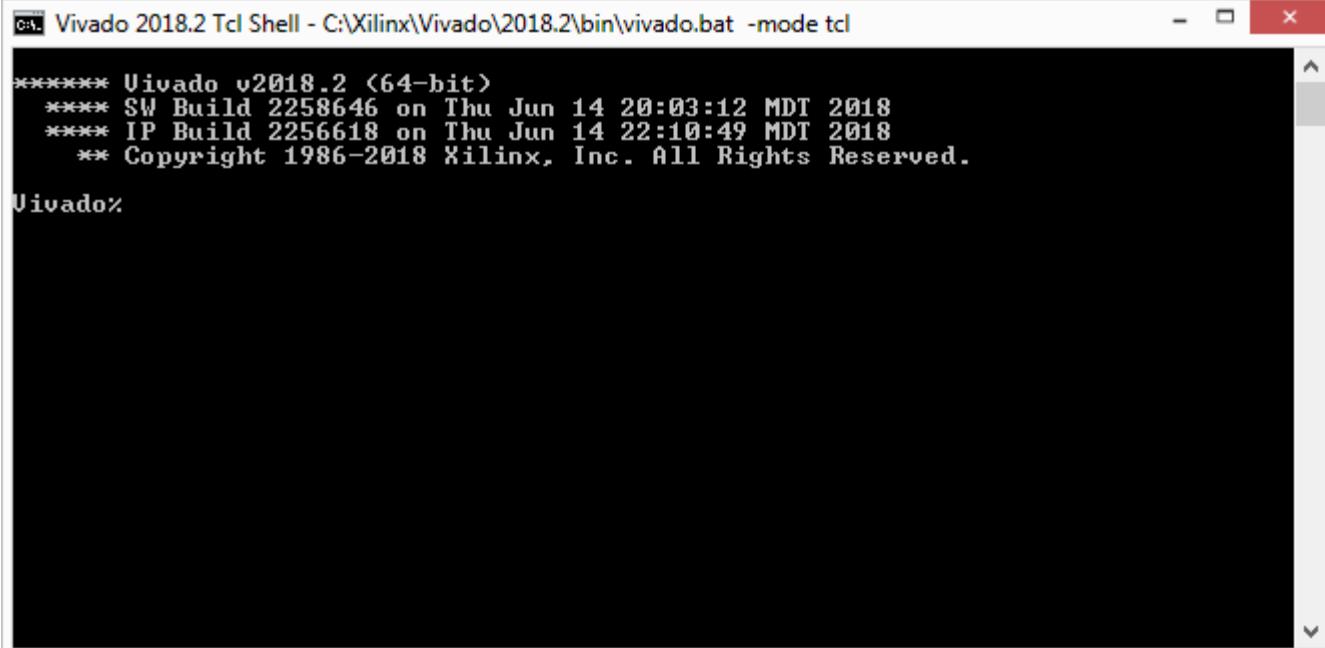
- > Set S21 to 000000 (1 = on, Position 1 → Position 6)
 - » This enables Master SPI configuration from the Dual MT25QU01G QSPI Flash



Generate PCIe MCS File

> Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 →
Vivado 2019.1 Tcl Shell



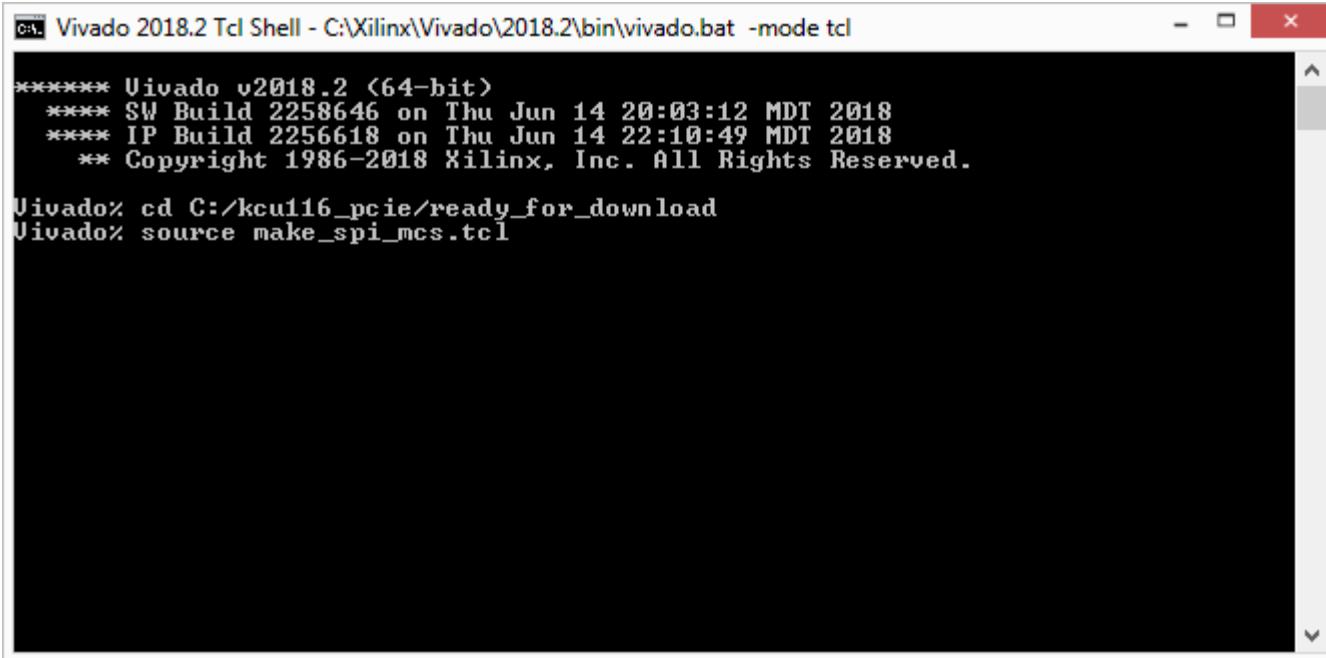
```
Vivado 2018.2 (64-bit)
 **** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
 **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
 ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

Vivado>
```

Program SPI Flash with PCIe Design

- > Create the Dual QSPI PCIe MCS files
- > In the Vivado Tcl Shell type:

```
cd C:/kcu116_PCIE/ready_for_download  
source make_spi_mcs.tcl
```



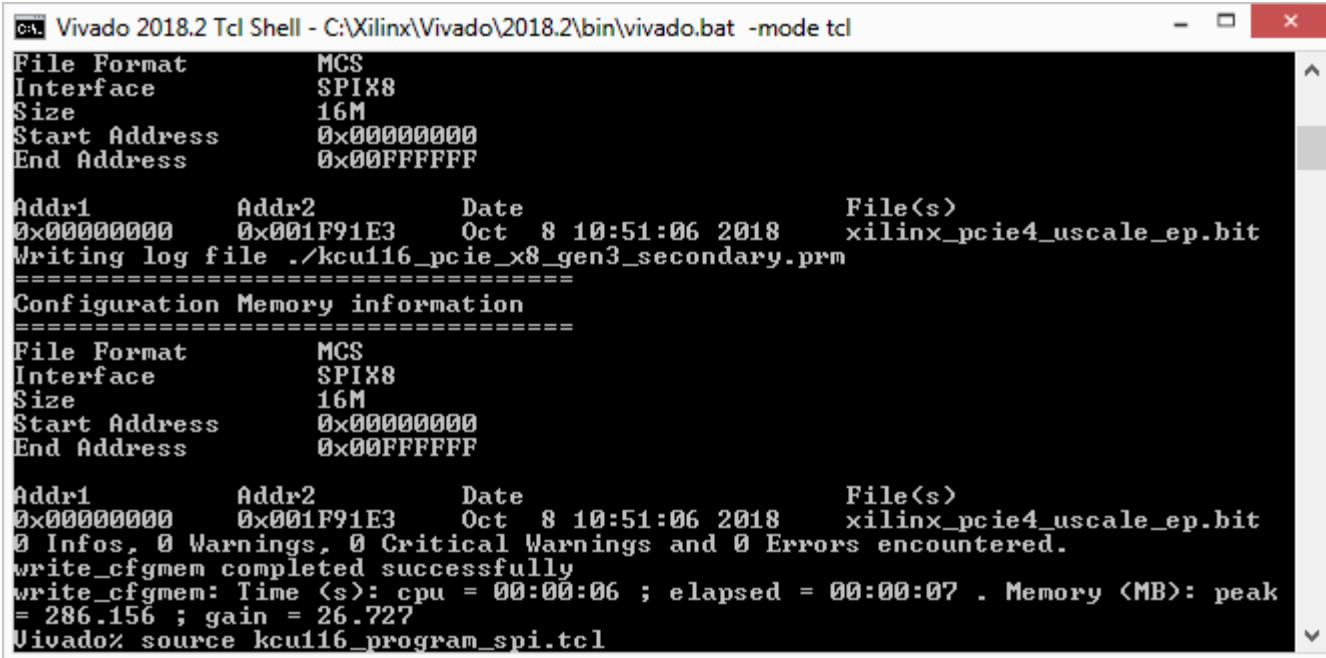
The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kcu116_PCIE/ready_for_download  
Vivado> source make_spi_mcs.tcl
```

Program SPI Flash with PCIe Design

- > Program the Dual QSPI Flash devices
- > In the Vivado Tcl Shell type:

```
source kcu116_program_spi.tcl
```



```
C:\ Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl
File Format      MCS
Interface        SPIx8
Size             16M
Start Address    0x00000000
End Address      0x00FFFFFF

Addr1           Addr2           Date          File(s)
0x00000000     0x001F91E3   Oct 8 10:51:06 2018  xilinx_pcie4_uscale_ep.bit
Writing log file ./kcu116_pcie_x8_gen3_secondary.prm
=====
Configuration Memory information
=====
File Format      MCS
Interface        SPIx8
Size             16M
Start Address    0x00000000
End Address      0x00FFFFFF

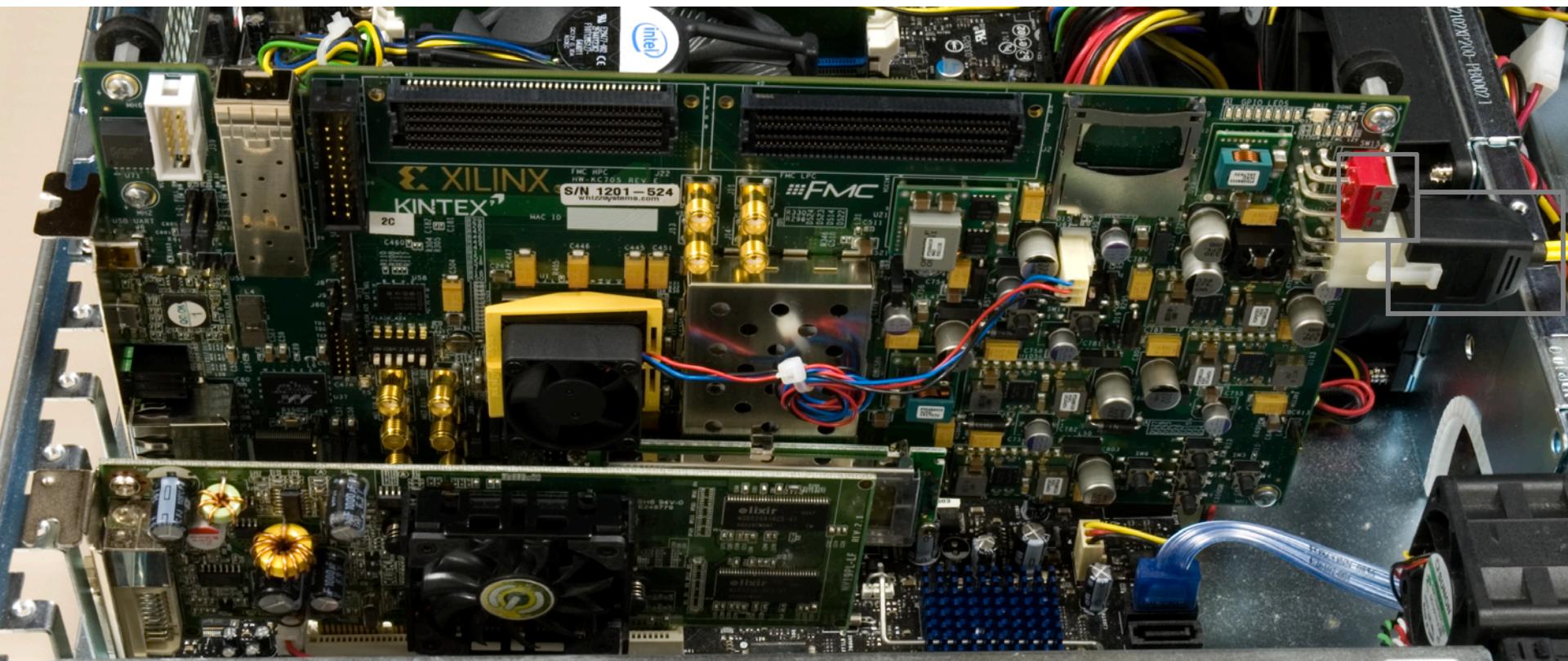
Addr1           Addr2           Date          File(s)
0x00000000     0x001F91E3   Oct 8 10:51:06 2018  xilinx_pcie4_uscale_ep.bit
0 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_cfm completed successfully
write_cfm: Time <s>: cpu = 00:00:06 ; elapsed = 00:00:07 . Memory <MB>: peak
= 286.156 ; gain = 26.727
Vivado% source kcu116_program_spi.tcl
```

Note: Takes about two minutes

Hardware Setup

- > Insert the KCU116 Board into a PCIe slot (KC705 shown)

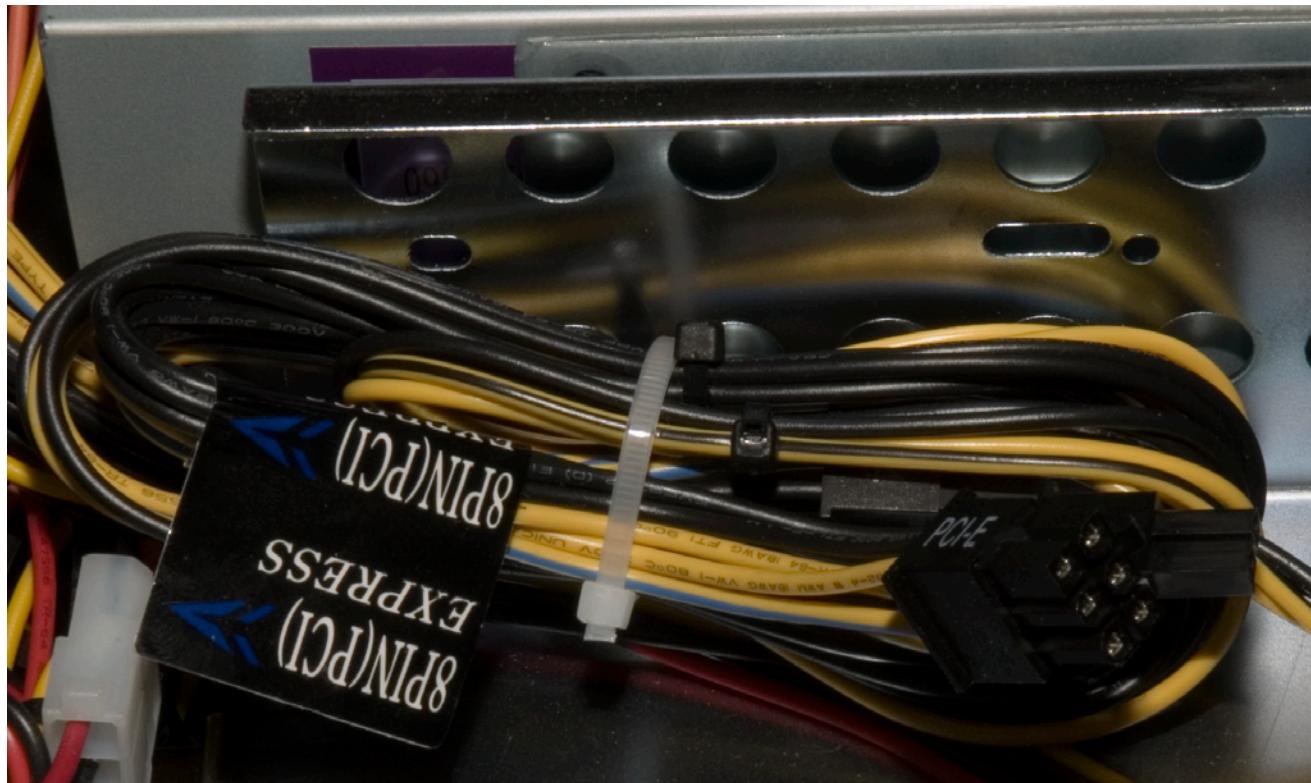
- » Use the included PC Power adapter; turn on Power Switch



Note: As per AR64404, you may need to do a warm-reset

Hardware Setup

- > Do not use the PCIe connector from the PC power supply

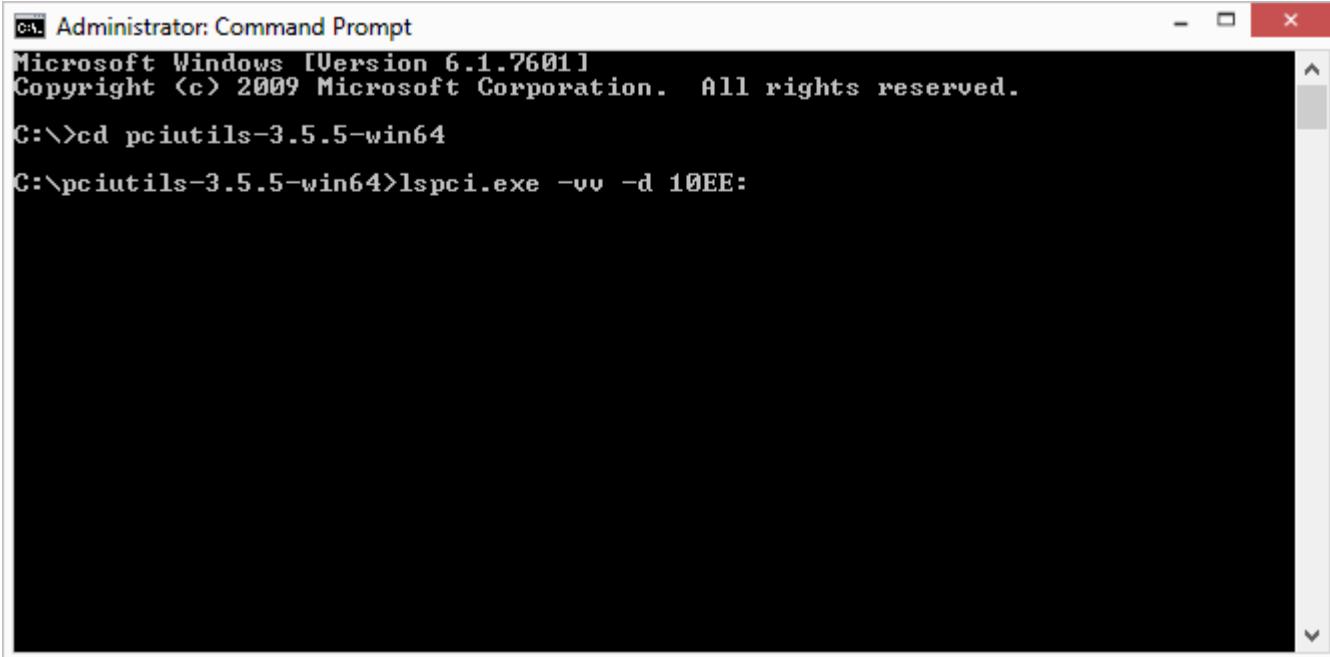


Running the PCIe x8 Gen3 Design

- > Power on the PC
- > Open an Administrator command prompt and type:

```
cd pciutils-3.5.5-win64
```

```
lspci.exe -vv -d 10EE:
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window title bar includes the standard Windows icons for minimize, maximize, and close. The command prompt itself displays the following text:

```
C:\>Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\>cd pciutils-3.5.5-win64
C:\pciutils-3.5.5-win64>lspci.exe -vv -d 10EE:
```

The command `lspci.exe -vv -d 10EE:` is shown at the bottom of the window, indicating it has been entered but has not yet produced any visible output.

Note: Modify path to match your version of the PCI Utils

Running the PCIe x8 Gen3 Design

- > Shown here on Linux, Xilinx at 8GT/s (Gen3) and Width x8

```
xilinx@localhost:/home/xilinx

File Edit View Search Terminal Help
[root@localhost xilinx]# lspci -vv -d 10ee:
01:00.0 Memory controller: Xilinx Corporation Device 9038
    Subsystem: Xilinx Corporation Device 0007
    Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx-
    Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbsorb- <MAbort- >SERR- <PERR- INTx-
    Latency: 0
    Region 0: Memory at df900000 (32-bit, non-prefetchable) [size=1M]
    Capabilities: [40] Power Management version 3
        Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME(D0-,D1-,D2-,D3hot-,D3cold-)
        Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
    Capabilities: [48] MSI: Enable- Count=1/1 Maskable- 64bit+
        Address: 0000000000000000 Data: 0000
    Capabilities: [70] Express (v2) Endpoint, MSI 00
        DevCap: MaxPayload 1024 bytes, PhantFunc 0, Latency L0s <64ns, L1 <1us
            ExtTag+ AttnBtn- AttnInd- PwrInd- RBE+ FLReset-
        DevCtl: Report errors: Correctable- Non-Fatal- Fatal- Unsupported-
            RlxOrdRd+ ExtTag+ PhantFunc- AuxPwr- NoSnoop+
            MaxPayload 128 bytes, MaxReadReq 512 bytes
        DevSta: CorrErr+ UncorrErr- FatalErr- UnsuppReq+ AuxPwr- TransPend-
        LnkCap: Port #0, Speed 8GT/s, Width x8, ASPM not supported, Exit Latency L0s unlimited, L1 unlimited
            ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp+
        LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- CommClk+
            ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
        LnkSta: Speed 8GT/s, Width x8, TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
        DevCap2: Completion Timeout: Range BC, TimeoutDis+, LTR-, OBFF Not Supported
        DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-, LTR-, OBFF Disabled
        LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
            Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
            Compliance De-emphasis: -6dB
        LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+, EqualizationPhase1+
            EqualizationPhase2-, EqualizationPhase3-, LinkEqualizationRequest-
    Capabilities: [100 v1] Advanced Error Reporting
        UESTa: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
        UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
        UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC- UnsupReq- ACSViol-
        CESta: RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
        CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
        AERCap: First Error Pointer: 00, GenCap- CGenEn- ChkCap- ChkEn-
    Capabilities: [1c0 v1] #19
```

References



References

> PCIe Base Specification

- » PCI SIG Web Site
 - <http://pcisig.com>

> Xilinx PCI Express

- » Xilinx PCI Express Overview
 - <https://www.xilinx.com/products/technology/pci-express.html>
- » UltraScale+ Integrated Block for PCI Express Product Page
 - <https://www.xilinx.com/products/intellectual-property/pcie4-ultrascale-plus.html>
- » UltraScale+ Integrated Block for PCI Express Product Guide – PG213
 - https://www.xilinx.com/support/documentation/ip_documentation/pcie4_uscale_plus/v1_3/pg213-pcie4-ultrascale-plus.pdf
- » UltraScale+ Integrated Block for PCI Express – Release Notes
 - <https://www.xilinx.com/support/answers/65751.html>

References

- > **Micron NOR Flash**
 - » Micron MT25QU01G Flash
 - <https://www.micron.com/products/nor-flash/serial-nor-flash>
 - » Datasheet
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