I step ⇒ Algorithm

```
mult = 0
while ( a > 0 ) {
  mult = mult + b
  a = a - 1
}
```

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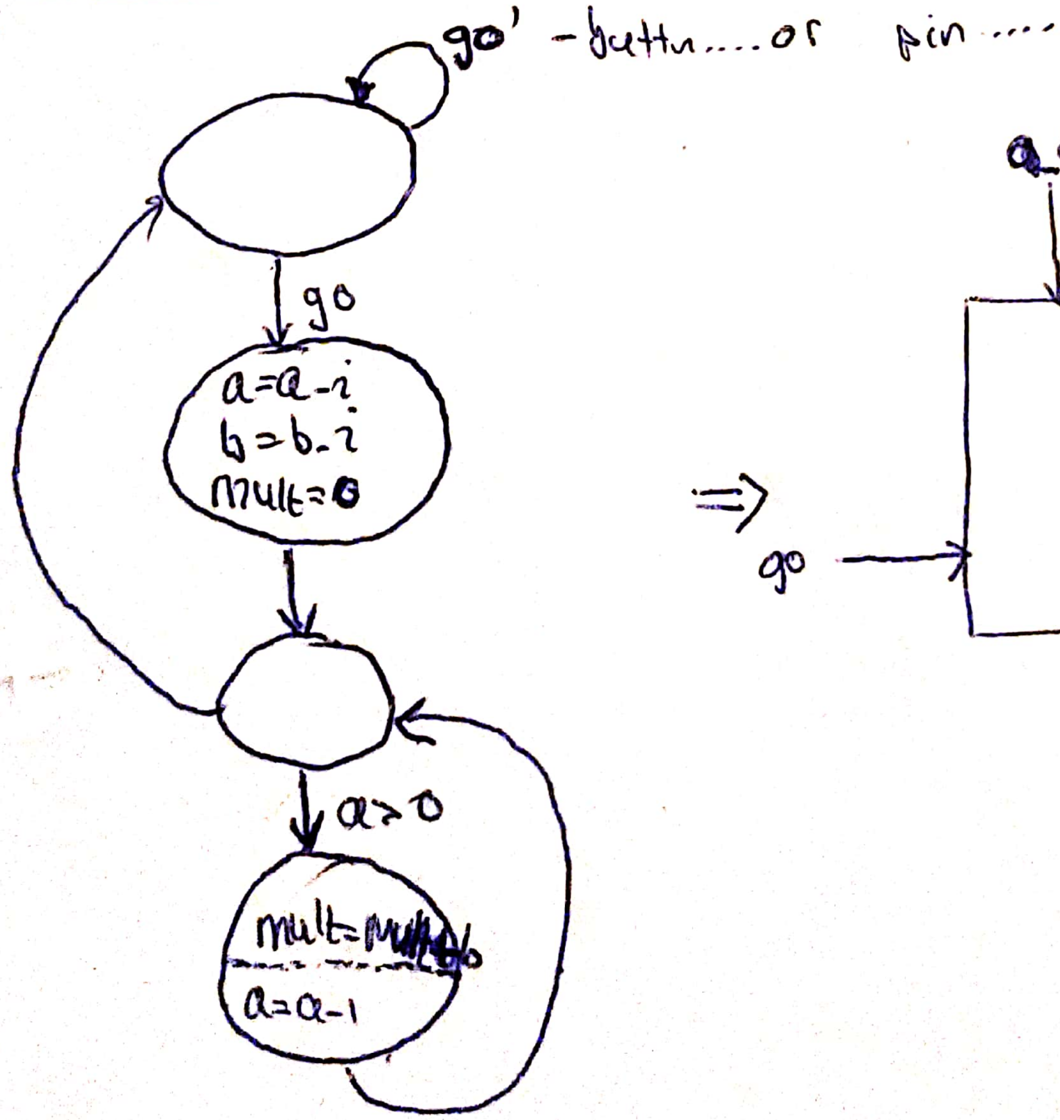
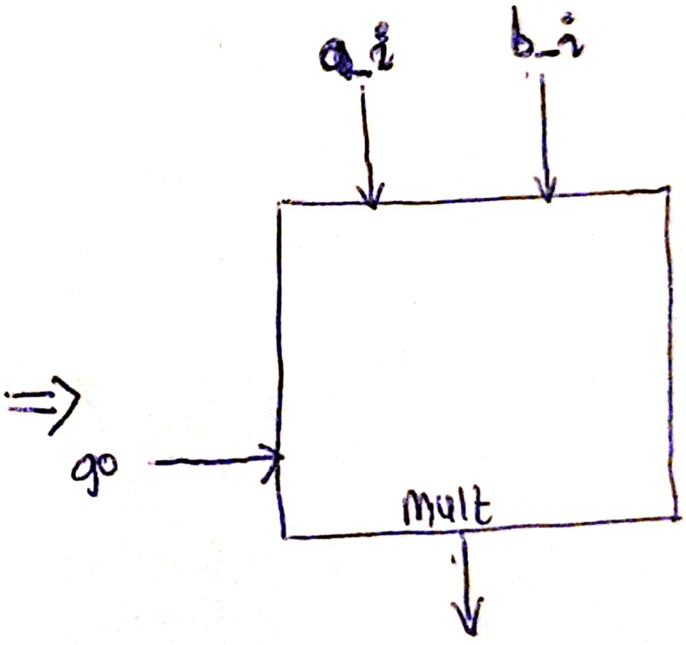
```
while ( !go )
a = a_i
b = b_i
    mult = 0 ( 16-bit also )
while ( a > 0 ) {
  mult = mult + b
  a = a - 1
}
```

Corresponding FSM





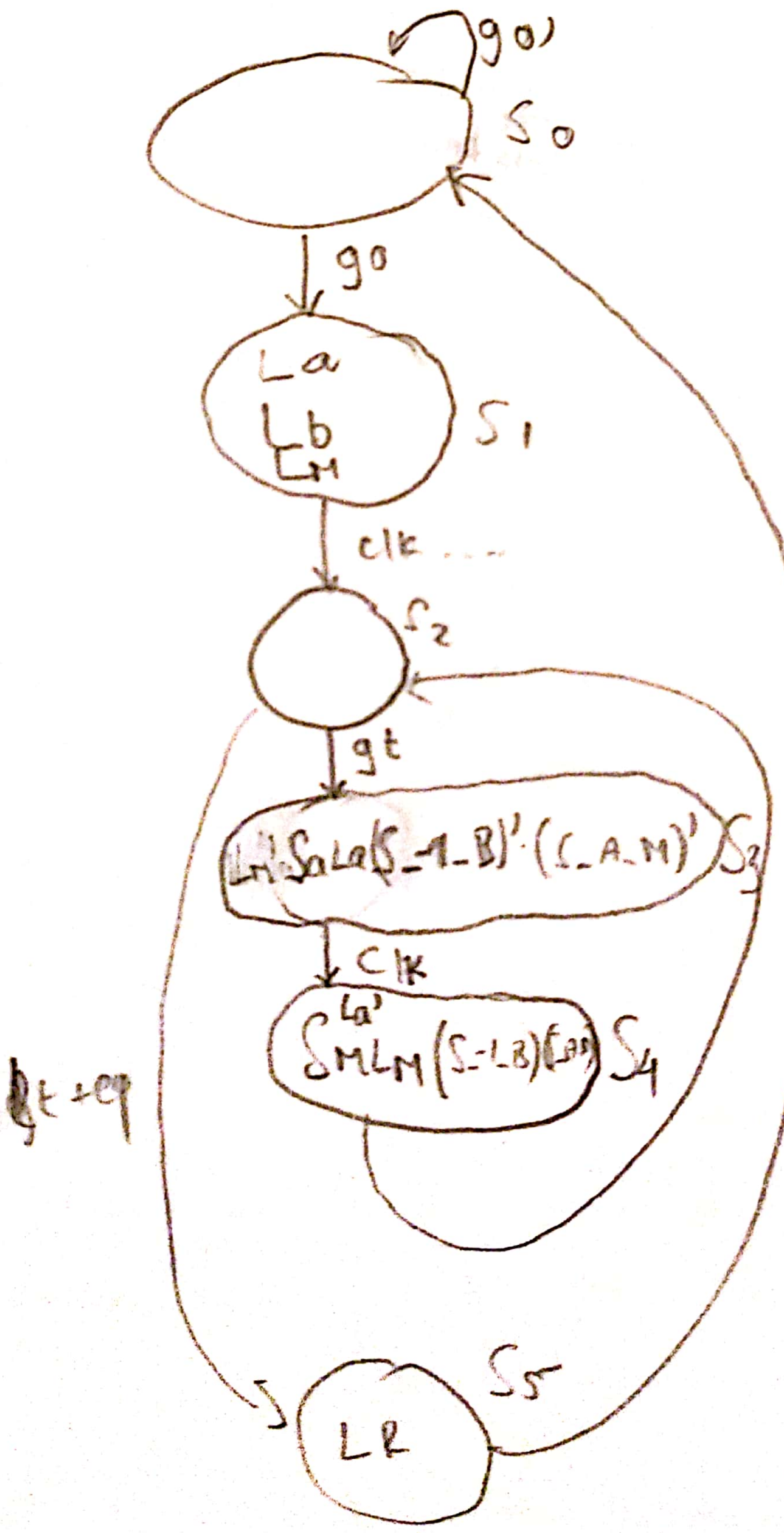
input : a (16 bit register)
b (16- bit register)

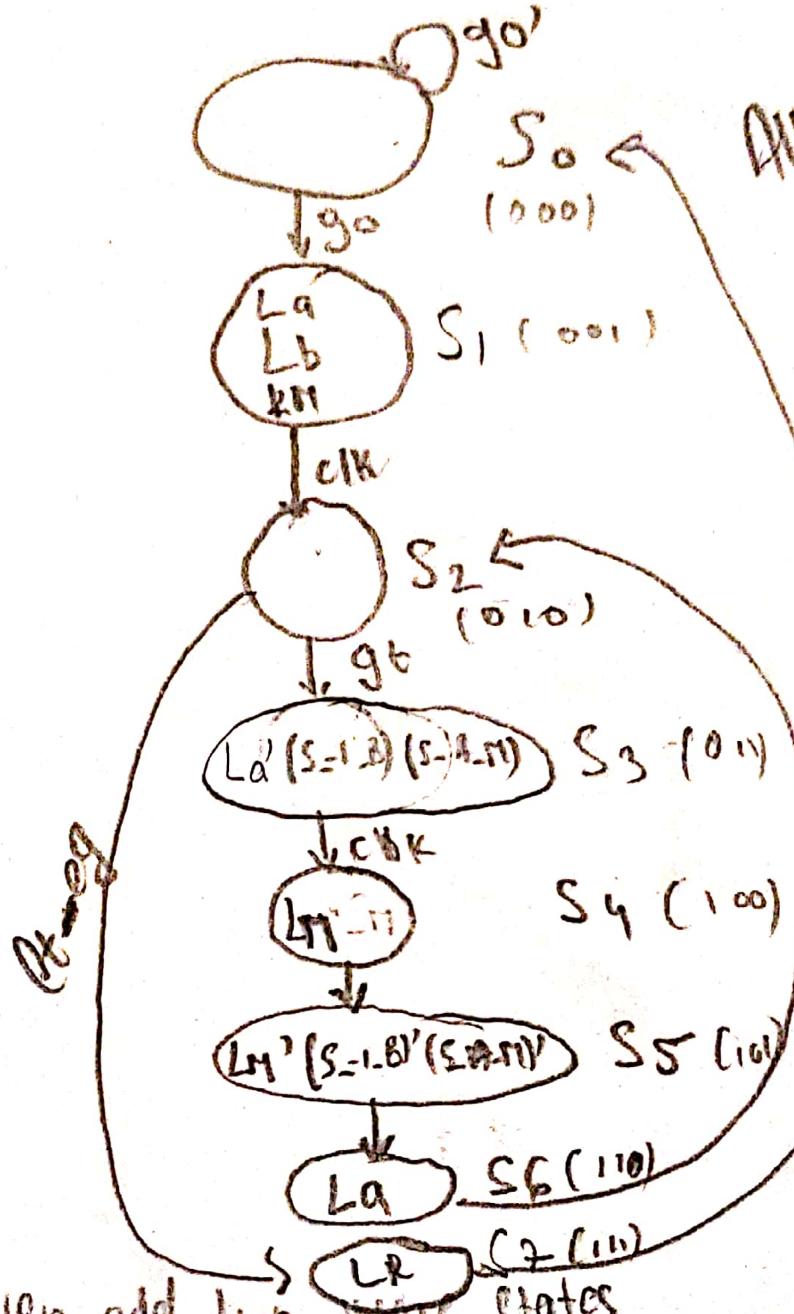
a_i (16 -bit pin)
b_i (16- bit pin)

0 pin (for comparing a with 0) } for while loop
comparator

-1 pin (for subtracting from a)

New /updated FSM (+1 state)





All eight states are used

maybe even add two ~~more~~ states like LM' (S_1_B)' (S_A_M)' and La' (S_1_B) (S_A_M)

to make sure it's set up correctly before doing addition ...

⇒ 8 states in total ⇒ still using only 3-bits for the states...

[illegible] table (FSM)

S_2	S_1	S_0	go	gt	lt_eq	N_2	N_1	N_0
0	0	0	0	–	–	0	0	0
0	0	0	1	–	–	0	0	1
0	0	1	–	–	–	0	1	0
0	1	0	–	1	0(-)	0	1	1
0	1	0	–	0(-)	1	1	1	1
0	1	1	–	–	–	1	0	0
1	0	0	–	–	–	1	0	1
1	0	1	–	–	–	1	1	0
1	1	0	–	–	–	0	1	0

$\underline{N_2} = S_2'S_1S_0'.(lt\_eq) + S_2'S_1S_0 + S_2S_1'S_0'$
$+ S_2S_1'S_0$
$= \boxed{S_2'S_1S_0'(lt\_eq) + S_2'S_1S_0 + S_2S_1'}$

$\underline{N_1} = S_2'S_1'S_0 + \mathbf{S_2'S_1S_0'}gt + S_2'S_1S_0'(lt\_eq)$
$+ S_2S_1'S_0 + S_2S_1S_0'$
$= S_2'S_1'S_0 + S_2'S_1S_0'(gt + lt\_eq)$
$S_2S_1'S_0 + S_2S_1S_0'$
$= \boxed{S_2'S_1'S_0 + S_2'S_1S_0'(gt + lt\_eq) + S_2(\underbrace{S_1'S_0 + S_1S_0'}_{S_1 \oplus S_0})}$

$N_0 = \boxed{S_2'S_1'S_0'go + S_2'S_1S_0'(gt + lt\_eq) + S_2S_1'S_0'}$

Output table

S_2 S_1 S_0	La	Lb	S_1_B	S_A_M	LM	LR	S_A	RM
S_0	0	0	0	0	0	0	-	0
S_1	1	1	0	0	0	0	0	1
S_2	0	0	0	0	0	0	0	0
S_3	0	$\overline{0}$	1	1	$\overline{0}$	$\overline{0}$	0	0
S_4	$\overline{0}$	$\overline{0}$	$\overline{1}$	1	1	$\overline{0}$	0	1
S_5	$\overline{0}$	$\overline{0}$	0	0	0	$\overline{0}$	1	1
S_6	1	$\overline{0}$	$\overline{0}$	$\overline{0}$	$\overline{0}$	$\overline{0}$	1	1
S_7	$\overline{0}$	$\overline{0}$	$\overline{0}$	$\overline{0}$	$\overline{0}$	1	-	1

$La = S_1 + S_6$

$Lb = S_1$

$S\_1\_B = S_3 + S_4$

$S\_A\_M = S_3 + S_4$

$LM = S_4$

$LR = S_7$

$S_A = S_5 + S_6$

$RM = S_1$