Application Report

Thermal Performance of QFN 12x12 Package for 600-V GaN Power Stage

Wenli Zhang, Yichi Zhang, Yong Xie, and Paul Brohlin

ABSTRACT

A new family of driver integrated gallium nitride (GaN) power stage products offered by Texas Instruments (TI) has been implemented in a low-cost, compact quad flat no-lead (QFN) package of a large 12-mm x 12-mm footprint. This enlarged QFN package can derive pronounced benefits of GaN's fast transition-rate and high switching-frequency capabilities as well as enhance its thermal performance thanks to the large exposed thermal pad, showing better power dissipation capability than other popular surface-mount packages such as TO Lead-Less and D^2PAK which are widely used for discrete power devices. With a proper thermal design, TI's new LMG342x GaN power stage products packaged in the QFN 12x12 format can fully satisfy the need for high power (> 3 kW) conversion applications.

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1 Introduction

High-voltage (> 600 V) gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are replacing their silicon (Si)-based counterparts in fast-charging adapters, data centers, telecommunications, electric vehicles, and other applications where the need for high-density, high-efficiency power system becomes pressing and prevalent, see GaN drives energy efficiency to the next level. Due to the reduction or removal of lead induced parasitics, surface-mount type packages are more suitable than through-hole types (e.g., TO-247) for GaN HEMT devices to exploit their use in power switching applications. Texas Instruments (TI) has implemented a direct-drive GaN solution by co-packaging a high-voltage GaN transistor and its driver with an integrated protection into one quad flat no-lead (QFN) package, see Direct-drive configuration for GaN devices. The fully released LMG341x product family uses the same QFN 8x8 (i.e., 8-mm x 8-mm footprint) package for devices of 150-, 70-, and 50-mΩ on-resistance, see Gallium nitride (GaN) ICs – Products. Enabled by this surface-mount packaging solution, TI's GaN transistor with its integrated driver not only eliminates common-source inductance and significantly reduces gate-loop inductance, but also allows the built-in functions of thermal and current protections, see Optimizing GaN performance with an integrated driver. However, the power dissipation capability of these products is limited because of the small exposed thermal pad area and package size. To address the rising need for high power applications such as 4-kW power supply units for server and telecom, a new QFN 12x12 package has been developed for TI's next-generation integrated GaN power stages (LMG342x). This application report documents the thermal performance of this new package.

2 New QFN 12x12 Package

The newly developed QFN 12x12 is a low-profile, leadless surface-mount package with an exposed copper (Cu) thermal pad and functional pins on the package bottom surface shown in Figure 2-1. It maintains the same electrical merits and functional integrations as the prior QFN 8x8 package solution used for TI's 600-V GaN power stage products. The improved package thermal design enables a high level of power dissipation and is implemented in this updated QFN 12x12 configuration.

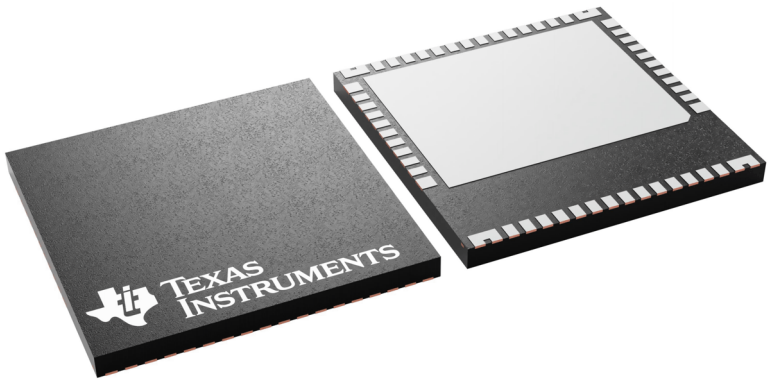


Figure 2-1. External Appearance of the QFN 12x12 Package (12 mm x 12 mm x 0.9 mm)

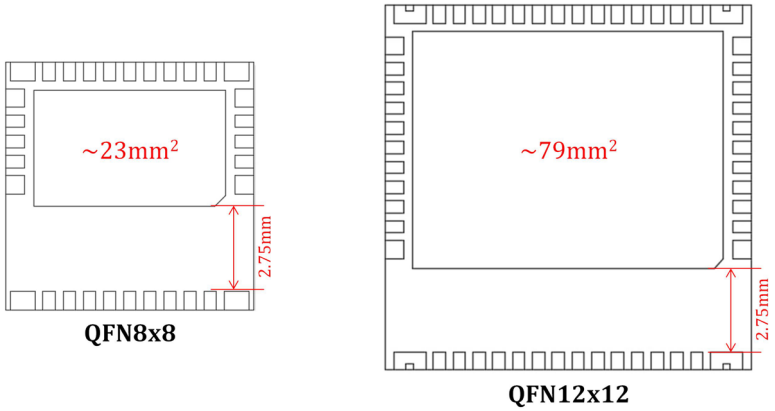


Figure 2-2. Comparison of the Pin Configuration on Package Bottom Surface

Figure 2-2 shows the QFN 12x12 package that has a 3x larger thermal pad area and the same creepage distance of 2.75 mm between the center thermal pad (tied to source internally) and bottom drain terminal pins compared to the preceding QFN 8x8 version. Table 2-1 compares the footprint and thermal pad area among TI's QFN and other popular surface-mount packages; TO Lead-Less (TOLL) and D^2PAK that are used for high-voltage GaN or silicon carbide (SiC) discrete devices. TI's QFN 12x12 has the largest exposed thermal pad area of 79mm^2 in comparison with competitors' packages. Although occupying more real estate on the printed circuit board (PCB) than the TOLL package, it possesses a greater effective area that can be used for heat dissipation through a bottom-side cooling system by showing 7% more thermal pad area over PCB footprint ratio.

Table 2-1. Footprint and Thermal Pad Area Comparison for Different Packages

MANUFACTURER	TI	TI	COMPETITOR A	COMPETITOR B
PACKAGE	QFN 8x8	QFN 12x12	TOLL 1	D^2PAK 2
Minimum footprint on PCB (mm^2)	64	144	116	165
Exposed thermal pad area (mm^2)	23	79	56	45
Thermal pad area / PCB footprint (%)	36	55	48	27

1. 600V GaN HEMT
2. 650V SiC MOSFET

3 Bottom-Side Cooling Configuration and Definition of $R_{\theta JC/P}$

3.1 Definition of $R_{\theta JC/P}$ for Package Thermal Performance

Two parallel heat flow paths from device junction to ambient are depicted in Figure 3-1 with a corresponding one-dimensional thermal resistance (R_θ) circuit model. Table 3-1 lists the descriptions for various R_θ parameters indicated in Figure 3-1 and discussed in this report. The bottom-side cooled QFN 12x12 package is designed to mainly dissipate heat from the mounting PCB through thermal interface material (TIM) and attached heatsink to ambient. Minimal heat is pulled away from package top to ambient in this typical bottom-side cooling configuration. The more efficient the bottom path is, the less power is dissipated from the top side. Therefore, $R_{\theta JA}$ for an efficient bottom-side cooled system can be estimated using Equation 1:

$$R_{\theta JA} \cong R_{\theta JC(bot)} + R_{\theta PCB} + R_{\theta TIM} + R_{\theta H/S} \quad (1)$$

$R_{\theta JC(bot\ or\ top)}$, defined as the thermal resistance between device junction and package surface used for heat removal, is universally reported in manufacturers' datasheet. However, using this parameter to compare package thermal performance directly is misleading under certain circumstances, especially among different types of packages. For example, the same 600-V Si MOSFET may have $R_{\theta JC(bot)}$ of 0.8 °C/W when packaged in D^2PAK but of 0.6 °C/W in QFN 8x8, because D^2PAK has a thicker Cu tab. This does **NOT** mean that thermally QFN 8x8 is a better package than D^2PAK. Though increasing the package thermal resistance $R_{\theta JC(bot)}$, thicker Cu tab used in D^2PAK package for die attachment can generate a more uniform heat distribution inside the package before heat flux reaches the PCB top Cu layer. Moreover, a larger thermal tab allows system designers to add more Cu pad area and thermal vias on PCB to reduce its thermal resistance. The $R_{\theta TIM}$ is lowered subsequently because of more effective heat spreading on PCB. Therefore, it is important that a well thermally-designed package could facilitate a better power dissipation capability at system level by improving the efficiency of existing cooling elements and/or enabling the use of more effective thermal solutions. For a bottom-side cooled, surface-mount package, its thermal performance is inevitably coupled to the mounting board (and attached TIM if used). To better define and compare thermal performance of different packages a practical indicator $R_{\theta JC/P}$ (i.e., thermal resistance from junction to major cooling plane) is used in the following sections, and is defined in Equation 2:

$$R_{\theta JC/P} = R_{\theta JC(bot)} + R_{\theta PCB} + R_{\theta TIM} \quad (2)$$

$R_{\theta H/S}$ or $R_{\theta Coldplate}$ is excluded from Equation 2 for this definition because it is independent of device package design and more a function of its own characteristics (e.g., material and structure) and other use conditions such as flow rate of air/coolant.

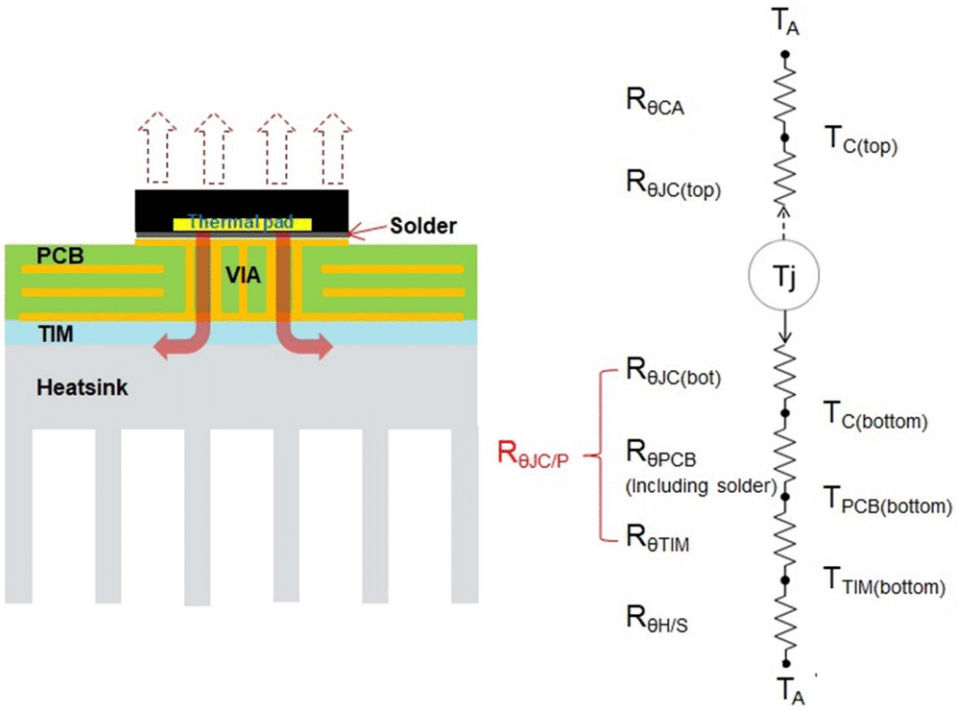


Figure 3-1. Typical Cooling Design for Surface-Mount Device with Bottom Thermal Pad

Table 3-1. List of Thermal Resistance (R_θ) Parameters, Unit (°C/W)

SYMBOL	DESCRIPTION
$R_{\theta JA}$	Junction-to-ambient thermal resistance
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance
$R_{\theta CA}$	Case-to-ambient thermal resistance
$R_{\theta JC/P}$	**Junction-to-cooling plane thermal resistance**
$R_{\theta PCB}$	Thermal resistance of PCB (including solder layer)
$R_{\theta TIM}$	Thermal resistance of thermal interface material (TIM)
$R_{\theta H/S}$	Thermal resistance of heatsink

3.2 Design Recommendations for Bottom-Side Cooling System

More details on how to optimize each cooling element in the system-level thermal design can be found in published application reports SNOAA14 and SNOA946. Some key points are summarized below:

- Use thick Cu (2 oz. recommended) for multilayer PCB to spread out heat and remove solder mask for bottom Cu heat spreading plane
- Design sufficient numbers of thermal vias to reduce $R_{\theta PCB}$ and fill vias by conductive epoxy or Cu if possible
- Use 1.6 mm or thinner PCB if applicable and apply proper pressure to prevent board warpage when clamping it to heatsink or coldplate
- Control thermal pad solder joint void percentage of less than 25% in total and 10% the largest
- Make careful tradeoffs between adding more Cu pad/thermal via coverage on PCB and the resultant extra parasitic capacitance and inductance
- Add cooling element on package top surface only as a supplement due to insufficient power dissipation from bottom side
- Select proper TIM and heatsink to meet overall $R_{\theta JA}$ thermal requirement

4 Simulation Models and Results

4.1 Finite Element Models for Thermal Analysis

Simulation models were built using ANSYS finite element analysis (FEA) software in order to compare thermal performance (i.e., $R_{\theta JC/P}$) of different surface-mount packages. Illustrations of four models including QFN 8x8, QFN 12x12, TOLL, and D^2PAK packages are shown in Figure 4-1. The former two QFN packages are implemented for TI's 600-V GaN power stage products while the latter two are used by competitors for their commercially released 600-V GaN and 650-V SiC discrete devices respectively. Each surface-mount device is placed on the center of a 4-layer PCB in 40-mm x 40-mm surface area and 1.58-mm thickness.

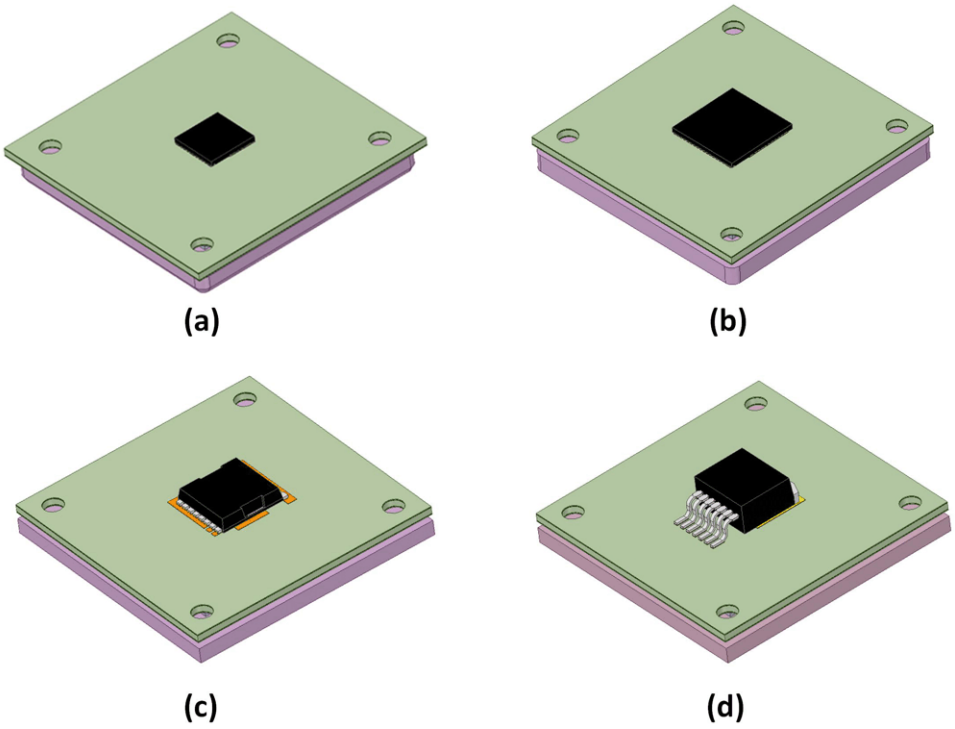


Figure 4-1. Simulation Models Built for Different Packages: (a) QFN 8x8, (b) QFN 12x12, (c) TOLL, and (d) D^2PAK

An example cross-sectional view of the generated model with a detailed description on the multilayer PCB structure is displayed in Figure 4-2. Most building elements including thermal via patten design (Figure 4-3) are the same for all built models except two items: PCB top Cu layer design and total numbers of thermal vias, which were adjusted to fit for the thermal pad area of each package for the purpose of a fair thermal performance comparison among different packages. Please note that the top Cu pad for heat spreading and the corresponding thermal via pattern/number can be further optimized for specific applications. Table 4-1 summarizes the key dimensional and thermal information for major modelling components.

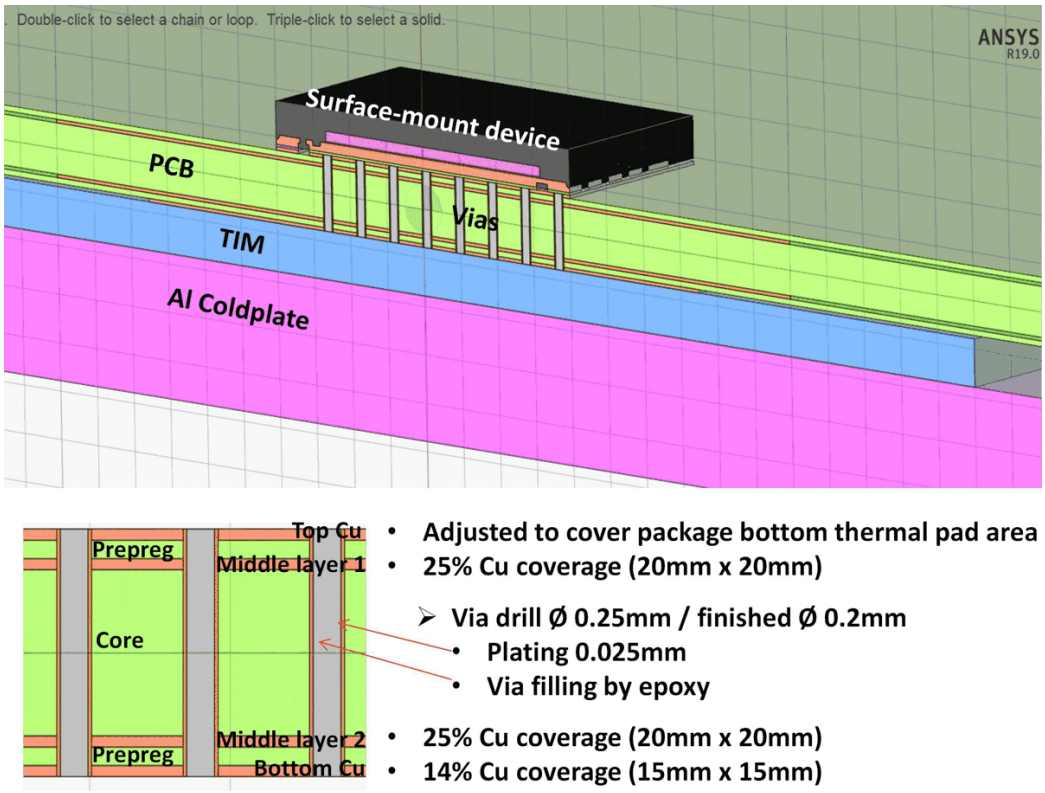


Figure 4-2. Cross-Section View of Simulation Model (QFN 8x8)

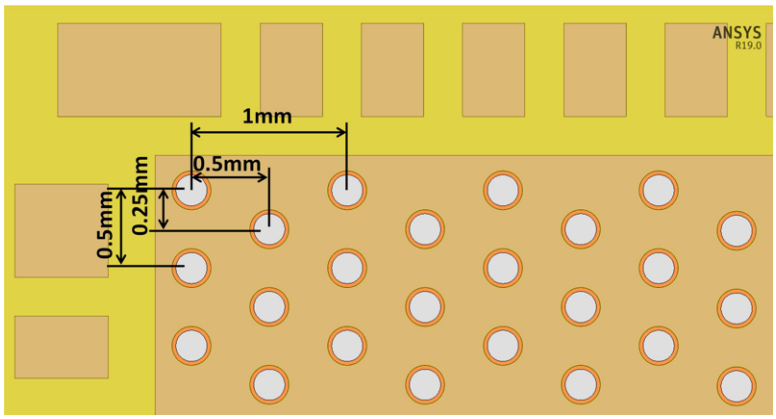


Figure 4-3. Thermal Via Pattern on PCB

Table 4-1. Properties of Simulation Model Components

COMPONENT	THICKNESS (mm)	MATERIAL	THERMAL CONDUCTIVITY (W/mK)
Solder	0.05	Lead-free solder	50
PCB	0.12 (prepreg)/1.06 (core)	FR4	0.3
	0.07 (4 layers)	Cu	385
Thermal Via	0.025	Cu plating	385
	0.2 (diameter)	Epoxy via filling	1
TIM	1	Gap filler pad	8
Coldplate	2.5	Aluminum alloy	160

4.2 Thermal Simulation Results

The steady-state FEA thermal simulations were performed with a loss dissipation of 10 W applied on the power device and a constant temperature of 30 °C set on coldplate. It was assumed that the heat generated by device only transfers downward to the coldplate through conduction and there is no heat removal by convection or radiation mechanisms in this thermal model. The system temperature distributions of all investigated package models are illustrated in Figure 4-4. The temperature at different nodes shown in the R_{θ} circuit model (Figure 3-1) can be obtained from these simulation results and used for thermal resistance calculation between different nodes. For example, the $R_{\theta JC/P}$ was calculated using the Equation 3 shown below:

$$R_{\theta JC/P} = (T_J - T_{C/P}) / \text{Power} \quad (3)$$

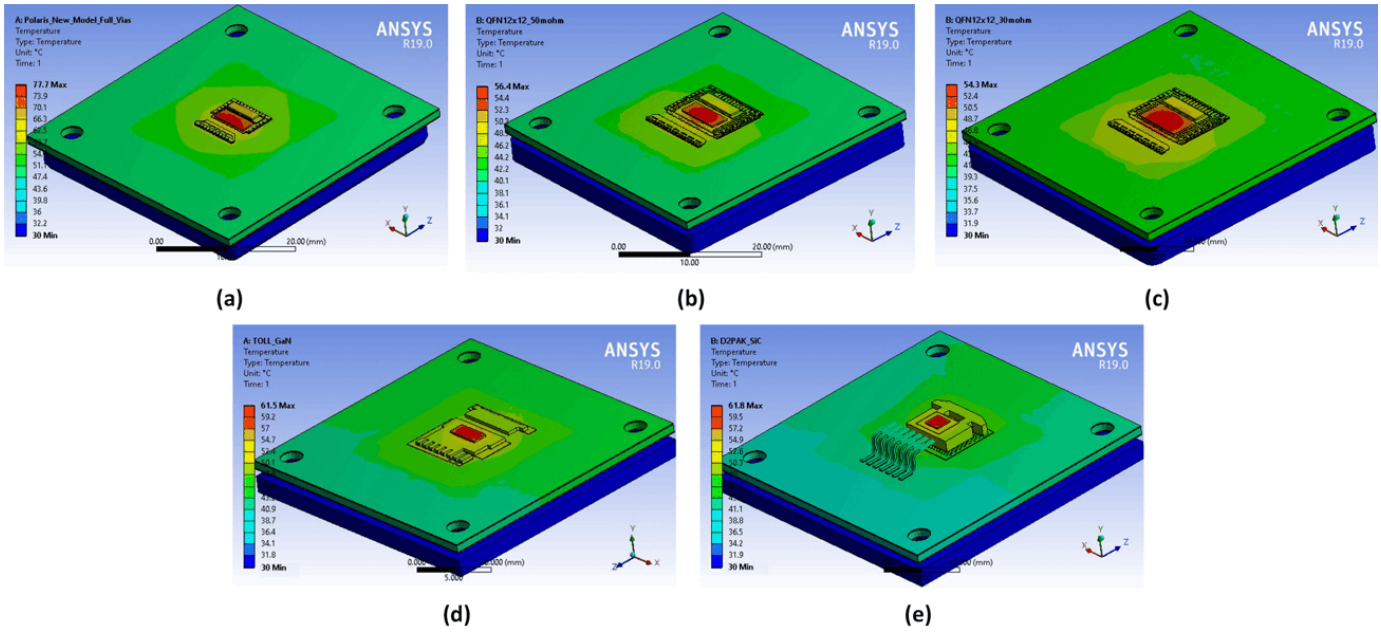


Figure 4-4. Simulation Results of Temperature Distribution for Different Packages: (a) QFN 8x8, (b) QFN 12x12 (50 mΩ), (c) QFN 12x12 (30 mΩ), (d) TOLL, and (e) D²PAK

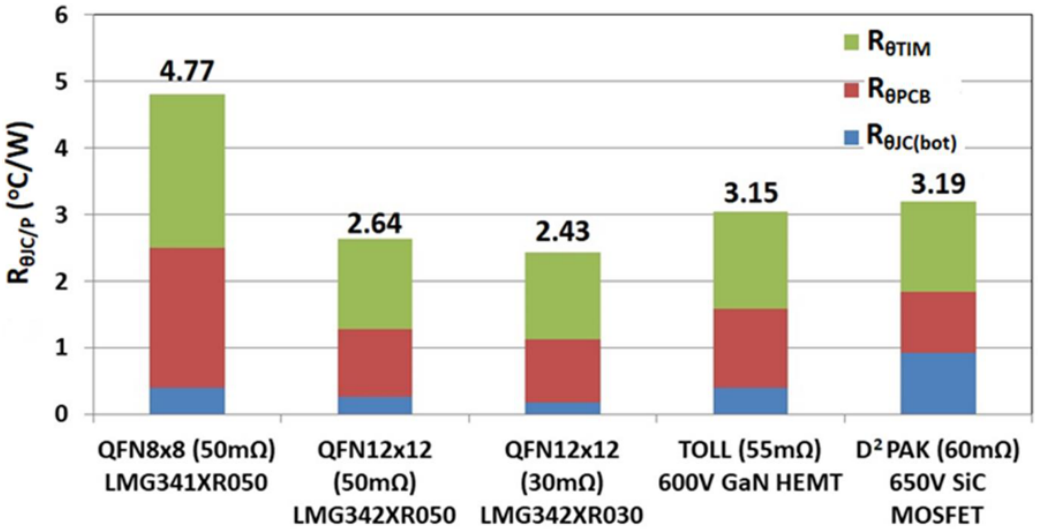
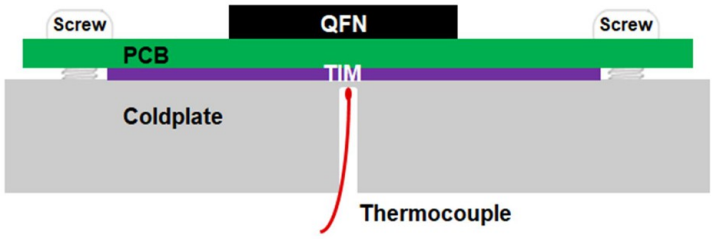


Figure 4-5. Comparison of R_θ Simulation Results for Different Surface-Mount Packages

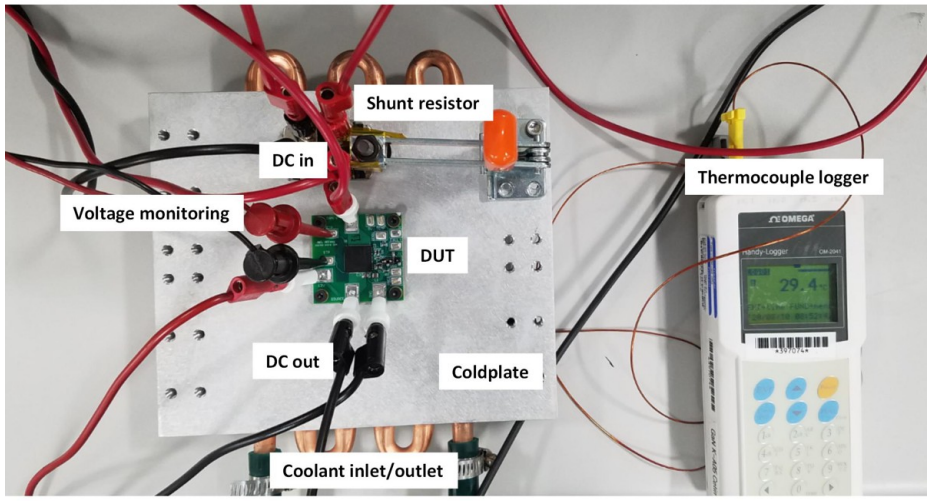
Based on the thermal simulation results, Figure 4-5 presents the calculated $R_{\theta JC/P}$ values for different products packaged in various formats. It is clearly demonstrated that for the same 50-mΩ on-resistance device the $R_{\theta JC/P}$ of QFN 12x12 package (2.64 °C/W) decreases more than 40% compared to that of QFN 8x8 package (4.77 °C/W). The 30-mΩ device in the same QFN 12x12 package performs slightly better than the 50-mΩ one mainly because the die size is larger for the lower on-resistance device. From the R_θ breakdown analysis also shown in Figure 4-5, it can be observed that the reduction of $R_{\theta JC/P}$ for QFN 12x12 package compared to its QFN 8x8 predecessor is mostly attributed to the decrease of $R_{\theta PCB}$ and $R_{\theta TIM}$. Such thermal performance improvement is realized by taking advantage of its larger thermal pad and package size which enables the use of a thermally more effective Cu mounting pad and more thermal vias in PCB design. Comparing with other bottom-side cooled, surface-mount packages (i.e., TOLL and D^2PAK) used for discrete power devices, QFN 12x12 package has a lower $R_{\theta JC/P}$ by about 16%, showing its thermal advantage.

5 Experimental Setup and $R_{\theta JC/P}$ Testing Results

To verify the thermal simulation results, a test bench setup for thermal resistance measurement has been designed and implemented. The 30-mΩ device in the QFN 12x12 package (LMG342xR030) was selected to investigate the consistency between simulation and experiment results. Following the simulation model construction design, a 4-layer PCB for thermal testing was populated and a LMG342xR030 unit was mounted on the center of it. It is exhibited in Figure 5-1 that the testing vehicle was pressed on a machined coldplate (Hi-Contact 6-Pass, Aavid) under approximately 20-psi pressure provided by mounting screws on four corners of the board. A 1-mm-thick gap filler pad TIM (GR80A, Fujipoly) was inserted between the exposed PCB bottom Cu pad and the coldplate which is connected to a chiller unit (6560M, PolyScience) with a running liquid coolant of 30 °C. For measuring the cooling plane temperature ($T_{C/P}$), a thermocouple tip was placed 2 mm underneath the top surface of coldplate through a drilled 2.5-mm-diameter blind hole. $T_{C/P}$ was read and recorded by a data logger (OM-2041, Omega). To generate a controlled loss inside the package, direct current was used to heat the device junction, and the dissipated power was calculated by voltage and current measured across the testing unit.



(a)



(b)

Figure 5-1. Experimental Setup for R_θ Measurement: (a) Cross-Section Illustration and (b) Top-View Photo

As a temperature sensitive parameter, the on-resistance ($R_{DS,ON}$) of monitored device was utilized to calculate junction temperature (T_J) in thermal resistance measurement. Before testing, the $R_{DS,ON}$ – T_J correlation of the testing unit was calibrated inside a thermal chamber (107, TestEquity) where the device junction was passively heated by the temperature controlled environment. Active heating of the junction was minimized owing to the small measuring current of only 80-100 mA. An example calibration curve with a fitting equation for the measured temperature range of 25-125 °C is presented in Figure 5-2. Another method to estimate T_J is to use an infra-red (IR) thermal camera to directly measure the hot spot on top of the package during testing. As mentioned in Definition of $R_{\theta JC/P}$ for Package Thermal Performance, very minimal heat is dissipated from the package top side in an efficient bottom-side cooling system. The measured top case temperature is therefore very close to device T_J.

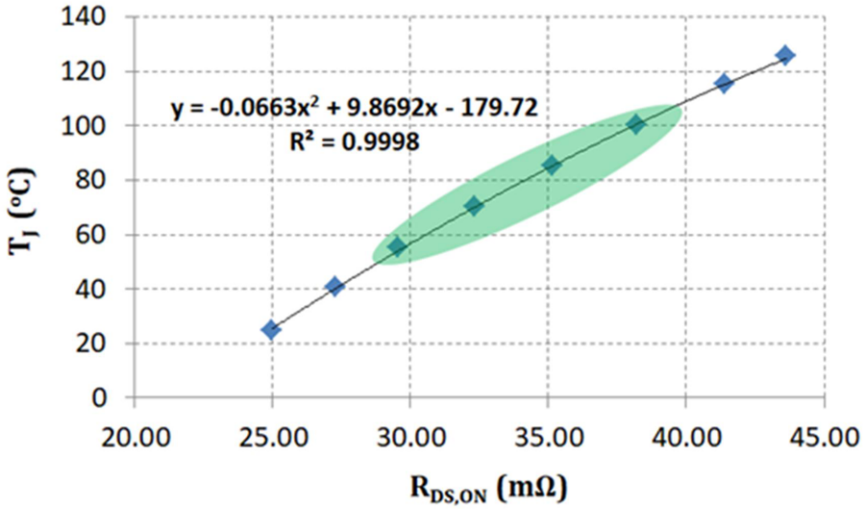


Figure 5-2. Calibration Curve for $R_{DS,ON}$ and T_J Correlation

Figure 5-3 shows the measured maximum top case temperature of a LMG342xR030 device tested under different dissipated powers. The testing results of $R_{\theta JC/P}$ calculated from both $R_{DS,ON}$ – T_J correlation and IR measurement are summarized in Figure 5-4 . There is no distinctive difference of $R_{\theta JC/P}$ results obtained from two methods under three different tested power levels. Furthermore, a satisfactory agreement (< 8% discrepancy) between simulation and experiment results is also noticed, which verifies the thermal simulation results for package competitive analysis described in Figure 4-5. Explanations for the slightly higher $R_{\theta JC/P}$ from measurement could be the imperfections of the testing vehicle and setup which are not considered in the simulation model, such as barrel cracking of the PCB thermal vias, solder void in the joint layer between device thermal pad and PCB mounting area, and uneven pressure applied on TIM.

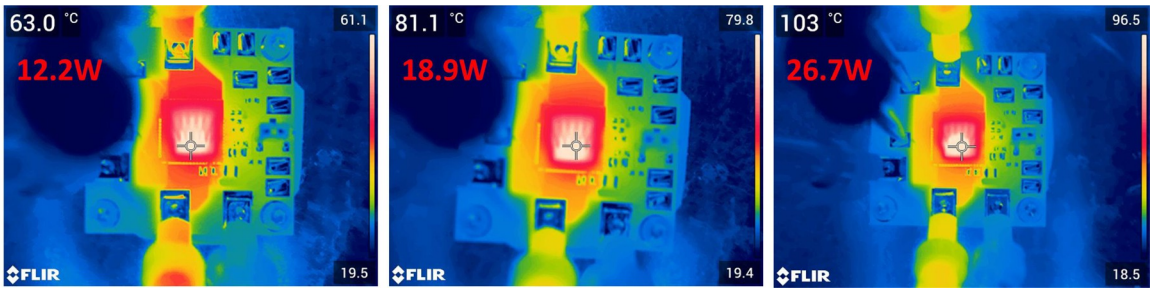


Figure 5-3. IR Thermal Images for QFN 12x12 Unit Tested on Different Power Levels

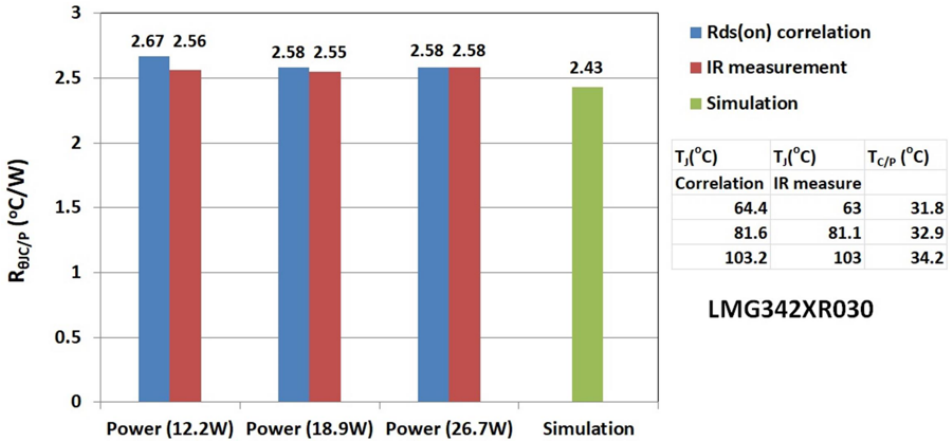


Figure 5-4. Experimental Results of $R_{\theta JC/P}$ Tested on Different Power Levels

As indicated in Figure 4-5, the $R_{\theta TIM}$ contributes more than 40% of $R_{\theta JC/P}$ for the investigated cooling system, which is critical for the overall system thermal performance ($R_{\theta JA}$) in real applications. However, the thermal conductivity of TIM published in datasheet by different manufacturers is difficult to use for material down-select because they are not always measured using the same methodology. Therefore, a bench testing is preferably needed to choose a proper TIM to be used in the system. Different TIMs were tested in this reported work using the same experimental setup so as to compare their thermal characteristics. The testing results and other related information were summarized in Table 5-1. It is demonstrated that using the same TIM (GR80A) in a thinner format (0.5 mm) or a more thermally conductive TIM (GR130A) from the same manufacturer can effectively reduce the $R_{\theta JC/P}$. TIM A material obtained from another vendor shows similar thermal performance as the benchmark GR80A TIM but has a lower thermal conductivity reported in its datasheet, while TIM B material lists a high thermal conductivity of 20 W/mK but its performance is equivalent to GR130A TIM with claimed 13 W/mK thermal conductivity. Adhesive tape is another commonly used TIM which does not require additional clamping force to secure the cooling elements on the PCB or other heated surfaces after initial installation. This material is cheaper but its thermal resistance is higher compared to gap filler pad TIM. The testing result for TIM C listed in Table 5-1 is given as an example. The measured $R_{\theta JC/P}$ using tape TIM is considerably higher than that using the gap filler pad TIM, which is much thicker.

Table 5-1. Summary of $R_{\theta JC/P}$ Results Using Different TIMs

PRODUCT	TYPE	THICKNESS (mm)	THERMAL CONDUCTIVITY (W/mk) on DATASHEET	COST	$R_{\theta JC/P}$ (°C/W)
GR80A	Gap filler pad	1	8	x1	2.58
GR80A	Gap filler pad	0.5	8	X0.7	2.33
GR130A	Gap filler pad	1	13	x3	2.21
TIM A	Gap filler pad	1	7.5	X1.1	2.60
TIM B	Gap filler pad	1	20	X2	2.26
TIM C	Tape	0.25	1.2	x0.07	5.72

6 Thermal Performance of QFN 12x12 Package on Half-Bridge Evaluation Board

An evaluation board (LMG3422EVM-043) incorporating all design tradeoffs was built consisting of two LMG3422R030 devices configured in half-bridge topology. A 35-mm x 50-mm x 20-mm elliptical fin heatsink (UB3550-20B, Alpha Novatech) and a 12-V, 1.68-W DC fan (F-3010H12BIII-16, Cofan) were selected to cool the system. Using four sets of push-pins and springs, a constant 20-psi pressure was applied to press the heatsink onto the back side of PCB with a 0.5-mm-thick gap filler pad TIM (GR80A, Fujipoly) in between.

The test was setup in a synchronous buckconverter configuration, with 400-V bus voltage, 20-A output current and power level at 4 kW. The test waveform is shown in Figure 6-1, with green waveform being the inductor current and pink waveform being the switching node voltage. As the zoomed-in waveform presented in Figure 6-2 , the active GaN device has turn-on speed of over 120 V/ns with maximum speed of 150 V/ns benefiting from the minimized common-source inductance of this integrated package. Moreover, the optimized power loop allows the overshoot voltage to be less than 50 V in this test at such high switching speed. The thermal performance of the system was measured under this operating condition with the DC fan directly being attached on and blowing air to the heatsink. IR thermal image (Figure 6-3) shows the QFN 12x12 package case temperature of 99.3 °C which stays well below the maximum operating temperature (125 °C) recommended for this LMG3422R030 GaN power stage product. The measured $R_{\theta JA}$ is 3.8 °C/W for this bottom-side cooling system.

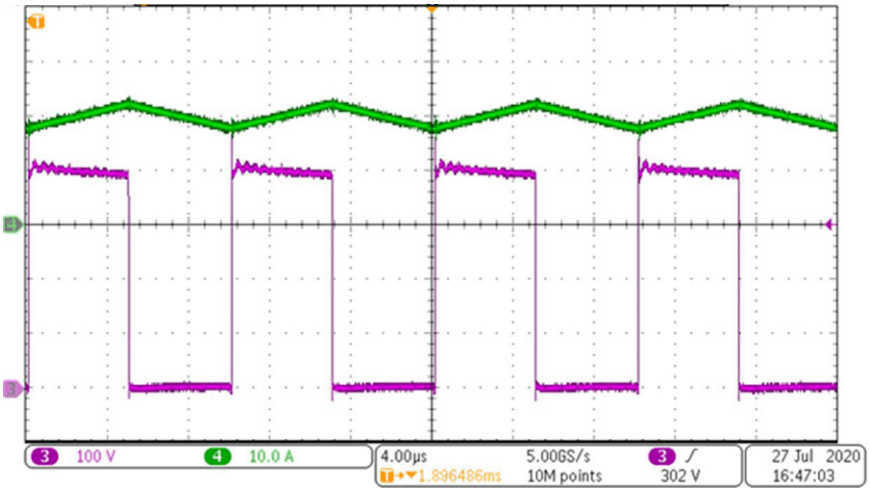


Figure 6-1. Power Stage Testing Waveform of LMG3422EVM-043

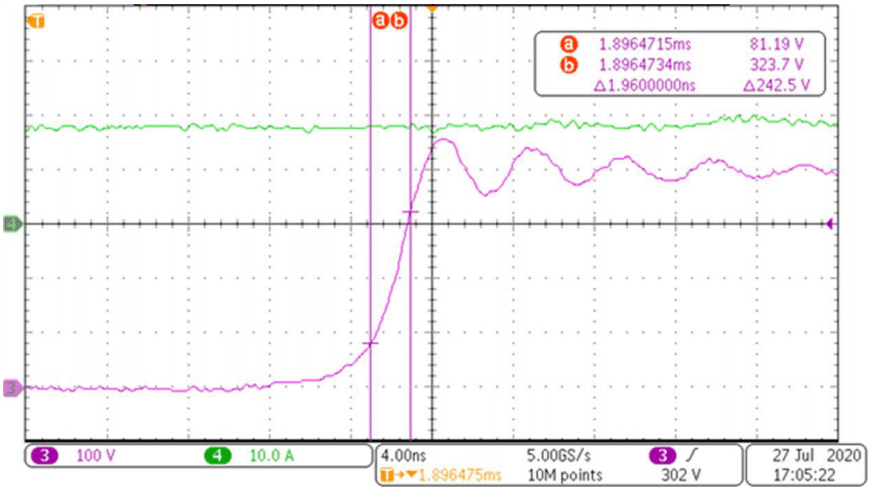


Figure 6-2. Zoomed-In Waveform at Switching Node

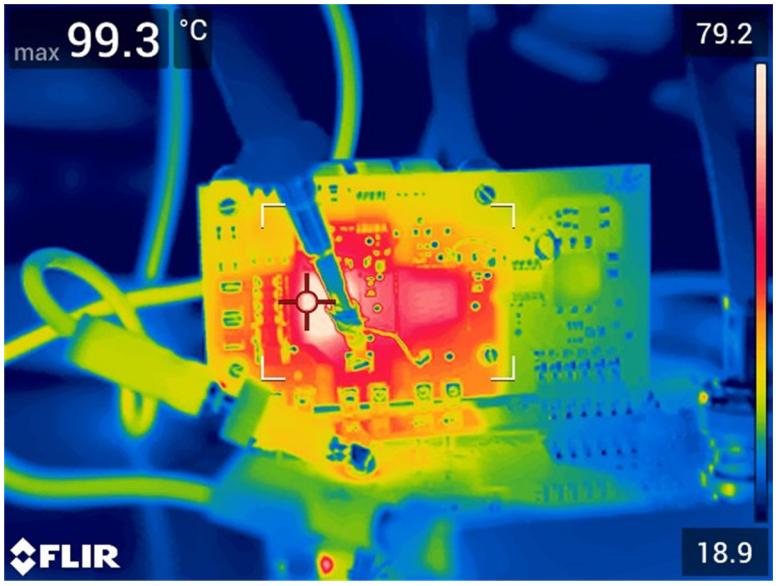


Figure 6-3. IR Thermal Image for EVM Under Testing

7 Summary

Package thermal performance of power devices is equally important as its mechanical and electrical characteristics impacting system efficiency, reliability, and power density. In power applications where the heat dissipation is the utmost requirement, it becomes even more critical for market adoption. The simulation results have demonstrated that $R_{\theta JC/P}$ value of TI's new QFN 12x12 package is 45% lower than that of its previous QFN 8x8 package for the same 50-mΩ product. Additionally, TI's 50-mΩ GaN power stage in QFN 12x12 package shows about 16% less $R_{\theta JC/P}$ than competitors' 600-V and 650-V discrete devices of similar on-resistance enclosed in a TOLL or D^2PAK package. Experimental testing results show less than 8% difference from simulation outcomes. A particular use case was presented based on a half-bridge design using LMG3422R030 devices. The synchronous buck converter running at 4-kW power was demonstrated with a measured case temperature of 99.3 °C on top of the high-side device package. While switching at high speed and high frequency with integrated protections, TI's high-voltage GaN power stages in the new QFN 12x12 package can release more power out of this wide-bandgap semiconductor for applications requiring system-size reduction and power-density, power-efficiency enhancement.

8 References

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (February 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265