82C284/883

Clock Generator and Ready Interface for 80C286 Processors

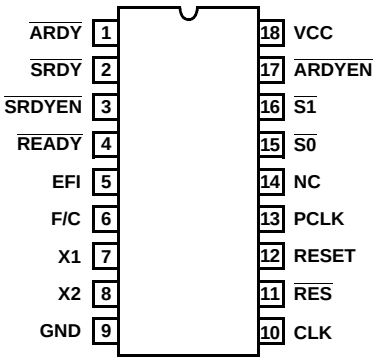
March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Generates System Clock for 80C286 Processors**
- **Generates System Reset Output from Schmitt Trigger Input**
  - **Improved Hysteresis**
- **Uses Crystal or External Signal for Frequency Source**
  - **Dynamically Switchable Between Two Input Frequencies**
- **Provides Local $\overline{\text{READY}}$ and MULTIBUS™ $\overline{\text{READY}}$ Synchronization**
- **Static CMOS Technology**
- **Single +5V Power Supply**
- **Available in 18 Lead CERDIP Package**

Pinout

82C284/883
(CERDIP)
TOP VIEW



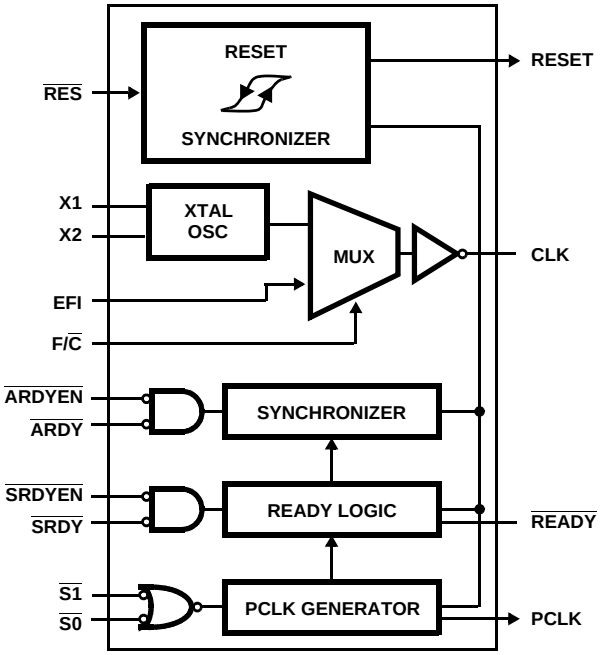
Description

The Intersil 82C284/883 is a clock generator/driver which provides clock signals for 80C286 processors and support components. It also contains logic to supply READY to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
MD82C284-12/883	-55^{o}C to +125^{o}C	CERDIP	F18.3

Functional Diagram



FN2968.1

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied. . . . . GND -0.1V to VCC +1.0V
ESD Classification . . . . . Class 2

Thermal Information

Thermal Resistance	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
CERDIP Package	80	20

Gate Count . . . . . 200 Gates
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C
Junction Temperature . . . . . +175^{o}C
Lead Temperature (Soldering 10s) . . . . . +300^{o}C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Temperature Range. . . . . -55^{o}C to +125^{o}C
Operating Supply Voltage. . . . . +4.5V to +5.5V
EFI Rise Time (From 0.8V to 3.2V). . . . . 8ns (Max)
EFI Fall Time (From 3.2V to 0.8V) . . . . . 8ns (Max)

TABLE 1. 82C284/883 D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-	0.8	V
Input HIGH Voltage	VIH	VCC = 5.5V	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	2.2	-	V
EFI, F/$\overline{C}$ Input High Voltage	VIHC	VCC = 5.5V	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	3.2	-	V
$\overline{RES}$ HIGH Voltage	VIHR	VCC = 5.5V	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	VCC -0.8	-	V
$\overline{RES}$ Input Hysteresis	VHYS	VCC = 5.5V	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	0.5	-	V
RESET, PCLK Output LOW Voltage	VOL	IOL = 5mA, VCC = 4.5V, Note 2	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-	0.4	V
RESET, PCLK Output Voltage	VOH	IOH = -1mA, VCC = 4.5V, Note 2	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	VCC -0.4	-	V
$\overline{READY}$ Output LOW Voltage	VOLR	IOH = 10mA, VCC = 4.55V, Note 2	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-	0.4	V
CLK Output LOW Voltage	VOLC	IOL = 5mA, VCC = 4.5V, Note 2	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-	0.4	V
CLK Output HIGH Voltage	VOHC	IOH = -5mA, VCC = 4.5V, Note 2	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	VCC -0.4	-	V
Input Leakage Current	II	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-10	10	µA
Active Power Supply Current	ICCOP	82C284-10/883, Note 1	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-	48	mA
		82C284-12/883, Note 1	1, 2, 3	-55^{o}C ≤ T_A ≤ +125^{o}C	-	60	mA

NOTES:

1. ICCOP measured at 10MHz for the 82C284-10/883 and at 12.5MHz for the 82C284-12/883. VIN = GND or VCC, VCC = 5.5V, outputs unloaded.
2. Interchanging of force and sense conditions is permitted.

TABLE 2. 82C284/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested. A.C. timings are referenced to 0.8V and 2.0V points of the signals as illustrated in datasheet waveforms, unless otherwise specified.

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	
EFI LOW Time	t1	At VCC/2, Note 8	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	20	-	16	-	ns
EFI HIGH Time	t2	At VCC/2, Note 8	9, 10, 11	-55^{o}C ≤ T_A ≤ +125^{o}C	20	-	20	-	ns

TABLE 2. 82C284/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested. A.C. timings are referenced to 0.8V and 2.0V points of the signals as illustrated in datasheet waveforms, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	
Status Setup Time for Status Going Active	t5A		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	18	-	ns
Status Setup Time for Going Inactive	t5B		9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	16	-	ns
Status Hold Time	t6		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	1	-	ns
F/$\overline{C}$ Setup Time	t7		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
F/$\overline{C}$ Hold Time	t8		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	t9		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	15	-	ns
$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	t10		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	-	2	-	ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	t11	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	t12	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	25	-	ns
$\overline{RES}$ Setup Time	t13	Notes 3, 7	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	18	-	ns
$\overline{RES}$ Hold Time	t14	Notes 3, 7	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	8	-	ns
CLK Period	t16		9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	40	-	ns
CLK LOW Period	t17	Notes 2, 6	9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	11	-	ns
CLK HIGH Time	t18	Notes 2, 6	9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	13	-	ns
$\overline{READY}$ Inactive Delay	t21	At 0.8V, Note 4, Test Condition 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
$\overline{READY}$ Active Delay	t22	At 0.8V, Note 4	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	24	-	18	ns
PCLK Delay	t23	CL = 75pF, Test Condition 1	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	20	-	16	ns
RESET Delay	t24	CL = 75pF, Test Condition 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	27	-	26	ns
PCLK LOW Time	t25	CL = 75pF, Note 5	9, 10, 11	$-55^oC \le T_A \le +125^oC$	t16-10	-	t16-10	-	ns
PCLK HIGH Time	t26	CL = 75pF, Note 5	9, 10, 11	$-55^oC \le T_A \le +125^oC$	t16-10	-	t16-10	-	ns

TABLE 2. 82C284/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested. A.C. timings are referenced to 0.8V and 2.0V points of the signals as illustrated in datasheet waveforms, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	

NOTES:

1. VCC = 4.5V and 5.5V unless otherwise specified. CLK loading: CL = 100pF.
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t1 and t2. The recommended crystal loading for CLK frequencies of 8MHz to 20MHz are 25pF from pin X1 to GND, and 15pF from pin X2 to GND; for CLK frequencies from 20MHz to 25MHz the recommended loading is 15pF from pin X1 to GND, and 15pF from X2 to GND. These recommended values are ±5pF and include all stray capacitance. Decouple VCC and GND as close to the 80C284/883 as possible.
3. This is an asychronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
4. The pull-up resistor value for the $\overline{\text{READY}}$ pin is 620Ω with the rated 150pF load.
5. t16 refers to any allowable CLK period.
6. When using a crystal with the recommended capacitive loading, CLK output HIGH and LOW times are guaranteed to meet 80C286 requirements.
7. Measured from 1.0V on the CLK to 0.8V on the $\overline{\text{RES}}$ waveform for $\overline{\text{RES}}$ active, and to 4.2V on the $\overline{\text{RES}}$ waveform for $\overline{\text{RES}}$ inactive.
8. Input test waveform characteristics: VIL= 0.0V, VIH = 4.5V.

TABLE 3. 82C284/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	10MHz		12MHz		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	CIN	FREQ = 1MHz, All measurements are referenced to device GND	1	$T_A = +25^oC$	-	10	-	10	pF
EFI HIGH to CLK LOW Delay	t15A		1, 2	$-55^oC \le T_A \le +125^oC$	-	30	-	25	ns
EFI LOW to CLK HIGH Delay	t15B		1, 3	$-55^oC \le T_A \le +125^oC$	-	35	-	30	ns
CLK Rise Time	t19	1.0V to 3.6V, CL = 100pF	1	$-55^oC \le T_A \le +125^oC$	-	8	-	8	ns
CLK Fall Time	t20	3.6V to 1.0V, CL = 100pF	1	$-55^oC \le T_A \le +125^oC$	-	8	-	8	ns
X1 HIGH to CLK	t27		1, 4	$-55^oC \le T_A \le +125^oC$	-	35	-	30	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Measured from 3.2V on the EFI waveform to 1.0V on the CLK.
3. Measured from 0.8V on the EFI waveform to 3.6V on the CLK.
4. Measured from 3.6V on the X1 input to 3.6V on the CLK.

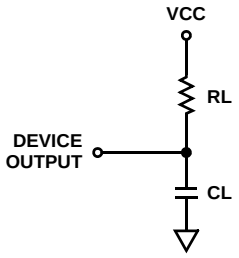
TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

A.C. Test Conditions



TEST CONDITION	RL	CL
1	750Ω	75pF
2	620Ω	150pF
3	∞	75pF

A.C. Specifications

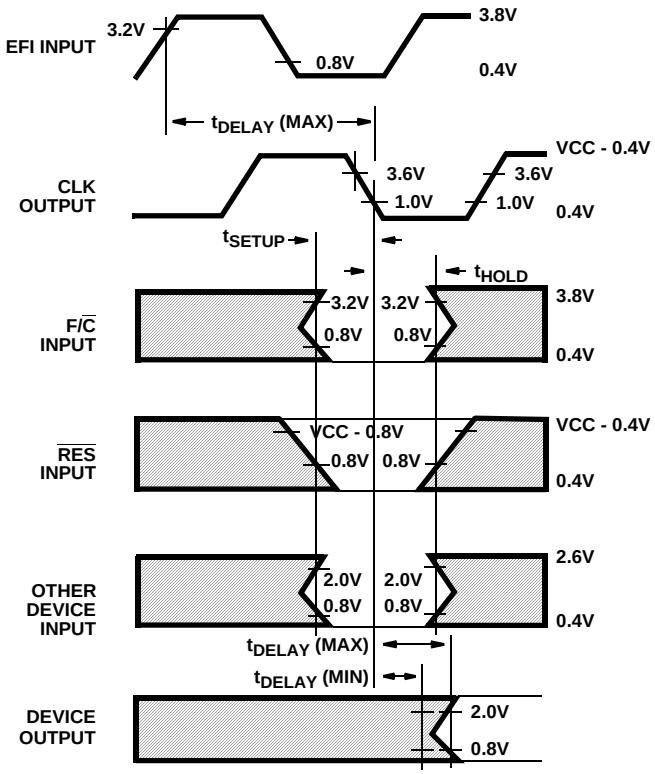


FIGURE 1. A.C. DRIVE, SETUP, HOLD AND DELAY TIME MEASUREMENT POINTS

Timing Waveforms

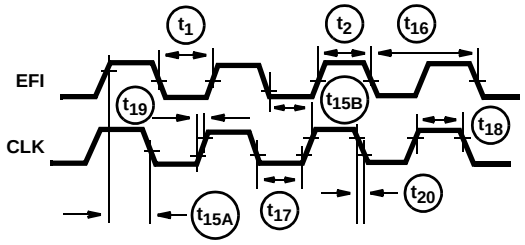
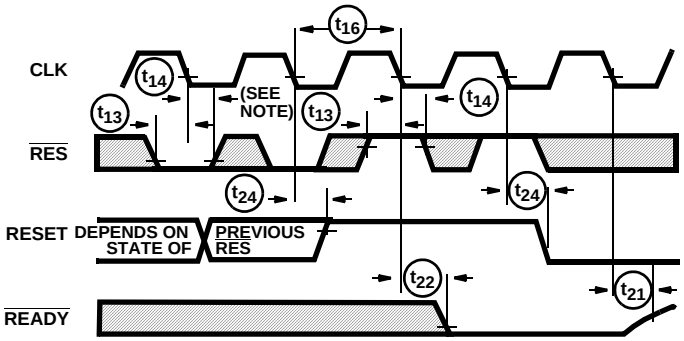


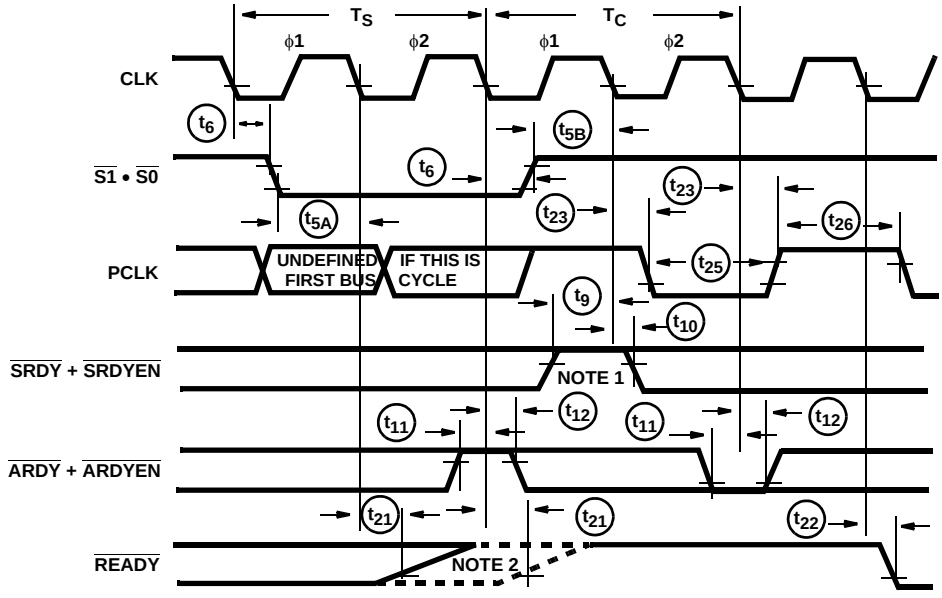
FIGURE 2. CLK AS A FUNCTION OF EFI

NOTE: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.



NOTE: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

FIGURE 3. RESET AND $\overline{\text{READY}}$ TIMING AS A FUNCTION OF $\overline{\text{RES}}$ WITH $\overline{\text{S1}}$, $\overline{\text{S0}}$, $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ AND $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ HIGH



NOTES:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ or $\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ are active before and/or during the first bus cycle after RESET, $\overline{\text{READY}}$ may not be deasserted until the falling edge of $\phi 2$ of T_S.

FIGURE 4. $\overline{\text{READY}}$ AND PCLK TIMING WITH $\overline{\text{RES}}$ HIGH

Timing Waveforms (Continued)

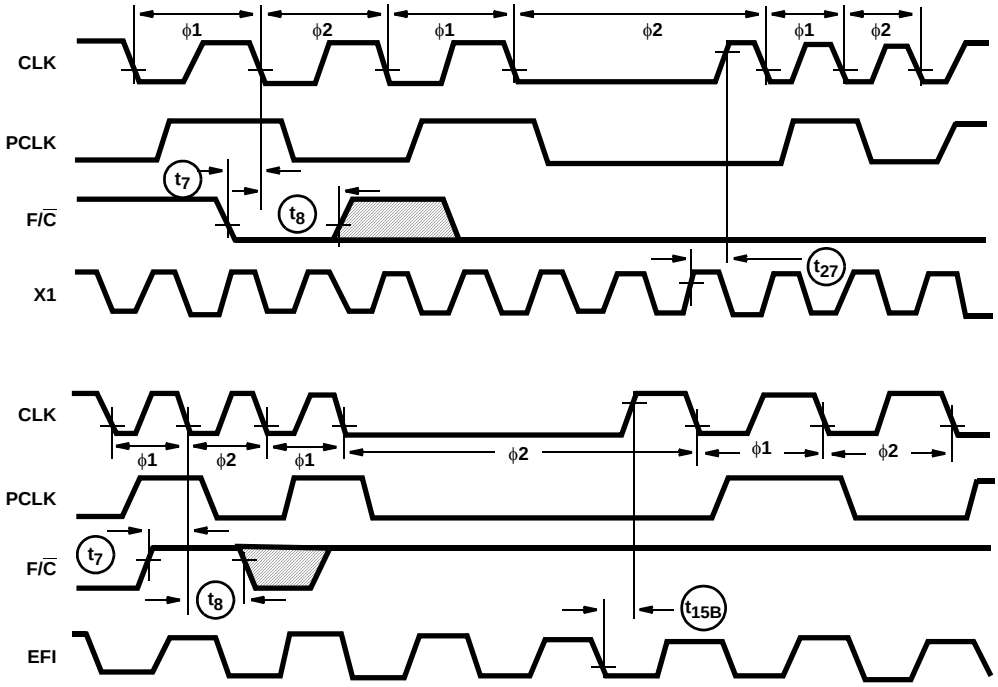
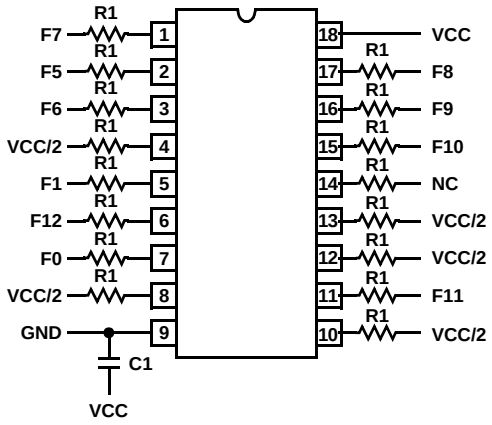


FIGURE 5. CLK AS A FUNCTION OF F/C, PCLK, X1, AND EFI DURING DYNAMIC FREQUENCY SWITCHING

NOTE: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

Burn-In Circuit

18 LEAD CERDIP



NOTES:

1. Supply Voltage: VCC = 5.5V, ±0.5V, GND = 0V. Driver Voltage: VIH = 4.5V ± 10%, VIL = 0V
2. Input Voltage Limits: VIL (Max) = 0.4V, VIH (Min) = 2.6V
3. Component Values: R1 = 47kΩ, C1 = 0.1μF (Min)
4. Oven type and frequency requirements microtest, F0 through F12.
5. Approximate current per unit. ICC = 0.3mA.
6. Special requirements:
   (a) Electrostatic Discharge Sensitive. Proper precautions must be used when handling units.
   (b) All power supplies must be at zero volts when the boards are inserted into the ovens. After insertion, apply VCC first, then activate the driver power supplies.
7. Oscilloscope measurements: To be on loaded boards before insertion into the oven.

Die Characteristics

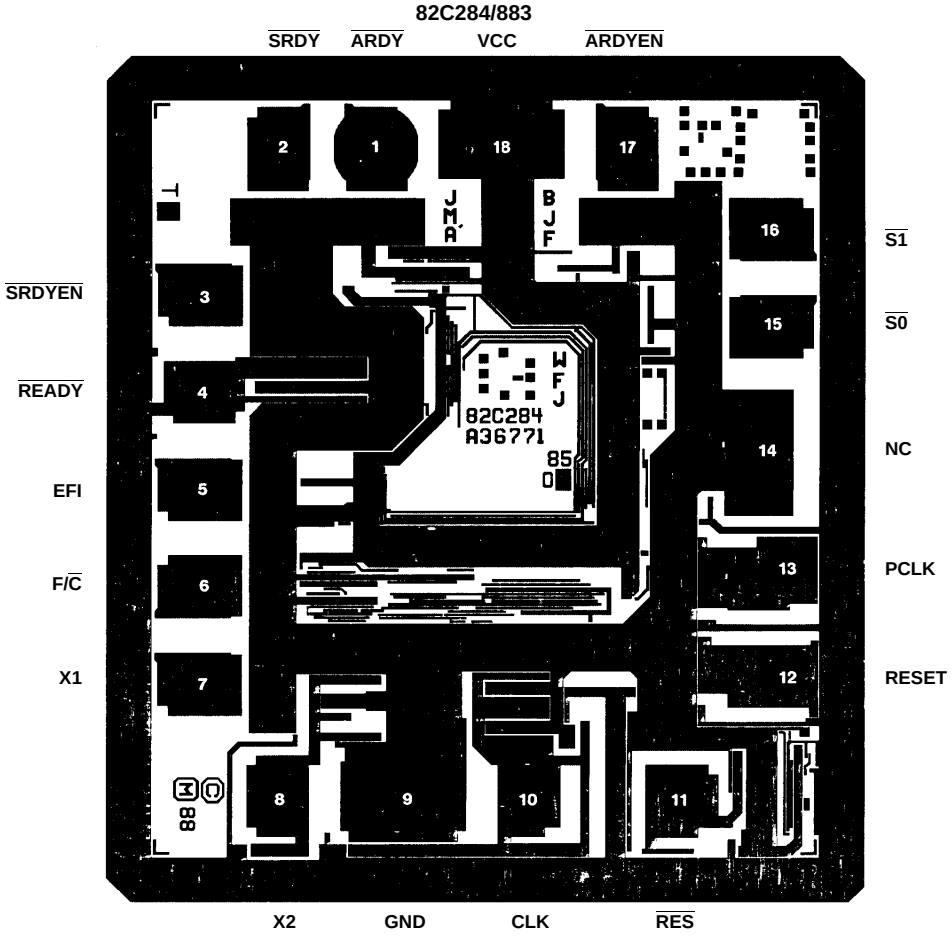
DIE DIMENSIONS:
63 mils x 69 mils x 19 mils ± 1 mil

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2

Metallization Mask Layout



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