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CMIS 310
HOMEWORK #5 – Week #5

This homework is worth 10% of your course grade.

Read each problem carefully. Failure to follow the instructions for a problem will result in a zero score for that problem.

Submit the completed Homework via Assignment in LEO.

1. Do Exercise 2 in Chapter 6 (Memory) of Null and Lobur

   Suppose a computer using direct mapped cache has 2^32 words of main memory and a cache of 1024 blocks, where each cache block contains 32 words.

   a. How many blocks of main memory are there?

      32 = 2^5. 2^32 (words in main) /2^5 (words per block) = **2^27 blocks**

   b. What is the format of a memory address as seen by the cache, that is, what are the sizes of the tag, block, and word fields?

      Total address is 32 bits (main memory). **Word is 5 bits (2^5 = 32 words per block). Block is 10 bits (2^10 is 1024 blocks). The tag is the rest of the 17 Bits (32 - 5 - 10 = 17).**

   c. To which cache block will the memory reference $000063FA_{16}$ map? 000063FA = 0000 0000 0000 0000 0110 0011 1111 1010**.** First 5 bits are the word field (11010). Then the next 10 bits are the block field (1100011111_2) which is **block 799**

2. Do Exercise 4 in Chapter 6 (Memory) of Null and Lobur

   Suppose a computer using fully associative cache has 2^24 words of main memory and a cache of 128 blocks, where each cache block contains 64 words.

   a. How many blocks of main memory are there?

      2^6 = 64. 2^24 (words in main memory) / 2^6 (words per block)= **2^18 blocks of main memory**

   b. What is the format of a memory address as seen by the cache, that is, what are the sizes of the tag and word fields?

24 bits for the address with 6 bits for the word and the rest 18 for the tag (in the opposite order of tag|word)

c. To which cache block will the memory reference 01D87216 map?

There is no block field for fully associative mapping technique so it can be mapped to any block

3. Do Exercise 6 in Chapter 6 (Memory) of Null and Lobur

A 2-way set associative cache consists of four sets. Main memory contains 2K blocks of eight words each.

a. Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.

There is the tag, set, and word fields for this mapping technique. Total address bits are 14 bits (2^1*2^10*2^3 = 2^14). Set = 2 bits (2^2 = 4). Word = 3 bits (2^3 = 8). The rest 9 bits are the tag (14-3-2 = 9).

b. Compute the hit ratio for a program that loops 3 times from locations 8 to 51 in main memory. You may leave the hit ratio in terms of a fraction.

Hit rate = hits/hits+misses. 8 Blocks of 8 words: 8-15, 16-23, 24-31, 32-39, 40-47, 48-51.

ITERATION 1:
Block start 8, 16, 24 would be initial miss (empty way 0) then 7 hits in set 1-3 (respectively).
Block start 32 would be initial miss (empty way 1) then 7 hits in set 0 (since block 0-7 would occupy way 0).
Block 40 would be initial miss (empty way 1) then 7 hits in set 1.
Block start 48 would be initial miss (empty way 1) then 3 hits (49, 50, 51) into set 2. Iteration 1 had 6 misses and 38 hits (7*5 + 3).

ITERATION 2 and 3:
Block start 8, 16, 24, 32, 40, 49 would hits 8 in set 0-4 since they are there already.
Each iteration would have 0 misses and 44 hits (5 blocks *8 hits per block + 4 hits for 48-51 block)

Total misses: 6
Total hits: 38+44+44 = 126
Hit Ration: 126/132

4. Do Exercise 8 in Chapter 6 (Memory) of Null and Lobur

   Suppose a computer using set associative cache has 2^21 words of main memory and a cache of 64 blocks, where each cache block contains 4 words.

   a. If this cache is 2-way set associative, what is the format of a memory address as seen by the cache, that is, what are the sizes of the tag, set, and word fields?

      There is the tag, set and word fields for 2-way set associative mapping technique. Total address bits are 21 bits. Set field is 5 bits (2^6 (cache blocks) / 2^1 (2 sets each)). Word field is 2 bits (2^2 = 4 words per block). Tag field is the rest 14 bits

   b. If this cache is 4-way set associative, what is the format of a memory address as seen by the cache?

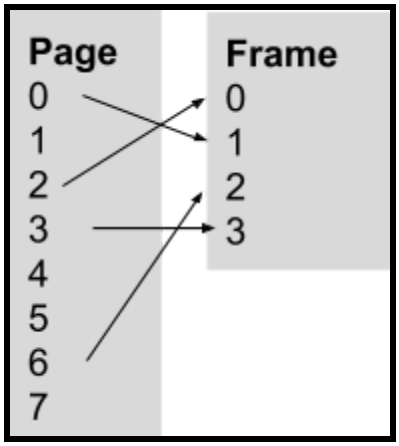
      There is the tag, set and word fields for 4-way set associative mapping technique. Total address bits are 21 bits. Set field is 4 bits (2^6 (cache blocks) / 2^2 (4 sets each)). Word field is 2 bits (2^2 = 4 words per block). Tag field is the rest 15 bits

5. Do Exercise 12 in Chapter 6 (Memory) of Null and Lobur

   Suppose a process page table contains the entries shown below. Using the format shown in Figure 6.15a, indicate where the process pages are located in memory.

Frame	Valid Bit
1	1
-	0
0	1
3	1
-	0
-	0
2	1
-	0

   The following drawing shows where the process pages are located. It shows hows the contents of the virtual memory address pages correlate to the physical memory address frames:


Page
0
1
2
3
4
5
6
7
Frame
0
1
2
3