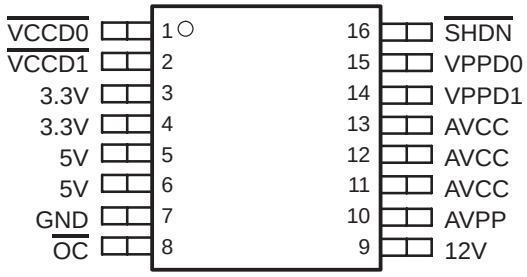
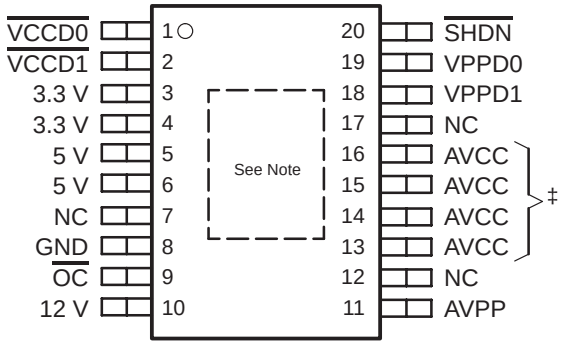
- **Fully Integrated V_{CC} and V_{pp} Switching for Single-Slot PC Card™ Interface**
- **Low $r_{DS(on)}$ (70-mΩ 5-V V_{CC} Switch and 3.3-V V_{CC} Switch)**
- **Compatible With Industry-Standard Controllers**
- **3.3-V Low-Voltage Mode**
- **Meets PC Card Standards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short-Circuit and Thermal Protection**
- **Space-Saving 16-Pin SSOP (DB) and 20-Pin HTSSOP (PWP)**
- **Compatible With 3.3-V, 5-V, and 12-V PC Cards**
- **Break-Before-Make Switching**

DB PACKAGE† (TOP VIEW)



† TPS2211A is pin-for-pin compatible with TPS2211 and TPS2212.

PW and PWP§ PACKAGE (TOP VIEW)



NC − No internal connection
‡ Must be tied together externally as close to the device as possible.
§ PowerPAD applies to PWP package only.

description

The TPS2211A PC Card power-interface switch provides an integrated power-management solution for a single PC Card. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit, using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power, and is compatible with many PCMCIA controllers.

The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card. controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

The TPS2211A features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. Bias power can be derived from either the 3.3-V or 5-V inputs. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

End equipment for the TPS2211A includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		
	PLASTIC SMALL OUTLINE (DB)	PLASTIC SMALL OUTLINE (PW)	PowerPAD™ PLASTIC SMALL OUTLINE (PWP)
−40°C to 85°C	TPS2211AIDB	TPS2211APW	TPS2211APWP

The DB, PW, and PWP packages are only available left-end taped and reeled (indicated by the R suffix on the device type, e.g. TPS2211AIDBR).

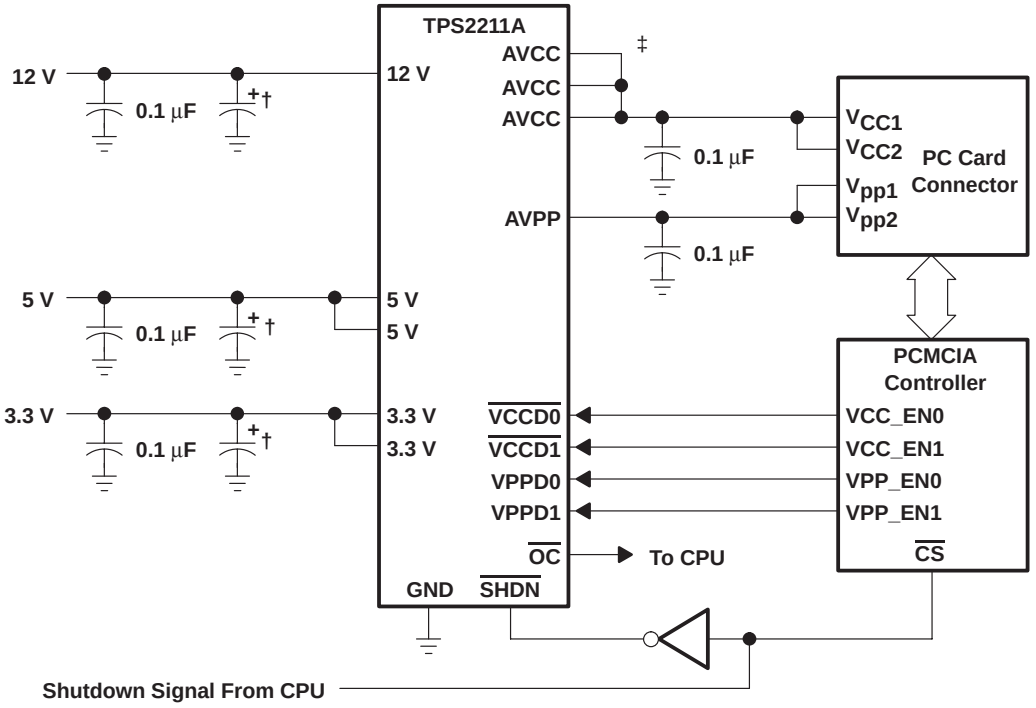
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).
LinBiCMOS, PowerPAD are trademarks of Texas Instruments.

SELECTION GUIDE

DEVICE	V_{CC}			V_{pp}		
	3.3-V TYPICAL $r_{DS(on)}$ (Ω)	5-V TYPICAL $r_{DS(on)}$ (Ω)	RECOMMENDED MAXIMUM OUTPUT CURRENT (A)	3.3-V OR 5-V TYPICAL $r_{DS(on)}$ (Ω)	12-V MAXIMUM $r_{DS(on)}$ (Ω)	RECOMMENDED MAXIMUM OUTPUT CURRENT (A)
TPS2211AIDB	0.07	0.07	1	4	2	0.15
TPS2211APW	0.07	0.07	1	4	2	0.15
TPS2211APWP	0.07	0.07	1	4	2	0.15
TPS2211IDB	0.048	0.05	1	4	1	0.15
TPS2212IDB	0.16	0.16	0.25	4	1	0.15

typical PC-card power-distribution application



† Refer to power-supply considerations in application information for selection of appropiate capacitors on supply inputs.
‡ The diagram refers to the 16-pin DB package. It is recommended that the 3 AVCC pins be tied together externally to minimize power loss. For the 20-pin package, the 4 AVCC pins (13, 14, 15, and 16) must be tied together externally as close as possible to the device.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PW, PWP	DB		
3.3V	3, 4	3, 4	I	3.3-V V_{CC} input for card power and/or chip power if 5 V is not present
5V	5, 6	5, 6	I	5-V V_{CC} input for card power and/or chip power
12V	10	9	I	12-V V_{pp} input card power
AVCC	13, 14, 15, 16	11, 12, 13	O	Switched output that delivers 0 V, 3.3-V, 5-V, or high impedance to card; must be tied together externally for the 20-pin PWP package.
AVPP	11	10	O	Switched output that delivers 0 V, 3.3-V, 5-V, 12-V, or high impedance to card
GND	8	7		Ground
NC	7, 12, 17	−		No internal connection
$\overline{OC}$	9	8	O	Logic-level overcurrent reporting output that goes low when an overcurrent conditions exists
$\overline{SHDN}$	20	16	I	Logic input that shuts down the device and sets all power outputs to high-impedance state
$\overline{VCCD0}$	1	1	I	Logic input that controls voltage of AVCC (see control-logic table)
$\overline{VCCD1}$	2	2	I	Logic input that controls voltage of AVCC (see control-logic table)
VPPD0	19	15	I	Logic input that controls voltage of AVPP (see control-logic table)
VPPD1	18	14	I	Logic input that controls voltage of AVPP (see control-logic table)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(5V)}$ . . . . . −0.3 V to 7 V
$V_{I(3.3V)}$ . . . . . −0.3 V to 7 V
$V_{I(12V)}$ . . . . . −0.3 V to 14 V
Logic input voltage . . . . . −0.3 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output current (each card): $I_{O(VCC)}$ . . . . . internally limited
$I_{O(VPP)}$ . . . . . internally limited
Operating virtual junction temperature range, T_J . . . . . −40°C to 150°C
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB−16	800 mW	8.0 mW/°C	440 mW	320 mW
PW−20	741.3 mW	7.41 mW/°C	407.7 mW	296.5 mW
PWP−20	2740 mW	27.4 mW/°C	1507 mW	1096 mW

These devices are mounted on a Low-K PCB with 0 LFM.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(12V)}$	0	13.5	V
Output current	$I_{O(AVCC)}$		1	A
	$I_{O(AVPP)}$		150	mA
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics, T_A = −40°C to 85°C (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
	Switch resistance	5 V to AVCC	$V_{I(5V)}$ = 5 V		70	120	mΩ
		3.3 V to AVCC	$V_{I(3.3V)}$ = 3.3 V		70	120	
		5 V to AVPP	T_A = 25°C		4	6	Ω
		3.3 V to AVPP	T_A = 25°C		4	6	
		12 V to AVPP	T_A = 25°C		1	2	
$V_{O(AVPP)}$	Clamp low voltage		I_{pp} at 10 mA		0.3	0.8	V
$V_{O(AVCC)}$	Clamp low voltage		I_{CC} at 10 mA		0.1	0.8	V
I_{lkg}	Leakage current	I_{pp} high-impedance state	T_A = 25°C		1	10	µA
			T_A = 85°C			50	
		I_{CC} high-impedance state	T_A = 25°C		1	10	
			T_A = 85°C			50	
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = 5 V, $V_{O(AVPP)}$ = 12 V		40	75	µA
		$V_{I(5V)}$ = 0 V, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = 12 V		50	90	
		Shutdown mode	$V_{O(AVCC)}$ = $V_{O(AVPP)}$ = Hi-Z			1	
I_{OS}	Short-circuit output-current limit	$I_{O(AVCC)}$	T_A = 85°C, output powered into a short to GND	1		2.5	A
		$I_{O(AVPP)}$		180		400	mA
	Thermal shutdown‡	Trip point, T_J			140		°C
		Hysteresis			10		°C

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
‡ Specified by design, not tested in production·

logic section

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level, $\overline{OC}$	$V_{I(5V)}$ = 5 V, I_O = 0.2 mA	$V_{I(5V)}$ − 0.4		V
	$V_{I(5V)}$ = 0 V, I_O = 0.2 mA, $V_{I(3.3V)}$ = 3.3 V	$V_{I(3.3V)}$ − 0.4		
Logic output low level, $\overline{OC}$	I_O = 1 mA		0.4	V

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics‡

PARAMETER		TEST CONDITIONS§		MIN	TYP	MAX	UNIT
t_r	Rise times, output	$V_{O(AVCC)}$ (5 V)			2.8		ms
		$V_{O(AVPP)}$ (12 V)			6		
t_f	Fall times, output	$V_{O(AVCC)}$ (5 V)			5		
		$V_{O(AVPP)}$ (12 V)			19		
t_{pd}	Propagation delay (see Figure1)	$V_{I(VPPD0)}$ to $V_{O(AVPP)}$ (12 V)	t_{on}		7		ms
			t_{off}		23		
		$V_{I(VCCD1)}$ to $V_{O(AVCC)}$ (3.3 V)	t_{on}		2.8		
			t_{off}		12		
		$V_{I(VCCD0)}$ to $V_{O(AVCC)}$ (5 V)	t_{on}		3.7		
			t_{off}		13		

‡ Switching characteristics are with C_L = 150 µF.
§Refer to Parameter Measurement Information

PARAMETER MEASUREMENT INFORMATION

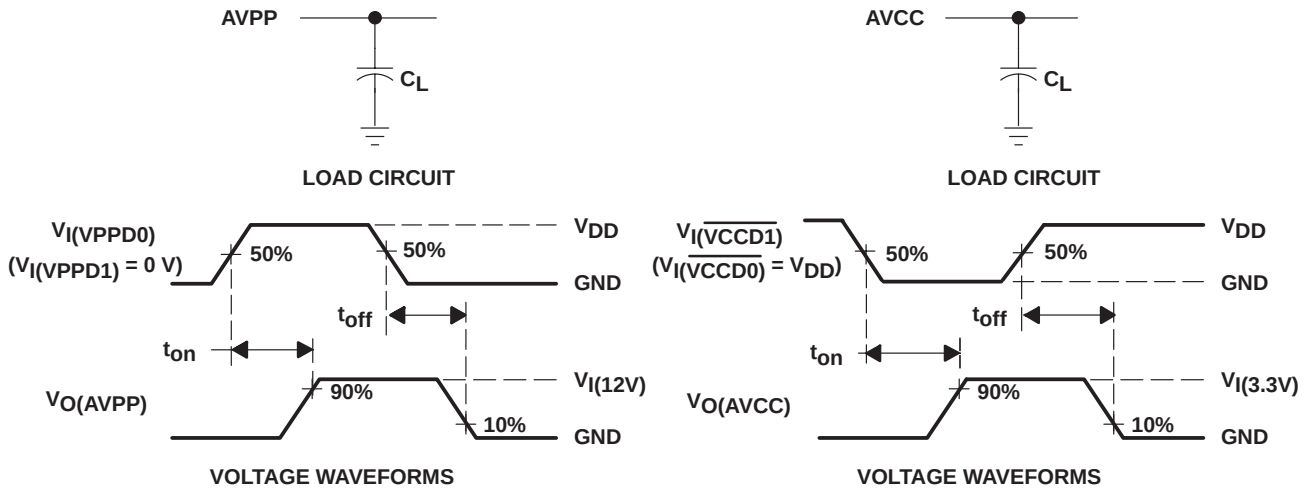


Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

	FIGURE
AVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch	2
AVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch	3
AVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch	4
AVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch	5
AVCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch	6
AVCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch	7
AVCC Propagation Delay and Rise Time With 150-µF Load, 5-V Switch	8
AVCC Propagation Delay and Fall Time With 150-µF Load, 5-V Switch	9
AVPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch	10
AVPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch	11
AVPP Propagation Delay and Rise Time With 150-µF Load, 12-V Switch	12
AVPP Propagation Delay and Fall Time With 150-µF Load, 12-V Switch	13

PARAMETER MEASUREMENT INFORMATION

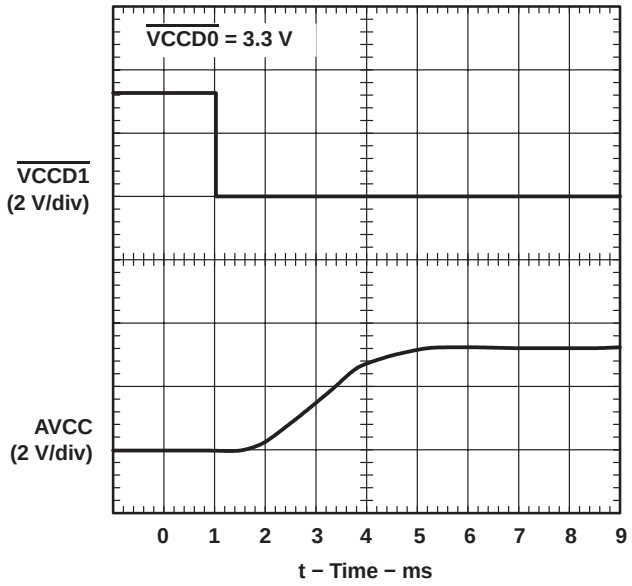


Figure 2. AVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch

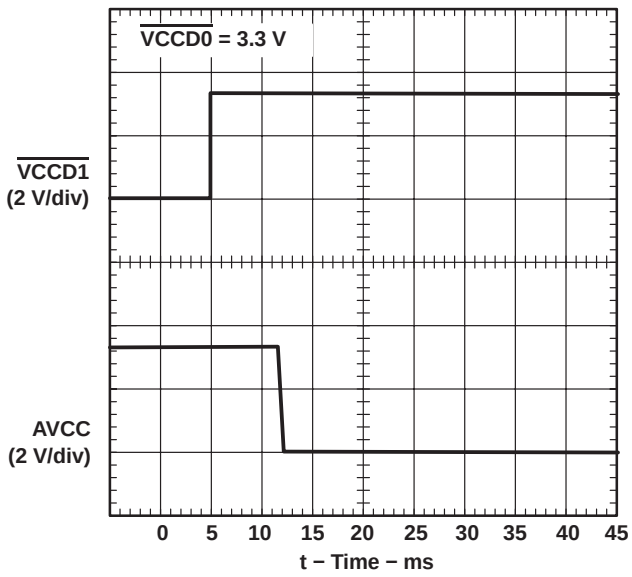


Figure 3. AVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch

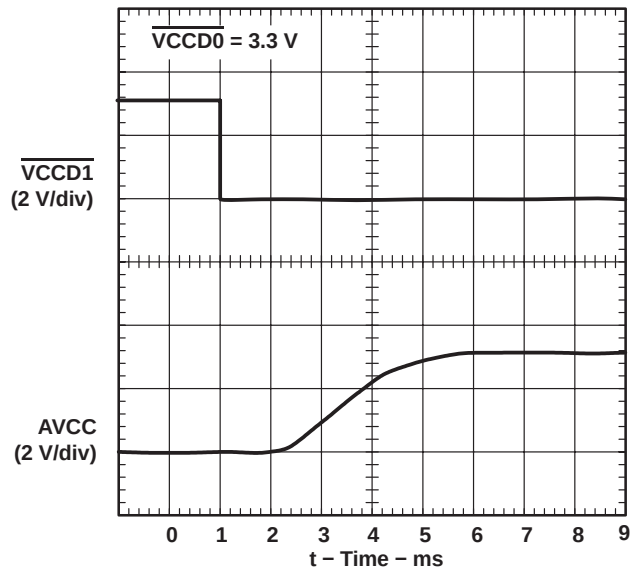


Figure 4. AVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch

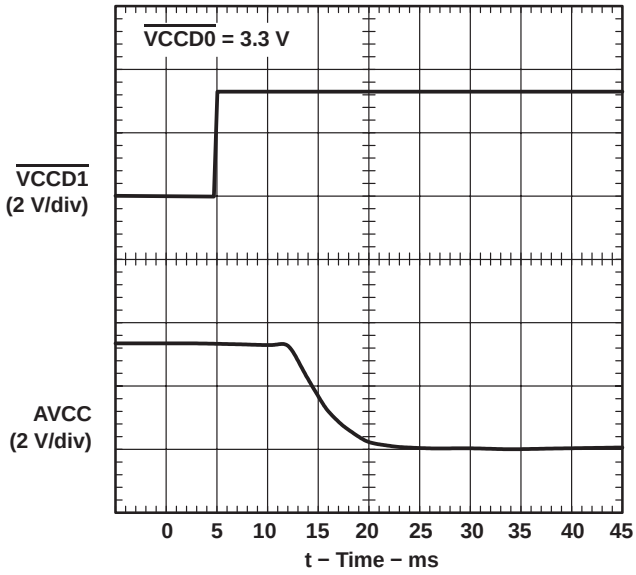


Figure 5. AVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch

PARAMETER MEASUREMENT INFORMATION

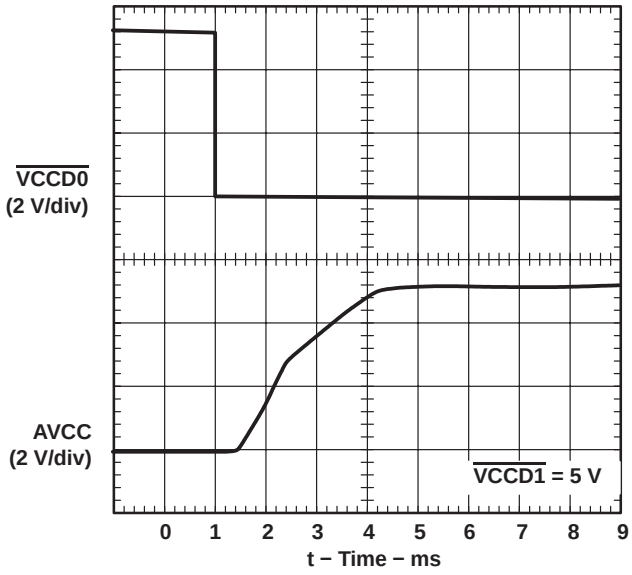


Figure 6. AVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch

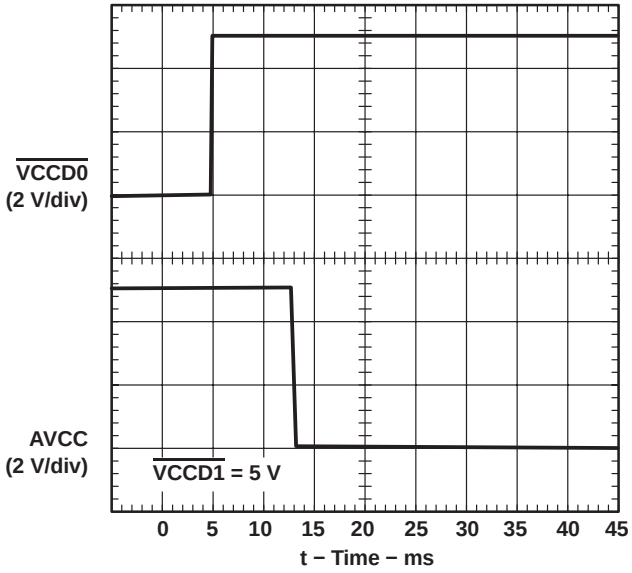


Figure 7. AVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch

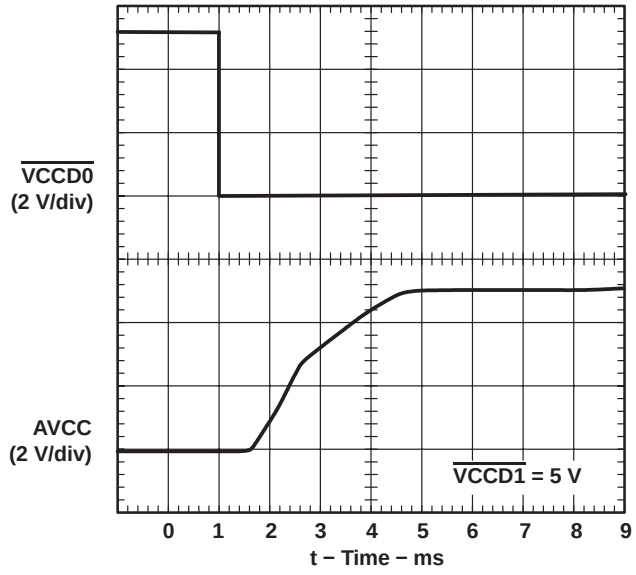


Figure 8. AVCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch

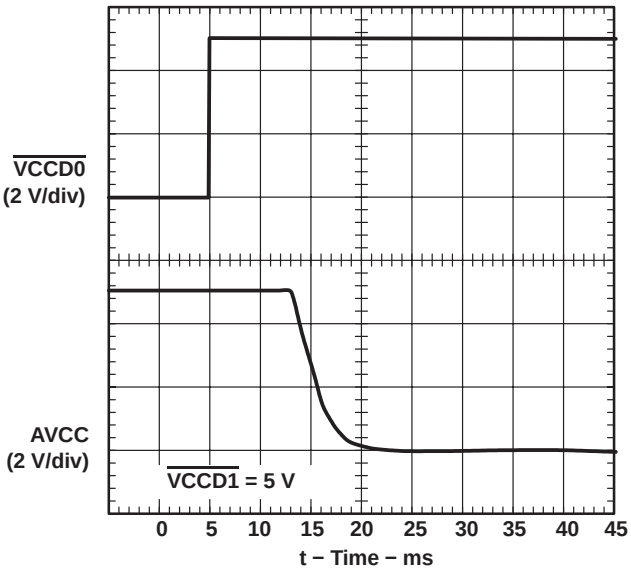


Figure 9. AVCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

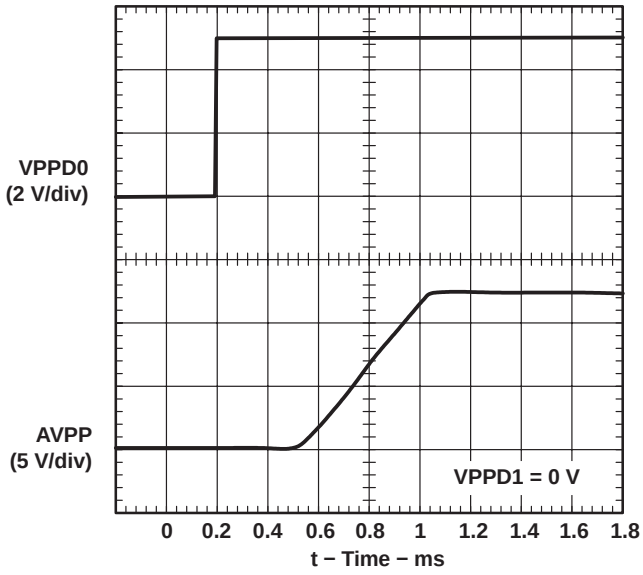


Figure 10. AVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch

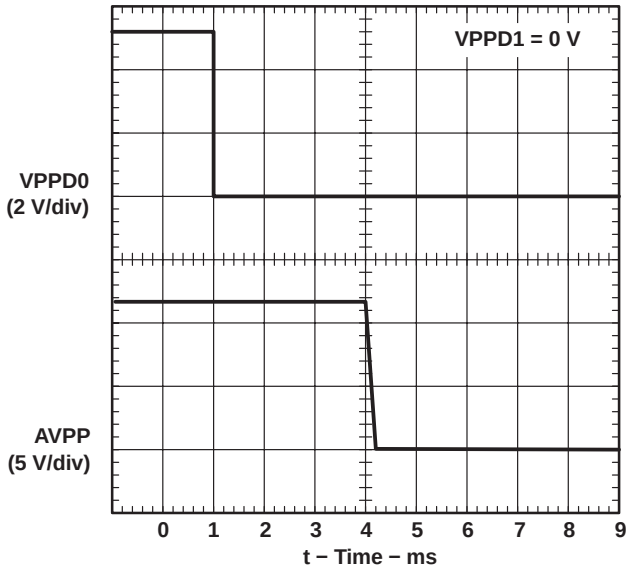


Figure 11. AVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch

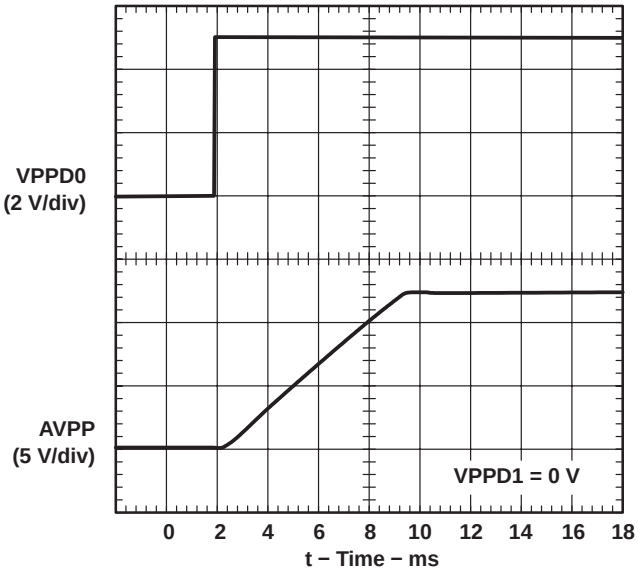


Figure 12. AVPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch

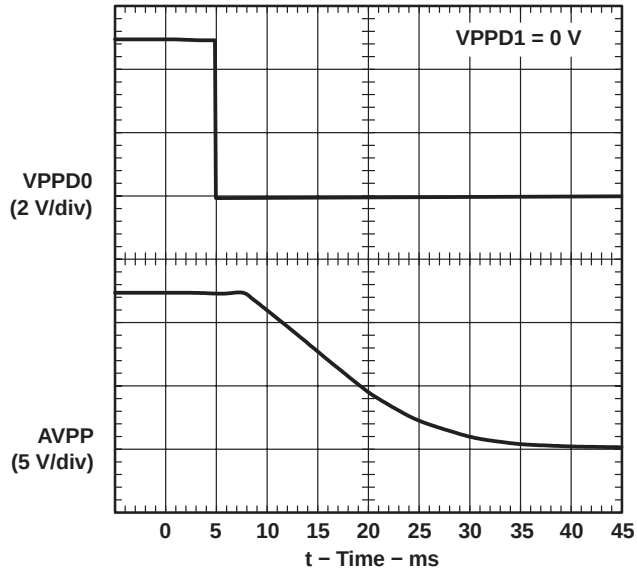


Figure 13. AVPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$I_{CC(5V)}$	Supply current	vs Junction temperature	14
$I_{CC(3.3V)}$	Supply current	vs Junction temperature	15
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V VCC switch	vs Junction temperature	16
$r_{DS(on)}$	Static drain-source on-state resistance, 3.3-V VCC switch	vs Junction temperature	17
$r_{DS(on)}$	Static drain-source on-state resistance, 12-V VPP switch	vs Junction temperature	18
$V_{O(AVCC)}$	Output voltage, 5-V VCC switch	vs Output current	19
$V_{O(AVCC)}$	Output voltage, 3.3-V VCC switch	vs Output current	20
$V_{O(AVPP)}$	Output voltage, 12-V VPP switch	vs Output current	21
$I_{OS(AVCC)}$	Short-circuit current, 5-V VCC switch	vs Junction temperature	22
$I_{OS(AVCC)}$	Short-circuit current, 3.3-V VCC switch	vs Junction temperature	23
$I_{OS(AVPP)}$	Short-circuit current, 12-V VPP switch	vs Junction temperature	24

5-V SUPPLY CURRENT vs JUNCTION TEMPERATURE

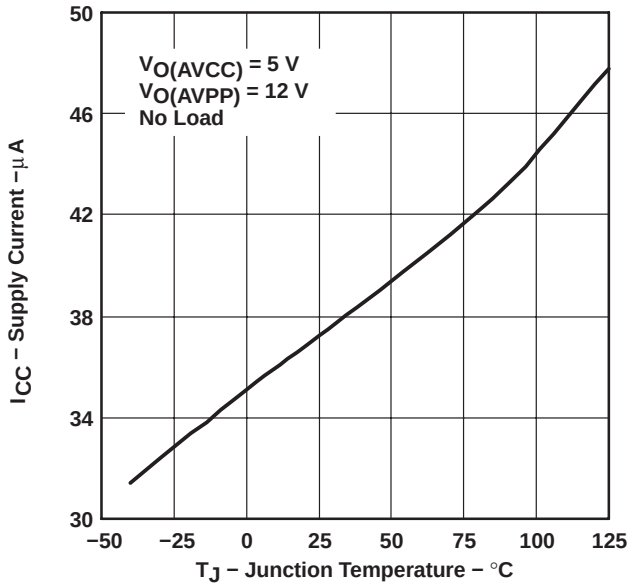


Figure 14

3.3-V SUPPLY CURRENT vs JUNCTION TEMPERATURE

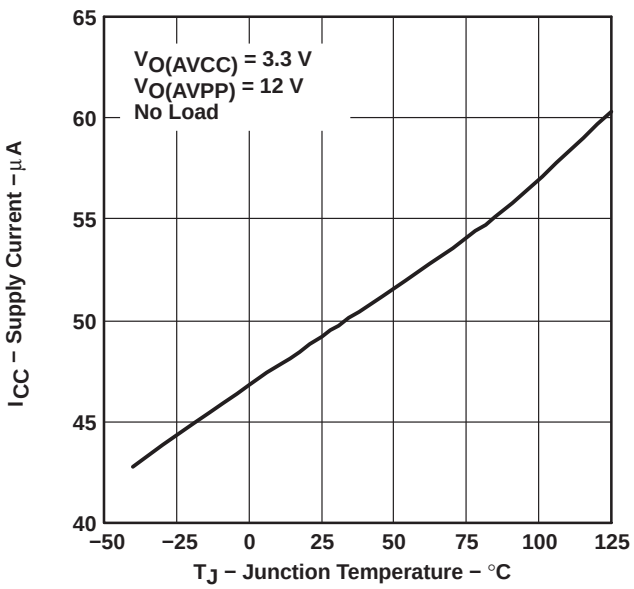


Figure 15

TYPICAL CHARACTERISTICS

5-V AVCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

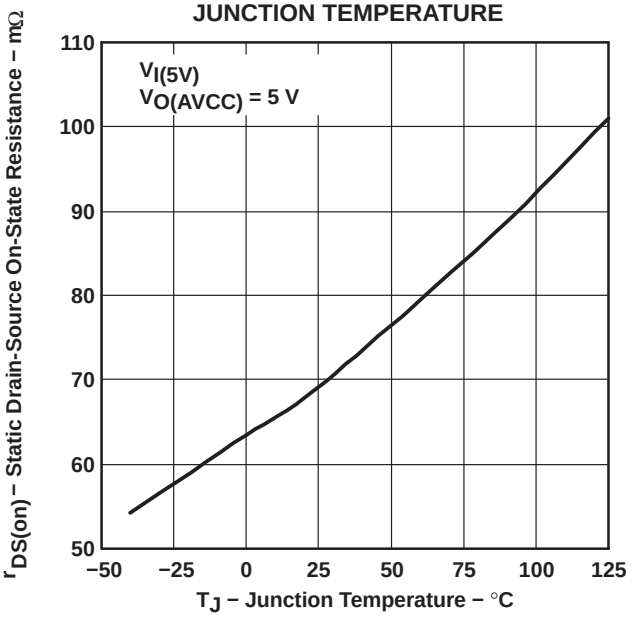


Figure 16

3.3-V AVCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

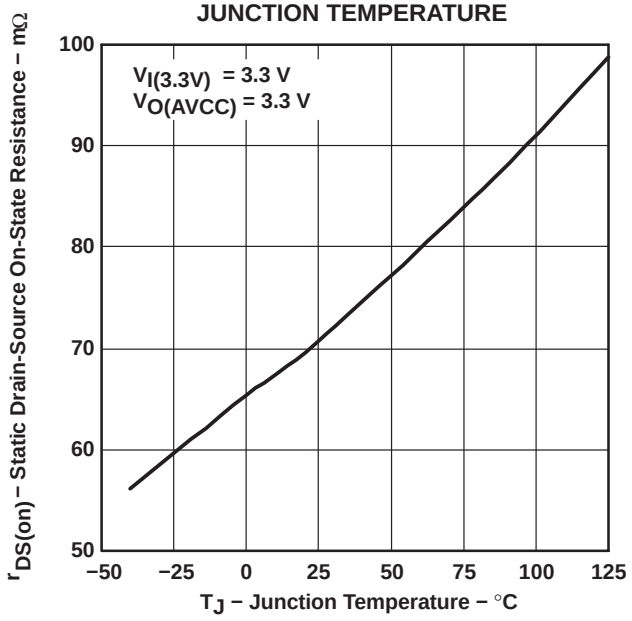


Figure 17

12-V AVCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

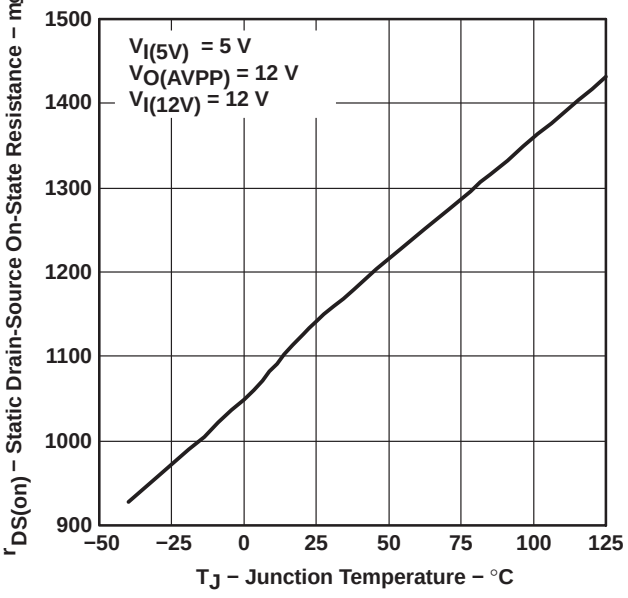


Figure 18

5-V AVCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

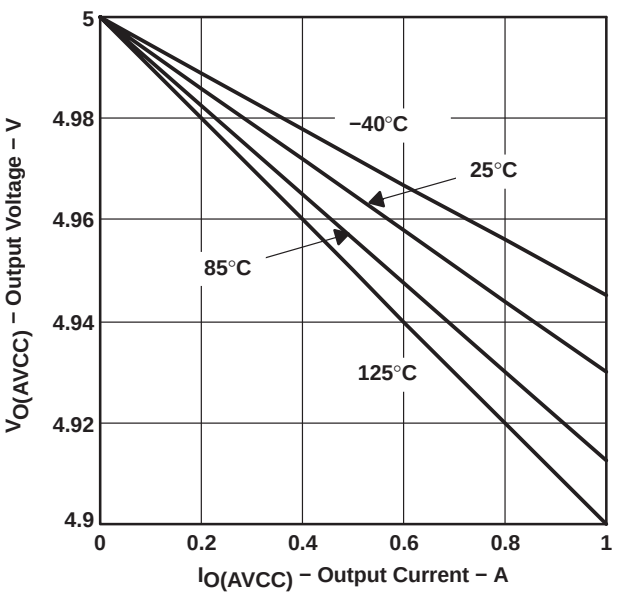


Figure 19

TYPICAL CHARACTERISTICS

3.3-V AVCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

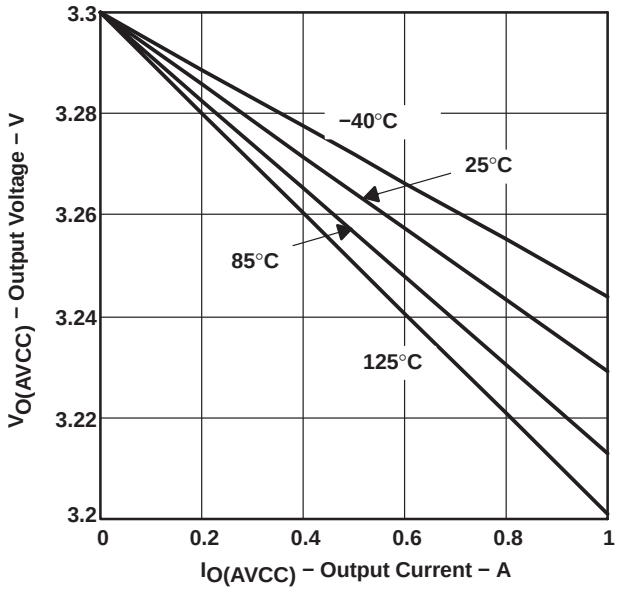


Figure 20

12-V AVCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

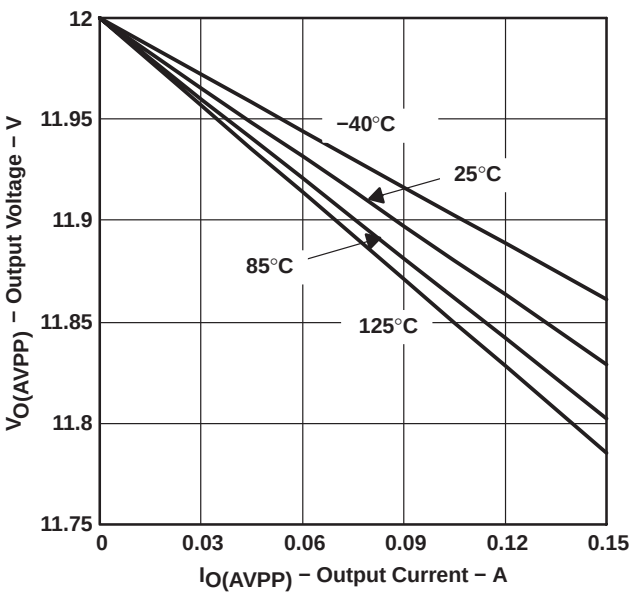


Figure 21

5-V AVCC SWITCH
SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

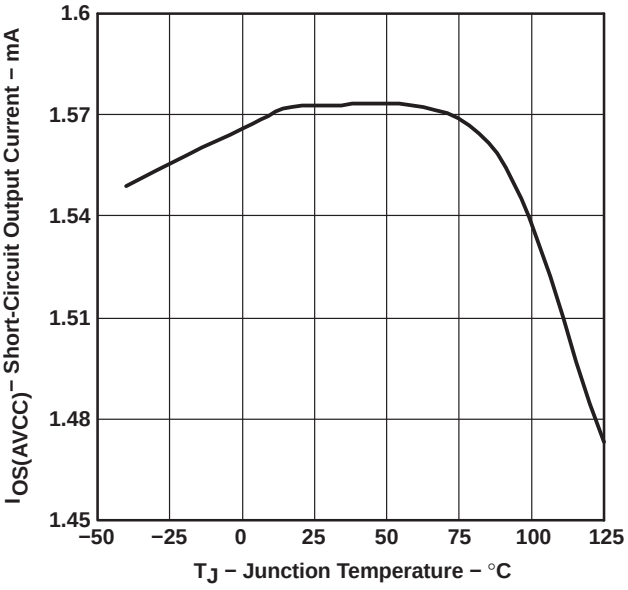


Figure 22

3.3-V AVCC SWITCH
SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

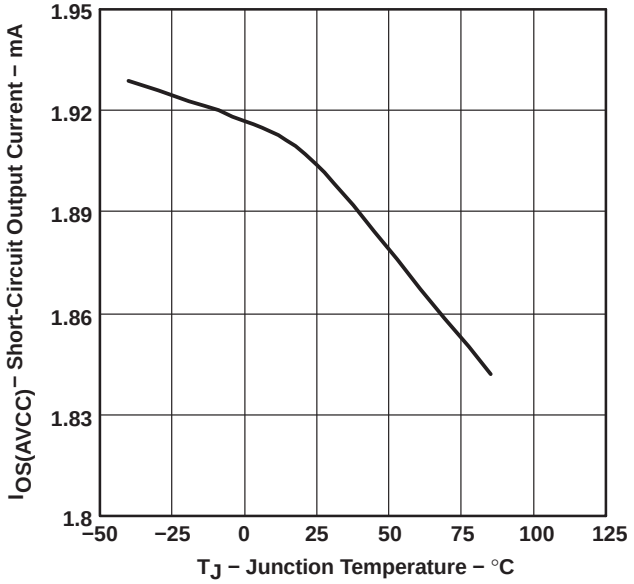


Figure 23

TYPICAL CHARACTERISTICS

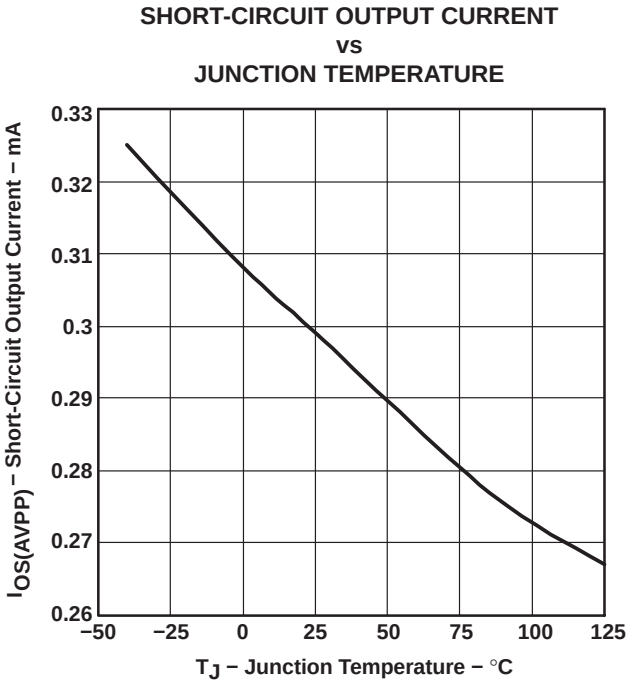


Figure 24

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug and play* concept, i.e. cards and hosts from different vendors should be compatible.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connectors. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

APPLICATION INFORMATION

designing for voltage regulation

The current PCMCIA specification for output voltage regulation of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card results from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design limits the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop (V_{DS}) for the TPS2211 is the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this leaves 100 mV for the allowable voltage drop across the TPS2211A. The voltage drop is the output current multiplied by the switch resistance of the TPS2211. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2211A divided by the output switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The AVCC outputs deliver 1 A continuous at 5 V and 3.3 V within regulation over the operating temperature range. Using the same equations, the PCMCIA specification for output voltage regulation of the 3.3 V output is 300 mV. Using the voltage drop percentages for power supply regulation (2%) and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV. The 12-V outputs (AVPP) of the TPS2211A can deliver 150 mA continuously.

overcurrent and overtemperature protection

PC Cards are inherently subject to damage from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in a sudden loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor and requires troubleshooting and repair, usually by the manufacturer, when fuses are blown.

The TPS2211A uses sense FETs to check for overcurrent conditions in each of the AVCC and AVPP outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when an overcurrent condition is detected providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2211A controls the rise time of the AVCC and AVPP outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2211A engages. If the AVCC or AVPP outputs are driven below ground, the TPS2211A may latch nondestructively in an off state. Cycling power reestablishes normal operation.

Overcurrent limiting for the AVCC outputs is designed to activate if powered up into a short in the range of 1 A to 2.5 A, typically at about 1.6 A. The AVPP outputs limit from 180 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power dissipation ratings are exceeded. Thermal limiting disables power output until the device has cooled.

APPLICATION INFORMATION

12-V supply not required

Most PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which require that power be present at all times. The TPS2211A offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V input. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12-V switch inputs when the 12-V input is not used. Additional power savings are realized by the TPS2211A during a software shutdown, in which quiescent current drops to a maximum of 1 μA.

3.3-V low-voltage mode

The TPS2211A operates in a 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)}$ = 0). This allows host and PC Cards to be operated in low-power 3.3-volts-only modes such as sleep or pager modes. Note that in these operation modes, the TPS2211A derives its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card.

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2211A meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3-V power. This functions as a power reset and ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge. The TPS2211A offers a selectable V_{CC} and V_{pp} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications.

output ground switches

PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes.

power-supply considerations

The TPS2211A has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched AVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2211A, the power supply inputs should be bypassed with a 4.7-μF, or larger, electrolytic or tantalum capacitor paralleled by a 0.1-μF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-μF, or larger, ceramic capacitor; doing so improves the immunity of the TPS2211A to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2211A and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below −0.3 V.

APPLICATION INFORMATION

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16 through 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

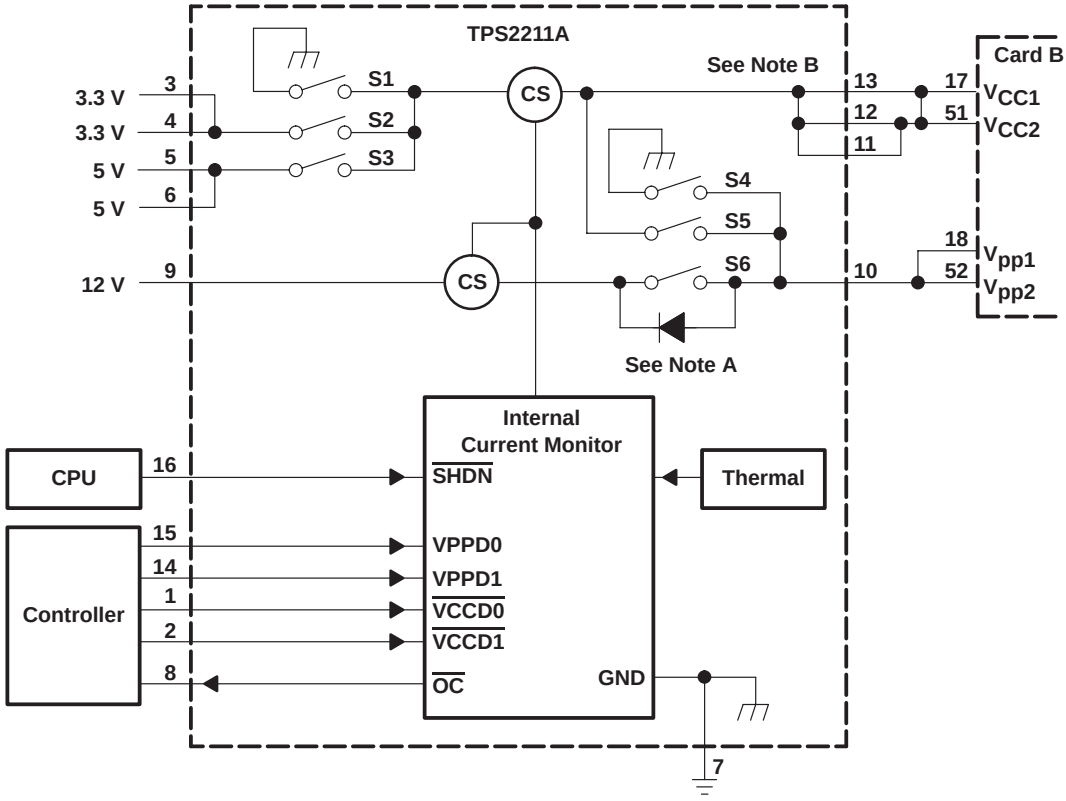
Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A, R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

ESD protection

All TPS2211A inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The AVCC and AVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-μF capacitors protects the devices from discharges up to 10 kV.



NOTE A: MOSFET switch S6 has a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.
NOTE B: The diagram refers to the 16-pin DB package.

Figure 25. Internal Switching Matrix, TPS2211A Control Logic

APPLICATION INFORMATION

TPS2211A control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	VPPD0	VPPD1	S4	S5	S6	AVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	AVCC†
1	1	0	OPEN	OPEN	CLOSED	VPP (12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC

AVCC

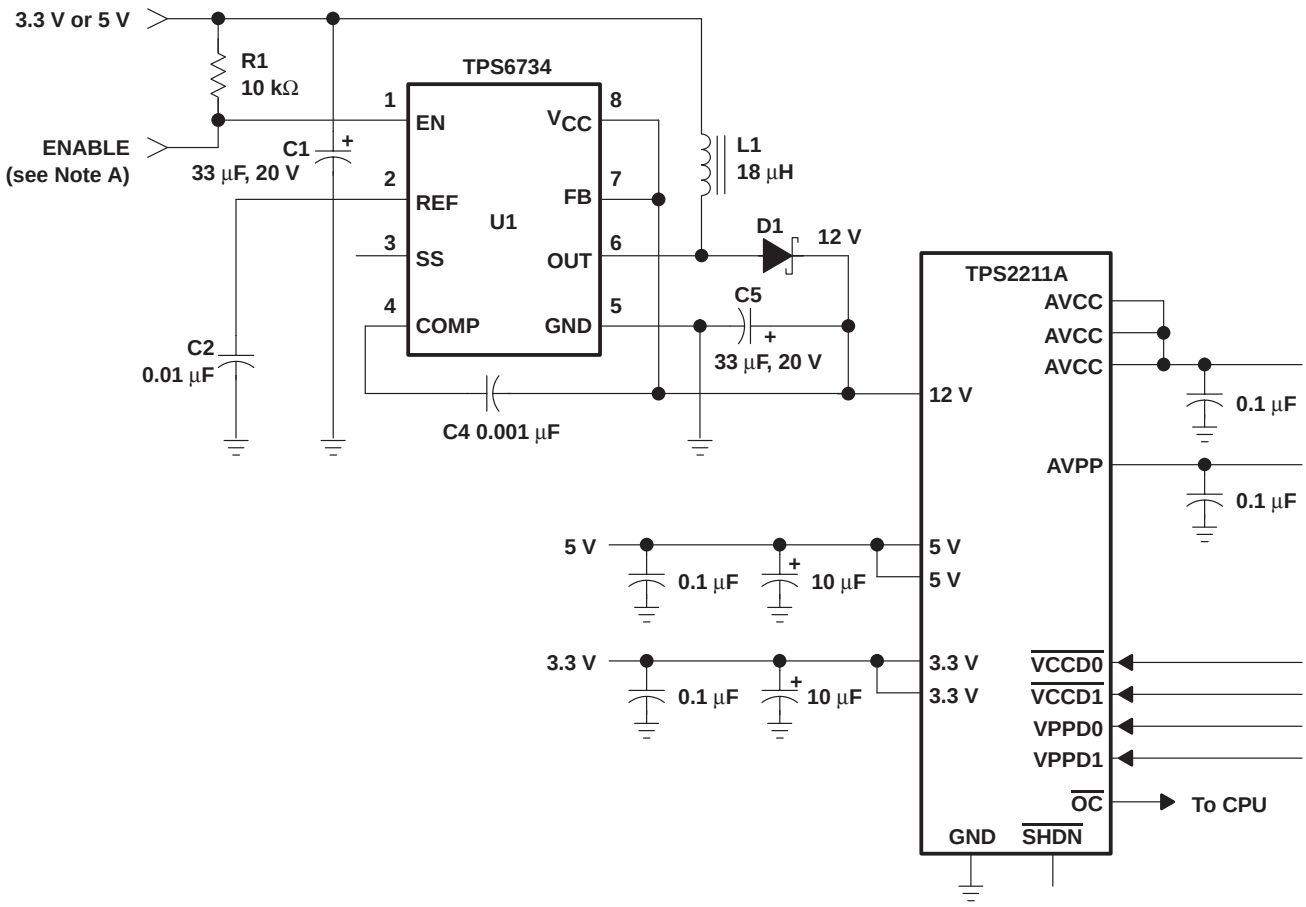
CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	$\overline{\text{VCCD1}}$	$\overline{\text{VCCD0}}$	S1	S2	S3	AVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).

APPLICATION INFORMATION



NOTE A: The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 26. TPS2211A With TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2211AIDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PU2211A	Samples
TPS2211AIDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PU2211A	Samples
TPS2211AIDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PU2211A	Samples
TPS2211AIDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PU2211A	Samples
TPS2211APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2211A	Samples
TPS2211APWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2211A	Samples
TPS2211APWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2211A	Samples
TPS2211APWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2211A	Samples
TPS2211APWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2211A	Samples
TPS2211APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2211A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

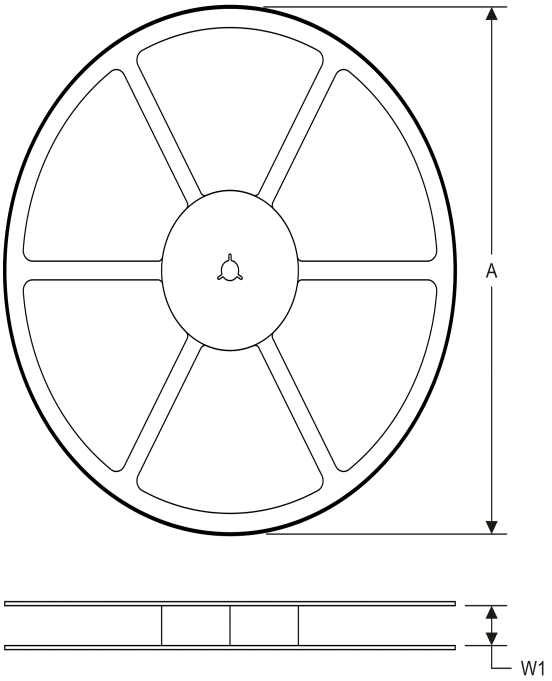
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

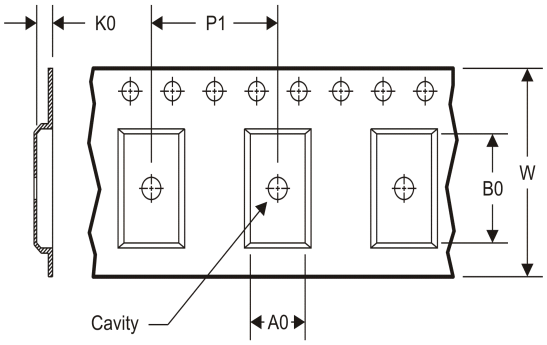
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



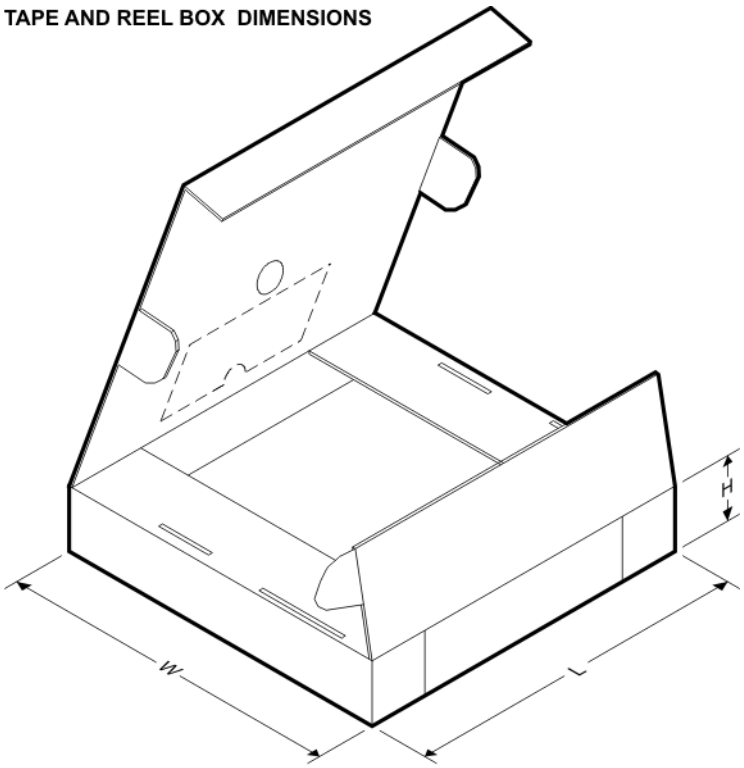
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2211AIDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TPS2211APWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS2211APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

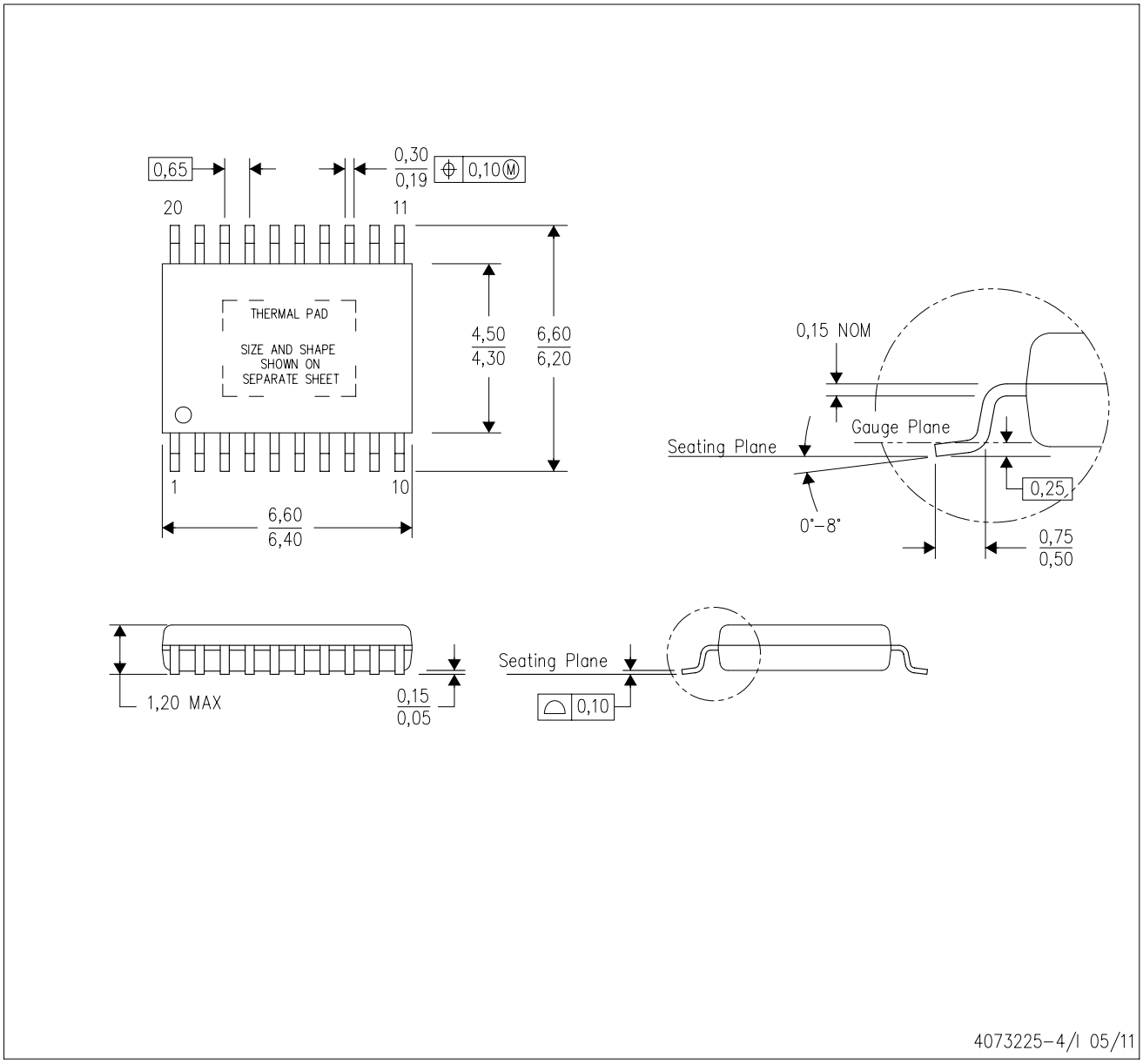
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2211AIDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TPS2211APWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0
TPS2211APWR	TSSOP	PW	20	2000	367.0	367.0	38.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

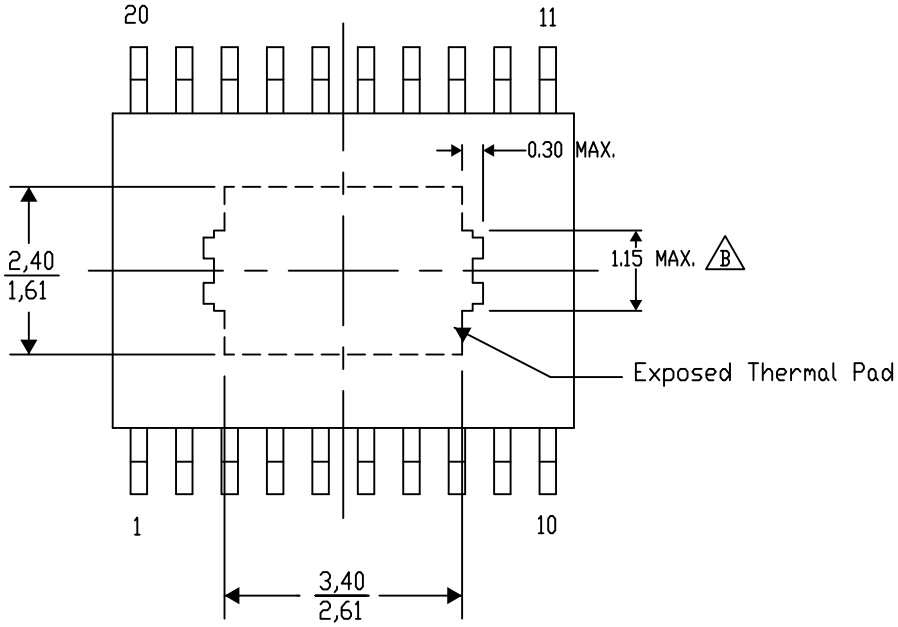
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

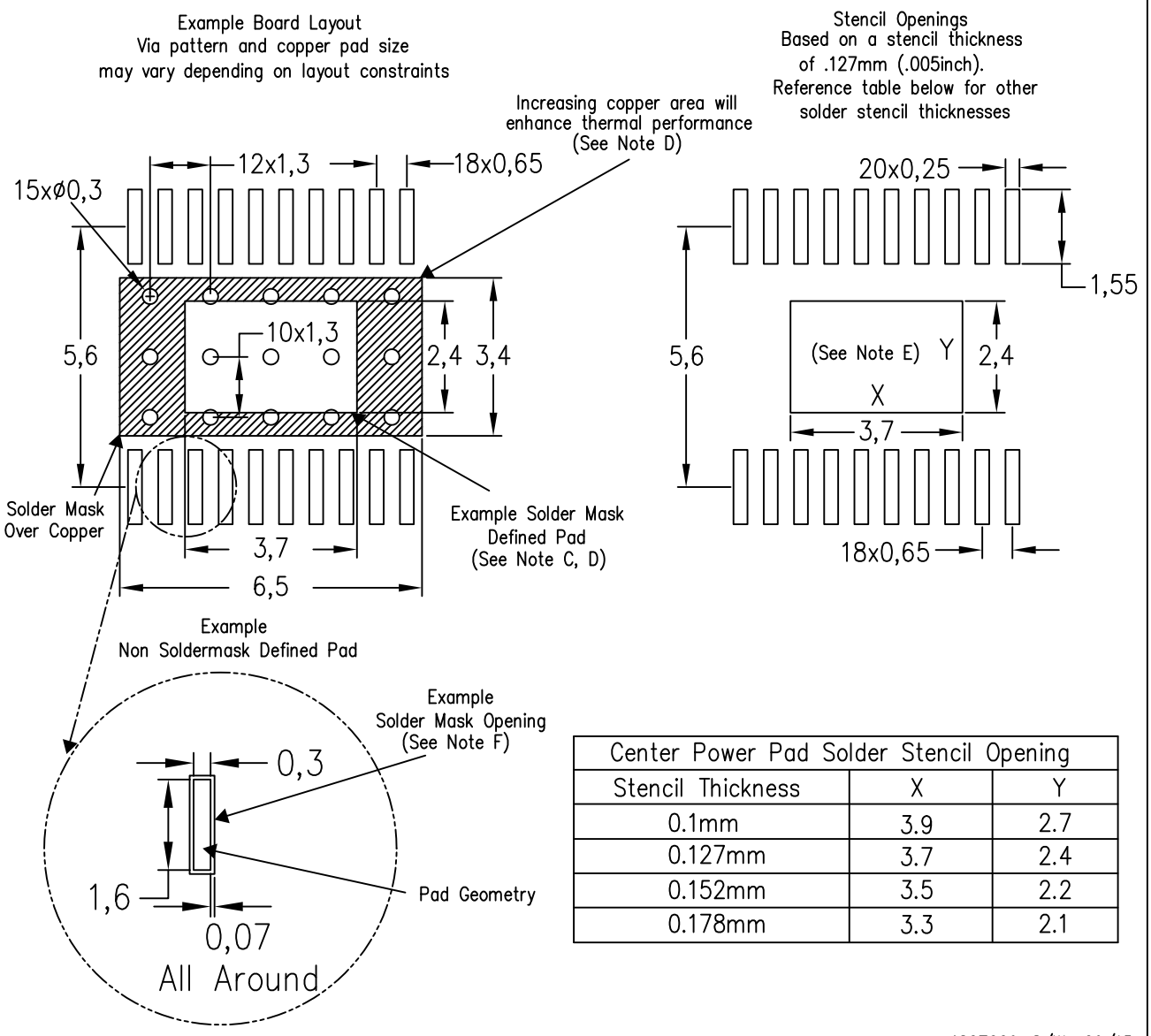
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

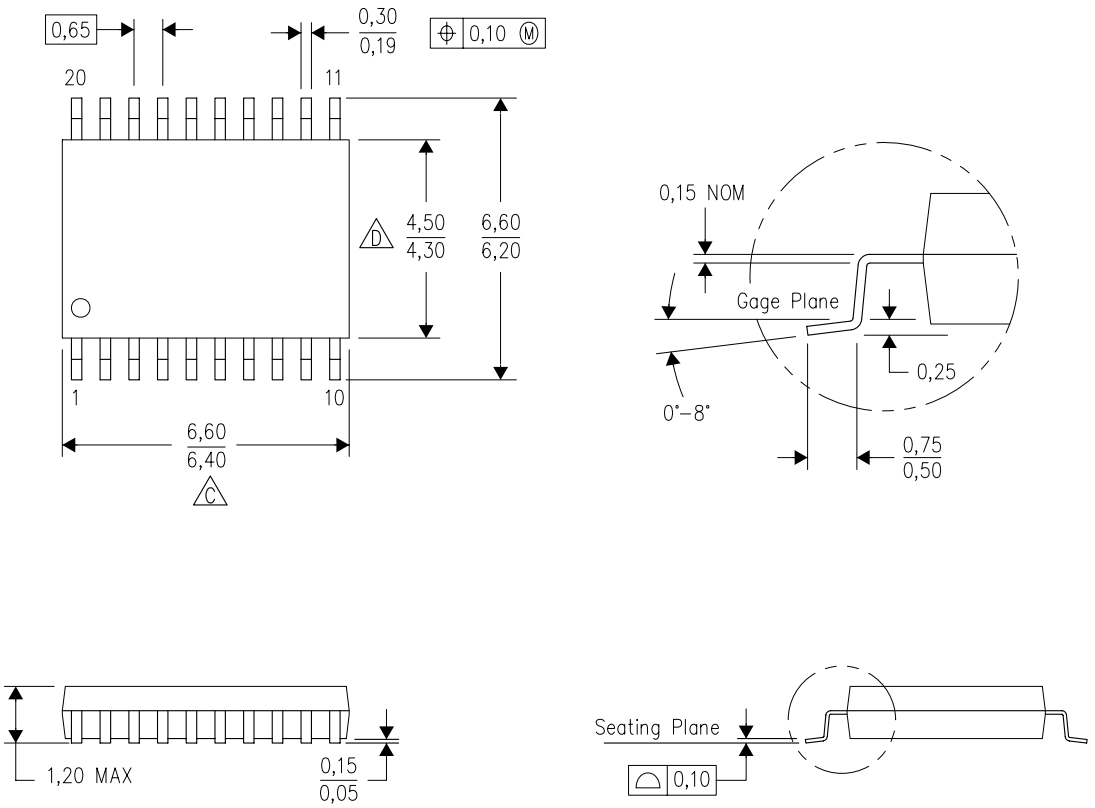


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

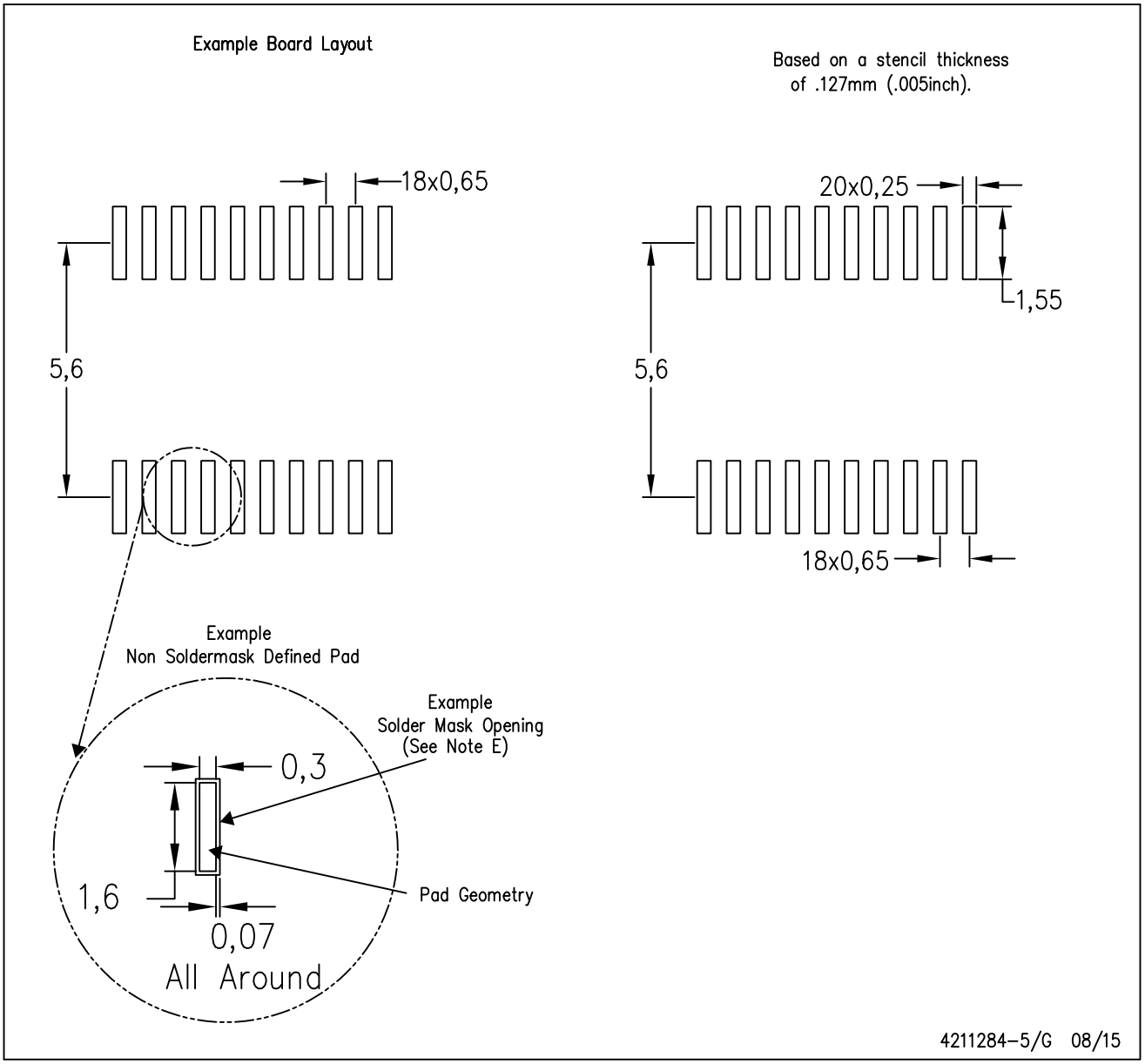
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE

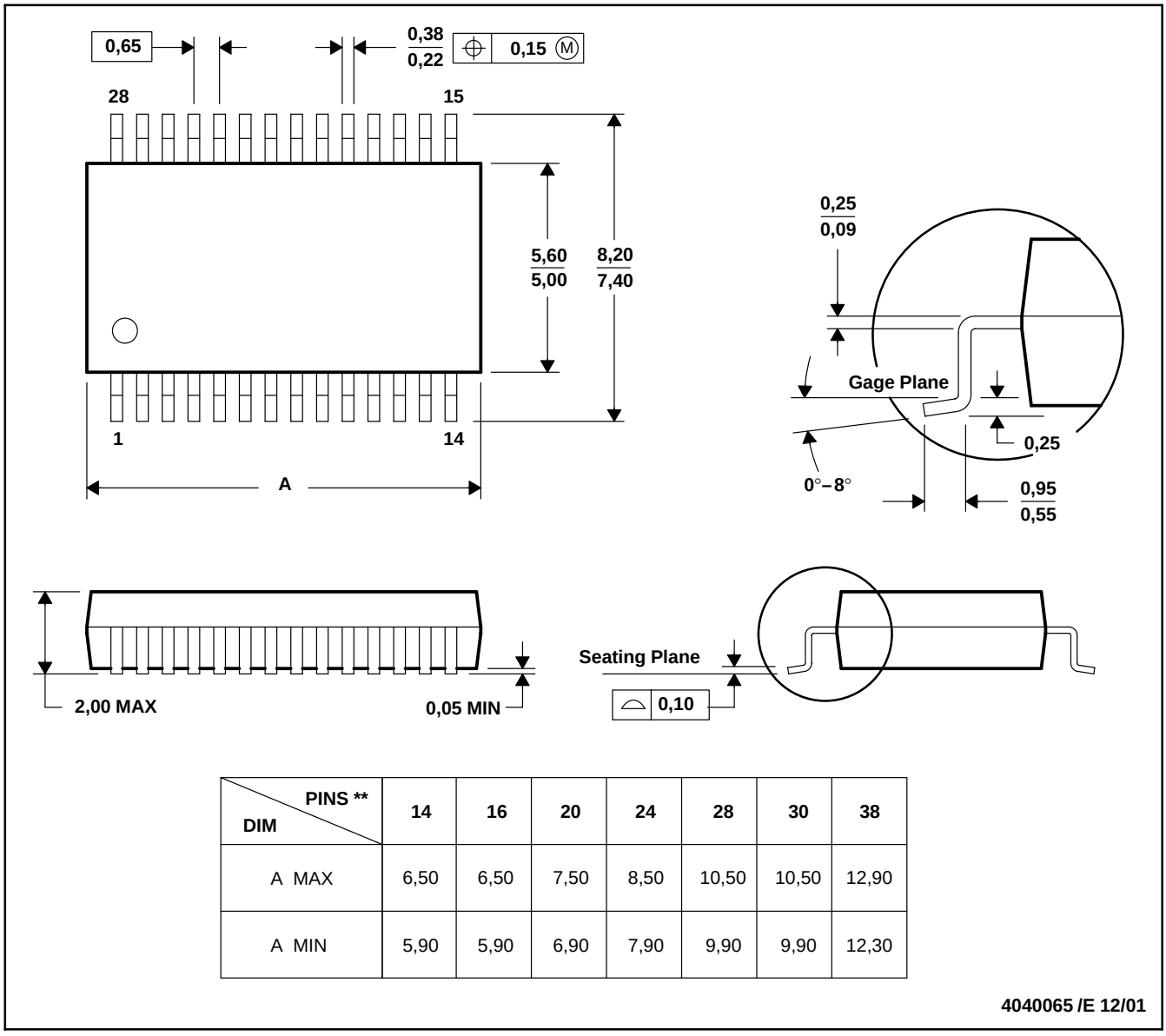


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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