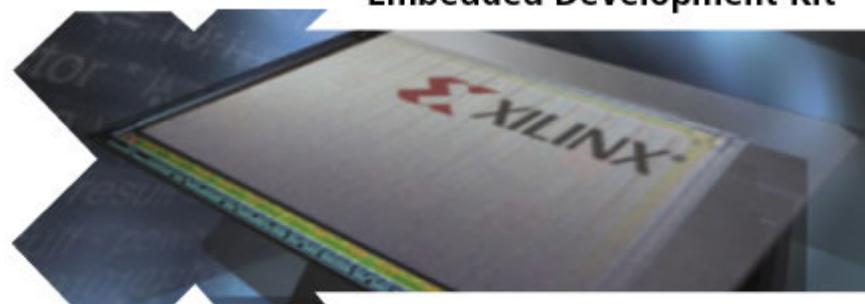




# ML510 BSB1 Std IP Design Adding PCores

February 2009

Embedded Development Kit



**PowerPC**



**Platform Studio™**



**MicroBlaze™**



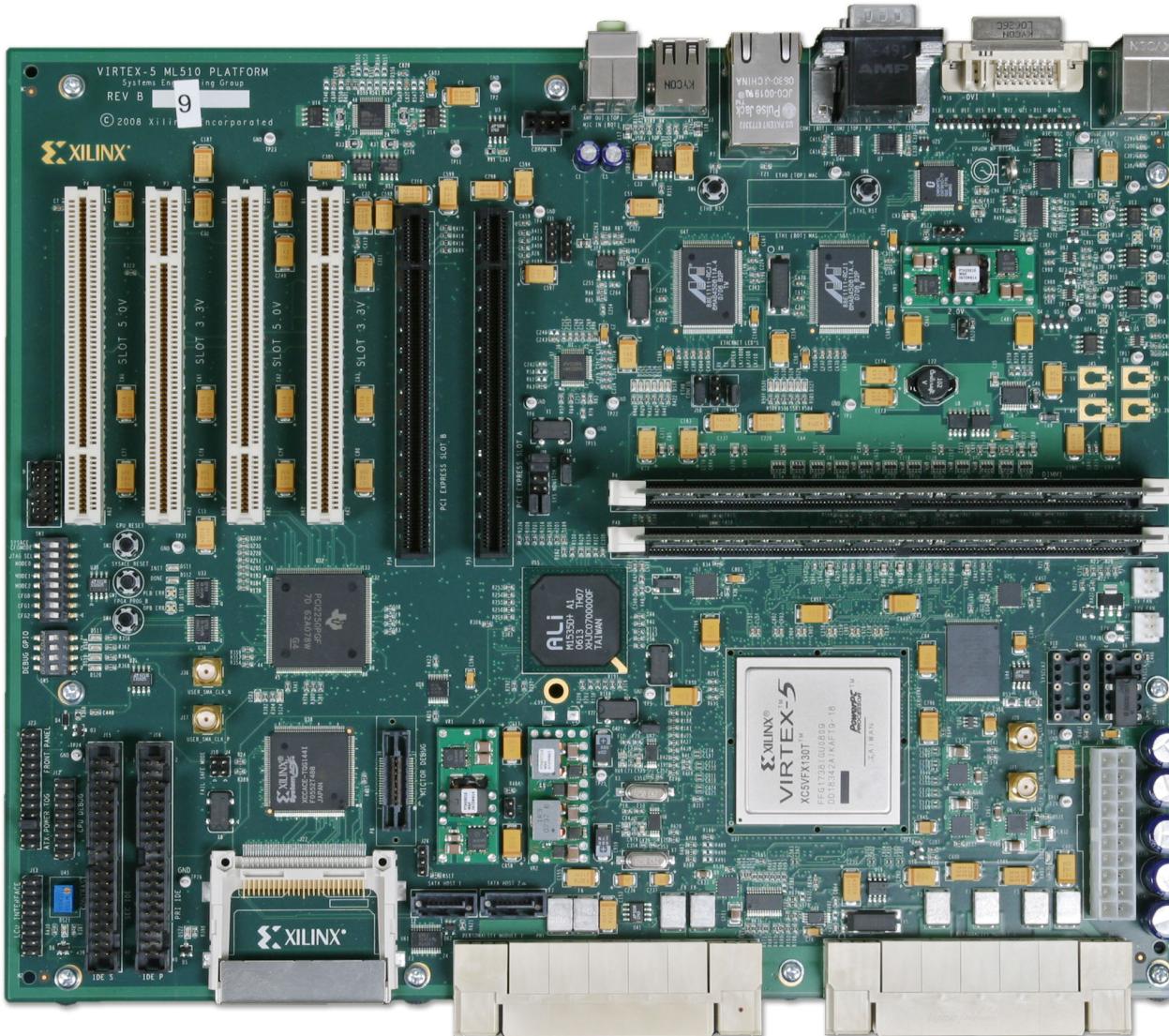
**XILINX®**

# Overview

- Hardware Setup
- Software Requirements
- Adding PCI
- Generate a Bitstream
- Transfer the Bitstream onto the FPGA
- Loading a Bootloop into the Block RAM



# Xilinx ML510 Board

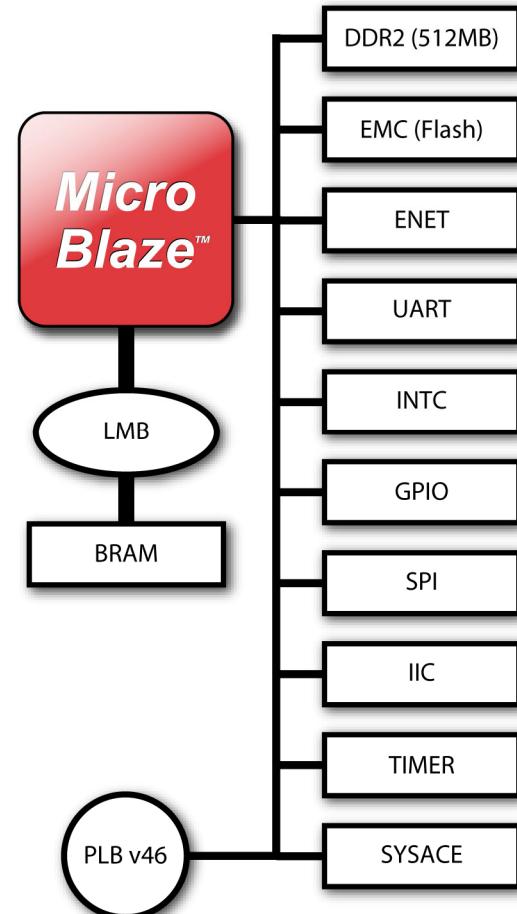


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# ML510 BSB1 MB

- The ML510 BSB1 MicroBlaze design hardware includes:
  - DDR2 Interface (DIMM0)
  - BRAM
  - External Memory Controller (EMC)
  - Networking
  - UART
  - Interrupt Controller
  - GPIO
  - SPI
  - IIC
  - Timer
  - System ACE CF Interface
  - PLB v46 Bus

ML510 BSB DIMM0 System



# Additional Setup Details

- Refer to ml510\_overview\_setup.ppt for details on:
  - Software Requirements
  - ML510 Board Setup
    - Equipment and Cables
    - Software
    - Network
  - Terminal Programs
    - This presentation requires the 9600-8-N-1 Baud terminal setup

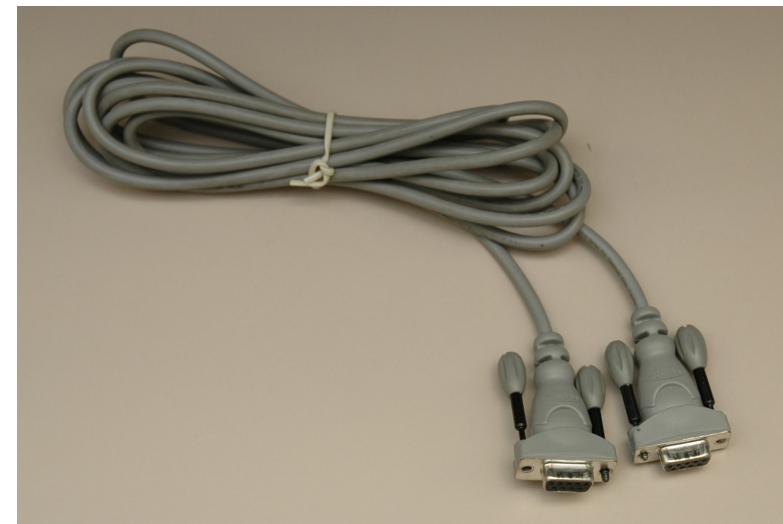


# Hardware Setup

- Connect the Xilinx Platform Cable USB to the ML510 board

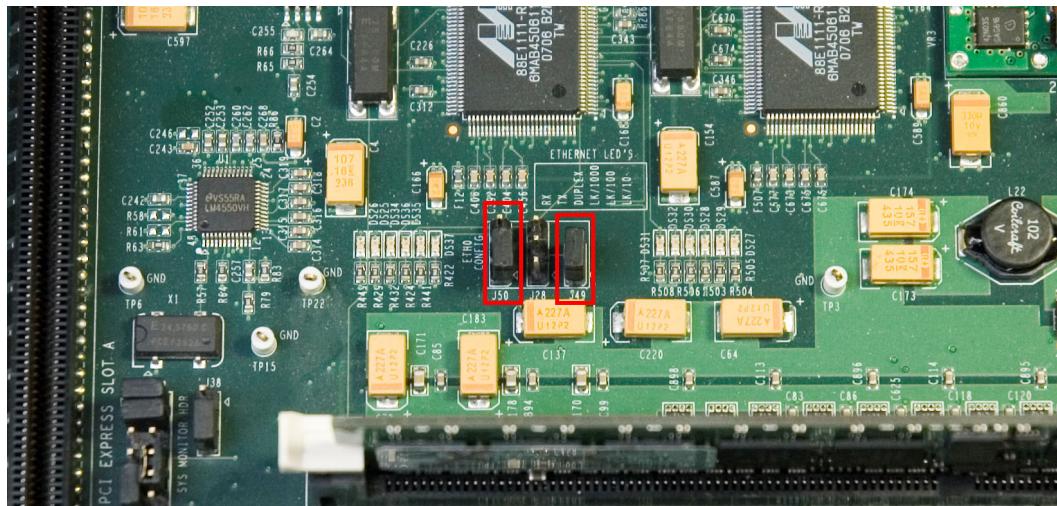


- Connect the RS232 null modem cable to the ML510 board



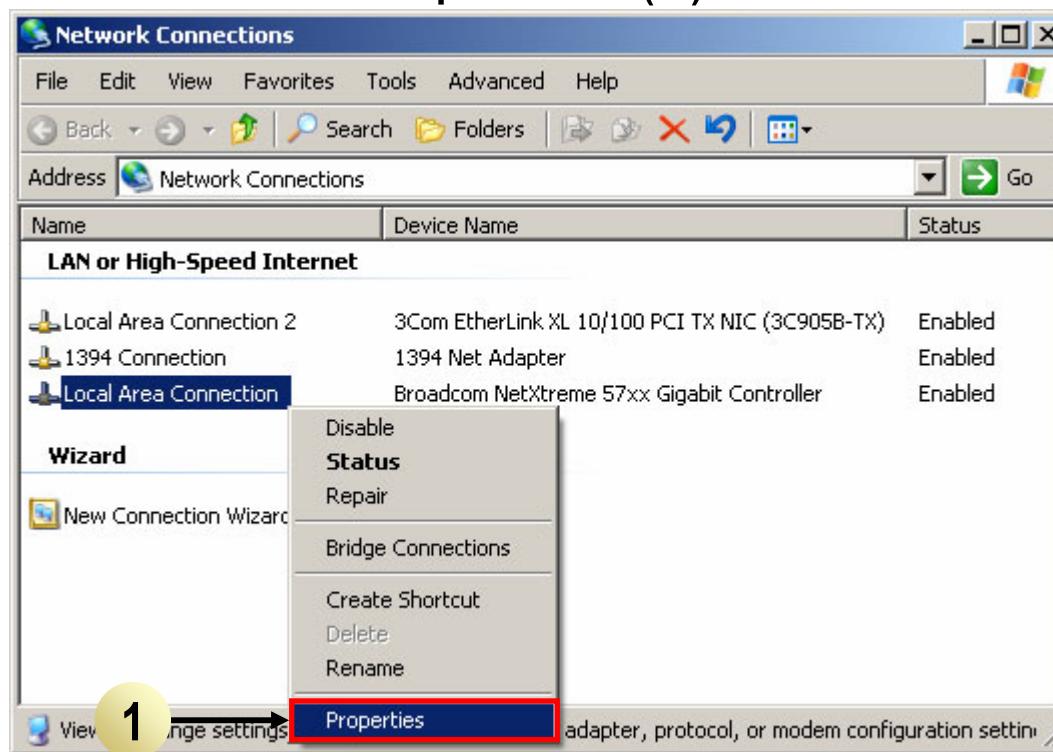
# Hardware Setup

- Set ML510 PHY0 Jumpers for RGMII
  - Set both J50 to 1-2 and connect J49; leave J28 open



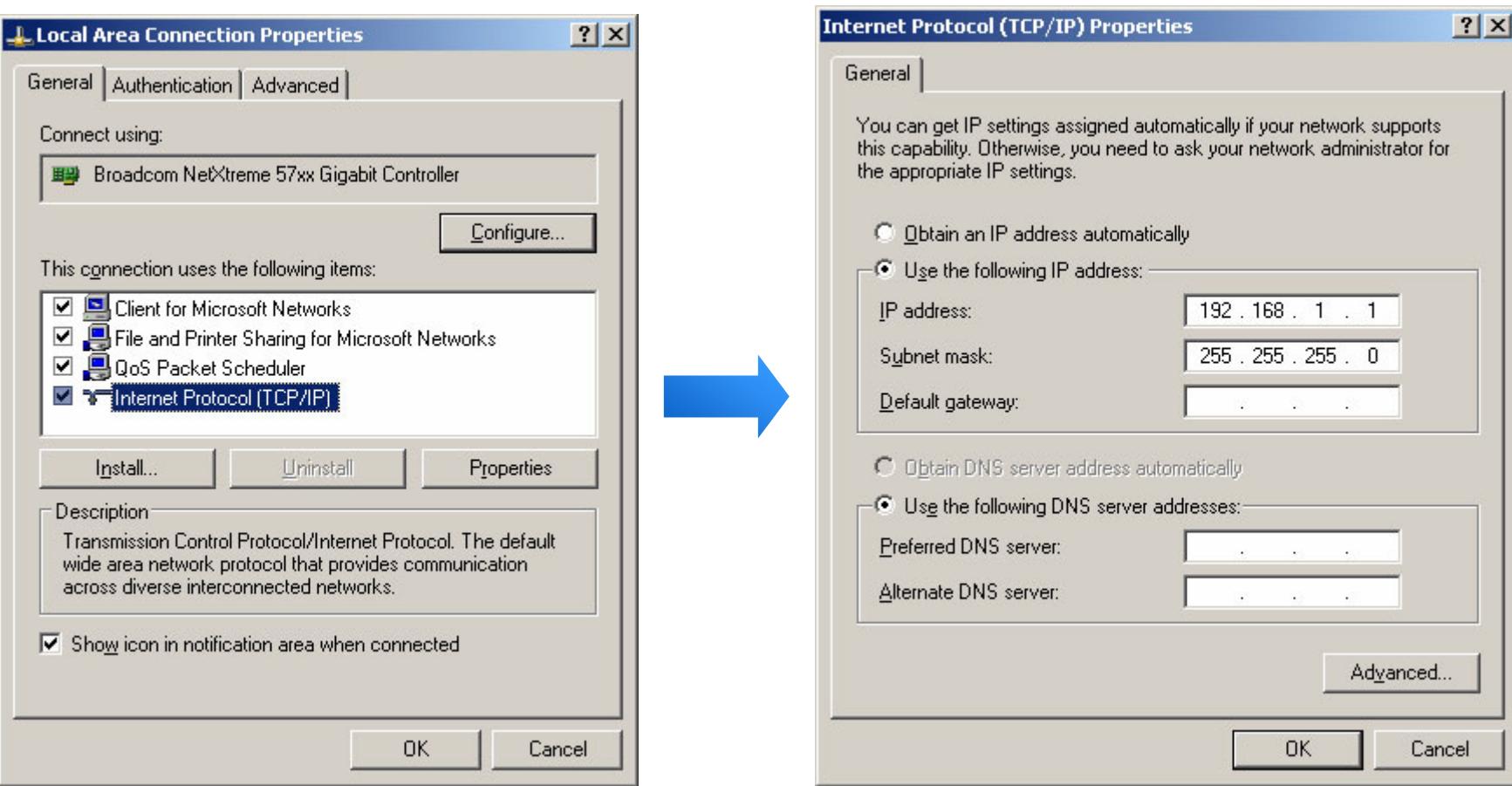
# Network Setup

- A Gigabit Ethernet Adapter on your PC is required
- In the Network Connections, right-click on the Ethernet Adapter and select Properties (1)



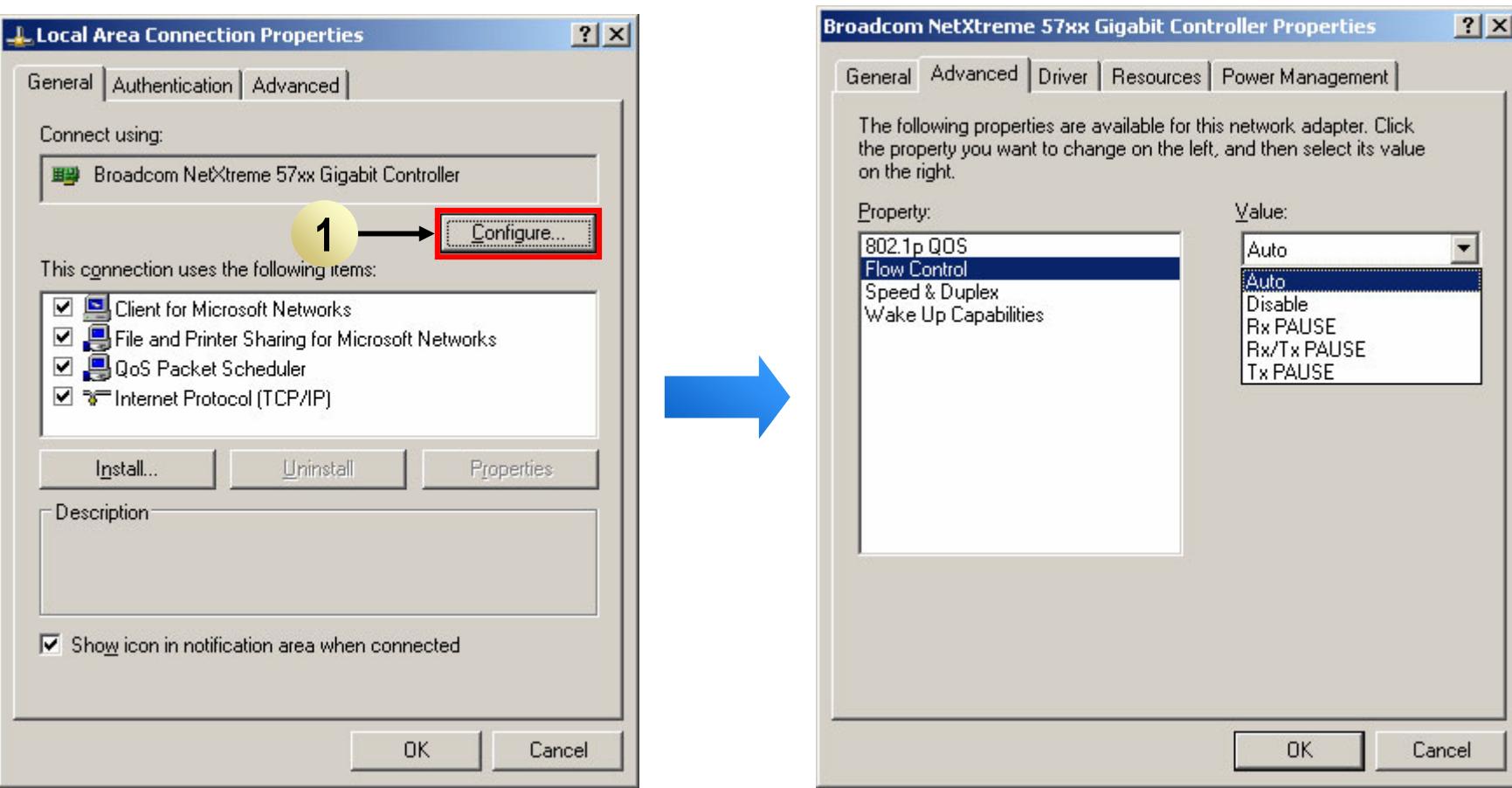
# Network Setup

- Set your host (PC) to an IP Address of 192.168.1.1:



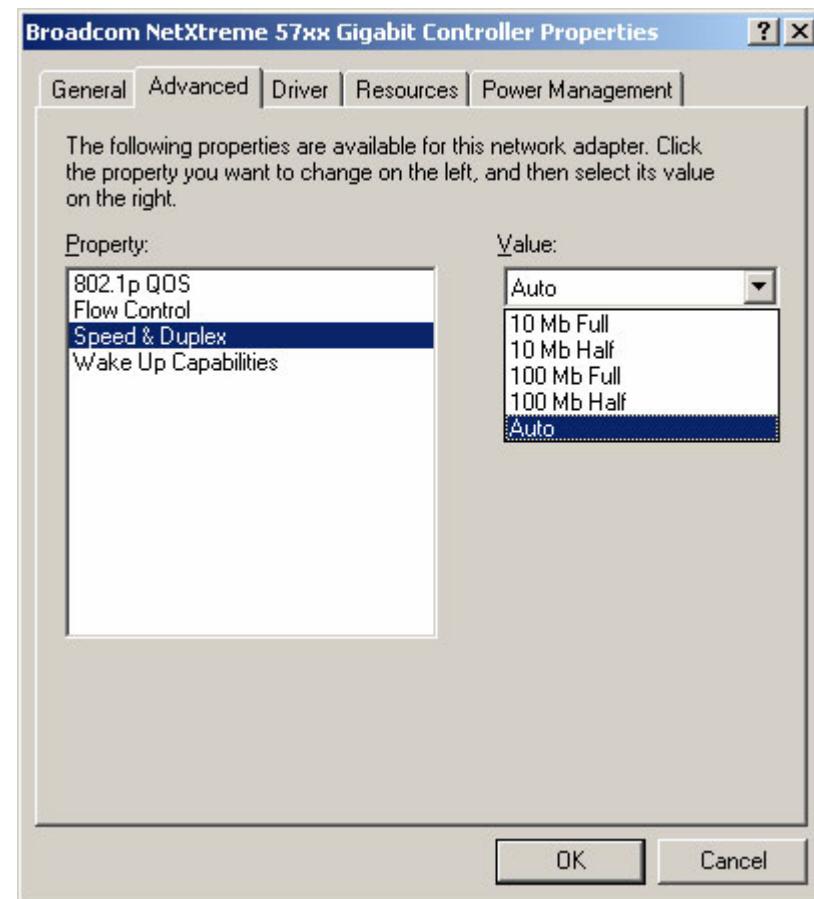
# Network Setup

- Click Configure (1)
  - Set the Flow Control to Auto



# Network Setup

- Set Speed & Duplex to Auto



# Network Setup

- Connect an Ethernet cable from the top ML510 Ethernet port to the Gigabit Ethernet Adapter



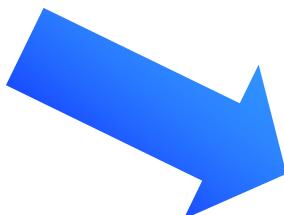
# ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



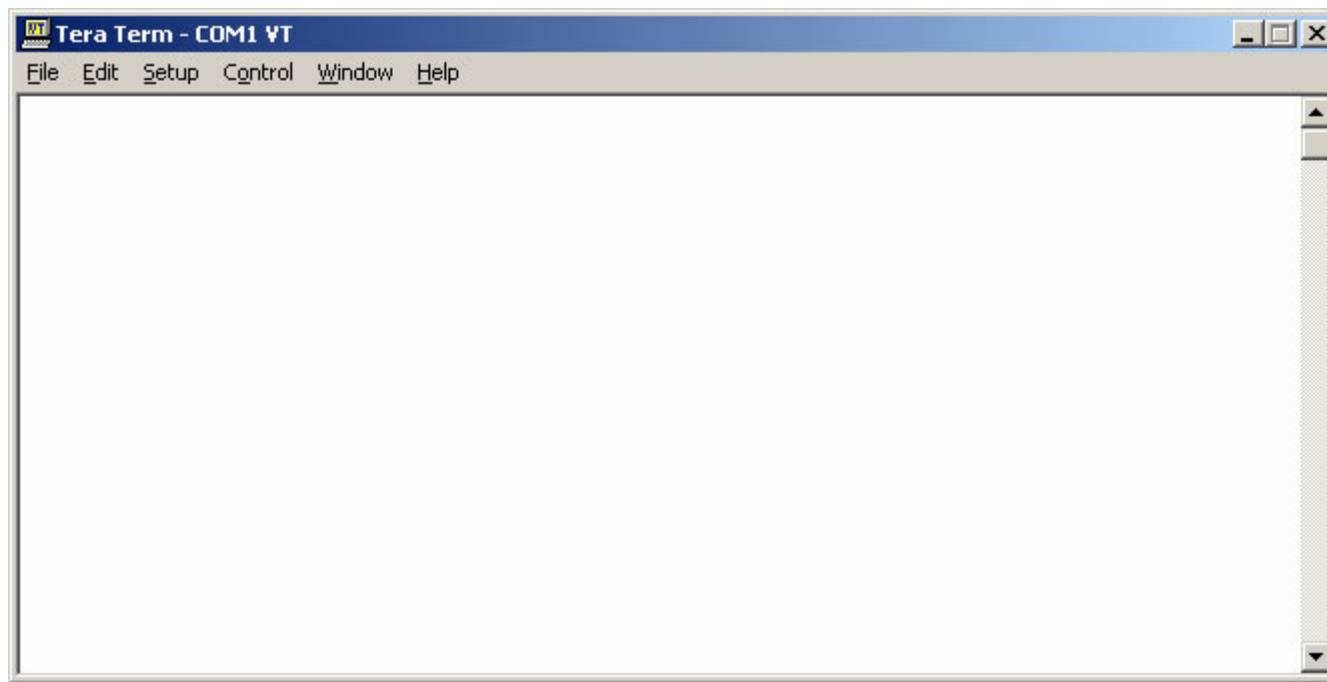
# EDK Software Requirement

- Xilinx EDK 10.1i SP3 software



# Software Setup

- Start the Terminal Program:



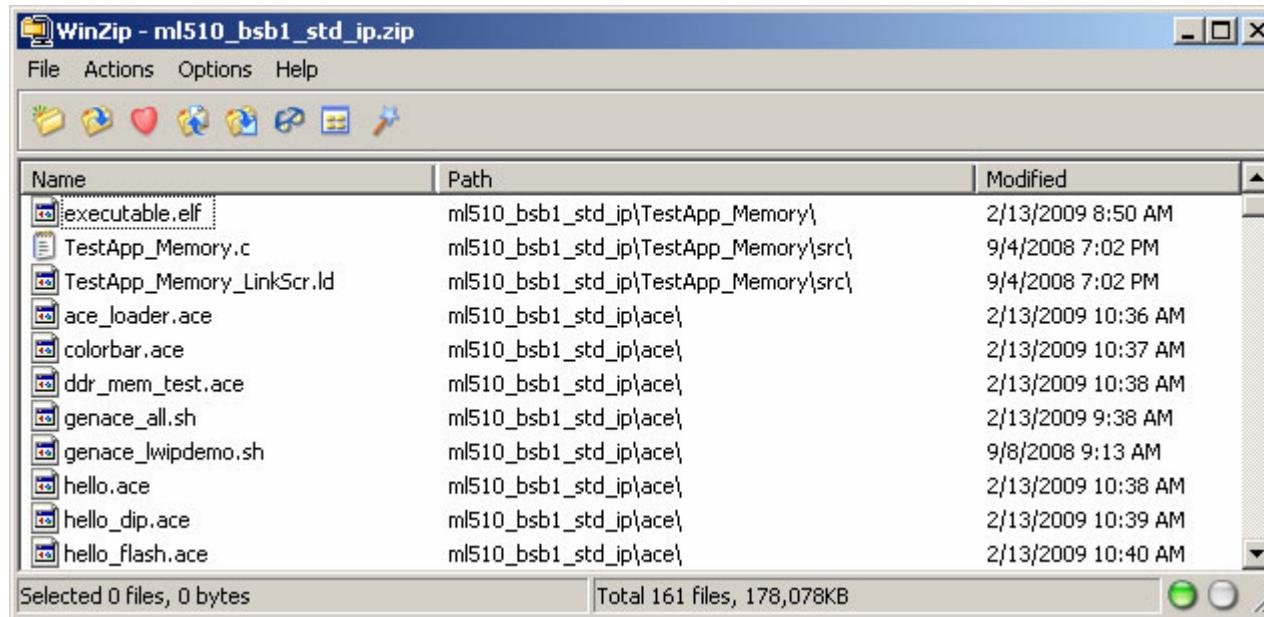
# Using the Pre-Built Design

- Unzip **ml510\_bsb1\_pccores.zip** and locate pre-built bitstream and executable software files:
  - ml510\_bsb1\_pccores/implementation/download.bit**
  - ml510\_bsb1\_pccores/microblaze\_0/code/\*.elf**
- Configure FPGA
  - Launch XPS project, **ml510\_bsb\_system.xmp**
  - From the menu, select **Project → Launch EDK Shell** and type:  
**impact -batch etc/download.cmd**
  - Go to [Slide 62](#), to run the software application
- For a tutorial on how to create the contents of the **ml510\_bsb1\_pccores.zip** continue to the next slide



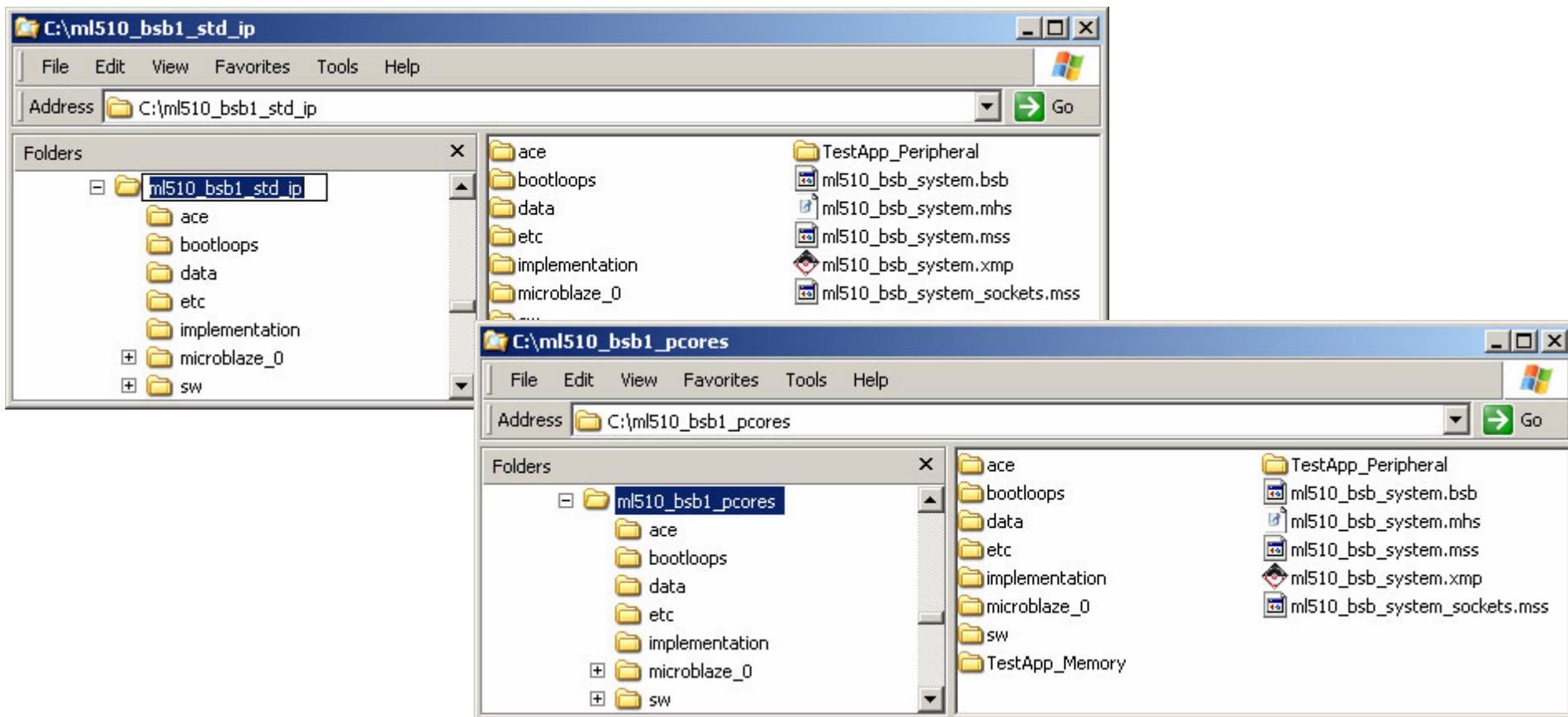
# Extracting the Design

- Unzip the ml510\_bsb1\_std\_ip.zip file
  - This creates ISE and EDK project directories



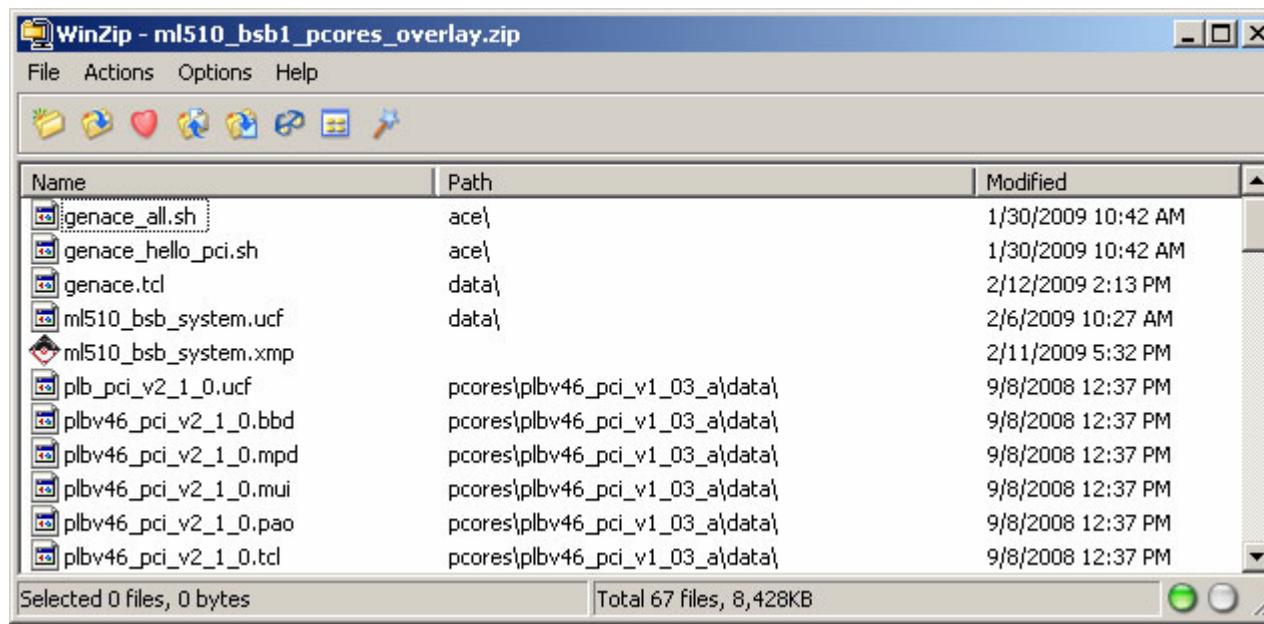
# Extracting the Design

- Rename the project directory to ml510\_bsb1\_pccores



# Extracting the Design

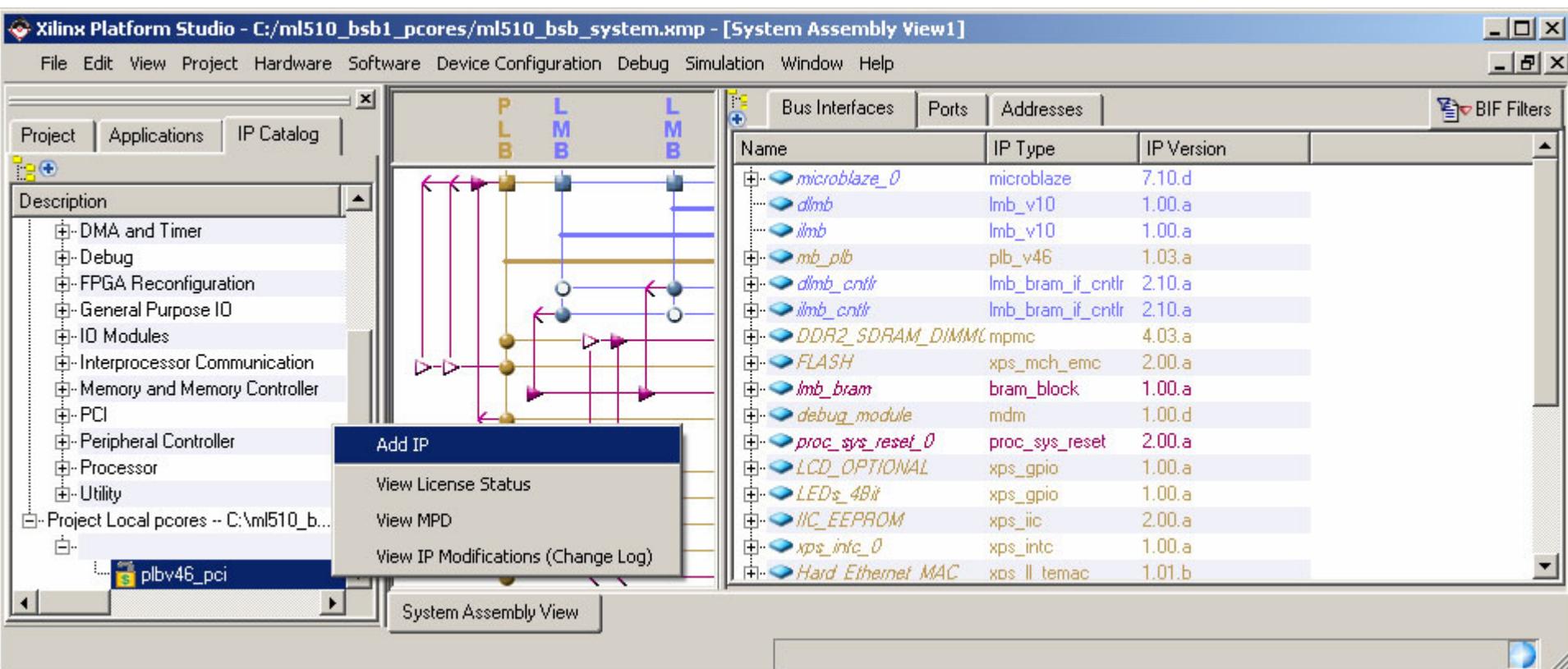
- Unzip the ml510\_bsb1\_pccores\_overlay.zip file
  - Unzip to the ml510\_bsb1\_pccores directory
  - Includes fix for AR 31638 – PCI BAR Mislabeling
  - This adds pccores, software and updated UCF files to the design directory



# Add and Configure IP

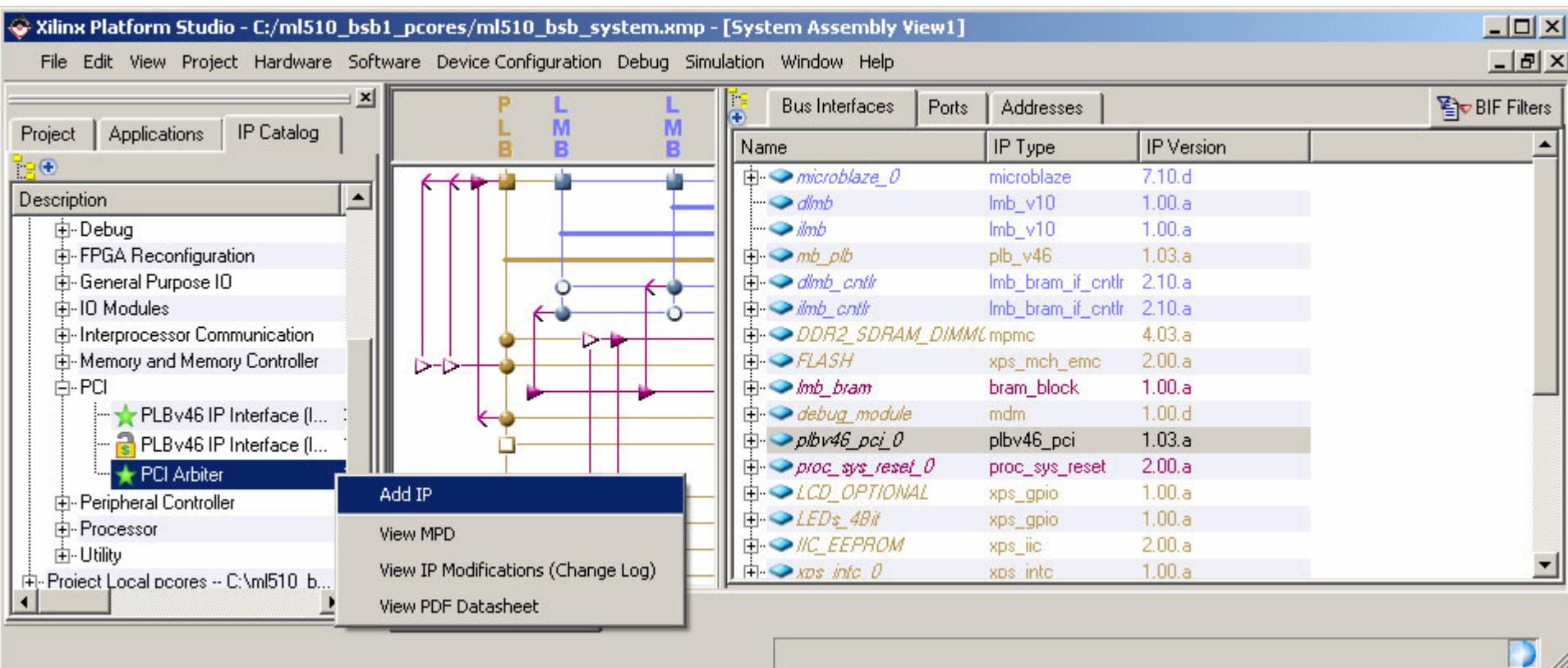
# Add Pcores

- Launch EDK project <design path>\ml510\_bsb\_system.xmp
- Right-click on the **plbv46\_pci** and select **Add IP...**



# Add Pcores

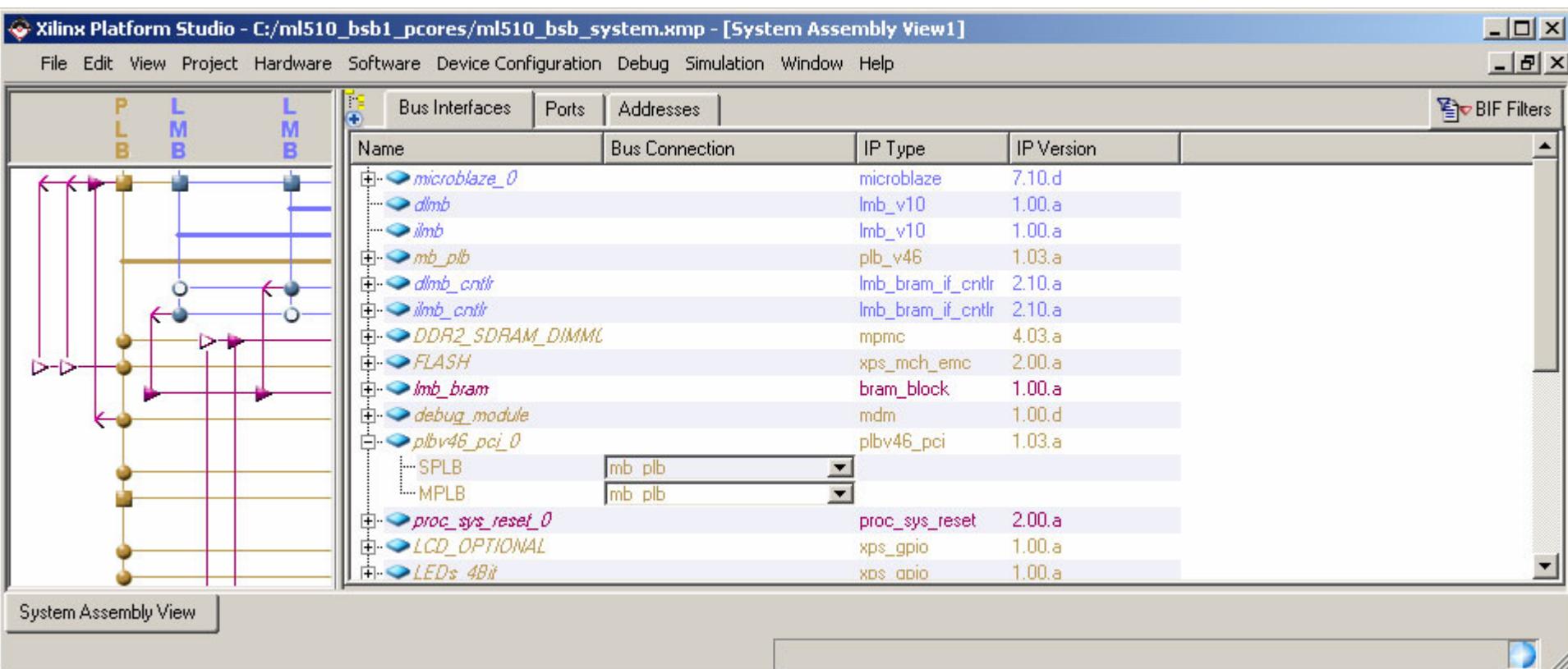
- Right-click on the PCI Arbiter and select Add IP...



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# Connect Buses

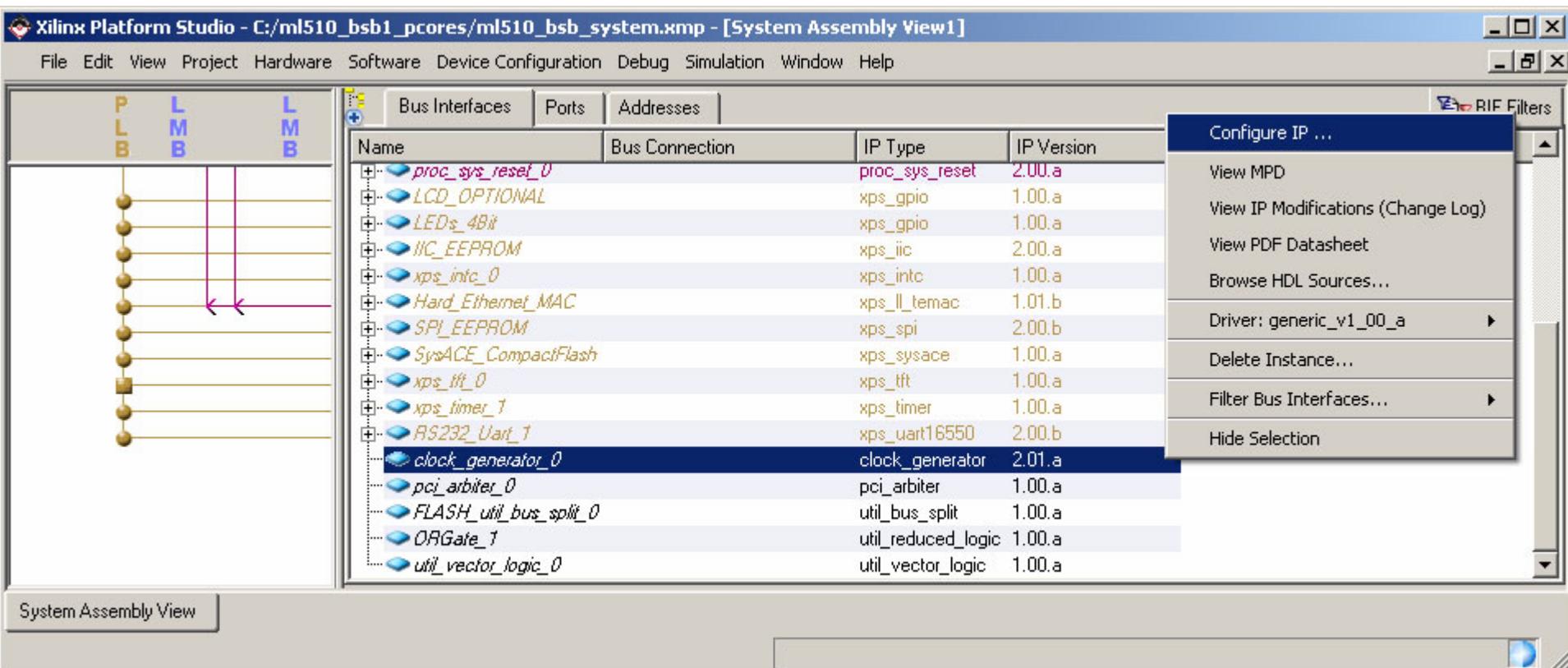
- Connect the PLB buses on the **plbv46\_pci\_0**
  - SPLB to **plib\_v46\_0**
  - MPLB to **plib\_v46\_0**



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# Configure IP

- Right-click on the clock\_generator\_0 and select Configure IP...

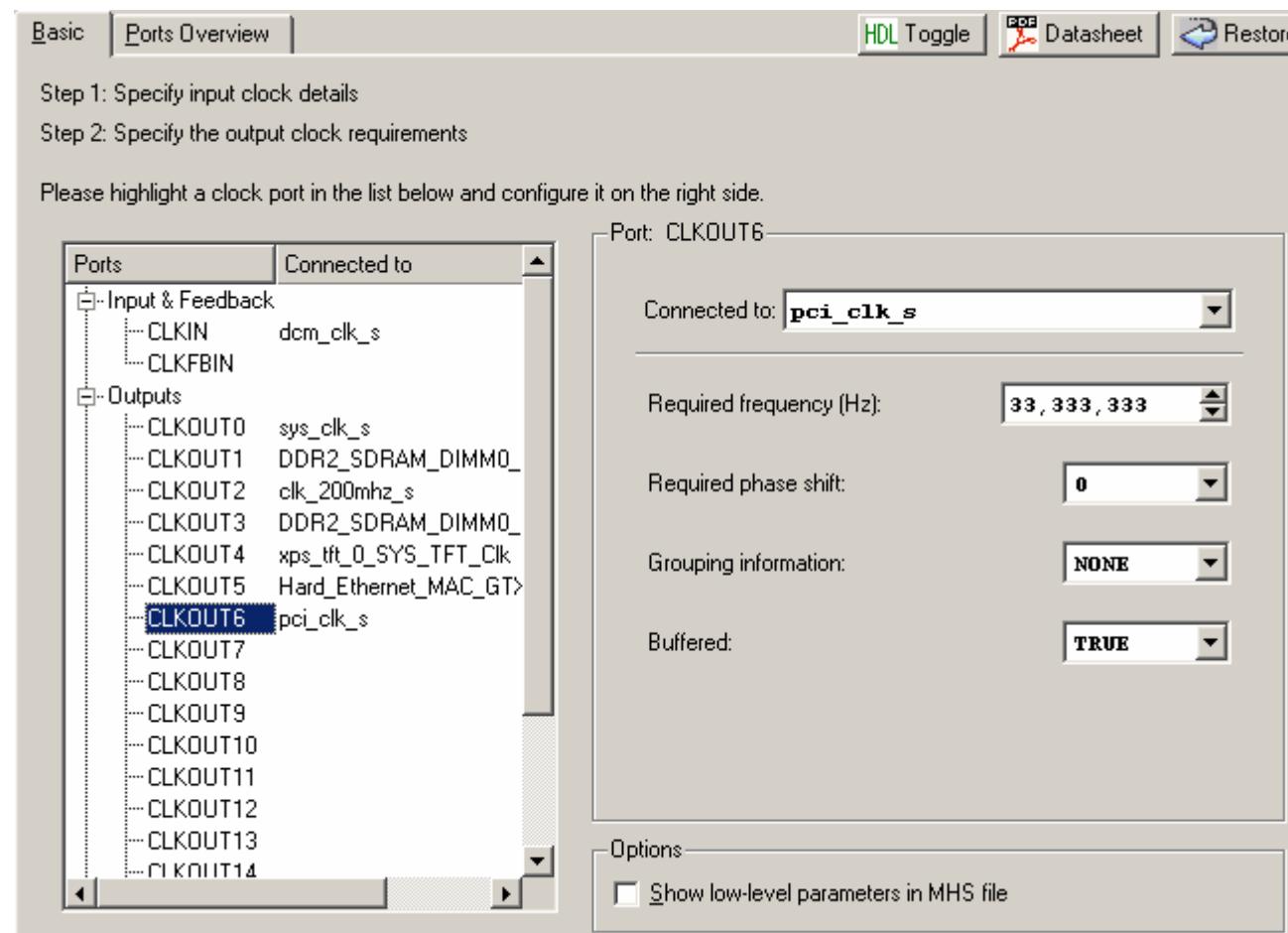


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# Configure IP

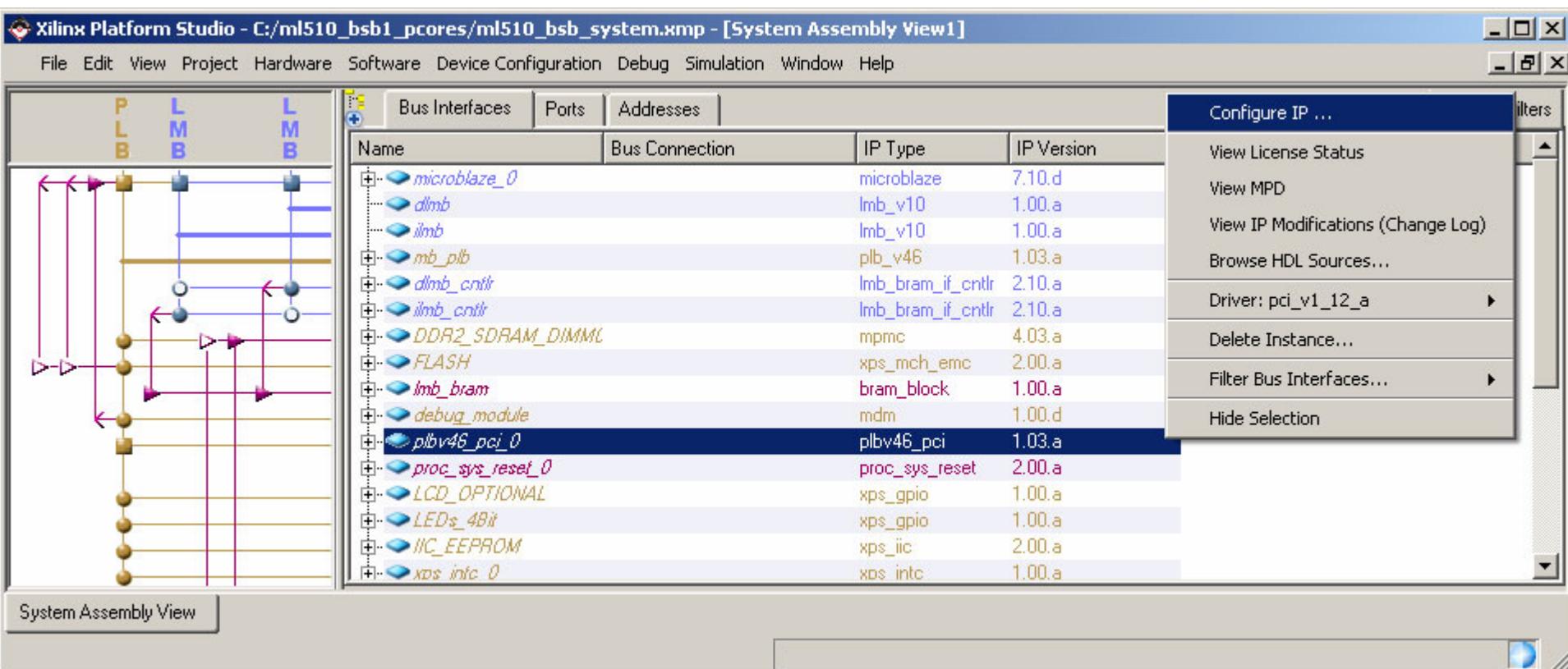
- Connect CLKOUT6 to net pci\_clk\_s

- Set the frequency to  
**33,333,333 MHz**



# Configure IP

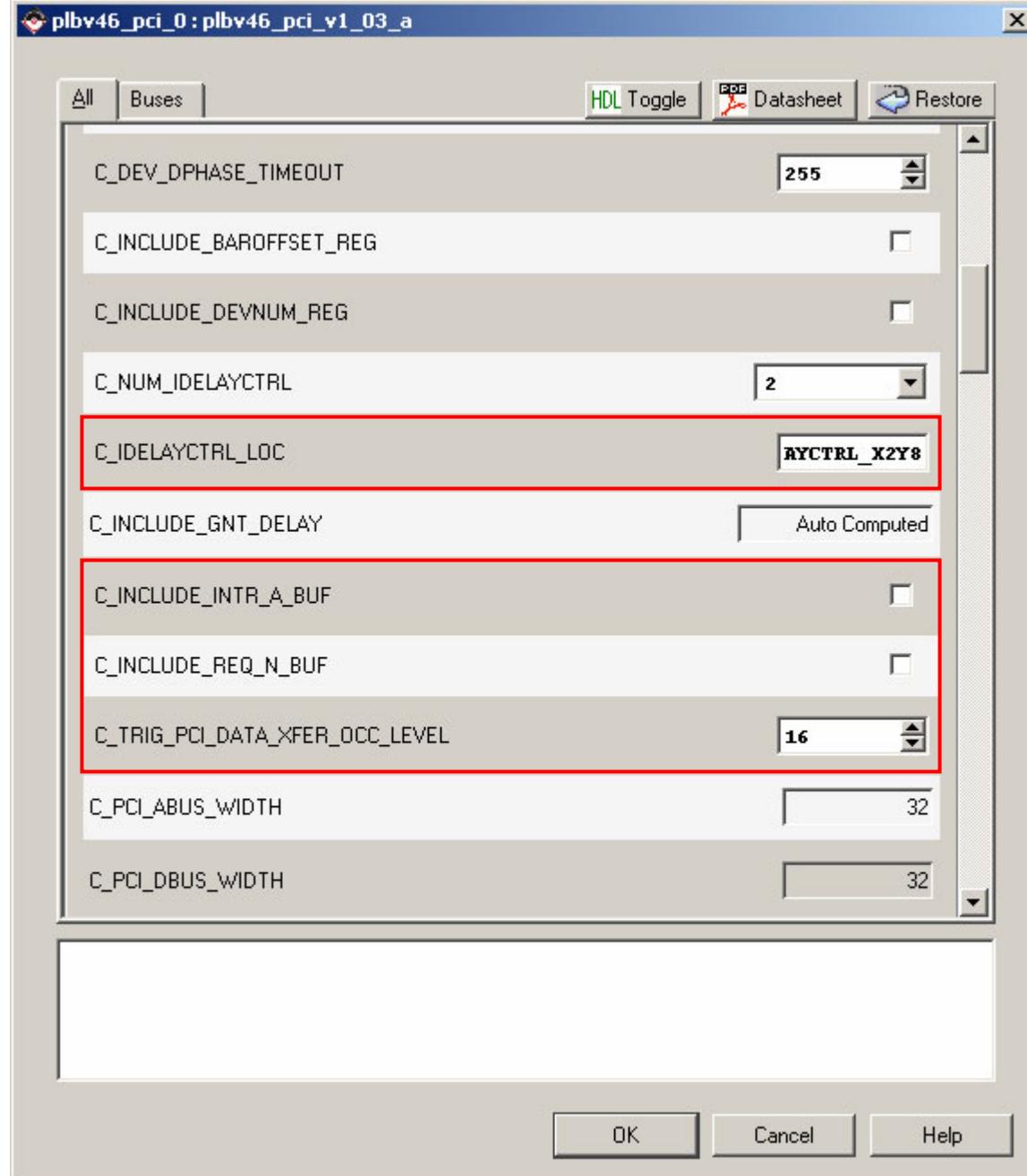
- Right-click on the `plbv46_pci_0` and select **Configure IP...**



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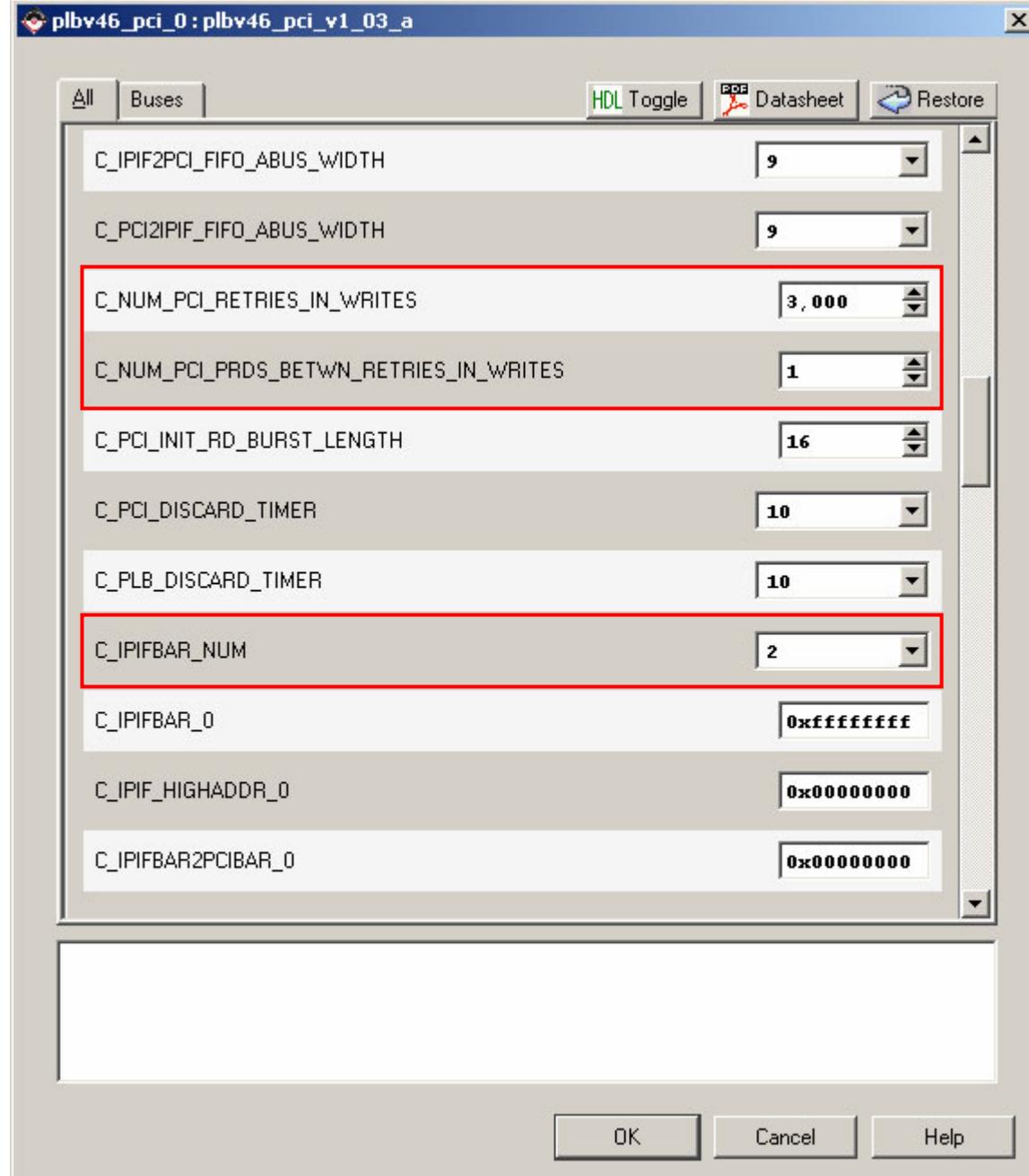
# Configure IP

- Under the All tab, make the following settings:
  - Set IDELAYCTRL LOCs to **IDELAYCTRL\_X2Y7-IDELAYCTRL\_X2Y8**
  - De-select **INTR\_A** and **REQ\_N** IO-buffers
  - Set IPIF2PCI OCC to **16**



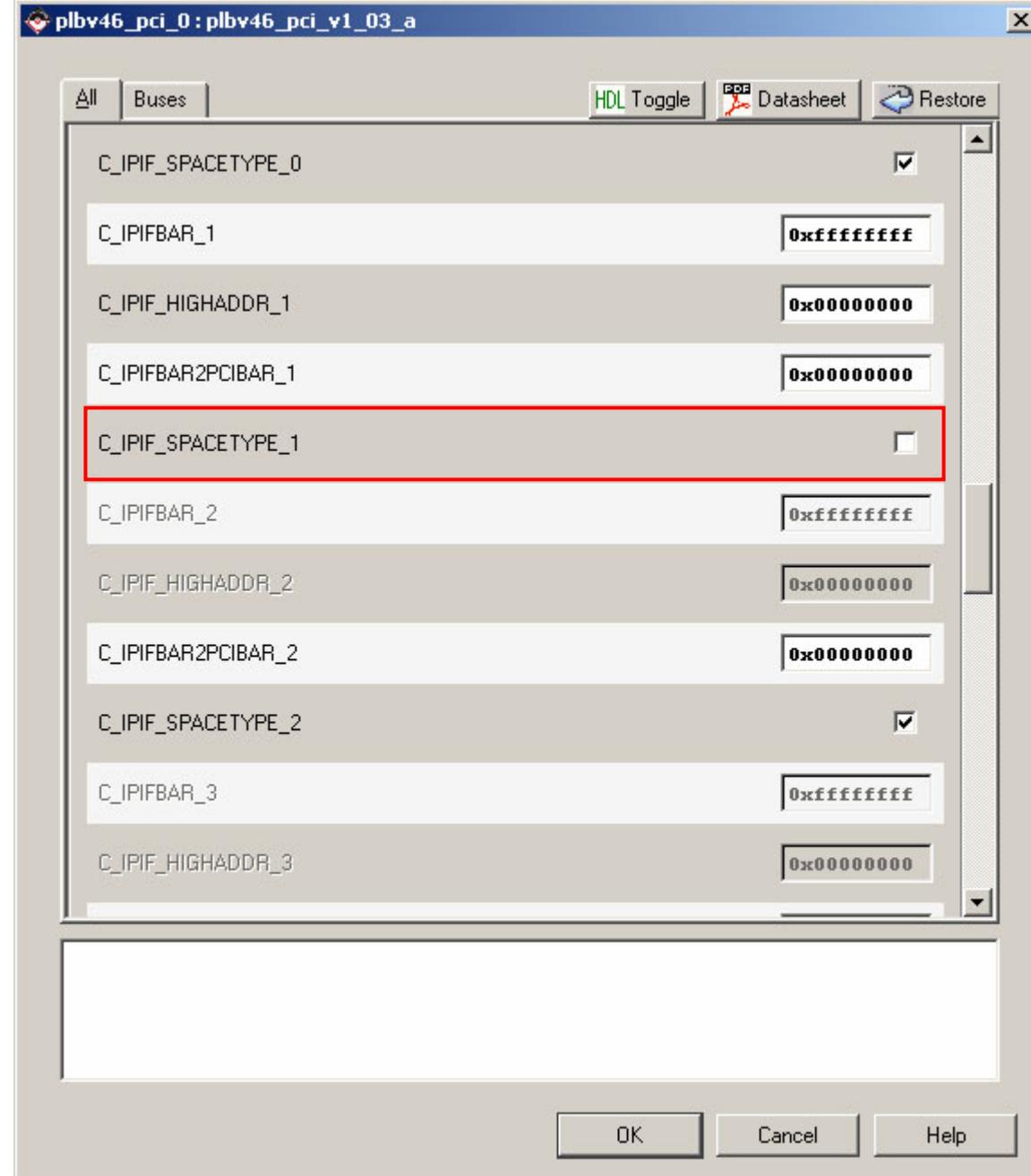
# Configure IP

- Under the All tab, make the following settings:
  - Retry attempts: 3,000
  - Clocks between retries: 1
  - Number IPIF Devices: 2



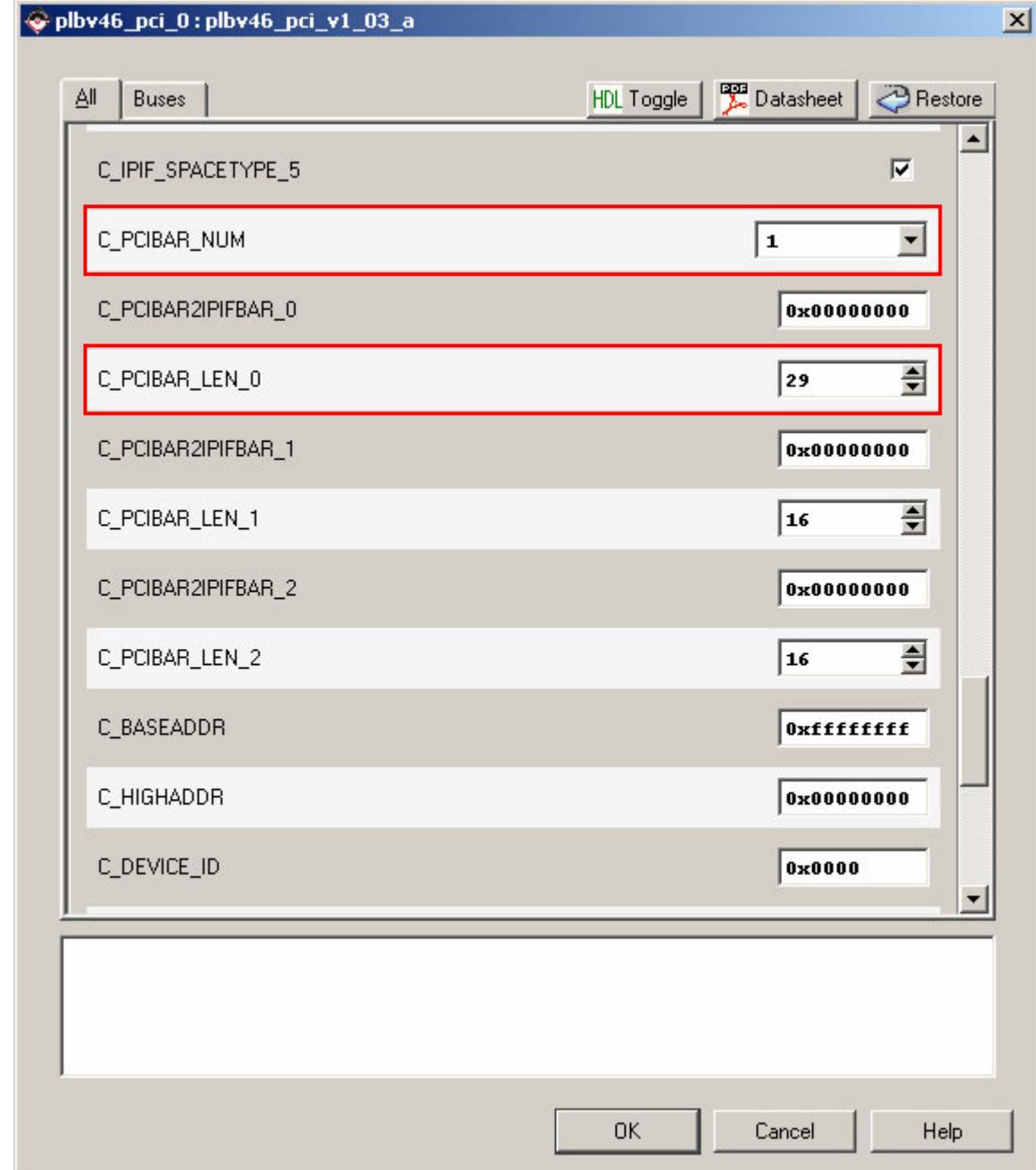
# Configure IP

- Under the All tab,  
de-select IPIF BAR1  
Memory Designator
  - Set BAR1 to **I/O Space**



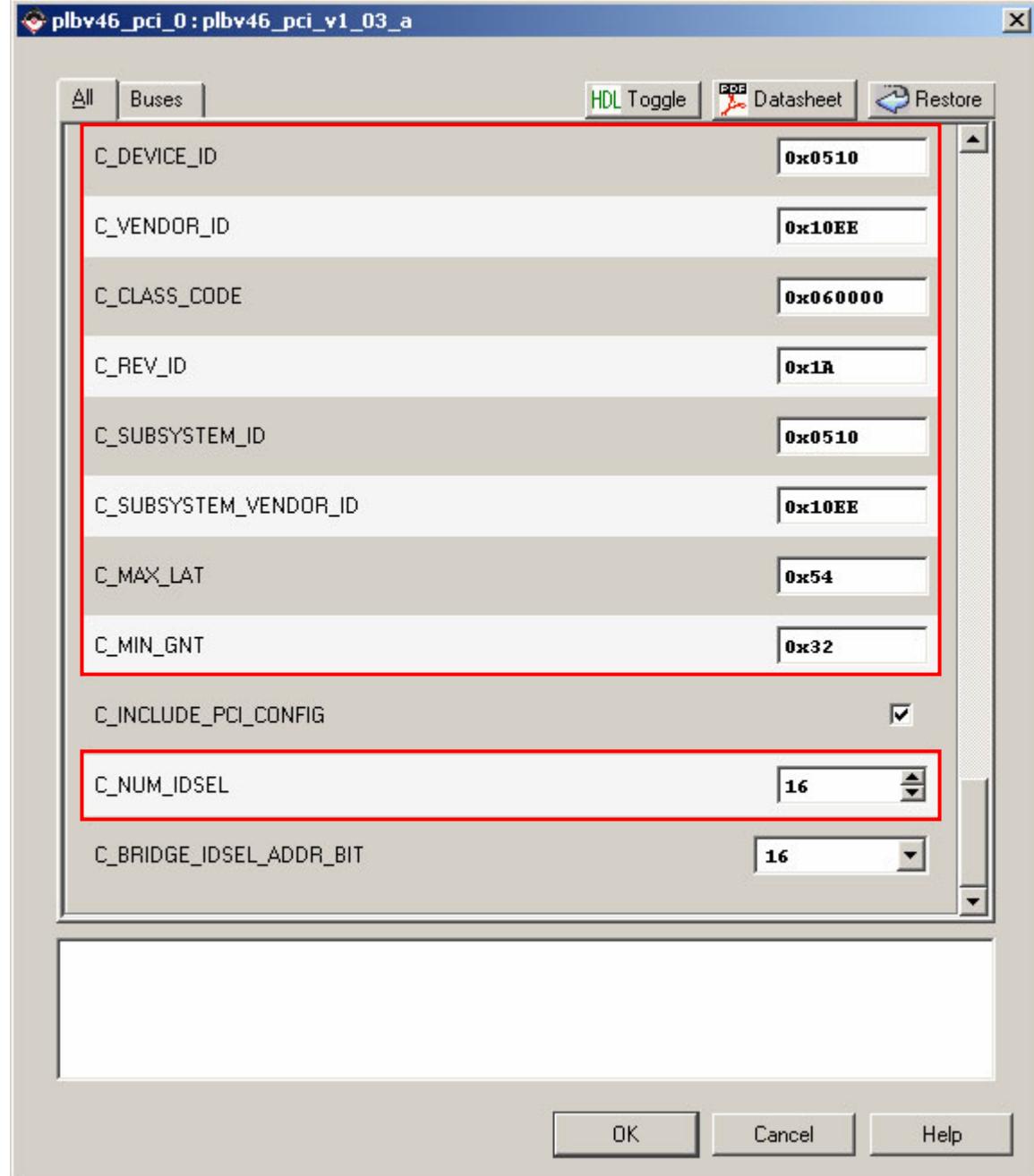
# Configure IP

- Under the All tab:
  - Number PCI Devices: 1
  - Set Power of 2 for PCI BAR0 to 29



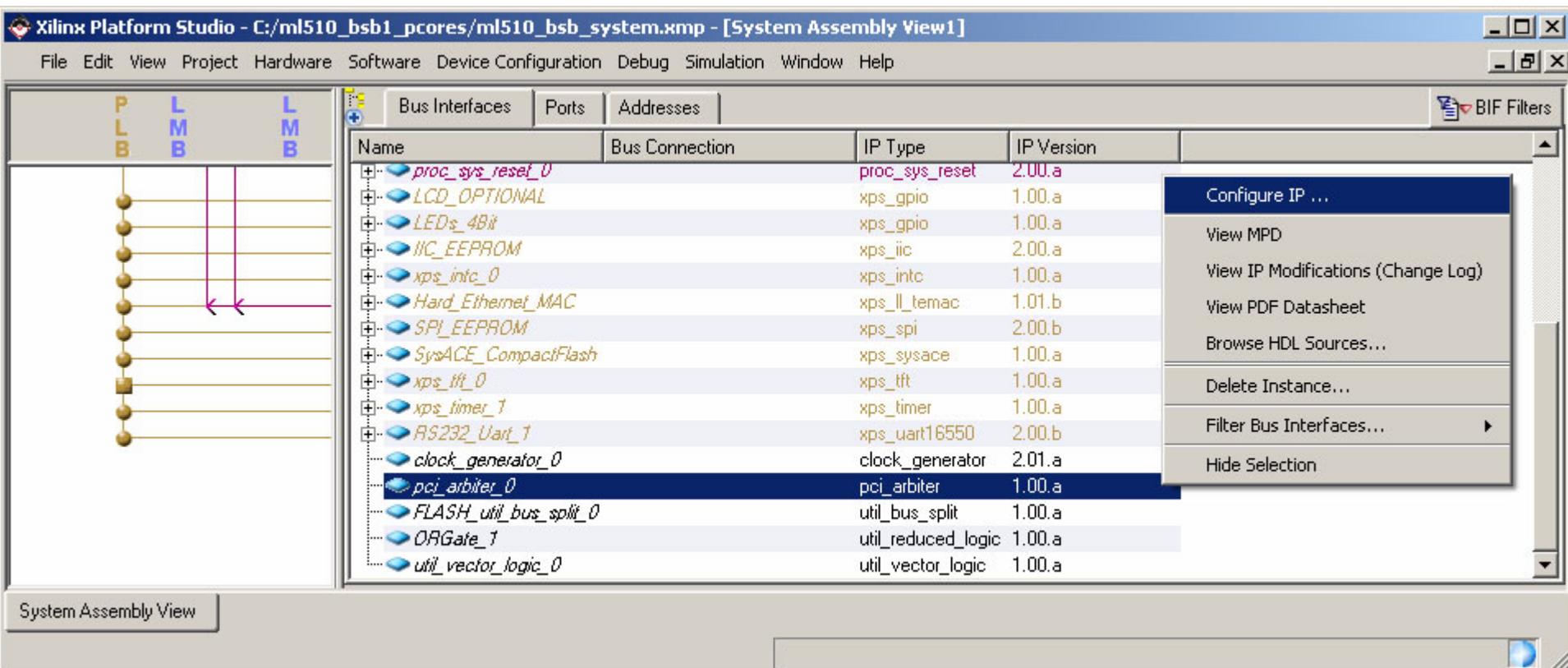
# Configure IP

- Under the All tab, make the following settings:
  - Device ID: **0x0510**
  - Vendor ID: **0x10EE**
  - Class Code: **0x060000**
  - Rev ID: **0x1A**
  - Subsystem ID: **0x0510**
  - Subsystem Vendor ID: **0x10EE**
  - Max Latency: **0x54**
  - Min Grant: **0x32**
  - Number IDSEL: **16**



# Configure IP

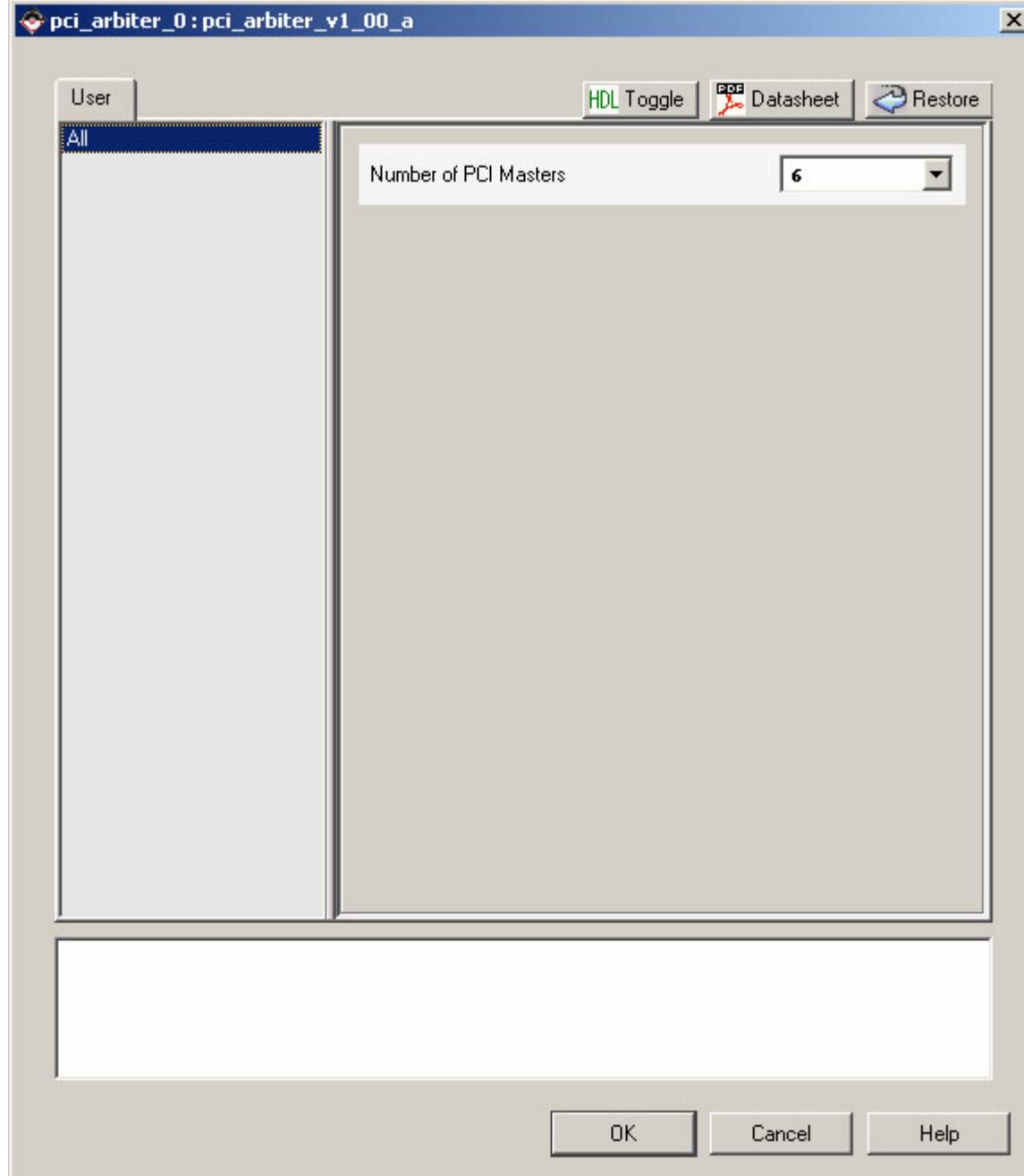
- Right-click on the **pci\_arbiter\_0** and select **Configure IP...**



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# Configure IP

- Under the All tab, set the Number of PCI Masters to 6

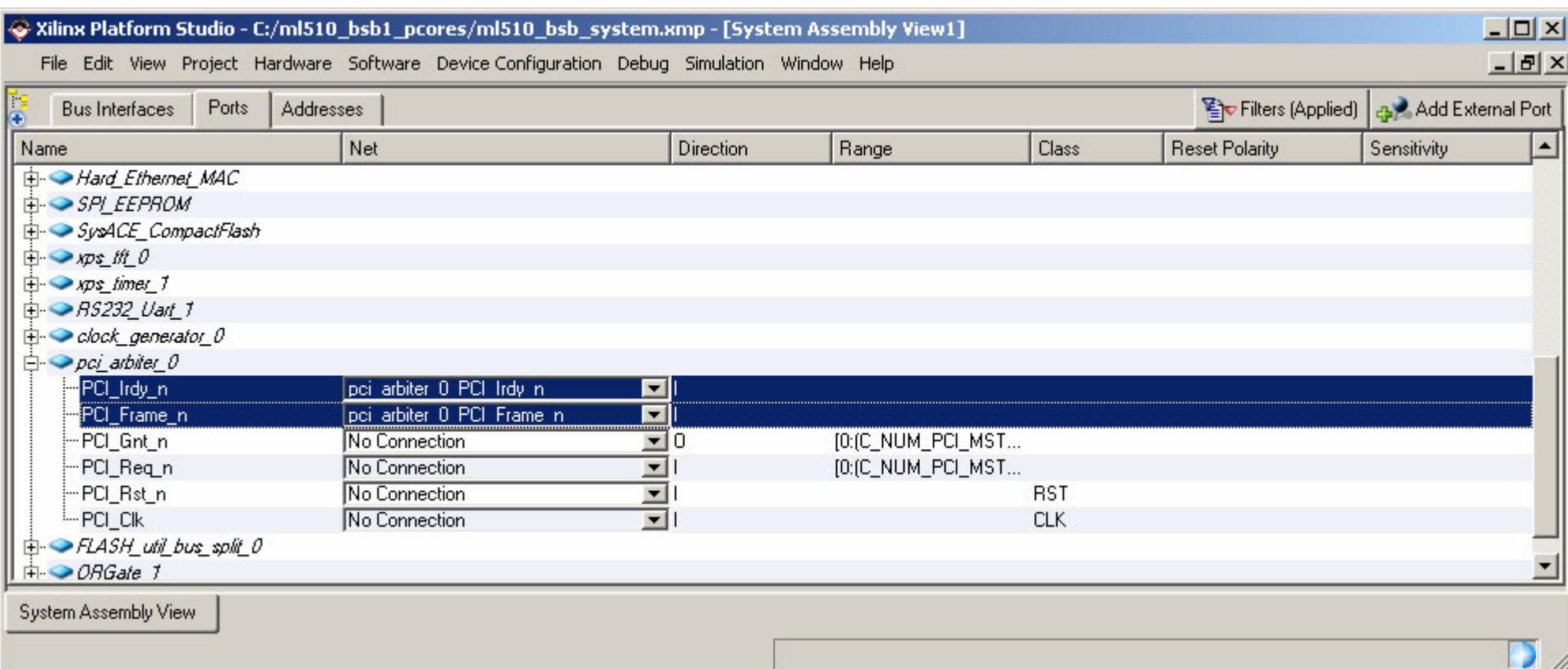


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# Add External Ports

# Connect PCI IP

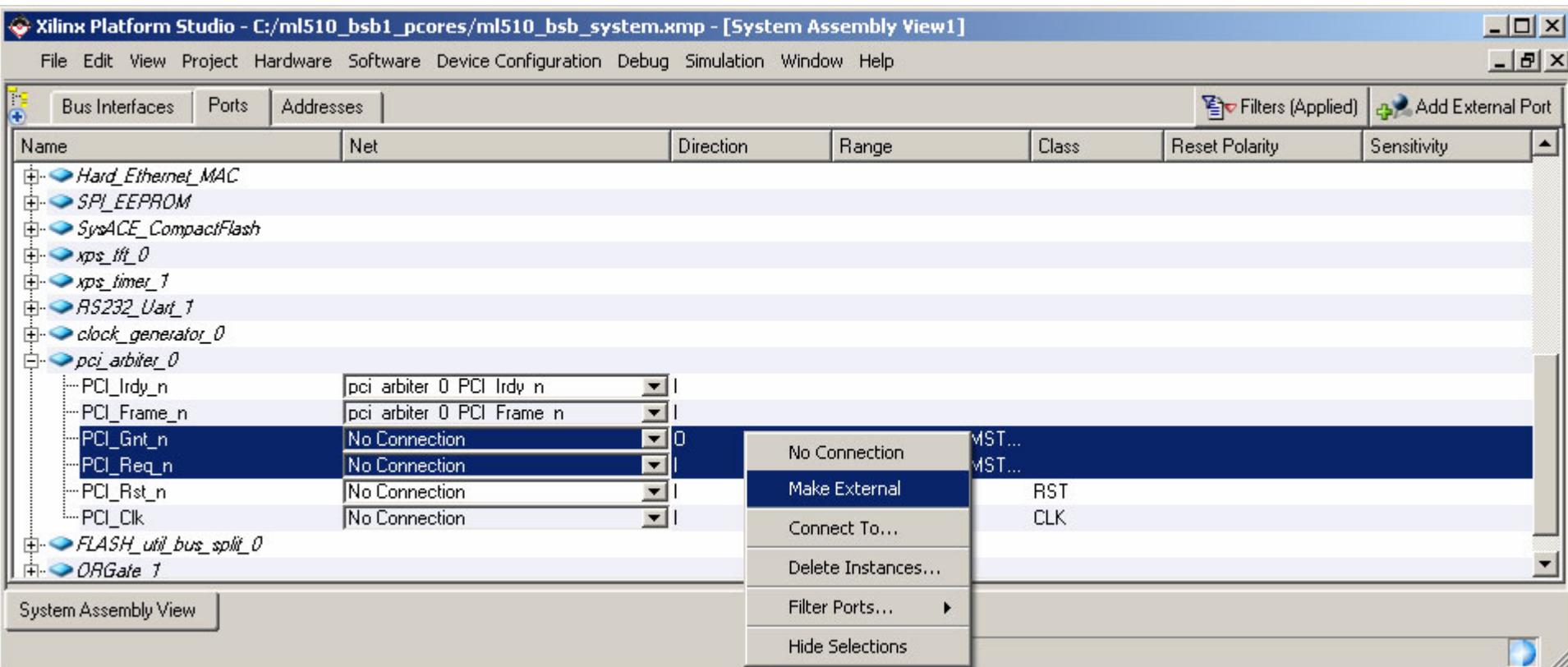
- Under the Ports tab, expand **pci\_arbiter\_0**
- Select New Connection for **PCI\_Irdy\_n** and **PCI\_Frame\_n**



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# Connect PCI IP

- Select Make External for PCI\_Gnt\_n and PCI\_Req\_n



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# Connect PCI IP

- Connect **PCI\_Rst\_n** to **sys\_rst\_s**
- Connect **PCI\_Clk** to **pci\_feedback\_s**

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
+ Hard_Ethernet_MAC						
+ SPI EEPROM						
+ SysACE_CompactFlash						
+ xps_ifi_0						
+ xps_timer_7						
+ RS232_Uart_1						
+ clock_generator_0						
- pci_arbiter_0						
PCI_Irty_n	pci arbiter 0 PCI Irty n					
PCI_Frame_n	pci arbiter 0 PCI Frame n					
PCI_Gnt_n	pci arbiter 0 PCI Gnt n		0	[0:(C_NUM_PCI_MST...]		
PCI_Req_n	pci arbiter 0 PCI Req n			[0:(C_NUM_PCI_MST...]		
PCI_Rst_n	sys rst s			RST		
PCI_Clk	pci feedback s			CLK		
+ FLASH_util_bus_split_0						
+ ORGate_1						

System Assembly View



# Connect PCI IP

- Expand `plbv46_pci_0` and select New Connection for **IP2INTC\_Irpt**, **REQ\_N\_toArb**, and **GNT\_N**

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
plbv46_pci_0						
IP2INTC_Irpt	plbv46_pci_0 IP2INTC_Irpt	0		INTERRUPT		LEVEL_HIGH
PCI_monitor	No Connection	0	[0:(12 + C_PCI_DBUS...]			
IRDY_I	No Connection	0				
FRAME_I	No Connection	0				
REQ_N_toArb	plbv46_pci_0 REQ_N_toArb	0				
INTR_A_int	No Connection	0				
BusPCI_INTR	No Connection	1				
RCLK	No Connection	1				
PCLK	No Connection	1				
RST_N	No Connection	1				
GNT_N	plbv46_pci_0 GNT_N	1				
REQ_N	No Connection	0				
SERR_N	No Connection	10				
PERR_N	No Connection	10				
INTR_A	No Connection	0				



# Connect PCI IP

- Connect these ports to these nets:
  - IRDY\_I to pci\_arbiter\_0\_PCI\_Irdy\_n
  - FRAME\_I to pci\_arbiter\_0\_PCI\_Frame\_n

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
plbv46_pci_0						
IP2INTC_Irpt	plbv46_pci_0_IP2INTC_Irpt	0		INTERRUPT		LEVEL_HIGH
PCI_monitor	No Connection	0	[0:(12 + C_PCI_DBUS...)			
IRDY_I	pci arbiter 0 PCI_Irdy_n	0				
FRAME_I	pci arbiter 0 PCI_Frame_n	0				
REQ_N_toArb	plbv46_pci_0_REQ_N_toArb	0				
INTR_A_int	No Connection	0				
Bus2PCI_INTR	No Connection	1				
RCLK	No Connection	1				
PCLK	No Connection	1				
RST_N	No Connection	1				
GNT_N	plbv46_pci_0_GNT_N	1				
REQ_N	No Connection	0				
SERR_N	No Connection	10				
PERR_N	No Connection	10				
INTR_A	No Connection	0				

System Assembly View



# Connect PCI IP

- Connect these ports to these nets:
  - RCLK to **clk\_200mhz\_s**
  - PCLK to **pci\_feedback\_s**

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
plbv46_pci_0						
IP2INTC_Irpt	plbv46 pci 0 IP2INTC Irpt	0		INTERRUPT		LEVEL_HIGH
PCI_monitor	No Connection	0	[0:(12 + C_PCI_DBUS...)			
IRDY_I	pci arbiter 0 PCI Irdy n	0				
FRAME_I	pci arbiter 0 PCI Frame n	0				
REQ_N_toArb	plbv46 pci 0 REQ_N toArb	0				
INTR_A_int	No Connection	0				
Bus2PCI_INTR	No Connection	1				
RCLK	clk_200mhz_s	1				
PCLK	pci feedback_s	1				
RST_N	No Connection	1				
GNT_N	plbv46 pci 0 GNT_N	1				
REQ_N	No Connection	0				
SERR_N	No Connection	10				
PERR_N	No Connection	10				
INTR_A	No Connection	0				

System Assembly View



# Connect PCI IP

- Connect these ports to these nets:
  - RST\_N to sys\_rst\_s

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

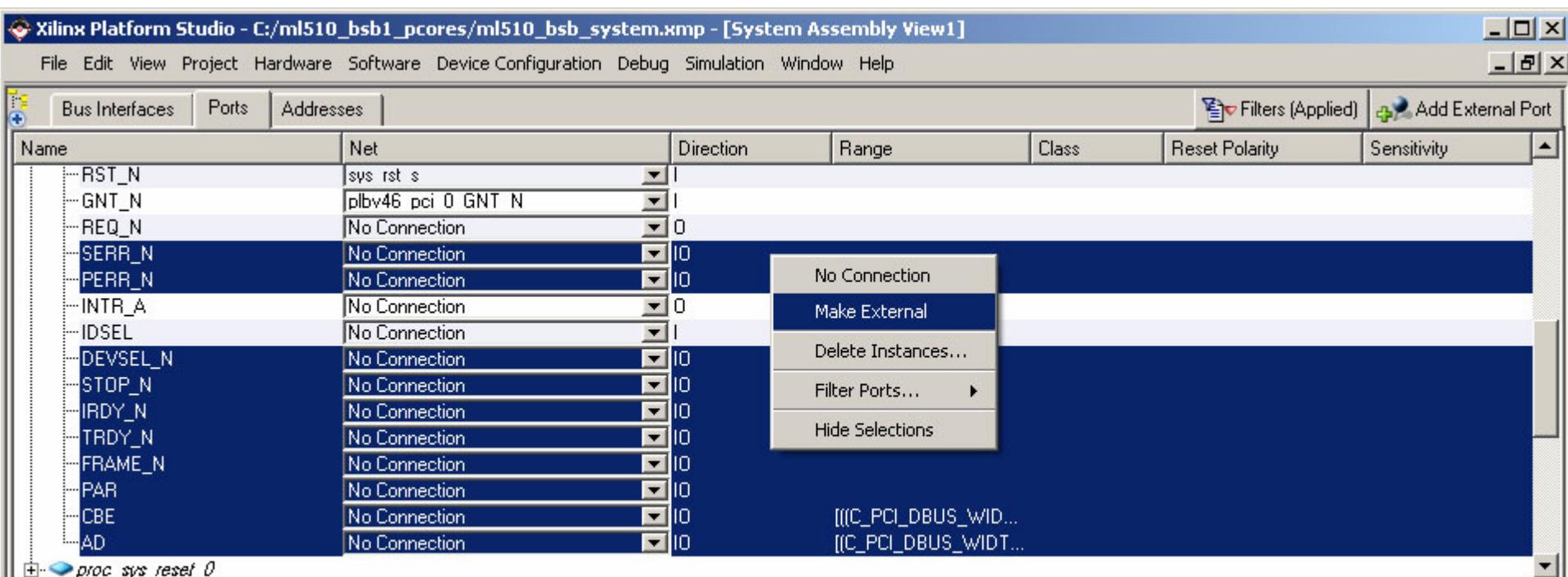
Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
plbv46_pci_0						
IP2INTC_Irpt	plbv46 pci 0 IP2INTC Irpt	0		INTERRUPT		LEVEL_HIGH
PCI_monitor	No Connection	0	[0:(12 + C_PCI_DBUS...)			
IRDY_I	pci arbiter 0 PCI Irdy n	0				
FRAME_I	pci arbiter 0 PCI Frame n	0				
REQ_N_toArb	plbv46 pci 0 REQ_N_toArb	0				
INTR_A_int	No Connection	0				
Bus2PCI_INTR	No Connection	1				
RCLK	clk_200mhz s	1				
PCLK	pci feedback s	1				
RST_N	sys_rst_s	1				
GNT_N	plbv46 pci 0 GNT_N	1				
REQ_N	No Connection	0				
SERR_N	No Connection	10				
PERR_N	No Connection	10				
INTR_A	No Connection	0				



# Connect PCI IP

- Select Make External for these ports:
  - **SERR\_N, PERR\_N, DEVSEL\_N, STOP\_N, IRDY\_N, TRDY\_N, FRAME\_N, PAR, CBE, and AD**



# Connect PCI IP

- Expand `pci_arbiter_0` and *prepend* these nets to these ports:
  - `PCI_Gnt_n`: "`plbv46_pci_0_GNT_N &`"
  - `PCI_Req_n`: "`plbv46_pci_0_REQ_N_toArb &`"

The screenshot shows the Xilinx Platform Studio interface with the title bar "Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]". The menu bar includes File, Edit, View, Project, Hardware, Software, Device Configuration, Debug, Simulation, Window, and Help. The toolbar has icons for Bus Interfaces, Ports, Addresses, Filters (Applied), and Add External Port. The main window displays the System Assembly View with a table of bus interfaces. The table columns are Name, Net, Direction, Range, Class, Reset Polarity, and Sensitivity. The table rows include Hard\_Ethernet\_MAC, SPI EEPROM, SysACE\_CompactFlash, xps\_if\_0, xps\_timer\_7, RS232\_Uart\_1, clock\_generator\_0, and pci\_arbiter\_0. The pci\_arbiter\_0 row is expanded, showing its internal ports: PCI\_Irty\_n, PCI\_Frame\_n, PCI\_Gnt\_n, PCI\_Req\_n, PCI\_Rst\_n, and PCI\_Clk. The PCI\_Gnt\_n and PCI\_Req\_n ports are highlighted in blue, indicating they have been modified. The PCI\_Gnt\_n port is connected to "plbv46\_pci\_0\_GNT\_N & pci\_arbiter\_0\_PCI\_Gnt\_n", and the PCI\_Req\_n port is connected to "plbv46\_pci\_0\_REQ\_N\_toArb & pci\_arbiter\_0\_PCI\_Req\_n". The RST and CLK columns show "RST" and "CLK" respectively.

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
Hard_Ethernet_MAC						
SPI_EEPROM						
SysACE_CompactFlash						
xps_if_0						
xps_timer_7						
RS232_Uart_1						
clock_generator_0						
pci_arbiter_0						
PCI_Irty_n	pci arbiter 0 PCI Irty n					
PCI_Frame_n	pci arbiter 0 PCI Frame n					
PCI_Gnt_n	plbv46_pci_0_GNT_N & pci arbiter 0_PCI_Gnt_n		[0:C_NUM_PCI_MST...]			
PCI_Req_n	plbv46_pci_0_REQ_N_toArb & pci arbiter 0_PCI_Req_n		[0:C_NUM_PCI_MST...]			
PCI_Rst_n	sys rst s			RST		
PCI_Clk	pci feedback s				CLK	
FLASH_util_bus_split_0						
ORGate_1						



Example: "plbv46\_pci\_0\_GNT\_N & pci\_arbiter\_0\_PCI\_Gnt\_n"

# Connect PCI IP

- Add 5 External Ports:
  - Name these ports: **PCI\_P\_CLK0\_R**, **PCI\_P\_CLK1\_R**, **PCI\_P\_CLK3\_R**, **PCI\_P\_CLK4\_R**, and **PCI\_P\_CLK5\_R**
  - Connect all 5 ports to **pci\_clk\_s**

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
External Ports						
PCI_P_CLK5_R	pci clk s	0				
PCI_P_CLK4_R	pci clk s	0				
PCI_P_CLK3_R	pci clk s	0				
PCI_P_CLK1_R	pci clk s	0				
PCI_P_CLK0_R	pci clk s	0				
plbv46_pci_0_AD	plbv46 pci 0 AD	I/O	[31:0]			
plbv46_pci_0_CBE	plbv46 pci 0 CBE	I/O	[3:0]			
plbv46_pci_0_PAR	plbv46 pci 0 PAR	I/O				
plbv46_pci_0_FRAME_N	plbv46 pci 0 FRAME N	I/O				
plbv46_pci_0_TRDY_N	plbv46 pci 0 TRDY N	I/O				
plbv46_pci_0_IRDY_N	plbv46 pci 0 IRDY N	I/O				
plbv46_pci_0_STOP_N	plbv46 pci 0 STOP N	I/O				
plbv46_pci_0_DEVSEL_N	plbv46 pci 0 DEVSEL N	I/O				
plbv46_pci_0_PERR_N	plbv46 pci 0 PERR N	I/O				
plbv46_pci_0_SERR_N	plbv46 pci 0 SERR N	I/O				

System Assembly View



# Connect PCI IP

- Add an External Port, name this port: **PCI\_P\_CLK5**
  - Connect to net **pci\_feedback\_s**, set Direction to **I**, set Class to **CLK**, Frequency to **33333333**

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Frequency	Sensitivity
External Ports						
PCI_P_CLK5	pci_feedback_s	I		CLK	33333333	
PCI_P_CLK5_R	pci_clk_s	O				
PCI_P_CLK4_R	pci_clk_s	O				
PCI_P_CLK3_R	pci_clk_s	O				
PCI_P_CLK1_R	pci_clk_s	O				
PCI_P_CLK0_R	pci_clk_s	O				
plbv46_pci_0_AD	plbv46 pci 0 AD	I/O	[31:0]			
plbv46_pci_0_CBE	plbv46 pci 0 CBE	I/O	[3:0]			
plbv46_pci_0_PAR	plbv46 pci 0 PAR	I/O				
plbv46_pci_0_FRAME_N	plbv46 pci 0 FRAME_N	I/O				
plbv46_pci_0_TRDY_N	plbv46 pci 0 TRDY_N	I/O				
plbv46_pci_0_IRDY_N	plbv46 pci 0 IRDY_N	I/O				
plbv46_pci_0_STOP_N	plbv46 pci 0 STOP_N	I/O				
plbv46_pci_0_DEVSEL_N	plbv46 pci 0 DEVSEL_N	I/O				
plbv46_pci_0_PERR_N	plbv46 pci 0 PERR_N	I/O				

System Assembly View



# Connect PCI IP

- Add 4 External Ports:
  - Set the name *and* net to: **PCI\_INTA\_N**, **PCI\_INTB\_N**, **PCI\_INTC\_N**, and **PCI\_INTD\_N**
  - Set Direction to I, set Class to **INTERRUPT**, Sensitivity to **LEVEL\_LOW**

The screenshot shows the Xilinx Platform Studio interface with the title bar "Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]". The menu bar includes File, Edit, View, Project, Hardware, Software, Device Configuration, Debug, Simulation, Window, and Help. The tabs at the top are Bus Interfaces, Ports (selected), and Addresses. A toolbar with icons for Filters (Applied) and Add External Port is visible. The main area is a table titled "External Ports" with columns: Name, Net, Direction, Range, Class, Reset Polarity, and Sensitivity.

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
PCI_INTD_N	PCI INTD N	I		INTERRUPT		LEVEL LOW
PCI_INTC_N	PCI INTC N	I		INTERRUPT		LEVEL LOW
PCI_INTB_N	PCI INTB N	I		INTERRUPT		LEVEL LOW
PCI_INTA_N	PCI INTA N	I		INTERRUPT		LEVEL LOW
PCI_P_CLK5	pci feedback s	I		CLK		
PCI_P_CLK5_R	pci clk s	I/O				
PCI_P_CLK4_R	pci clk s	I/O				
PCI_P_CLK3_R	pci clk s	I/O				
PCI_P_CLK1_R	pci clk s	I/O				
PCI_P_CLK0_R	pci clk s	I/O				
plbv46_pci_0_AD	plbv46 pci 0 AD	I/O	[31:0]			
plbv46_pci_0_CBE	plbv46 pci 0 CBE	I/O	[3:0]			
plbv46_pci_0_PAR	plbv46 pci 0 PAR	I/O				
plbv46_pci_0_FRAME_N	plbv46 pci 0 FRAME N	I/O				
plbv46_pci_0_TRDY_N	plbv46 pci 0 TRDY N	I/O				



# Connect PCI IP

- Add this Interrupt port: **PCI\_SBR\_INT**
  - Set the Direction to I and the Sensitivity to **LEVEL\_HIGH**

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
External Ports						
PCI_SBR_INT	PCI_SBR_INT	I		INTERRUPT		LEVEL HIGH
PCI_INTD_N	PCI_INTD_N	I		INTERRUPT		LEVEL LOW
PCI_INTC_N	PCI_INTC_N	I		INTERRUPT		LEVEL LOW
PCI_INTB_N	PCI_INTB_N	I		INTERRUPT		LEVEL LOW
PCI_INTA_N	PCI_INTA_N	I		INTERRUPT		LEVEL LOW
PCI_P_CLK5	pci_feedback_s	I		CLK		
PCI_P_CLK5_R	pci_clk_s	O				
PCI_P_CLK4_R	pci_clk_s	O				
PCI_P_CLK3_R	pci_clk_s	O				
PCI_P_CLKT_R	pci_clk_s	O				
PCI_P_CLK0_R	pci_clk_s	O				
plbv46_pci_0_AD	plbv46_pci_0_AD	I/O	[31:0]			
plbv46_pci_0_CBE	plbv46_pci_0_CBE	I/O	[3:0]			
plbv46_pci_0_PAR	plbv46_pci_0_PAR	I/O				
plbv46_pci_0_FRAME_N	plbv46_pci_0_FRAME_N	I/O				



# Connect PCI IP

- Adjust the range on the PCI Request and Grant lines
  - From [0:5] to [1:5]

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
plbv46_pci_0_STOP_N	plbv46 pci 0 STOP N	I/O				
plbv46_pci_0_DEVSEL_N	plbv46 pci 0 DEVSEL N	I/O				
plbv46_pci_0_PERR_N	plbv46 pci 0 PERR N	I/O				
plbv46_pci_0_SERR_N	plbv46 pci 0 SERR N	I/O				
pci_arbiter_0_PCI_Req_n_pin	pci arbiter 0 PCI Req n	I	[1:5]			
pci_arbiter_0_PCI_Gnt_n_pin	pci arbiter 0 PCI Gnt n	O	[1:5]			
Hard_Ethernet_MAC_RGMII_T...	Hard Ethernet MAC RGMII TXD 0	O	[3:0]			
Hard_Ethernet_MAC_RGMII_T...	Hard Ethernet MAC RGMII TX CTL	O				
Hard_Ethernet_MAC_RGMII_T...	Hard Ethernet MAC RGMII TXC 0	O				
Hard_Ethernet_MAC_RGMII...	Hard Ethernet MAC RGMII RXD 0	I	[3:0]			
Hard_Ethernet_MAC_RGMII...	Hard Ethernet MAC RGMII RX CTI	I				
Hard_Ethernet_MAC_RGMII...	Hard Ethernet MAC RGMII RXC 0	I				
vga_reset_pin	sys periph reset n	O		RST	0	
xps_tft_0_TFT_HSYNC_pin	xps tft 0 TFT HSYNC	O				
xps_tft_0_TFT_VSYNC_pin	xps tft 0 TFT VSYNC	O				
xps_tft_0_TFT_DE_pin	xps tft 0 TFT DE	O				

System Assembly View



# Connect Interrupts

- Expand **xps\_intc\_0** and click on **Intr**

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

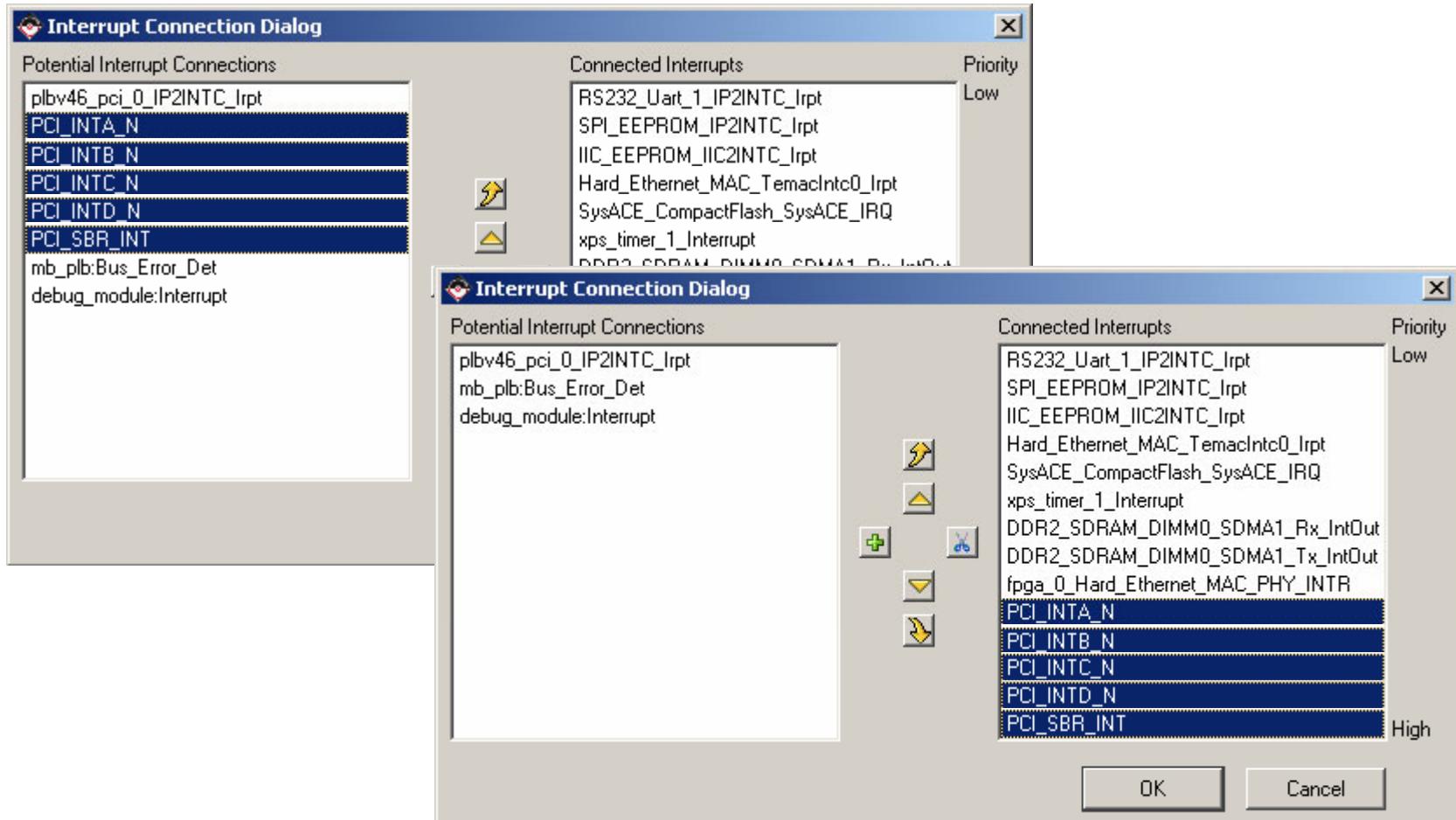
Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
+ proc_sys_reset_0						
+ LCD_OPTIONAL						
+ LEDS_4Bit						
+ IIC_EEPROM						
- xps_intc_0						
- Irq	Interrupt	0		INTERRUPT		EDGE_RISING
- Intr	L to H: RS232_Uart_1_IP2INTC_Irpt & SPI			IIC_NUM_INTR_INPU...	INTERRUPT	EDGE_RISING
+ Hard_Ethernet_MAC						
+ SPI EEPROM						
+ SysACE_CompactFlash						
+ xps_ifi_0						
+ xps_timer_1						
+ RS232_Uart_1						
+ clock_generator_0						
+ pci_arbiter_0						
+ FLASH util bus split_0						

System Assembly View



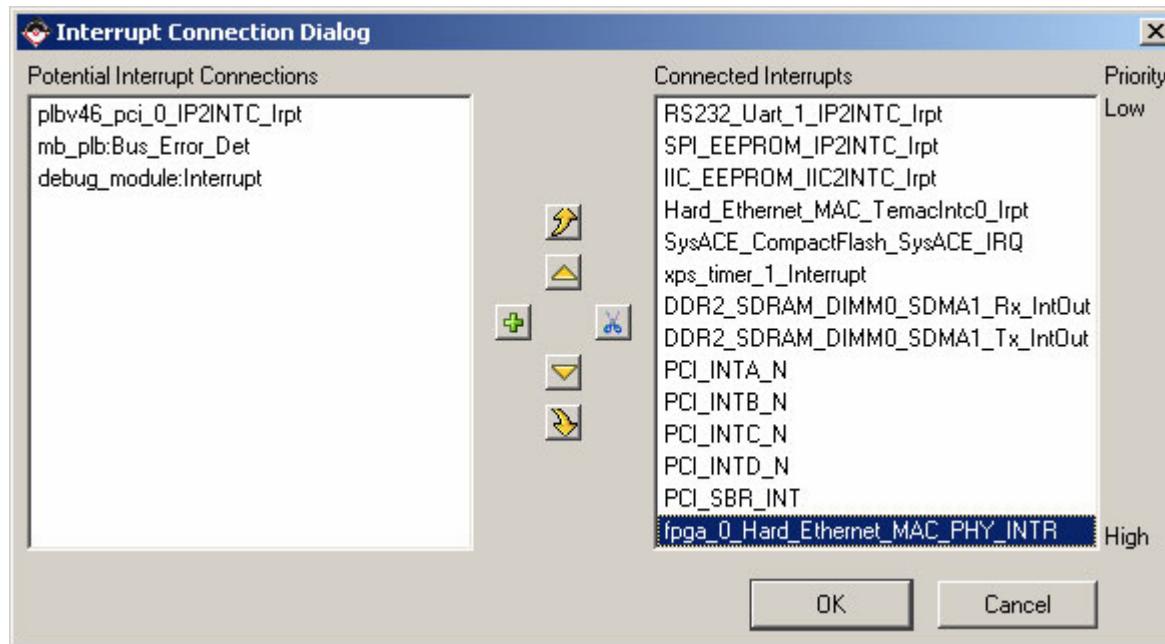
# Connect Interrupts

- Add PCI Interrupts



# Connect Interrupts

- At least one non-PCI interrupt should be highest priority



# Generate Addresses

# Generate Addresses

- Select the Addresses tab
  - Set the C\_IPIFBAR\_0 to a range of 512M
  - Set the C\_IPIFBAR\_1 to a range of 64M

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses  Generate Addresses

Instance	Name	Base Address	High Address	Size	Lock	Bus Interface(s)	Bus Connection
mb_plb	C_BASEADDR			U	<input type="checkbox"/>	Not Applicable	
plbv46_pci_0	C_BASEADDR			U	<input type="checkbox"/>	SPLB	mb_plb
plbv46_pci_0	C_IPIFBAR_0	0x00000000	0x1FFFFFFF	512M	<input type="checkbox"/>	SPLB	mb_plb
plbv46_pci_0	C_IPIFBAR_1	0x00000000	0x03FFFFFF	64M	<input type="checkbox"/>	SPLB	mb_plb
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	ilmb
LEDs_4Bit	C_BASEADDR	0x81400000	0x8140ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
LCD_OPTIONAL	C_BASEADDR	0x81420000	0x8142ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
IIC EEPROM	C_BASEADDR	0x81600000	0x8160ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_intc_0	C_BASEADDR	0x81800000	0x8180ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
Hard_Ethernet_MAC	C_BASEADDR	0x81c00000	0x81c0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
SysACE_CompactFlash	C_BASEADDR	0x83600000	0x8360ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_timer_1	C_BASEADDR	0x83c00000	0x83c0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
RS232_Uart_1	C_BASEADDR	0x83e00000	0x83e0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb

System Assembly View



# Generate Addresses

- Click Generate Addresses and view the new address

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses  Generate Addresses

Instance	Name	Base Address	High Address	Size	Lock	Bus Interface(s)	Bus Connection
mb_plb	C_BASEADDR			U	<input type="checkbox"/>	Not Applicable	
plbv46_pci_0	C_BASEADDR	0x85e00000	0x85e0ffff	64K	<input type="checkbox"/>	SPLB	mb_plb
plbv46_pci_0	C_IPIFBAR_0	0xe0000000	0xffffffff	512M	<input type="checkbox"/>	SPLB	mb_plb
plbv46_pci_0	C_IPIFBAR_1	0xd0000000	0xd3fffff	64M	<input type="checkbox"/>	SPLB	mb_plb
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	ilmb
LEDs_4Bit	C_BASEADDR	0x81400000	0x8140ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
LCD_OPTIONAL	C_BASEADDR	0x81420000	0x8142ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
IIC EEPROM	C_BASEADDR	0x81600000	0x8160ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_intc_0	C_BASEADDR	0x81800000	0x8180ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
Hard_Ethernet_MAC	C_BASEADDR	0x81c00000	0x81c0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
SysACE_CompactFlash	C_BASEADDR	0x83600000	0x8360ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_timer_1	C_BASEADDR	0x83c00000	0x83c0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
RS232_Uart_1	C_BASEADDR	0x83e00000	0x83e0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb

System Assembly View



# Lock Addresses

- Lock these new addresses

Xilinx Platform Studio - C:/ml510\_bsb1\_pcores/ml510\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses  Generate Addresses

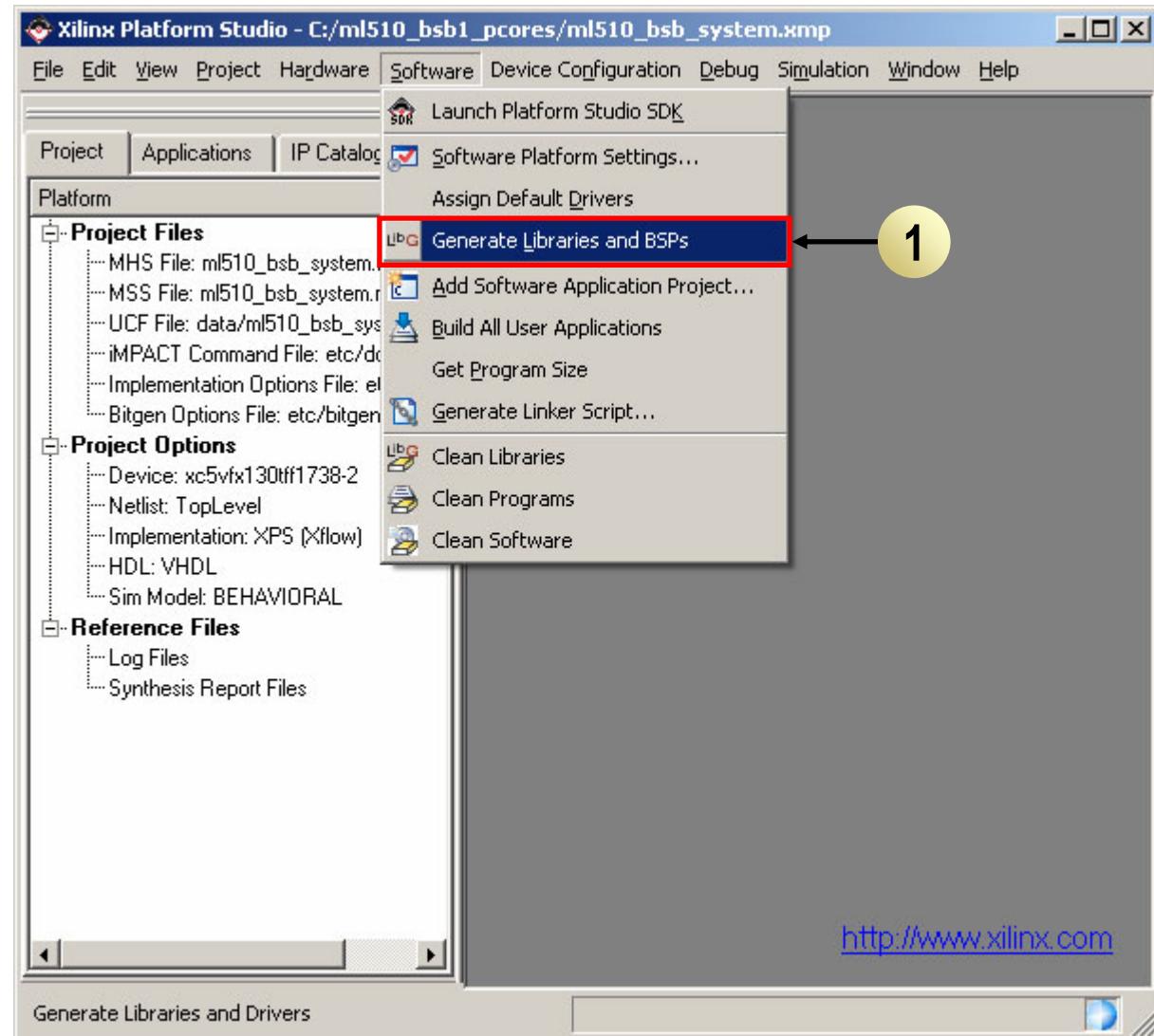
Instance	Name	Base Address	High Address	Size	Lock	Bus Interface(s)	Bus Connection
mb_plb	C_BASEADDR			U	<input checked="" type="checkbox"/>	Not Applicable	
plbv46_pci_0	C_BASEADDR	0x85e00000	0x85e0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
plbv46_pci_0	C_IPIFBAR_0	0xe0000000	0xffffffff	512M	<input checked="" type="checkbox"/>	SPLB	mb_plb
plbv46_pci_0	C_IPIFBAR_1	0xd0000000	0xd3fffff	64M	<input checked="" type="checkbox"/>	SPLB	mb_plb
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	ilmb
LEDs_4Bit	C_BASEADDR	0x81400000	0x8140ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
LCD_OPTIONAL	C_BASEADDR	0x81420000	0x8142ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
IIC EEPROM	C_BASEADDR	0x81600000	0x8160ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_intc_0	C_BASEADDR	0x81800000	0x8180ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
Hard_Ethernet_MAC	C_BASEADDR	0x81c00000	0x81c0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
SysACE_CompactFlash	C_BASEADDR	0x83600000	0x8360ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_timer_1	C_BASEADDR	0x83c00000	0x83c0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
RS232_Uart_1	C_BASEADDR	0x83e00000	0x83e0ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb



# Compile Design

# Generate Bitstream

- Generate the libraries needed to create the bitstream
  - Select **Software → Generate Libraries and BSPs (1)**

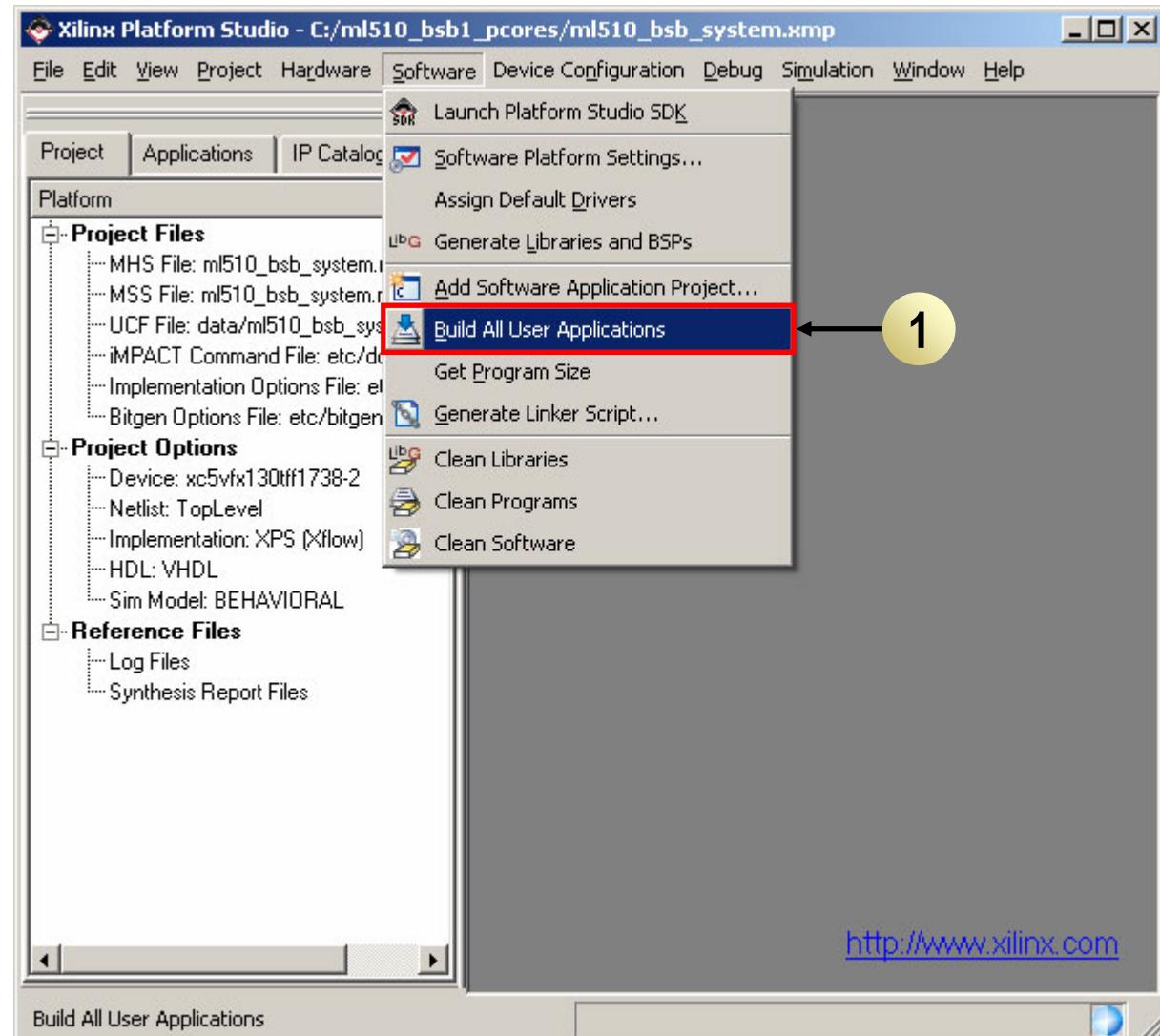


<http://www.xilinx.com>

 **XILINX**

# Generate Bitstream

- Compile the TestApp project and create an executable (executable.elf)
  - Select **Software** → **Build All User Applications** (1)

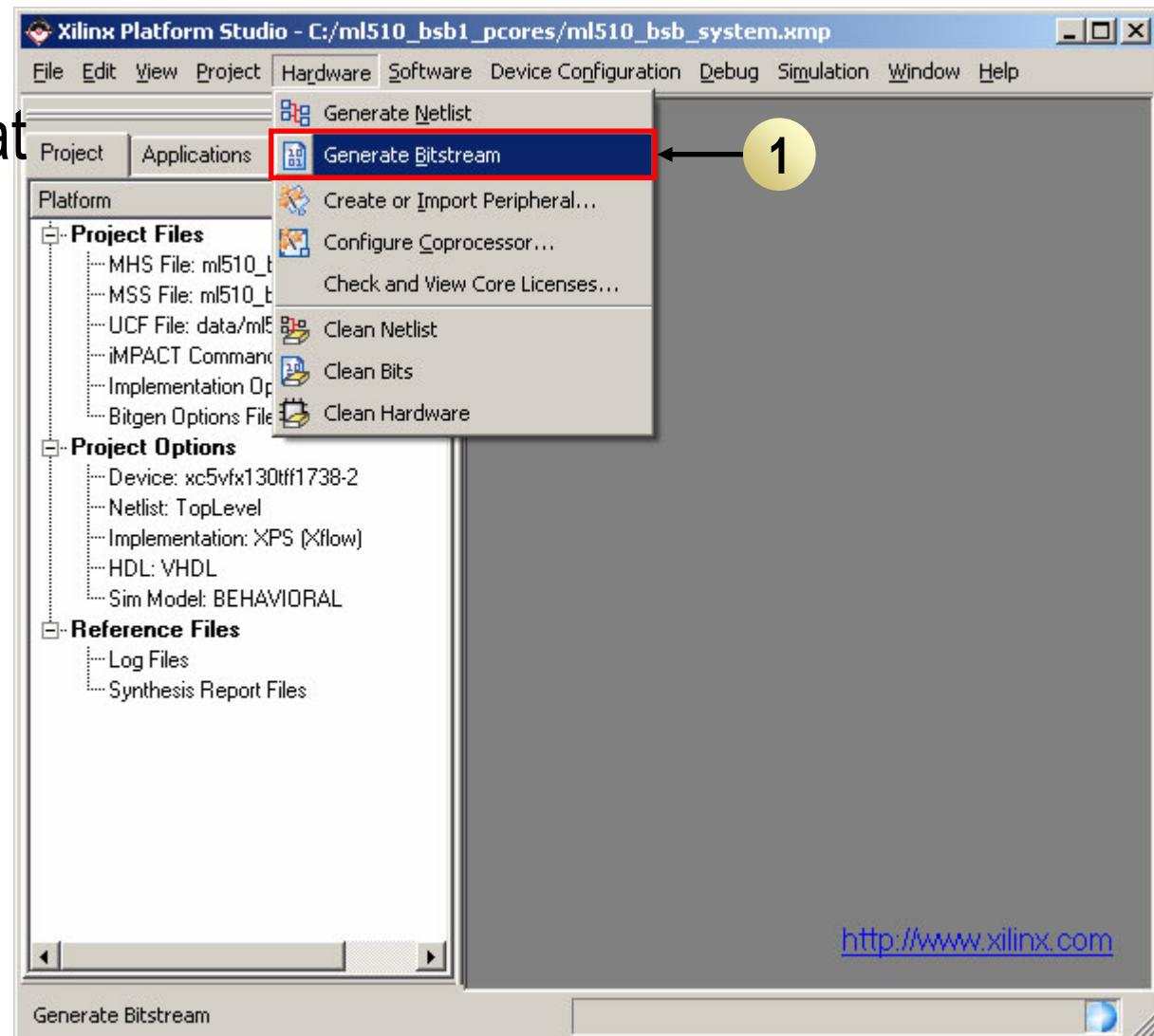


<http://www.xilinx.com>

 **XILINX**

# Generate Bitstream

- Create the hardware design (system.bit) that is located in <project directory>/implementation
  - Select **Hardware** → **Generate Bitstream (1)**  
**(Takes roughly 90 minutes)**



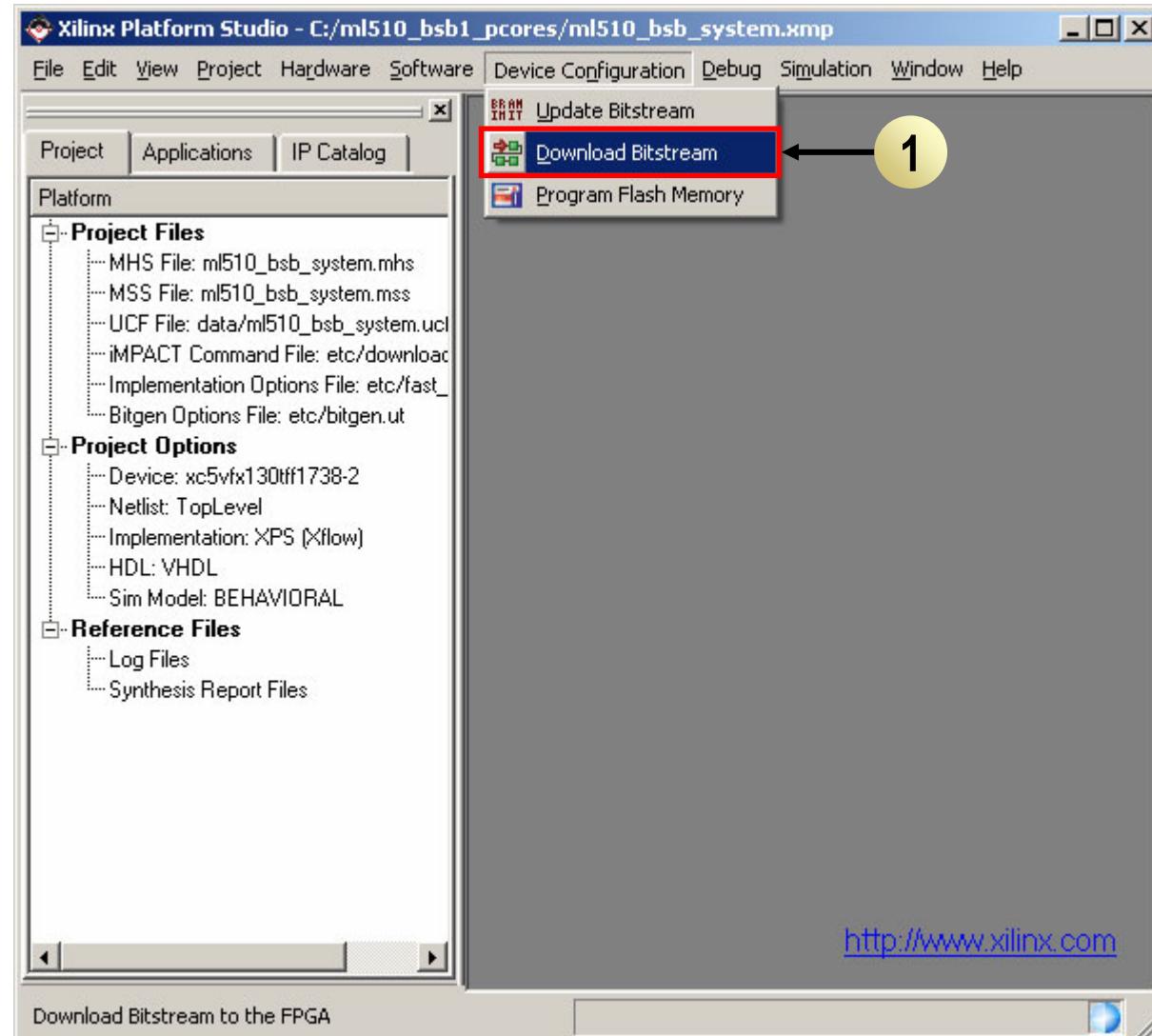
# Loading Bootloop into BRAM

- A concatenated software/hardware file, known as an ACE file, is useful for loading large programs, such as a Linux, VxWorks, or U-Boot into the external memory
- A bootloop program must be used to occupy the processor until the software is loaded into memory
- The following pages show how to initialize a bootloop program into block RAM and to test its existence



# Loading Bootloop into BRAM

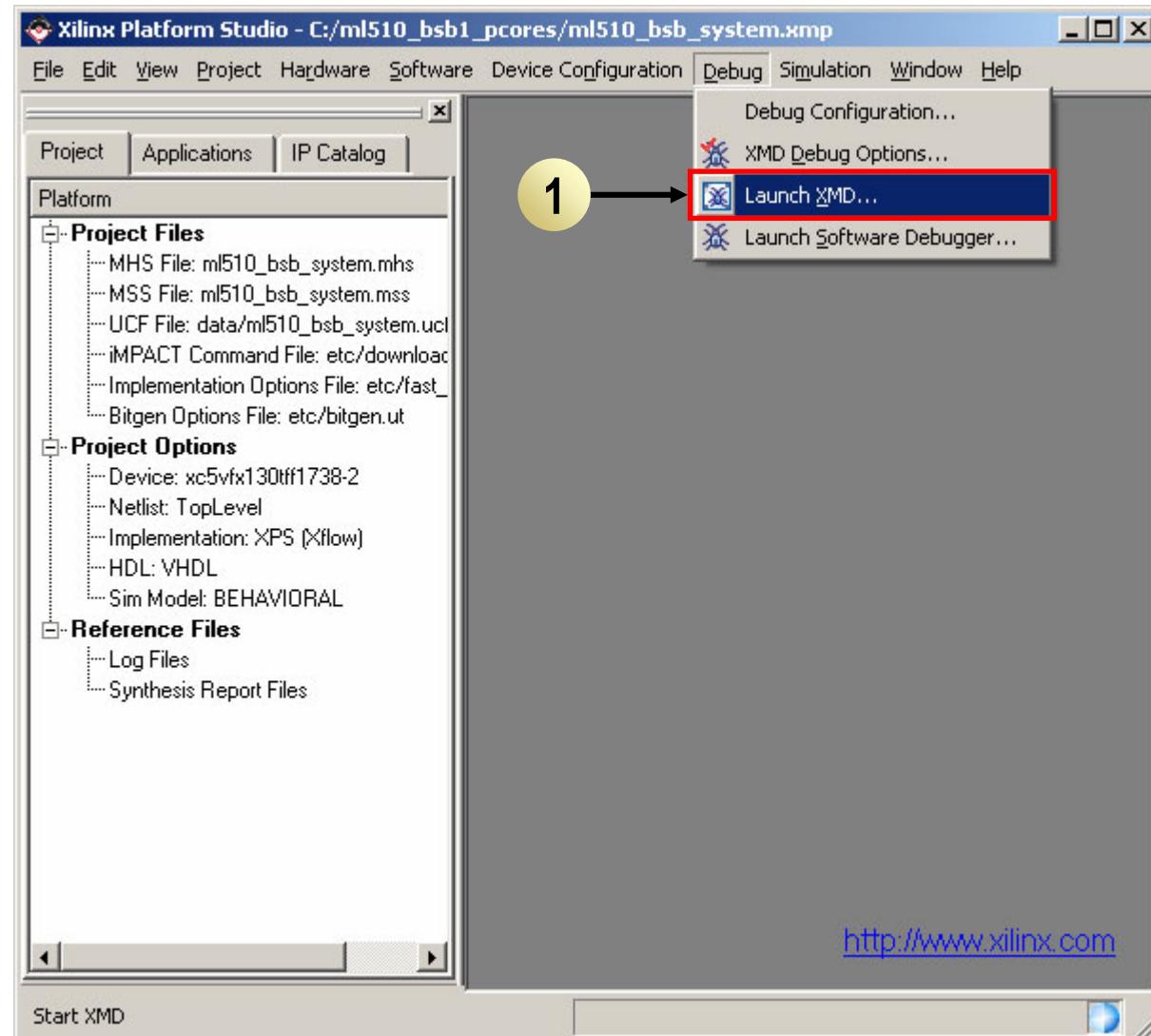
- Download the bitstream:
  - Select Device Configuration → Download Bitstream (1)



 XILINX®

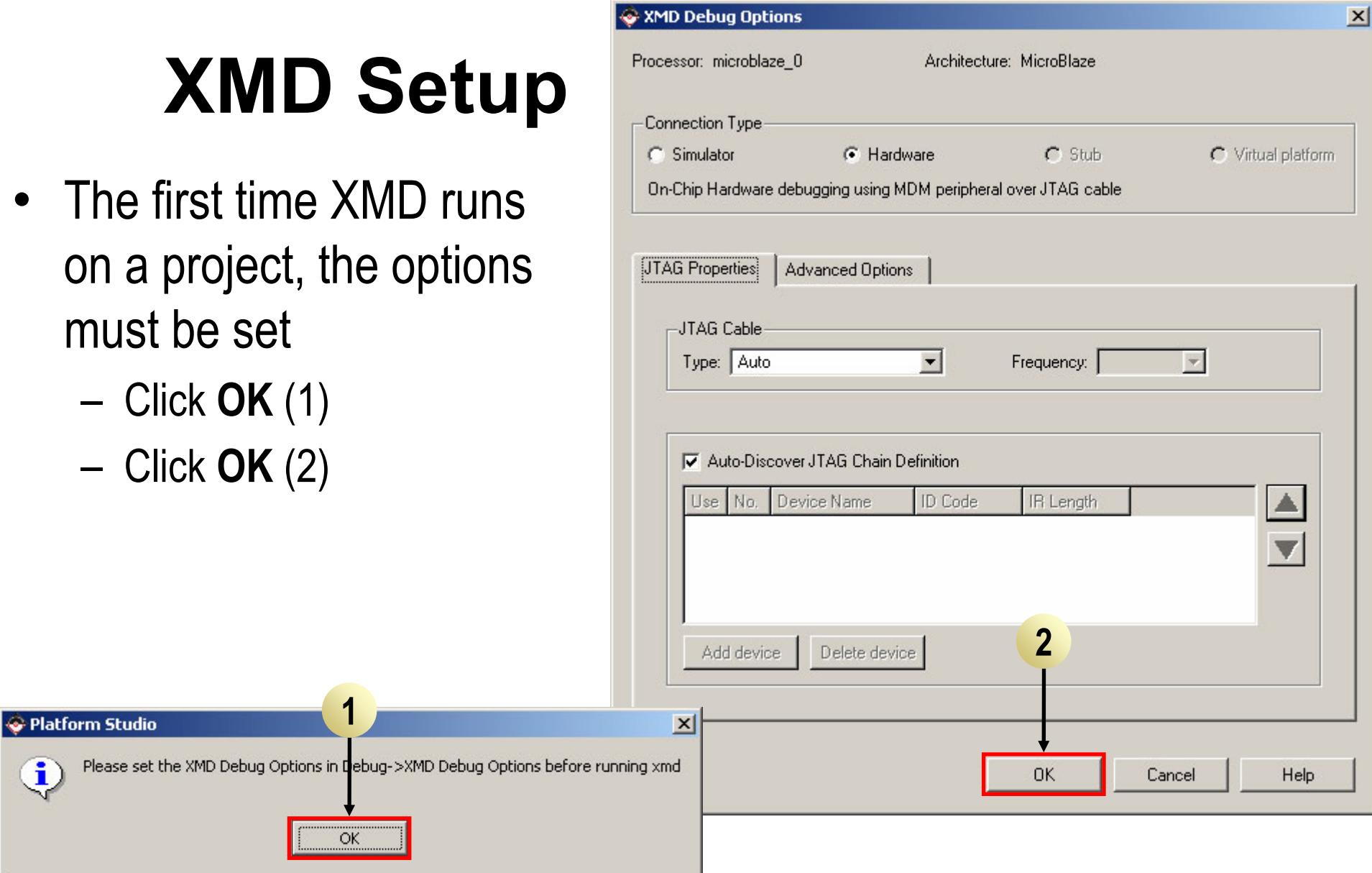
# Loading Bootloop into BRAM

- A memory read can be executed to test if the bootloop was successfully loaded
  - Select Debug → Launch XMD (1)



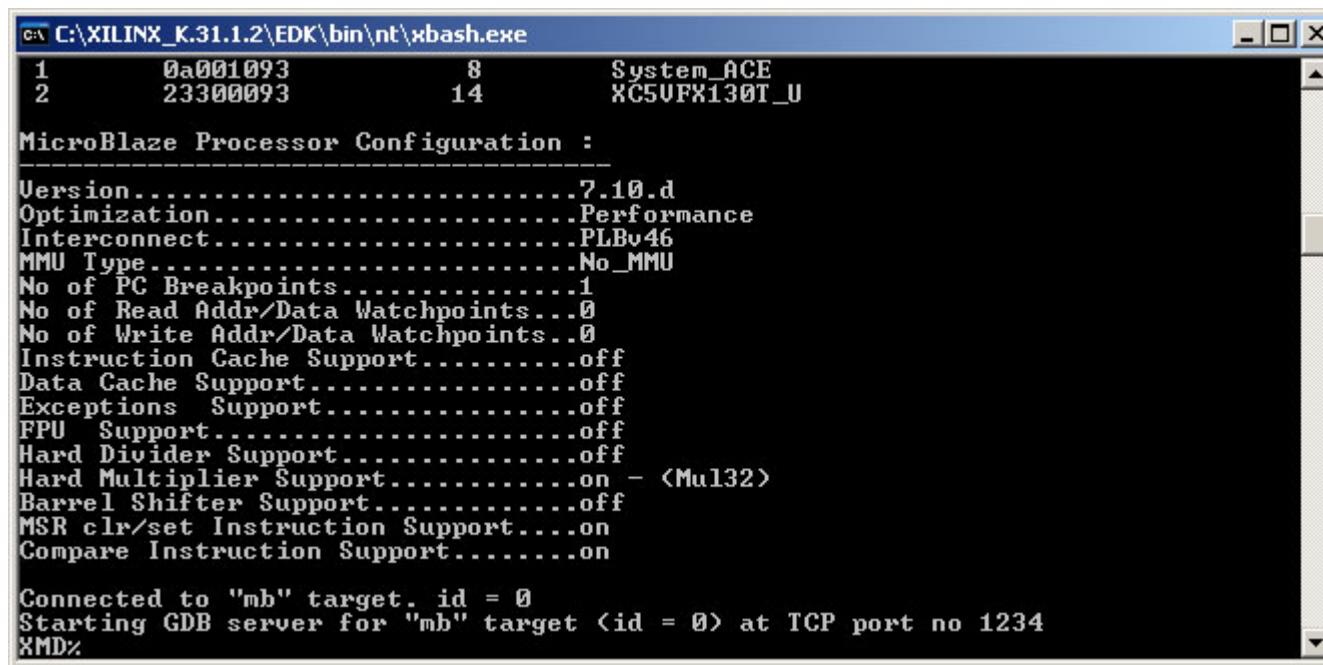
# XMD Setup

- The first time XMD runs on a project, the options must be set
  - Click **OK** (1)
  - Click **OK** (2)



# Loading Bootloop into BRAM

- XMD opens and connects to the processor, using the default options



```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
1      0a001093          8      System_ACE
2      23300093          14     XC5UFX130T_U

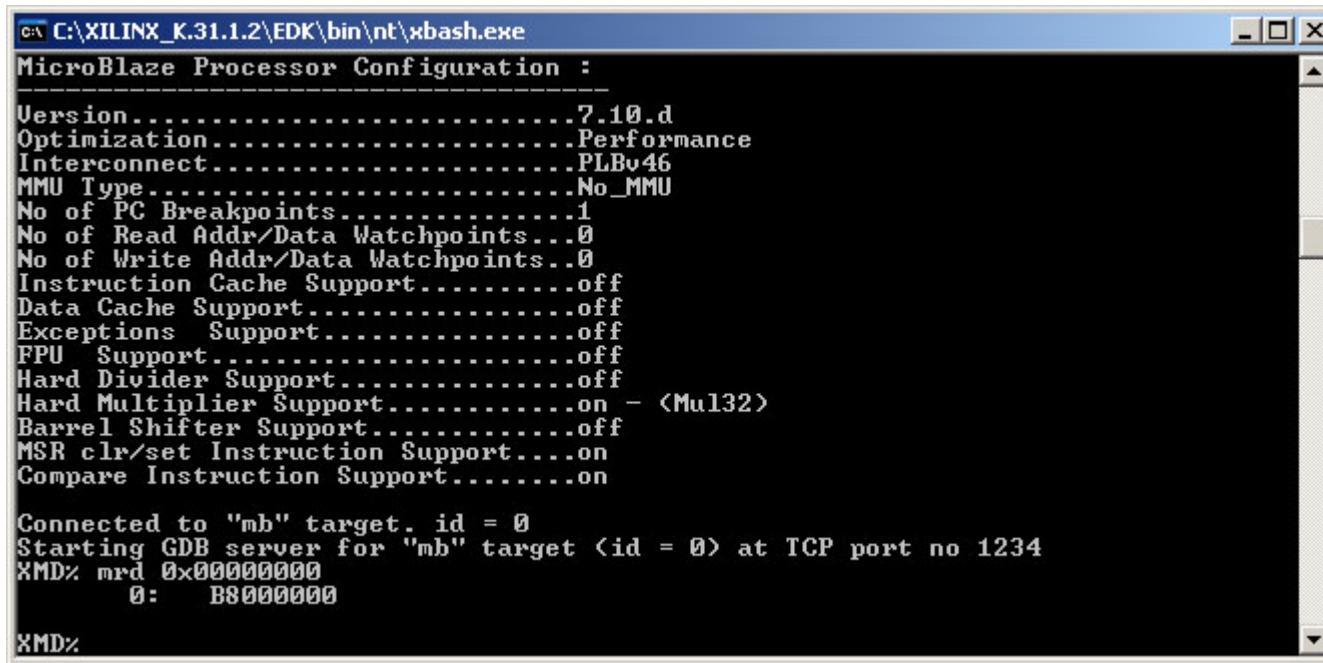
MicroBlaze Processor Configuration :
-----
Version..... 7.10.d
Optimization... Performance
Interconnect... PLBu46
MMU Type..... No_MMU
No of PC Breakpoints.... 1
No of Read Addr/Data Watchpoints.. 0
No of Write Addr/Data Watchpoints.. 0
Instruction Cache Support..... off
Data Cache Support..... off
Exceptions Support..... off
FPU Support..... off
Hard Divider Support..... off
Hard Multiplier Support..... on - <Mul32>
Barrel Shifter Support..... off
MSR clr/set Instruction Support... on
Compare Instruction Support..... on

Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD%
```



# Loading Bootloop into BRAM

- To execute a memory read, type **mrd 0x00000000**
- This will read the memory address at the reset vector; the value should be **0xB8000000** as shown below



```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
MicroBlaze Processor Configuration :
Version..... 7.10.d
Optimization..... Performance
Interconnect..... PLBv46
MMU Type..... No_MMU
No of PC Breakpoints..... 1
No of Read Addr/Data Watchpoints .. 0
No of Write Addr/Data Watchpoints.. 0
Instruction Cache Support..... off
Data Cache Support..... off
Exceptions Support..... off
FPU Support..... off
Hard Divider Support..... off
Hard Multiplier Support..... on - <Mul32>
Barrel Shifter Support..... off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on

Connected to "mb" target. id = 0
Starting GDB server for "mb" target <id = 0> at TCP port no 1234
XMD% mrd 0x00000000
0: B8000000

XMD%
```



# Download ELF File

- Download and run the hello\_pci ELF file from XMD  
dow microblaze\_0/code/hello\_pci.elf (1)  
con (2)

The screenshot shows a terminal window titled "C:\XILINX\_K.31.1.2\EDK\bin\nt\xbash.exe". The window contains the following text:

```
XMD% dow microblaze_0/code/hello_pci.elf
System Reset .... DONE
Downloading Program -- microblaze_0/code/hello_pci.elf
  section, .vectors.reset: 0x00000000-0x00000003
  section, .vectors.sw_exception: 0x00000008-0x0000000b
  section, .vectors.interrupt: 0x00000010-0x00000013
  section, .vectors.hw_exception: 0x00000020-0x00000023
  section, .text: 0x00000050-0x00001a47
  section, .init: 0x00001a48-0x00001a6b
  section, .fini: 0x00001a6c-0x00001a87
  section, .ctors: 0x00001a88-0x00001a8f
  section, .dtors: 0x00001a90-0x00001a97
  section, .rodata: 0x00001a98-0x000021fd
  section, .data: 0x00002200-0x00002313
  section, .eh_frame: 0x00002314-0x00002317
  section, .jcr: 0x00002318-0x0000231b
  section, .bss: 0x00002320-0x00002343
  section, .stack: 0x00002344-0x00002747
Setting PC with Program Start Address 0x00000000

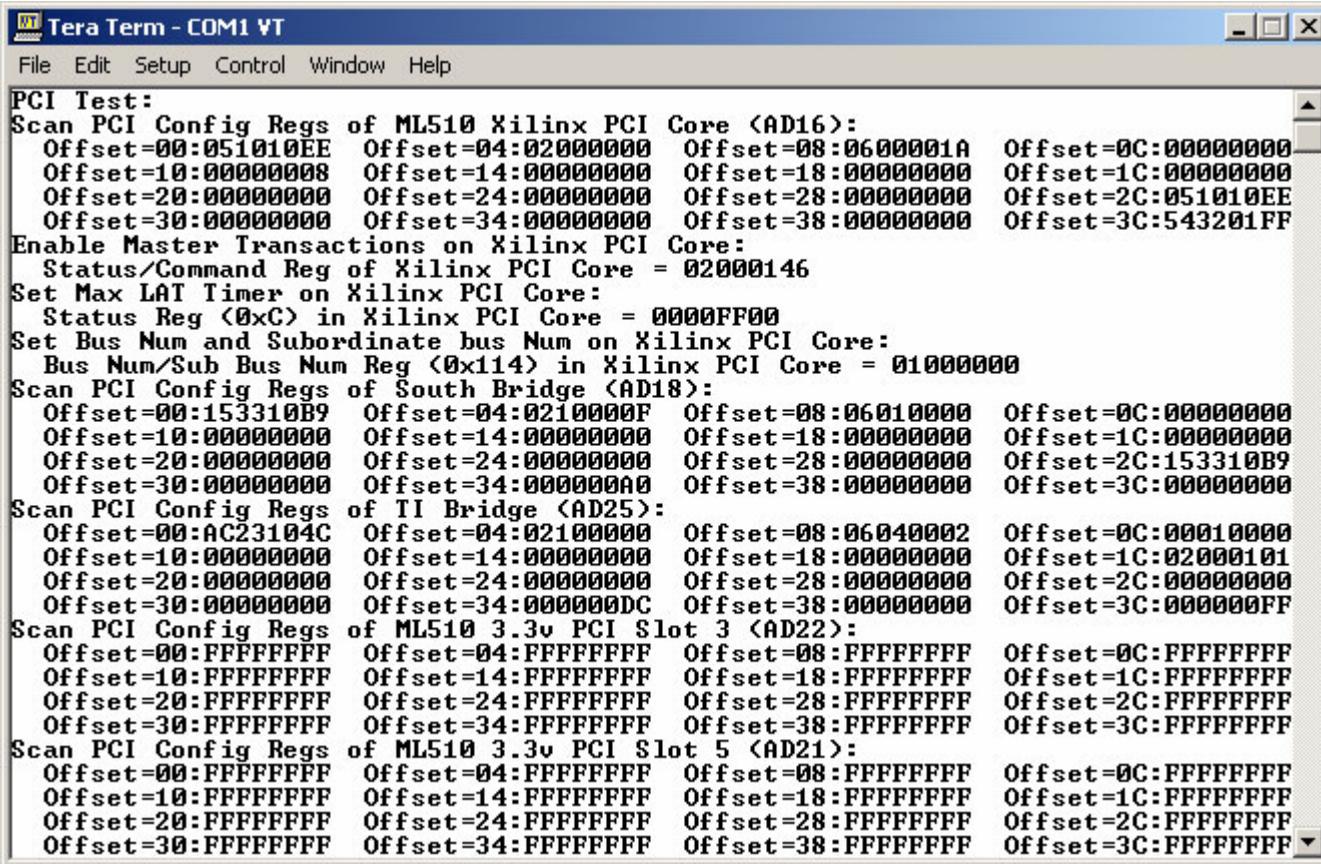
XMD% con
Info: Processor started. Type "stop" to stop processor
RUNNING> XMD%
```

Two numbered callouts point to specific lines in the terminal output:

- Callout 1 points to the command "XMD% dow microblaze\_0/code/hello\_pci.elf".
- Callout 2 points to the command "XMD% con".

# Run hello\_pci

- View the output in the terminal program



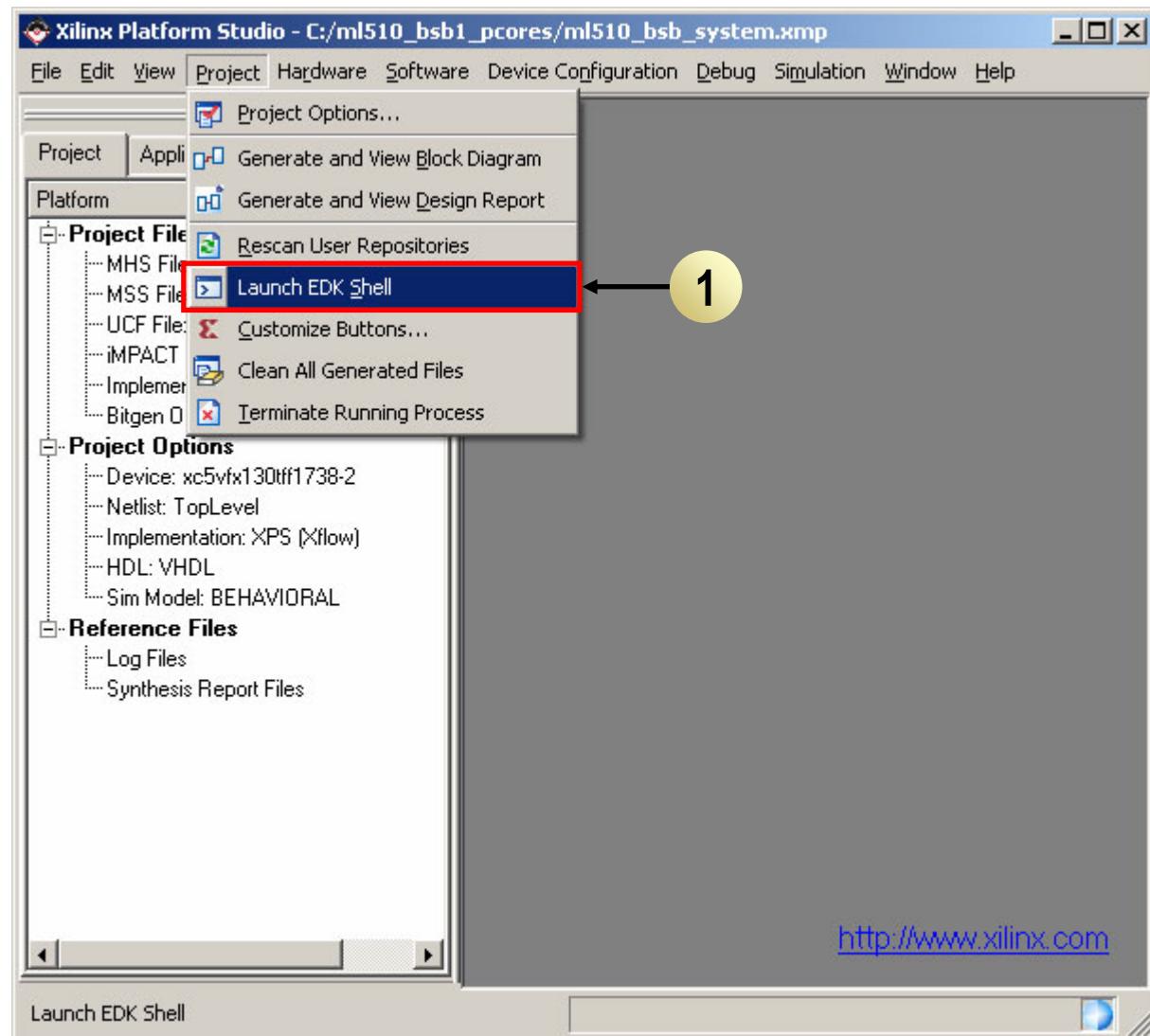
The screenshot shows a terminal window titled "Tera Term - COM1 VT". The window displays the output of a "PCI Test" script. The output includes several sections of configuration and status information for various PCI components on an ML510 board.

```
PCI Test:  
Scan PCI Config Regs of ML510 Xilinx PCI Core <AD16>:  
  Offset=00:051010EE  Offset=04:02000000  Offset=08:0600001A  Offset=0C:00000000  
  Offset=10:00000008  Offset=14:00000000  Offset=18:00000000  Offset=1C:00000000  
  Offset=20:00000000  Offset=24:00000000  Offset=28:00000000  Offset=2C:051010EE  
  Offset=30:00000000  Offset=34:00000000  Offset=38:00000000  Offset=3C:543201FF  
Enable Master Transactions on Xilinx PCI Core:  
  Status/Command Reg of Xilinx PCI Core = 02000146  
Set Max LAT Timer on Xilinx PCI Core:  
  Status Reg <0xC> in Xilinx PCI Core = 0000FF00  
Set Bus Num and Subordinate bus Num on Xilinx PCI Core:  
  Bus Num/Sub Bus Num Reg <0x114> in Xilinx PCI Core = 01000000  
Scan PCI Config Regs of South Bridge <AD18>:  
  Offset=00:153310B9  Offset=04:0210000F  Offset=08:06010000  Offset=0C:00000000  
  Offset=10:00000000  Offset=14:00000000  Offset=18:00000000  Offset=1C:00000000  
  Offset=20:00000000  Offset=24:00000000  Offset=28:00000000  Offset=2C:153310B9  
  Offset=30:00000000  Offset=34:000000A0  Offset=38:00000000  Offset=3C:00000000  
Scan PCI Config Regs of TI Bridge <AD25>:  
  Offset=00:AC23104C  Offset=04:02100000  Offset=08:06040002  Offset=0C:00010000  
  Offset=10:00000000  Offset=14:00000000  Offset=18:00000000  Offset=1C:02000101  
  Offset=20:00000000  Offset=24:00000000  Offset=28:00000000  Offset=2C:00000000  
  Offset=30:00000000  Offset=34:000000DC  Offset=38:00000000  Offset=3C:000000FF  
Scan PCI Config Regs of ML510 3.3v PCI Slot 3 <AD22>:  
  Offset=00:FFFFFFFF  Offset=04:FFFFFFFF  Offset=08:FFFFFFFF  Offset=0C:FFFFFFFF  
  Offset=10:FFFFFFFF  Offset=14:FFFFFFFF  Offset=18:FFFFFFFF  Offset=1C:FFFFFFFF  
  Offset=20:FFFFFFFF  Offset=24:FFFFFFFF  Offset=28:FFFFFFFF  Offset=2C:FFFFFFFF  
  Offset=30:FFFFFFFF  Offset=34:FFFFFFFF  Offset=38:FFFFFFFF  Offset=3C:FFFFFFFF  
Scan PCI Config Regs of ML510 3.3v PCI Slot 5 <AD21>:  
  Offset=00:FFFFFFF  Offset=04:FFFFFFF  Offset=08:FFFFFFF  Offset=0C:FFFFFFF  
  Offset=10:FFFFFFF  Offset=14:FFFFFFF  Offset=18:FFFFFFF  Offset=1C:FFFFFFF  
  Offset=20:FFFFFFF  Offset=24:FFFFFFF  Offset=28:FFFFFFF  Offset=2C:FFFFFFF  
  Offset=30:FFFFFFF  Offset=34:FFFFFFF  Offset=38:FFFFFFF  Offset=3C:FFFFFFF
```



# Create an ACE File

- Open an EDK shell
  - Select Project → Launch EDK Shell (1)
  - This shell is used for entering and executing the commands to create a concatenated (HW+SW ) ACE file



# Create an ACE File

- At the bash prompt, type (1):

```
cd ace
```

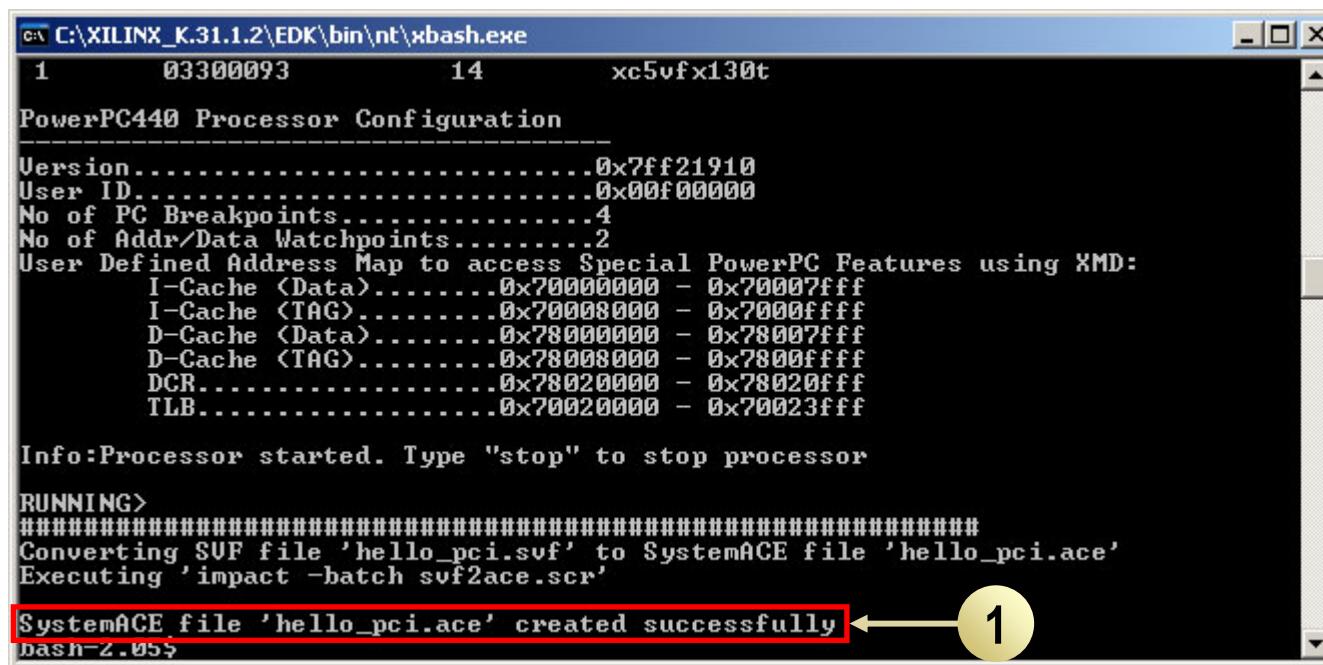
```
./genace_hello_pci.sh
```



A screenshot of a terminal window titled "bash-2.05\$". The window shows the command "cd ace" followed by "bash-2.05\$ ./genace\_hello\_pci.sh". A red rectangular box highlights the command "cd ace" and "bash-2.05\$ ./genace\_hello\_pci.sh". A yellow circle with the number "1" is positioned to the right of the red box, with a thin black arrow pointing from the circle to the red box.

# Create an ACE File

- This creates a concatenated (HW+SW) ACE file
  - Input: hello\_pci ELF file, download.bit bitstream
- The genace\_hello\_pci.sh uses XMD and a genace.tcl script with ML510 appropriate options to generate an ACE file (1)



The screenshot shows a terminal window titled 'C:\XILINX\_K.31.1.2\EDK\bin\nt\xbash.exe'. The window displays the output of a script that configures a PowerPC440 processor and converts an SVF file into a SystemACE file.

```
c:\ XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
1      03300093      14      xc5vfx130t

PowerPC440 Processor Configuration

Version..... 0x7ff21910
User ID..... 0x00f00000
No of PC Breakpoints..... 4
No of Addr/Data Watchpoints..... 2
User Defined Address Map to access Special PowerPC Features using XMD:
  I-Cache <Data>..... 0x70000000 - 0x70007fff
  I-Cache <TAG>..... 0x70008000 - 0x7000ffff
  D-Cache <Data>..... 0x78000000 - 0x78007fff
  D-Cache <TAG>..... 0x78008000 - 0x7800ffff
  DCR..... 0x78020000 - 0x78020fff
  TLB..... 0x70020000 - 0x70023fff

Info:Processor started. Type "stop" to stop processor

RUNNING>
#####
# Converting SVF file 'hello_pci.svf' to SystemACE file 'hello_pci.ace'
# Executing 'impact -batch svf2ace.scr'
#
SystemACE file 'hello_pci.ace' created successfully
bash-2.05$
```

A yellow circle with the number '1' is drawn around the line 'SystemACE file 'hello\_pci.ace' created successfully'.

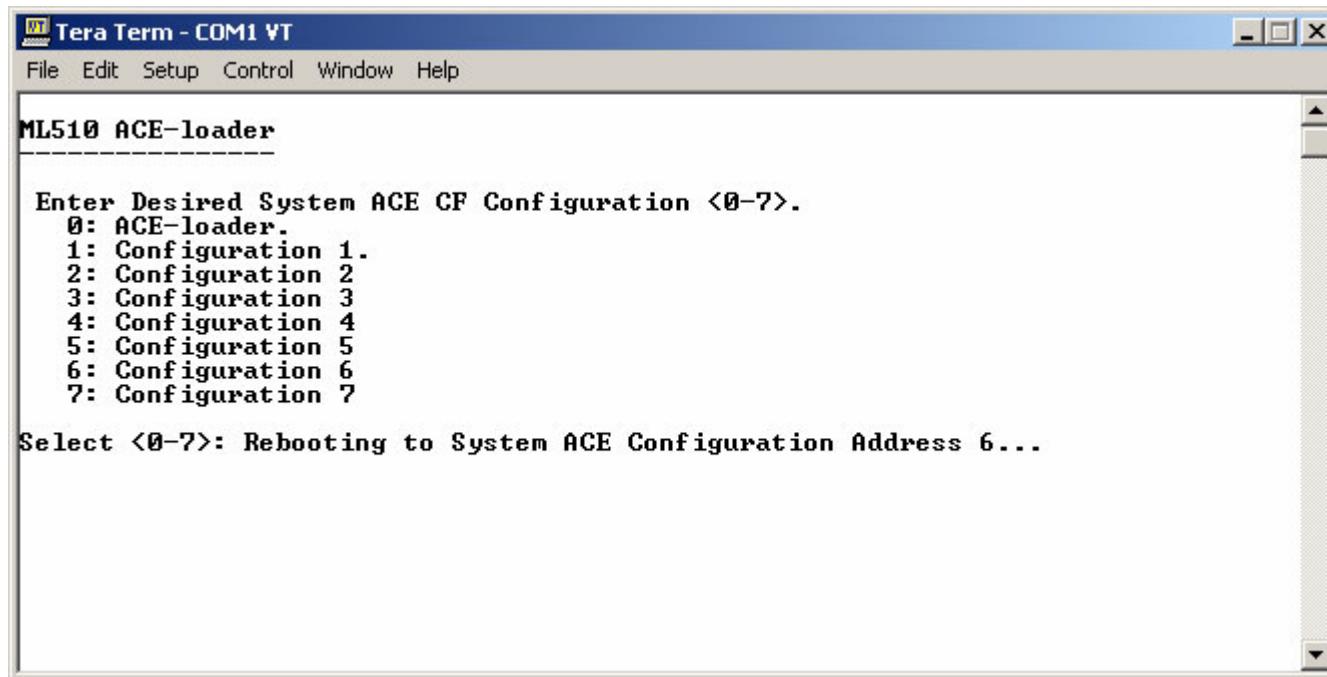
# Run ACE File

- Copy **hello\_pci.ace** to the XILINX\CF6 directory on your CompactFlash card
  - **Important:** Delete any existing ace files in this CF6 directory
  - **Note:** Use a CompactFlash reader to mount the CompactFlash as a disk drive



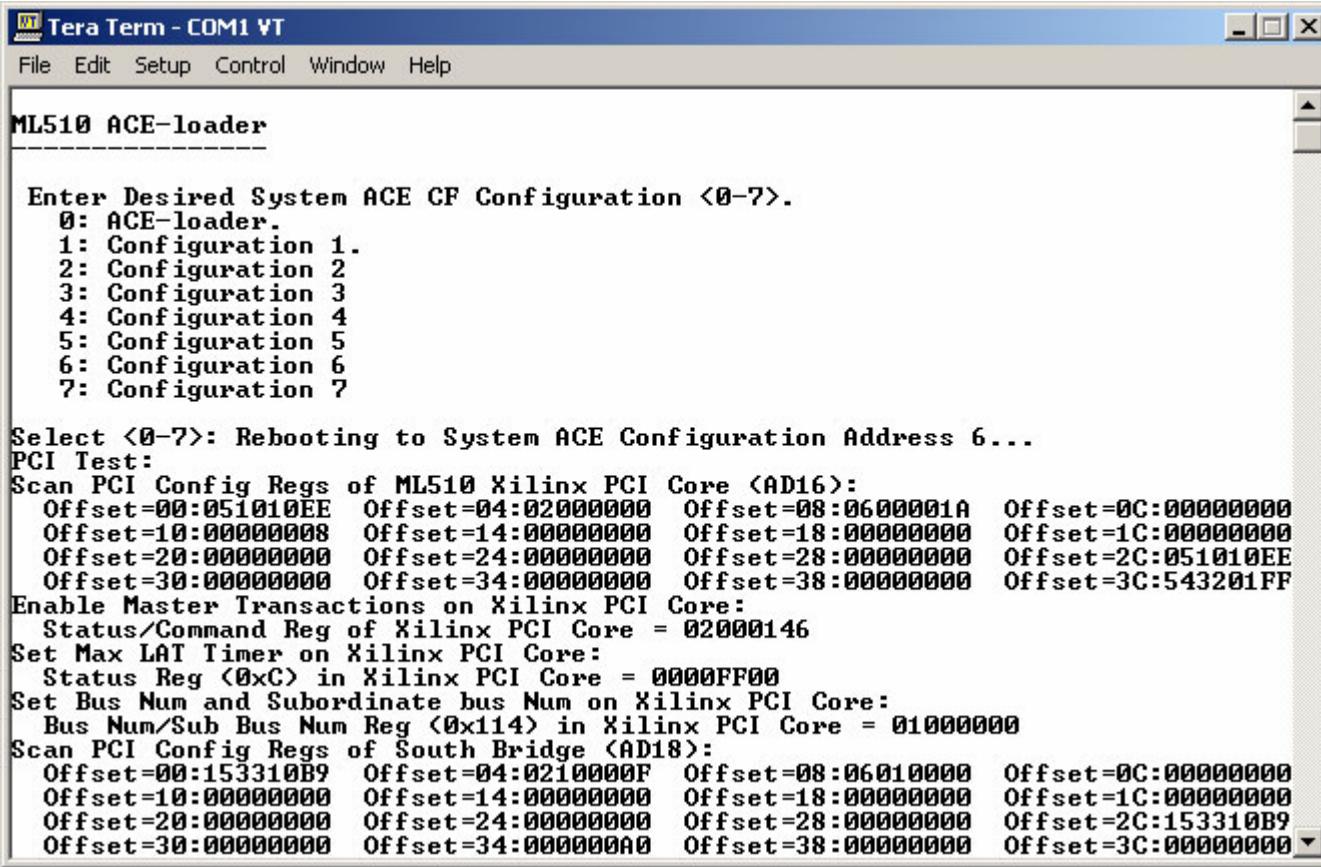
# Run ACE File

- Eject the CompactFlash from your PC and insert it back into the ML510
- Type **6** to run the newly created ACE file



# Run hello\_pci

- View the output in the terminal program



The screenshot shows a terminal window titled "Tera Term - COM1 VT". The window displays the output of the "hello\_pci" program. The output includes a configuration menu for the ML510 ACE-loader, a PCI test section listing memory mapped registers, and sections for enabling master transactions and setting bus numbers.

```
ML510 ACE-loader
Enter Desired System ACE CF Configuration <0-7>.
 0: ACE-loader.
 1: Configuration 1.
 2: Configuration 2
 3: Configuration 3
 4: Configuration 4
 5: Configuration 5
 6: Configuration 6
 7: Configuration 7

Select <0-7>: Rebooting to System ACE Configuration Address 6...
PCI Test:
Scan PCI Config Regs of ML510 Xilinx PCI Core <AD16>:
Offset=00:051010EE  Offset=04:02000000  Offset=08:0600001A  Offset=0C:00000000
Offset=10:00000008  Offset=14:00000000  Offset=18:00000000  Offset=1C:00000000
Offset=20:00000000  Offset=24:00000000  Offset=28:00000000  Offset=2C:051010EE
Offset=30:00000000  Offset=34:00000000  Offset=38:00000000  Offset=3C:543201FF
Enable Master Transactions on Xilinx PCI Core:
Status/Command Reg of Xilinx PCI Core = 02000146
Set Max LAT Timer on Xilinx PCI Core:
Status Reg <0xC> in Xilinx PCI Core = 0000FF00
Set Bus Num and Subordinate bus Num on Xilinx PCI Core:
Bus Num/Sub Bus Num Reg <0x114> in Xilinx PCI Core = 01000000
Scan PCI Config Regs of South Bridge <AD18>:
Offset=00:153310B9  Offset=04:0210000F  Offset=08:06010000  Offset=0C:00000000
Offset=10:00000000  Offset=14:00000000  Offset=18:00000000  Offset=1C:00000000
Offset=20:00000000  Offset=24:00000000  Offset=28:00000000  Offset=2C:153310B9
Offset=30:00000000  Offset=34:000000A0  Offset=38:00000000  Offset=3C:00000000
```

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