
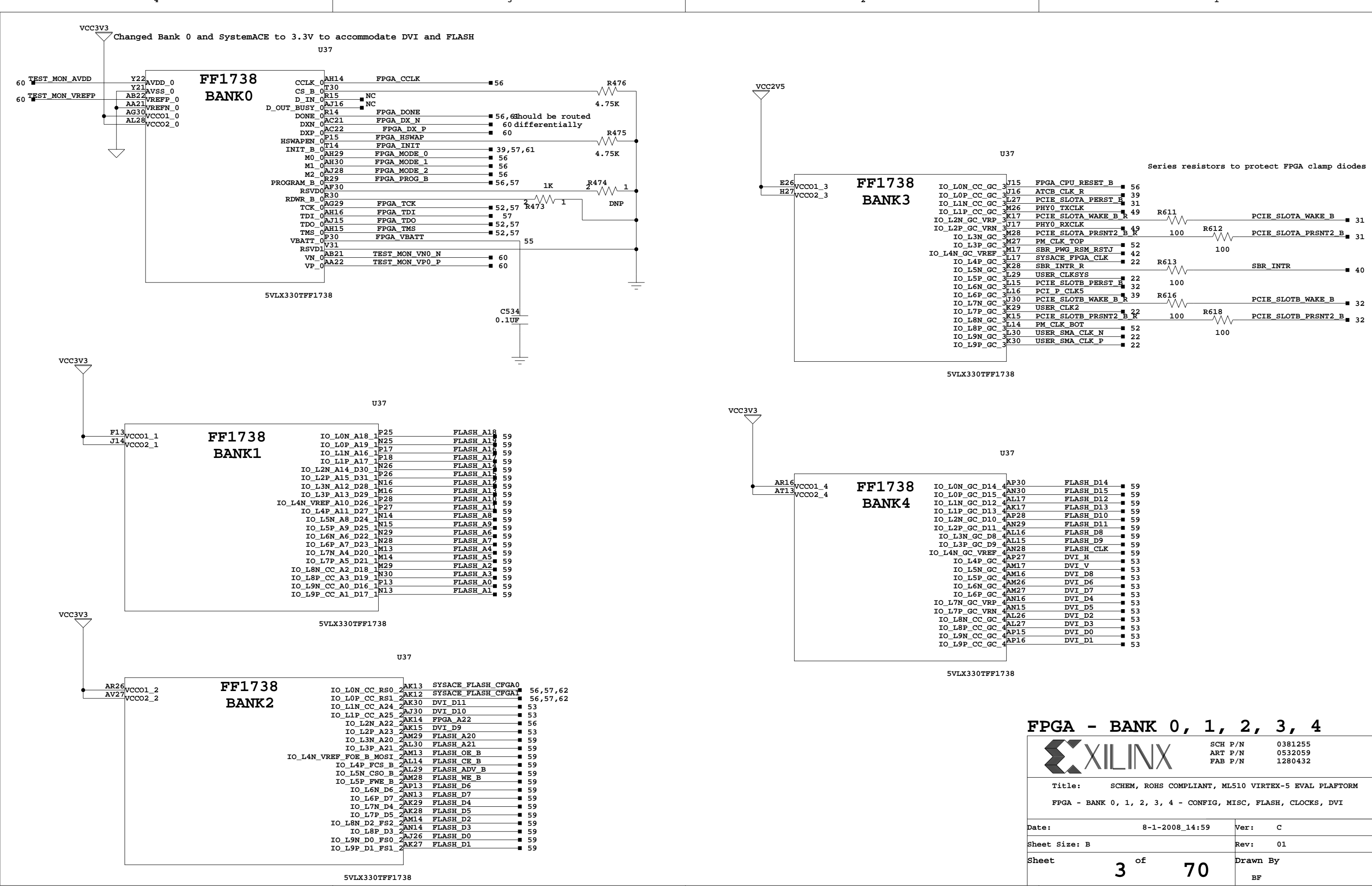


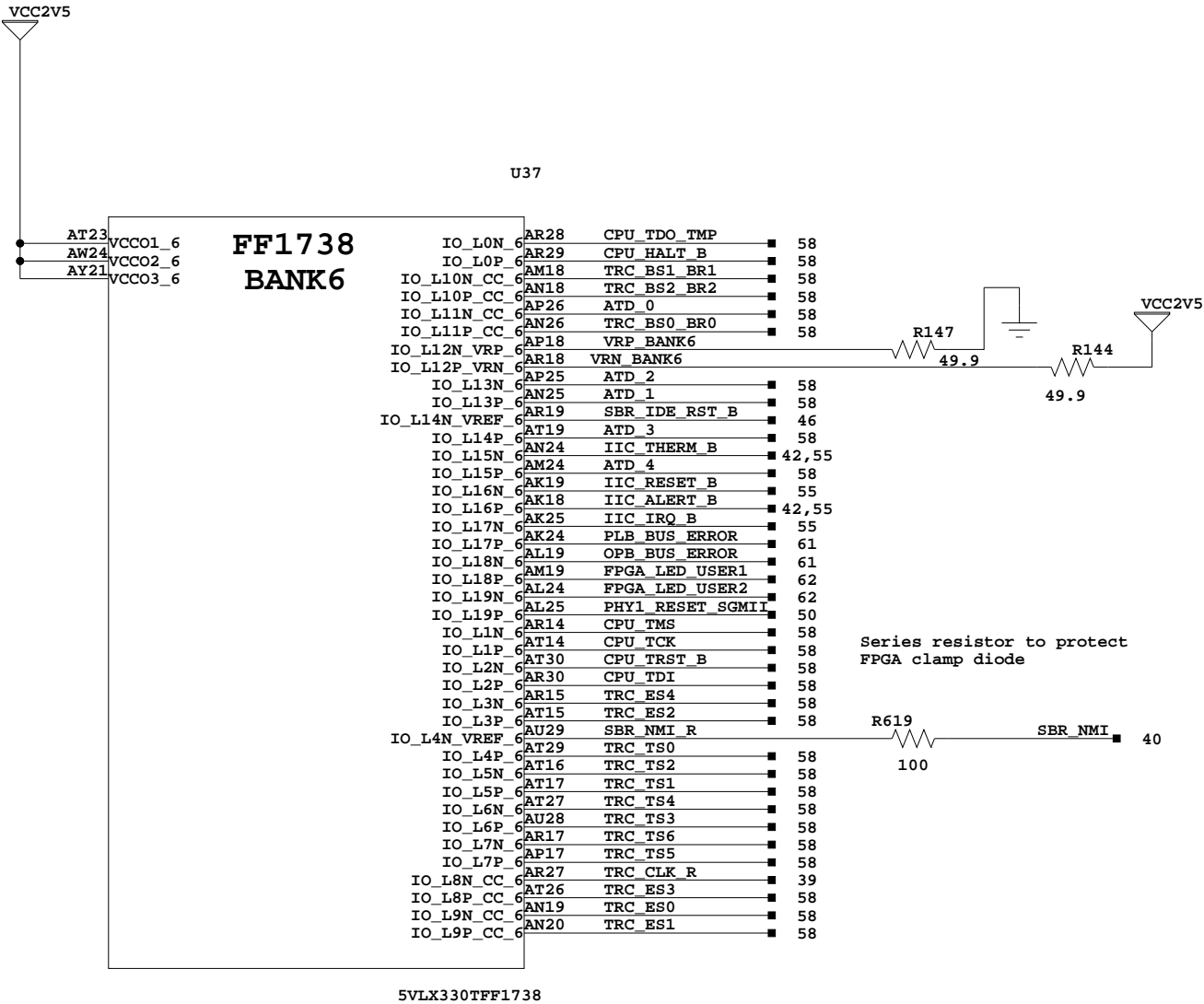
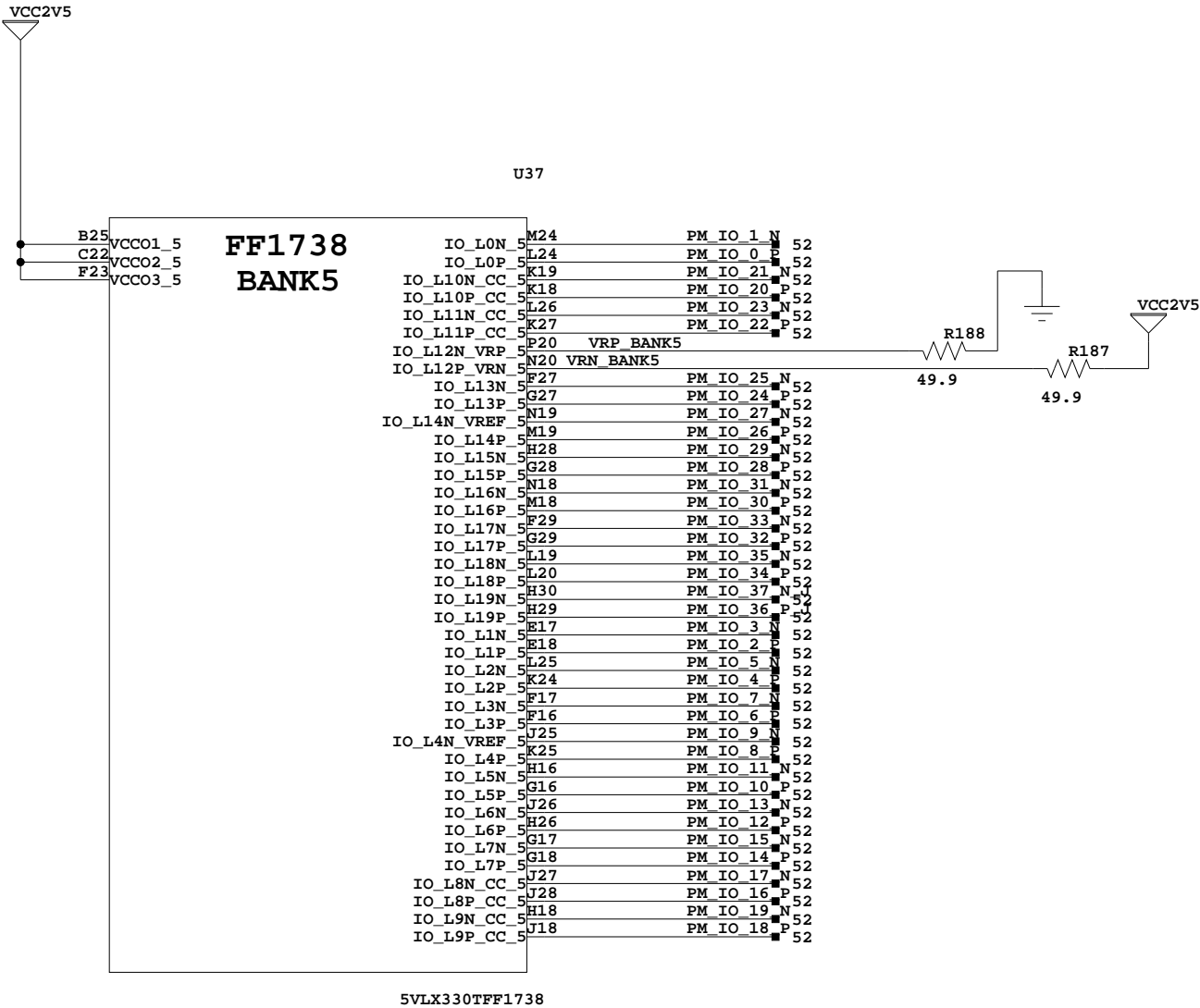
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5	FPGA - BANK 11,12
6	FPGA - BANK 13,15
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67	FPGA CORE AND IO VOLTAGE
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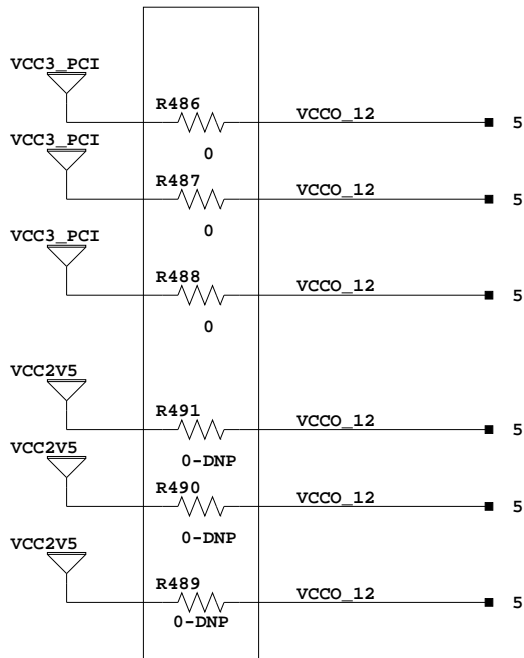
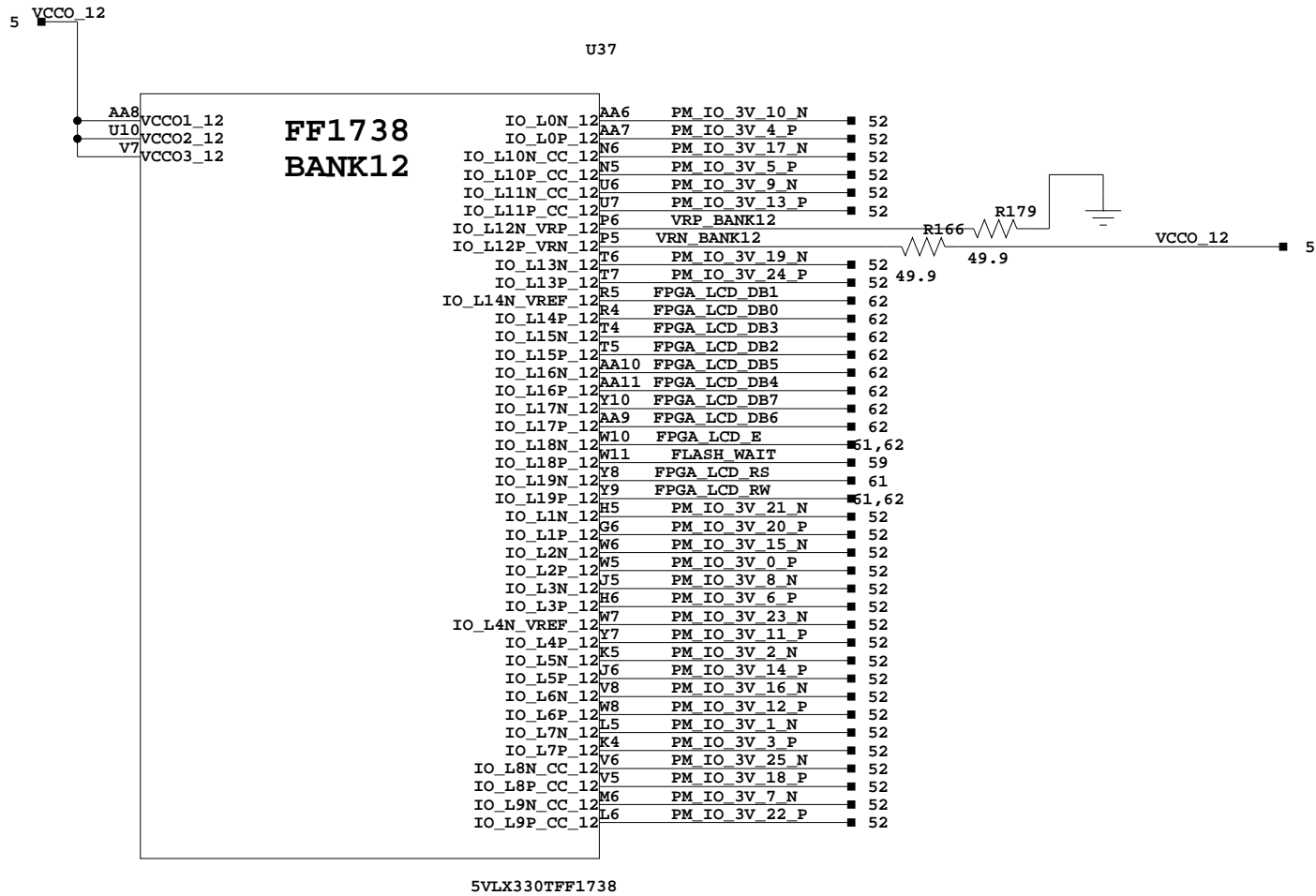
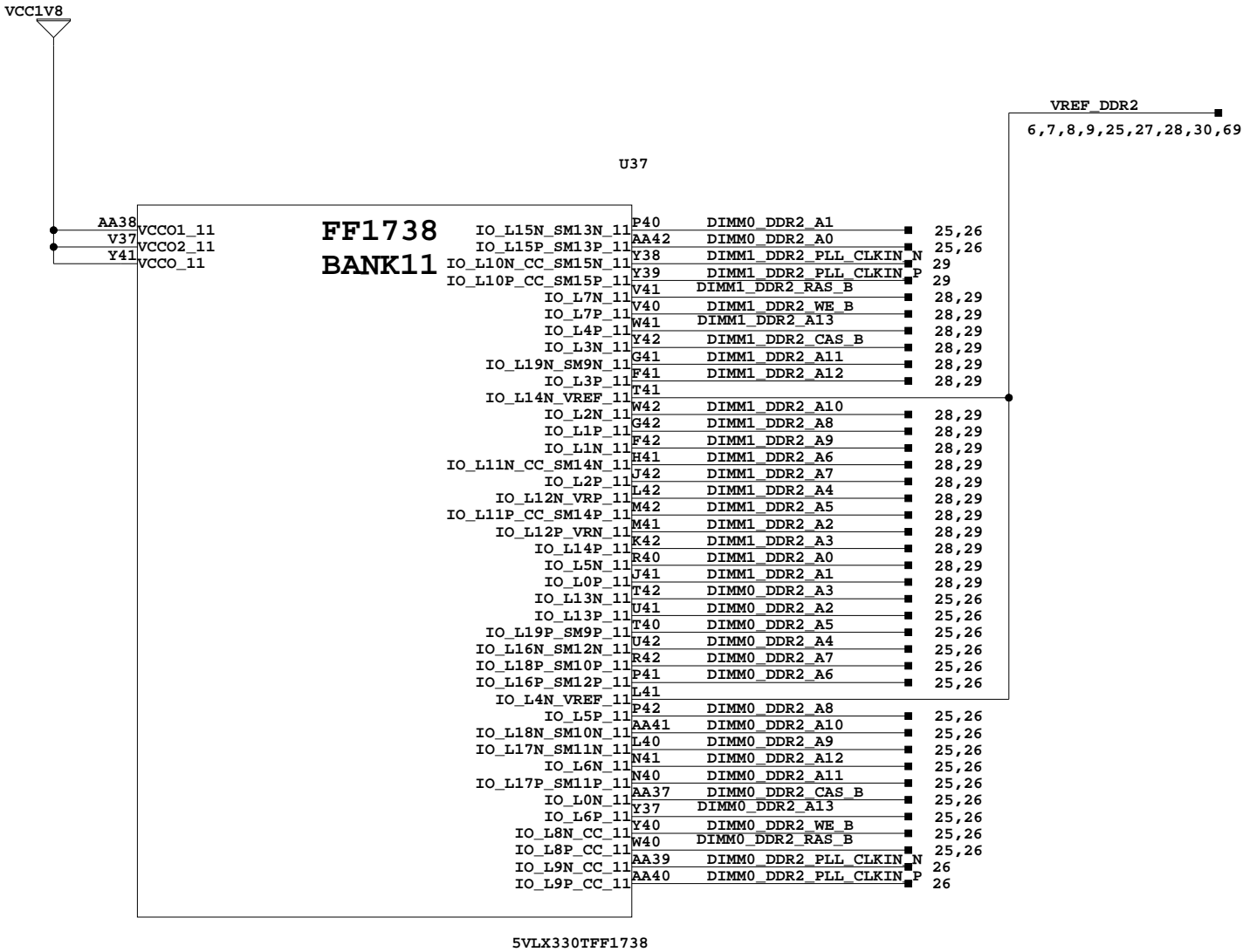
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		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
PAGE INDEX			
Date: 7-10-2008_10:19		Ver: C	
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FPGA - BANK 5,6

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
FPGA - BANK 5,6 - PM, DEBUG			
Date:	8-1-2008_15:03	Ver:	C
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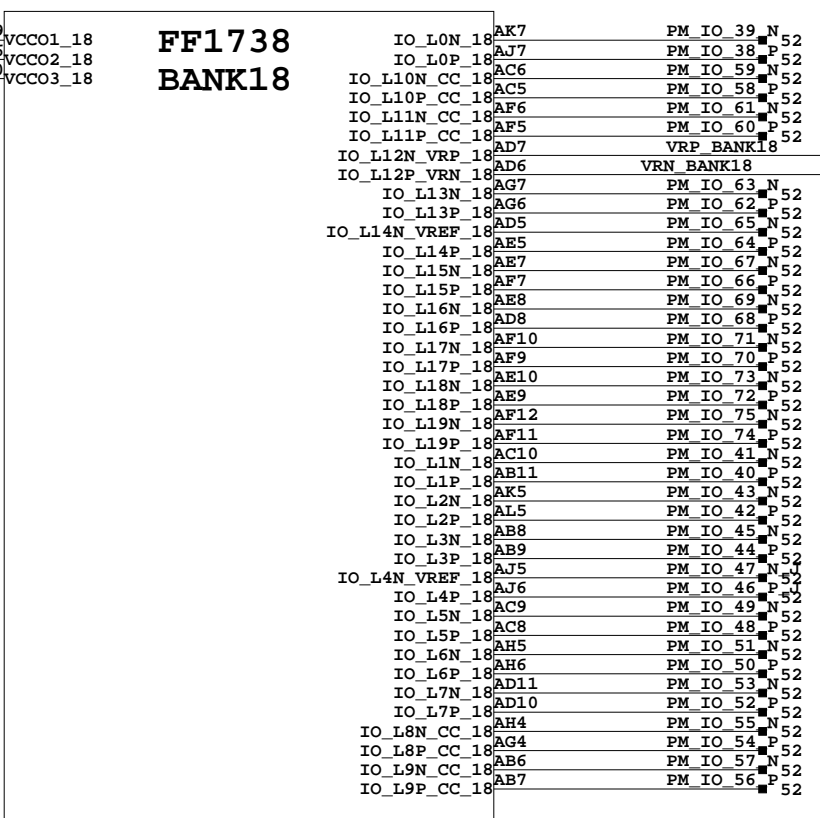
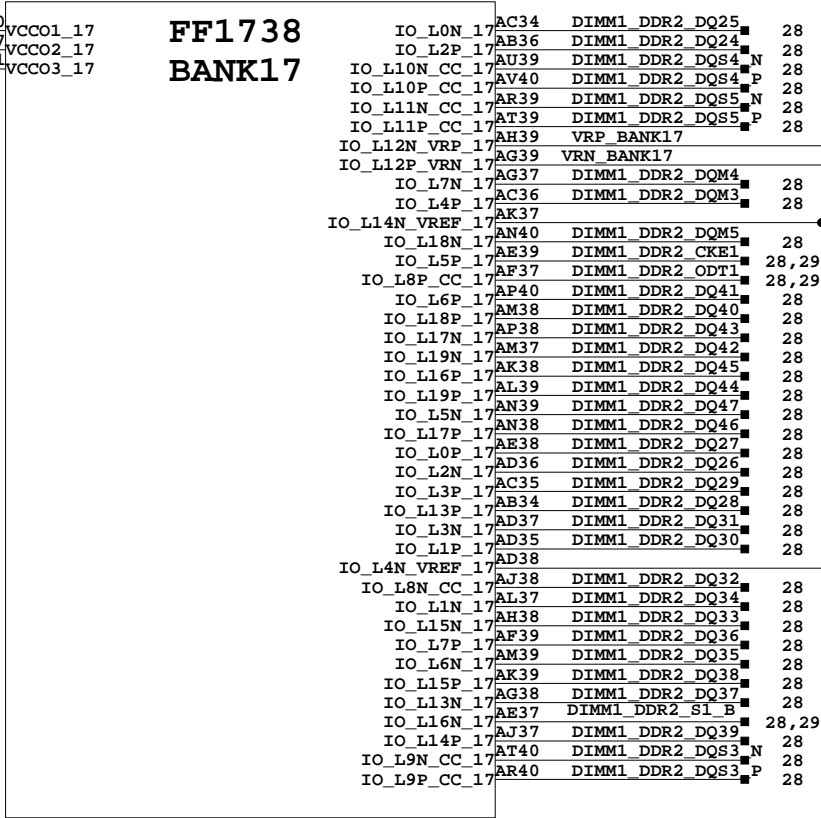
FPGA - BANK 11,12




SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

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FPGA - BANK 11,12 DDR2, PM, LCD

Date:	8-1-2008_15:03	Ver:	C
Sheet Size:	B	Rev:	01
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FPGA - BANK 17,18

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		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
FPGA - BANK 17,18 - DDR2, PM			
Date:	8-1-2008_15:03	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	7 of 70	Drawn By	BF

D

C

B

A

D

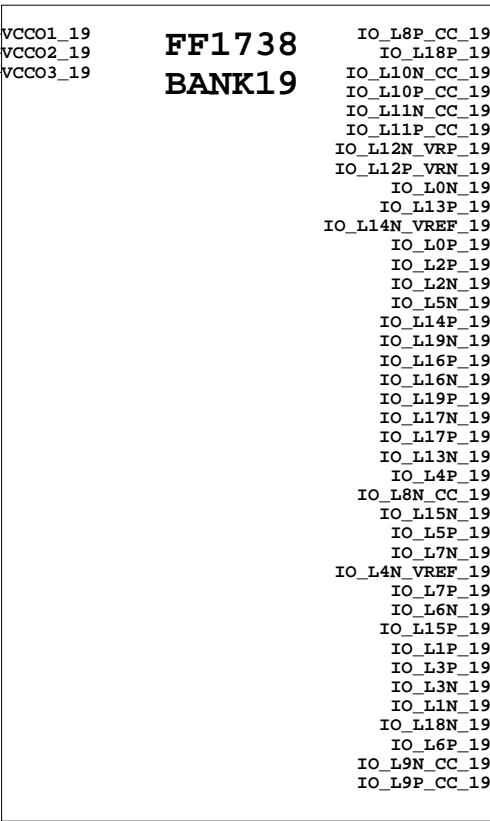
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B

A

VCC1V8

G40
K41
L38



5VLX330TFF1738

VREF_DDR2
5,6,7,9,25,27,28,30,69

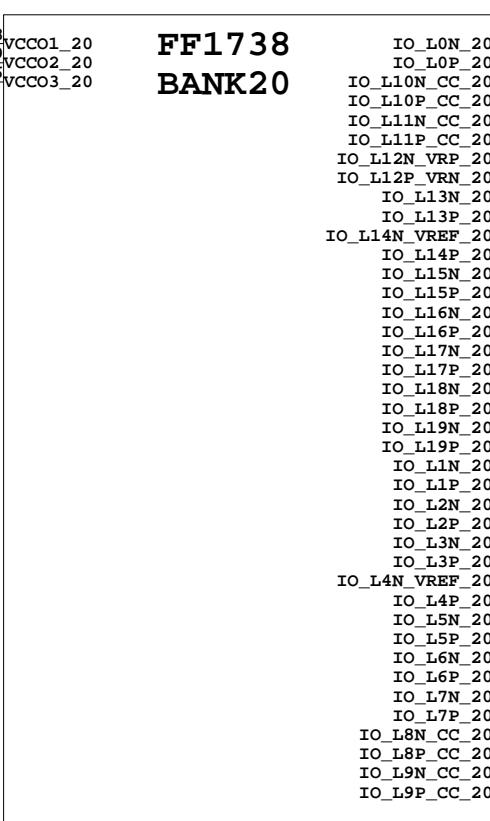
R277
49.9

49.9

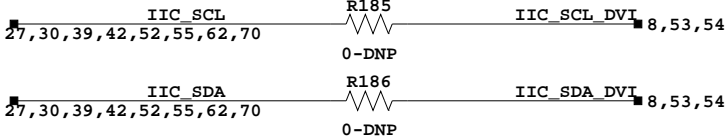
VCC1V8

VCC3_PCI

L8
P9
R6



5VLX330TFF1738



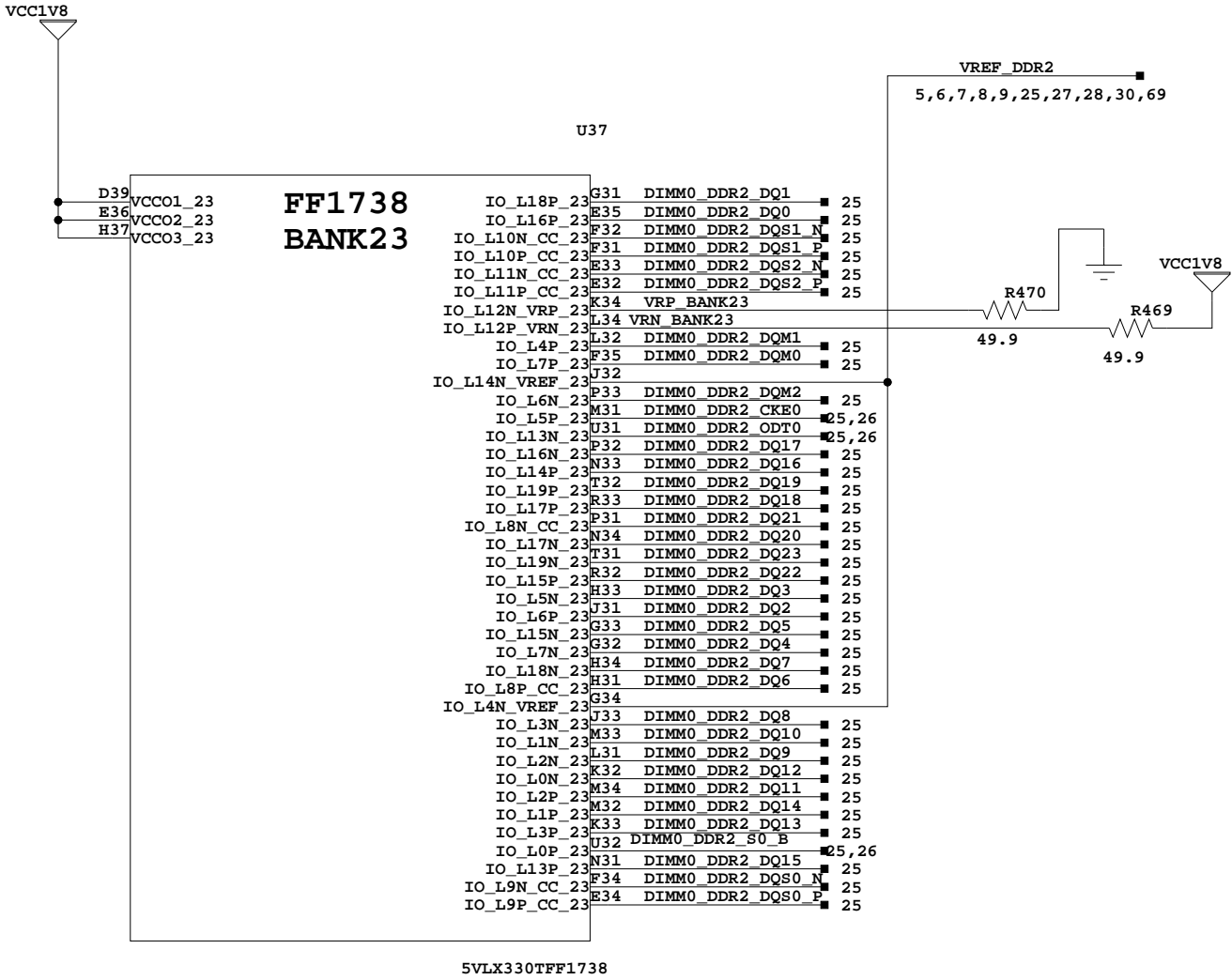
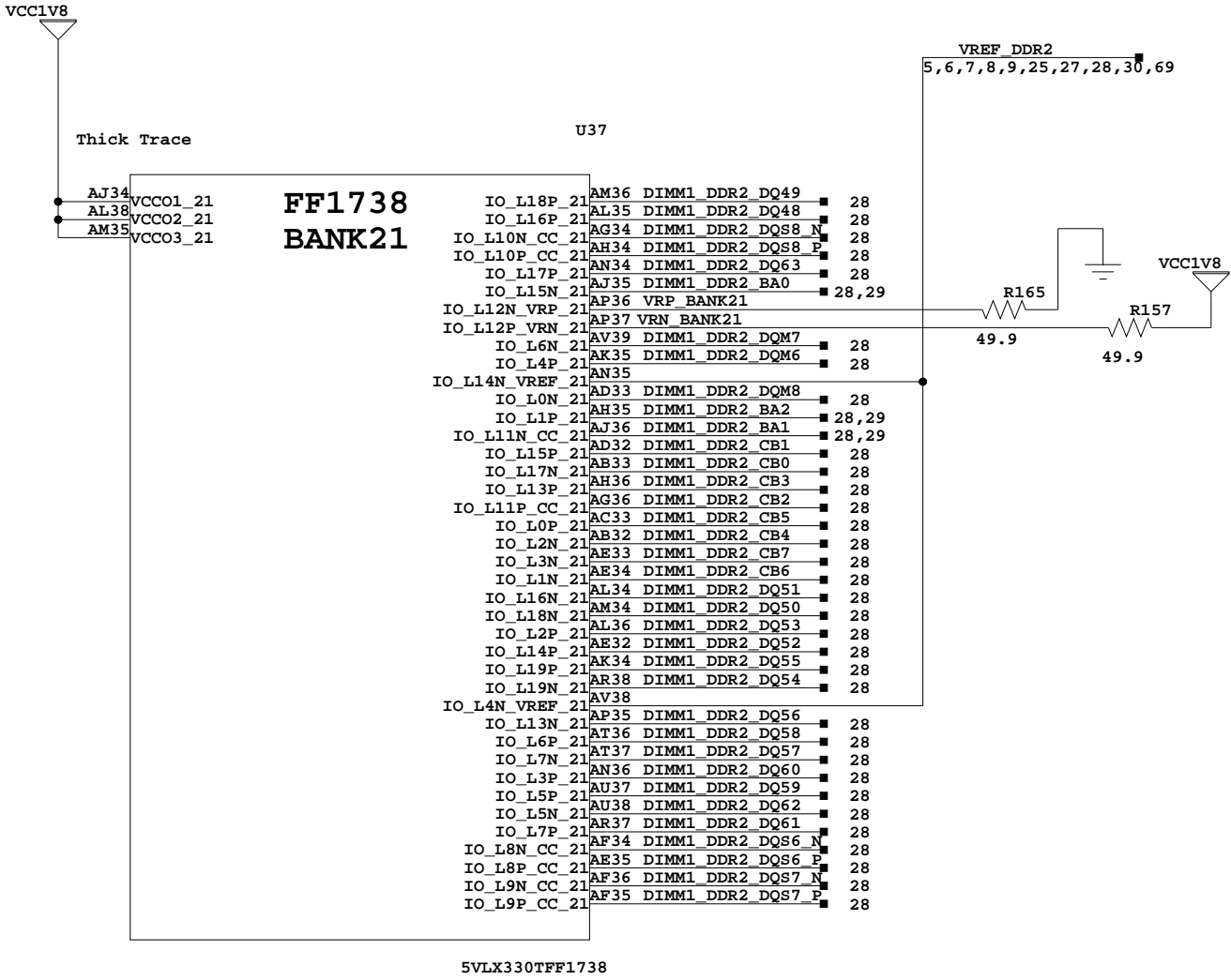
FPGA - BANK 19,20




SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA - BANK 19,20 DDR2, PCI, IIC, UART

Date:	8-1-2008_15:03	Ver:	C
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FPGA - BANK 21,23

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Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
FPGA - BANK 21,23 DDR2			
Date:	8-1-2008_15:03	Ver:	C
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VCC3_PCI

E6
G10
H7
VCCO1_24
VCCO2_24
VCCO3_24

FF1738
BANK24

IO_L0N_24	H11	PCI_P_RST_B	■33,35,37,38
IO_L0P_24	J12	PCI_P_LOCK_B	■33,35,37,38
IO_L10N_CC_24	L11	PCI_P_AD17	■33,35,37,40
IO_L10P_CC_24	L12	PCI_P_AD18	■33,35,37,40
IO_L11N_CC_24	G14	PCI_P_AD15	■33,35,37,40
IO_L11P_CC_24	G13	PCI_P_AD16	■33,35,37,40
IO_L12N_VRP_24	M12	PCI_P_AD13	■33,35,37,40
IO_L12P_VRN_24	M11	PCI_P_AD14	■33,35,37,40
IO_L13N_24	E13	PCI_P_AD11	■33,35,37,40
IO_L13P_24	F14	PCI_P_AD12	■33,35,37,40
IO_L14N_VREF_24	F12	PCI_P_AD9	■33,35,37,40
IO_L14P_24	N11	PCI_P_AD10	■33,35,37,40
IO_L15N_24	D12	PCI_P_AD7	■33,35,37,40
IO_L15P_24	E12	PCI_P_AD8	■33,35,37,40
IO_L16N_24	N10	PCI_P_AD5	■33,35,37,40
IO_L16P_24	P11	PCI_P_AD6	■33,35,37,40
IO_L17N_24	E14	PCI_P_AD3	■33,35,37,40
IO_L17P_24	D13	PCI_P_AD4	■33,35,37,40
IO_L18N_24	P10	PCI_P_AD1	■33,35,37,40
IO_L18P_24	R10	PCI_P_AD2	■33,35,37,40
IO_L19N_24	F15	PCI_P_CBE3_B	■33,35,37,40
IO_L19P_24	E15	PCI_P_AD0	■33,35,37,40
IO_L1N_24	G11	PCI_P_INTB_B	■84,35,36,37,38,40
IO_L1P_24	G12	PCI_P_INTA_B	■84,35,36,37,38,40
IO_L2N_24	F11	PCI_P_INTD_B	■84,35,36,37,38,40
IO_L2P_24	F12	PCI_P_INTC_B	■84,35,36,37,38,40
IO_L3N_24	F10	PCI_P_AD31	■33,35,37,40
IO_L3P_24	E10	PCI_FPGA_IDSEL	■39
IO_L4N_VREF_24	K13	PCI_P_AD29	■33,35,37,40
IO_L4P_24	K14	PCI_P_AD30	■33,35,37,40
IO_L5N_24	J11	PCI_P_AD27	■33,35,37,40
IO_L5P_24	K12	PCI_P_AD28	■33,35,37,40
IO_L6N_24	H13	PCI_P_AD25	■33,35,37,40
IO_L6P_24	J13	PCI_P_AD26	■33,35,37,40
IO_L7N_24	J10	PCI_P_AD23	■33,35,37,40
IO_L7P_24	H10	PCI_P_AD24	■33,35,37,40
IO_L8N_CC_24	H15	PCI_P_AD21	■33,35,37,39,40
IO_L8P_CC_24	H14	PCI_P_AD22	■33,35,37,40
IO_L9N_CC_24	L10	PCI_P_AD19	■33,35,37,40
IO_L9P_CC_24	K10	PCI_P_AD20	■33,35,37,40

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U37

VCC2V5

AP39
AR36
AU40
VCCO1_25
VCCO2_25
VCCO3_25

FF1738
BANK25

IO_L0N_25	AF31	PM_IO_77_N	■52
IO_L0P_25	AG31	PM_IO_76_P	■52
IO_L10N_CC_25	AU31	PHY1_MDC	■50
IO_L10P_CC_25	AV31	PHY1_INT_SGMII	■50
IO_L11N_CC_25	AT31	PHY0_TXER	■49
IO_L11P_CC_25	AT32	PHY1_MDIO	■50
IO_L12N_VRP_25	AN31	PHY0_TXD3	■49
IO_L12P_VRN_25	AP31	PHY0_TXCTL_TXEN	■49
IO_L13N_25	AP32	PHY0_TXD1	■49
IO_L13P_25	AR32	PHY0_TXD2	■49
IO_L14N_VREF_25	AP33	PHY0_RXER	■49
IO_L14P_25	AR33	PHY0_TXD0	■49
IO_L15N_25	AM33	PHY0_RXD3	■49
IO_L15P_25	AN33	PHY0_RXCTL_RXDV	■49
IO_L16N_25	AJ33	PHY0_RXD1	■49
IO_L16P_25	AK33	PHY0_RXD2	■49
IO_L17N_25	AK32	PHY0_RESET	■49
IO_L17P_25	AJ32	PHY0_RXD0	■49
IO_L18N_25	AM32	PHY0_MDC	■49
IO_L18P_25	AL32	PHY0_INT	■49
IO_L19N_25	AM31	PHY0_GTXCLK	■49
IO_L19P_25	AL31	PHY0_MDIO	■49
IO_L1N_25	AG33	PM_IO_79_N	■52
IO_L1P_25	AF32	PM_IO_78_P	■52
IO_L2N_25	AG32	PM_IO_81_N	■52
IO_L2P_25	AH33	PM_IO_80_P	■52
IO_L3N_25	AJ31	PM_IO_83_N	■52
IO_L3P_25	AH31	PM_IO_82_P	■52
IO_L4N_VREF_25	AV36	PM_IO_85_N	■52
IO_L4P_25	AV35	PM_IO_84_P	■52
IO_L5N_25	AT35	PM_IO_87_N	■52
IO_L5P_25	AU36	PM_IO_86_P	■52
IO_L6N_25	AT34	PM_IO_89_N	■52
IO_L6P_25	AU34	PM_IO_88_P	■52
IO_L7N_25	AR34	PM_IO_91_N	■52
IO_L7P_25	AR35	PM_IO_90_P	■52
IO_L8N_CC_25	AU33	PM_IO_93_N	■52
IO_L8P_CC_25	AU32	PM_IO_92_P	■52
IO_L9N_CC_25	AV34	PM_IO_95_N	■52
IO_L9P_CC_25	AV33	PM_IO_94_P	■52

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U37

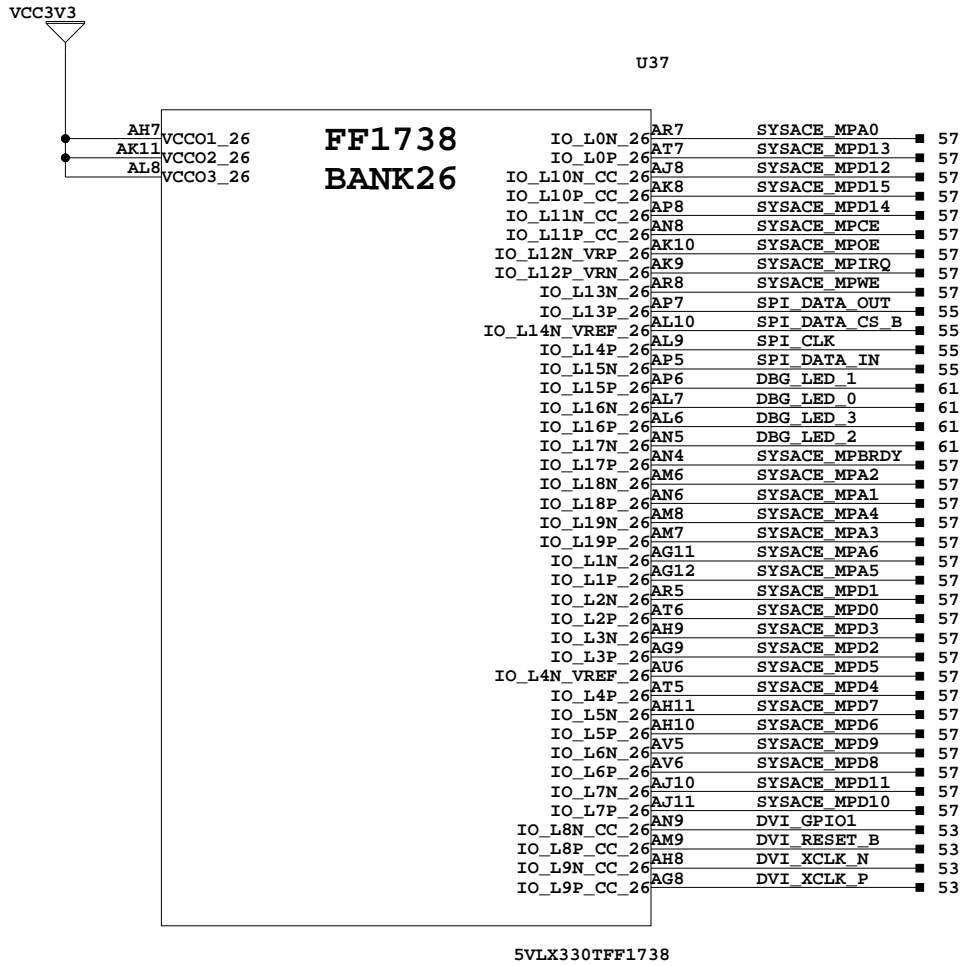
FPGA - BANK 24,25




SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

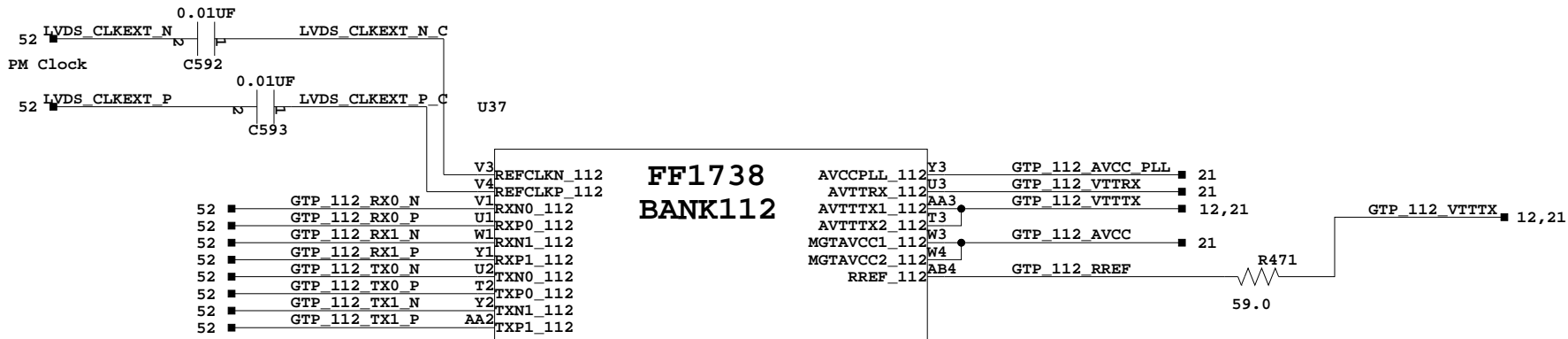
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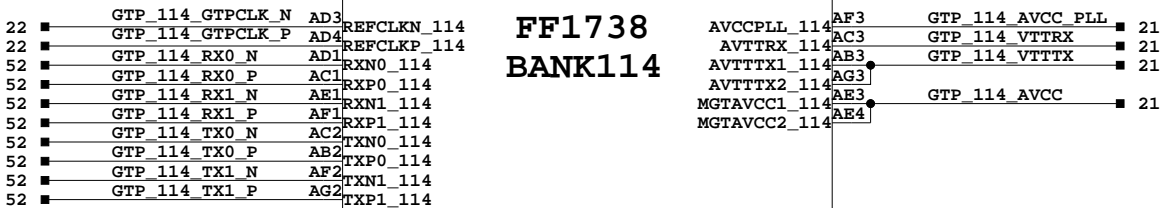
FPGA - BANK 26

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FPGA - BANK 26 SYSTEM ACE, DVI, SPI, LEDS			
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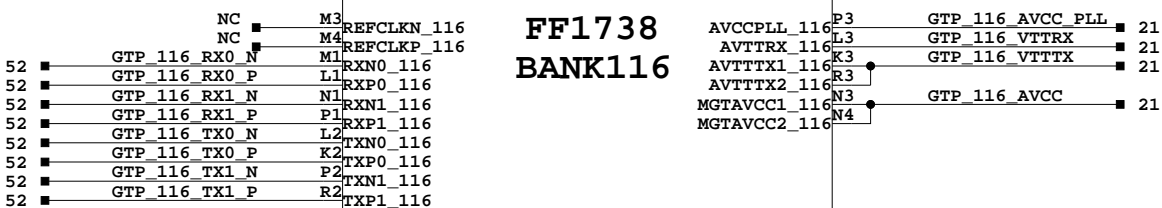
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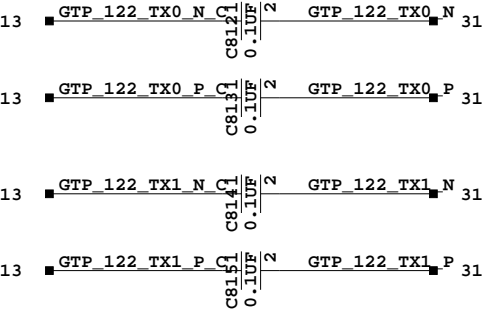
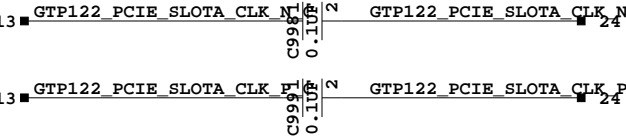
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FPGA - BANK 112, 114, 116

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FPGA-BANK 112, 114, 116 PERSONALITY MODULES			
Date:	8-1-2008_15:03	Ver:	C
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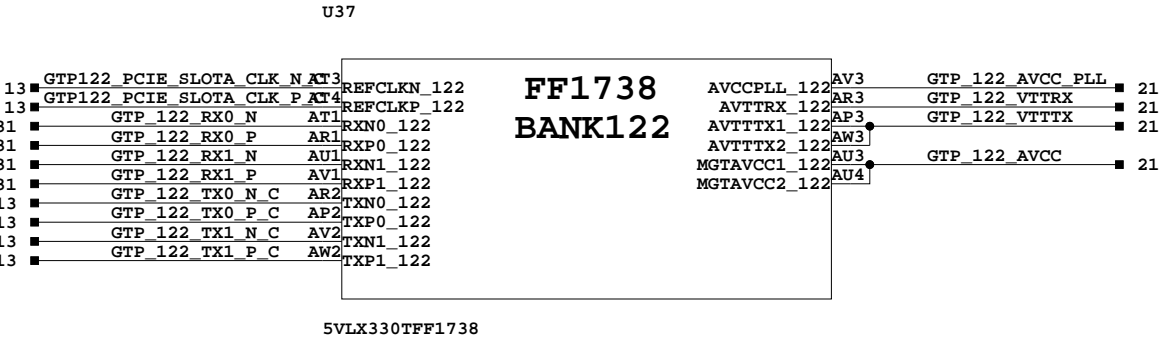
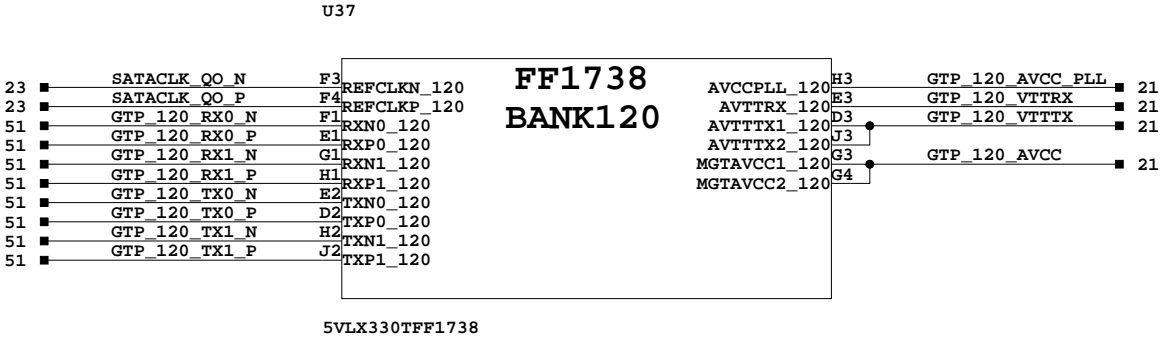
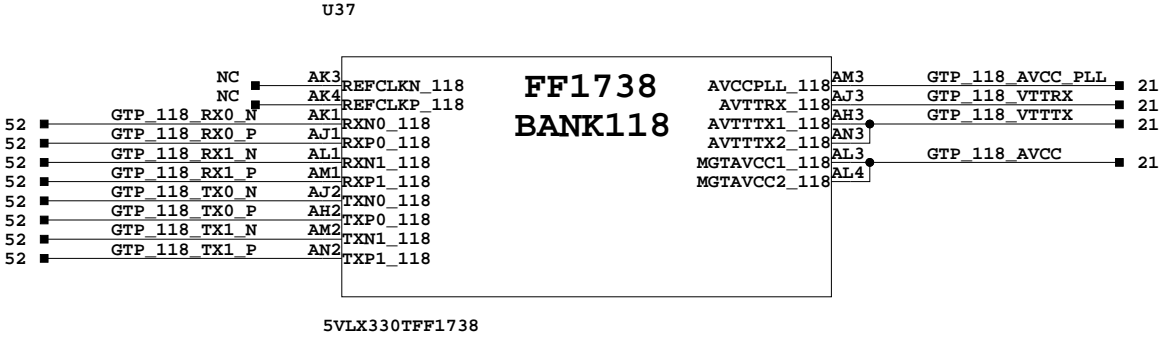
FPGA - BANK 118,120,122

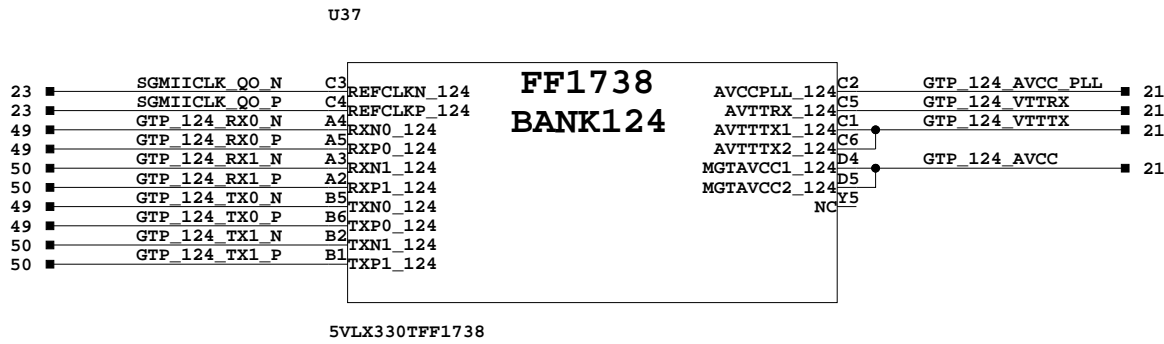
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FPGA - BANK 118,120,122 PM, SATA, PCI-E		
Date:	8-1-2008_15:03	Ver: C
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PM

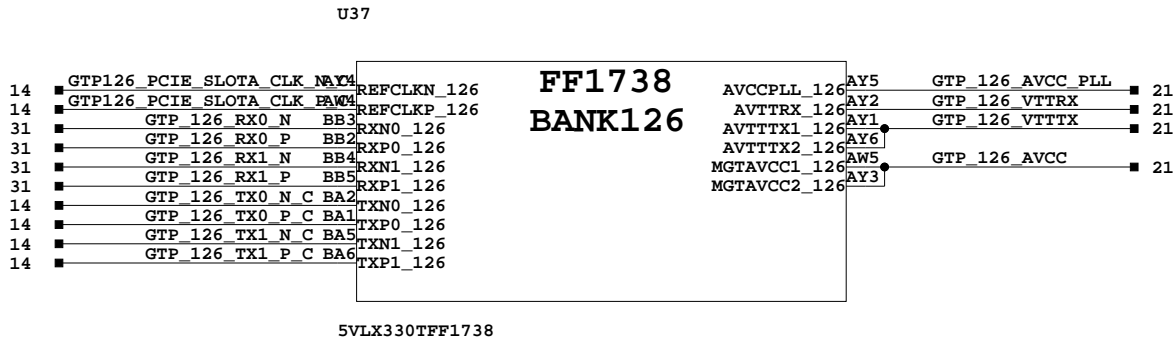
SATA
SATA Clock

PCie Slot A

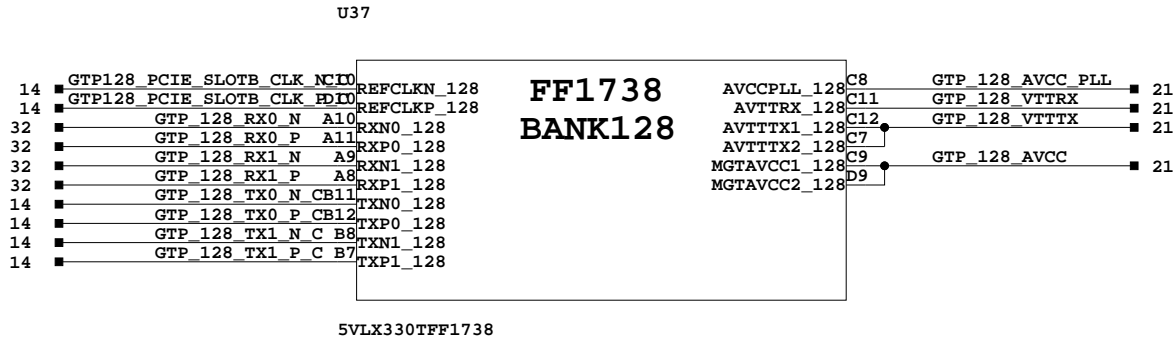




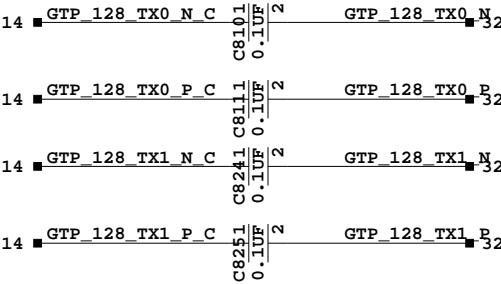
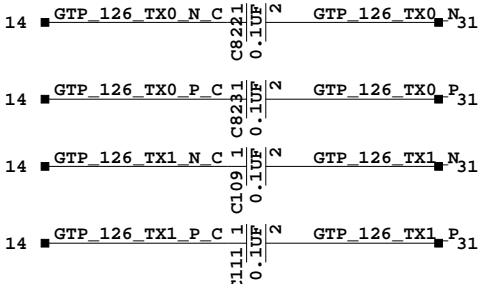
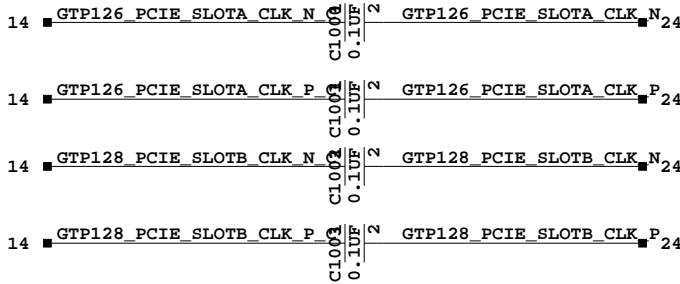
SGMII



PCIe Slot A

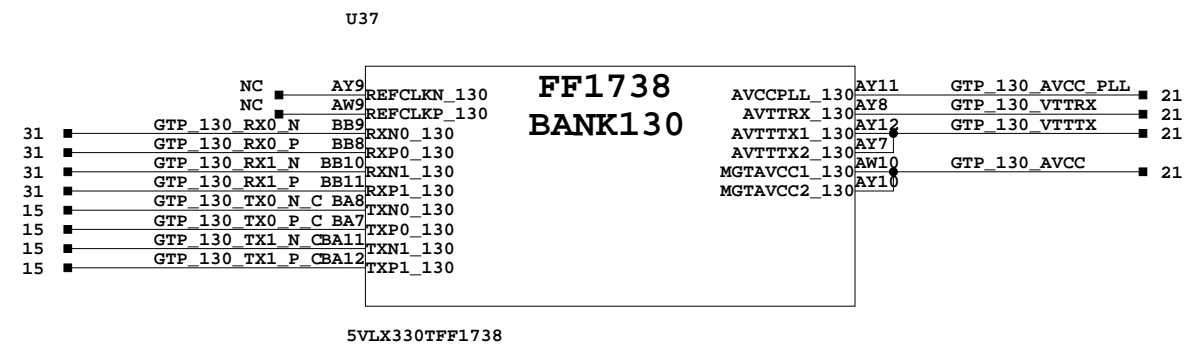


PCIe Slot B
(FX130T / FX200T / LX330T only)

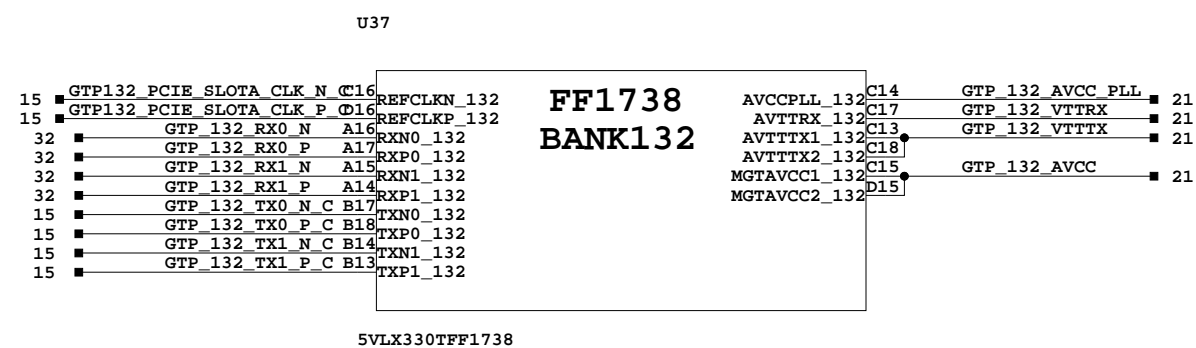


FPGA - BANK 124,126,128

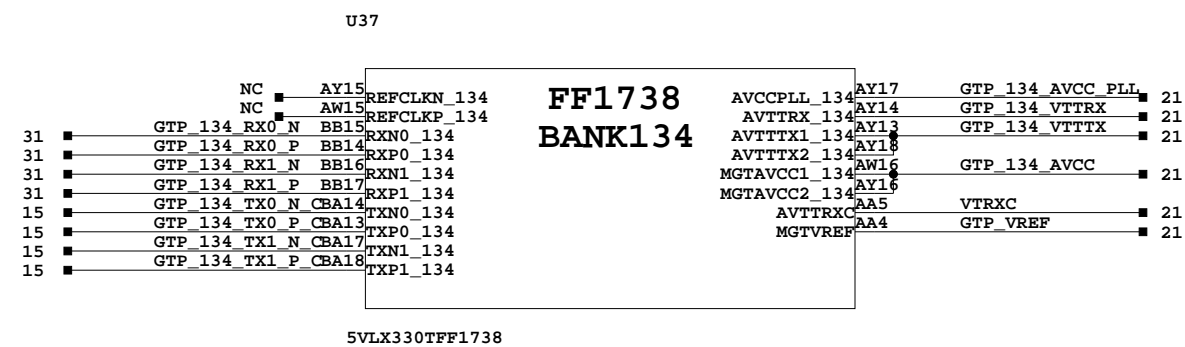
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FPGA - BANK 124,126,128 SGMII, PCI-E			
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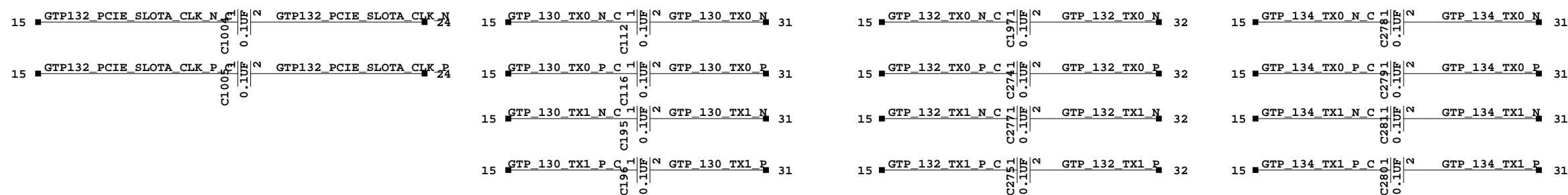
PCIe Slot A
(FX130T / FX200T / LX330T only)



PCIe Slot B
(FX200T / LX330T only)



PCIe Slot A
(FX200T / LX330T only)



FPGA - BANK 130,132,134



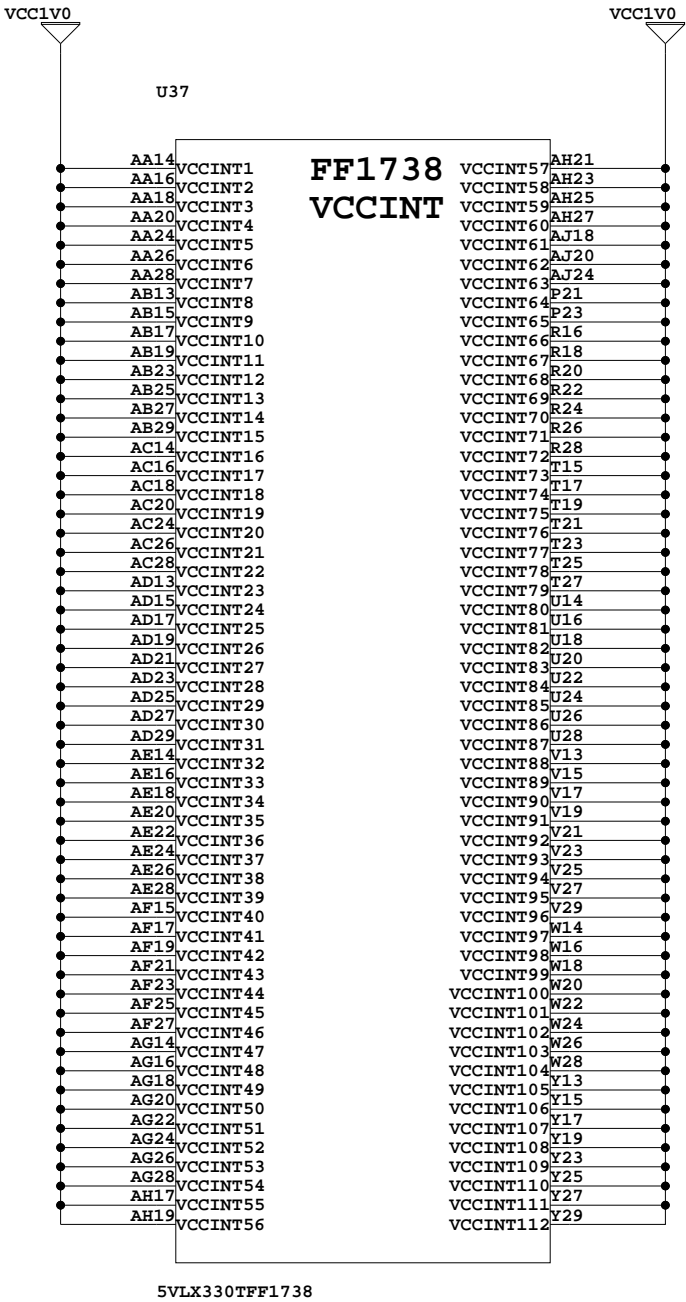
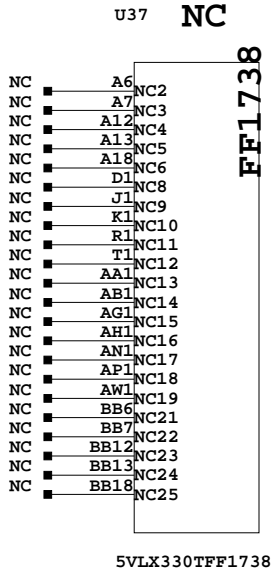
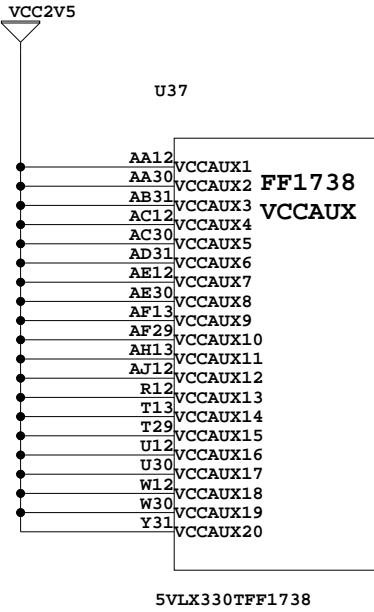
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FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA - BANK 130,132,134 PCI-E


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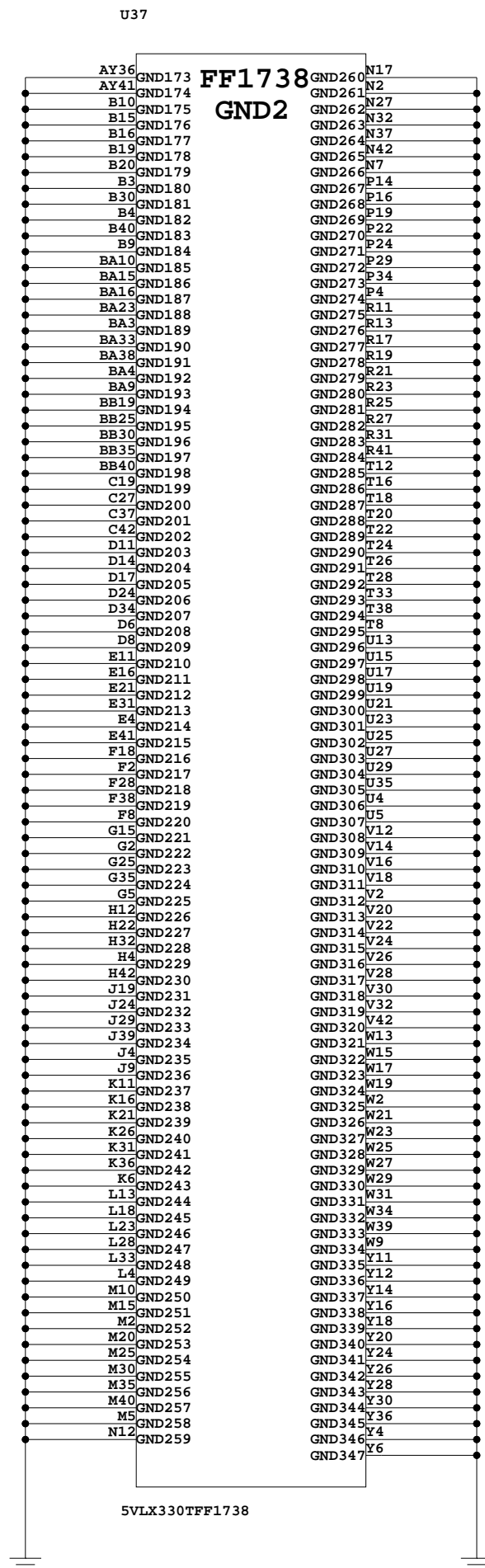
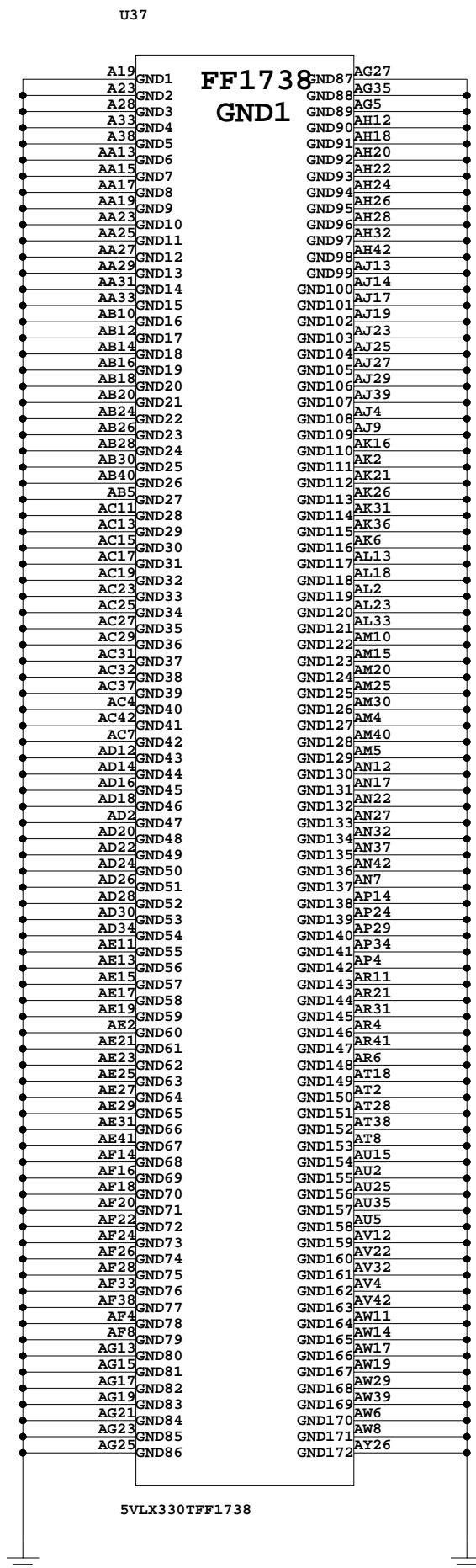
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FPGA - VCCAUX, VCCINT, NC

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
FPGA - VCCAUX, VCCINT, NC			
Date:	8-1-2008_15:04	Ver:	C
Sheet Size: B		Rev:	01
Sheet	16 of 70	Drawn By	BF



FPGA - GND



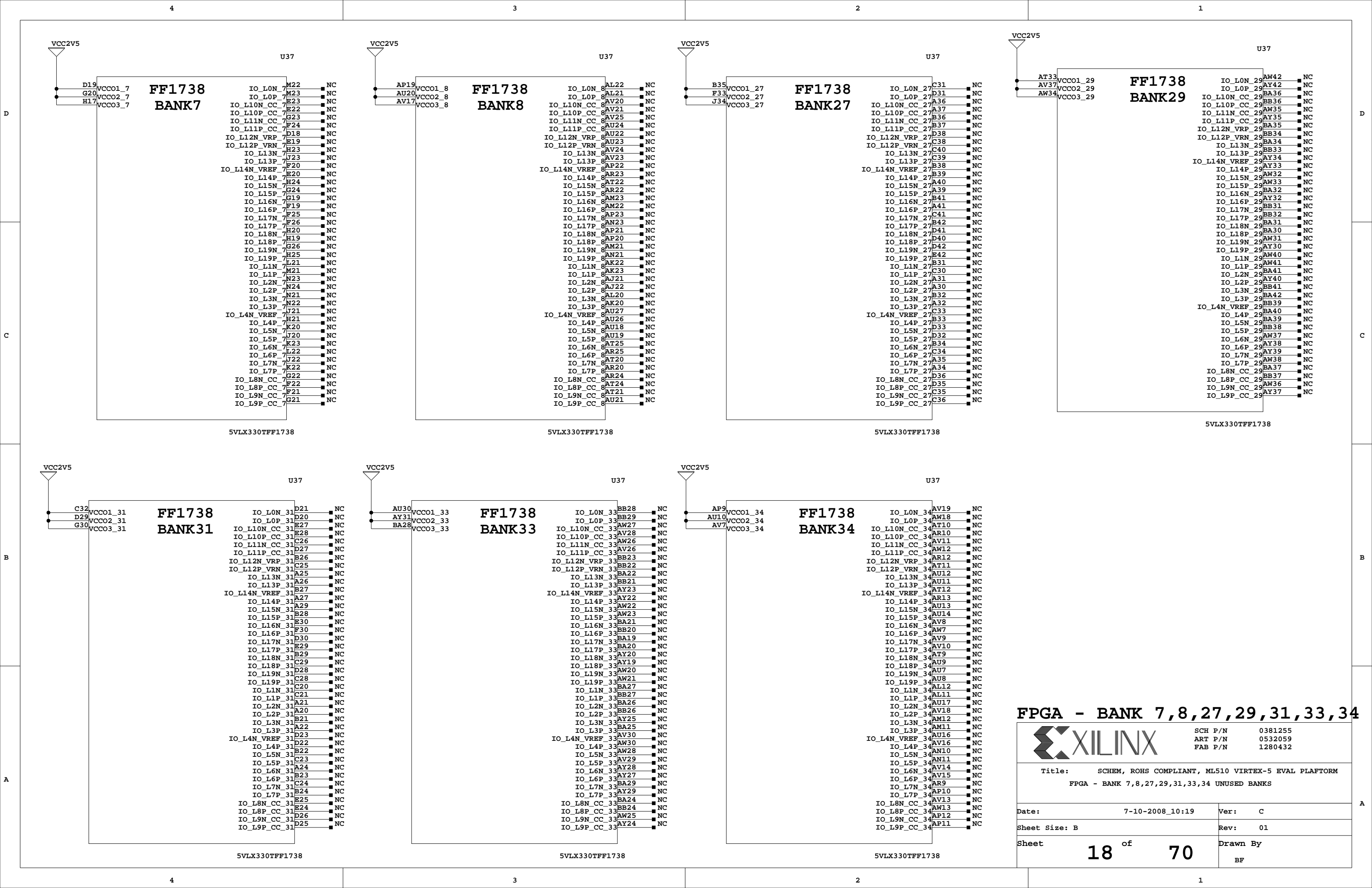
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA GROUND PINS


Date:	7-10-2008_10:19	Ver:	C
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Sheet Size: B	Rev: 01
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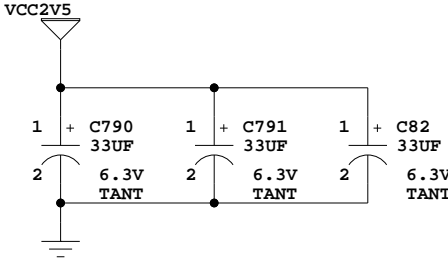
Sheet	17	of	70	Drawn By	BF
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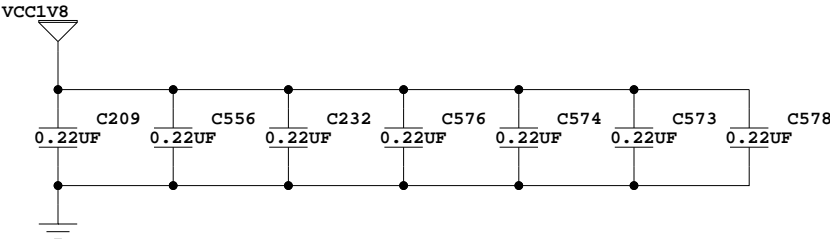
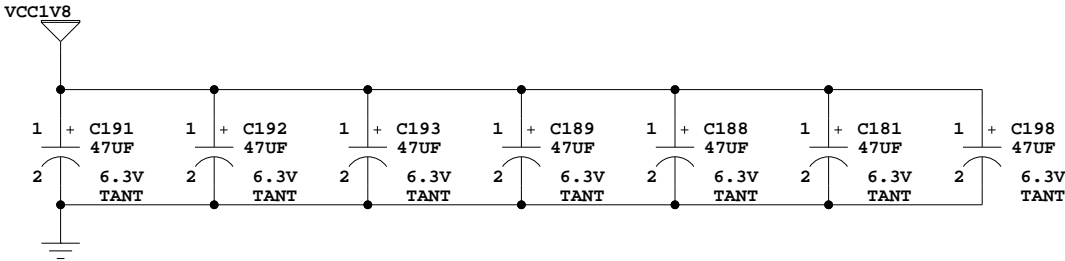
FPGA - BANK 7,8,27,29,31,33,34

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM FPGA - BANK 7,8,27,29,31,33,34 UNUSED BANKS			
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	18 of 70	Drawn By	BF

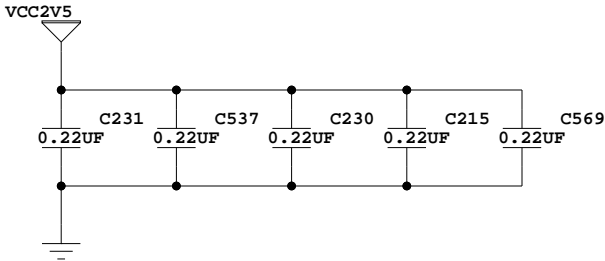
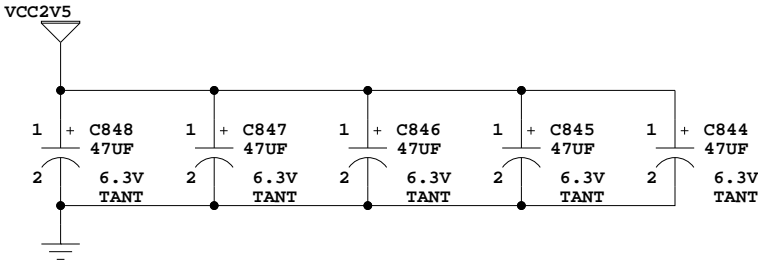
VCCAUX 2.5V



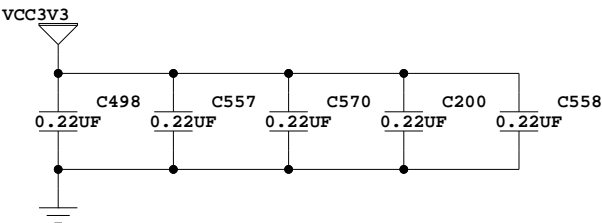
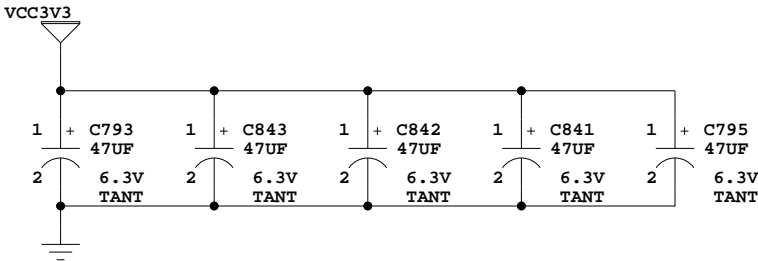
VCCO 1.8V



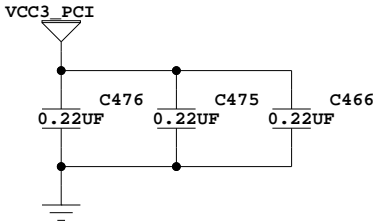
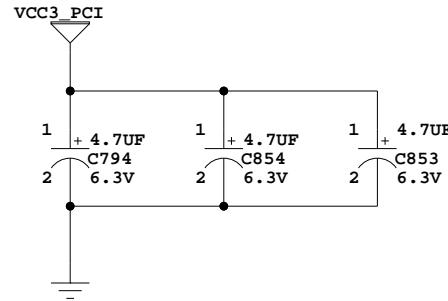
VCCO 2.5V



VCCO 3.3V




VCCO 3.0V PCI



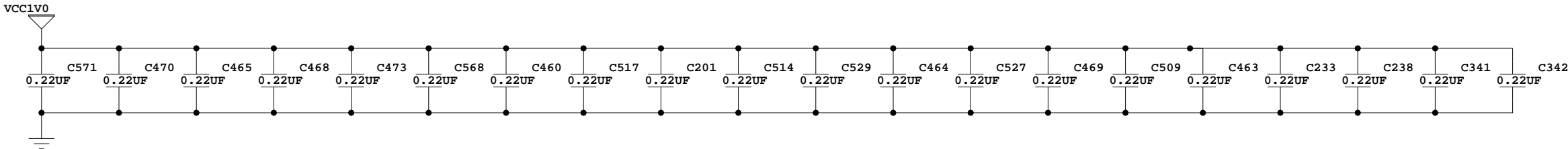
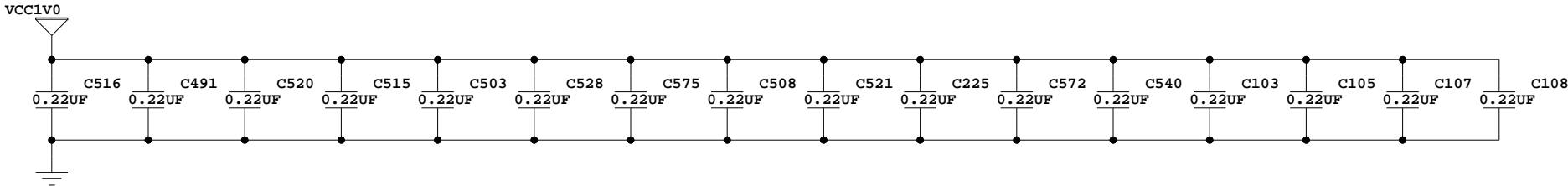
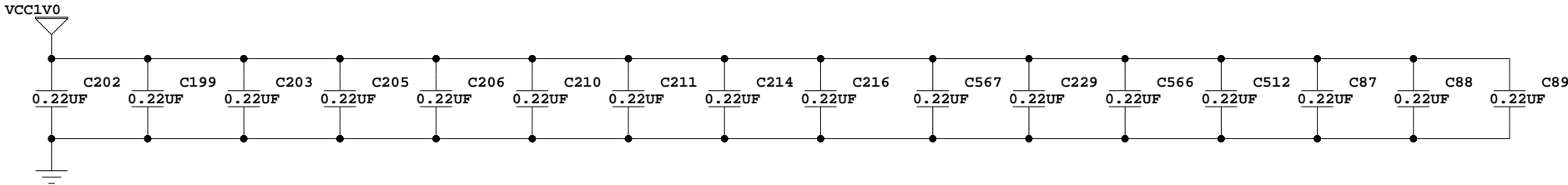
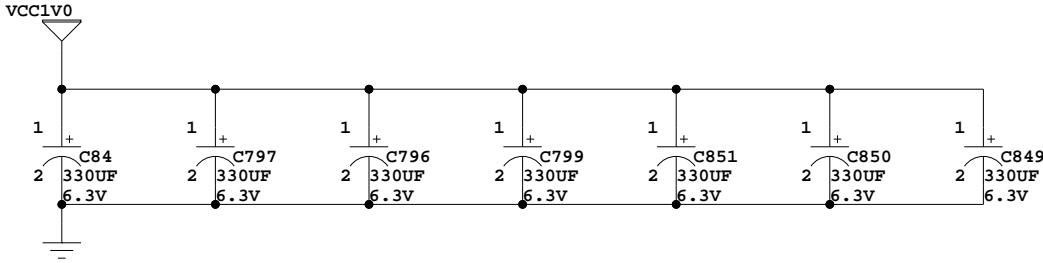
Supply	Banks Used	Capacitors Used
VCCAUX 2.5V	N/A	33uf: 3
VCCINT 1.0V	N/A	330uf: 7 / 0.22uf: 52
VCCO 3.3V	0,1,2,4,26	47uf: 5 / 0.22uf: 5
VCCO 2.5V	3,5,6,18,25	47uf: 5 / 0.22uf: 5
VCCO 1.8V	11,13,15,17,19,21,23	47uf: 7 / 0.22uf: 7
VCCO 3.0V PCI	12,20,24	47uf: 3 / 0.22uf: 3

Note: Bank 12 defaults to 3.0V_PCI


FPGA DECOUPLING

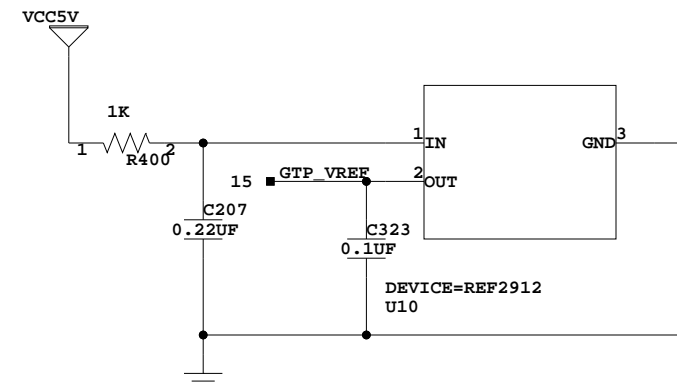
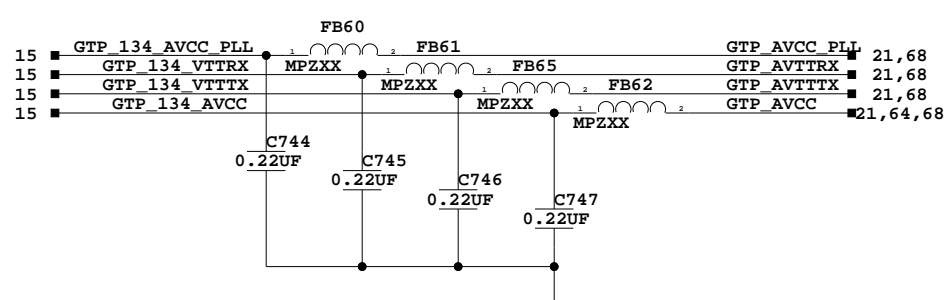
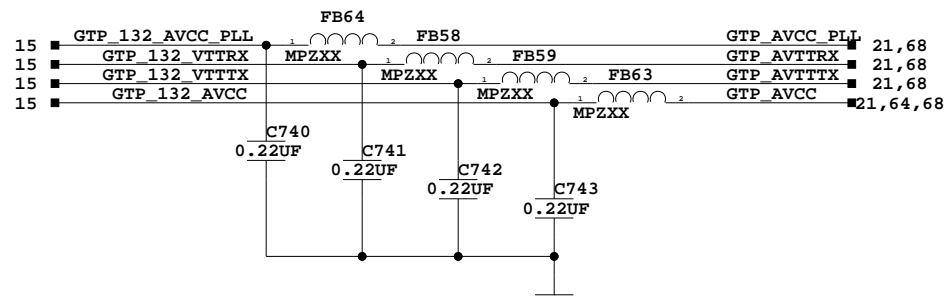
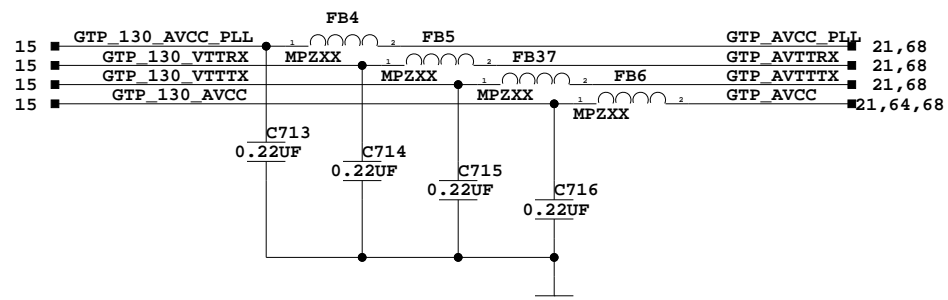
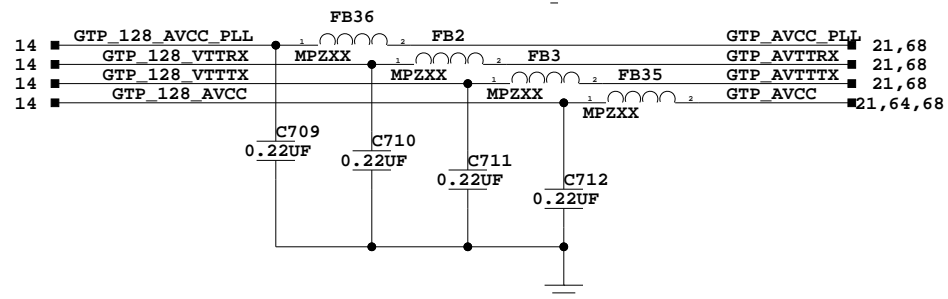
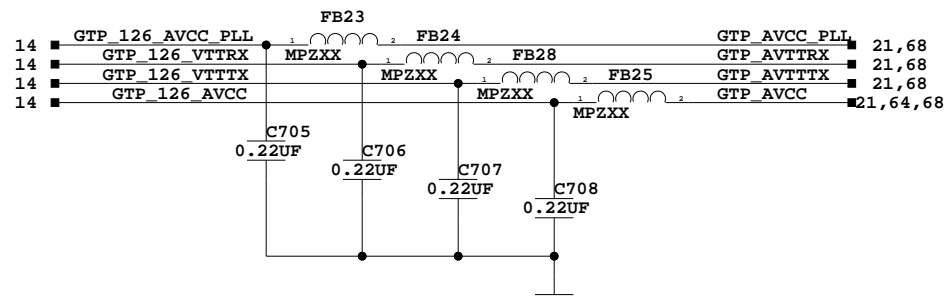
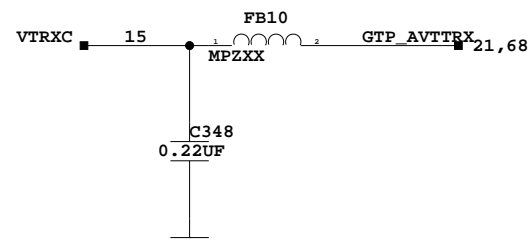
		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm			
FPGA DECOUPLING			
Date: 7-10-2008_10:19		Ver:	C
Sheet Size: B		Rev:	01
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VCCINT 1.0V



FPGA DECOUPLING PAGE 2

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
FPGA DECOUPLING PAGE 2		
Date:	7-10-2008_10:19	Ver: C
Sheet Size: B		Rev: 01
Sheet	20 of 70	Drawn By BF



GTP POWER FILTER



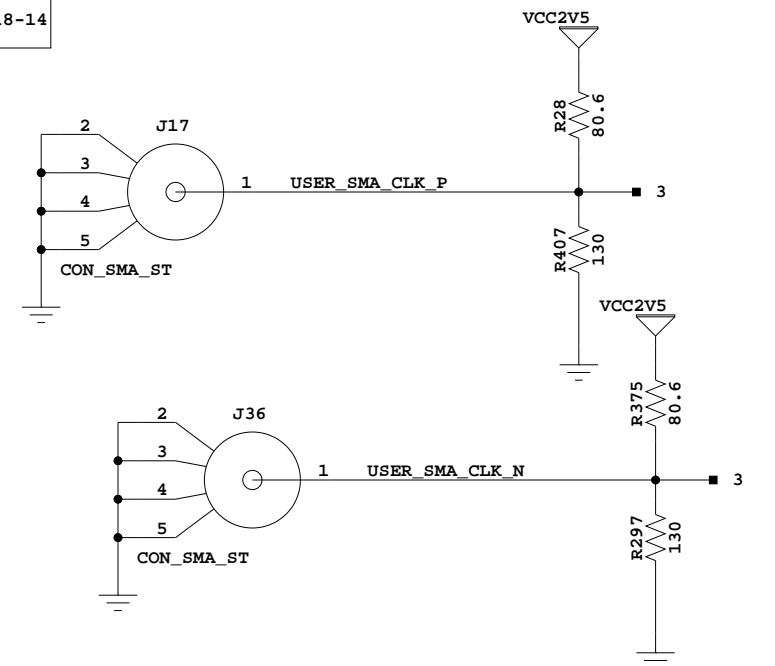
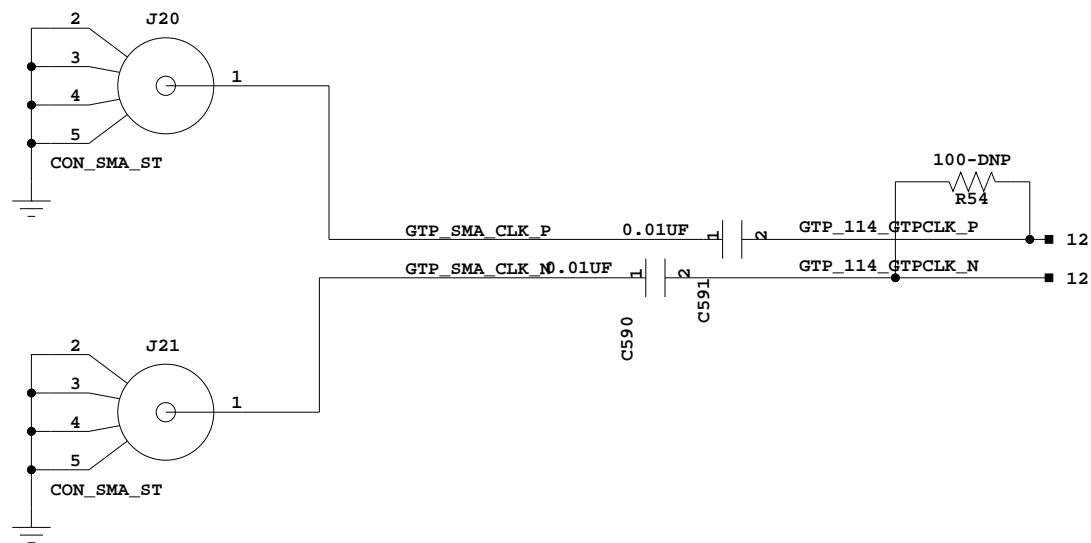
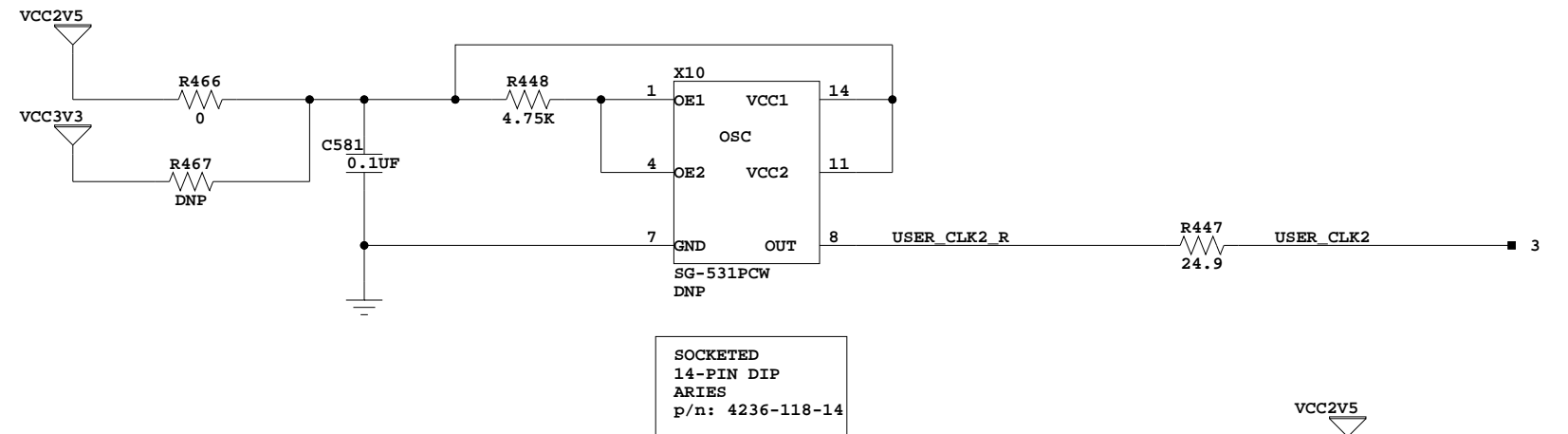
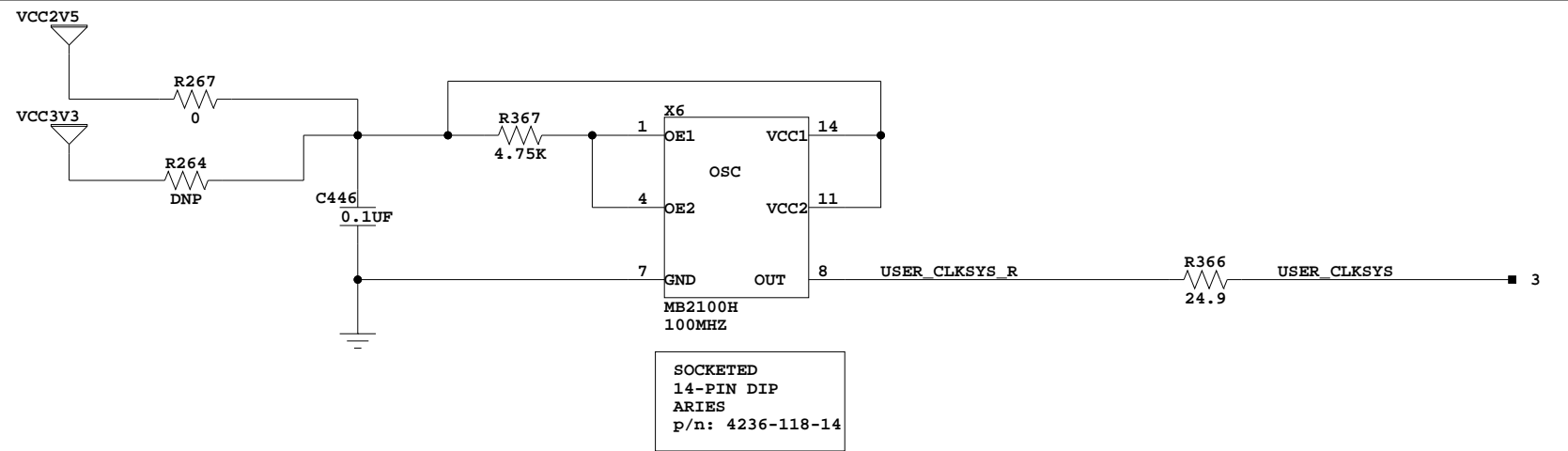
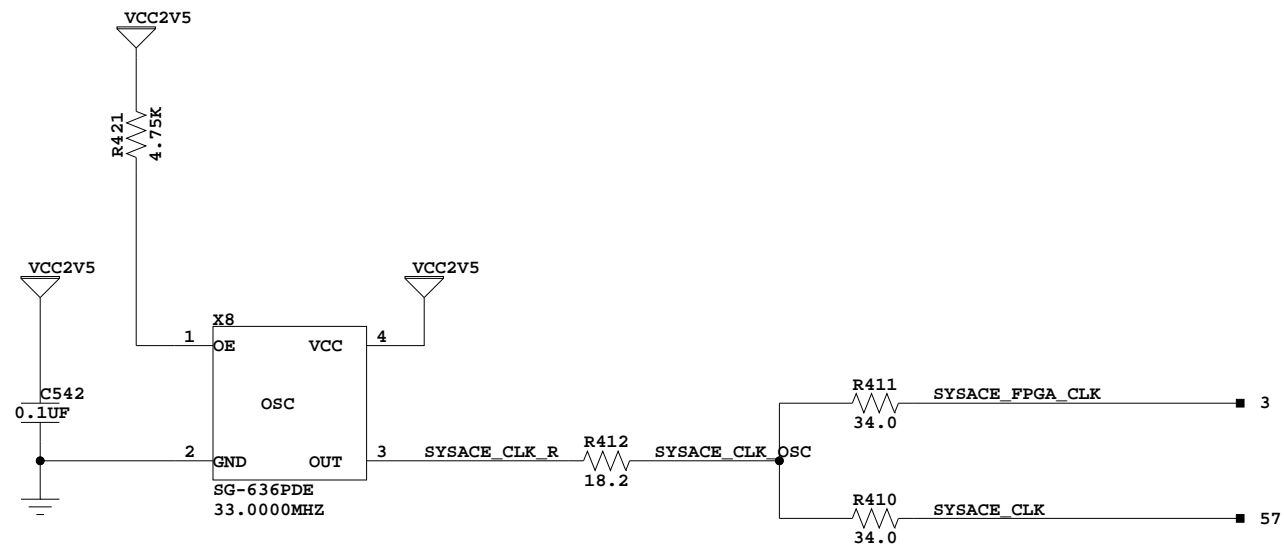
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
GTP POWER FILTER

Date:	7-10-2008_10:19	Ver:	C
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Sheet Size: B	Rev: 01
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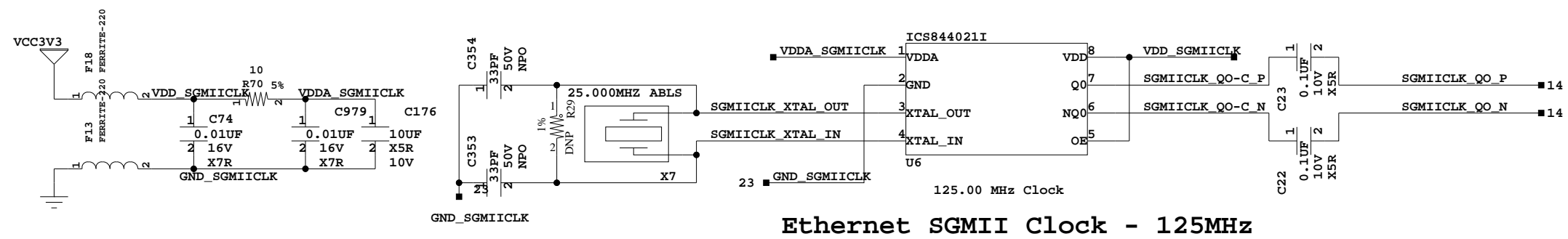
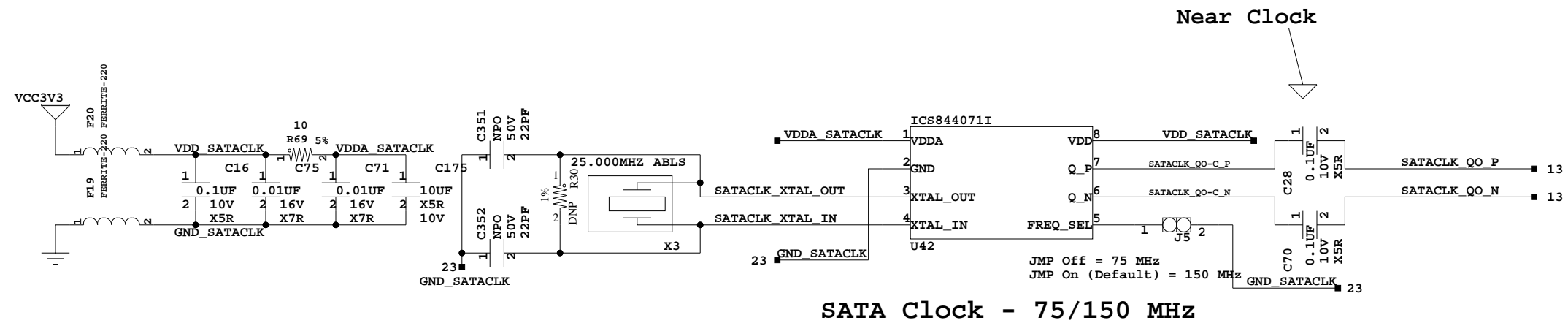
CLOCKS: USER,MGT,SYSACE



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

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Title:      SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
          CLKS: USR,MGT,SYSACE
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Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	22 of 70	Drawn By	BF



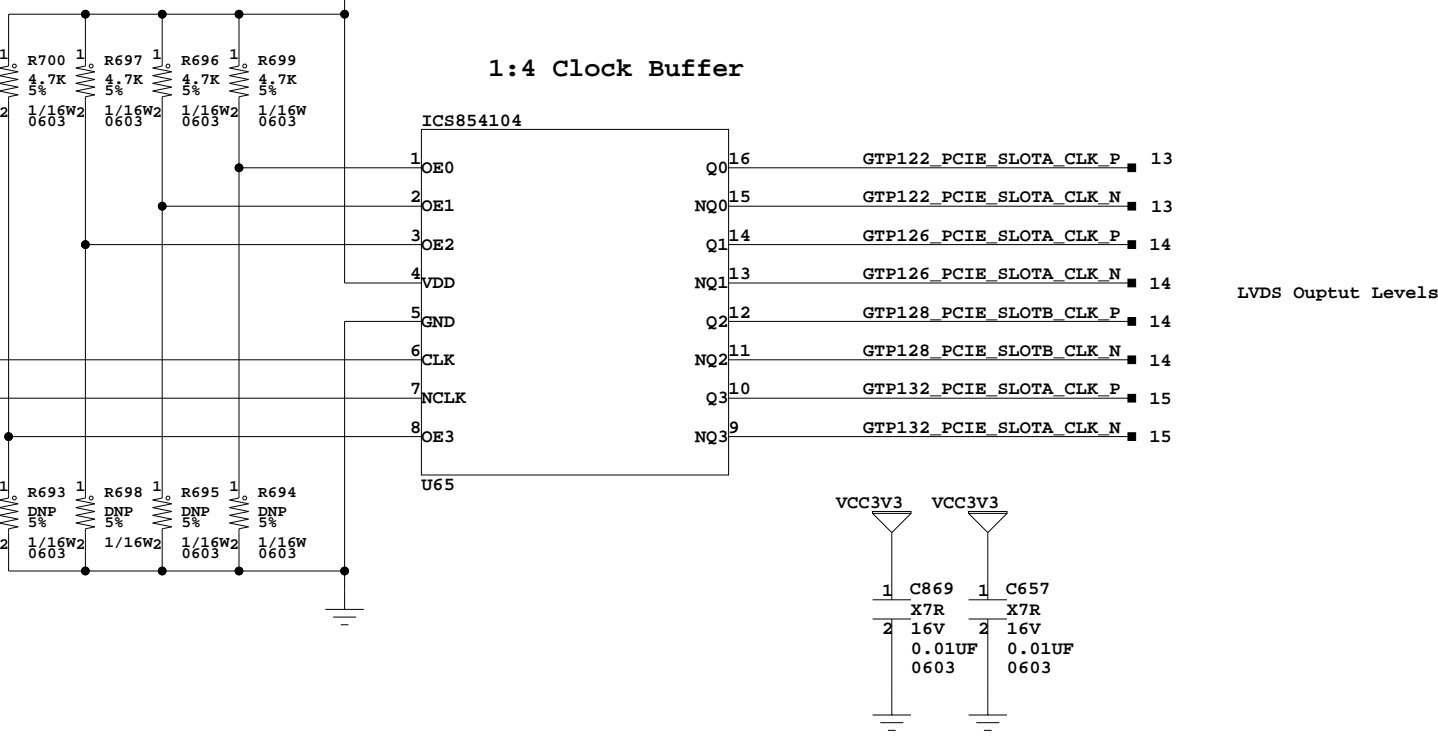
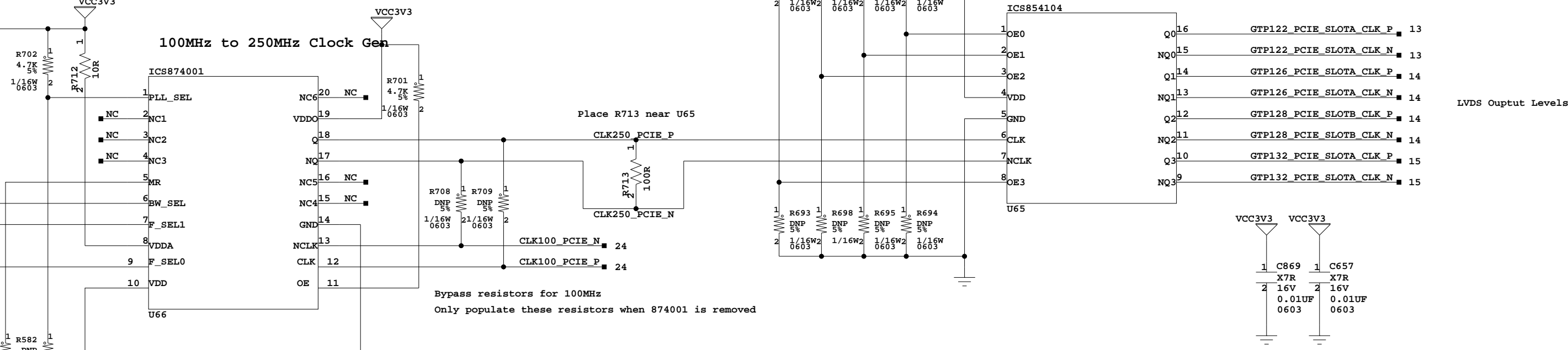
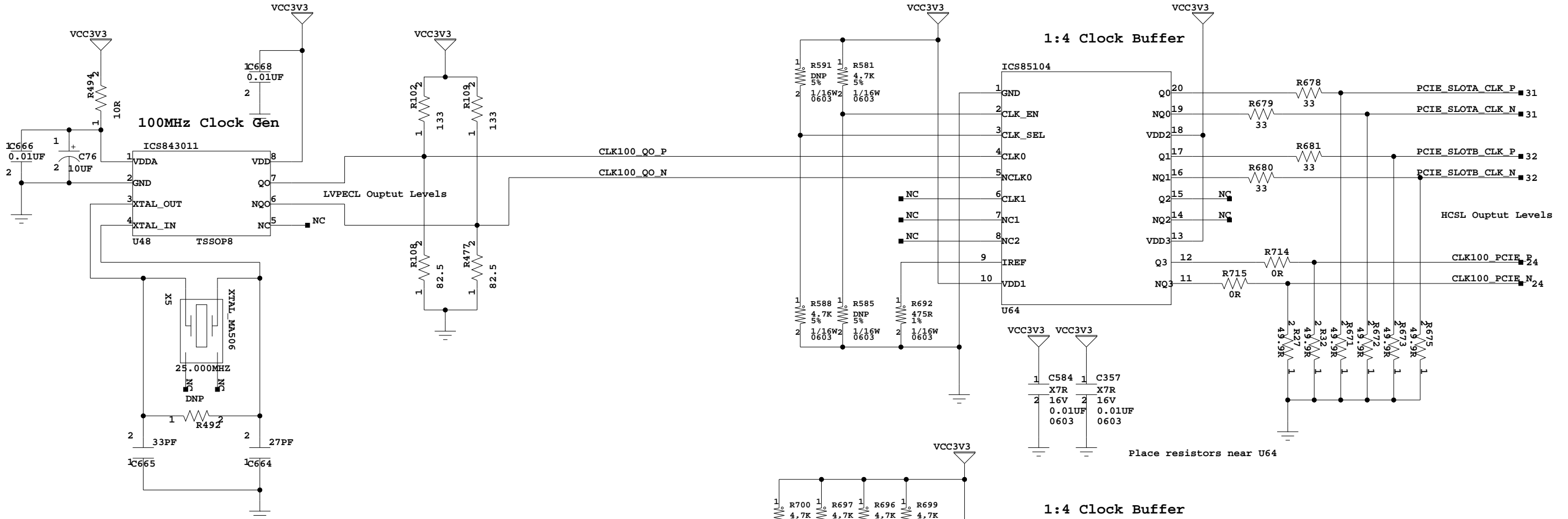
SATA, SGMII CLOCKS



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
SATA, SGMII CLOCKS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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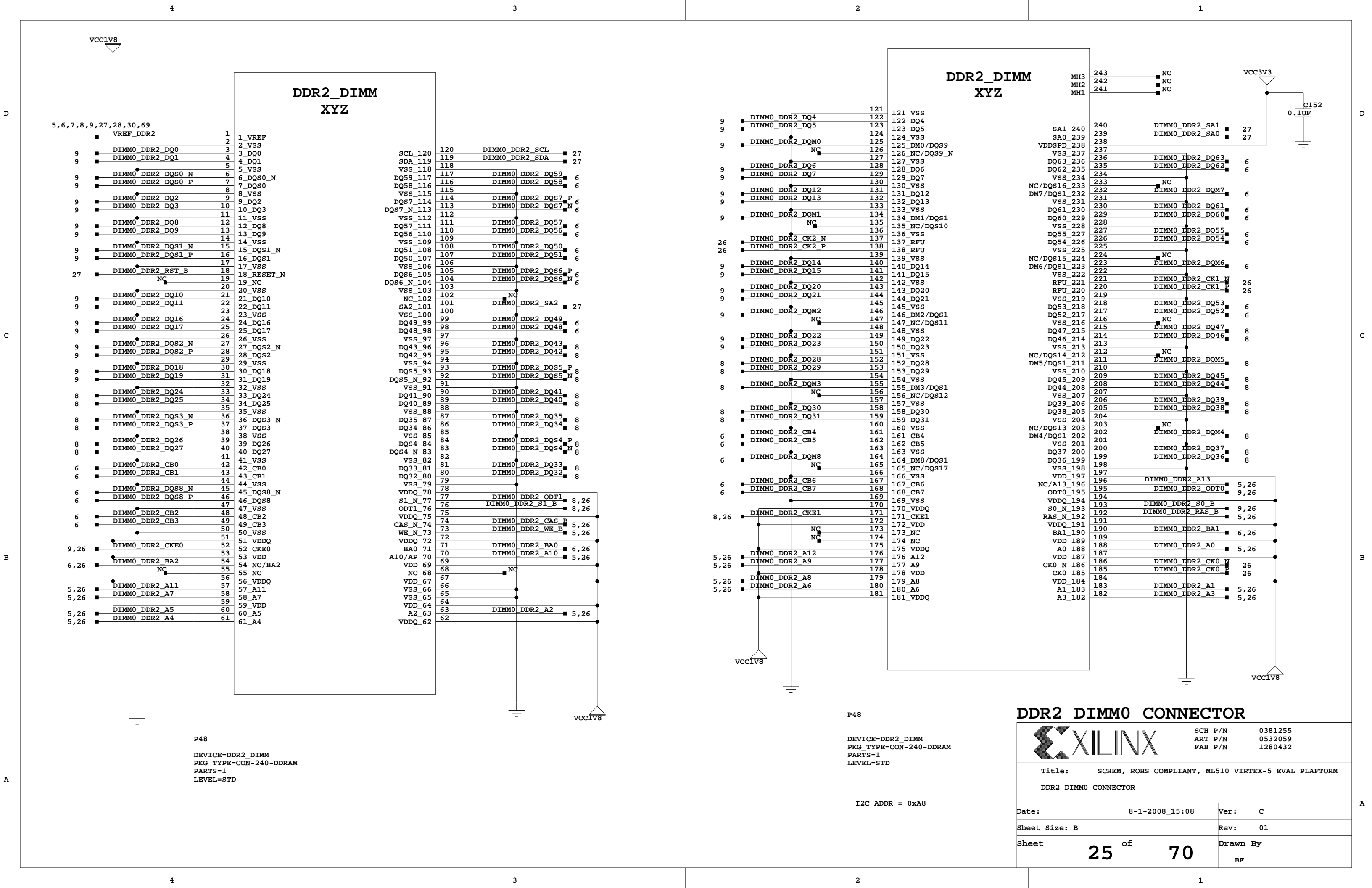


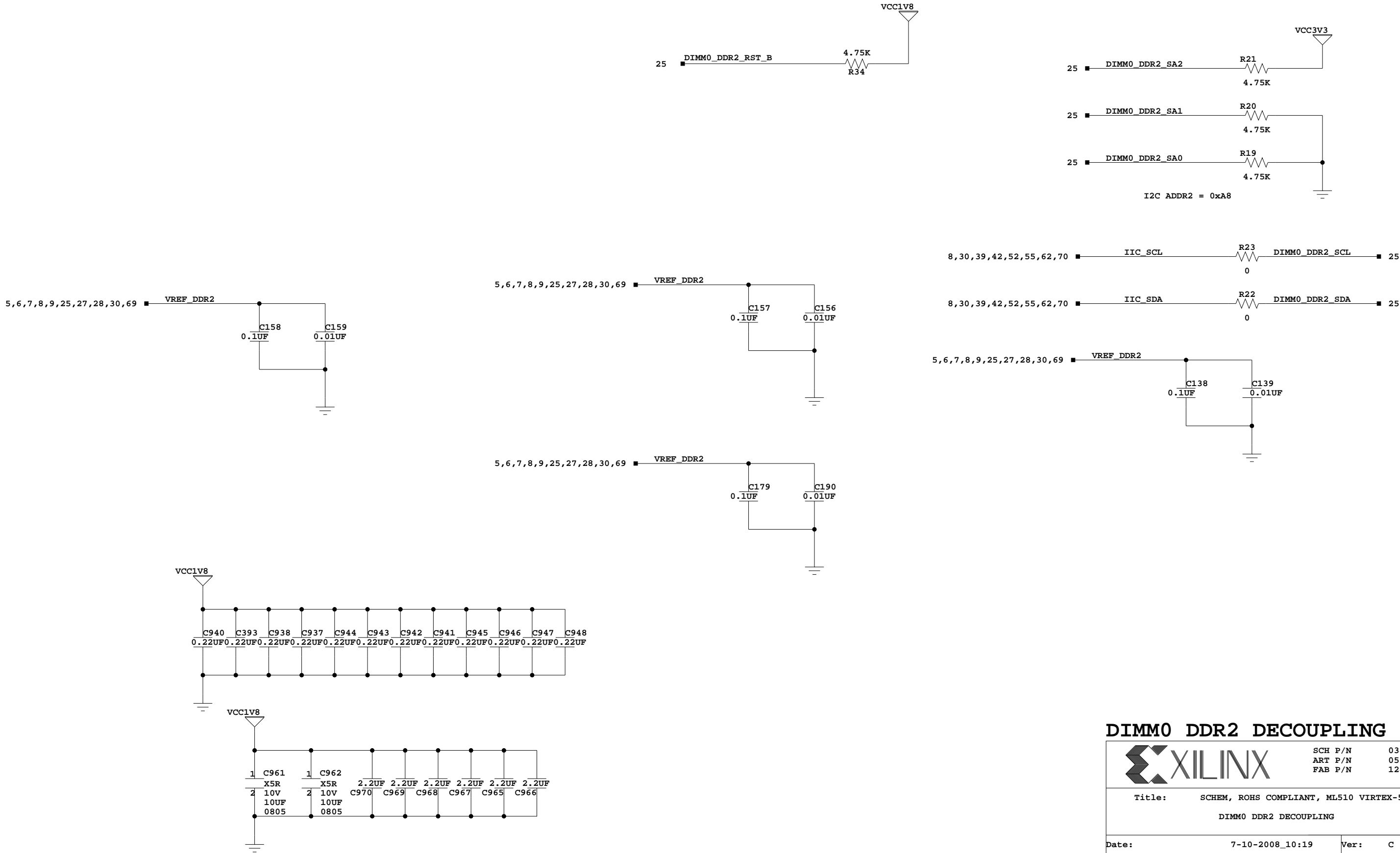
1:4 Clock Buffer

1:4 Clock Buffer

PCie CLOCKS

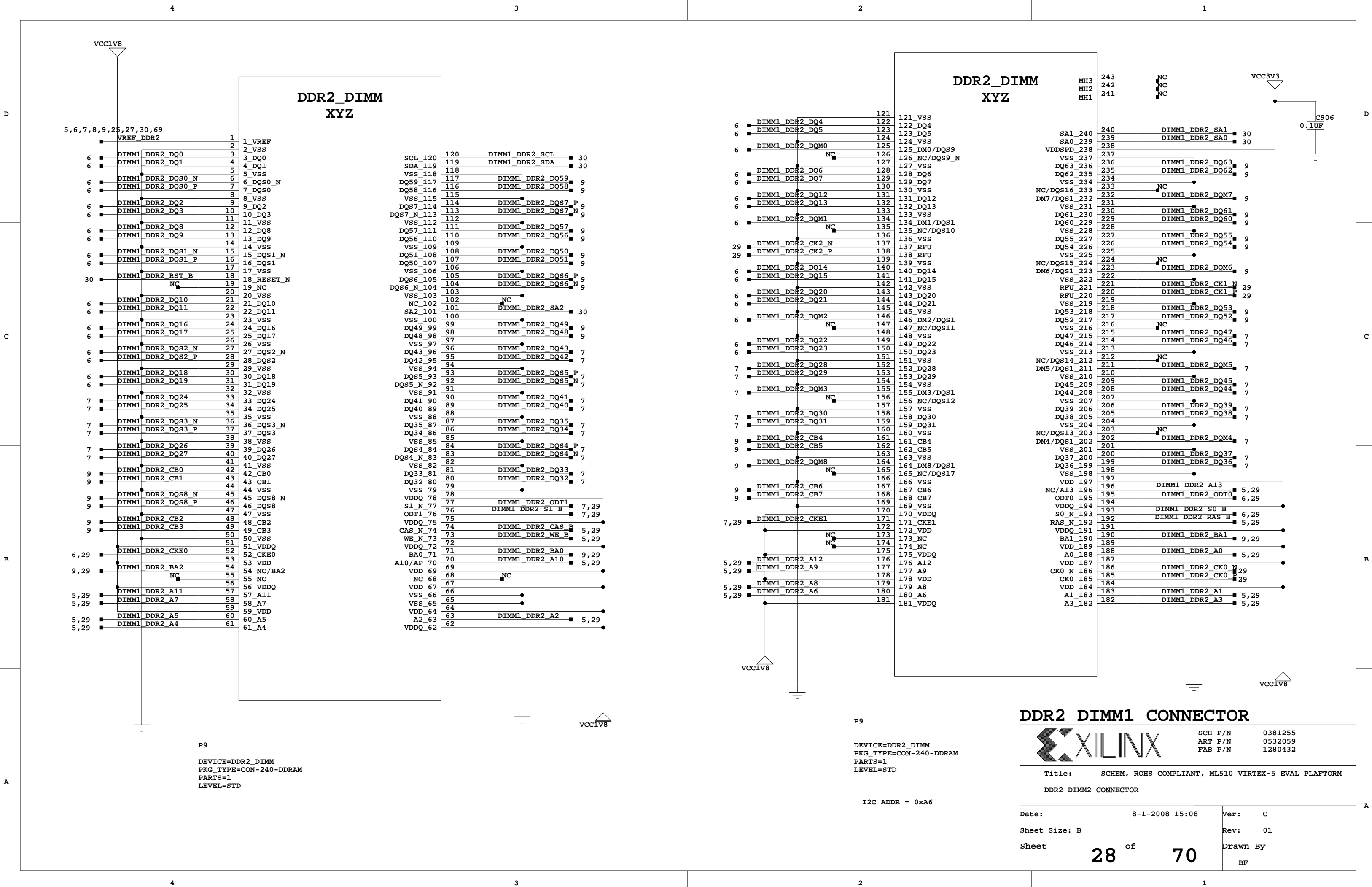
		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM PCIE CLOCKS			
Date: 7-10-2008_10:19		Ver:	C
Sheet Size: B		Rev:	01
Sheet 24 of 70		Drawn By BF	



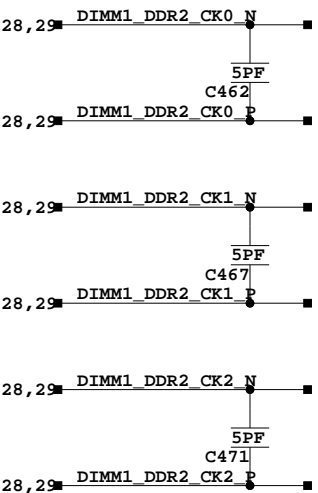
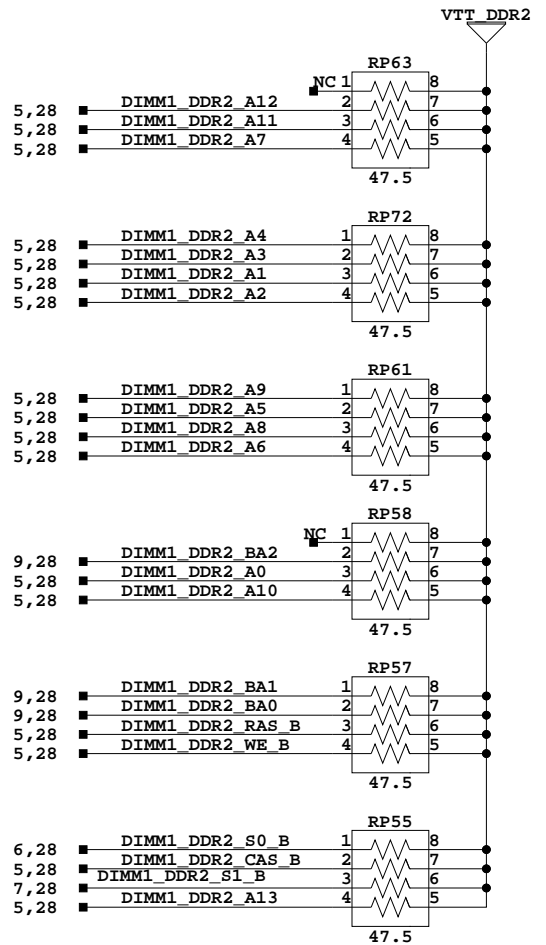
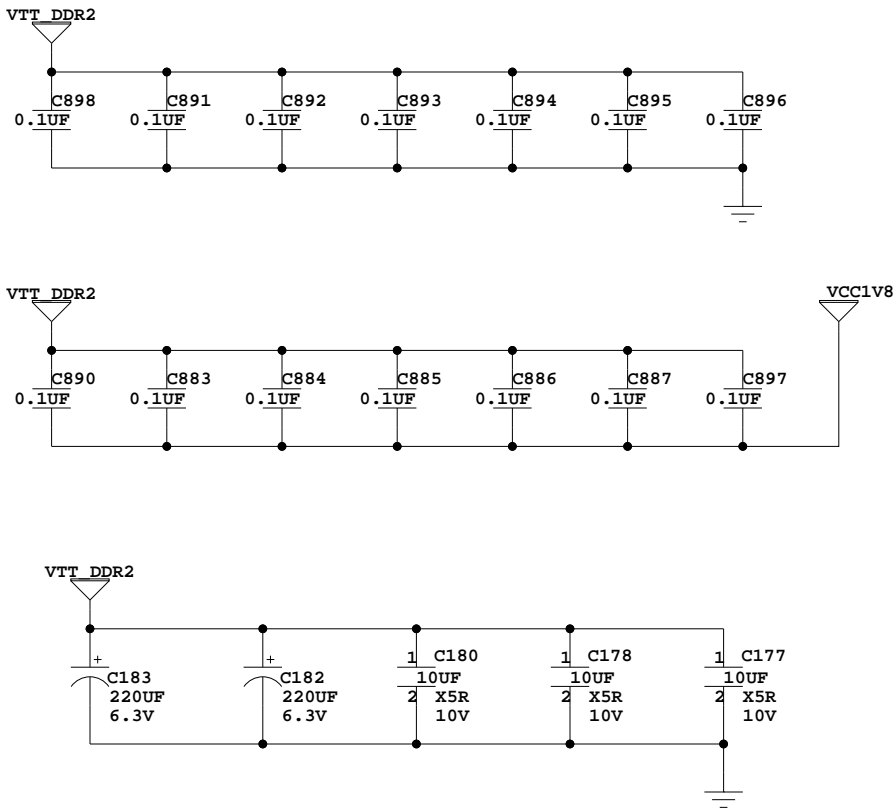


DIMM0 DDR2 DECOUPLING

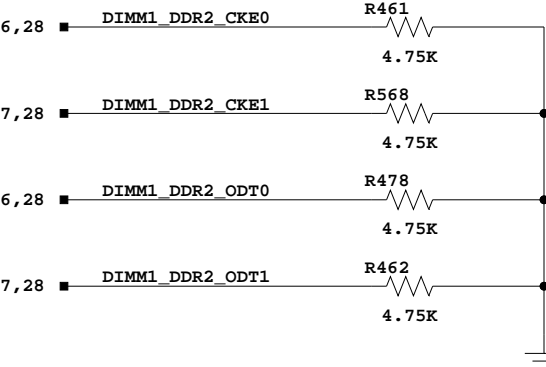
	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
DIMM0 DDR2 DECOUPLING		
Date:	7-10-2008_10:19	Ver: C
Sheet Size: B		Rev: 01
Sheet	27 of 70	Drawn By BF



Since this is a source-sink power supply, split of decoupling capacitors between VTT-GND and VTT-VCC1V8

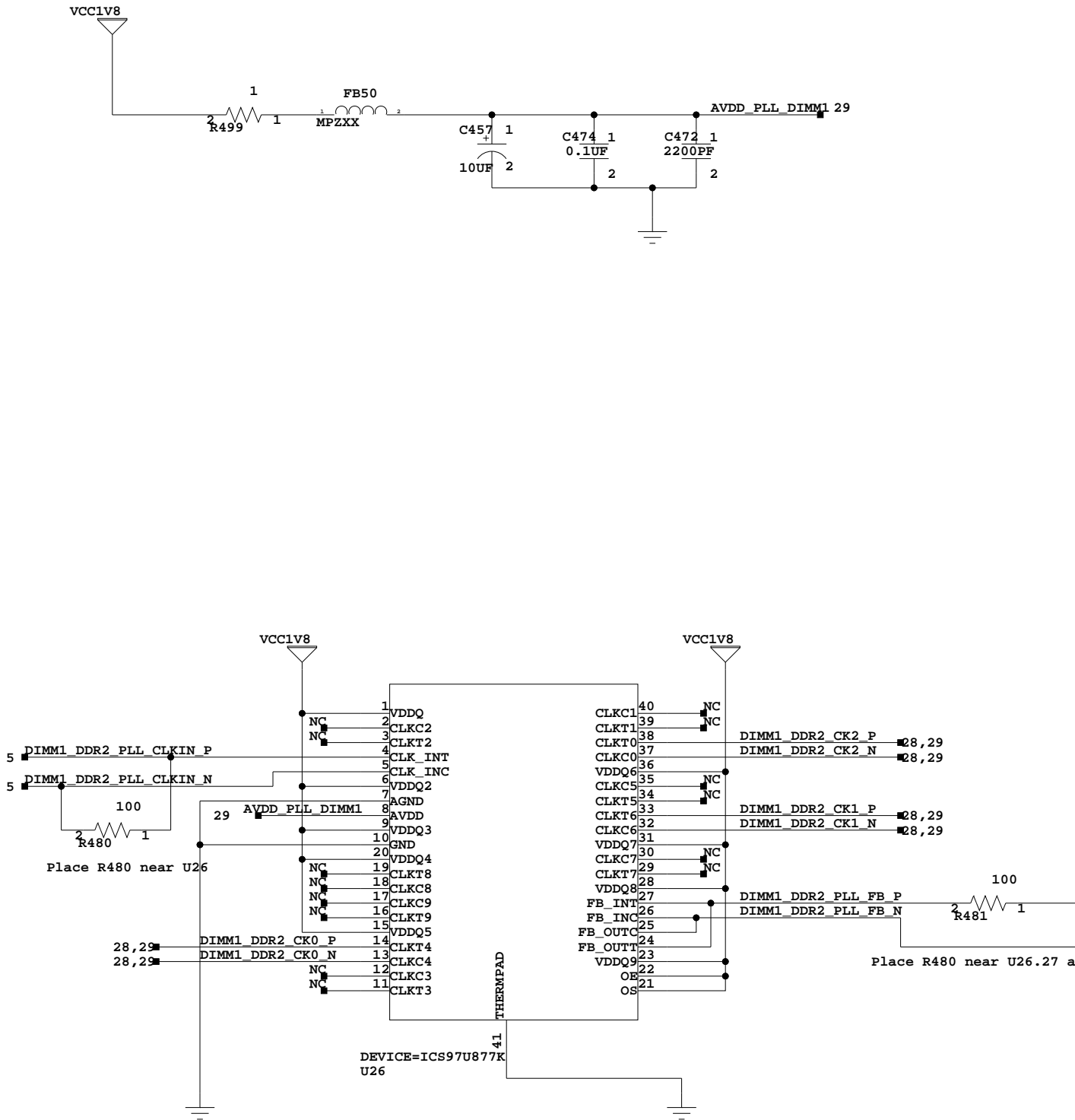


Place these 5pf caps near DDR2 DIMM1

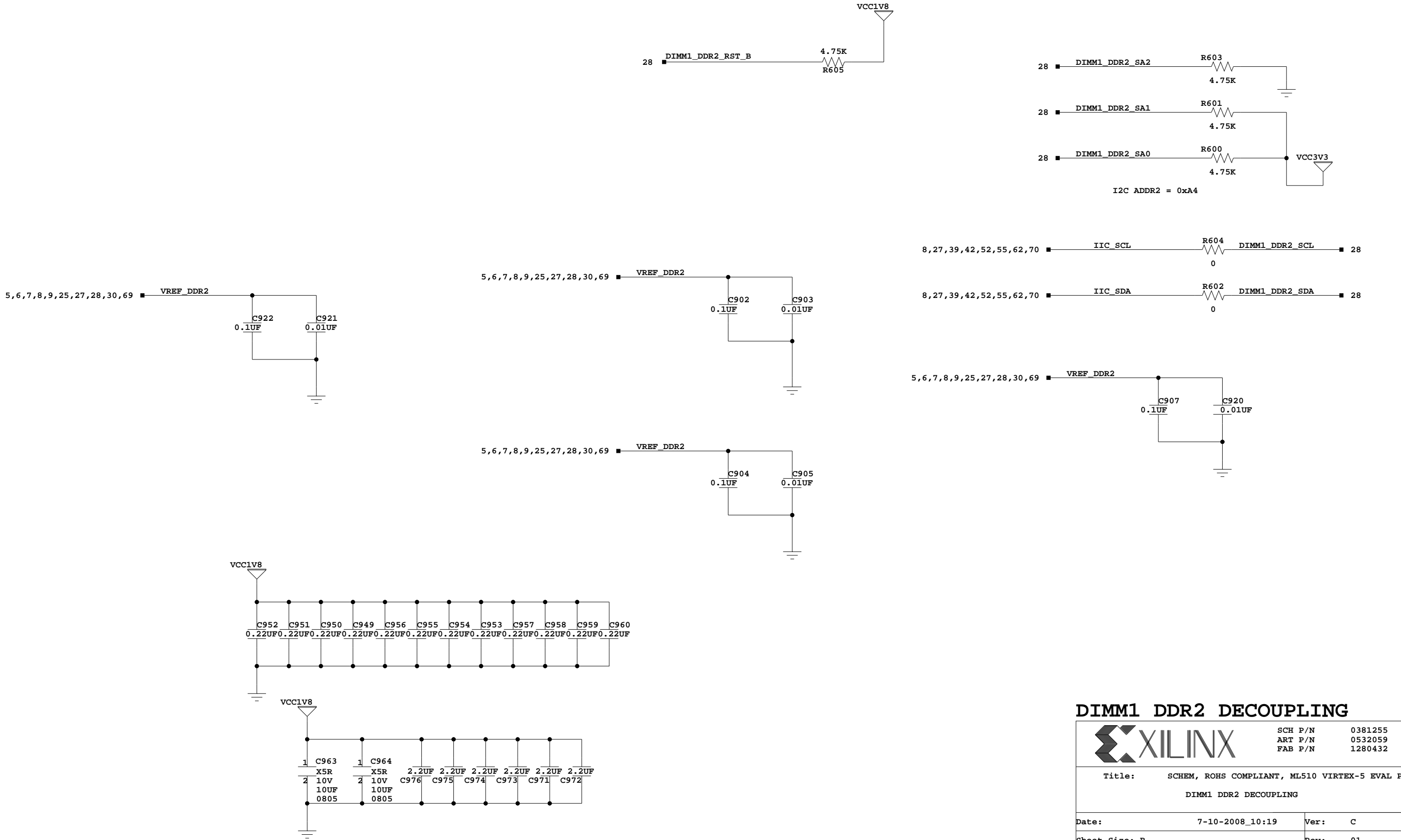


DIMM1_DDR2 SSTL-2 TERMINATION

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM DIMM1_DDR2 SSTL-2 TERMINATION			
Date:	7-10-2008_10:19	Ver:	C
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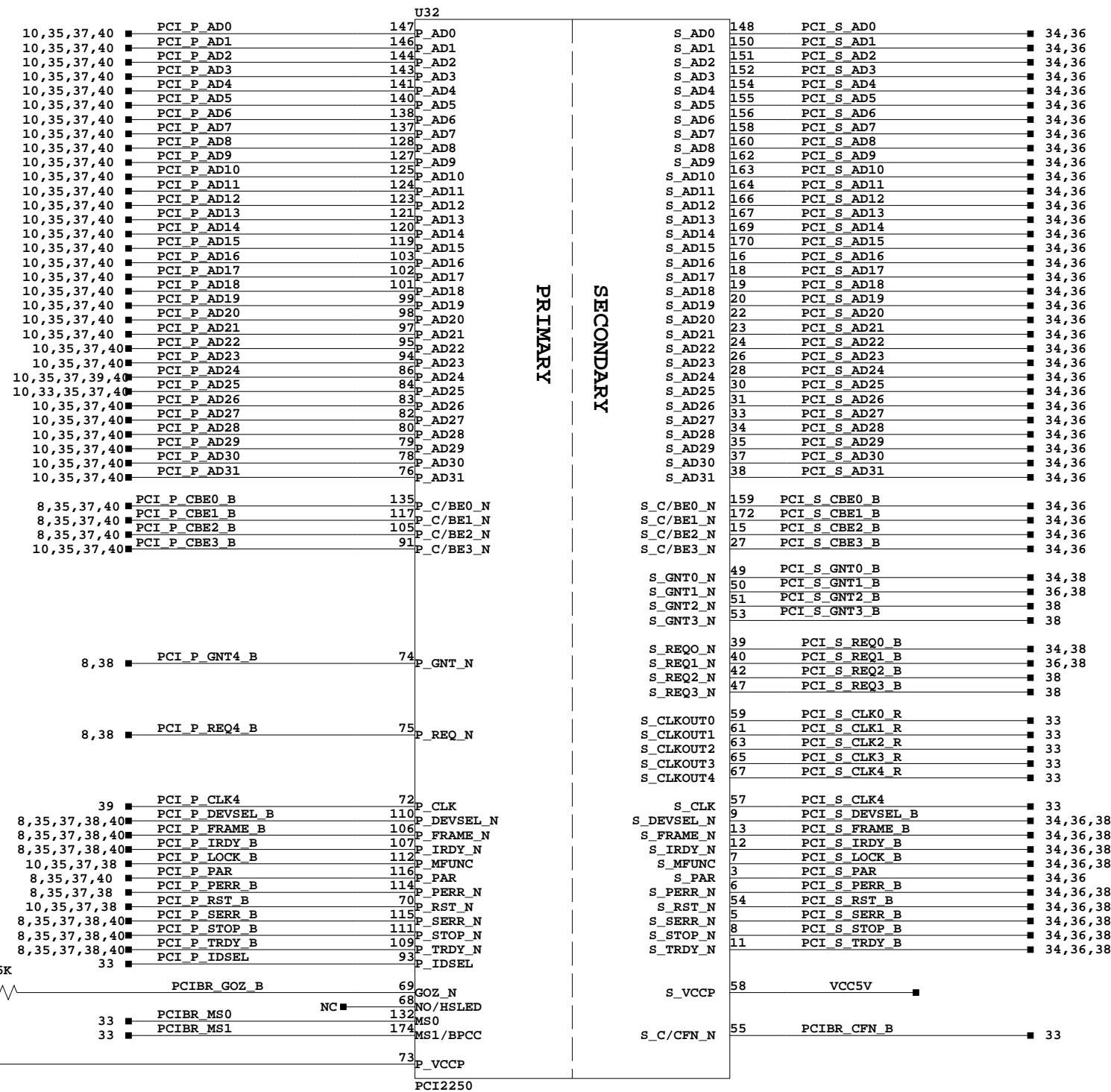
DIMM1_DDR2_PLL_FB* to be length matched to DIMM0_DDR2_CLKIN_*



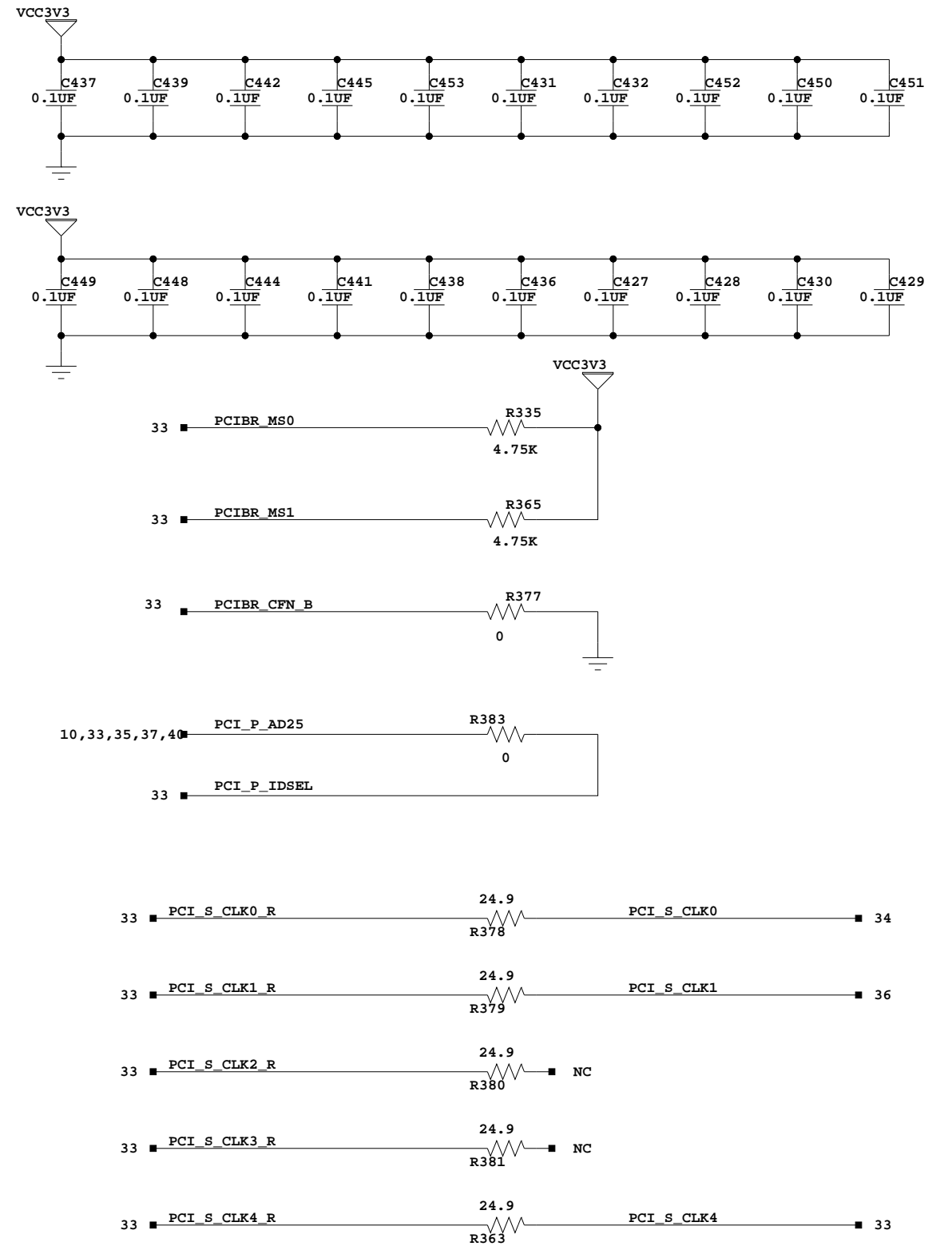
DIMM1 DDR2 DECOUPLING

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
DIMM1 DDR2 DECOUPLING			
Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
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```
PCI-PCI BRIDGE
PCI2250_PGF
```



VCC3V3:10,17,25,32,44,52,62,66,81,88,100
VCC3V3:108,118,126,139,145,153,161,168,176
GND:1,14,21,29,36,45,56,60,64,71,77,89
GND:96,104,113,122,130,133,142,149,157,165,171
NC=2,4,41,43,46,48,85,87,90,92,129,131,134,136,173,175



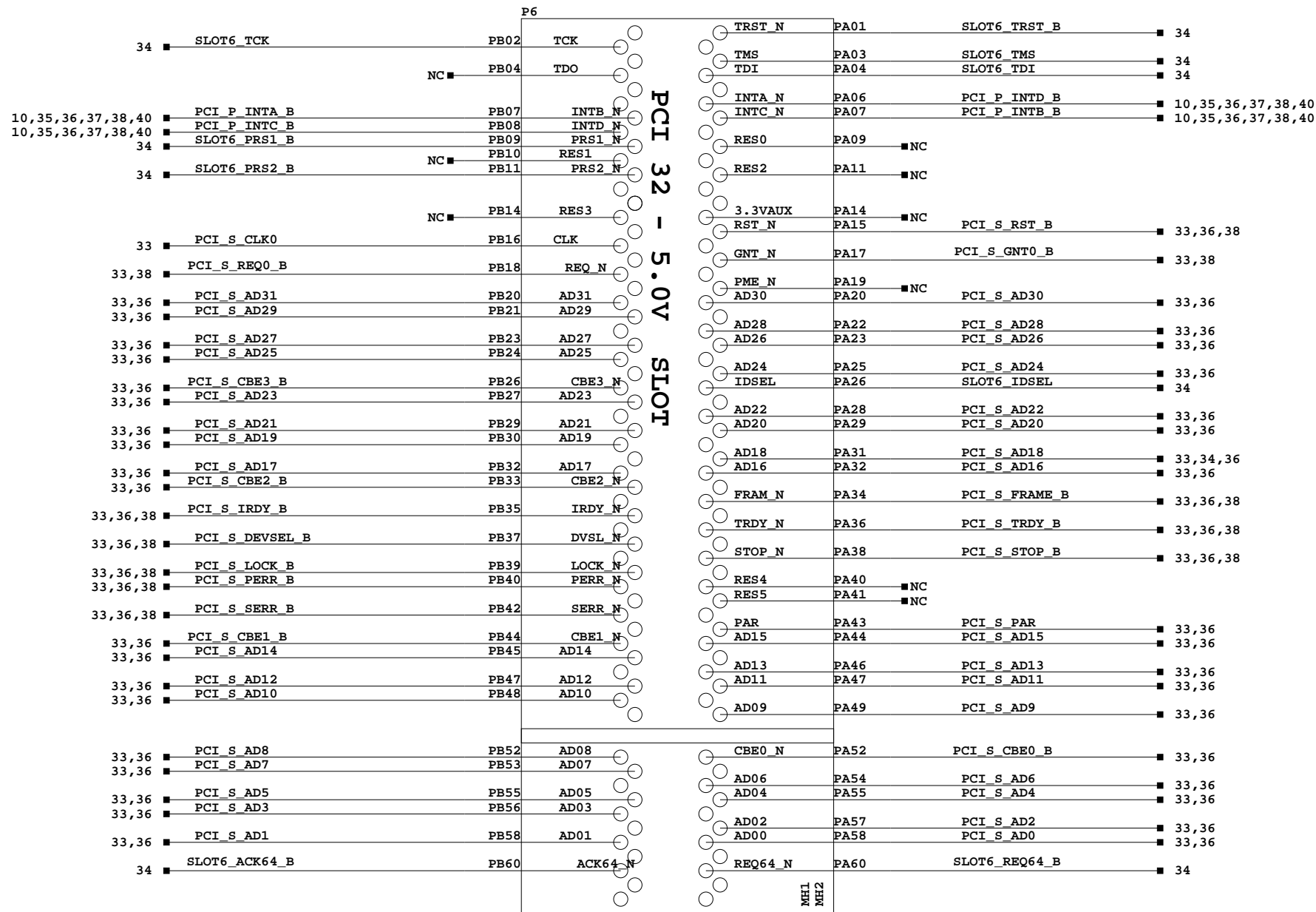
PCI-PCI BRIDGE



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI-PCI BRIDGE

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	33 of 70	Drawn By	BF

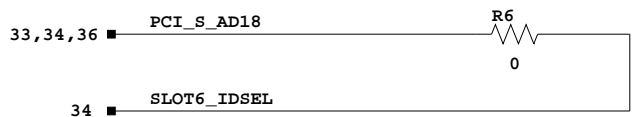
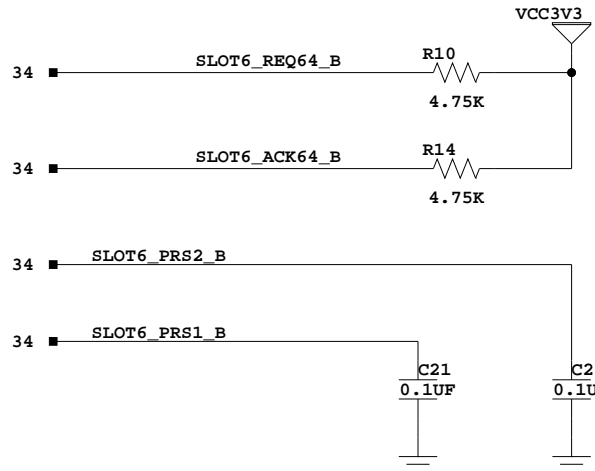
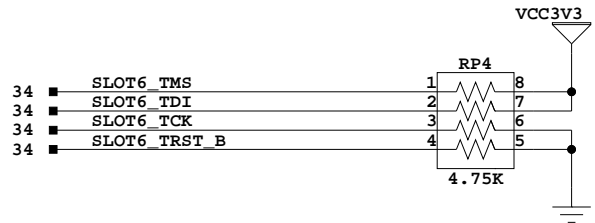
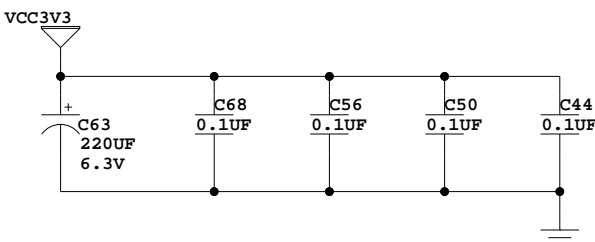
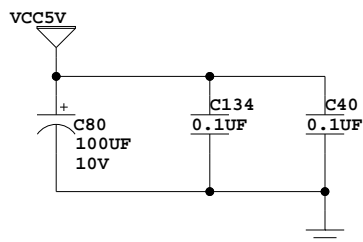
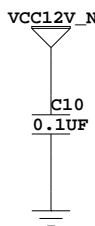
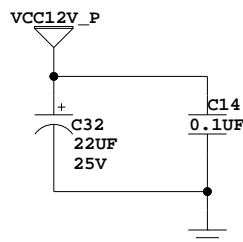


VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08,PA61,PA62,PB61,PB62

VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13



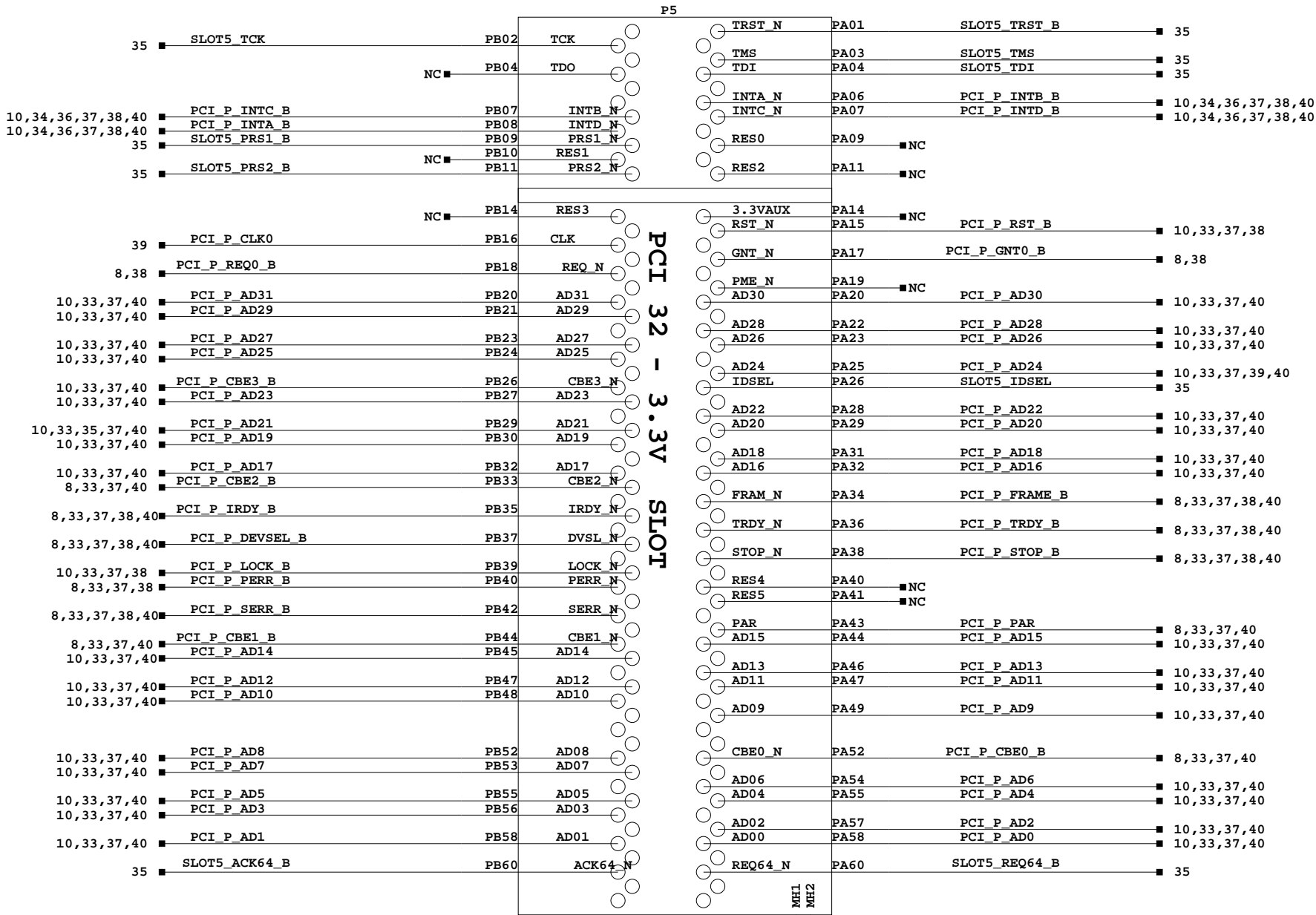
PCI SLOT 6, 5.0V, SECONDARY BUS



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

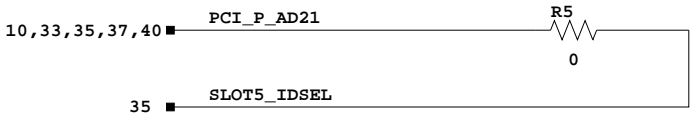
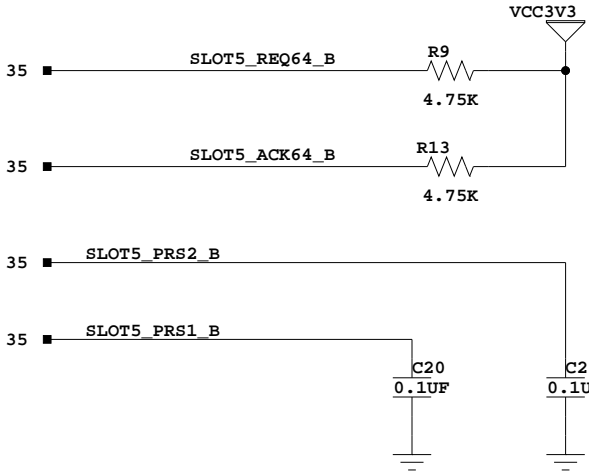
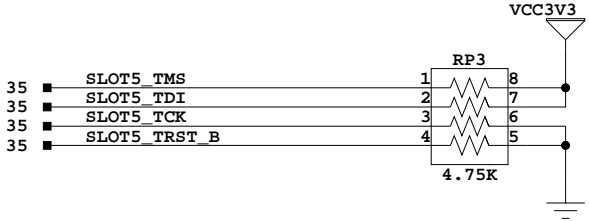
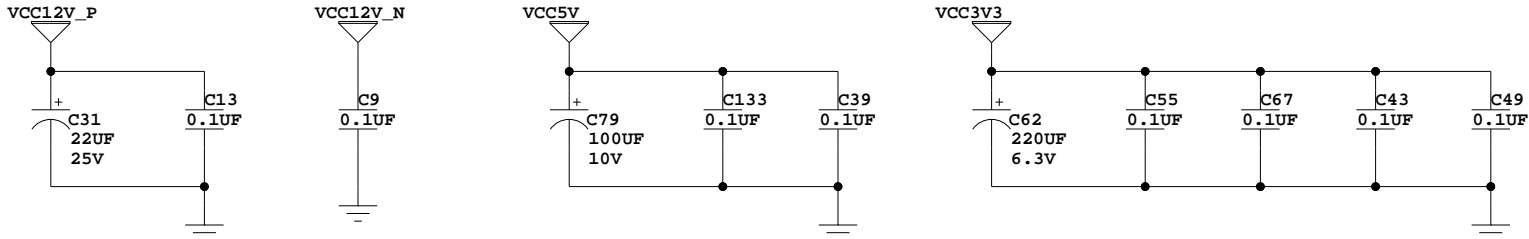
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm
PCI SLOT 6, 5.0V, SECONDARY BUS

Date:	7-10-2008_10:19	Ver:	C
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SIGNAL=GND; PA50, PA51, PB50, PB51

VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54
VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59
GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57



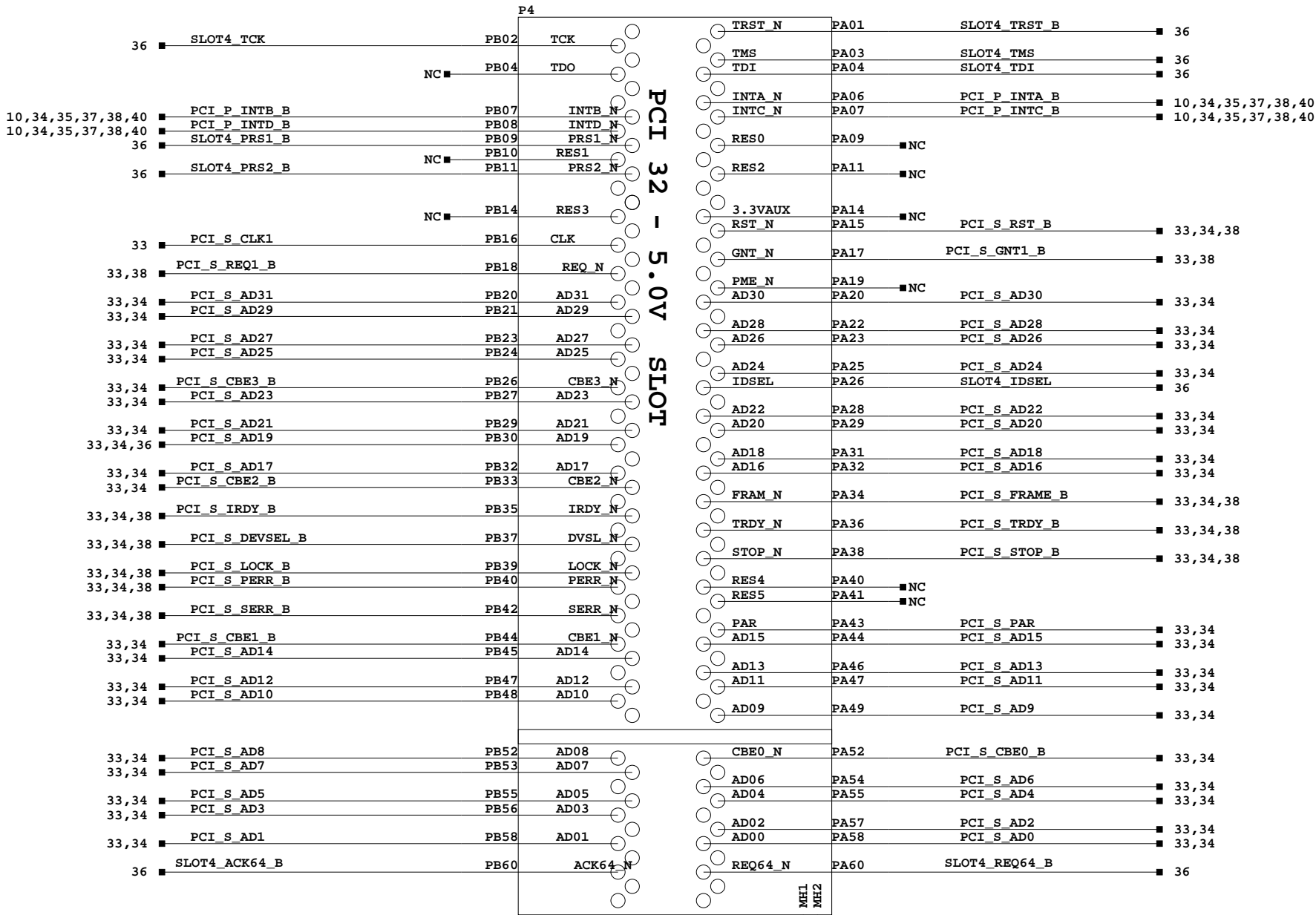
PCI SLOT 5, 3.3V, PRIMARY BUS



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm
PCI SLOT 5, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
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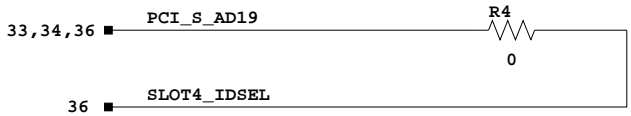
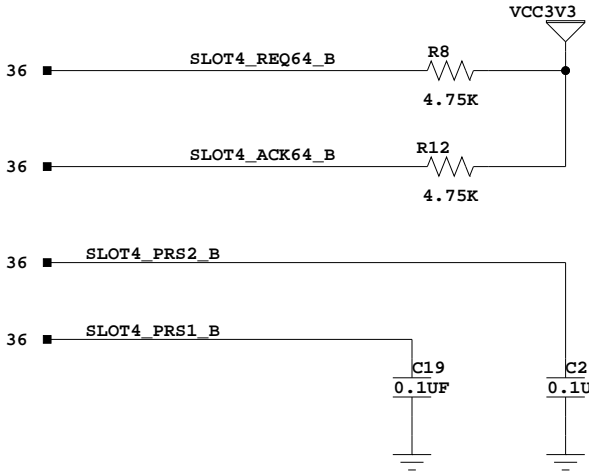
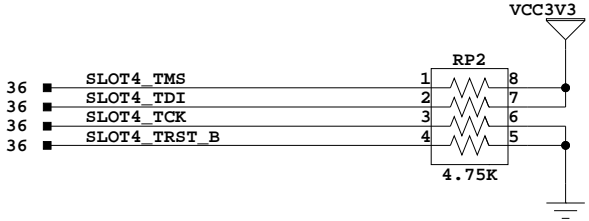
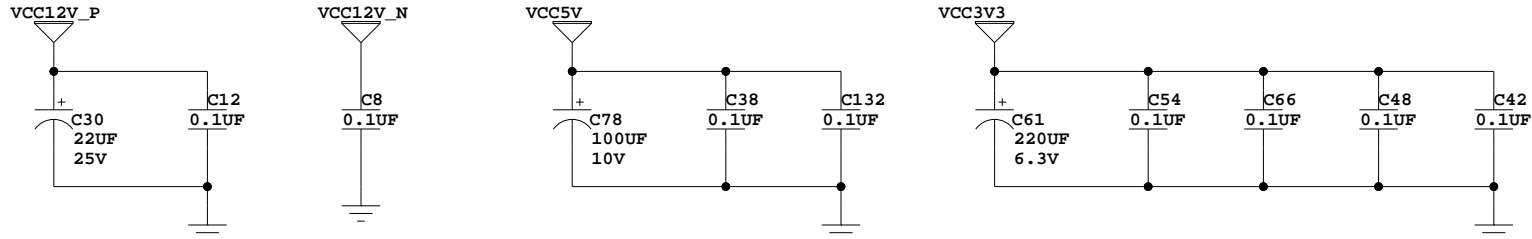


VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08,PA61,PA62,PB61,PB62

VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13



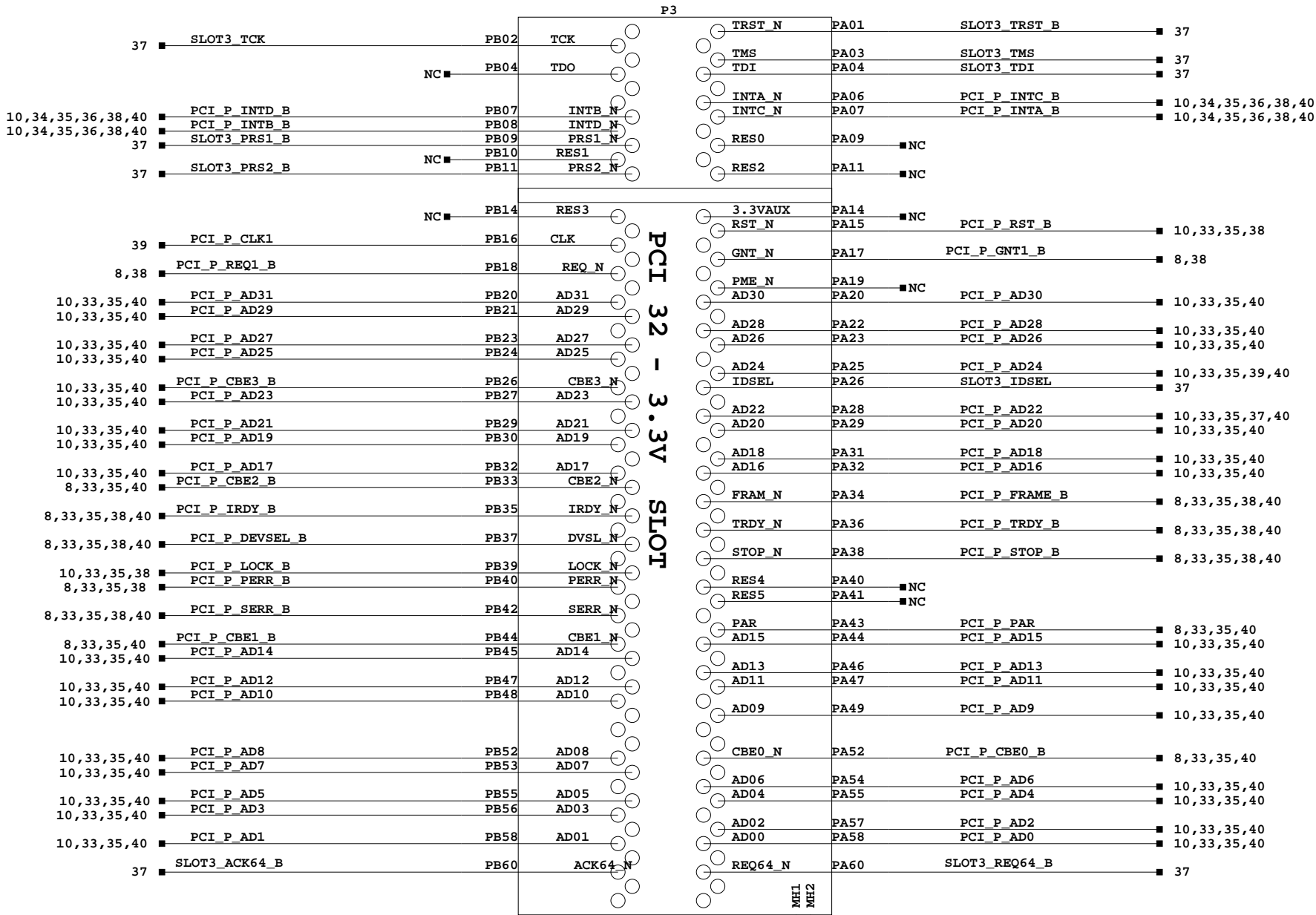
PCI SLOT 4, 5.0V, SECONDARY BUS



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SLOT 4, 5.0V, SECONDARY BUS

Date:	7-10-2008_10:19	Ver:	C
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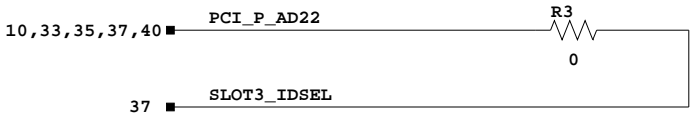
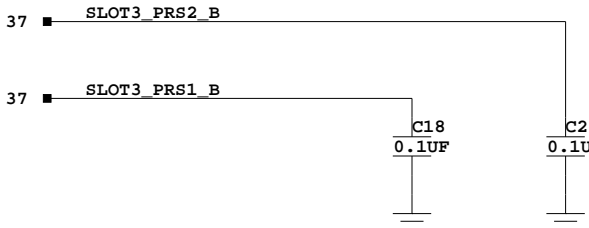
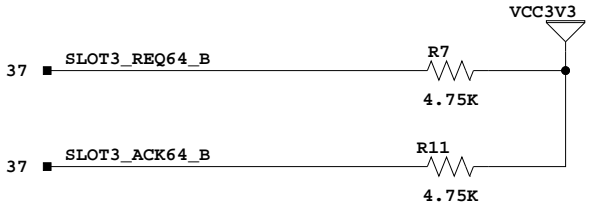
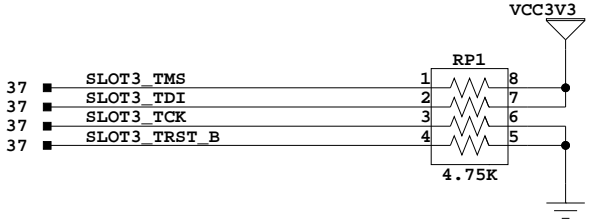
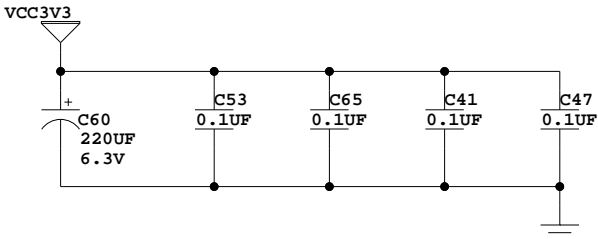
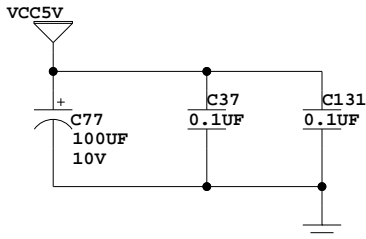
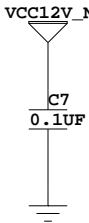
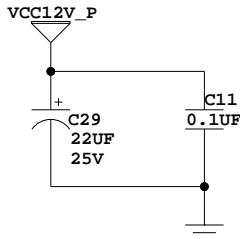


SIGNAL=GND; PA50, PA51, PB50, PB51

VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57



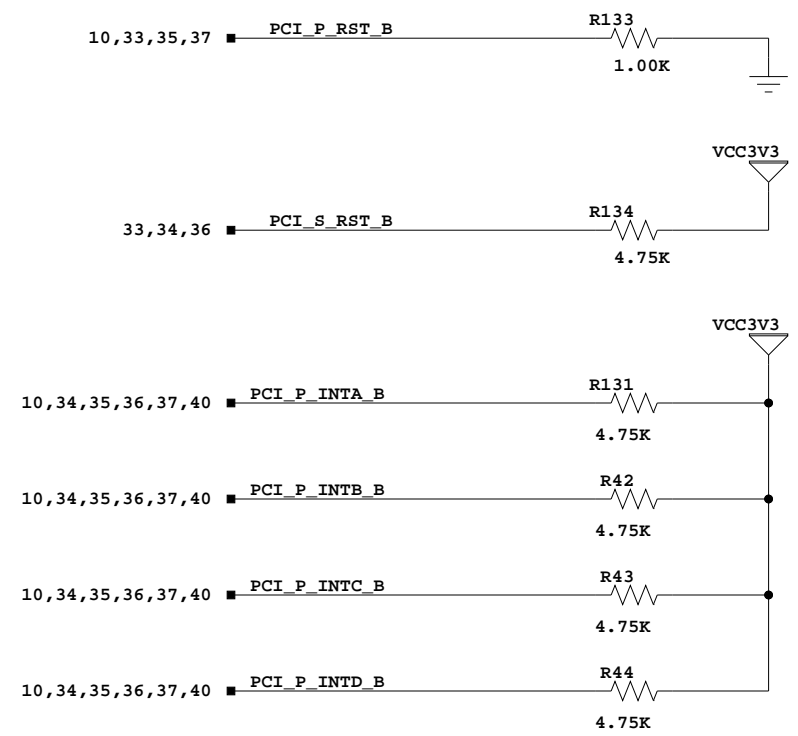
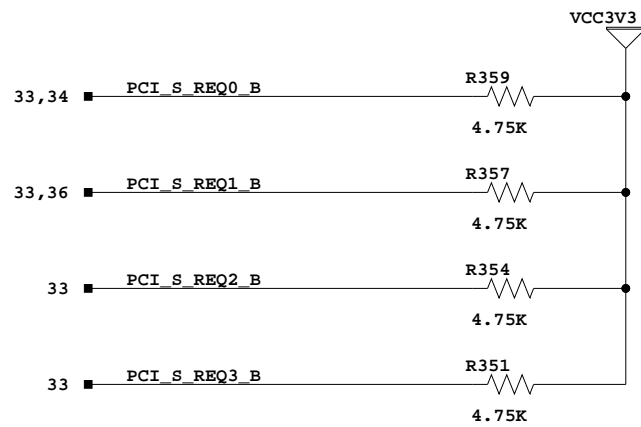
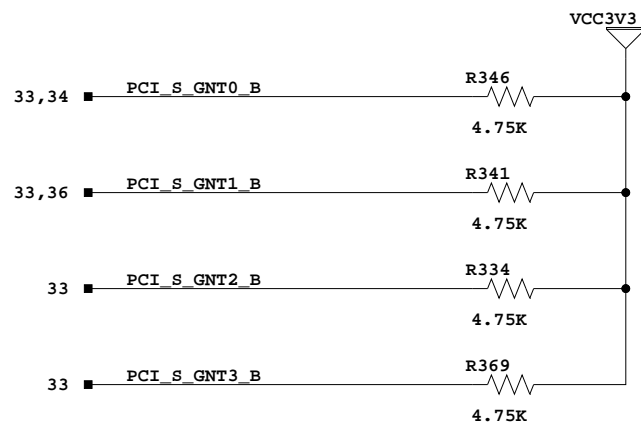
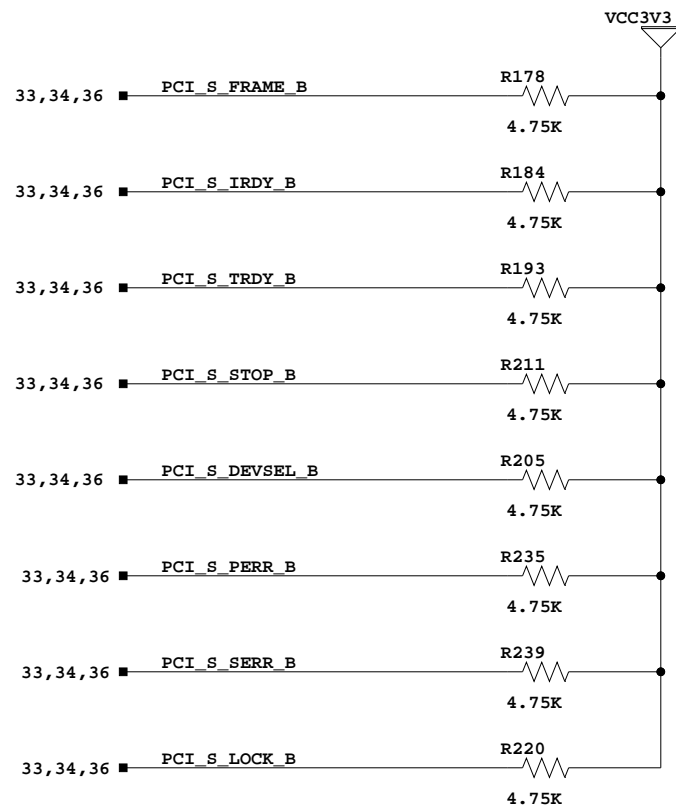
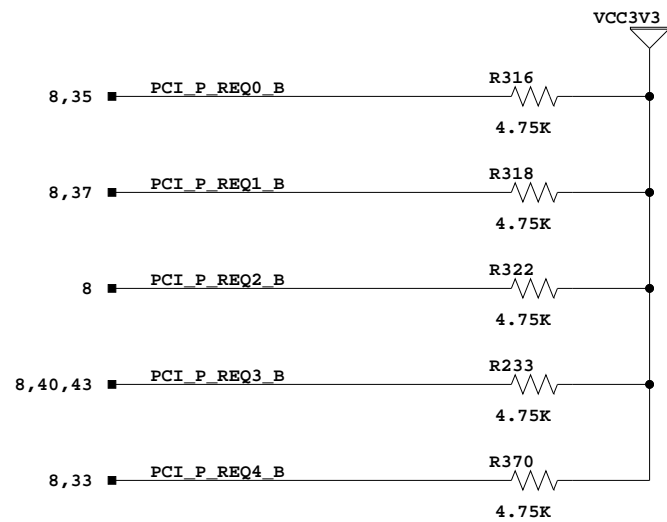
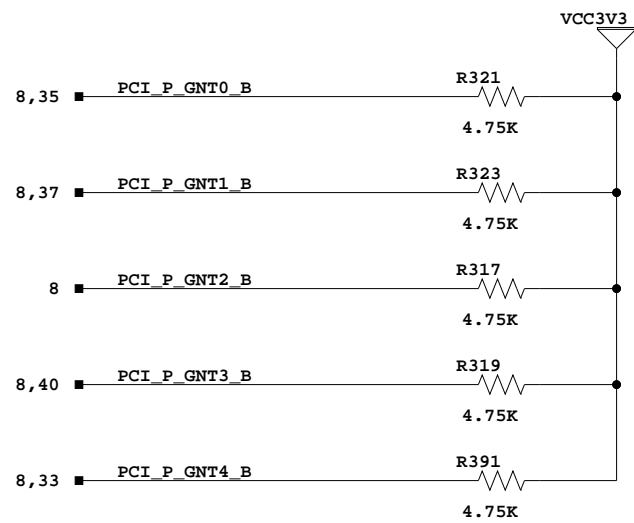
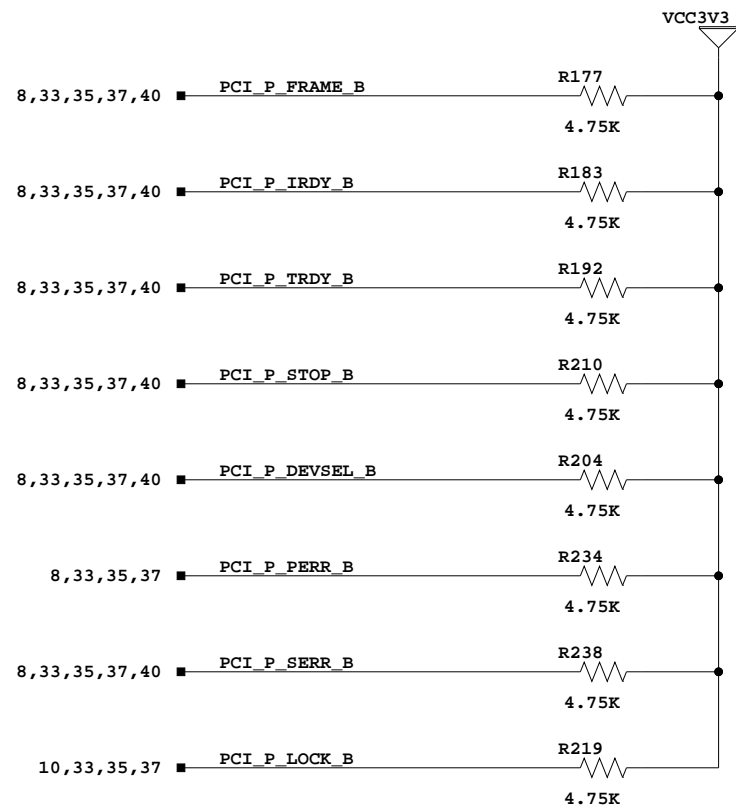
PCI SLOT 3, 3.3V, PRIMARY BUS



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SLOT 3, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
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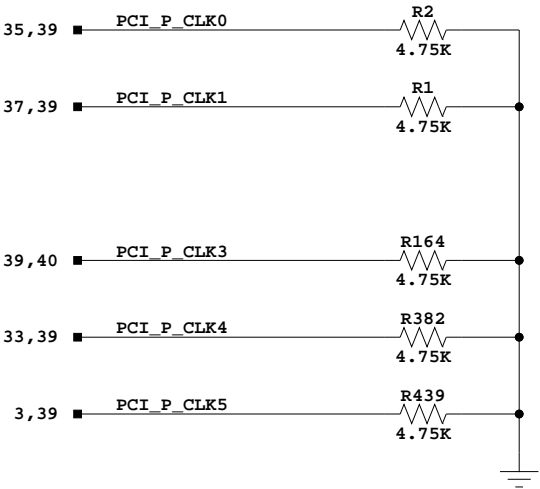
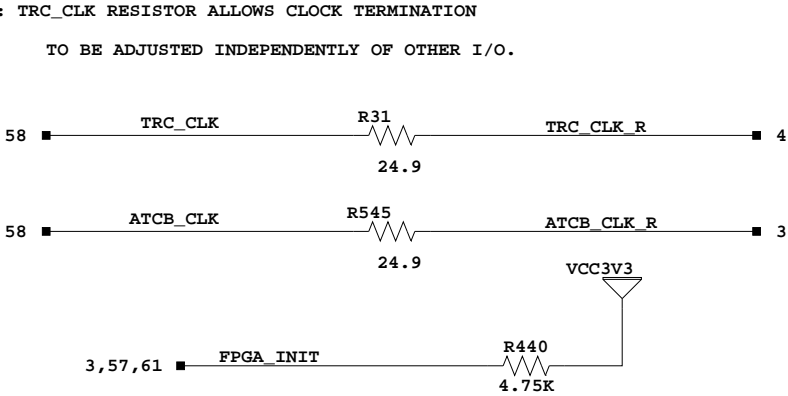
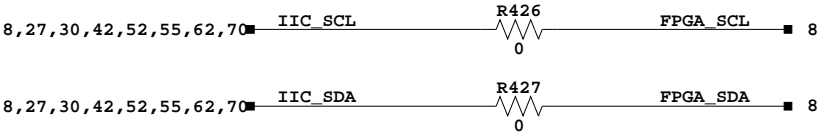
PCI BUS PULLUPS



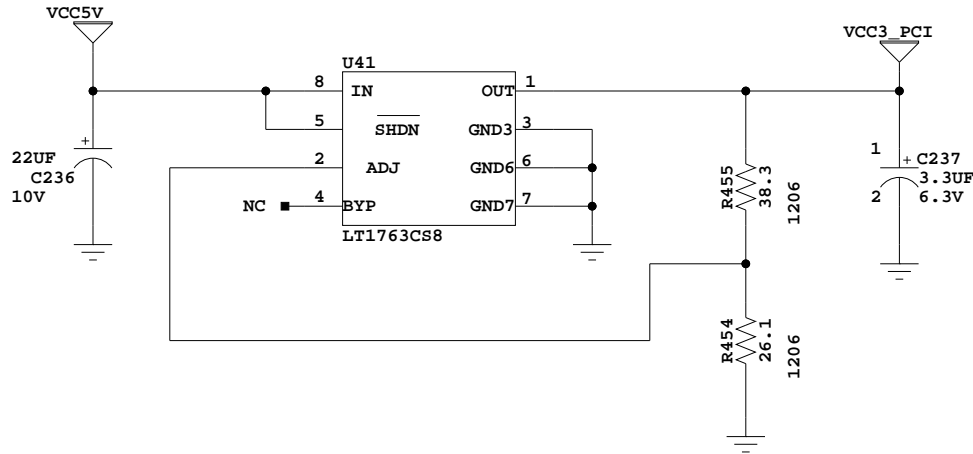
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAAFORM
PCI BUS PULLUPS

Date:	7-10-2008_10:19	Ver:	C
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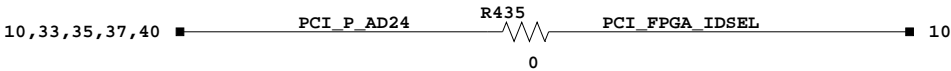
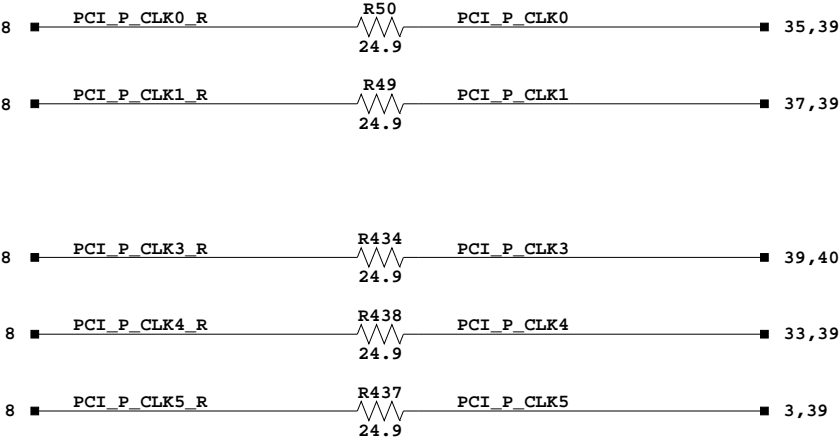


NOTE: THE PCI SPEC RECOMMENDS THAT
CLOCKS BE PULLED LOW WHEN THE
BUS IS NOT ACTIVELY CLOCKED.



NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN
FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT
THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON
THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY
THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.

NOTE: PCI_CLK RESISTORS ALLOW CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



PCI SUPPLY AND TERMINATION

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title:		SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM PCI SUPPLY AND TERMINATION	
Date:	7-10-2008_10:19	Ver:	C
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D

C

B

A

D

C

B

A

4

3

2

1

M1535D+

BGA352-50M
M1535DPLUS
U15

SOUTH BRIDGE 1/5

PCI INTERFACE

10,33,35,37	PCI_P_AD0	A9
10,33,35,37	PCI_P_AD1	B9
10,33,35,37	PCI_P_AD2	C9
10,33,35,37	PCI_P_AD3	A8
10,33,35,37	PCI_P_AD4	B8
10,33,35,37	PCI_P_AD5	C8
10,33,35,37	PCI_P_AD6	D8
10,33,35,37	PCI_P_AD7	A7
10,33,35,37	PCI_P_AD8	C7
10,33,35,37	PCI_P_AD9	D7
10,33,35,37	PCI_P_AD10	E7
10,33,35,37	PCI_P_AD11	A6
10,33,35,37	PCI_P_AD12	B6
10,33,35,37	PCI_P_AD13	C6
10,33,35,37	PCI_P_AD14	D6
10,33,35,37	PCI_P_AD15	E6
10,33,35,37	PCI_P_AD16	A2
10,33,35,37	PCI_P_AD17	B2
10,33,35,37	PCI_P_AD18	C2
10,33,35,37	PCI_P_AD19	D2
10,33,35,37	PCI_P_AD20	A1
10,33,35,37	PCI_P_AD21	B1
10,33,35,37	PCI_P_AD22	C1
10,33,35,37	PCI_P_AD23	D3
10,33,35,37,39	PCI_P_AD24	D1
10,33,35,37	PCI_P_AD25	E3
10,33,35,37	PCI_P_AD26	E2
10,33,35,37	PCI_P_AD27	E1
10,33,35,37	PCI_P_AD28	F3
10,33,35,37	PCI_P_AD29	F2
10,33,35,37	PCI_P_AD30	F1
10,33,35,37	PCI_P_AD31	G2
8,33,35,37	PCI_P_CBE0_B	B7
8,33,35,37	PCI_P_CBE1_B	A5
8,33,35,37	PCI_P_CBE2_B	B3
8,33,35,37	PCI_P_CBE3_B	D2

43	UNUSED_PU33V_1	B11
39	PCI_P_CLK3	E8

NC	B10
NC	C5

8,33,35,37,38	PCI_P_FRAME_B	A3
8,33,35,37,38	PCI_P_TRDY_B	C4
8,33,35,37,38	PCI_P_IRDY_B	D4
8,33,35,37,38	PCI_P_STOP_B	A4
8,33,35,37,38	PCI_P_DEVSEL_B	B4
8,33,35,37,38	PCI_P_SERR_B	D5
8,33,35,37,38	PCI_P_PAR	B5

8,38	PCI_P_GNT3_B	A10
8,38,43	PCI_P_REQ3_B	C11

10,34,35,36,37,38	PCI_P_INTA_B	F4
10,34,35,36,37,38	PCI_P_INTB_B	F5
10,34,35,36,37,38	PCI_P_INTC_B	G3
10,34,35,36,37,38	PCI_P_INTD_B	G4
43	UNUSED_INTEJ	G5
43	UNUSED_INTFJ	H4

VCC3V3	F6
	F7
	F14
	P6

AD0	OSC32KI	W6	OSC32K_I	40
AD1	OSC32KII	Y6	OSC32K_II	40
AD2				
AD3	PWG	U10	PWG_RSM_RSTJ	42
AD4				
AD5	OSC14M	D10	OSC14_CLK	40
AD6				
AD7	CLK32KO	V13	CLK32KO	43
AD8				
AD9	USBCLK	H5	USB_CLK	40
AD10				
AD11	INIT	C14	NC	
AD12	CPURST	B13	NC	
AD13	IGNNEJ	C13	NC	
AD14	INTR	B12	SBR_INTR	3,40
AD15	NMI	C12	SBR_NMI	4,40
AD16	A20MJ	A14	NC	
AD17				
AD18	FERRJ	A12	UNUSED_PU33V_4	43
AD19				
AD20				
AD21				
AD22				
AD23				
AD24				
AD25				
AD26				
AD27				
AD28				
AD29				
AD30				
AD31				
CBEJ0_N				
CBEJ1_N				
CBEJ2_N				
CBEJ3_N				
PCI_REQJ				
PCICLK				
PCI_STPJ				
PCIRSTJ				
FRAMEJ				
TRDYJ				
IRDYJ				
STOPJ				
DEVSELJ				
SERRJ				
PAR				
PHLDAJ				
PHOLDJ				
INTAJ_MI				
INTBJ_S0				
INTCJ_S1				
INTDJ_S2				
INTEJ				
INTFJ				
VCC_3C_1				
VCC_3C_2				
VCC_3C_3				
VCC_3C_4				
VCC_G				
VCC5V				
VCC3V3				
VCC3V3				
VCC3V3				

PDMA_REQJ	E4	UNUSED_PU5V_1	43
PDMA_GNTJ	E5	UNUSED_PU5V_2	43

VCC_5A_1	E10
VCC_5A_2	G6
VCC_5A_3	N6
VCC_5A_4	N15
VCC_5A_5	R15

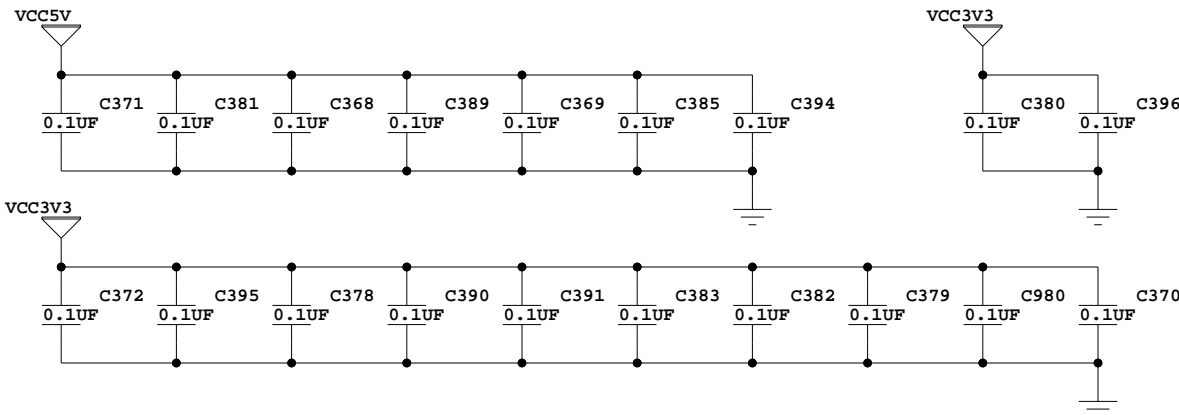
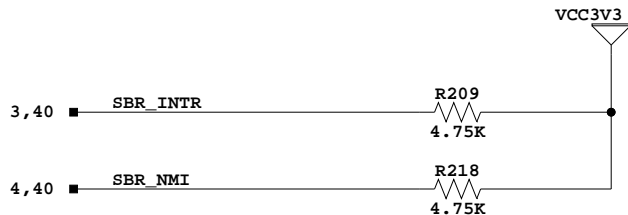
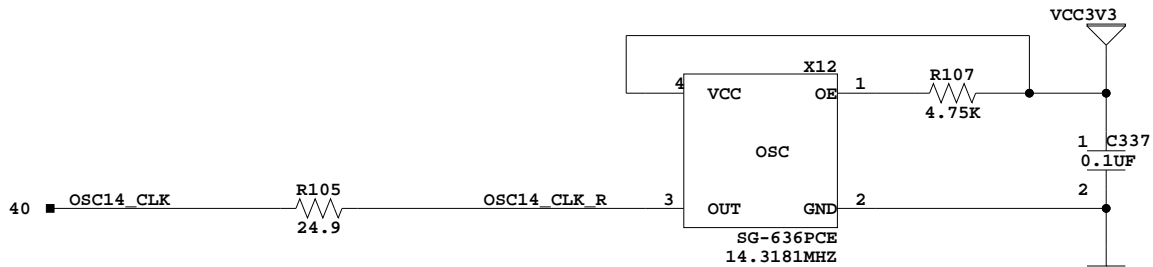
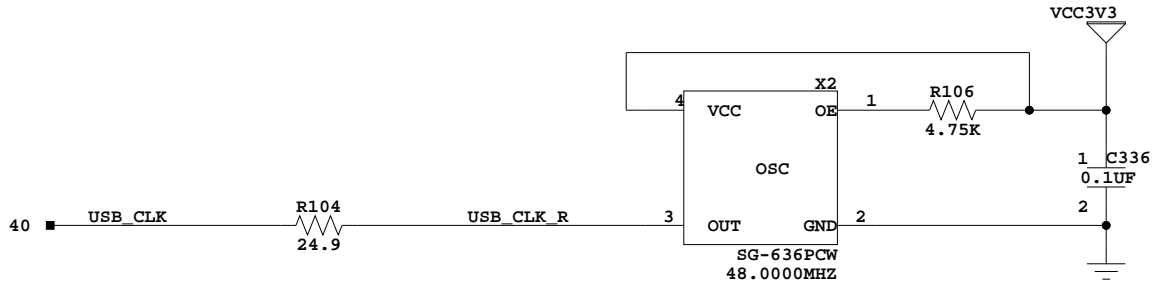
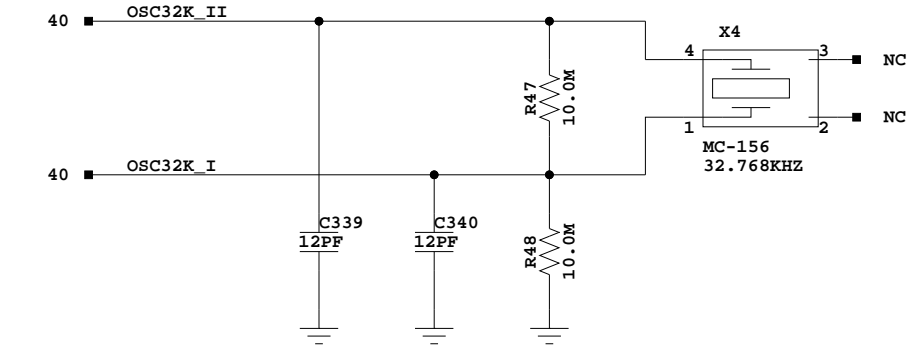
VCCR_5D_1	R7
VCCR_5D_2	R13

VCC_3B	P15
--------	-----

VCCR_3E_1	R6
VCCR_3E_2	R8
VCCR_3E_3	R14

UPSPWR	T10
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VCC_G	F15
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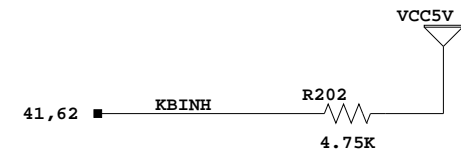
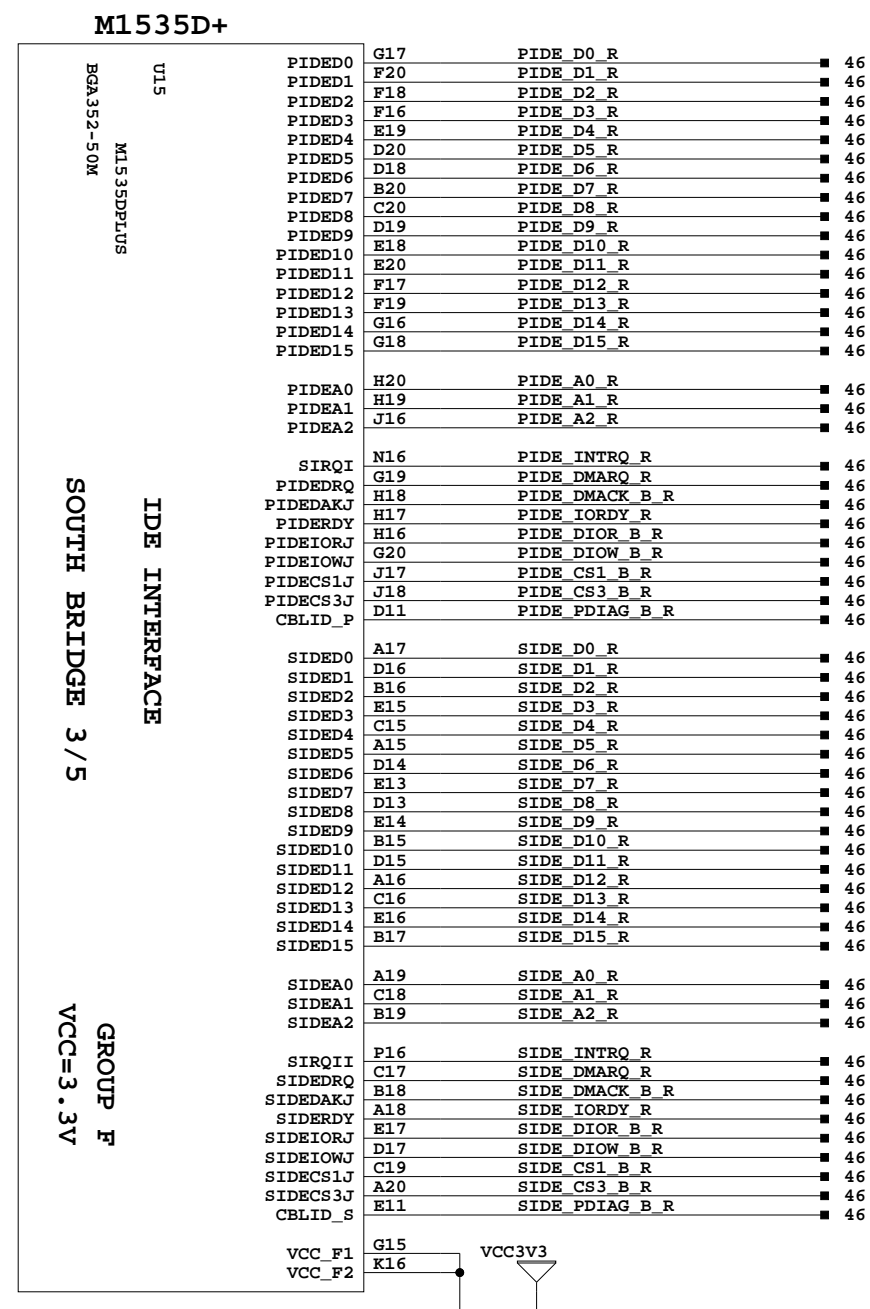
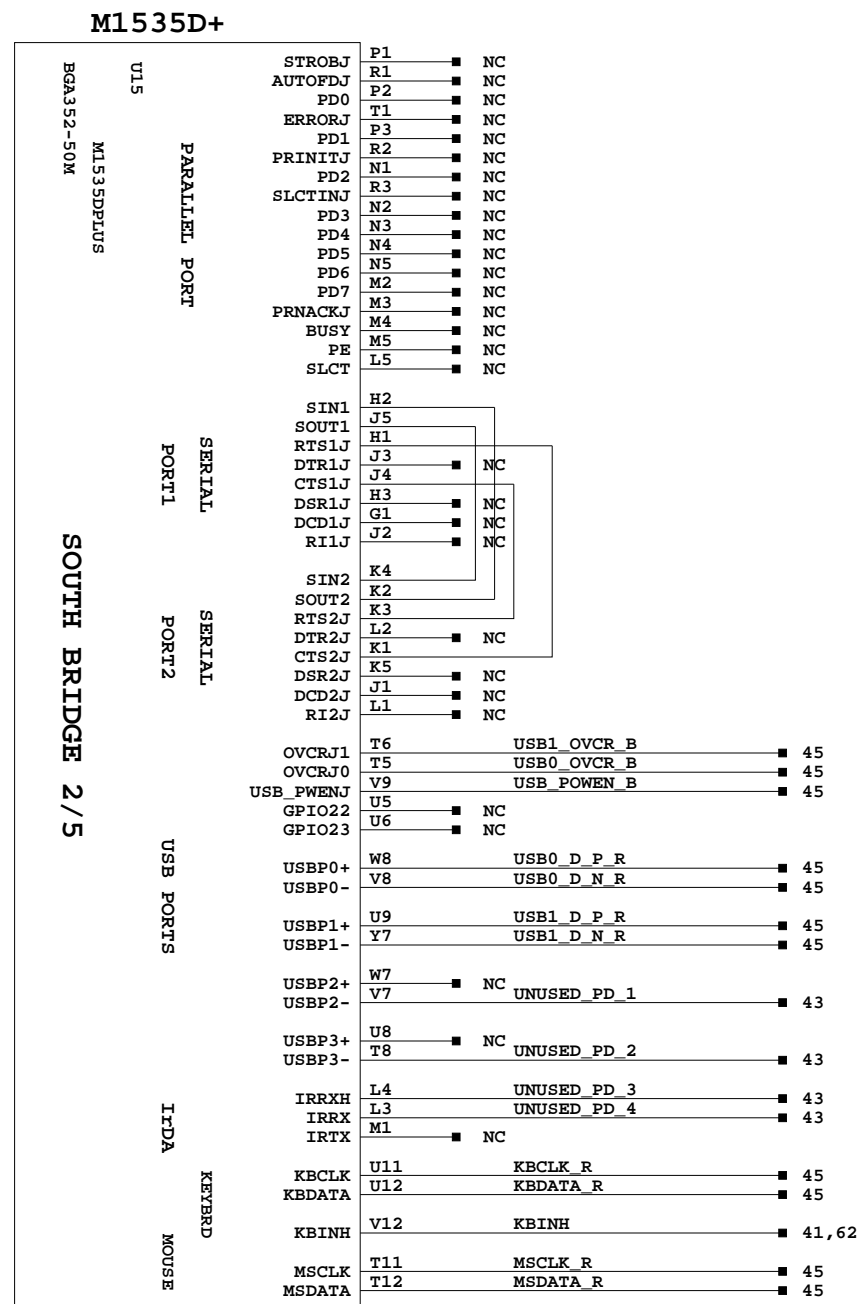
PCI SOUTH BRIDGE, PART 1



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SOUTH BRIDGE, PART 1

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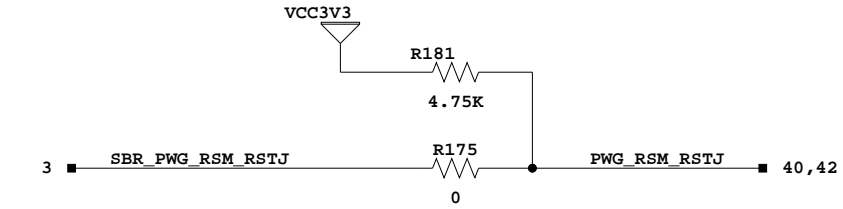
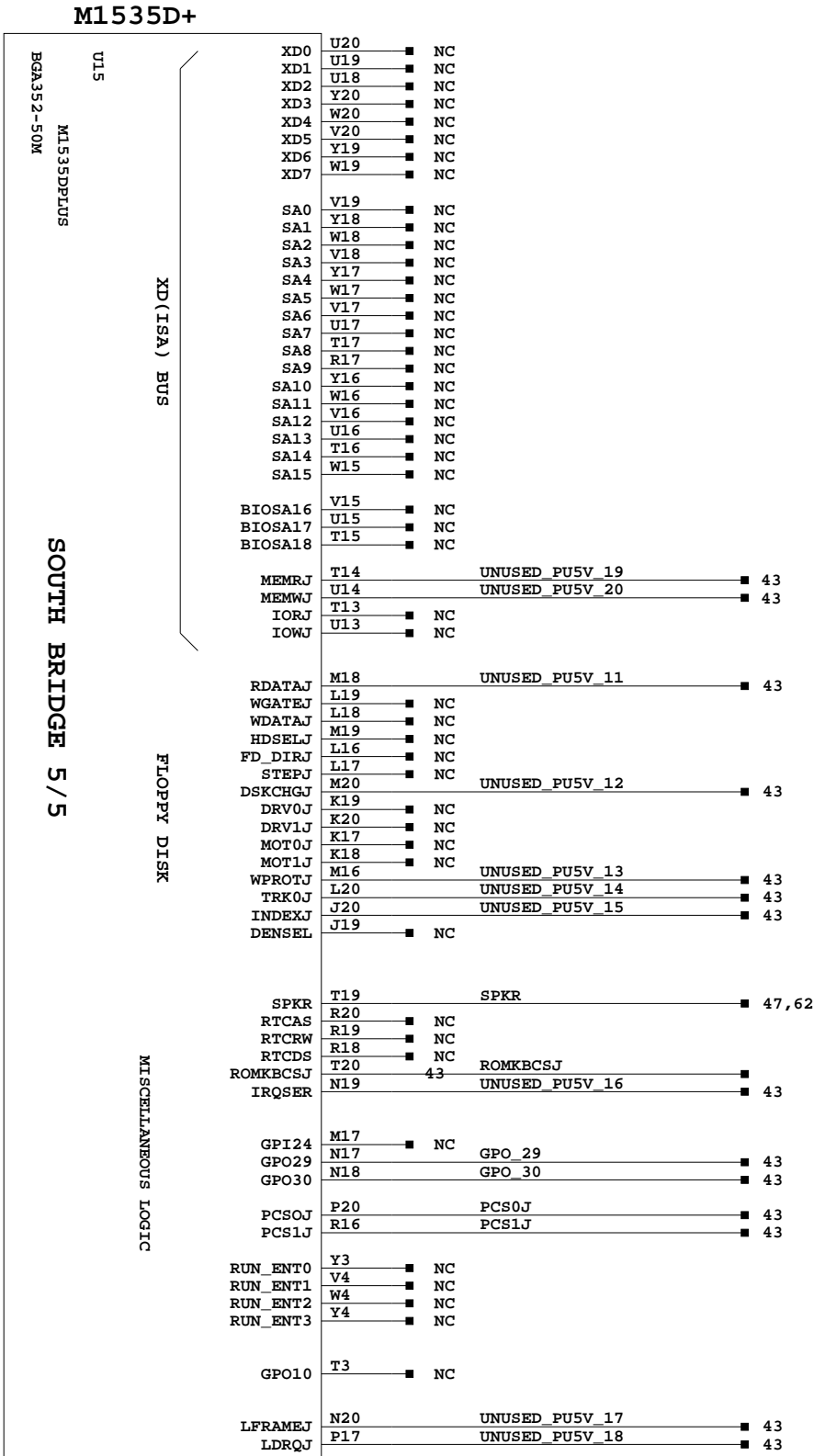
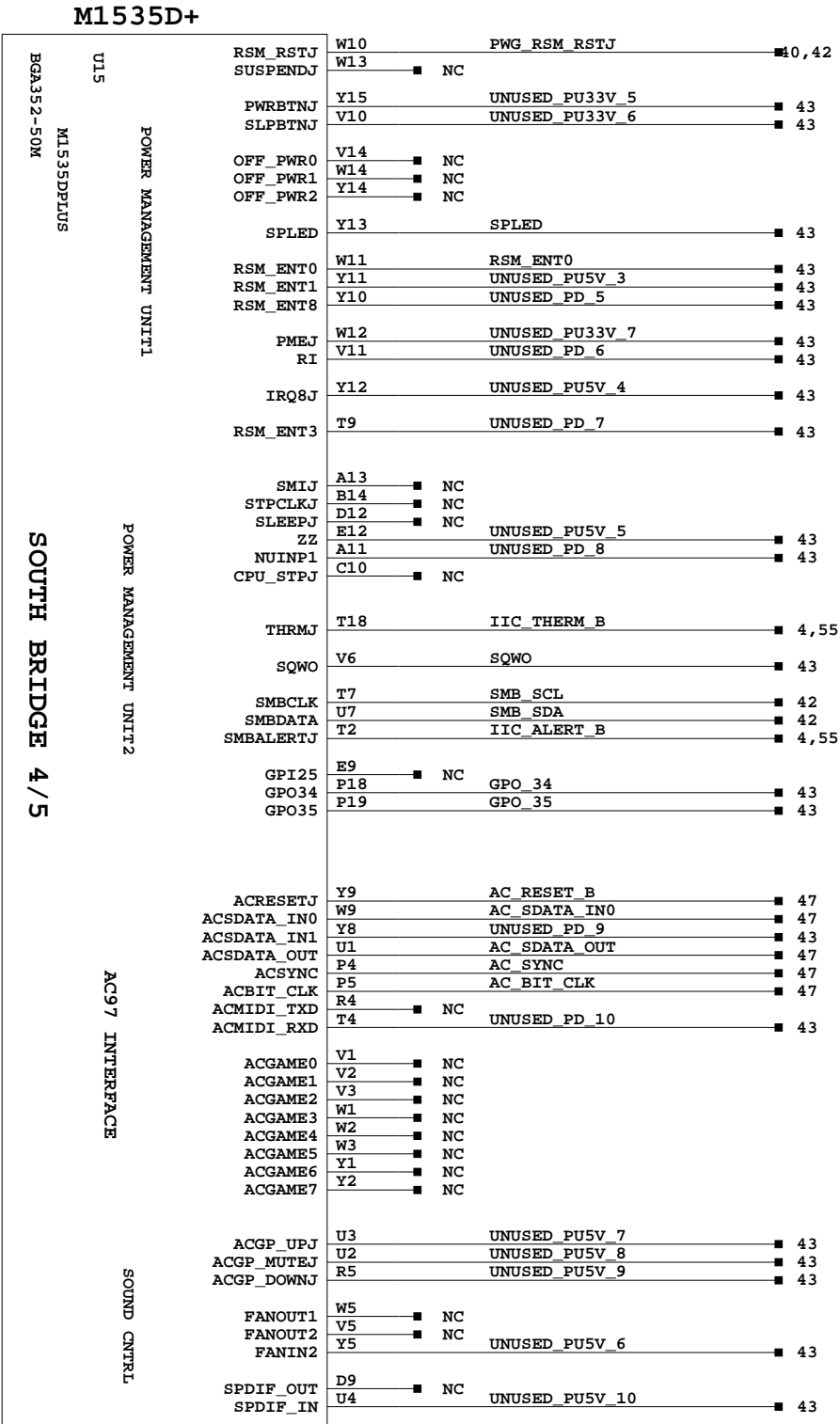
PCI SOUTH BRIDGE, PART 2-3



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SOUTH BRIDGE, PART 2-3

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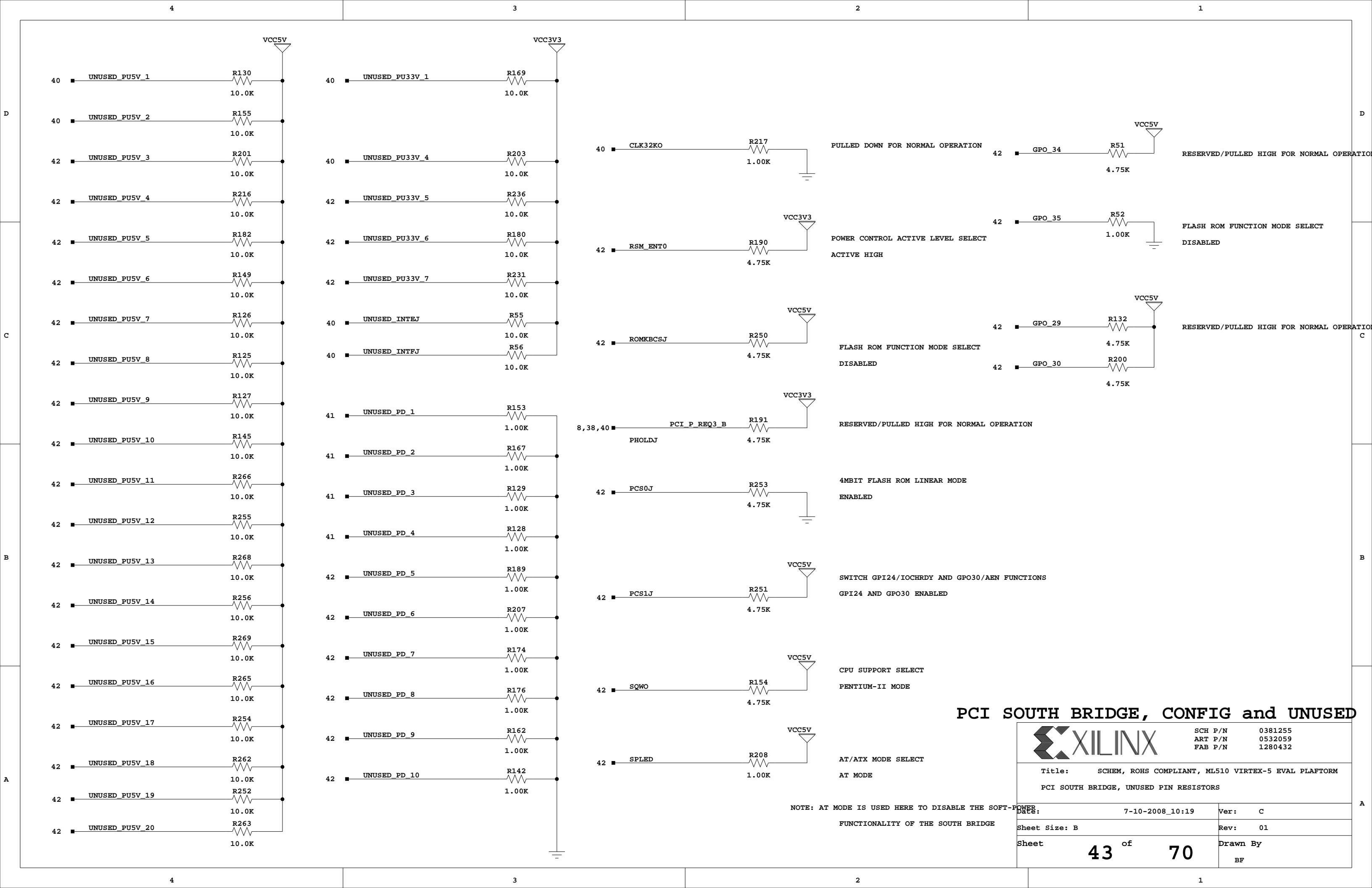
PCI SOUTH BRIDGE, PART 4-5

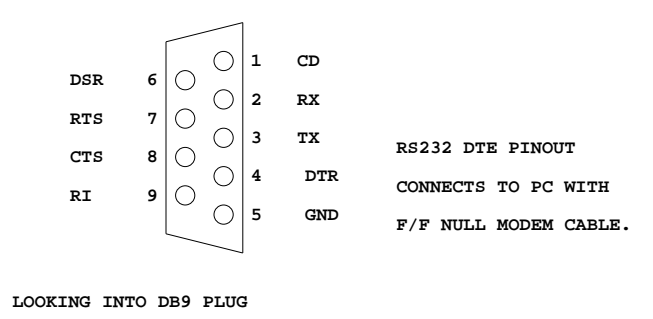
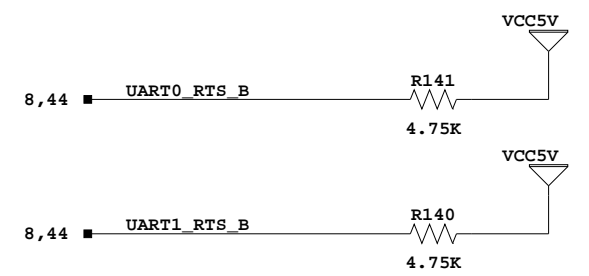
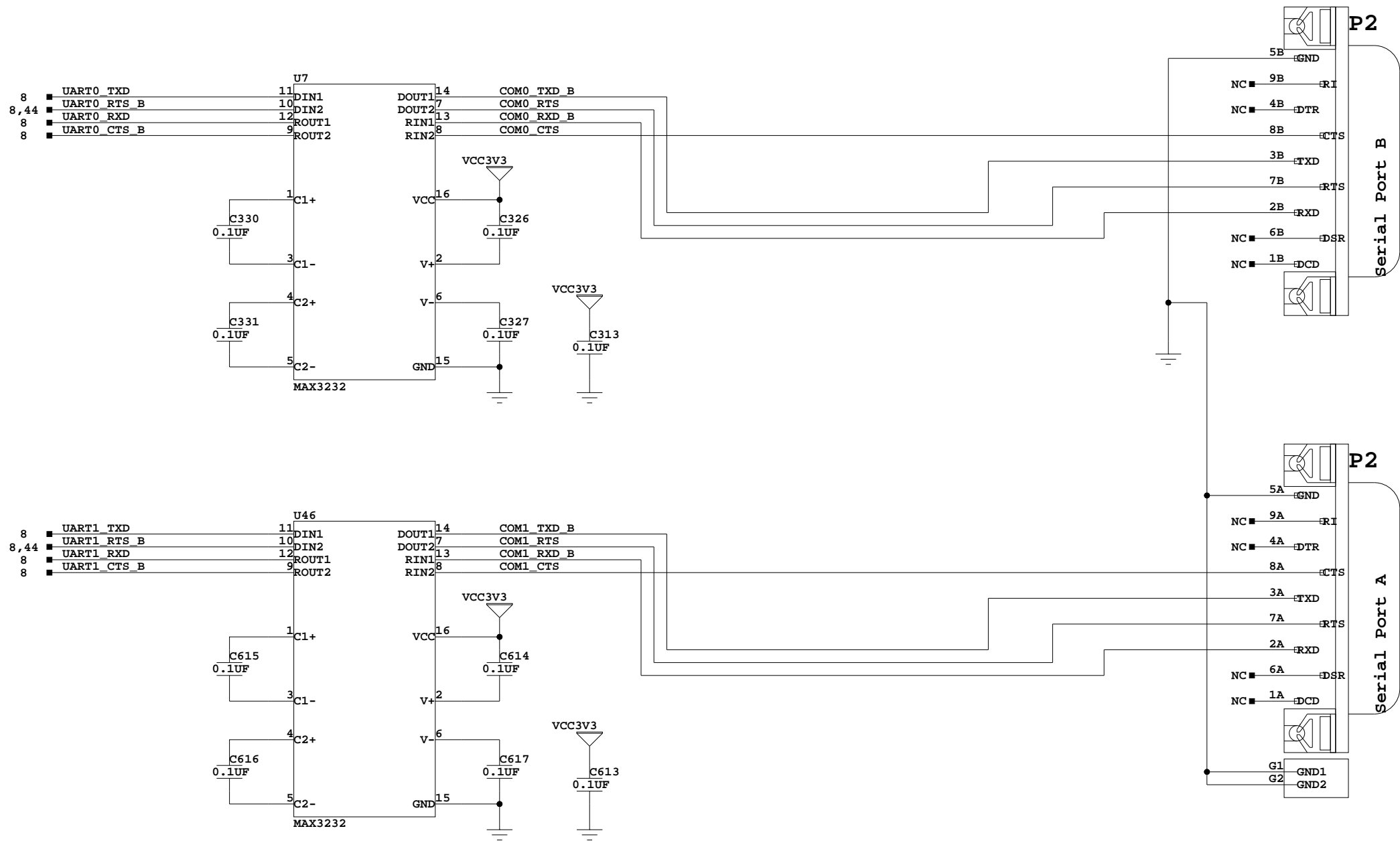


SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm
PCI SOUTH BRIDGE, PART 4-5

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Silkscreen:
"COM 1"

Silkscreen:
"COM 2"

RS232 SERIAL PORT INTERFACE

SCH P/N0381255

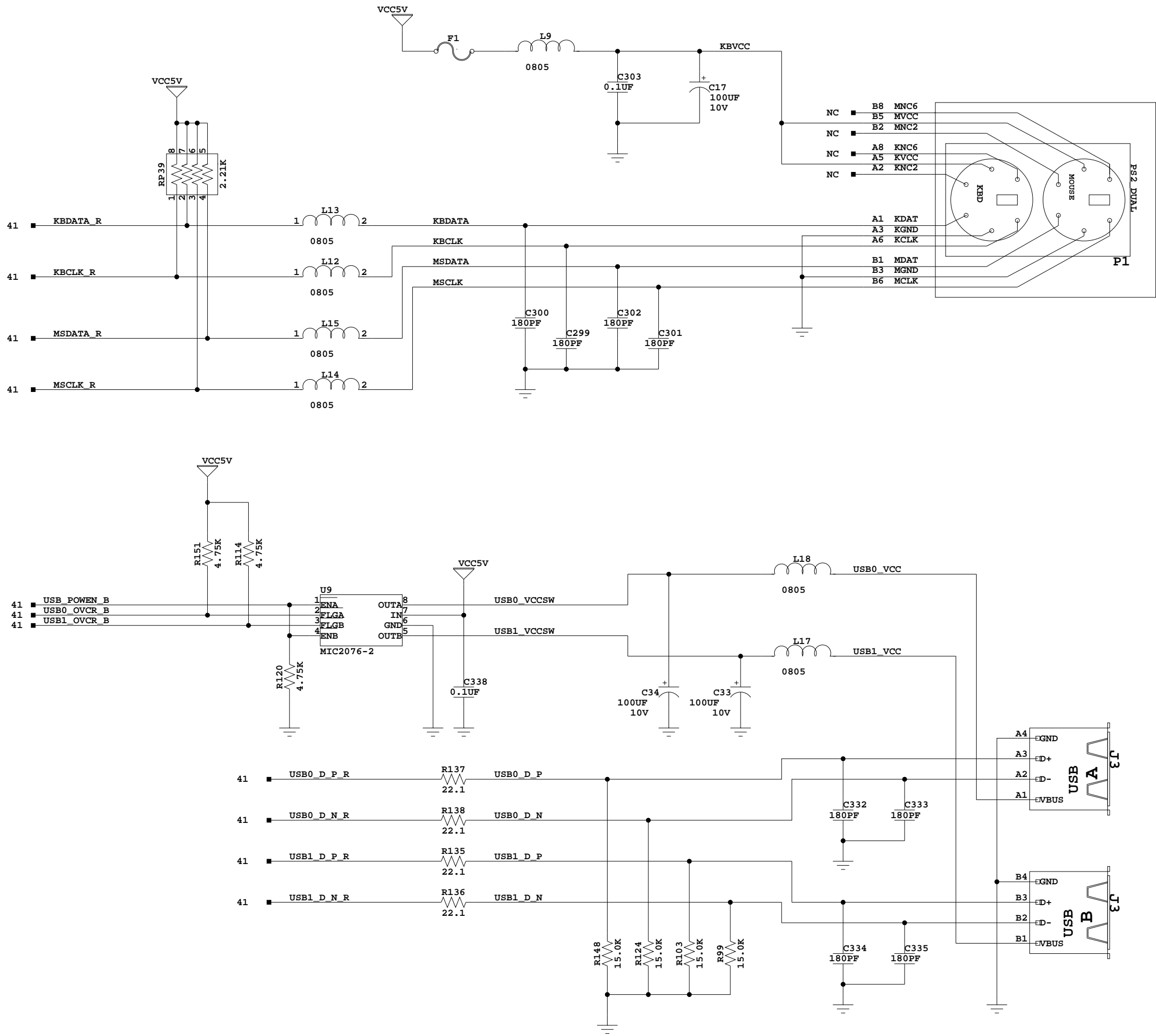
ART P/N0532059

FAB P/N1280432


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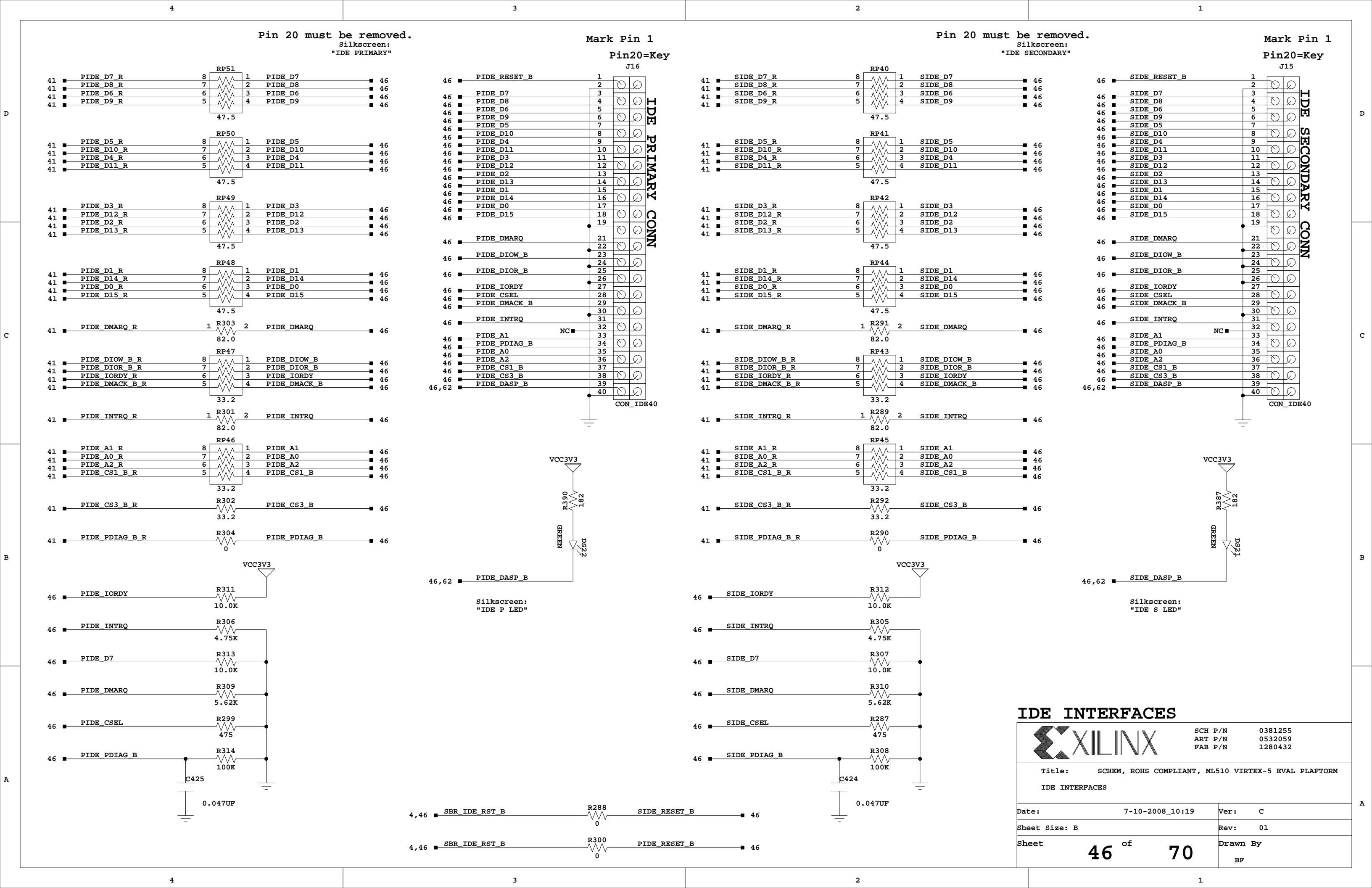
RS232 SERIAL PORT INTERFACE

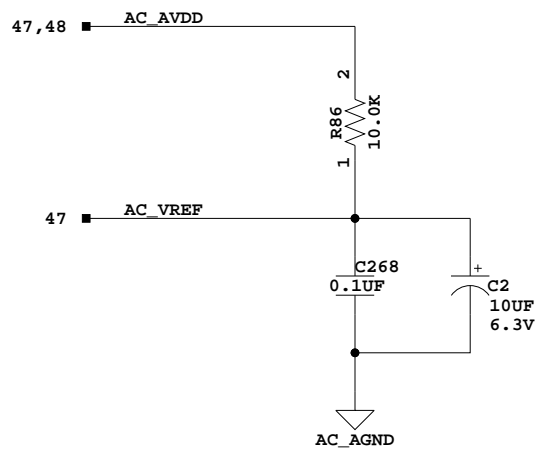
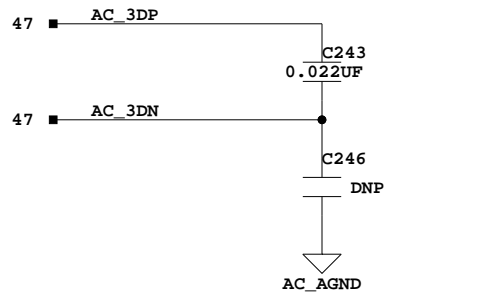
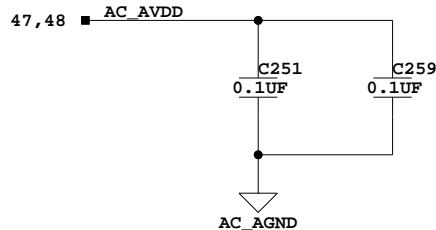
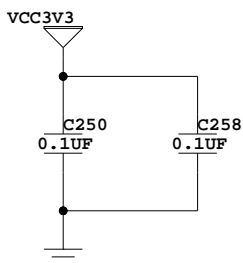
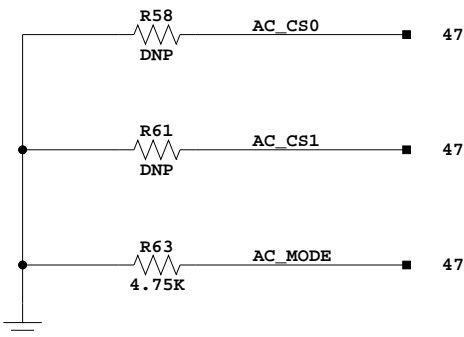
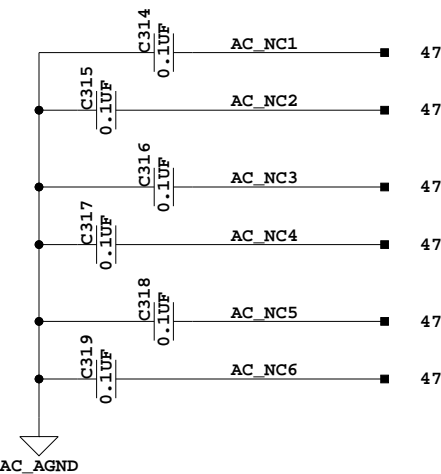
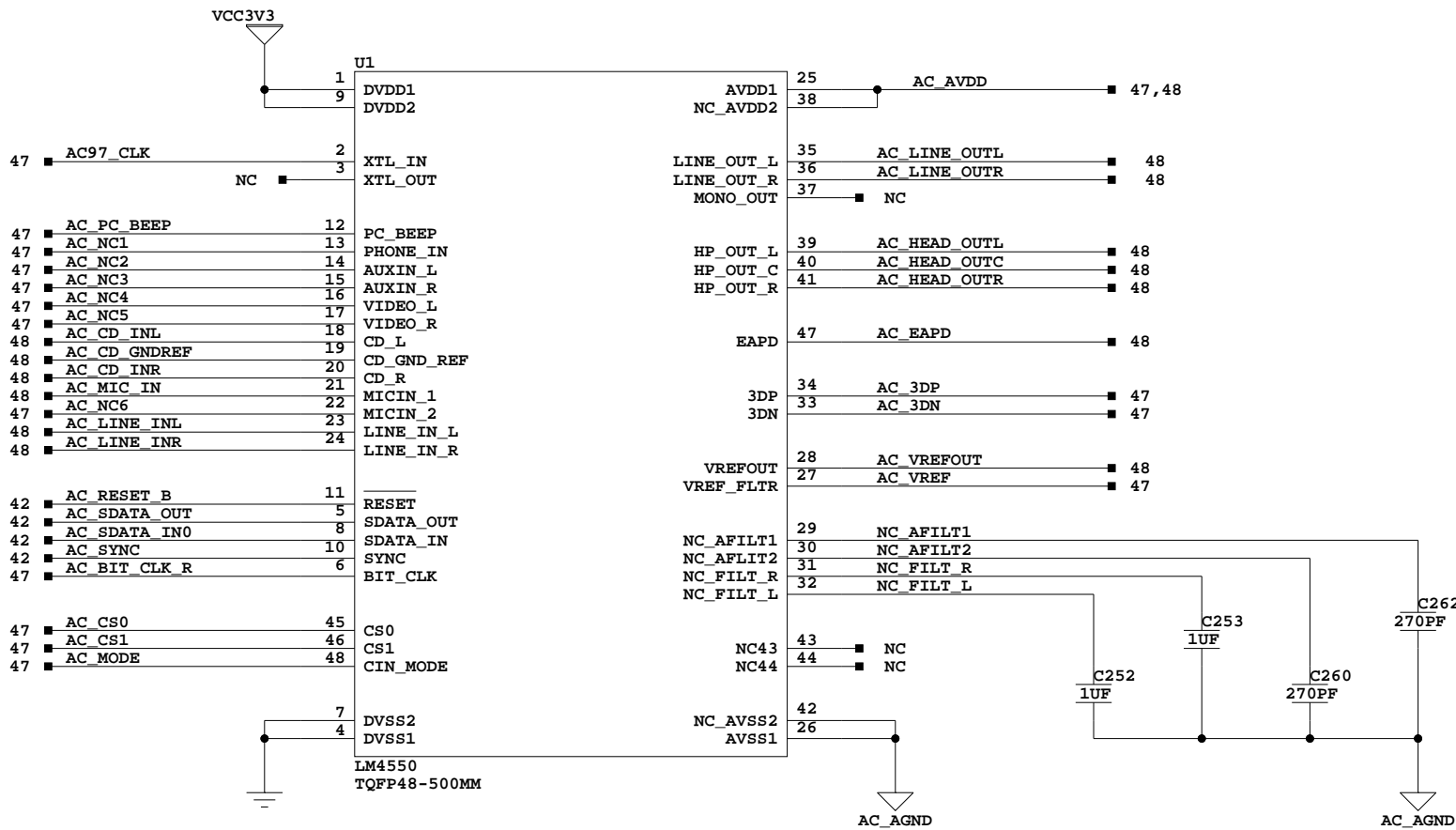
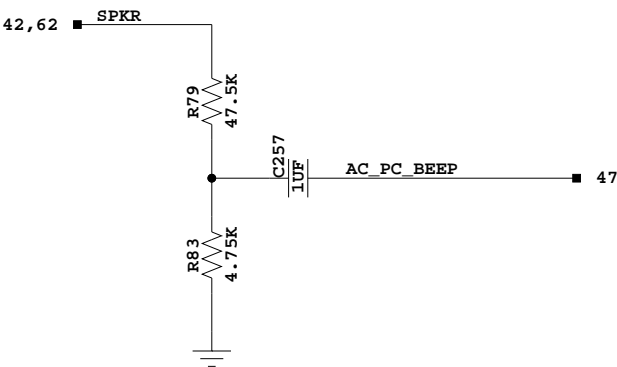
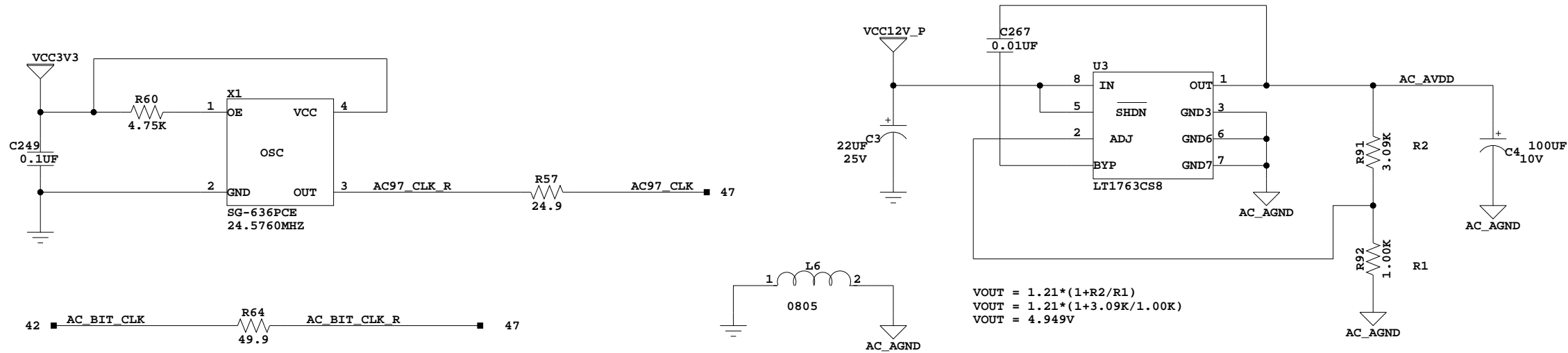
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KBD/MOUSE AND USB INTERFACES

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM		
KBD/MOUSE AND USB INTERFACES		
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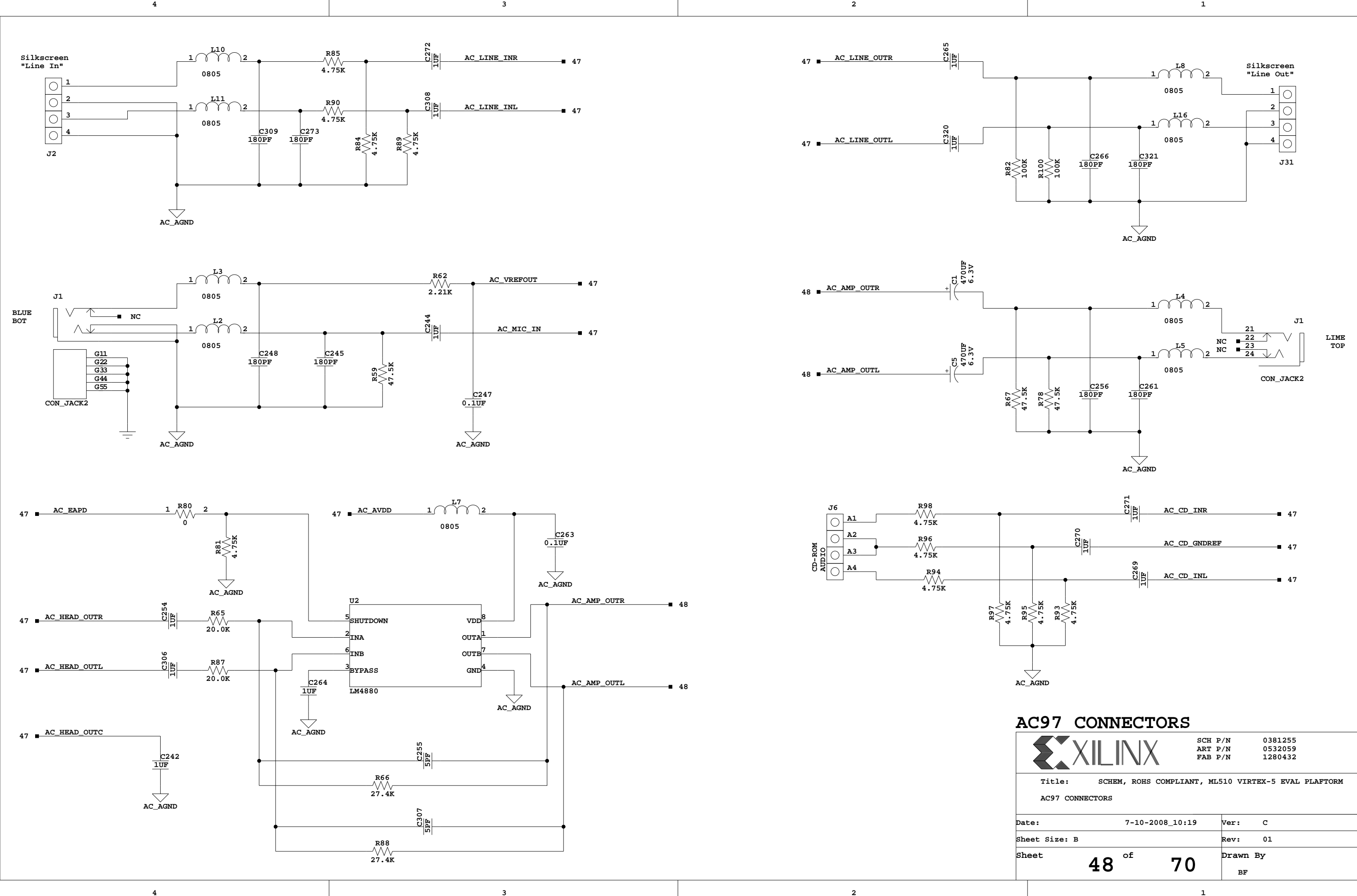
AC97 CODEC




SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
AC97 CODEC

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AC97 CONNECTORS

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm			
AC97 CONNECTORS			
Date:	7-10-2008_10:19	Ver:	C
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SGMII:
GTP 124_1

NOTE:
PHY ADDR = '00111'

NOTE:
BOTTOM SGMII

10/100/1000
RJ45 AND
MAGNETICS

DEVICE=RJ45_JC0-0019
P7
PARTS=1
LEVEL=STD
PKG_TYPE=RJ45_JC0-0019

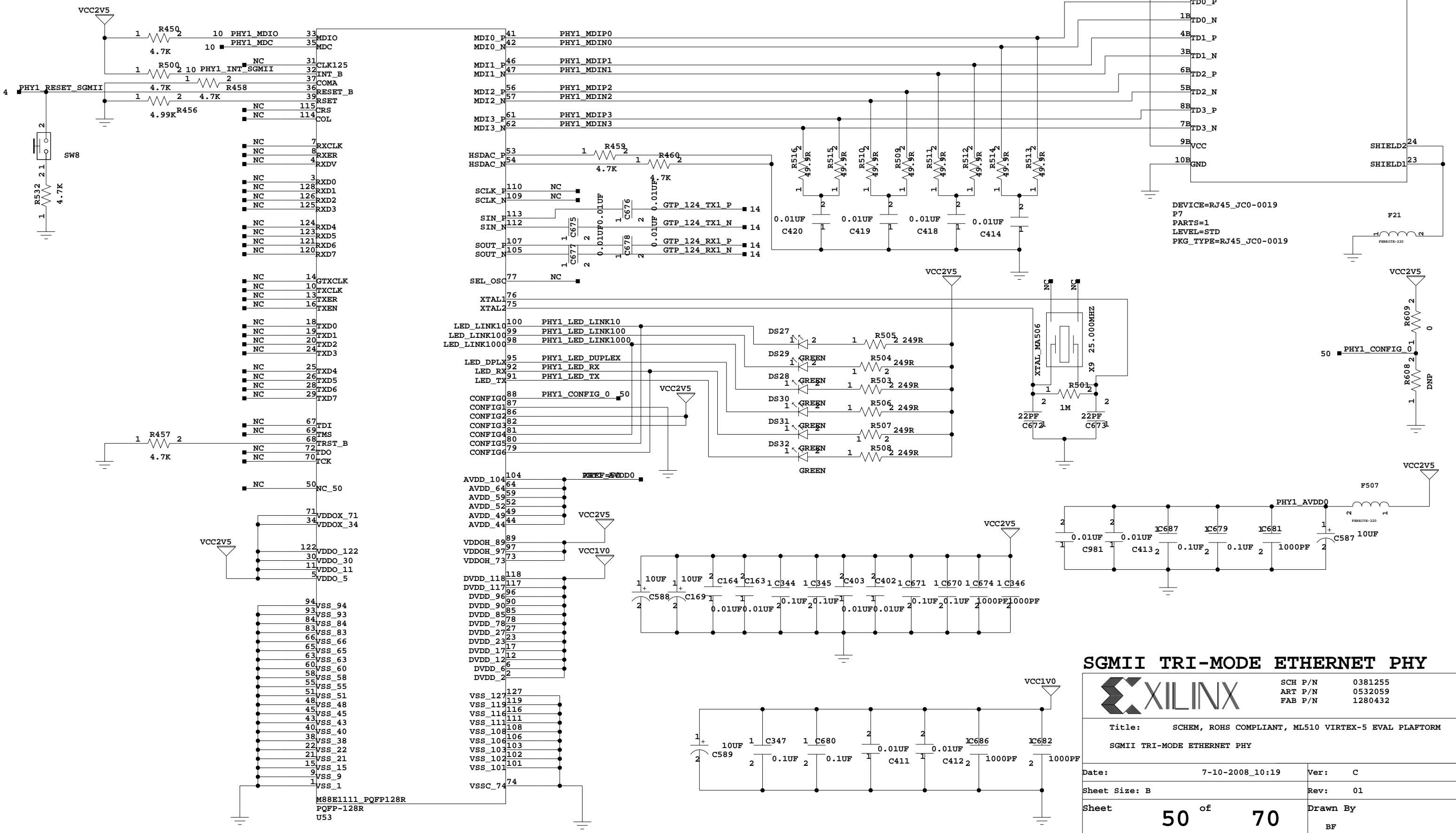
SGMII TRI-MODE ETHERNET PHY



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
SGMII TRI-MODE ETHERNET PHY

Date:	7-10-2008_10:19	Ver:	C
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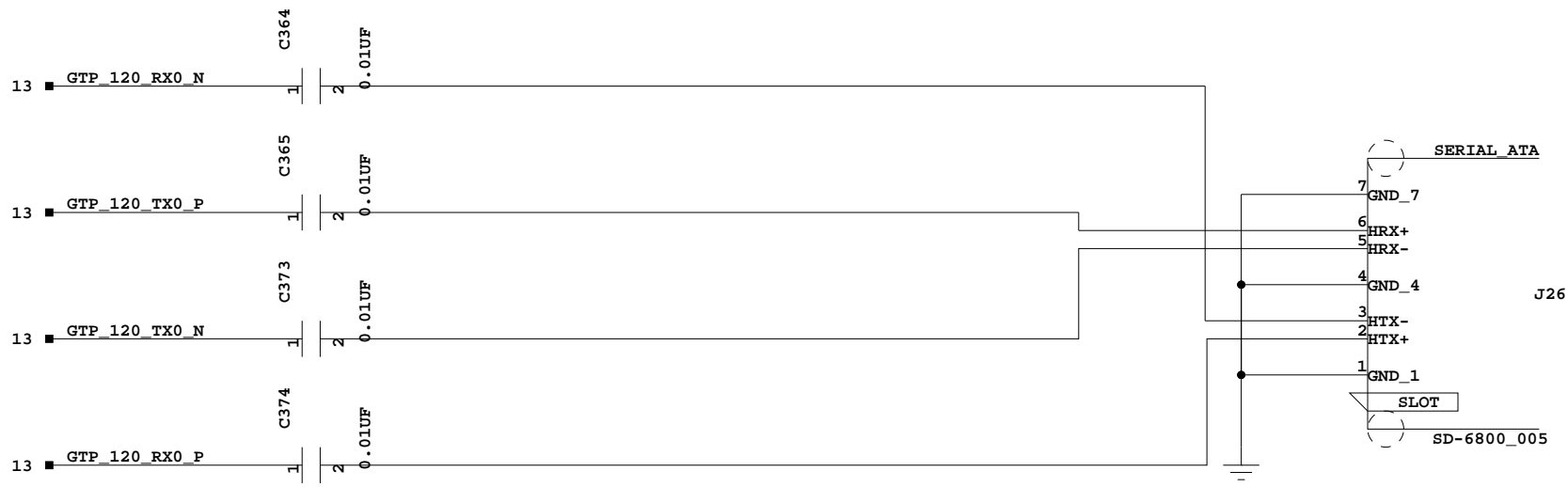
SATA Host 1

GTP 120_1




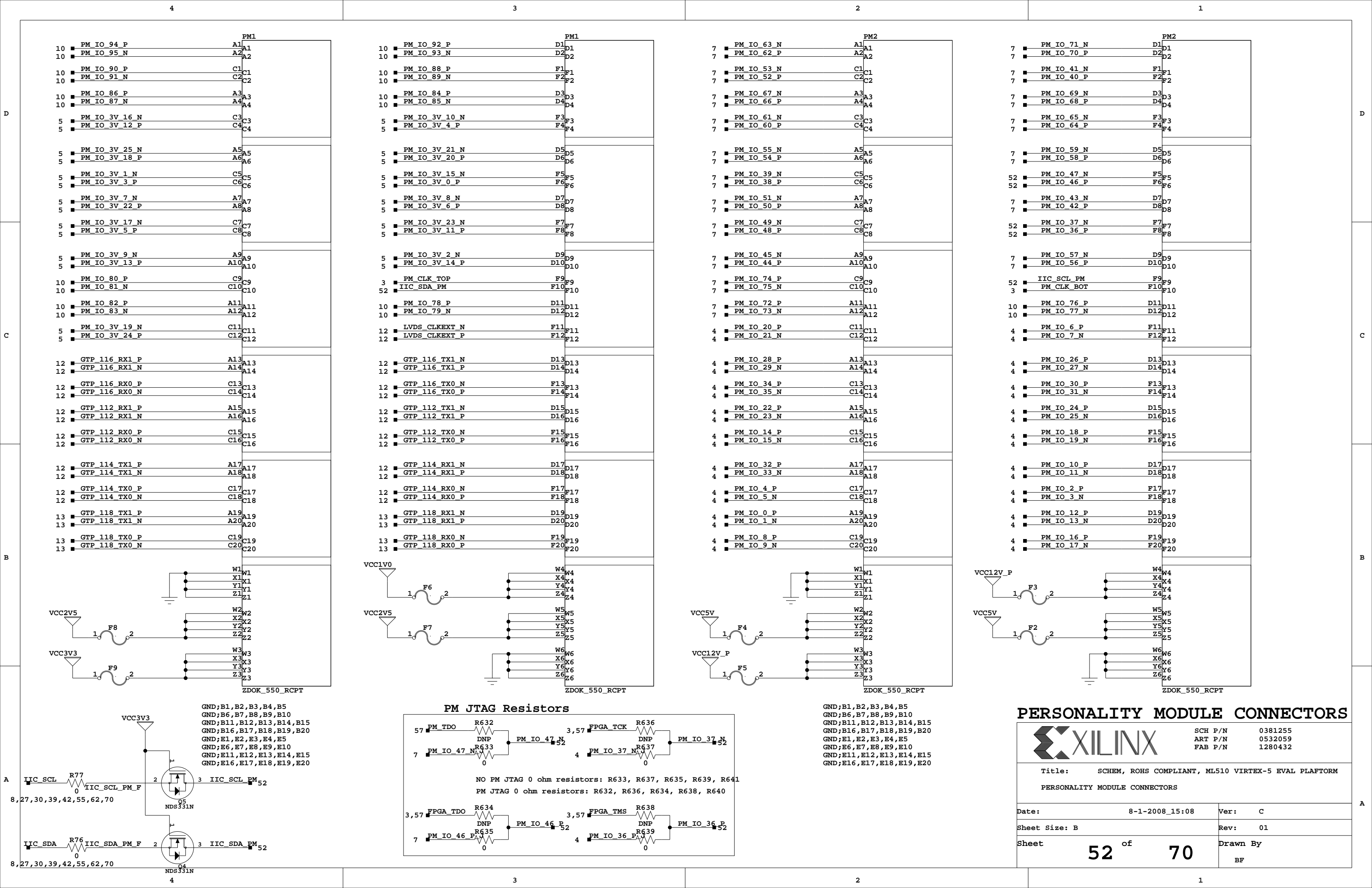
SATA Host 2

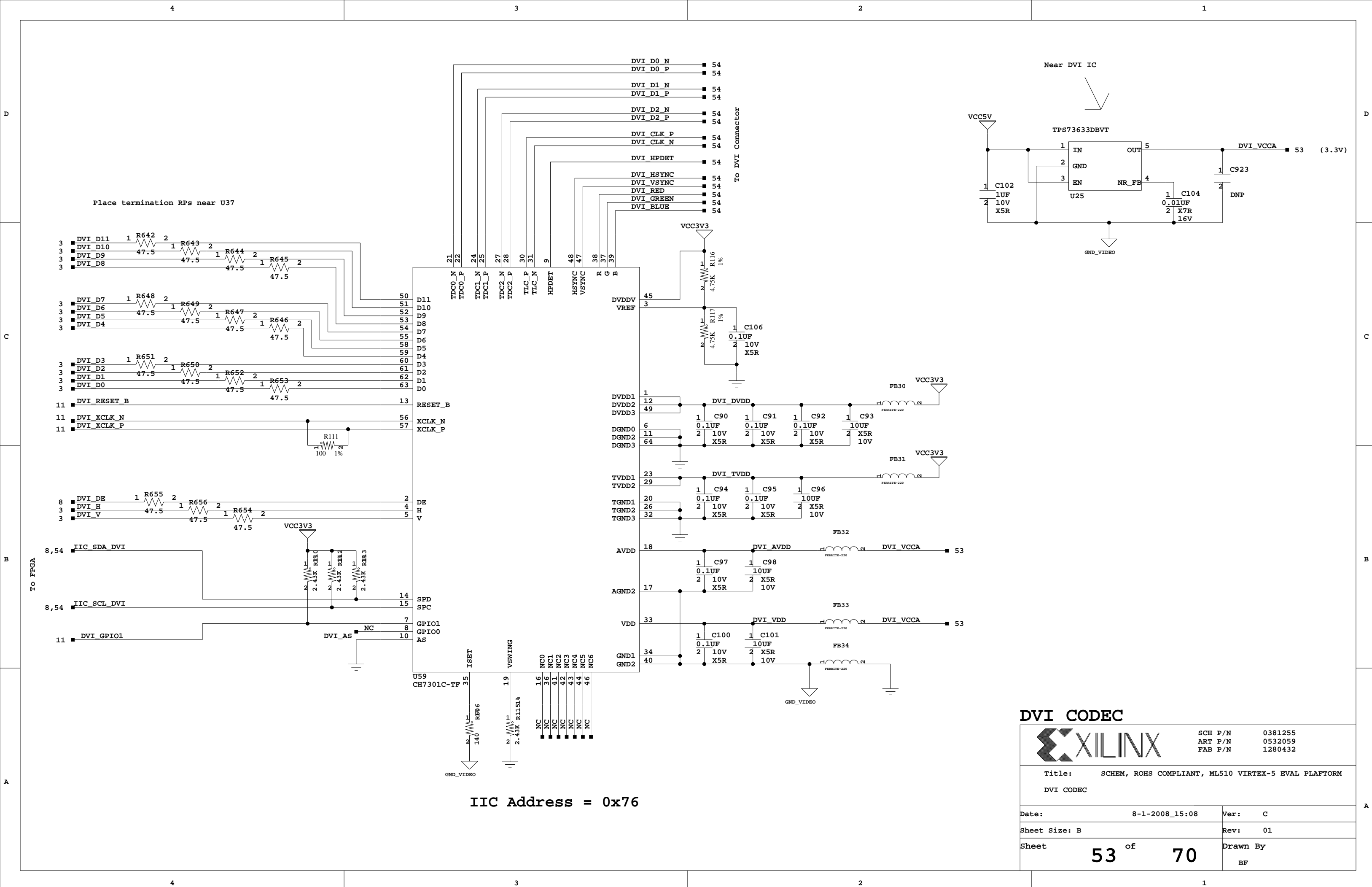
GTP 120_0

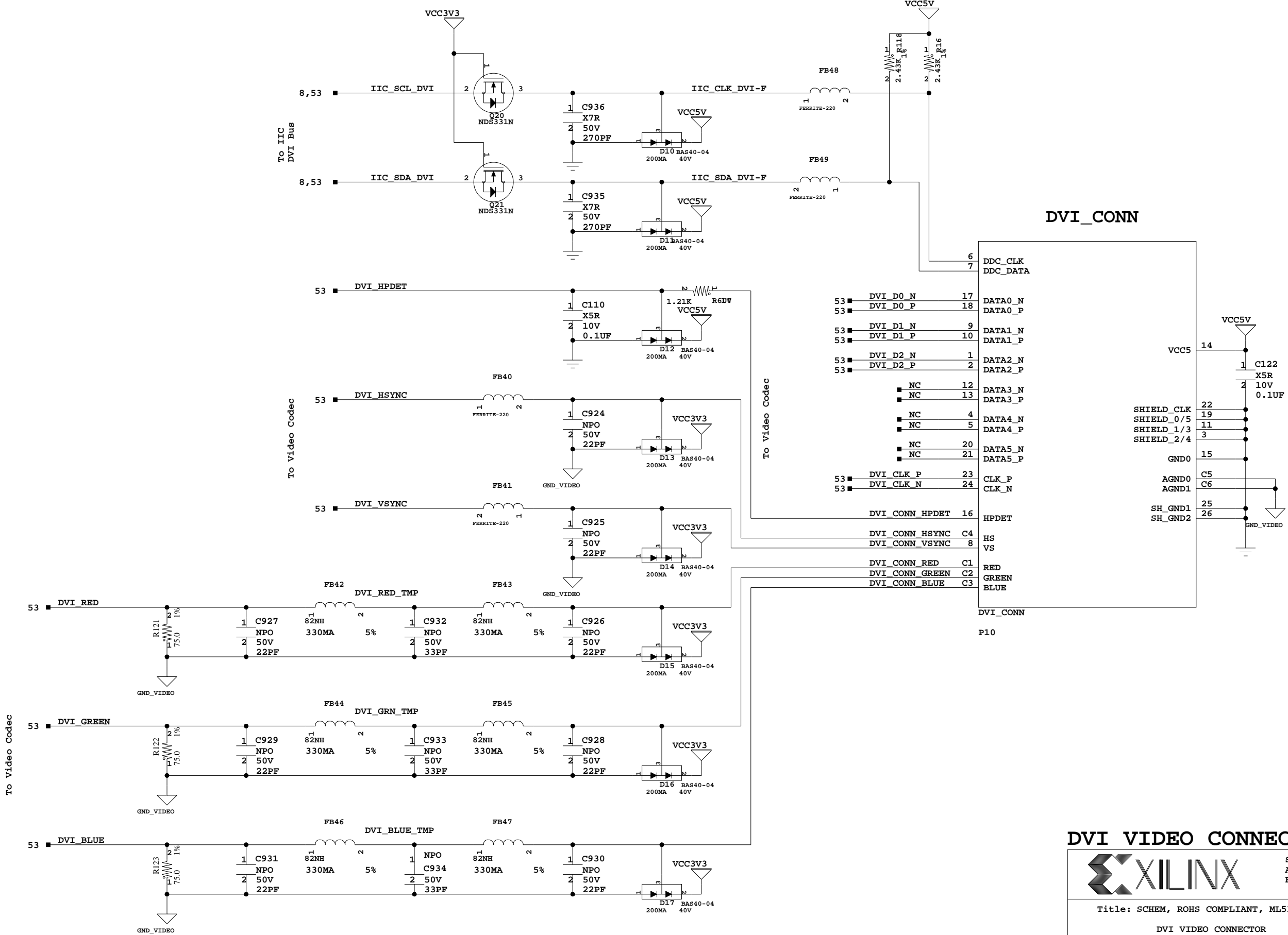


SATA INTERFACE

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
SATA INTERFACE			
Date:	7-10-2008_10:19	Ver:	C
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DVI VIDEO CONNECTOR



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm

DVI VIDEO CONNECTOR

Date: 7-10-2008_10:19

Ver: C

Sheet Size: B

Rev: 01

Sheet

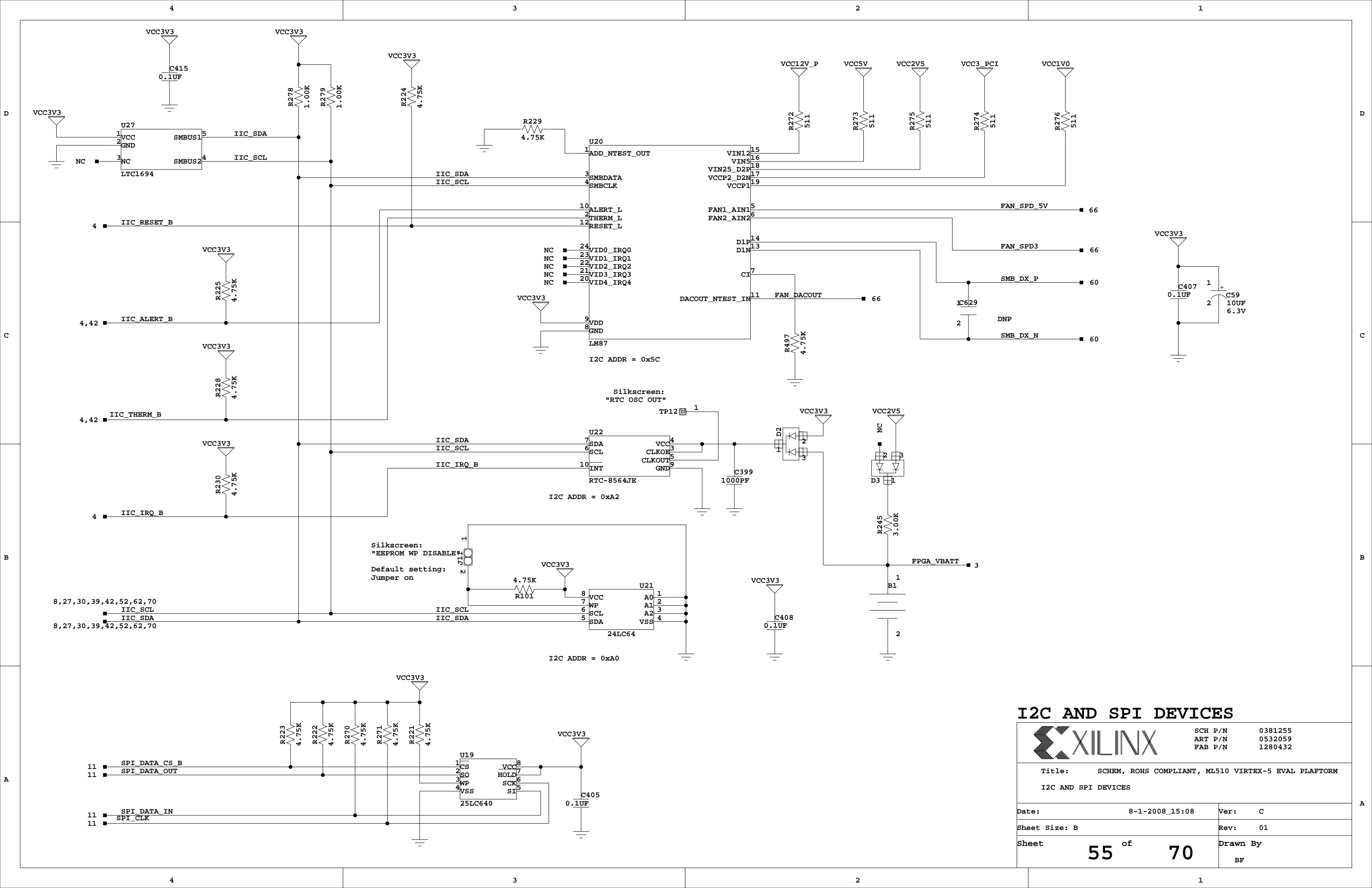
54

of


70

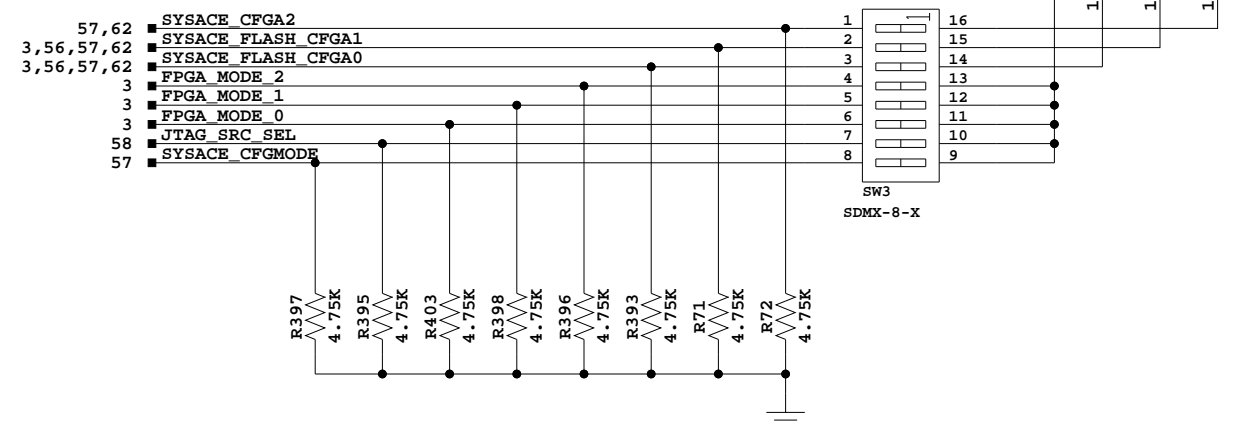
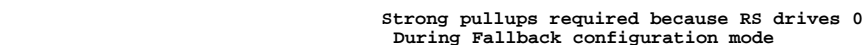
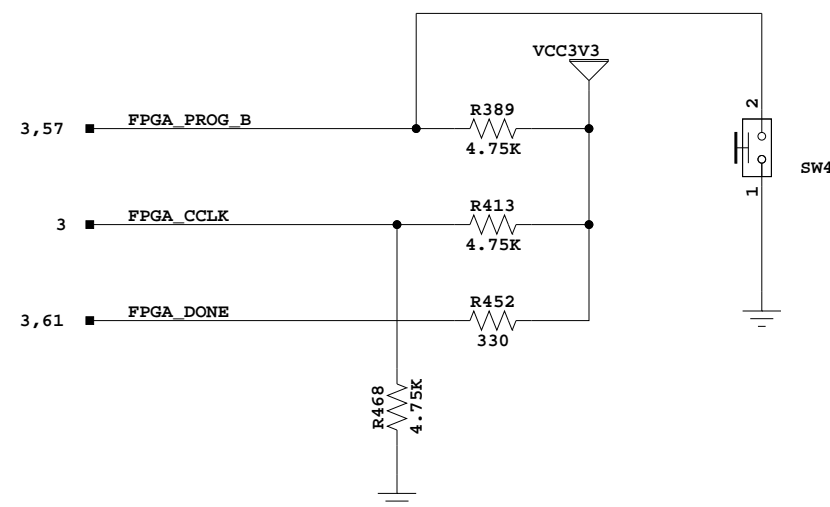
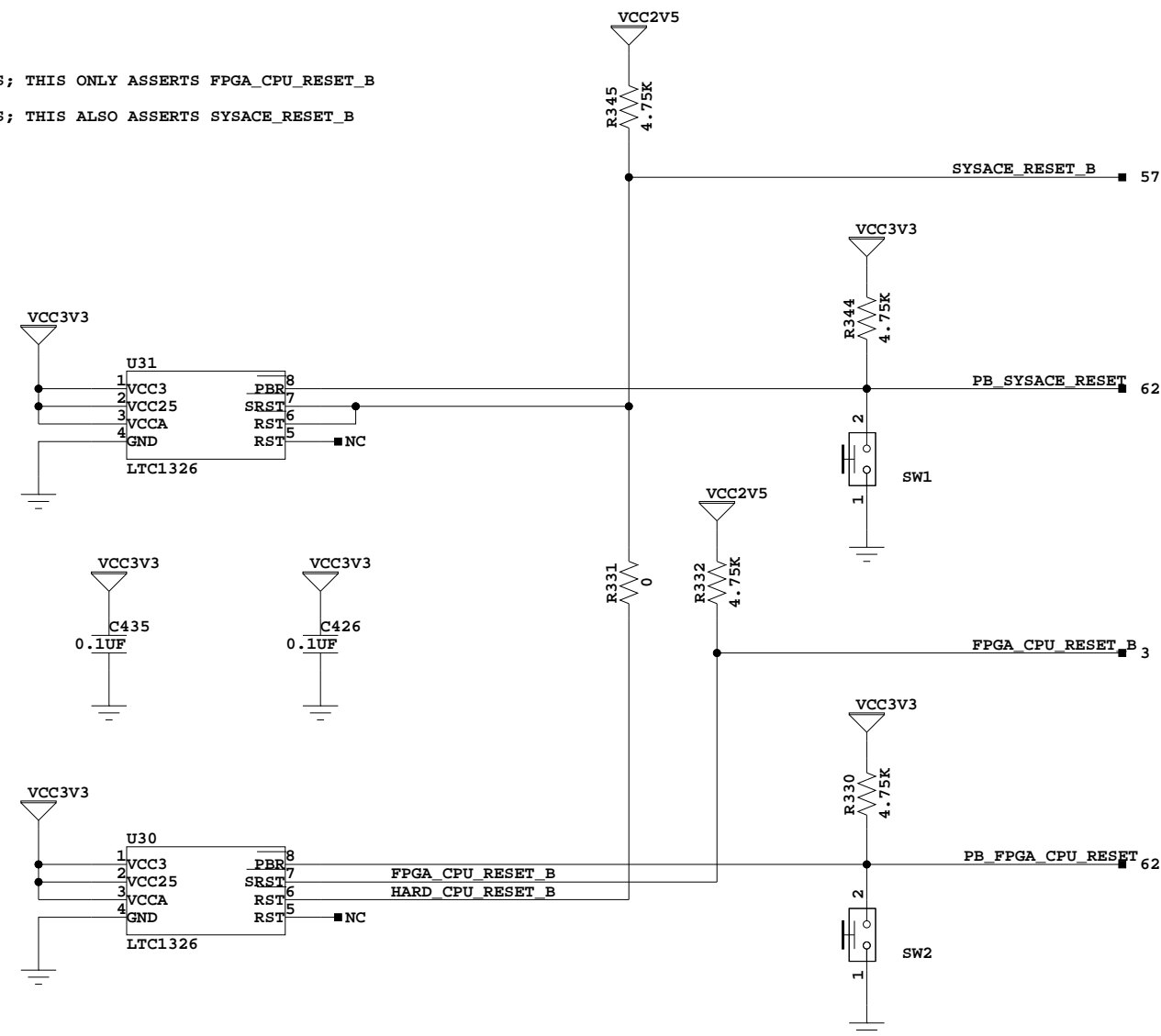
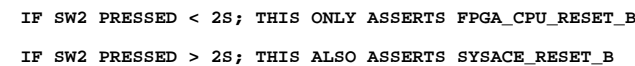
Drawn By

BF



I2C AND SPI DEVICES

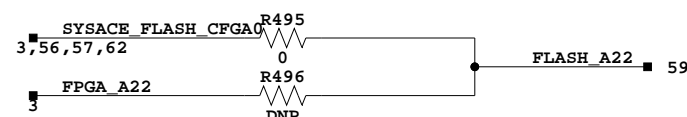
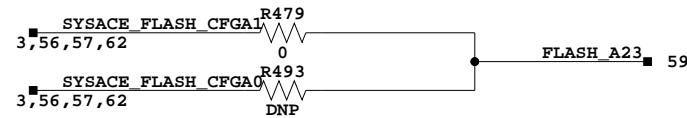
	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM		
I2C AND SPI DEVICES		
Date:	8-1-2008_15:08	Ver: C
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BPI Flash Addressing Scheme

	FPGA (U37) BPI Addr Pin	Schematic Net Name	Net Connection After Jumpering		Parellel Flash (U43) Addr Pin
4 x 64 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	FLASH_A23	R479-0ohm; R493-DNP	A24 (U43.26)
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A22	R495-0ohm; R496-DNP	A23 (U43.9)
	A22 (U37.AK14)	FPGA_A22	no connect		no connect
2 x 128 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	no connect	R479-DNP; R493-0ohm	no connect
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A23	R495-DNP; R496-0ohm	A24 (U43.26)
	A22 (U37.AK14)	FPGA_A22	FLASH_A22		A23 (U43.9)
Any Address Mode	A[21:0] (U37)	FLASH_A[21:0]	FLASH_A[21:0] N/A		A[22:1] (U43)

Note: See the ML510 User Guide for more details about BPI Flash



FPGA CONFIG, RESET, AND MISC I/O



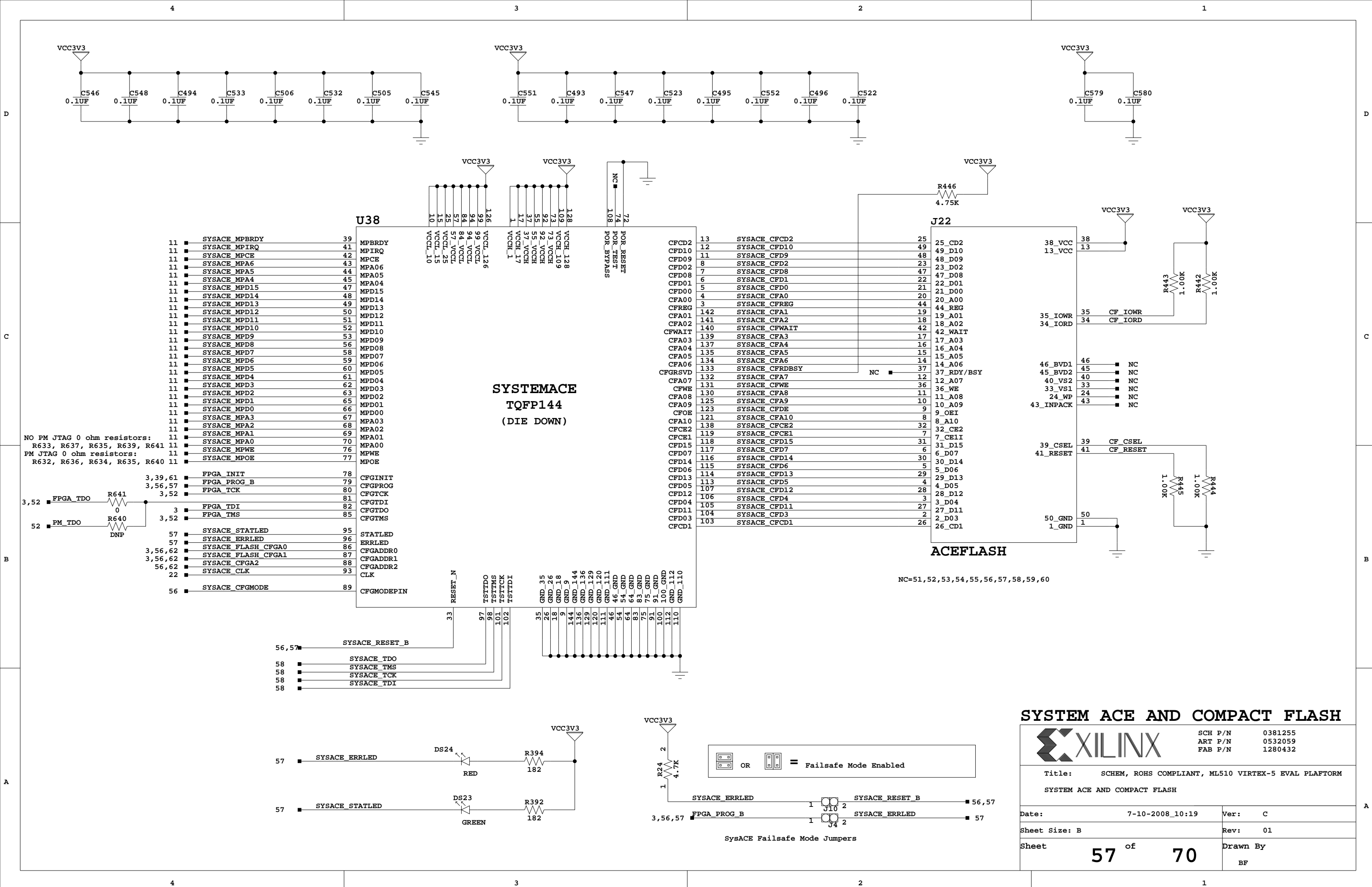
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

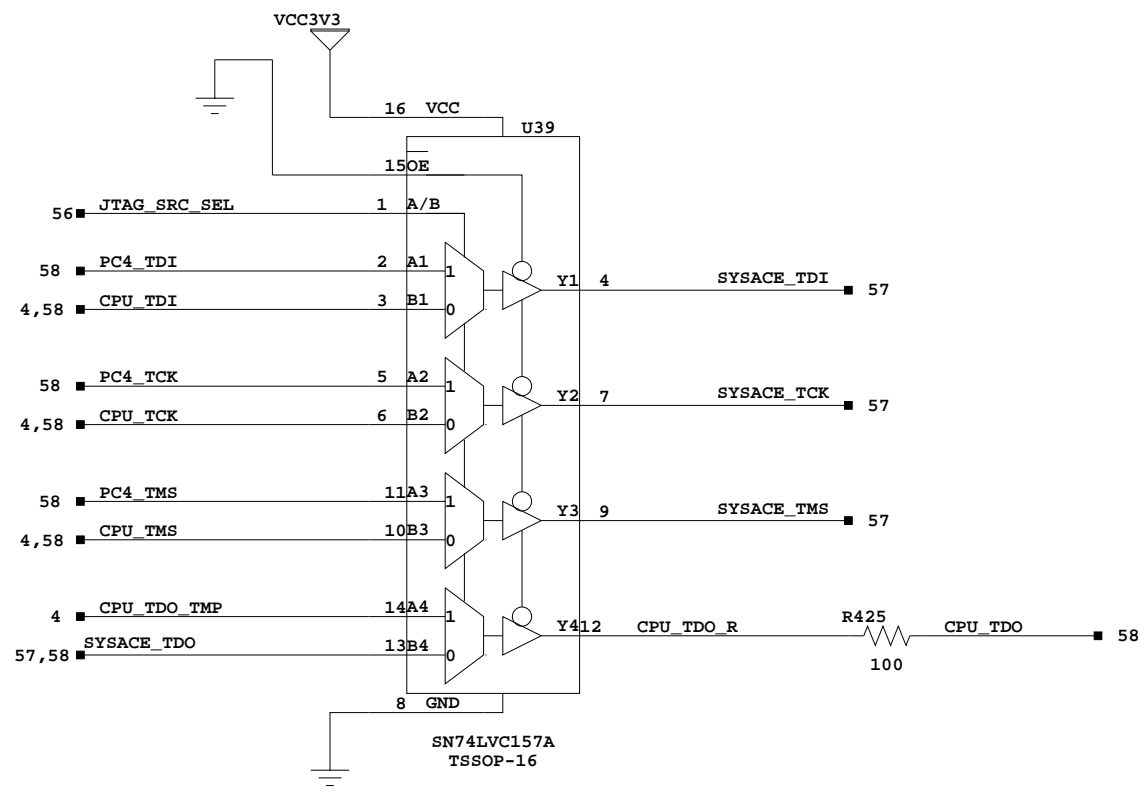
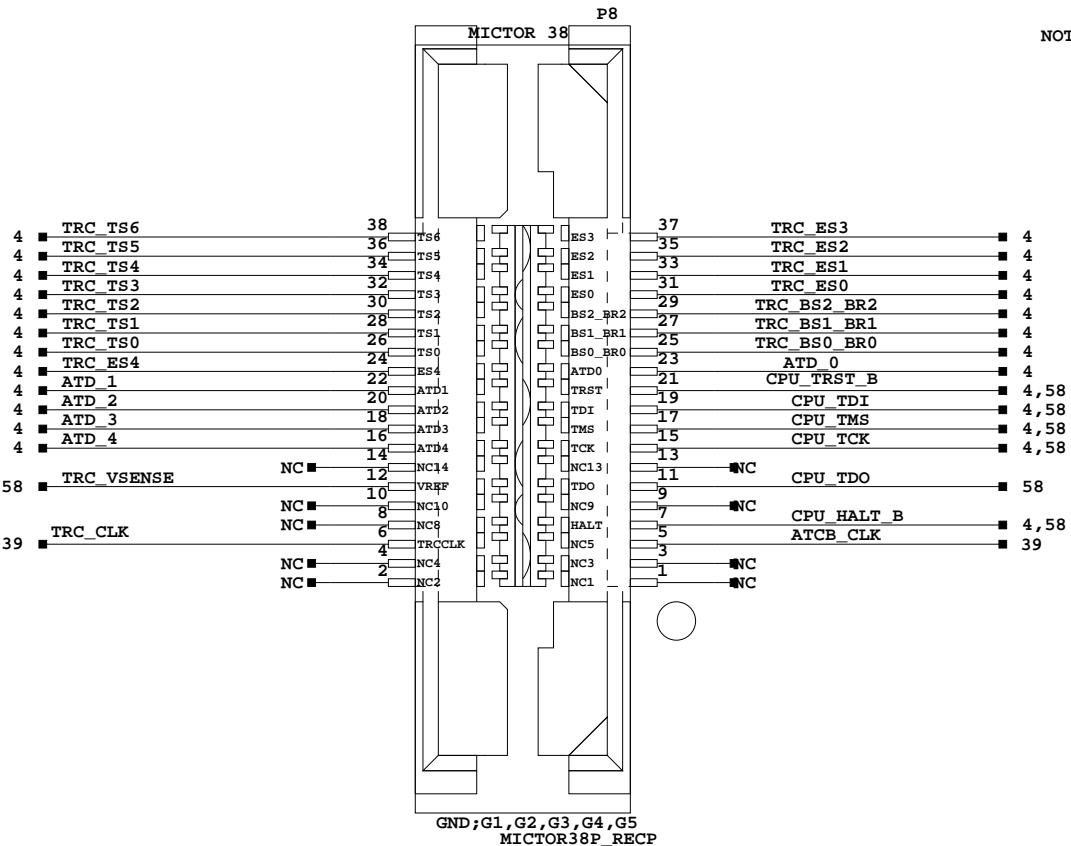
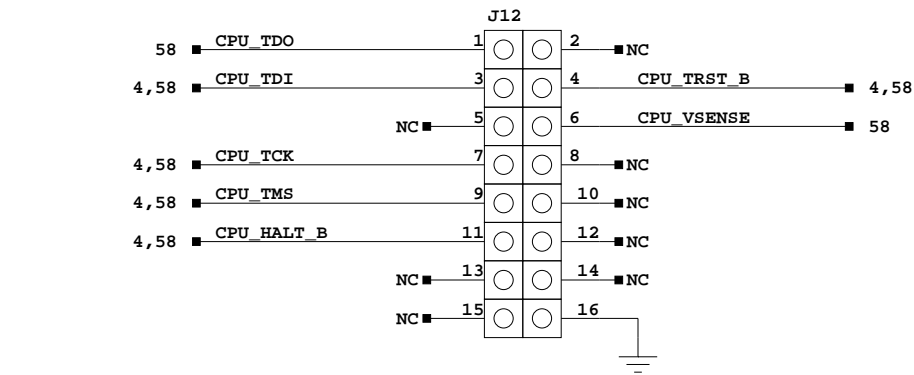
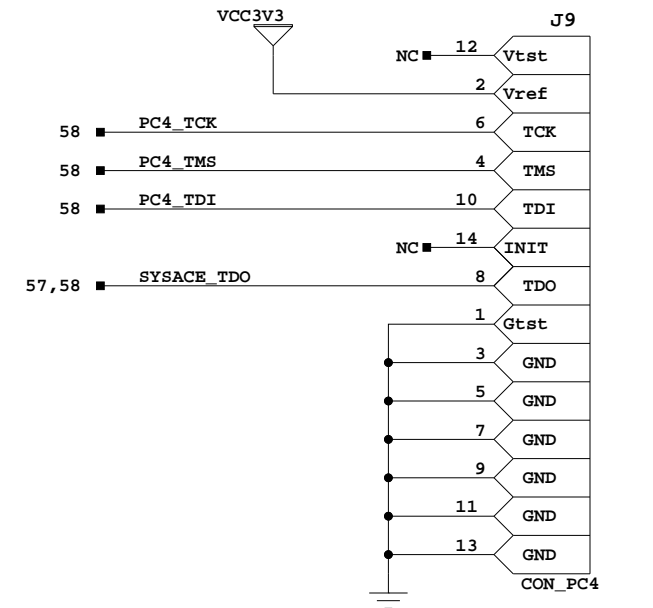
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA CONFIG, RESET, AND MISC I/O

Date: 7-10-2008 10:19 Ver: C

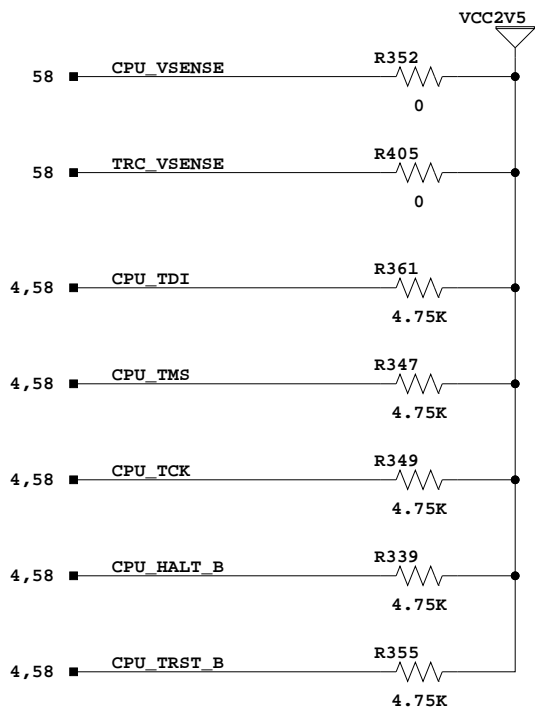
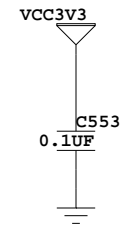
Sheet Size: B	Rev: 01
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Sheet	56	of	70	Drawn By	BF
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NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO 3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS. THE SERIES RESISTOR ON CPU_TDO IS INTENDED TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.



JTAG, DEBUG, TRACE CONNECTORS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
JTAG, DEBUG, TRACE CONNECTORS		
Date:	7-10-2008_10:19	Ver: C
Sheet Size: B		Rev: 01
Sheet	58 of 70	Drawn By BF

D

C

B

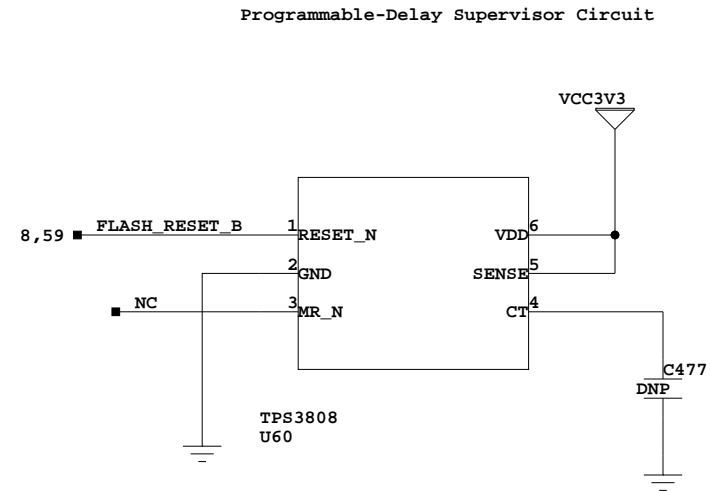
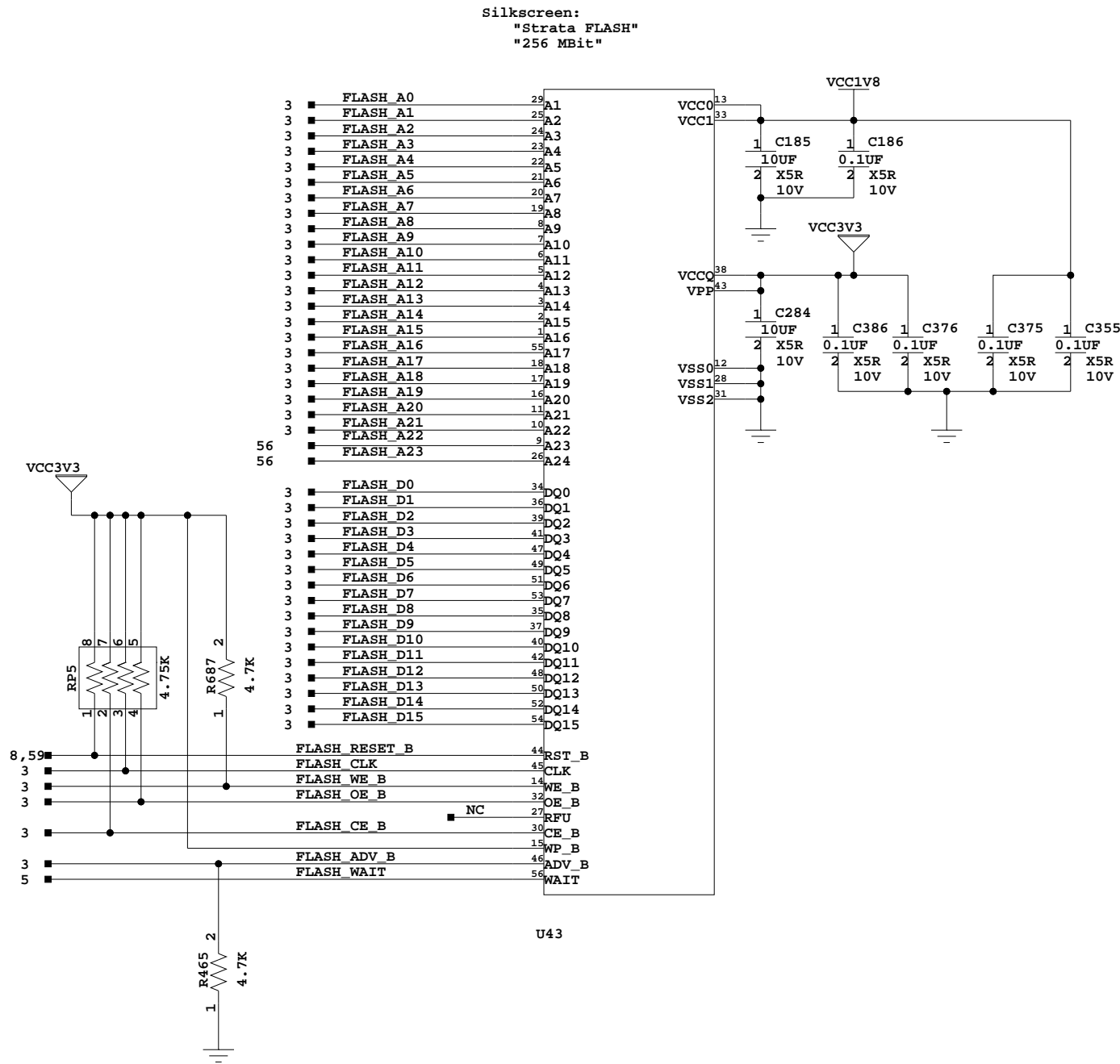
A

D

C


B

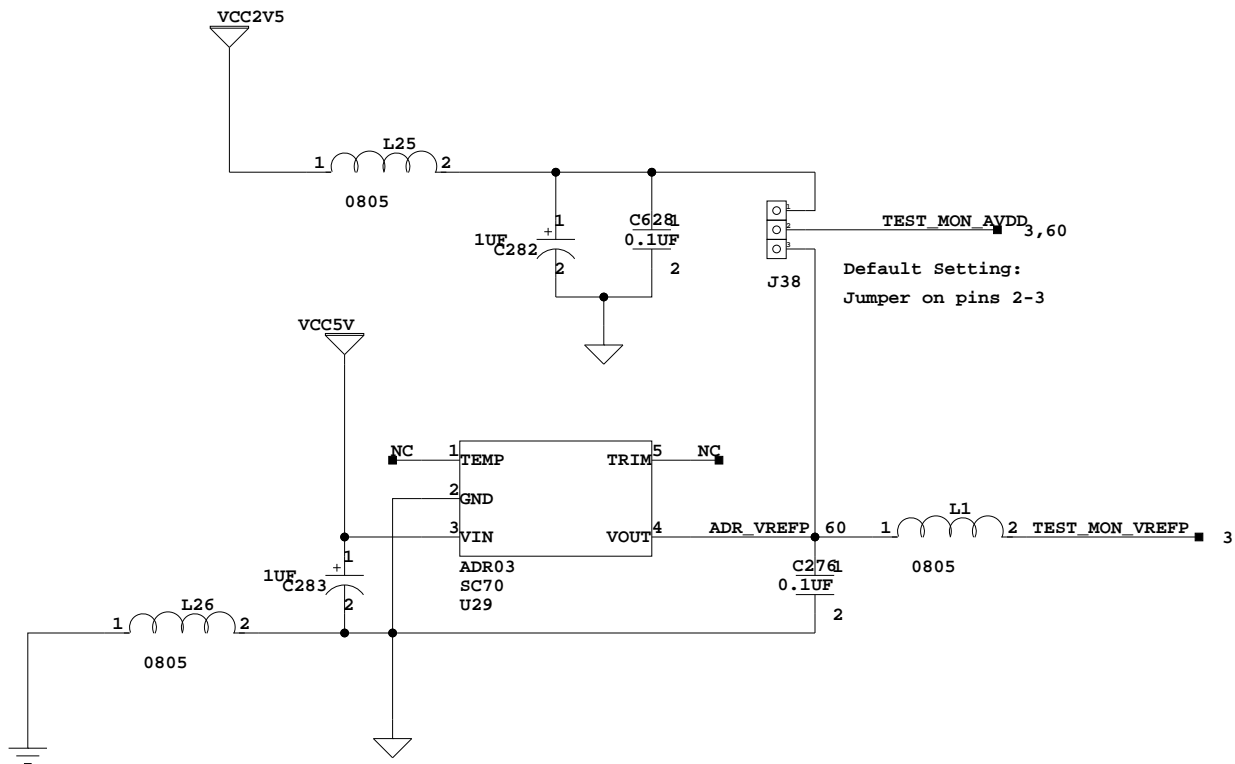
A



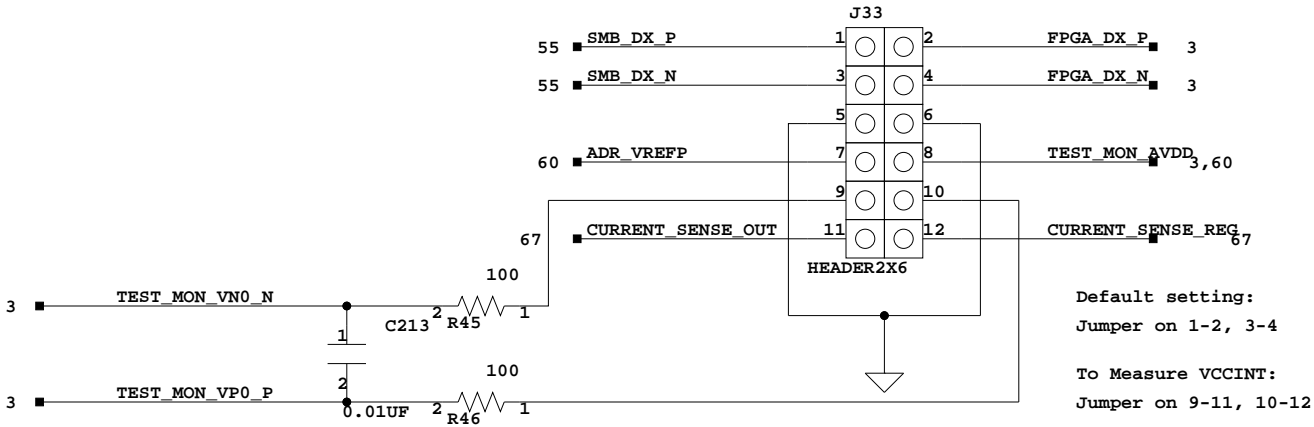
<Cap Value in nF> = (((<DELAY in S>)-(0.5*0.001)) *175)

SYNC. SRAM FLASH

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
SYNC. SRAM FLASH		
Date:	8-1-2008_15:08	Ver: C
Sheet Size: B		Rev: 01
Sheet	59 of 70	Drawn By BF



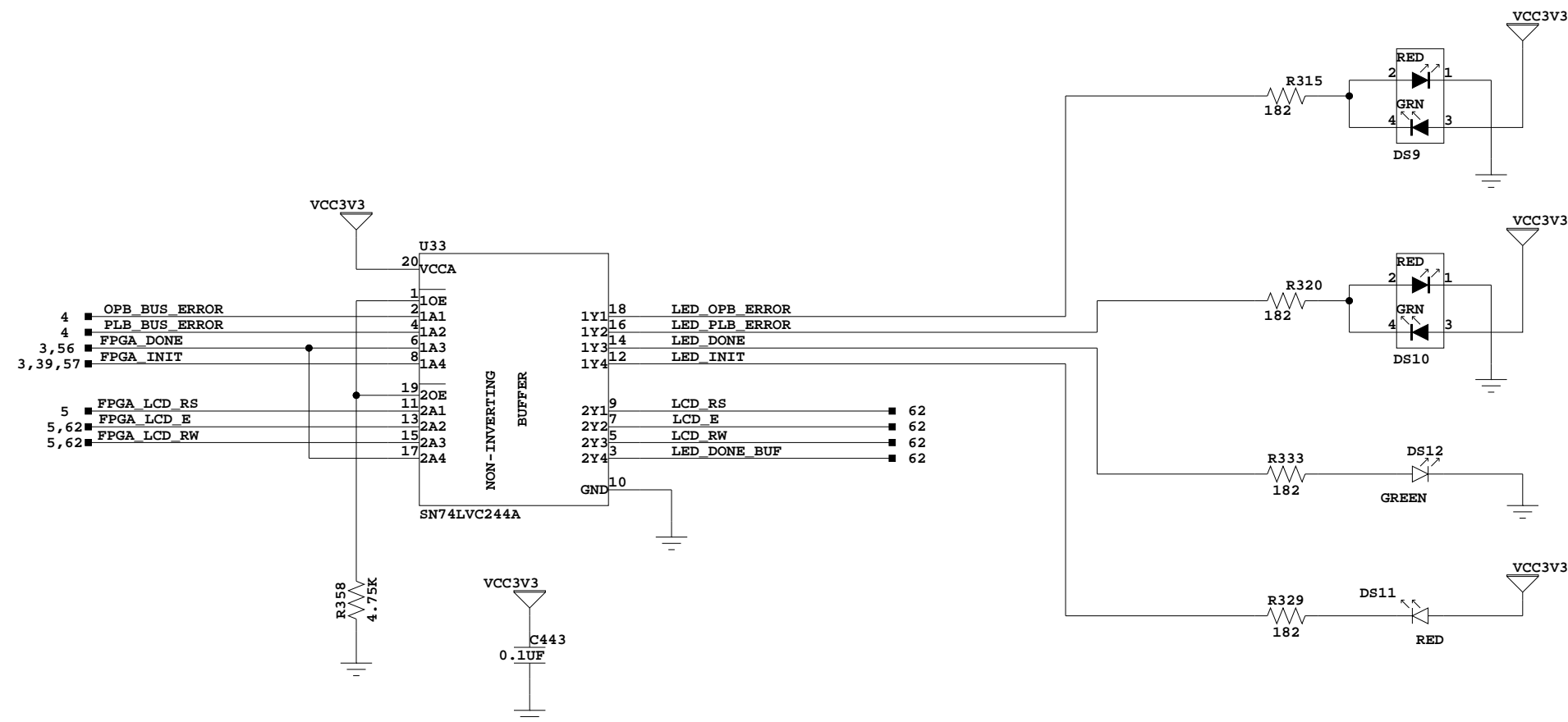
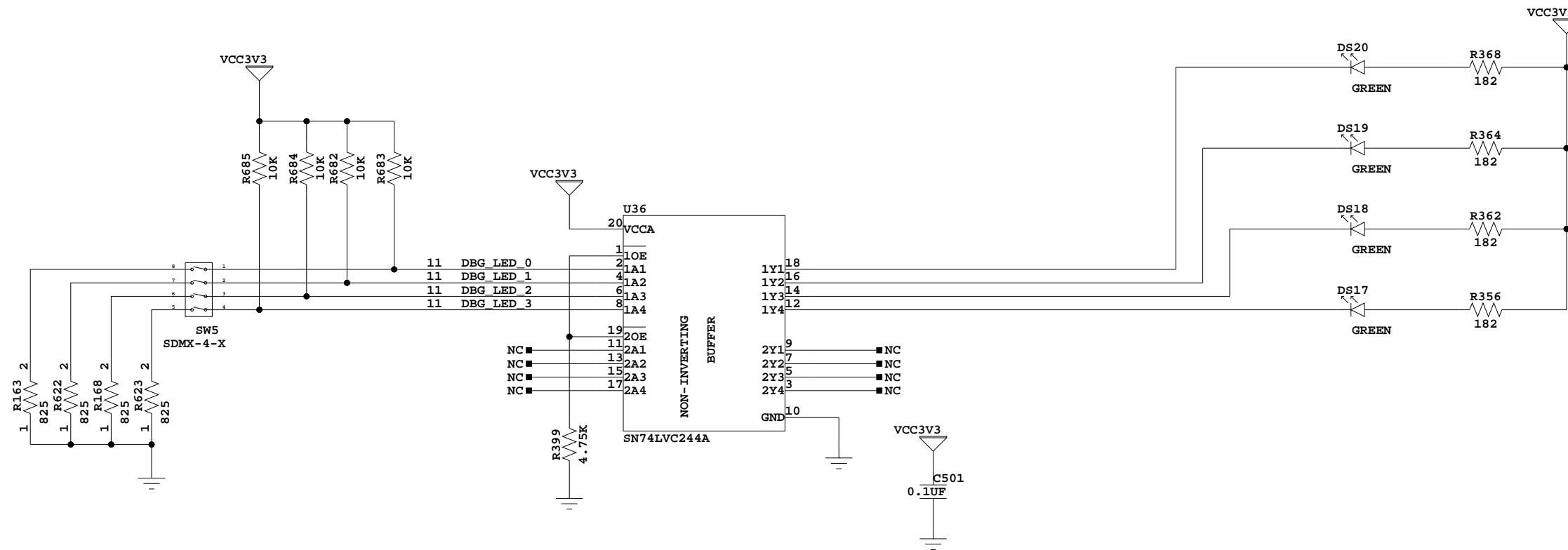
System Monitor Header for probing



place 100 ohm resistors and
0.01 cap near FPGA

SYSMON HEADER / AVDD VREFP SUPPLY

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFORM		
SYS MONITOR HEADER / FPGA AVDD VREFP SUPPLY		
Date:	8-1-2008_15:09	Ver: C
Sheet Size: B		Rev: 01
Sheet	60 of 70	Drawn By BF



DEBUG AND STATUS LEDS



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

```
Title:      SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM
DEBUG AND STATUS LEDS
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Date: 8-1-2008_15:08

Ver:	C
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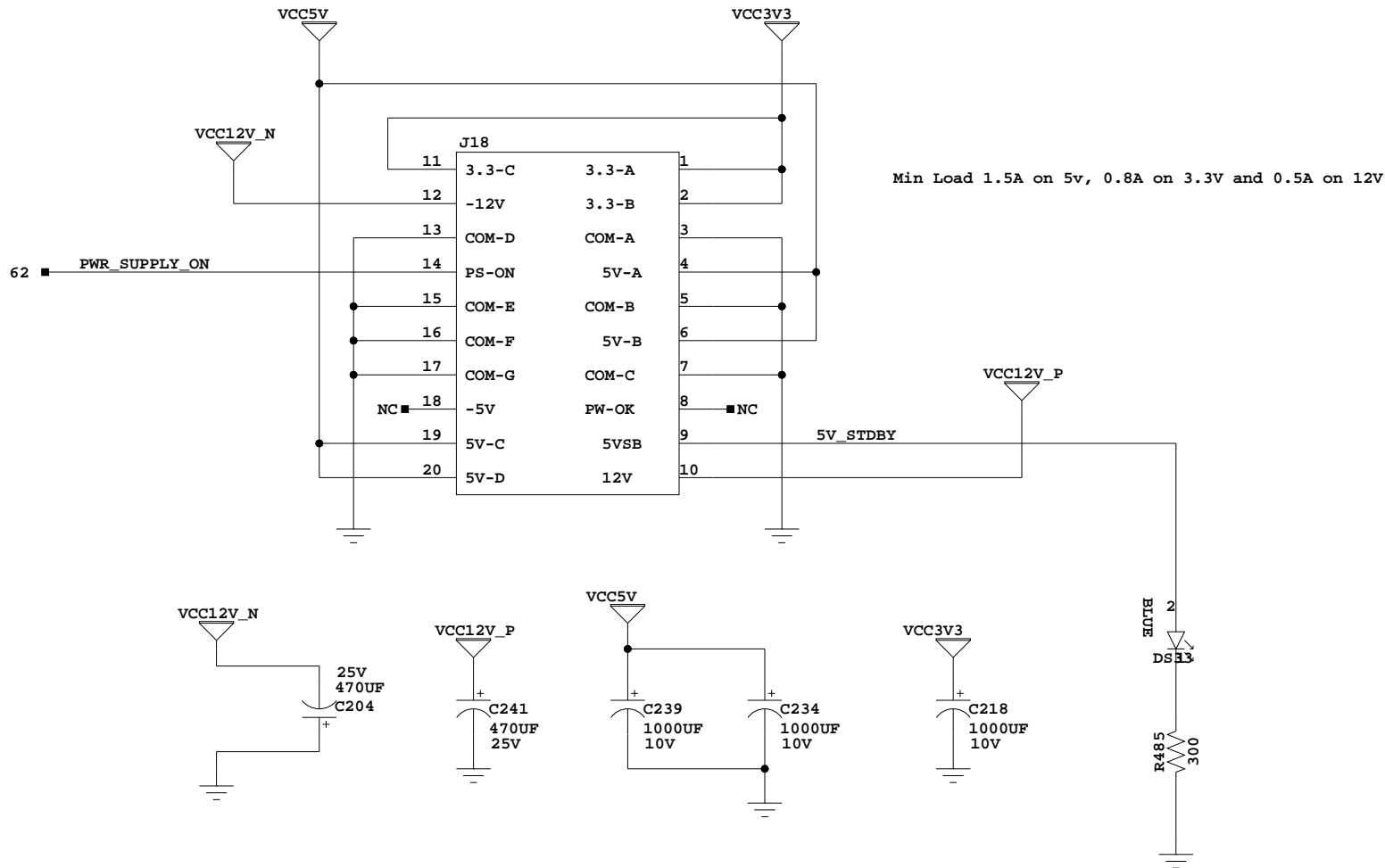
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Rev:	01
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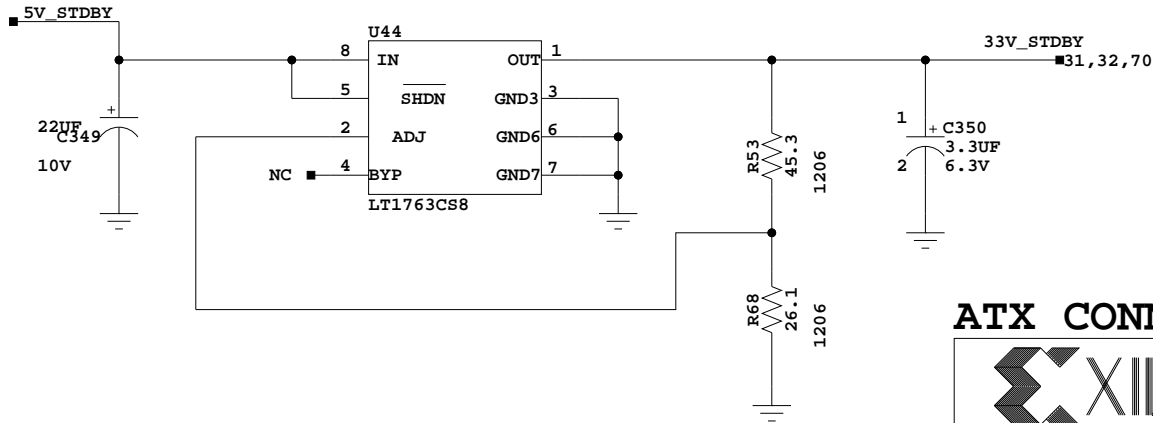
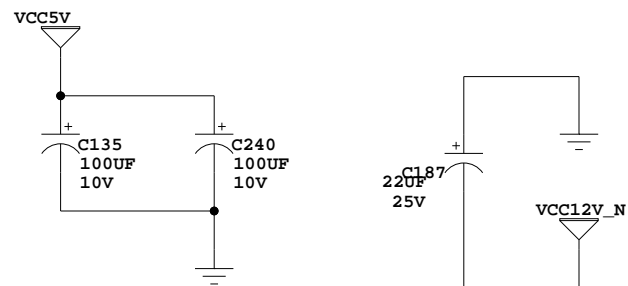
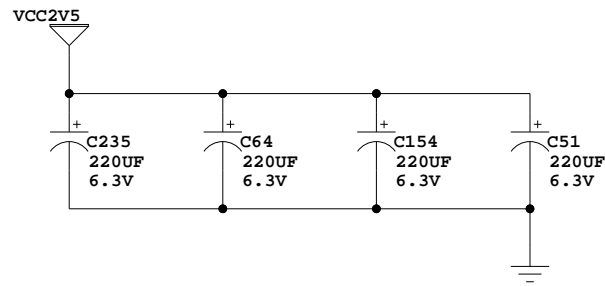
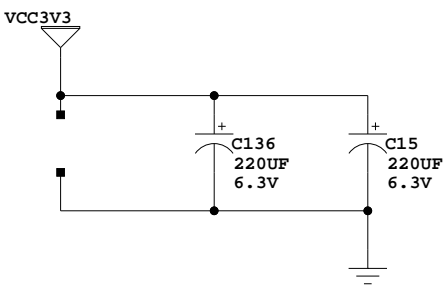
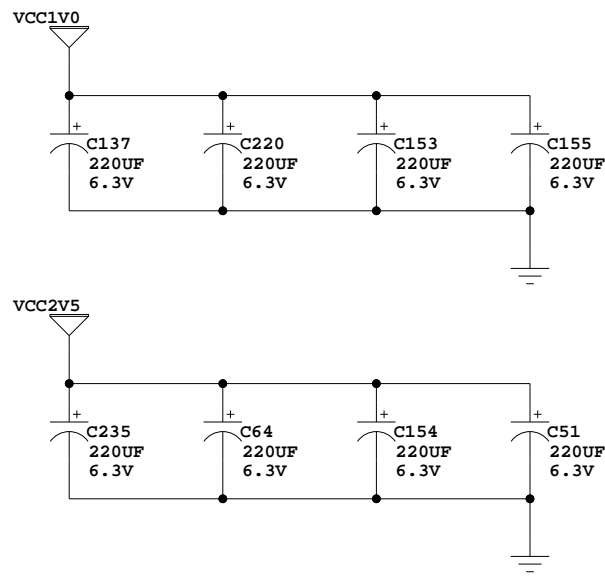
Sheet

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Drawn By
BF

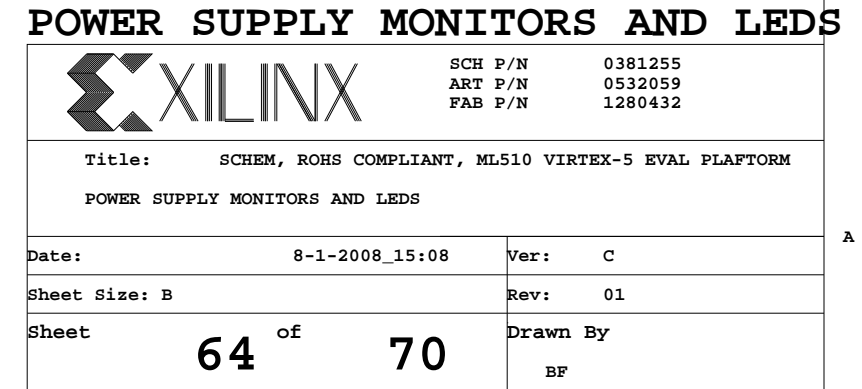


ATX Power Connector

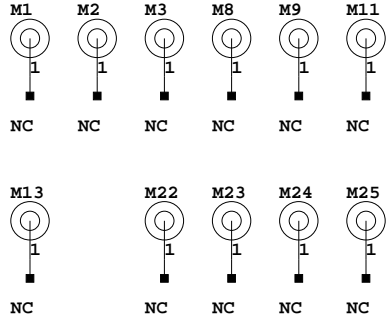
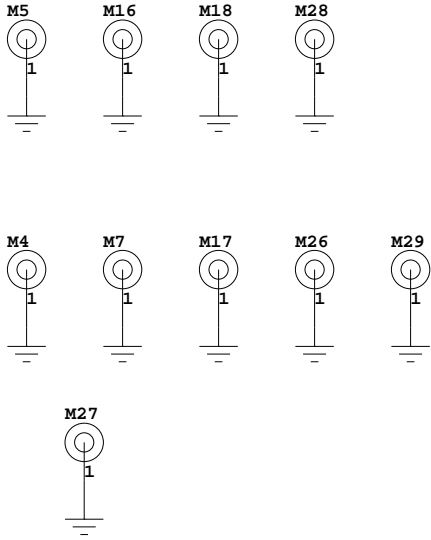


ATX CONNECTOR, PWR TOGGLE

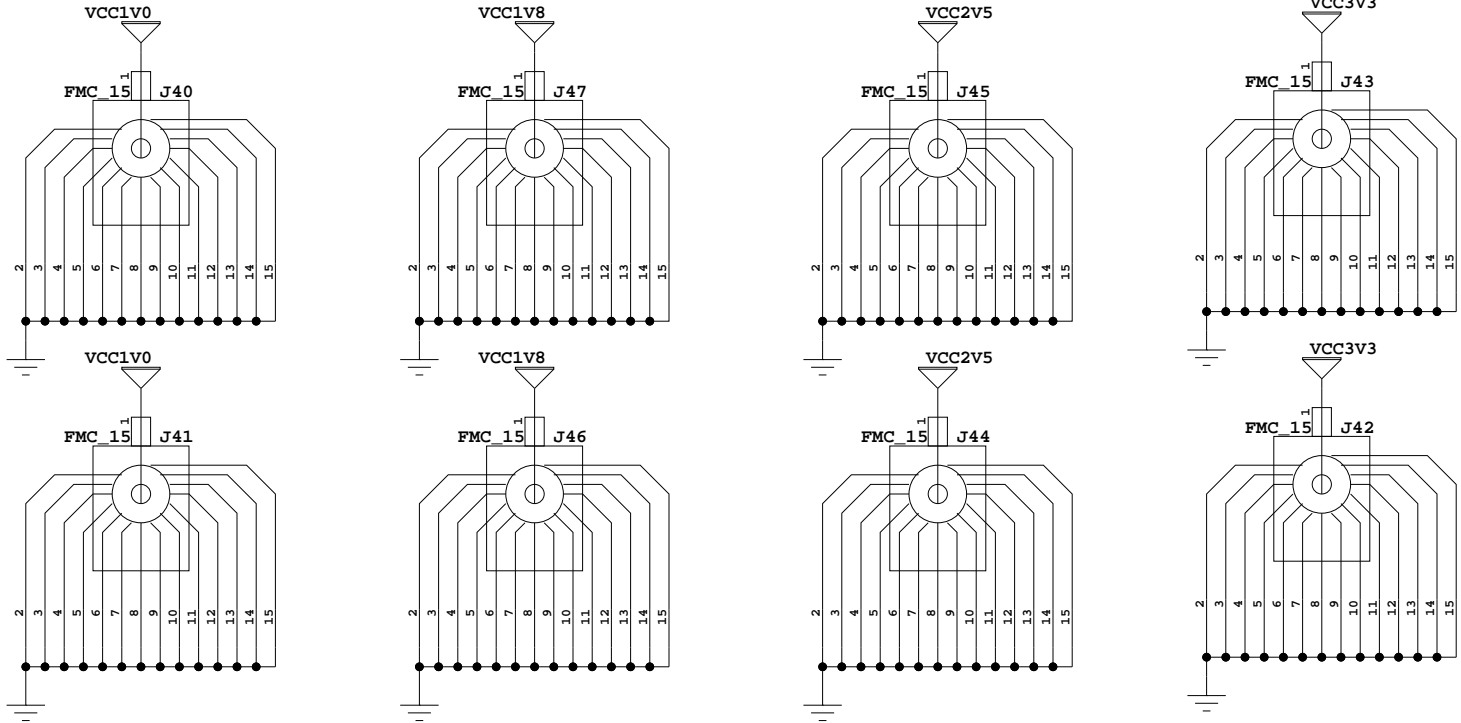
		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM ATX CONNECTOR, PWR TOGGLE AND HEADER			
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	63 of 70	Drawn By	BF



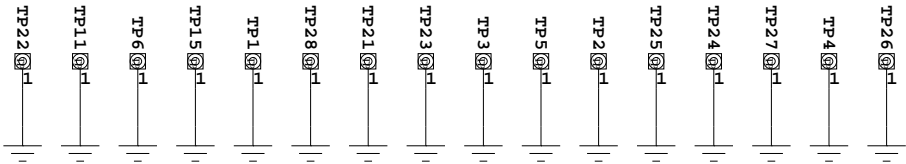
Mounting holes for ATX Form Factor



FMC connectors for power supply testing



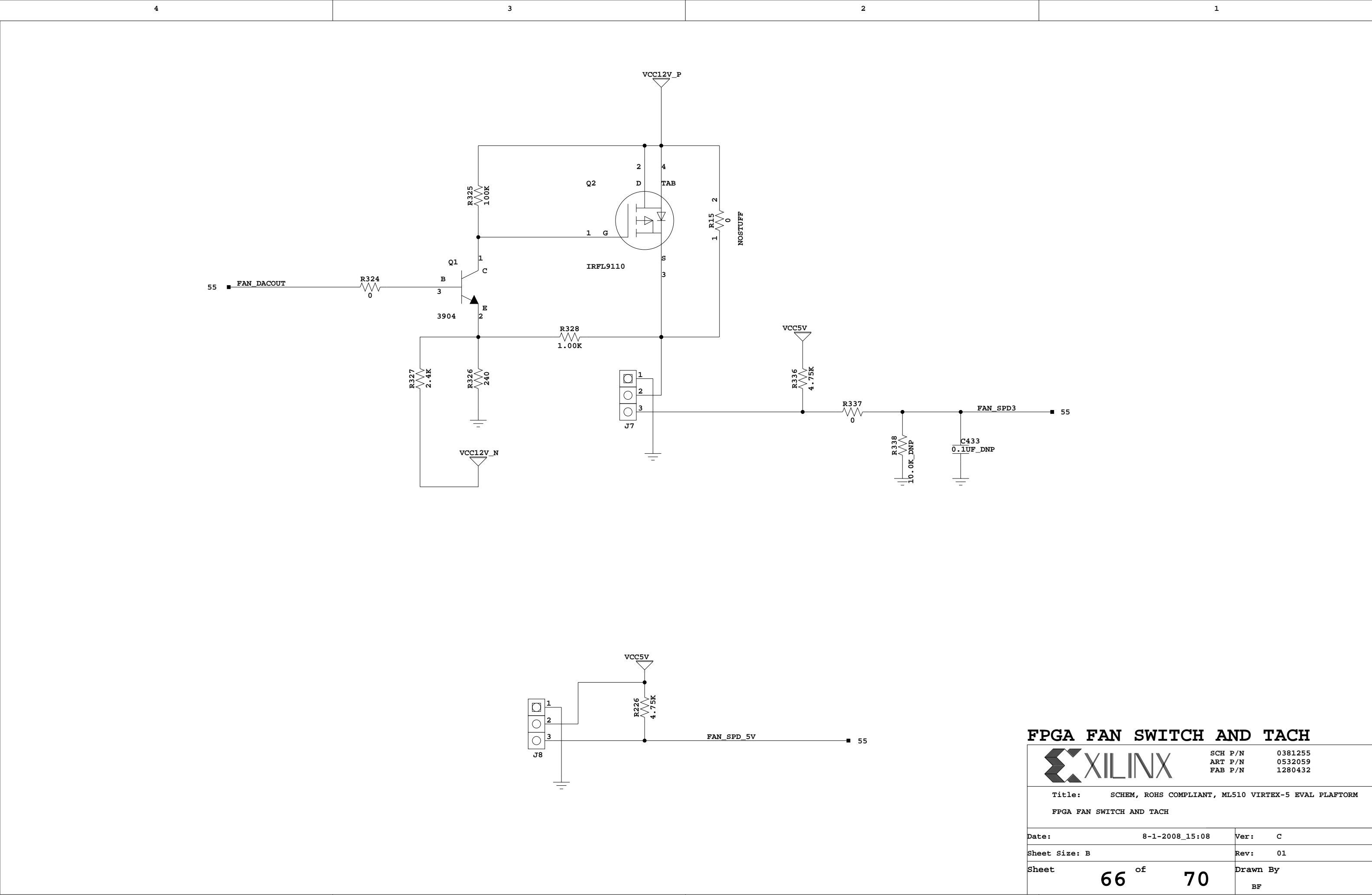
Spread out on the board.




Silkscreen:
"GND"

ATX MOUNTING HOLES / TEST POINTS

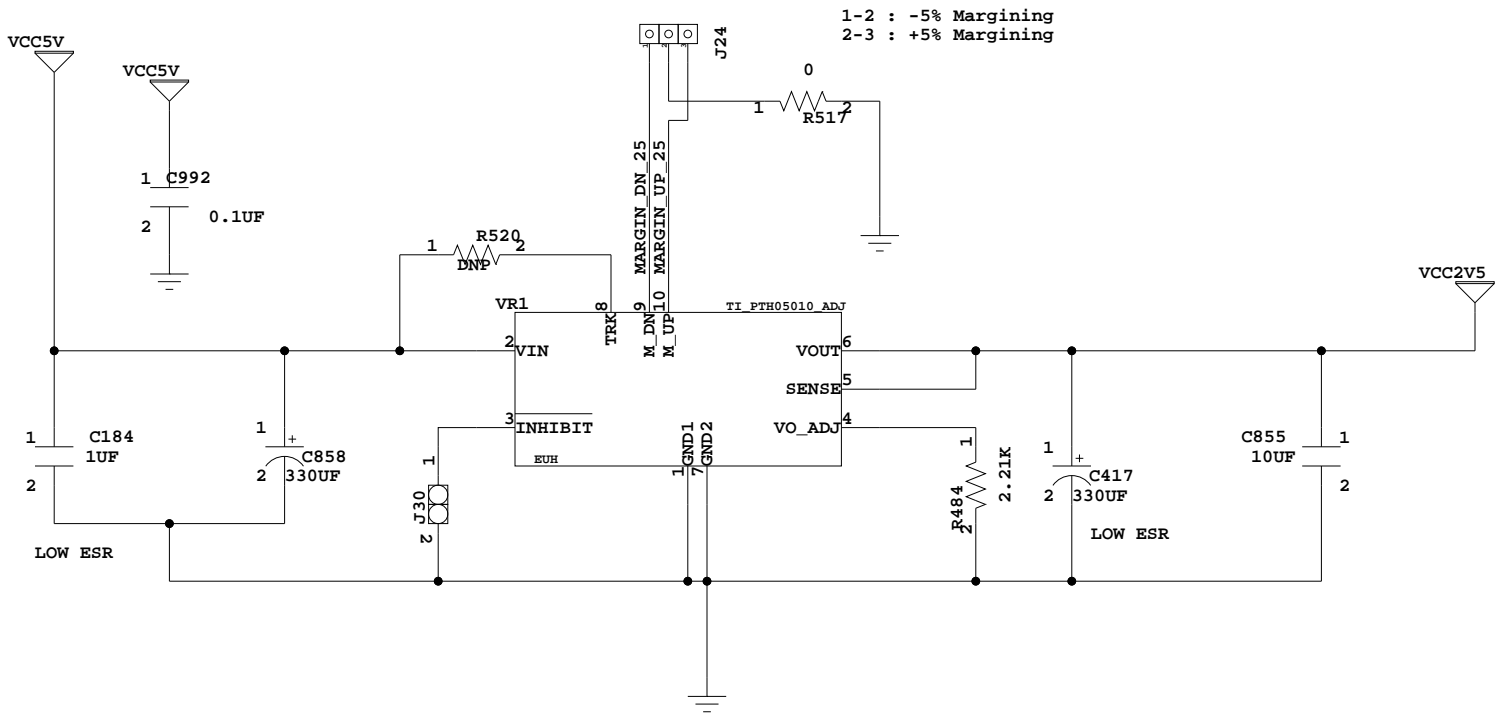
	SCH P/N	0381255
	ART P/N	0532059
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFORM ATX MOUNTING HOLES AND TEST POINTS	FAB P/N	1280432
Date: 8-1-2008_15:08	Ver: C	
Sheet Size: B	Rev: 01	
Sheet 65 of 70	Drawn By BF	



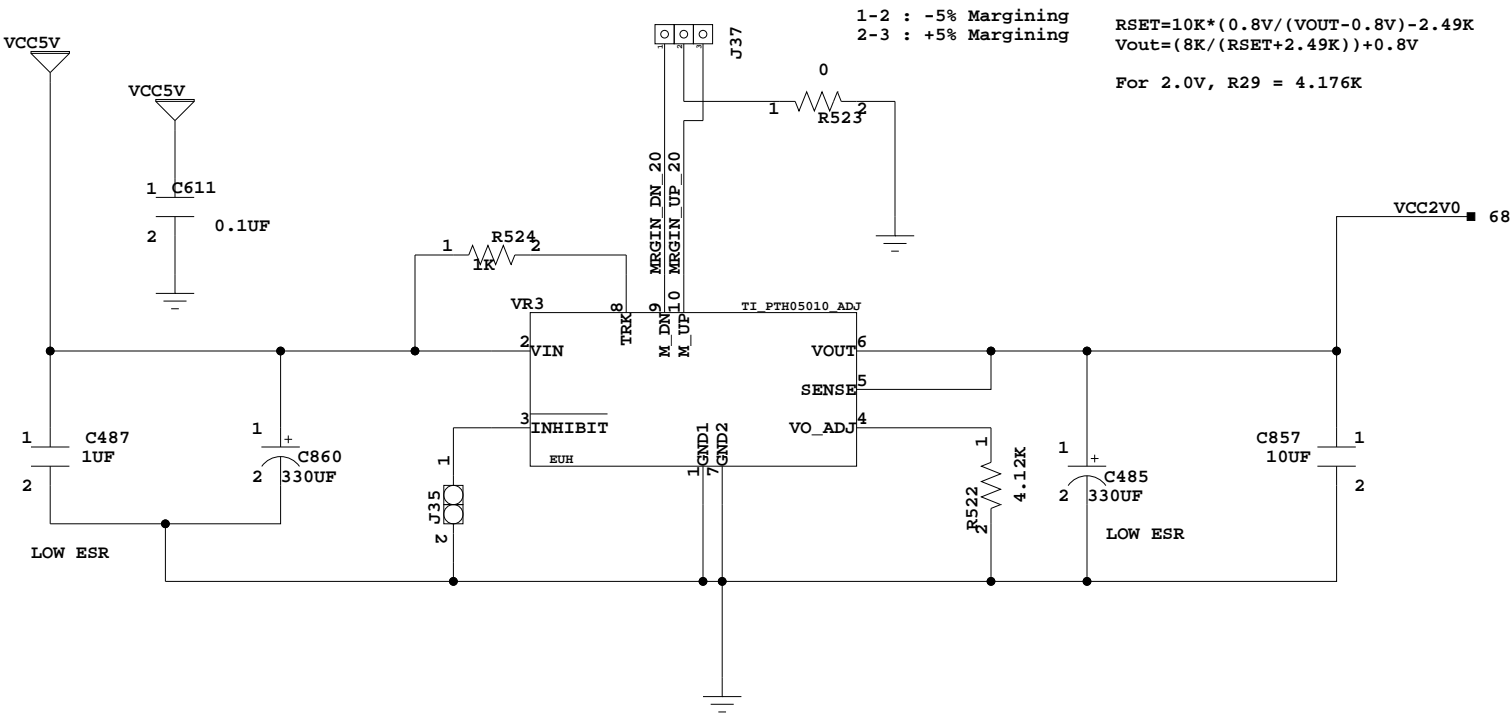
FPGA FAN SWITCH AND TACH

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM FPGA FAN SWITCH AND TACH		
Date:	8-1-2008_15:08	Ver: C
Sheet Size: B		Rev: 01
Sheet	66 of 70	Drawn By BF

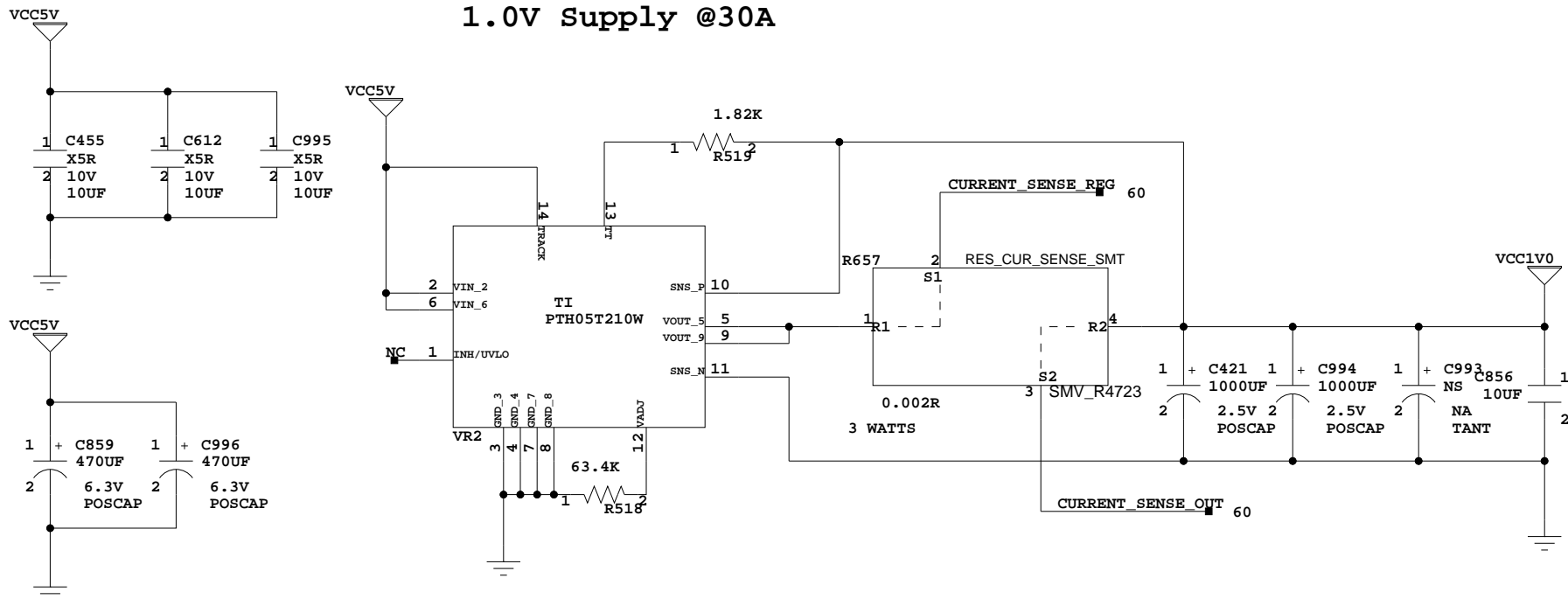
2.5V Supply @15A



2.0V Supply @15A

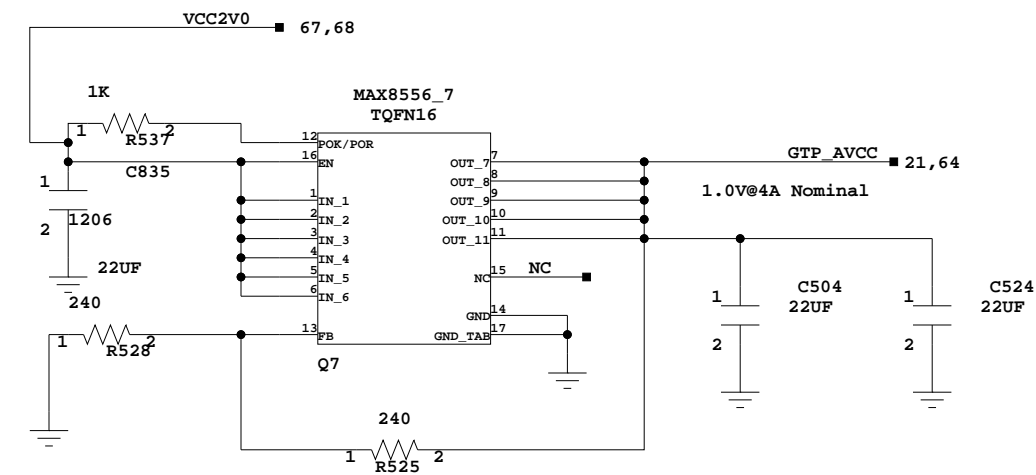
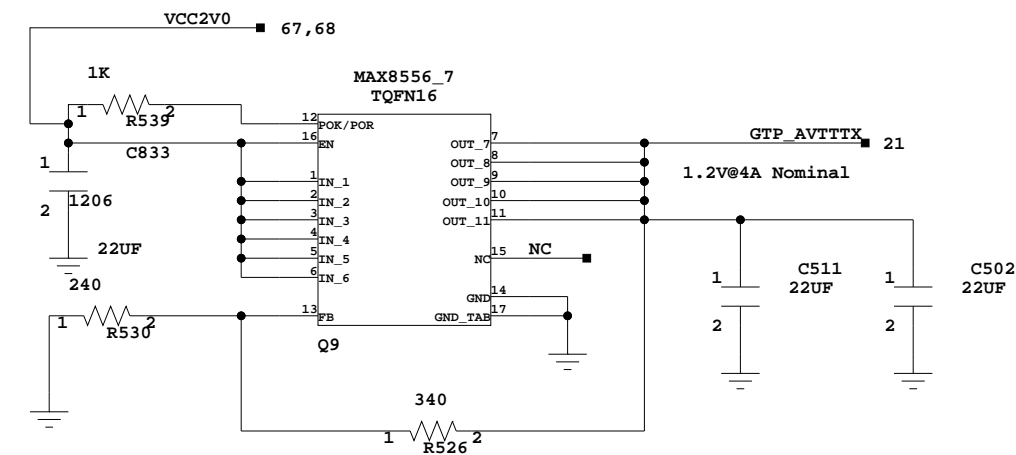
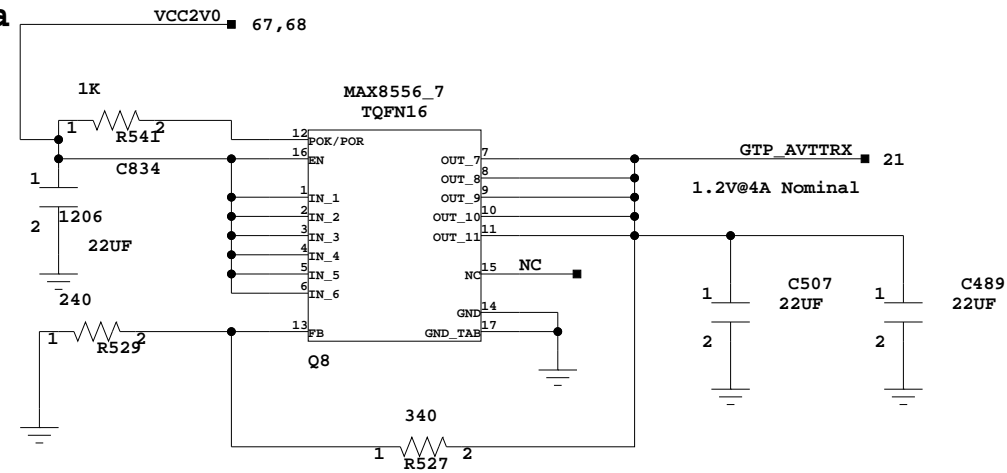
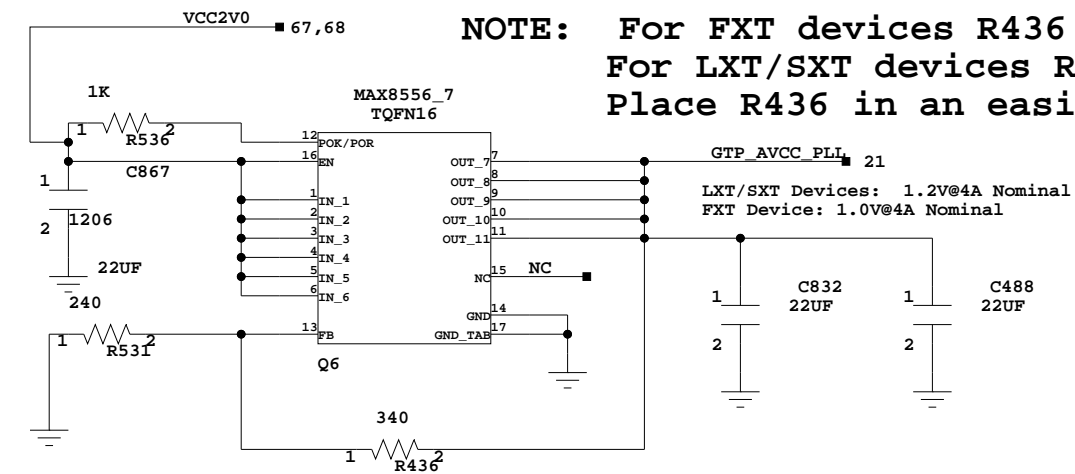


1.0V Supply @30A



FPGA CORE AND IO VOLTAGE

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM FPGA CORE AND IO VOLTAGE		
Date:	8-1-2008_15:08	Ver: C
Sheet Size: B		Rev: 01
Sheet	67 of 70	Drawn By BF



$$R2 = R1 * \{(Vout/0.5) - 1\}$$

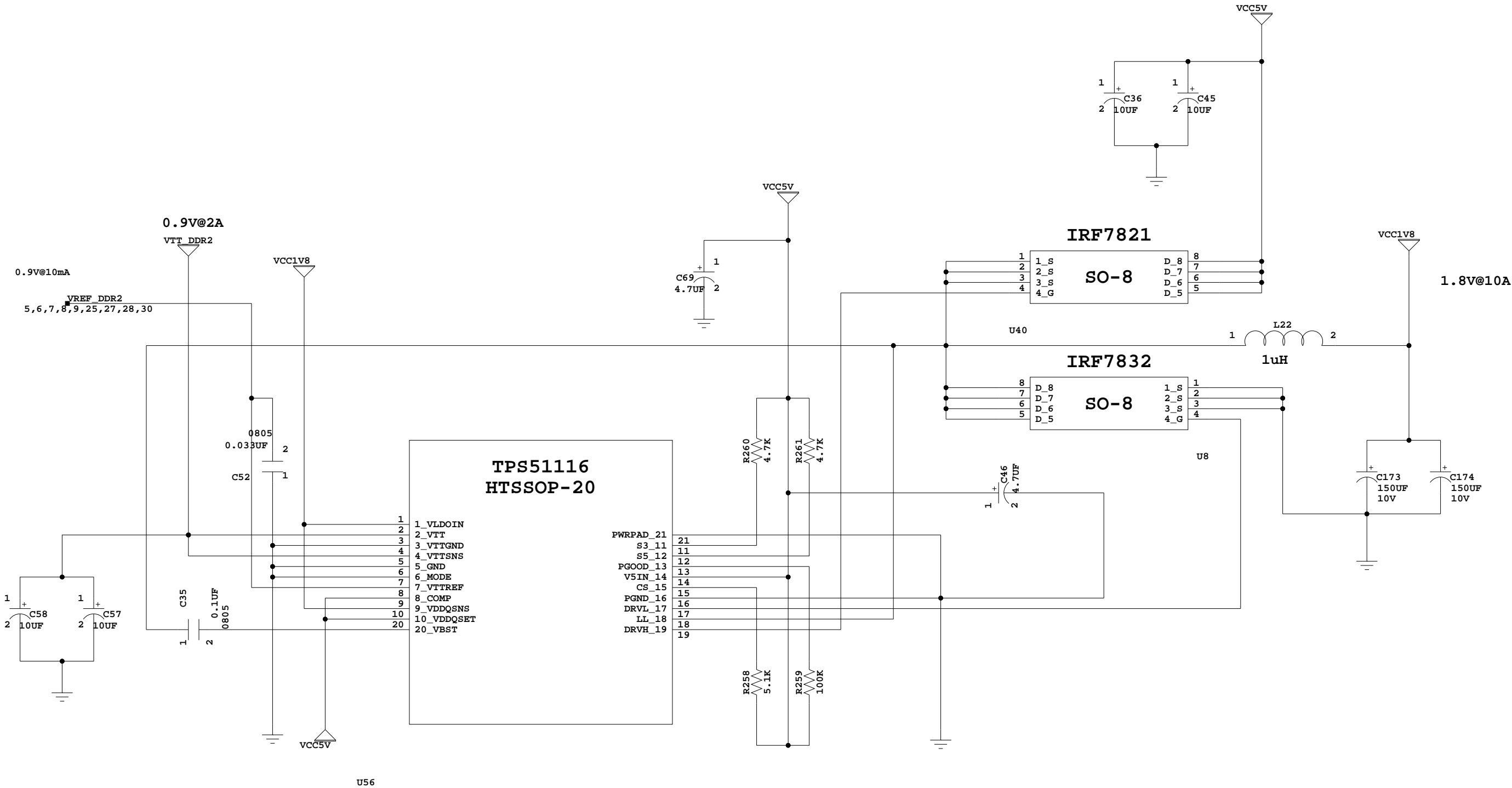
GTP POWER SUPPLIES



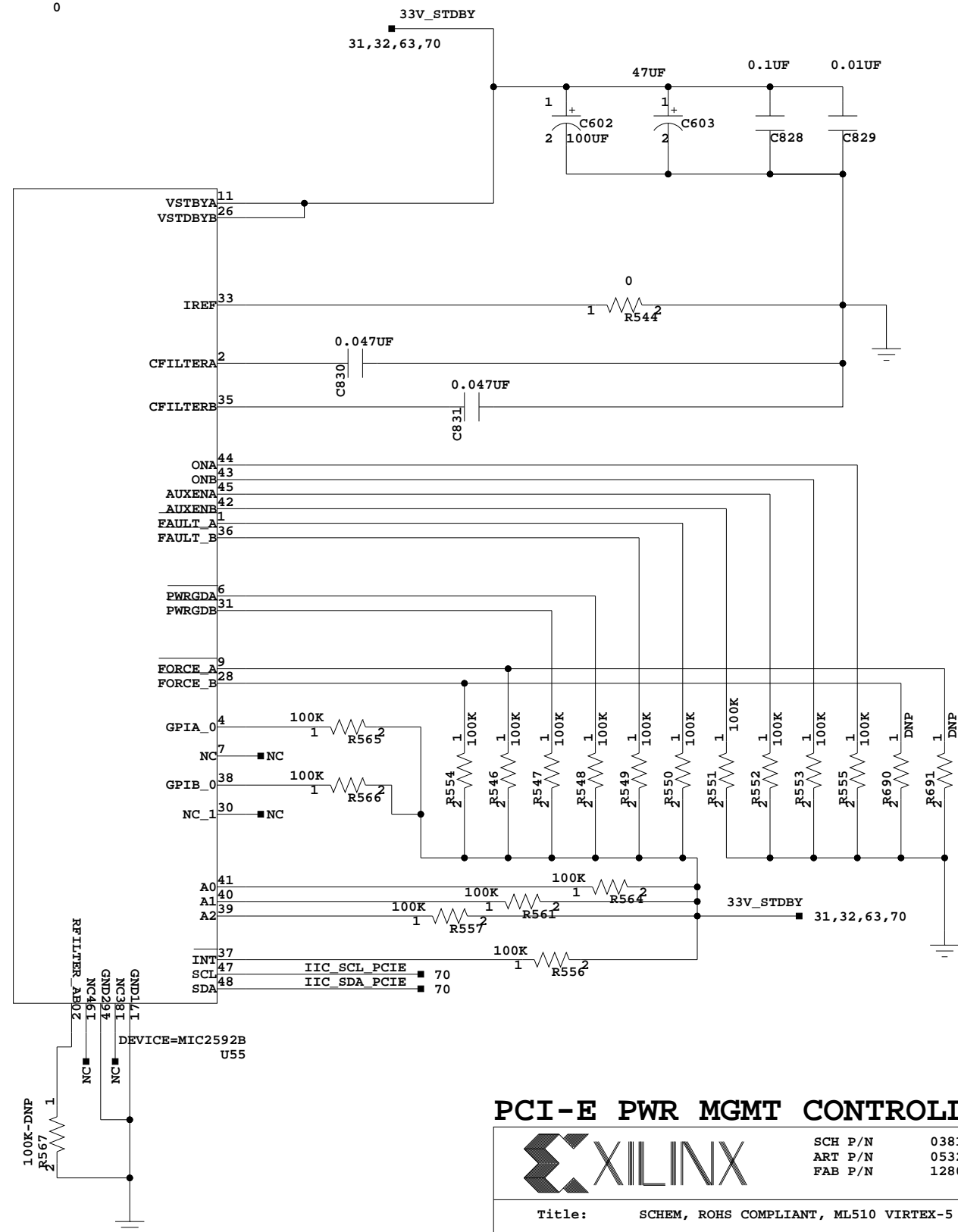
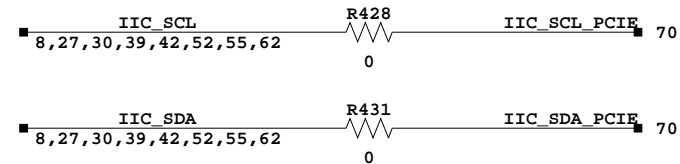
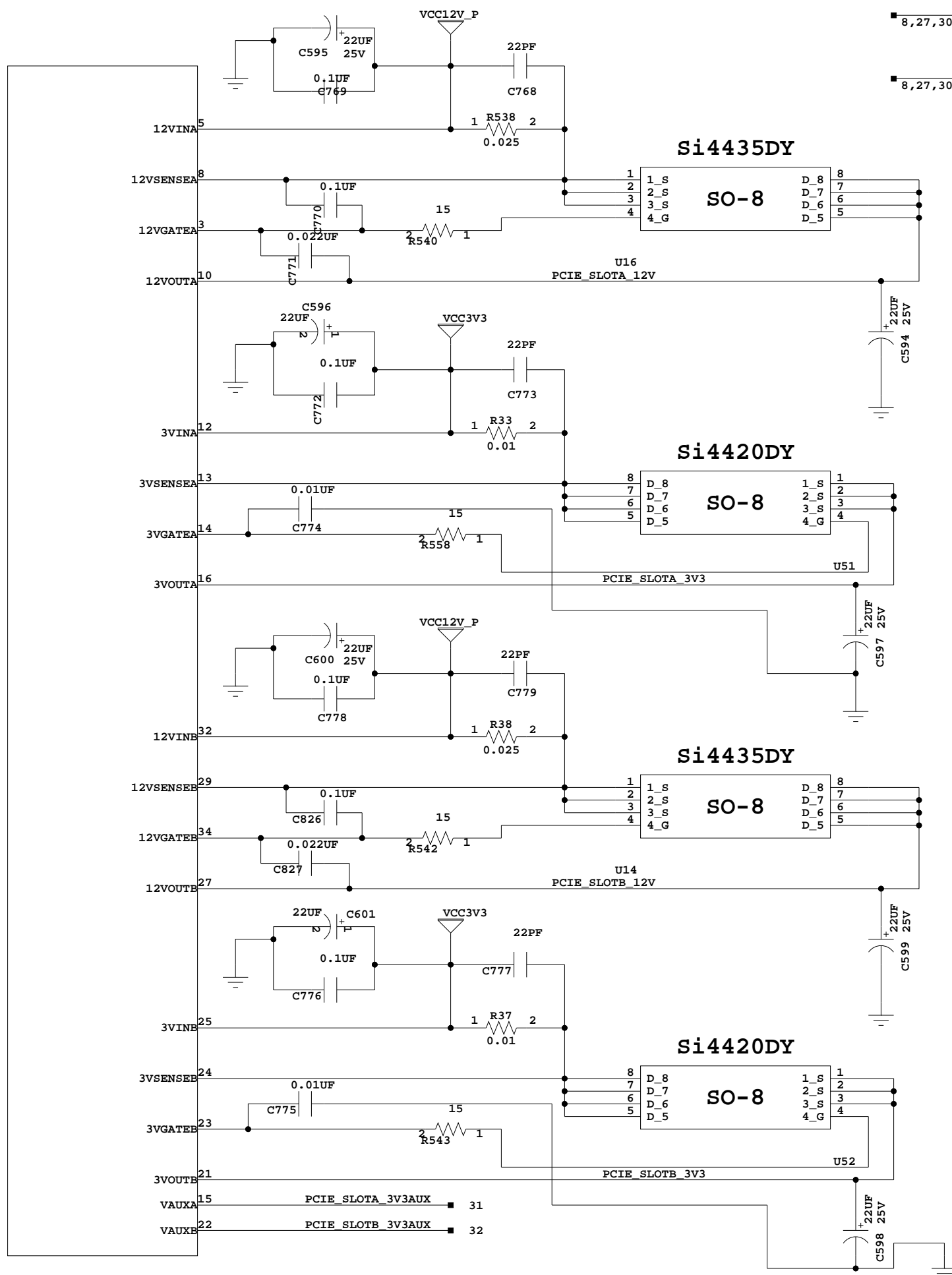
SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM
GTP POWER SUPPLIES

Date:	8-1-2008_15:08	Ver:	C
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DDR2 POWER SUPPLY		
<div><div></div><div>XILINX</div></div>		
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFORM DDR2 POWER SUPPLY		
Date: 8-1-2008_15:08	Ver: C	SCH P/N 0381255 ART P/N 0532059 FAB P/N 1280432
Sheet Size: B	Rev: 01	
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PCI-E PWR MGMT CONTROLLER



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI-E PWR MGMT CONTROLLER

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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