

| Spartan-3 Evaluation Board |              |
|----------------------------|--------------|
| Avnet Design Services      |              |
| www.em.avnet.com           |              |
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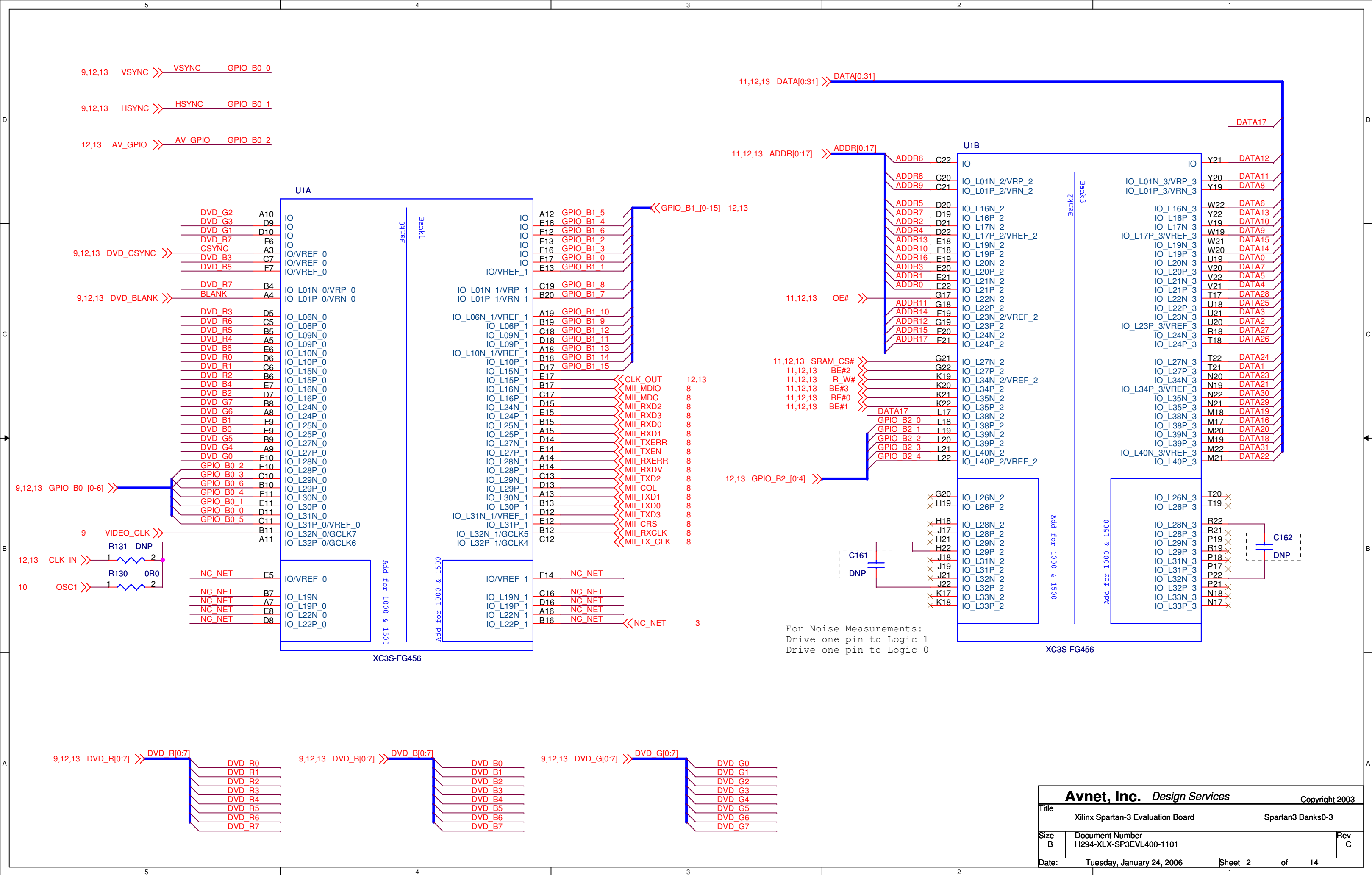
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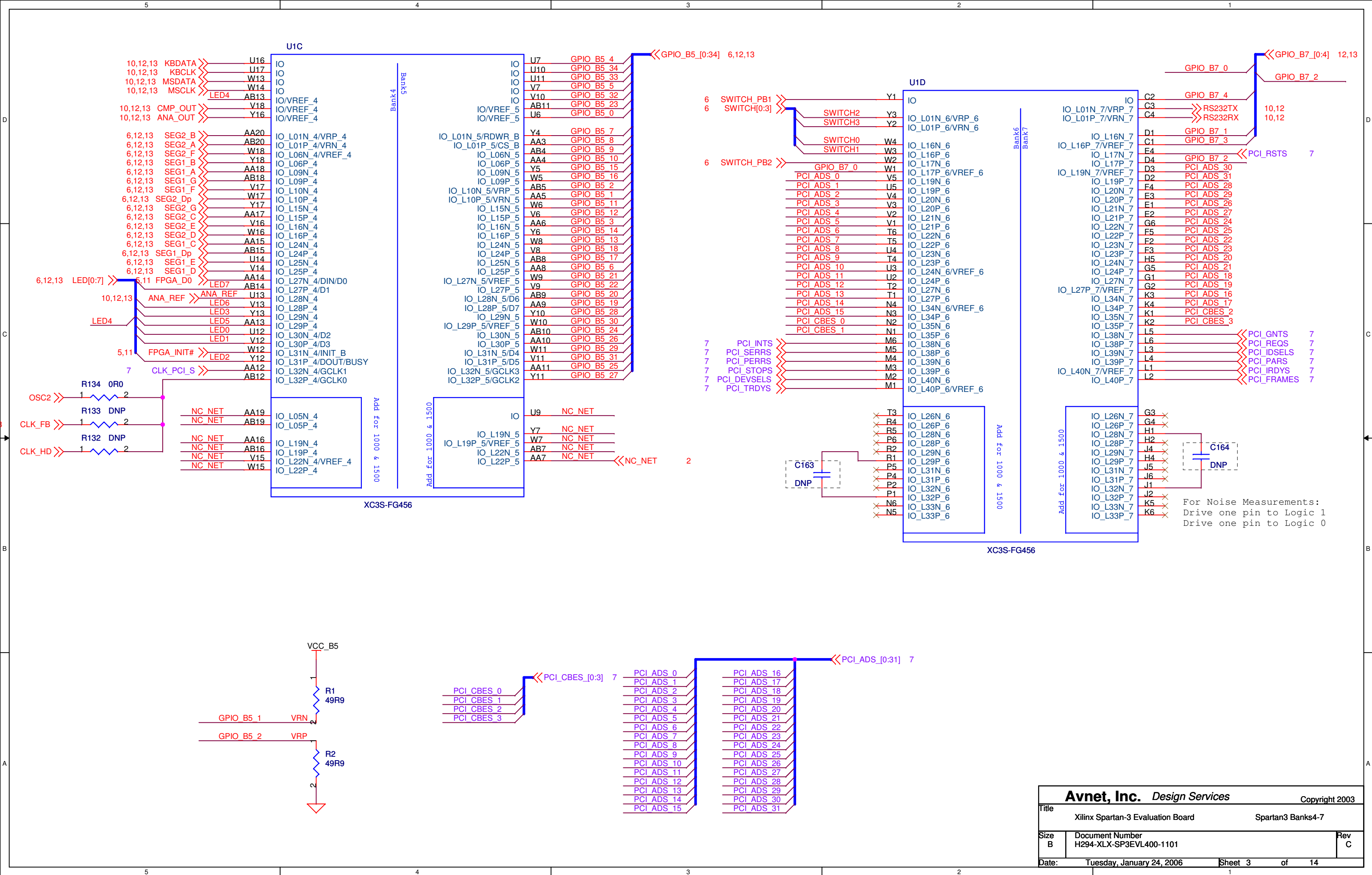
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| REV | SHEET | DESCRIPTION                                       | DATE    |
|-----|-------|---|---------|
| A   | ALL   | Prototype Release:                                | 27OCT03 |
| B   | ALL   | Production Release:                               |         |
| C   | ALL   | Production Release: Implemented XAPP646 & XAPP653 | 24JAN06 |

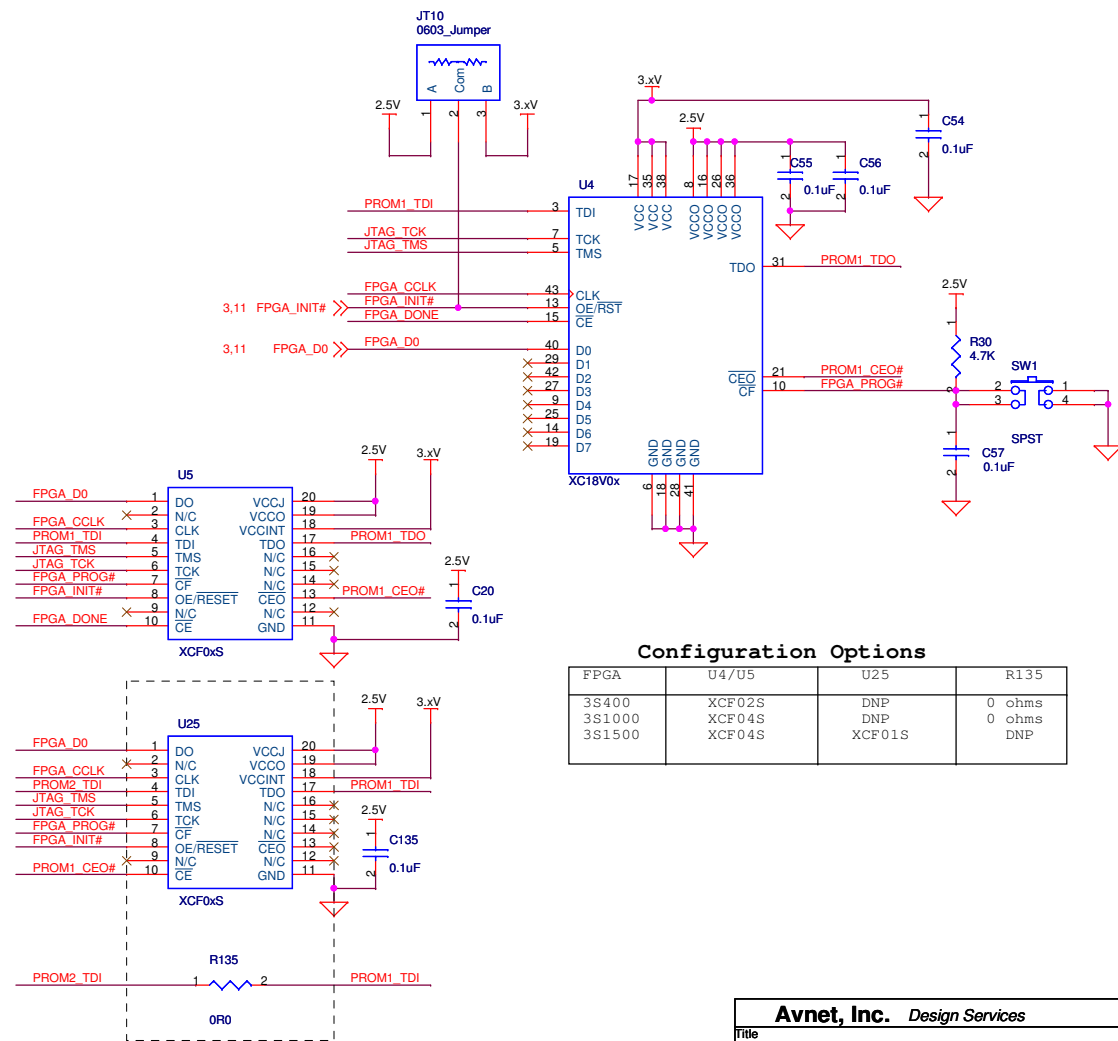
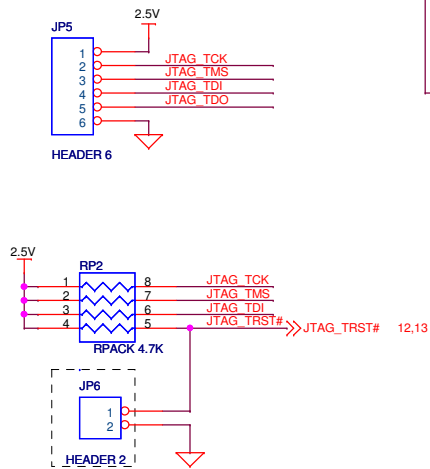
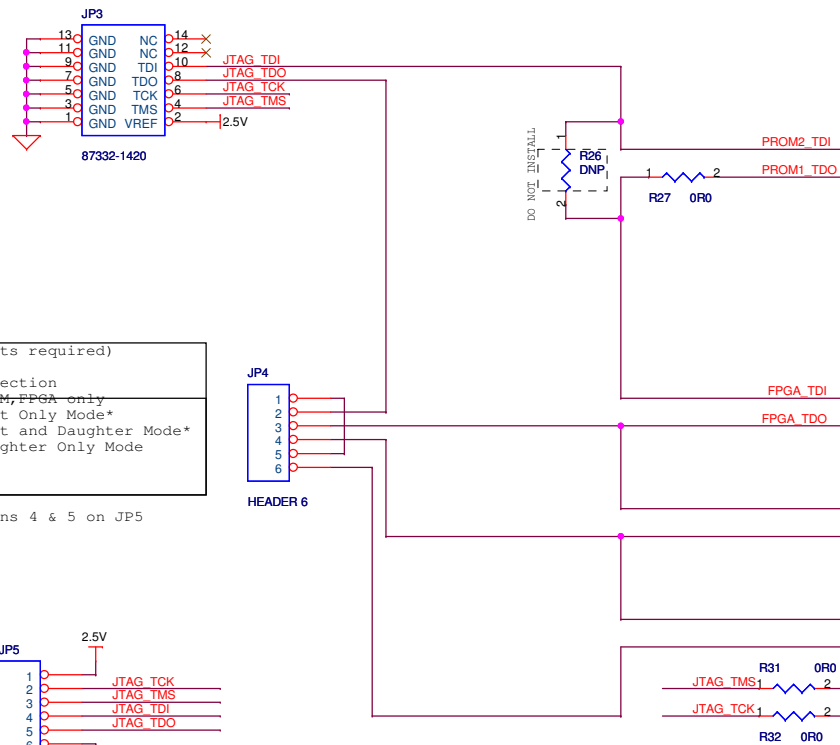
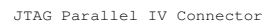
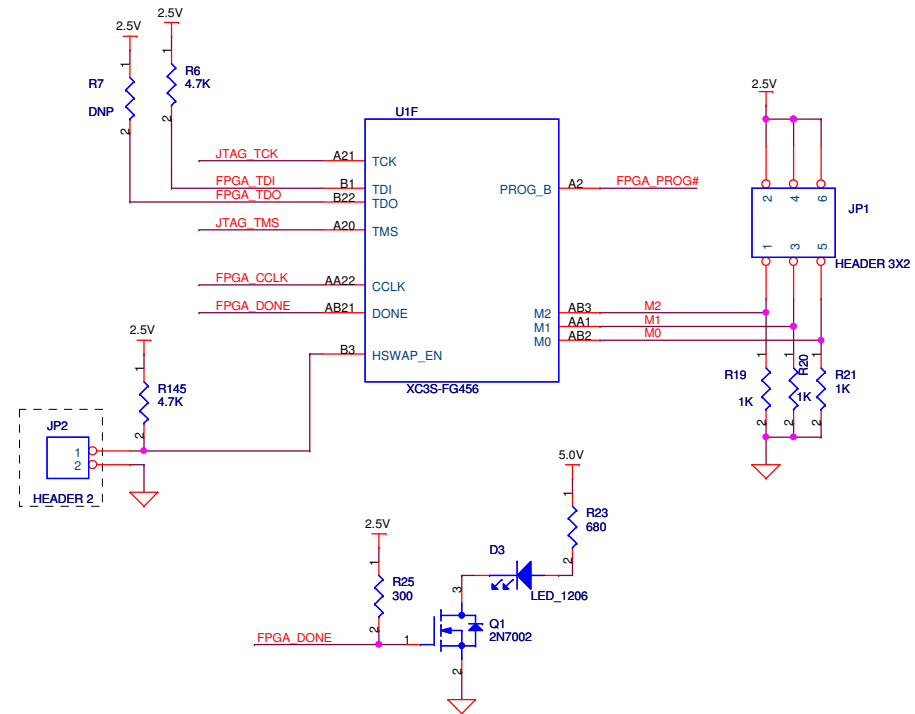
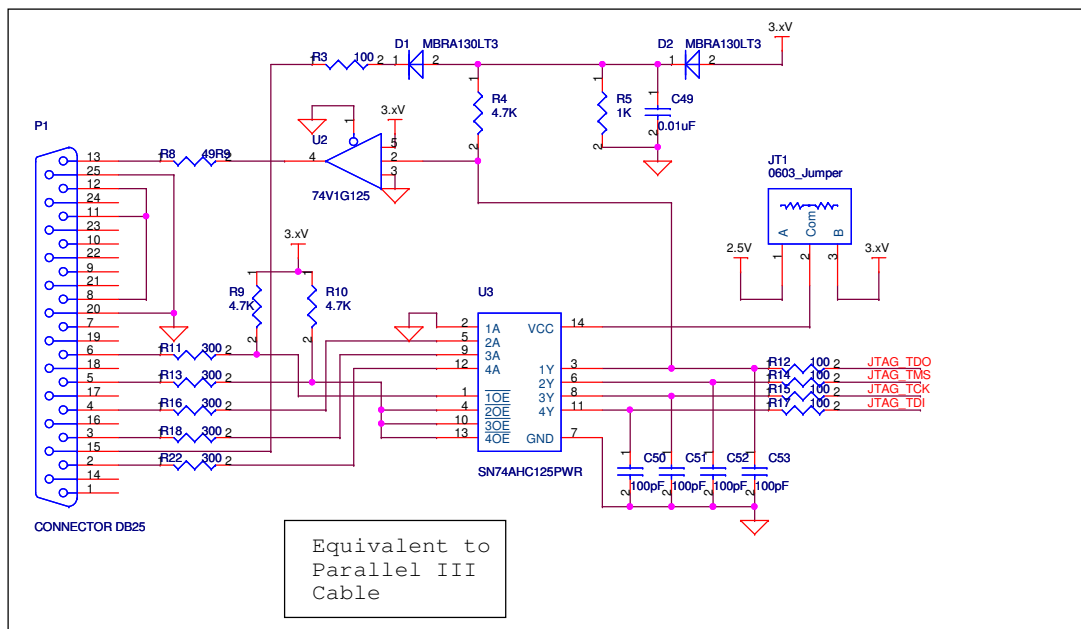


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|-----------------------------|--|--|----------------|
| Title                       |  | Xilinx Spartan3-400 Evaluation Board      Lead Sheet |                |
| Size<br>B                   | Document Number<br>H294-XLX-SP3EVL400-1101 |  | Rev<br>C       |
| Date:                       | Tuesday, January 24, 2006                  | Sheet 1  | of 14          |

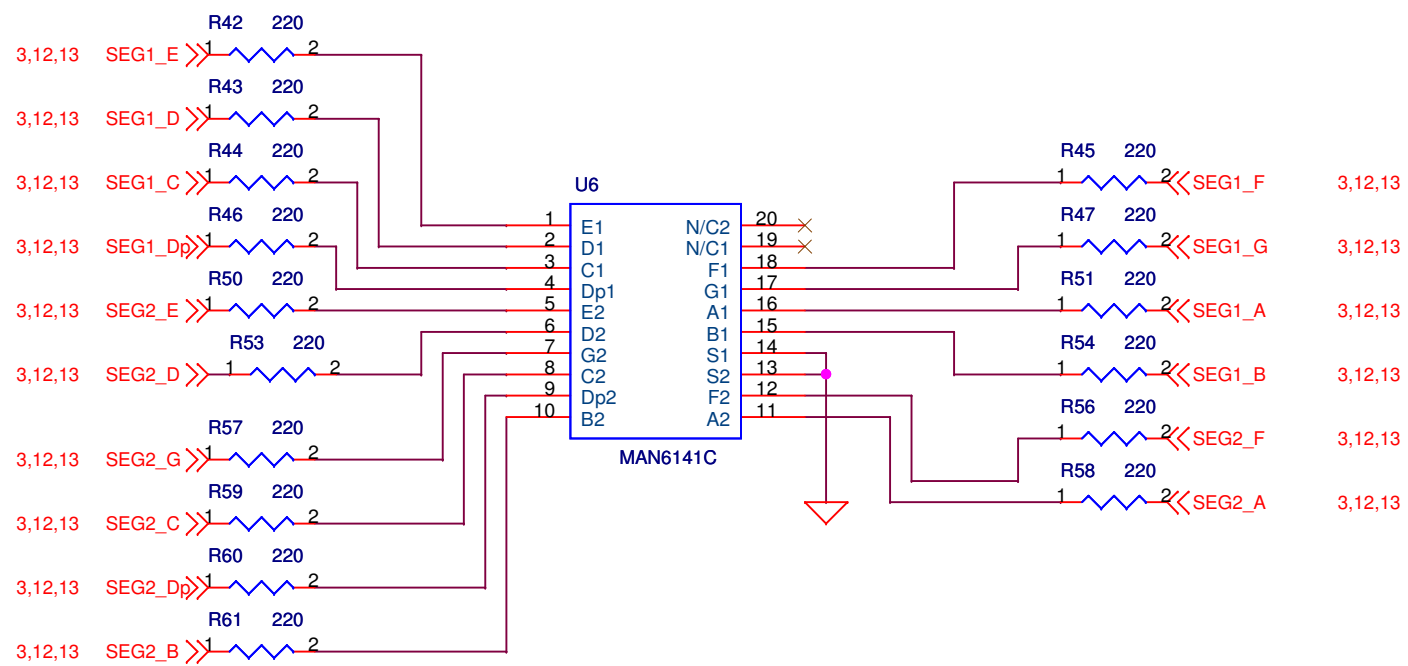
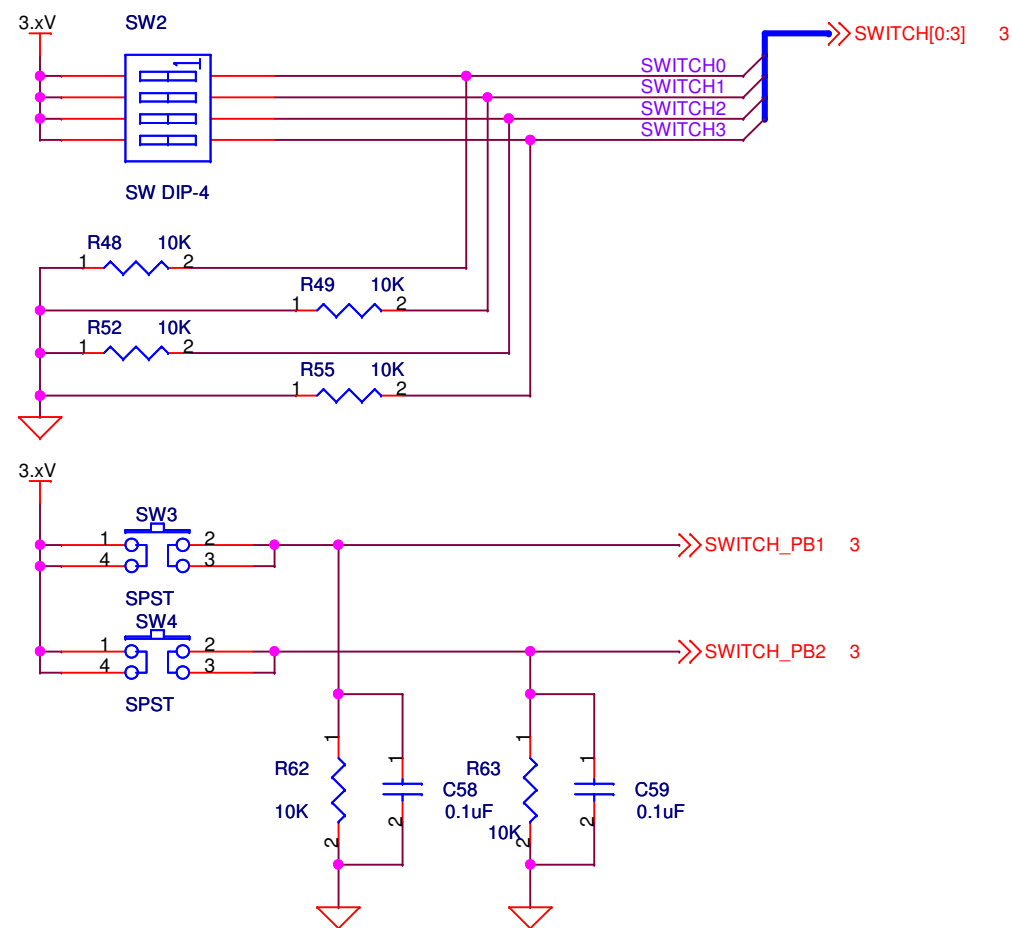
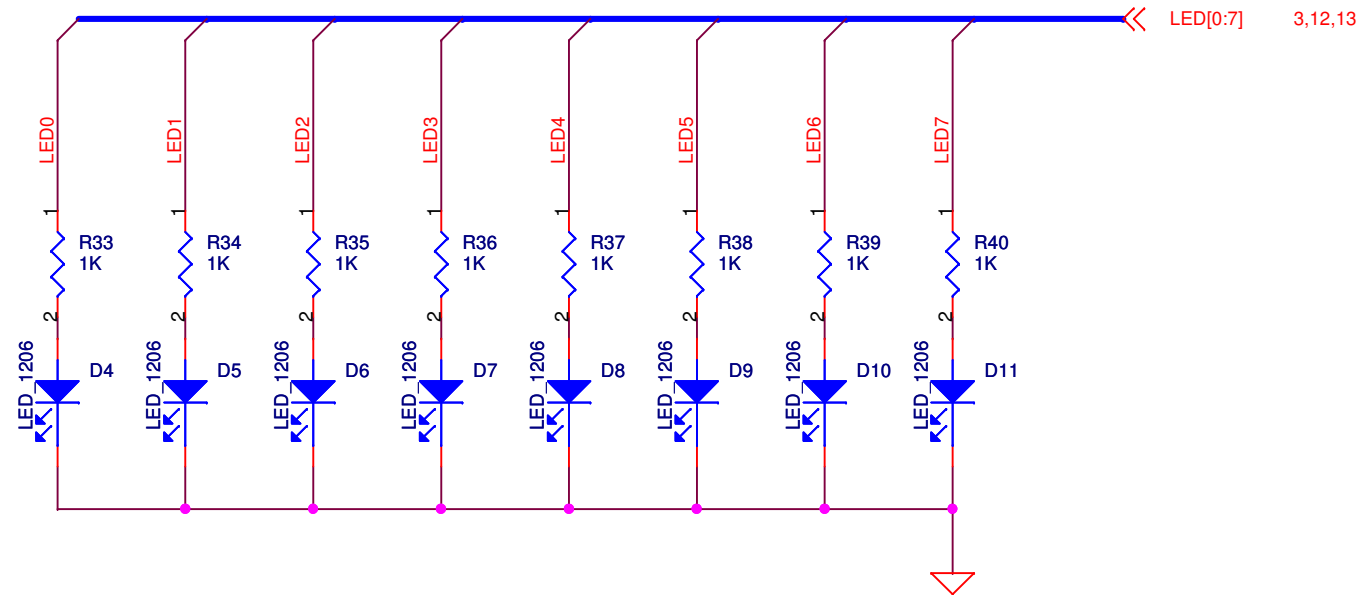
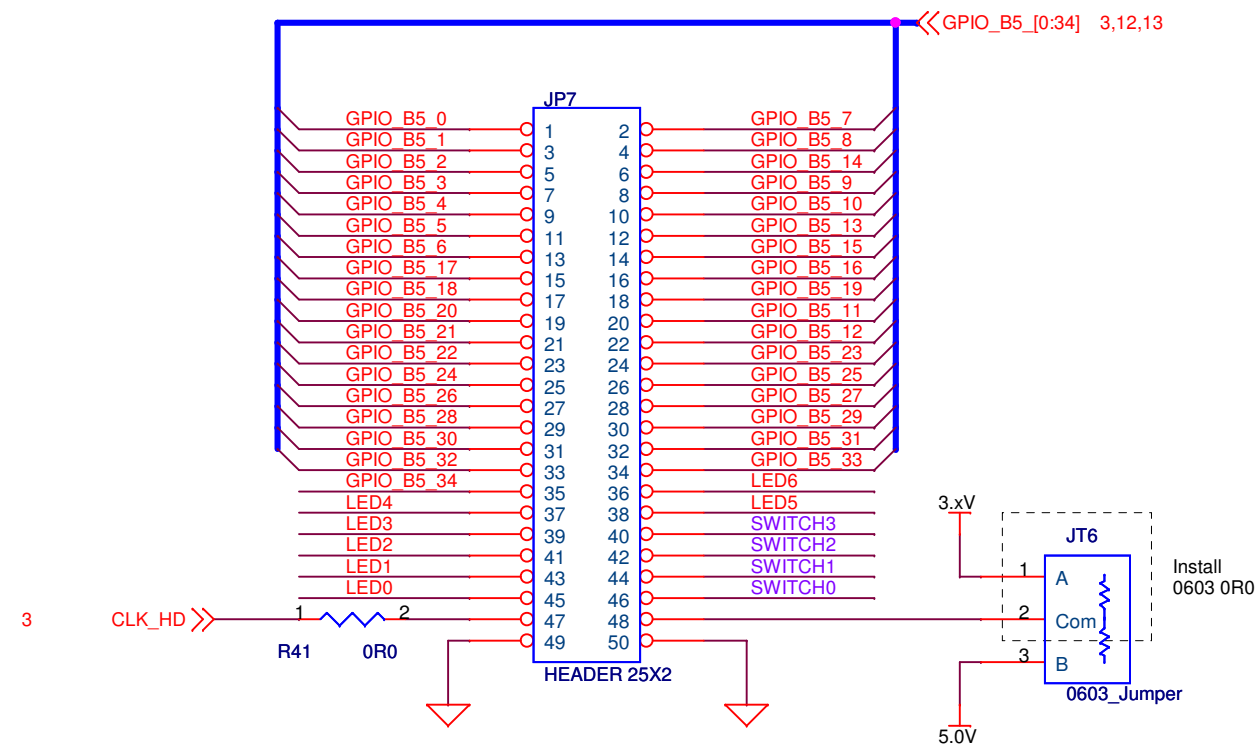




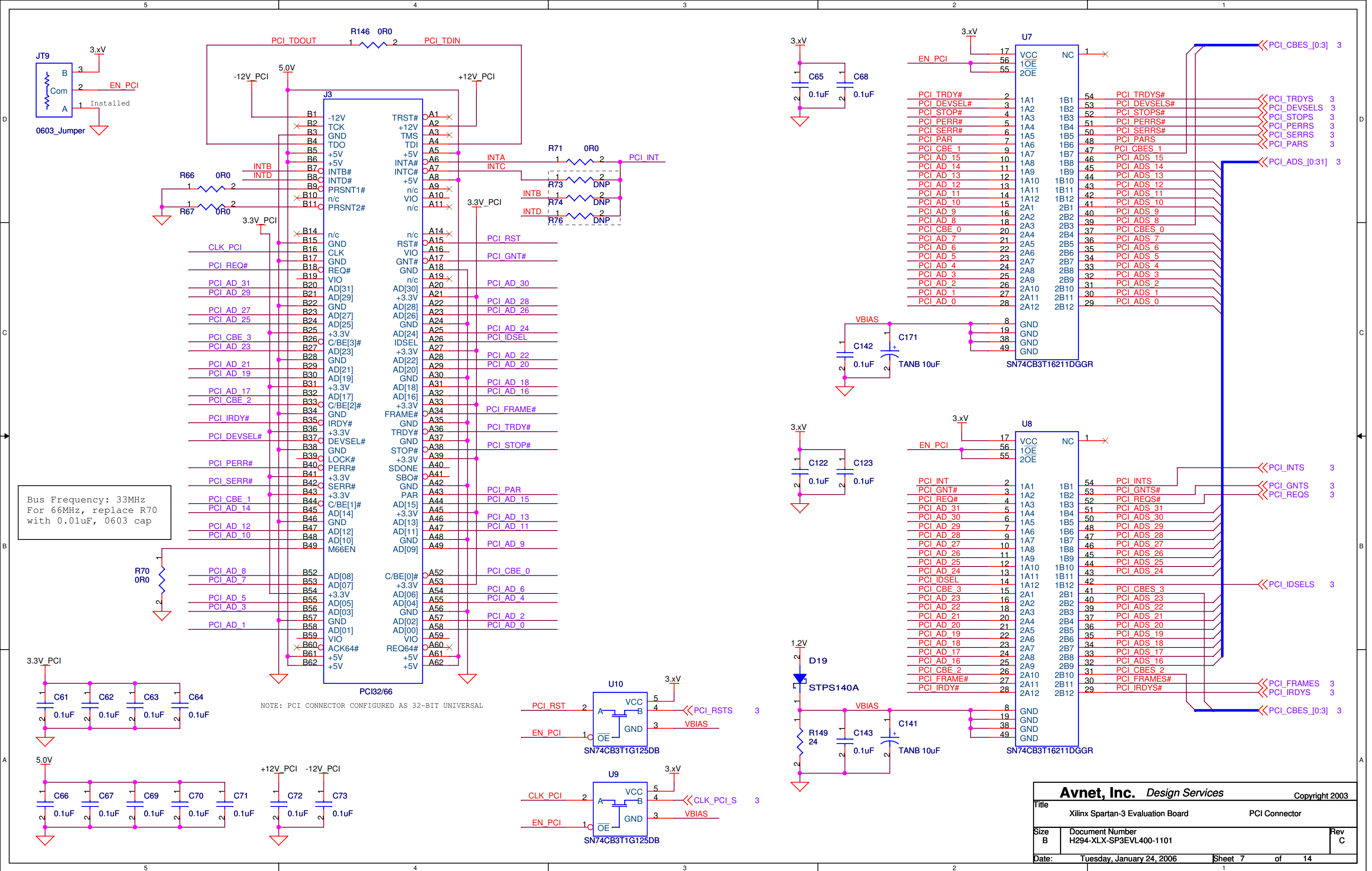


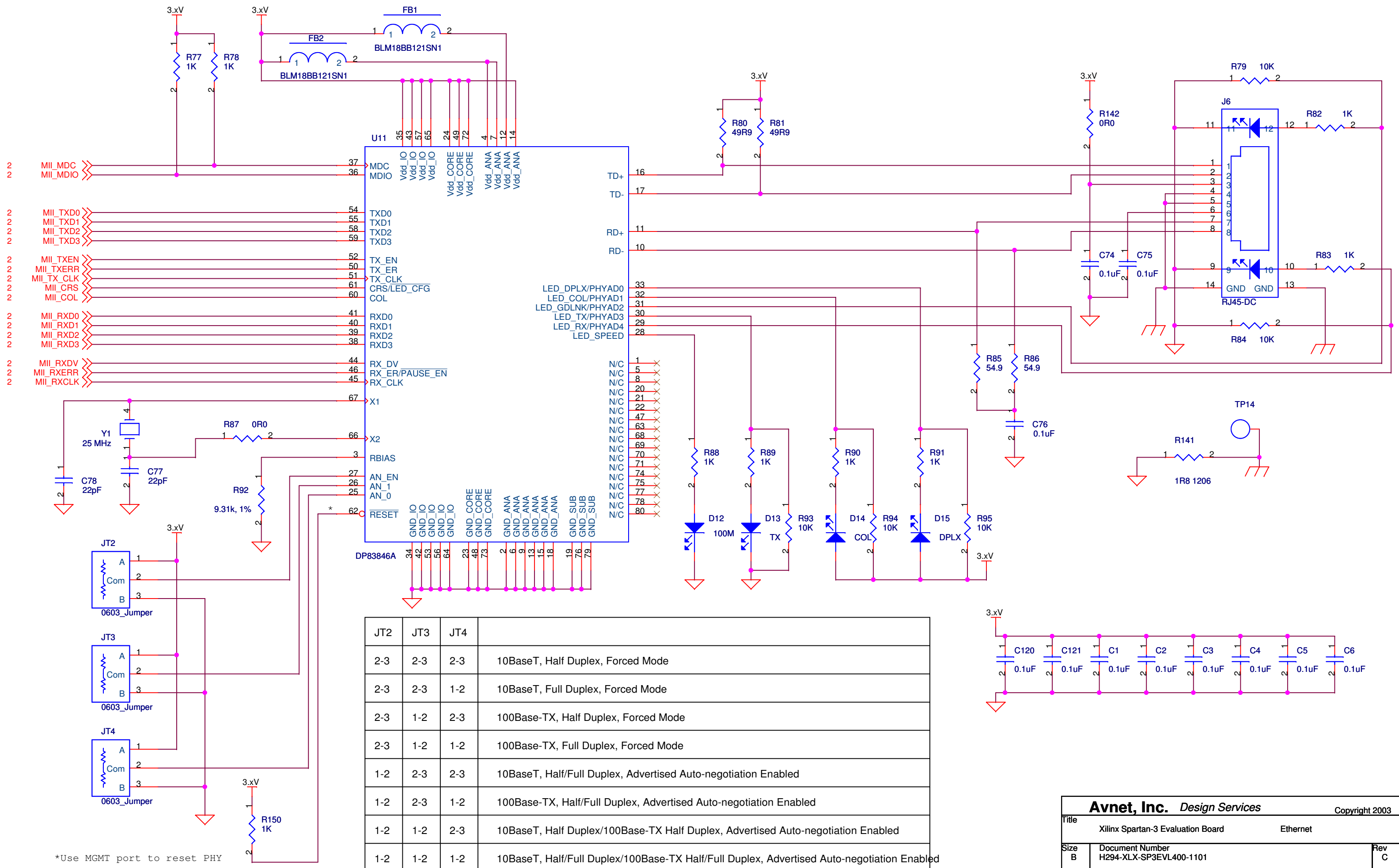


| Configuration Options |        |        |        |
|-----------------------|--------|--------|--------|
| FPGA                  | U4/U5  | U25    | R135   |
| 3S400                 | XCF02S | DNP    | 0 ohms |
| 3S1000                | XCF04S | DNP    | 0 ohms |
| 3S1500                | XCF04S | XCF01S | DNP    |





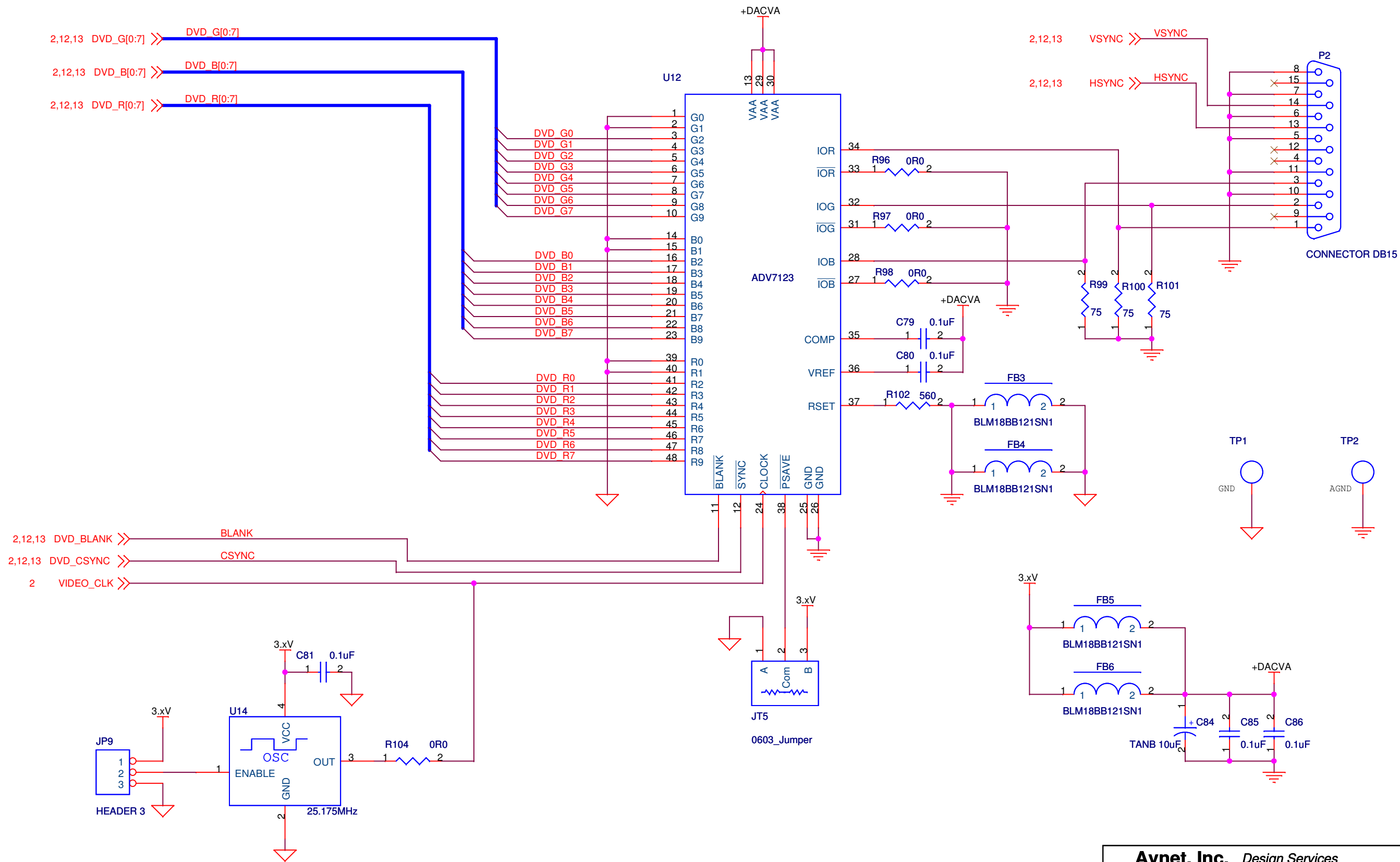




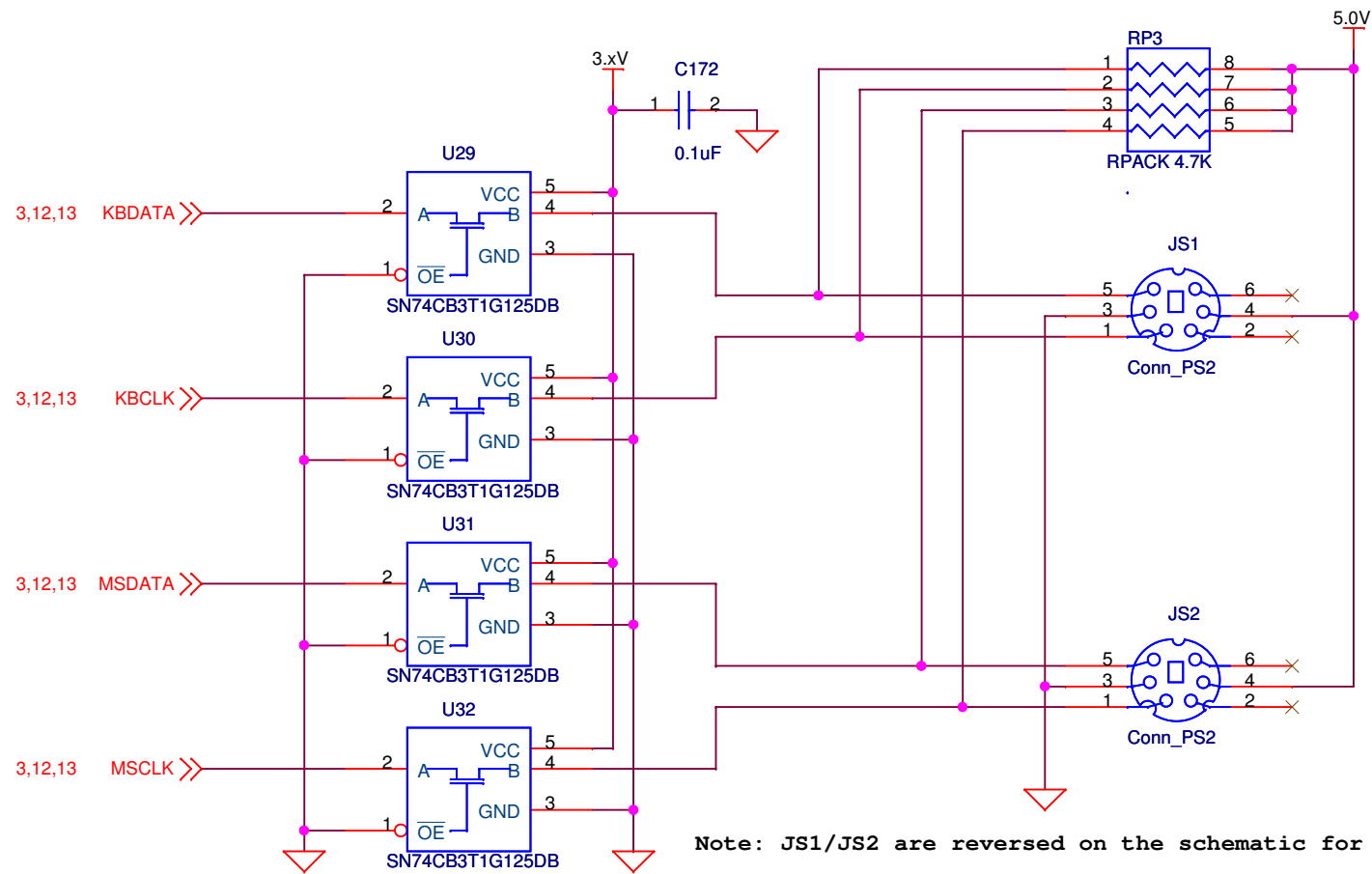
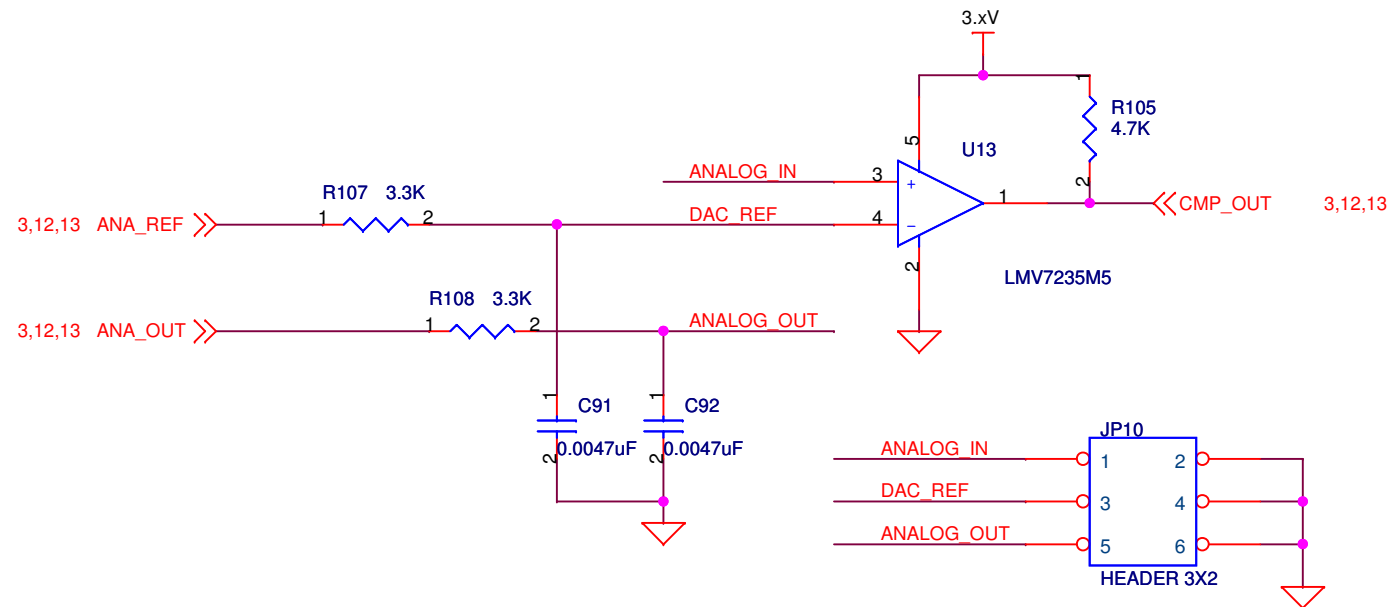
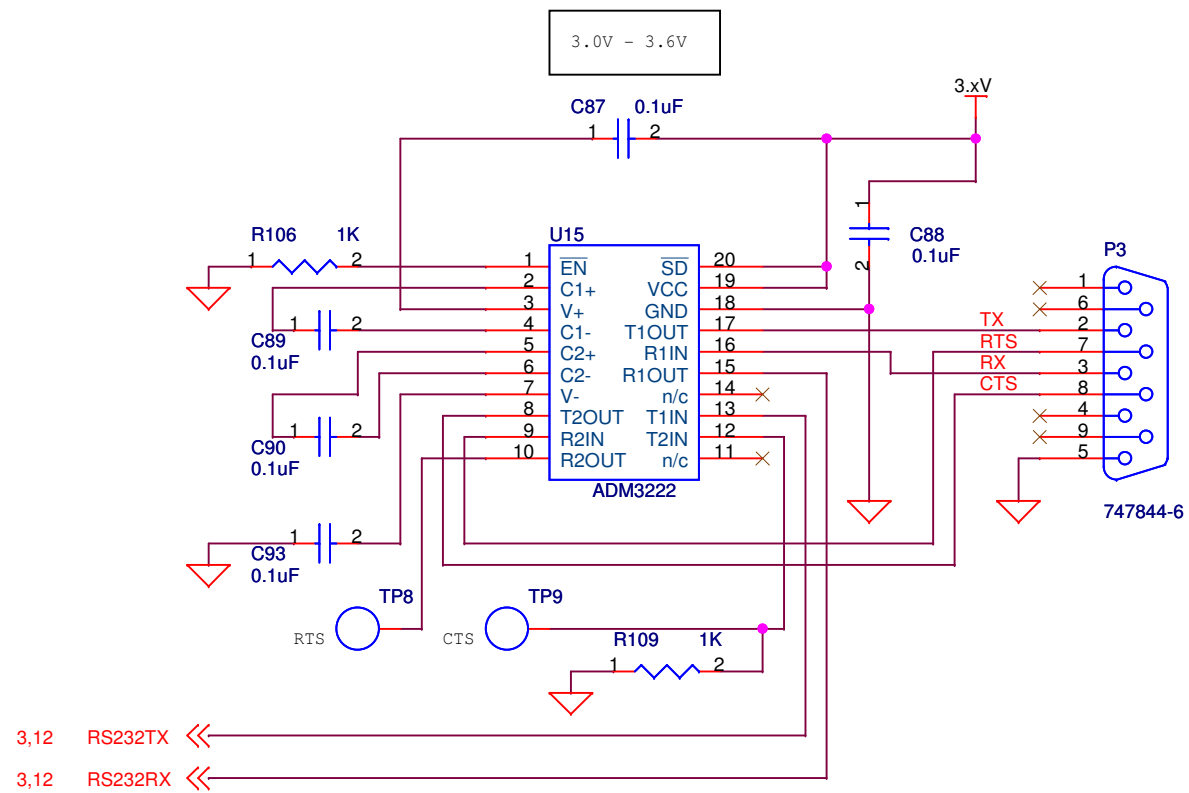
\*Use MGMT port to reset PHY

| JT2 | JT3 | JT4 |  |
|-----|-----|-----|--|
| 2-3 | 2-3 | 2-3 | 10BaseT, Half Duplex, Forced Mode  |
| 2-3 | 2-3 | 1-2 | 10BaseT, Full Duplex, Forced Mode  |
| 2-3 | 1-2 | 2-3 | 100Base-TX, Half Duplex, Forced Mode   |
| 2-3 | 1-2 | 1-2 | 100Base-TX, Full Duplex, Forced Mode   |
| 1-2 | 2-3 | 2-3 | 10BaseT, Half/Full Duplex, Advertised Auto-negotiation Enabled                             |
| 1-2 | 2-3 | 1-2 | 100Base-TX, Half/Full Duplex, Advertised Auto-negotiation Enabled                          |
| 1-2 | 1-2 | 2-3 | 10BaseT, Half Duplex/100Base-TX Half Duplex, Advertised Auto-negotiation Enabled           |
| 1-2 | 1-2 | 1-2 | 10BaseT, Half/Full Duplex/100Base-TX Half/Full Duplex, Advertised Auto-negotiation Enabled |



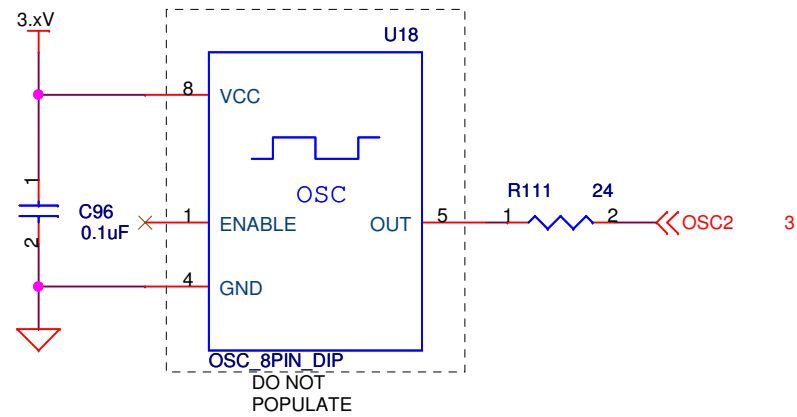
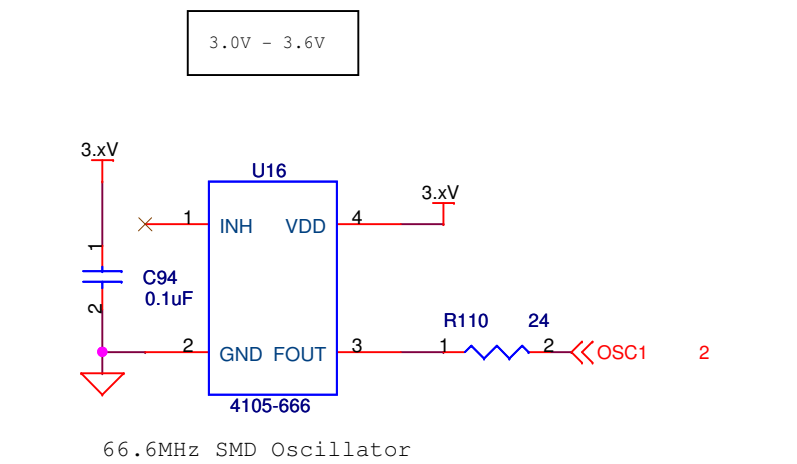


Note: 25.175MHz provides 640 X 480 VGA resolution

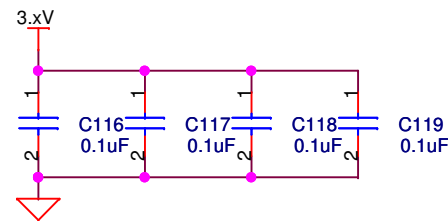
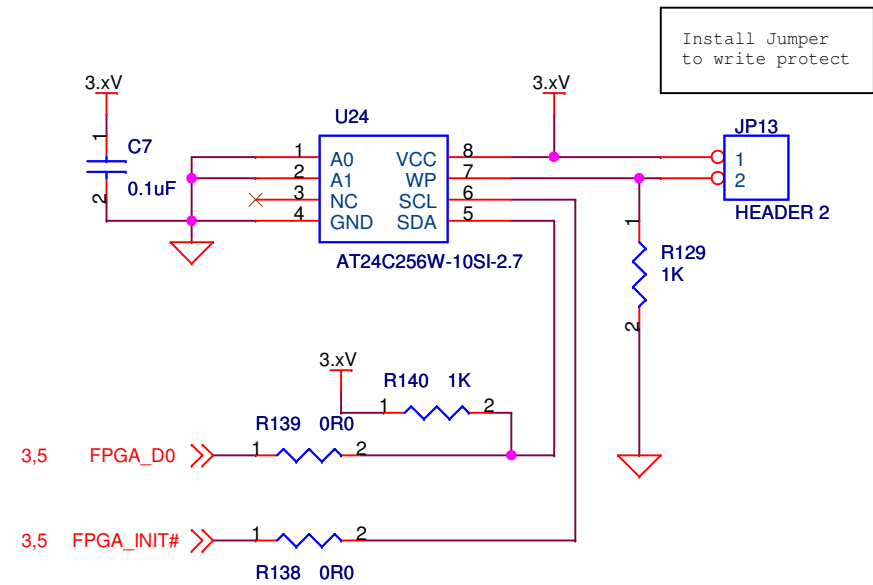
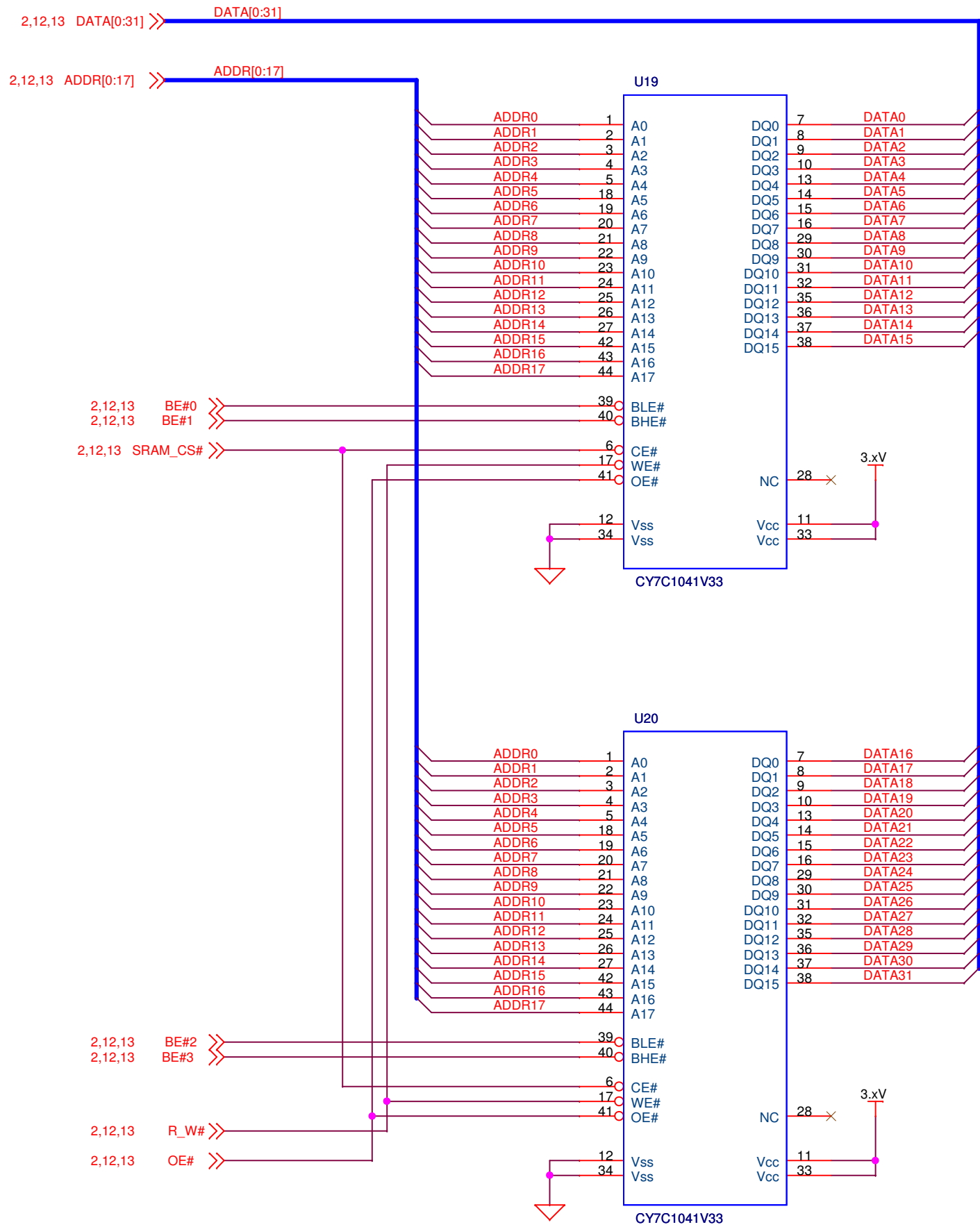


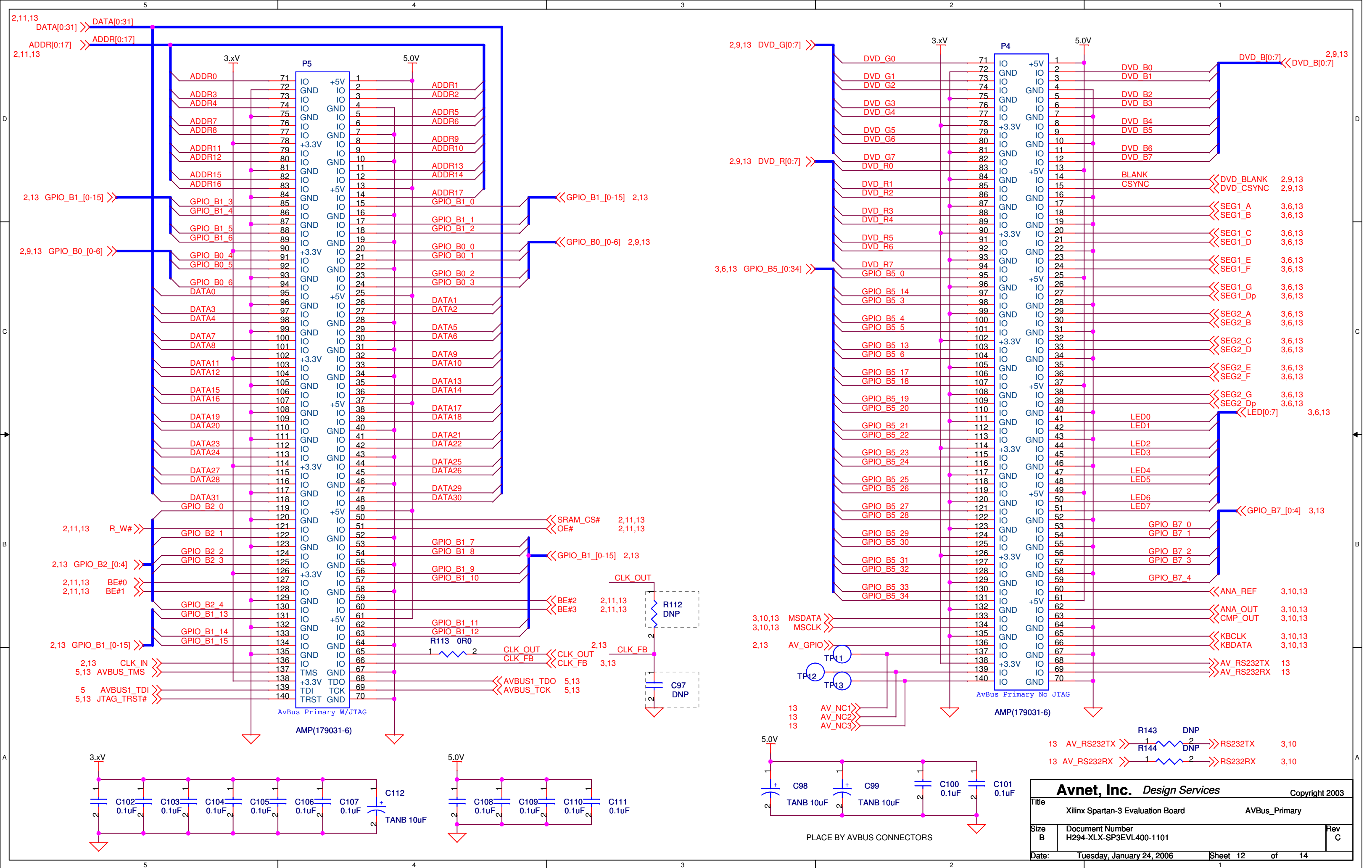
Note: JS1/JS2 are reversed on the schematic for easier connection.  
The physical connector on the PCB is ordered:

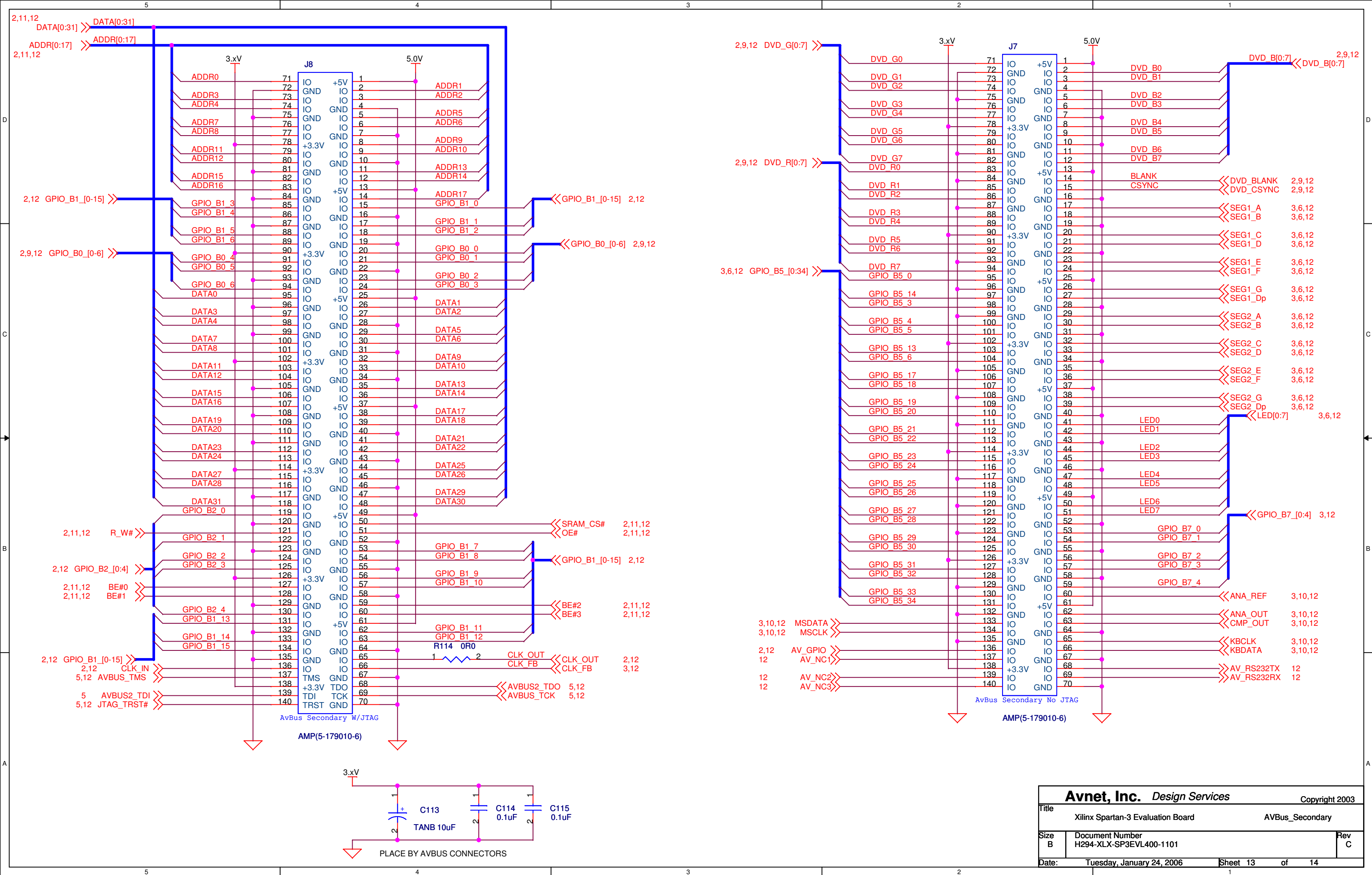
|   |   |
|---|---|
| 6 | 5 |
| 4 | 3 |
| 2 | 1 |



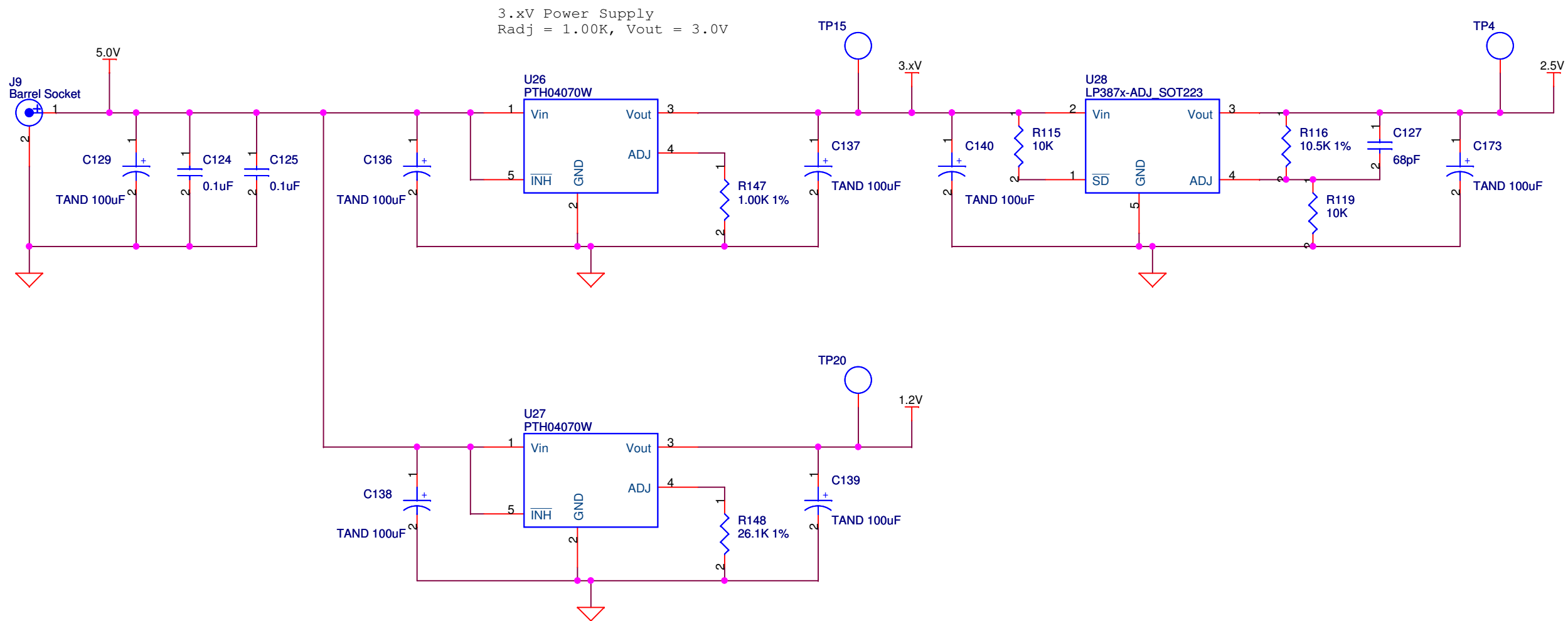
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|-----------------------------|---------------------------|--|----------------|
| Title                       |                           | Xilinx Spartan-3 Evaluation Board PS2_RS232_Analog |                |
| Size                        | Document Number           | Rev  |                |
| B                           | H294-XLX-SP3EVL400-1101   | C  |                |
| Date:                       | Tuesday, January 24, 2006 | Sheet 10   | of 14          |







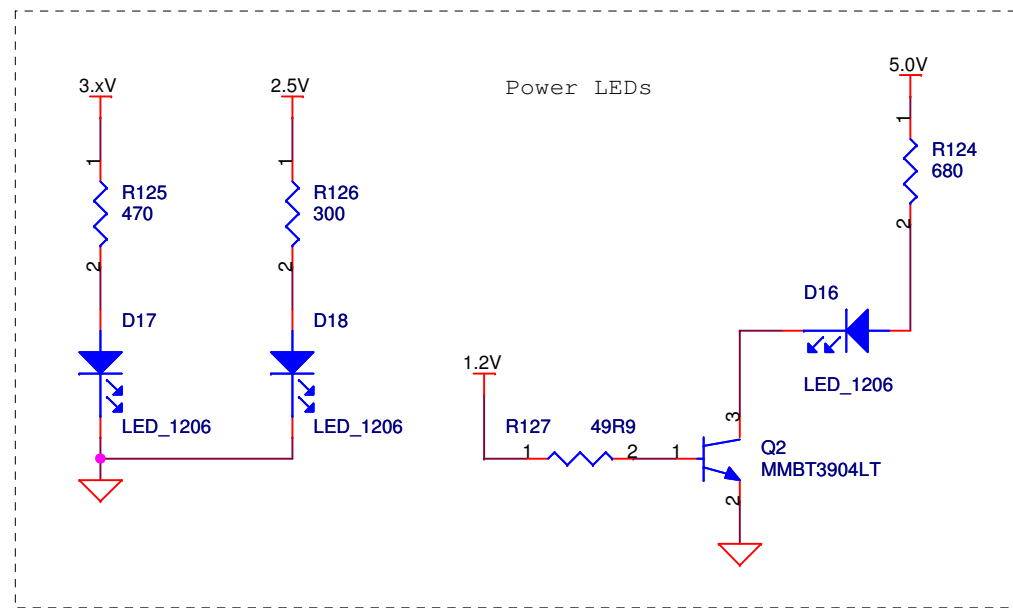
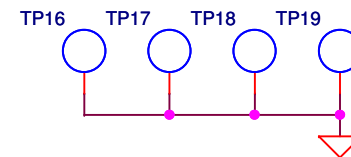
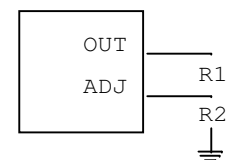




## LP3875 Output Voltage

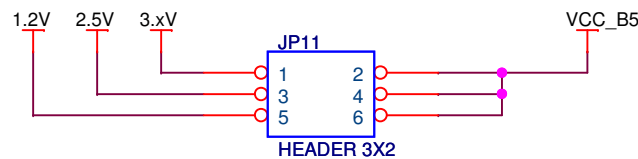
$$R1 = R2 \left( \frac{V_o}{1.216} - 1 \right)$$

$$V_o = 1.216 \left( \frac{R1}{R2} + 1 \right)$$

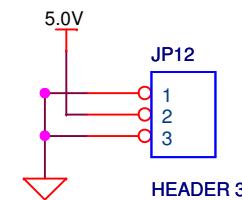


## FPGA Bank I/O Voltage Selection

(Shunt required. One voltage must be selected at all times. Do not switch VCCO voltages while power is applied to the board.)



## Active HeatSink Power



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|        |                             |                                   |       |       |       |
|--------|-----------------------------|-----------------------------------|-------|-------|-------|
| Title  |                             | Xilinx Spartan-3 Evaluation Board |       | Power |       |
| Size B | Document Number             | H294-XLX-SP3EVL400-1101           |       |       | Rev C |
| Date:  | Wednesday, January 18, 2006 | Sheet 14                          | of 14 |       |       |