AR# 25245

MIG v2.0 - How do I determine whether the PAR template routes are properly used for Spartan-3 DDR/DDR2 SDRAM designs?

Description

The Local Clocking scheme used to capture data in all Spartan-3 family memory designs output by MIG requires Place and Route (PAR) template routes to properly place the delayed strobe and data bits.

How do I determine whether the PAR template routes are properly used for these Spartan-3 MIG designs?

Solution

Starting with the MIG 2.1 release, this information is available in the MIG User Guide > DDR2 Debug Guide. Please see the MIG User Guide for further information.

Template routing is required to properly route the delayed strobe (dqs*_delayed_col*), as well as the data (dq bits) in the MIG Spartan-3 family DDR and DDR2 SDRAM designs.

For the data bits to be routed properly, the environment variable XIL_ROUTE_ENABLE_DATA_CAPTURE must be enabled when PAR is run.

This environment variable is set in the implementation script file ("ise_flow.bat") provided in the "/par" MIG output directory.

For the delayed strobe to be properly routed, the strobe is placed on local clock routing.

PAR automatically treats Local Clocks as template routes and locks down the routes correctly without using the environment variable.

Data Bits

The template router set through the environment variable ensures that the data bits are routed from a PAD to a Distributed Memory to capture the data in an Async FIFO using the Local Clock to write the data and a Global Clock to read the data.

These routes require a template to guarantee that the delay remains constant between all data bits.

Once the design is implemented, load it into the FPGA Editor to visually verify the template routes for the data bits, as follows:

1. Open the design in FPGA Editor by selecting Start -> Programs -> Xilinx ISE 9.1i -> Accessories -> FPGA Editor.

2. Select File -> Open and browse to the design's ".ncd" and ".pcf" files to launch the design.

3. In some cases, turning Stub Trimming off will provide a better picture of the route.
To do this, select File -> Main Properties and turn off "Stub Trimming" in the "General" tab.
When Stub Trimming is enabled, FPGA Editor does not display the entire route.
If Stub Trimming is disabled, you can see the entire length of the routing segment.
Stub Trimming is enabled in the pictures below.

4. Search within the "List1" window for "*dq*" under the "All Nets" drop-down.
Select all of the DQ data bit nets (e.g., main_00/top0/dq(0)) within the window and highlight these nets by clicking the "hilite" button in the right-hand column.
This allows for visual inspection of the delay routes.
Zoom into the area with the highlighted nets and verify that the placement looks like one of the following two figures:

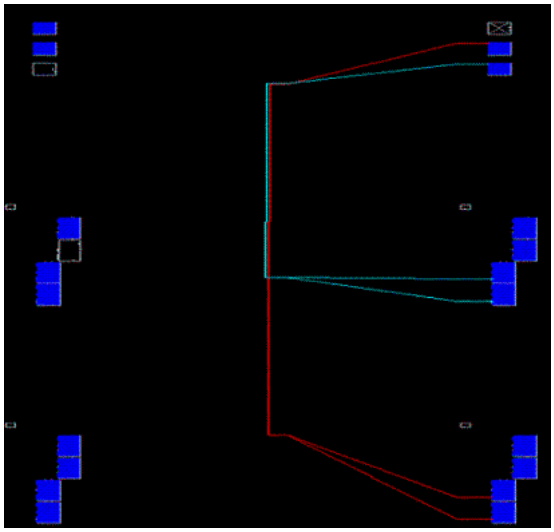

Figure 1. DQ Placement (Top/Bottom)

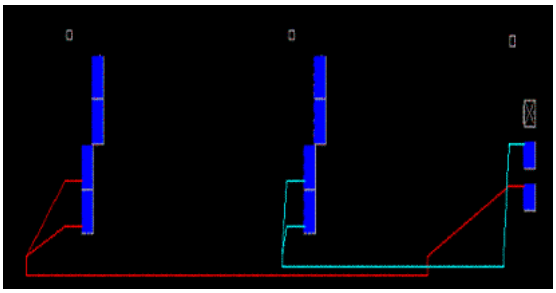

Figure 2. DQ Placement (Left/Right)

5. Next, verify that the delays on the nets are consistent.
Again, select all of the DQ data bit nets in the "List1" window.
This time click on the "delay" button located in the right-hand column.
This lists the worst-case delay for the DQ bits.
Using this delay information, you can quickly identify inconsistent routing.
There should be less than 75 ps of skew (ideally less then 50 ps) between the data nets.
The delay values will depend on the device speed grade and Top/Bottom versus Left/Right implementation but have been observed to range between 300-700 ps.

If you prefer, you can export the delay information to view the report in an Excel spreadsheet.
Select File -> Export to export the delay information to a ".csv" file.

Delayed Strobe

The delayed strobes (dqs*_delayed_col*) in the Spartan-3 families DDR/DDR2 designs use the local clocking resources available in the device for the clock routing.

The local routing resources used depend on the pin placement specified during generation in the MIG tool.

Full hex lines that have low skew are located throughout the device.

Left and right implementations use Vertical Full Hex (VFULLHEX) lines for local clock routing.

Top and bottom implementations use VLONG, VFULLHEX, and HFULLHEX lines for local clock routing.

PAR routes from the Local Clock PAD to a series of LUTs to implement the scheme explained in detail in XAPP768c located at:
http://www.xilinx.com/support/software/memory/protected/XAPP768c.pdf
(Registration required.)

From the output of the final LUT delay, the delayed strobe/Local Clock (dqs*_delayed_col*) will route to all of the FIFO bits.

To verify the pin-out and usage of the template router, the net skew and max delay on the local clock (dqs*_delayed_col*) must be within spec.

To verify these values, open the PAR report (.par file) and scroll to the "Clock Report" section.

For most Spartan-3 families the "Net Skew" will be less than 40 ps and the "Max Delay" will be approximately 550 ps.

For Spartan-3A and Spartan-3A DSP devices, the "Net Skew" will be less then 65 ps and the "Max Delay" will be approximately 400 ps.

For information on pin placement, see (Xilinx Answer 24935).

You can then use the FPGA Editor again to view the local clock placement.

To view the template routes for the delayed strobes, search in the "List1" window for "*dqs*_delayed_col*" in the "All Nets" drop-down.

Select all of the nets (ex - main_00/top0/data_path0/dqs0_delayed_col0) and select "hilite" from the right-hand column.

This command highlights the nets of interest.

You can then zoom into this range of highlighted signals to view the placement.

If local clocking is used, you will see one of the following two structures:

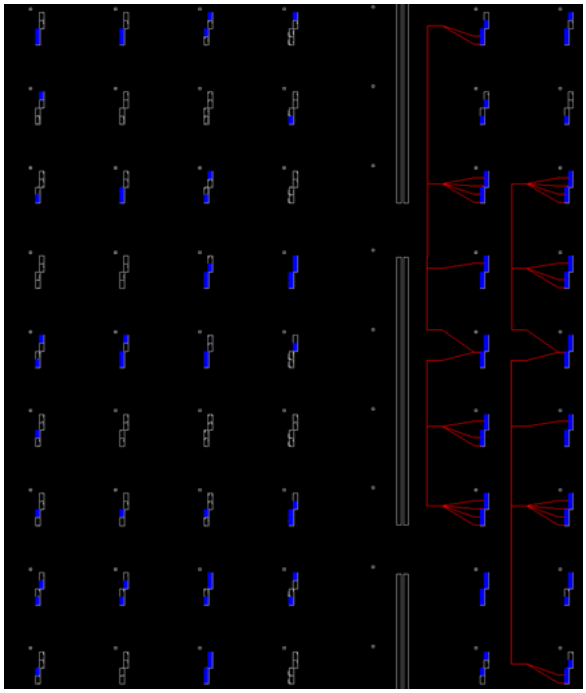

*Figure 3. Local Clock (Left/Right) for "dqs*_delayed_col*" LUT Delay Elements*

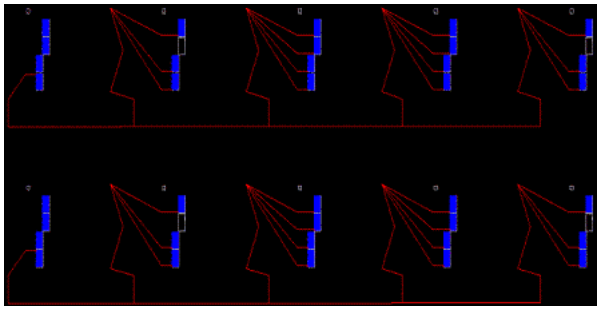

*Figure 4. Local Clock (Top/Bottom) for "dqs*_delayed_col*" LUT Delay Elements*

If the skew and delays are within spec and the layout for the Local Clock and Data bits match the above figures, the template routes have been properly implemented.

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