LYR178-101D (SDSP Development Platform)

RefDes	Qty	Description	Value	Part Number	MRP
PCB1	1	Printed Circuit Board	N/A	LYR178-101D	690-274-D
BOM1	1	IC 512 Mb, 667Mhz, DDR2 SODIMM 200p +1.8V, non ECC, Unbuffered ROHS=OK	N/A	MT4HTF6464HY-667E1	209-047
BOM2	1	Compact Flash 256MB	N/A	CF256-12-251 256MB	872-004

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REVISION HISTORY

Date	Description	Revision
2007-07-04	Remove EXP interface and replace it with a second FMC interface	0.90
2007-07-04	Add an adjustable power module to power the second FMC module VIO	0.90
2007-07-05	Add a separate trace for DDR2 CKE1 signals and an additionnal 4.75K pulldown	0.90
2007-07-05	Add terminations on DQs signals close to fpga	0.90
2007-07-05	Add 4.7pF between clocks signals	0.90
2007-07-05	Change DVI AVDD supply to +3.6V	0.90
2007-07-05	Add a 1.0K serie resistor to terminate DVI_DETECT close to DVI connector	0.90
2007-07-05	Add resistors on U6 pins 41, 42, 43 and 46 to make possible the use of both CH7301 or CH7303	0.90
2007-07-05	Add 2 FMC connectors for Power Analysis	0.90
2007-07-25	Add a second LCD as a dual footprint	0.91
2007-08-02	Change FMC Presence Pull-Up for 1Kohm	0.92
2007-08-02	Remove Mictor connector and shroud	0.92
2007-08-02	Connect LA17 and LA28 signals of FMC Site 2 to GCLK FPGA pins	0.92
2007-08-02	Use FPGA LHCLK pins to connect FMC site 1 CLK_M2C, LA17 and LA28 signals	0.92
2007-08-02	POWER_GOOD signals disconnected from FPGA	0.92
2007-08-21	Change Input Voltage to +5V instead of +12V	0.93
2007-08-21	Add a switcher to supply 12V@2A from +5V input	0.93
2008-01-30	Change clock generator U26 text comment for 125MHz instead of 200MHz and 31.25MHz instead of 33MHz	0.94

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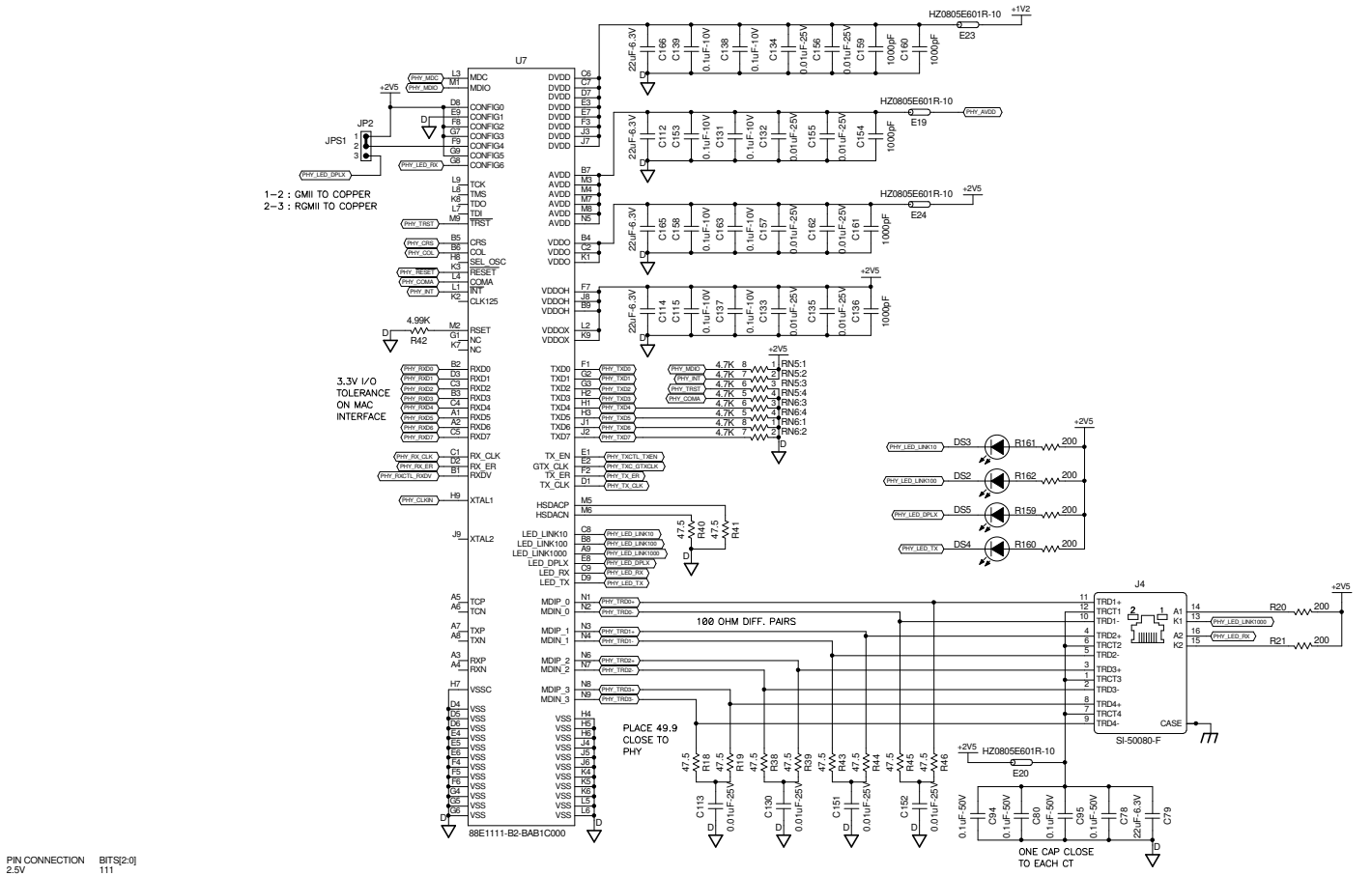
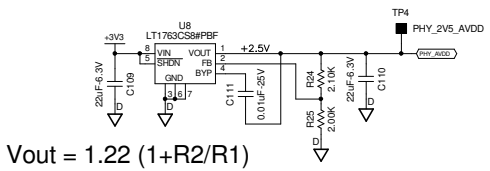
Reference number: {No de Ref}		Paper size: C
Filename: LYR178-101D.sch	Printing date and hour: Thu Jan 31, 2008 13:14:48	Rev.: D
Drawn by: Roger Gagnon	Approved by: David Bourget	Page: 1 of 14



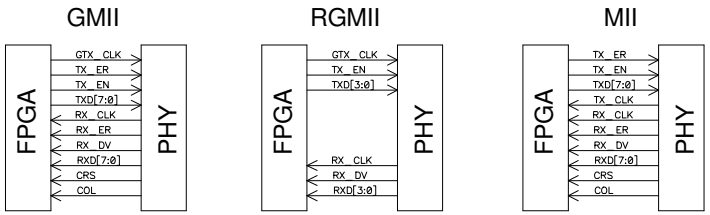
PIN CONNECTION	BITS[2:0]
2.5V	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

PIN	BIT[2]	BIT[1]	BIT[0]	
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	111
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	111
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM	010

PHYADDR[4:0] = 00111
ENA_PAUSE=0
ANEG[3:0]=1111=ADVERTISE ALL CAPABILITIES
ENAXC=1=ENABLE CROSSOVER
DIS_125=1=DISABLE CLOCK 125MHZ
HWCFG_MODE[3:0]=1111=GMII TO COPPER
HWCFG_MODE[3:0]=1011=RGMII TO COPPER
DIS_FC=1=DISABLE FIBER/COPPER AUTOSELECT
DIS_SLEEP=1=DISABLE ENERGY DETECT
SEL_TWSI=0=SELECT MDC/MDIO INTERFACE
INT_POL=1=INT IS ACTIVE LOW
75/50=0=50 OHM FOR FIBER



Vout = 1.22 (1+R2/R1)



ETHERNET

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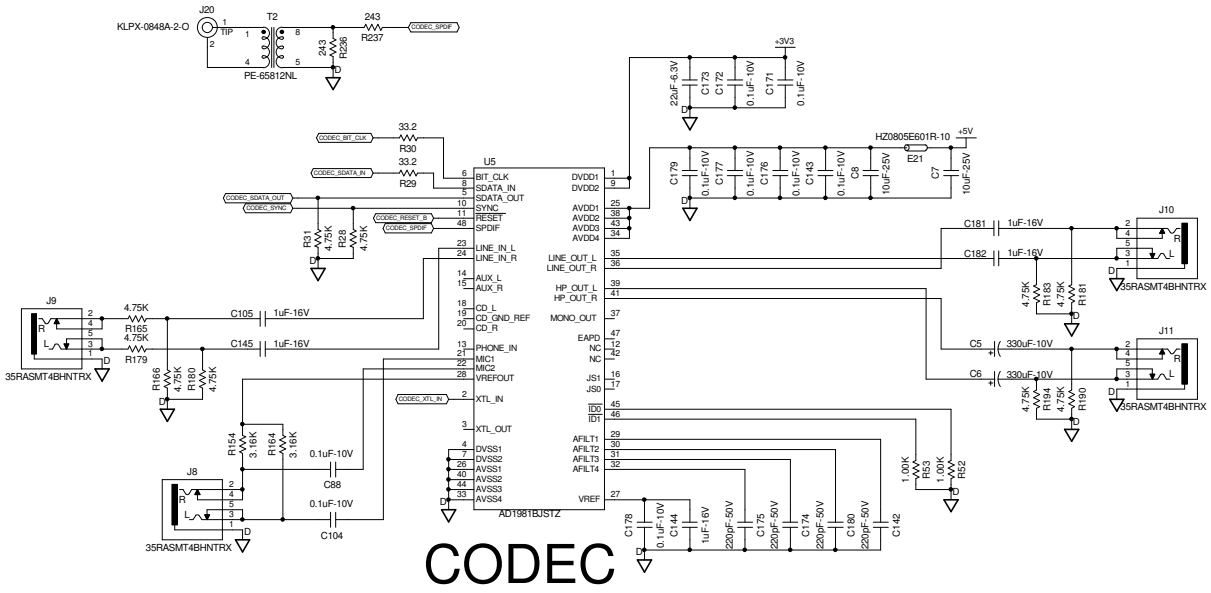

CODEC

AUDIO

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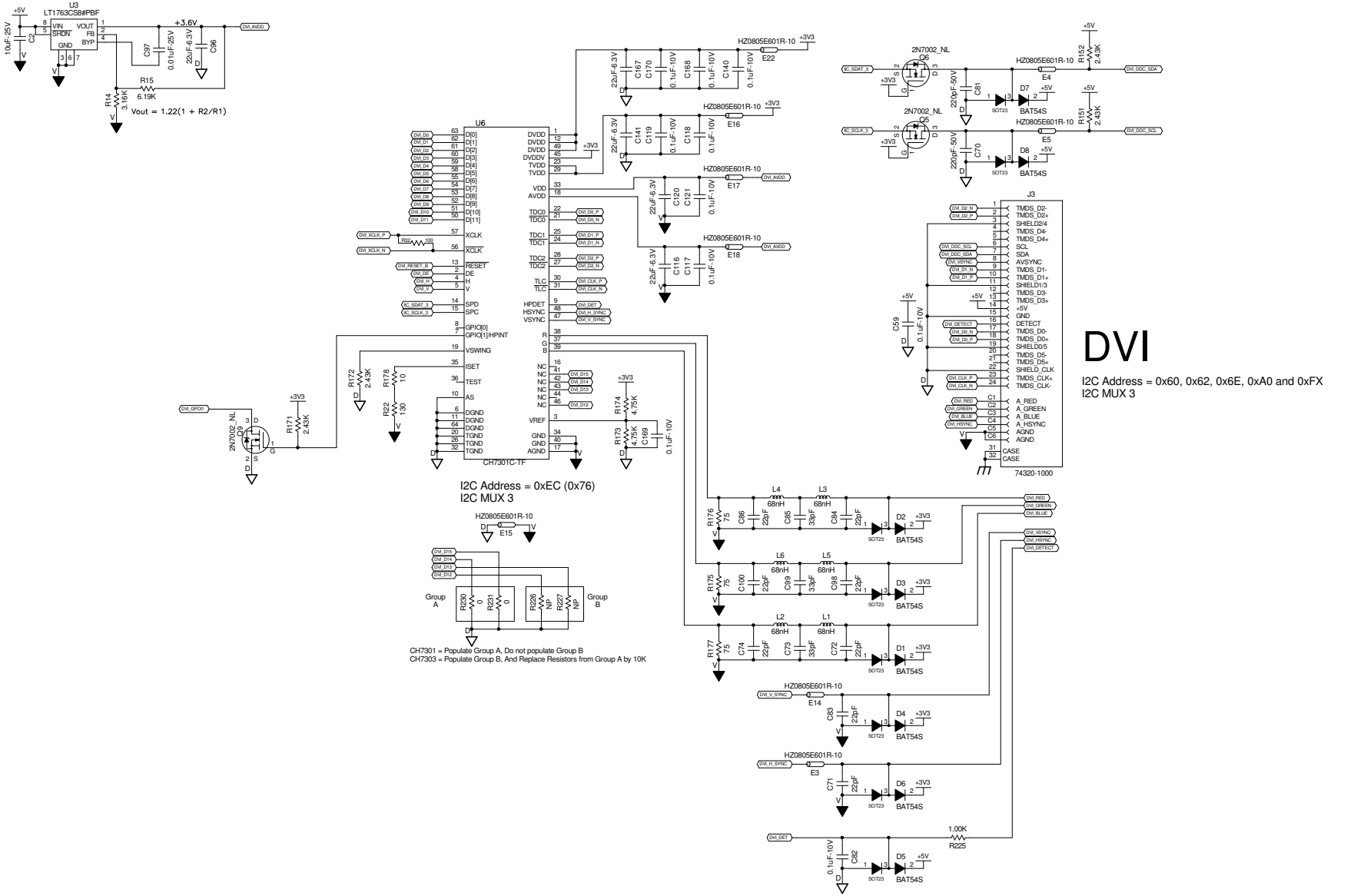

VIDEO

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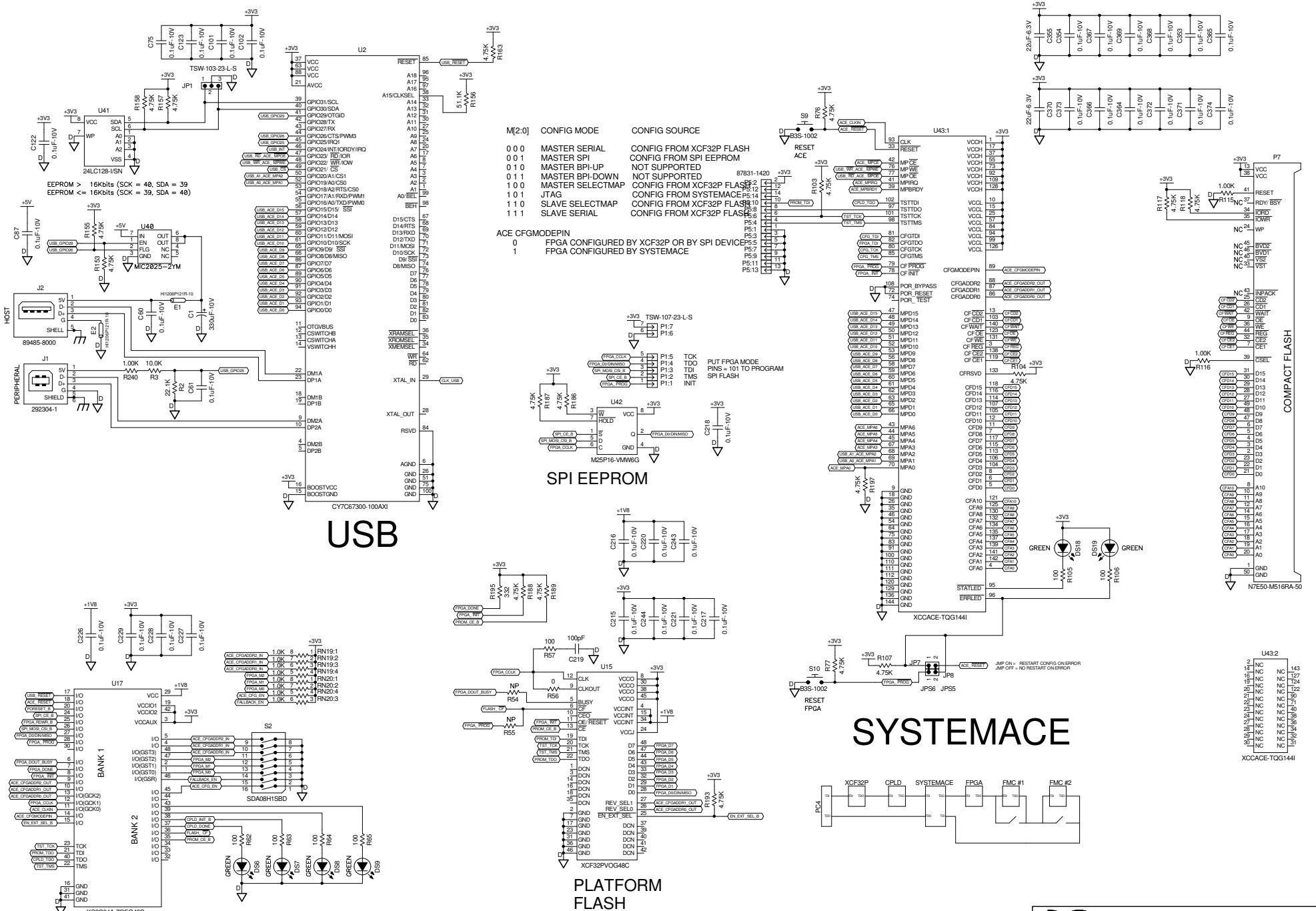

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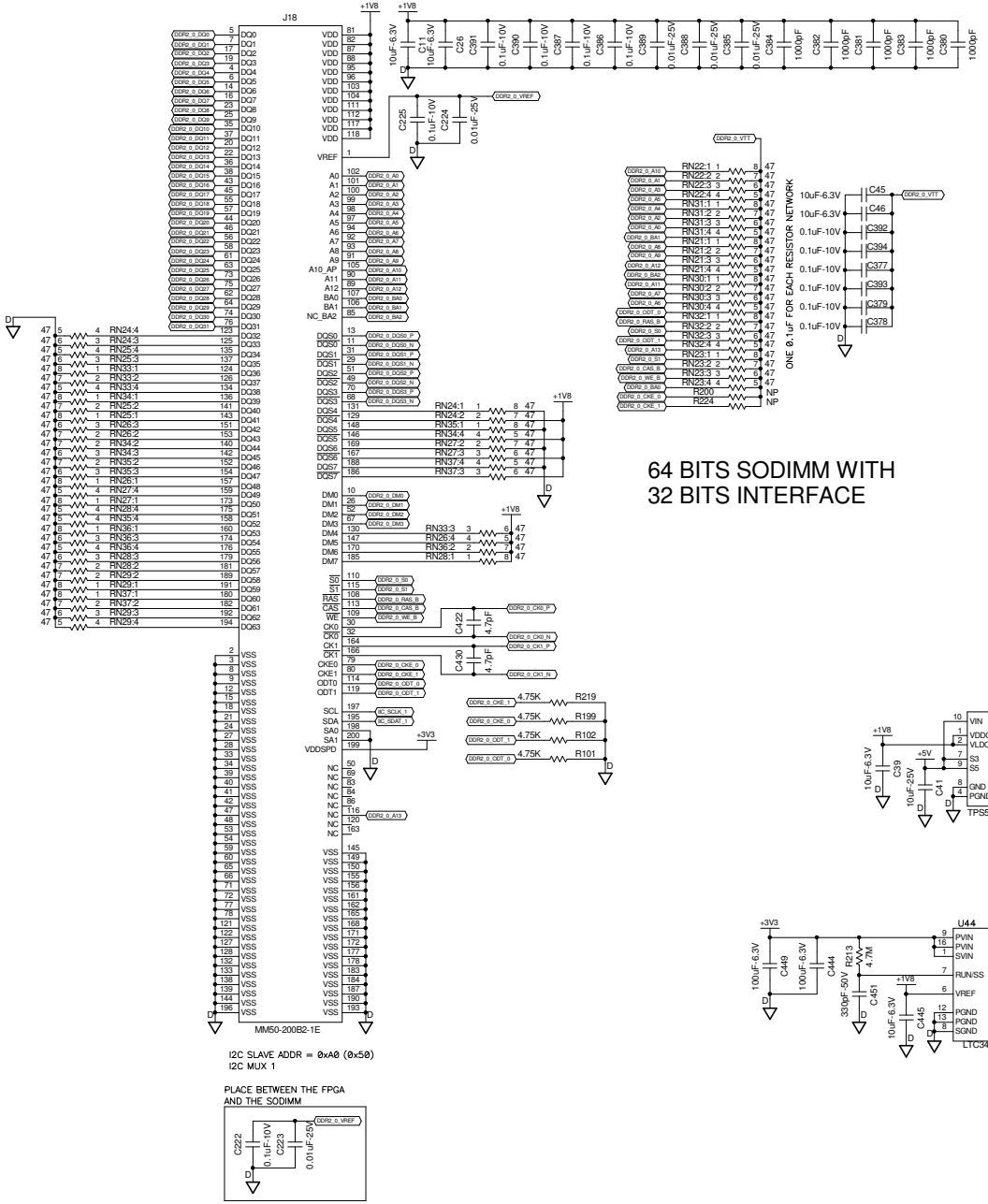

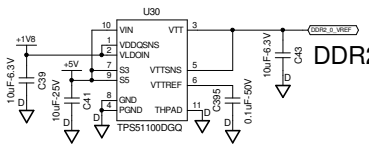

DDR2 SODIMM

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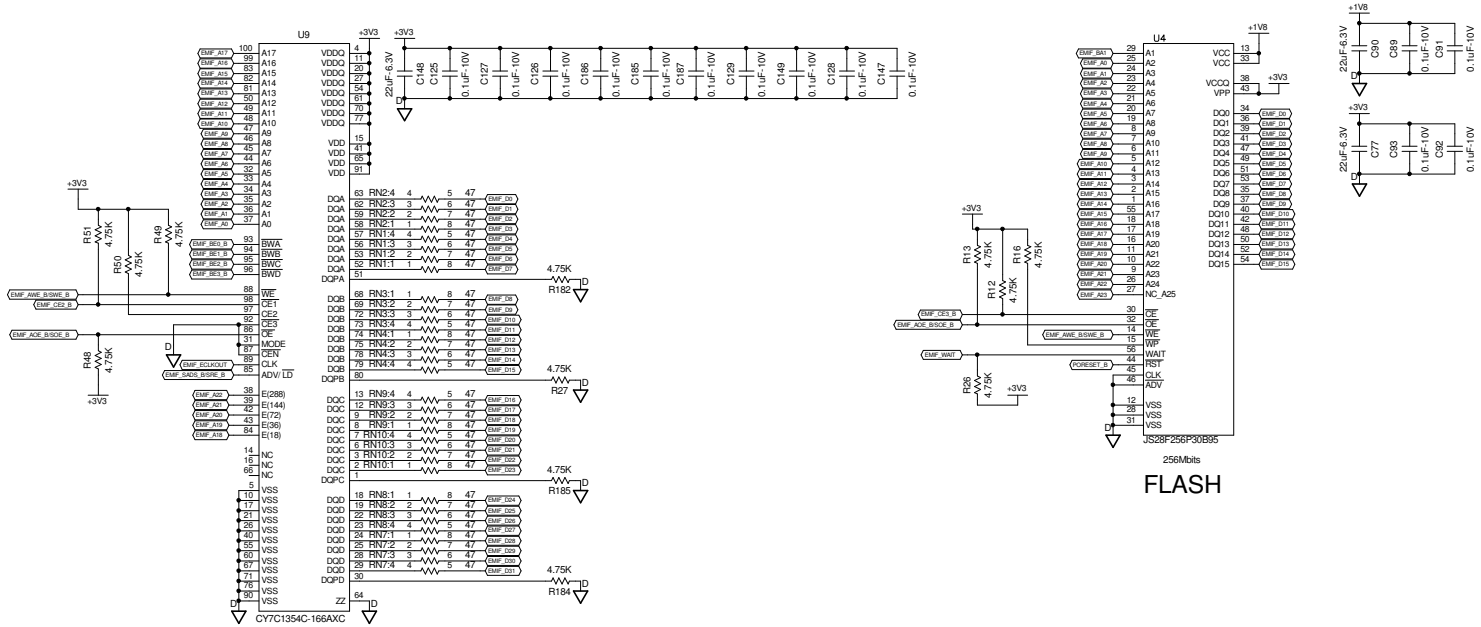

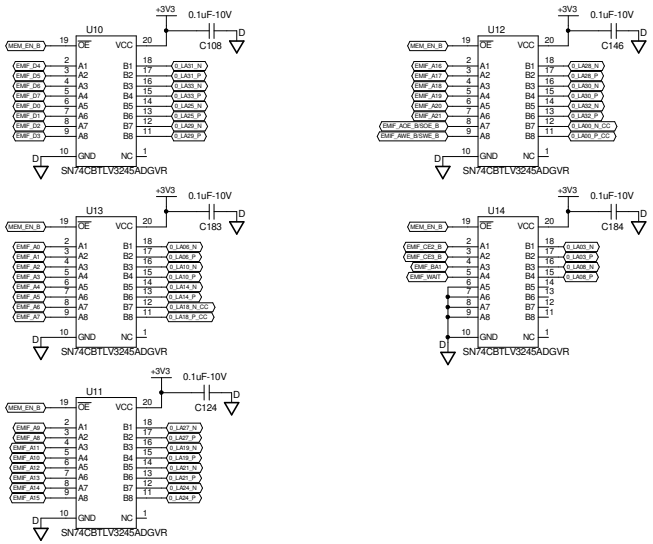

SRAM + FLASH

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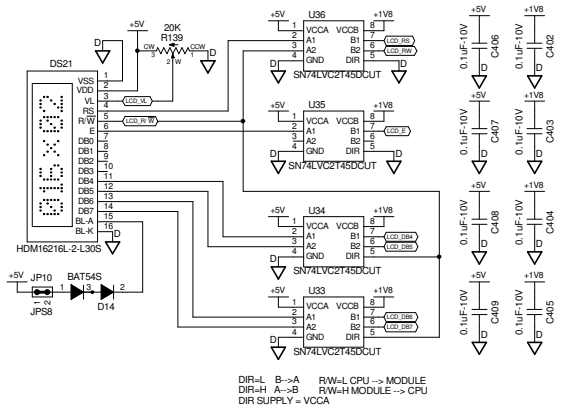
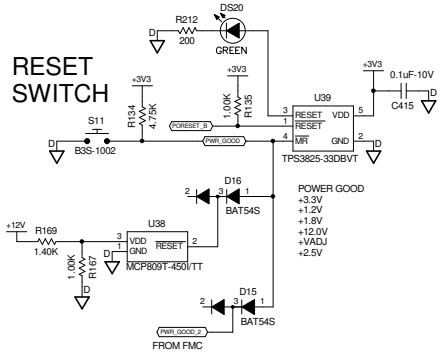
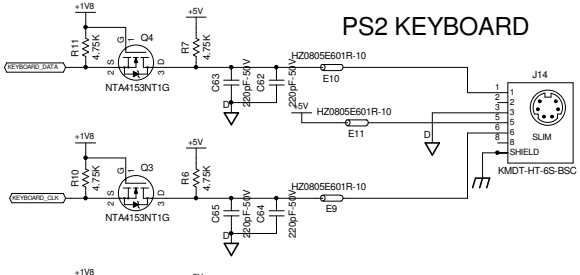
LCD DISPLAY



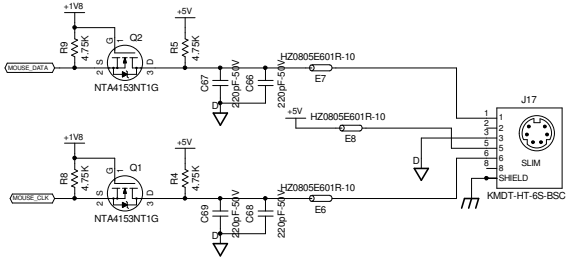
RESET SWITCH



PS2 KEYBOARD



PS2 MOUSE



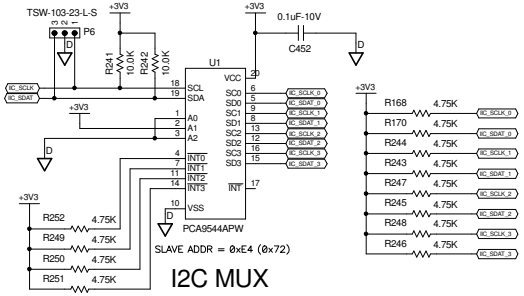
Mux 0:
Hex Device
0xA8 I2C EEPROM
0x58 Fan Controller
0xE4 I2C Mux

Mux 1:
Hex Device
0xD4 Clock Generator
0xA0 DDR2 SODIMM EEPROM
0x62 SODIM EEPROM SWP
0x66 SODIM EEPROM CWP
0x60 SODIM EEPROM PSWP
0xE4 I2C Mux

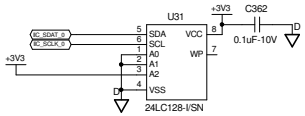
Mux 2:
Hex Device
0xA0 FMC1 EEPROM
0xX0/0xX8 FMC1 Optional
0xA2 FMC2 EEPROM
0xX2/0xXA FMC2 Optional
0xA4 Digital Pot
0xE4 I2C Mux

Mux 3:
Hex Device
0xA0 E-DDC
0x60 E-DDC
0x62 E-DDC
0x6E E-DDC/CI
0xFX DDC Display Dependent Devices
0xEC Video Encoder
0xE4 I2C Mux

I2C MUX



I2C EEPROM



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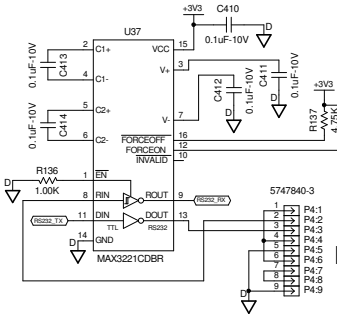
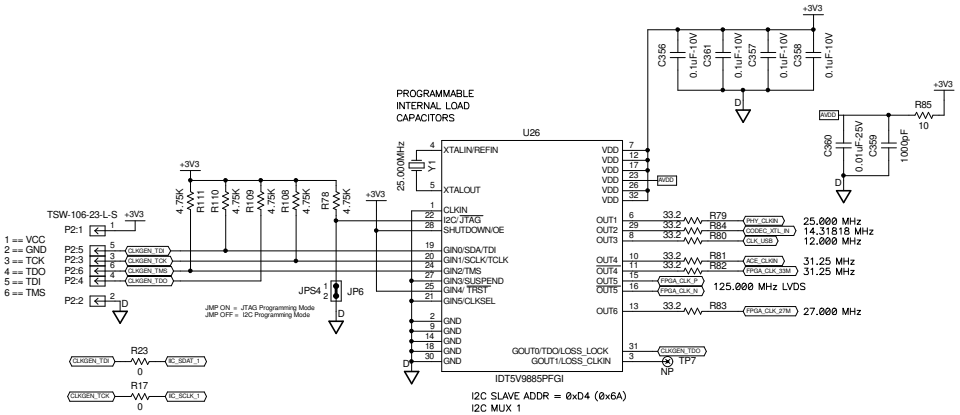
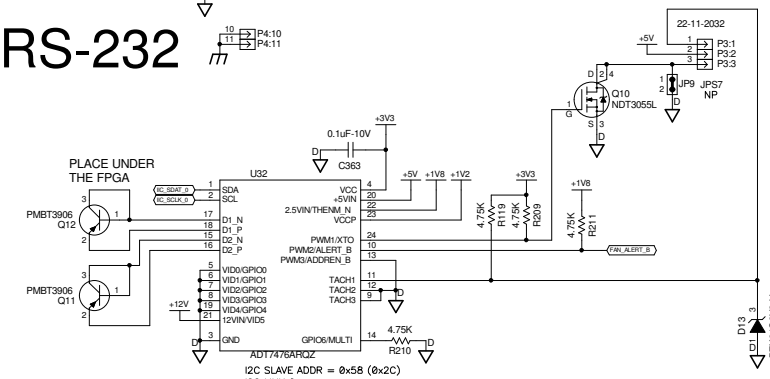


RS-232

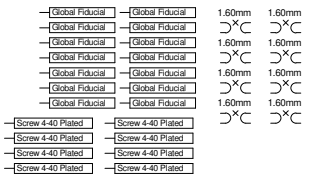
CLOCK GENERATOR



FAN CONTROLLER



MISC



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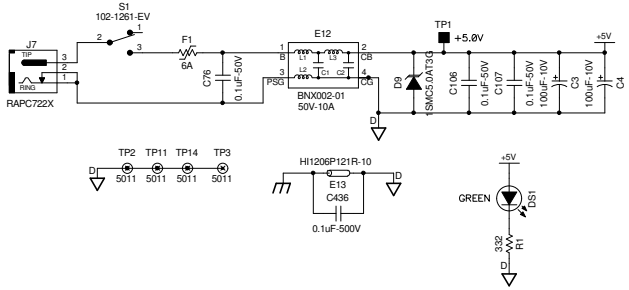
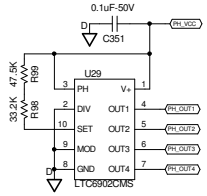
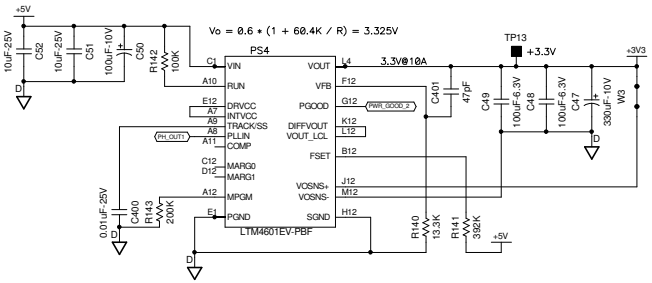


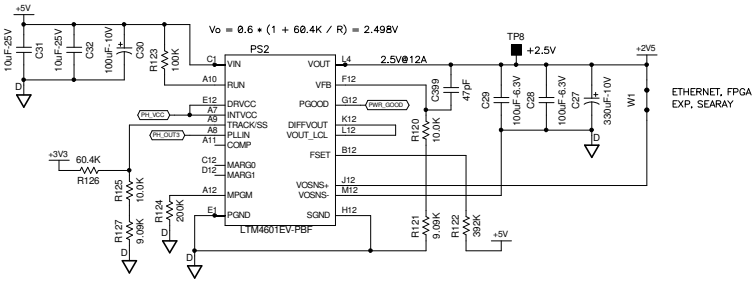


2 PHASE: PH = GND M = 1
3 PHASE: PH = OPEN M = 3
4 PHASE: PH = V+ M = 4

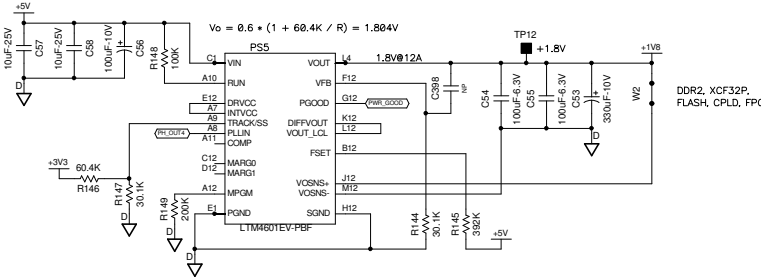
Fout = 2MHz - 20MHz : DIV = GND N = 1
Fout = 200KHz - 2MHz : DIV = OPEN N = 10
Fout = < 200KHz : DIV = V+ N = 100

Fout = (10MHz / N * M) * (20K / RSET) = 620KHz
M = 4
N = 1
Rset = 80.6K

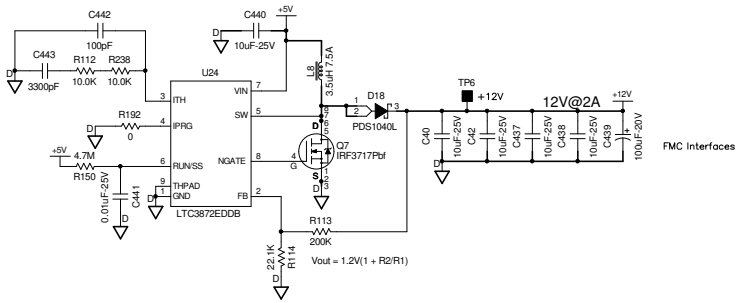




ETHERNET, FPGA
EXP, SEARAY



DDR2, XCF32P,
FLASH, CPLD, FPGA



FMC Interfaces

POWER_1

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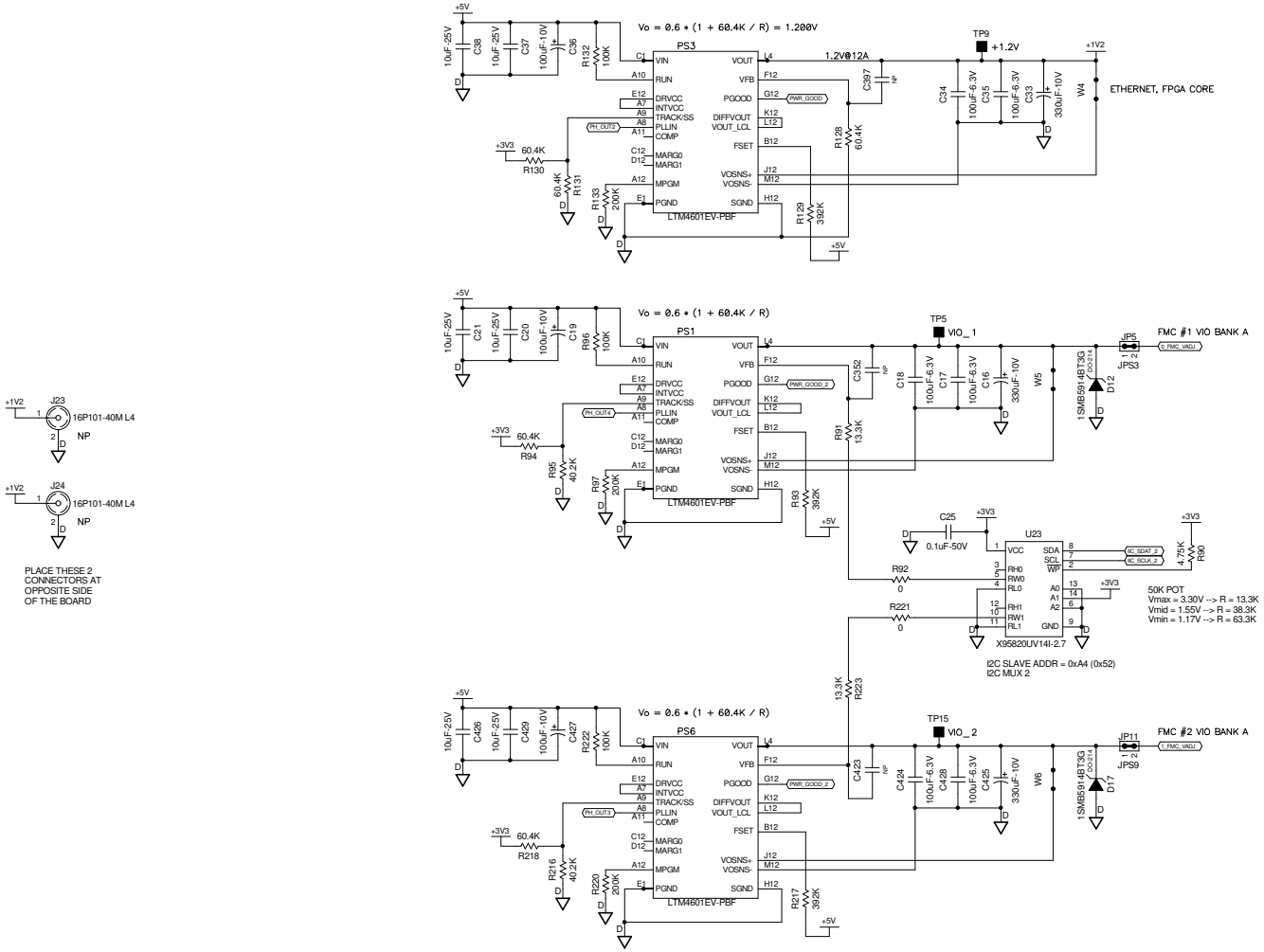

POWER_2

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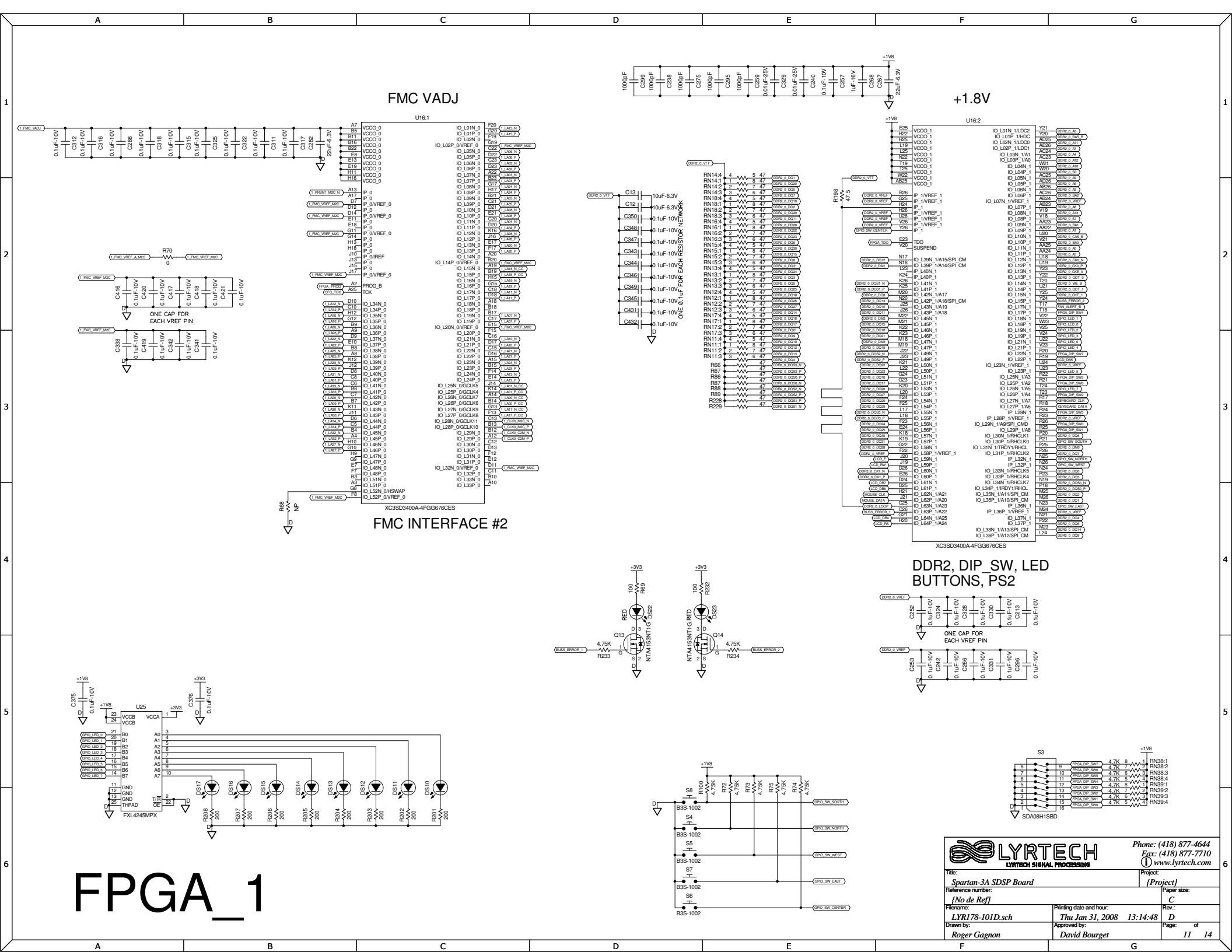

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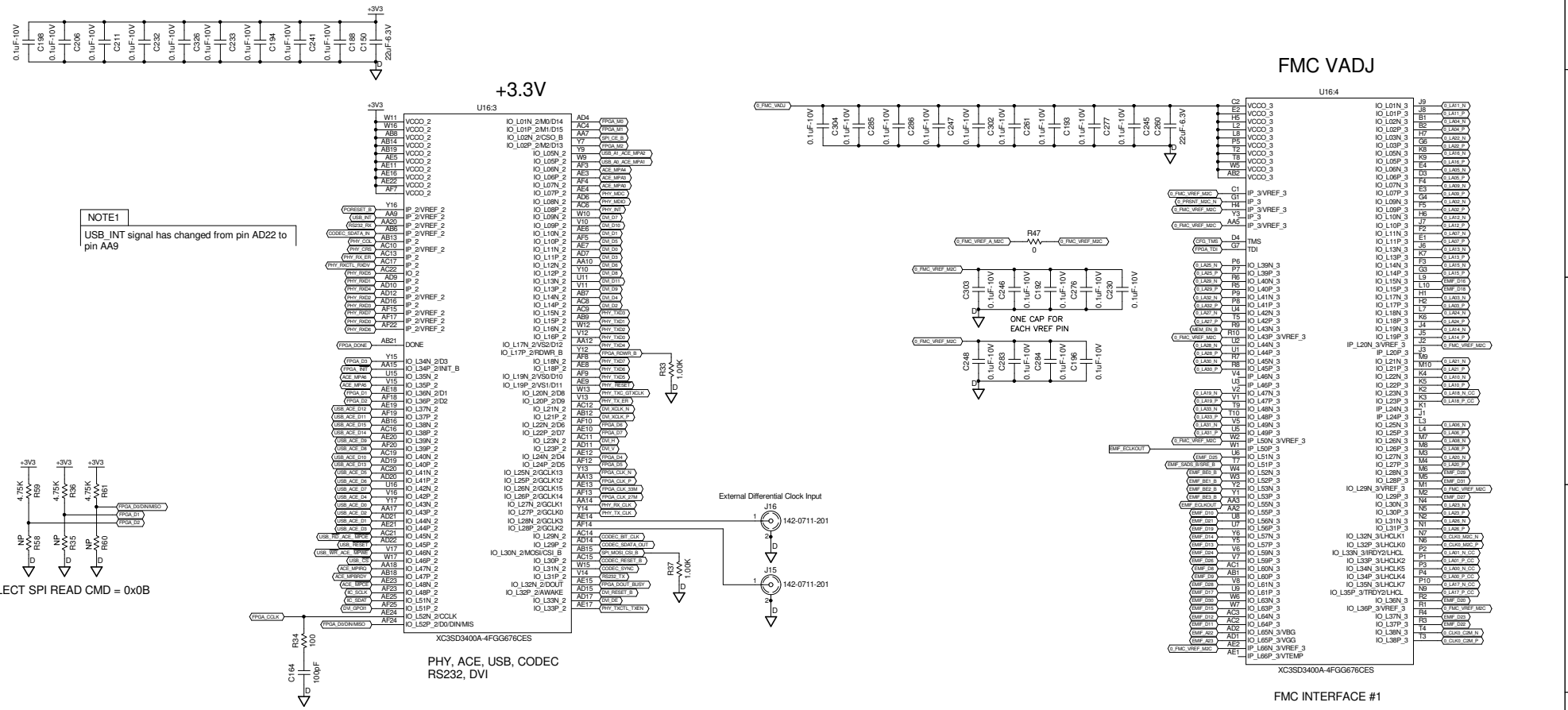

FPGA_2

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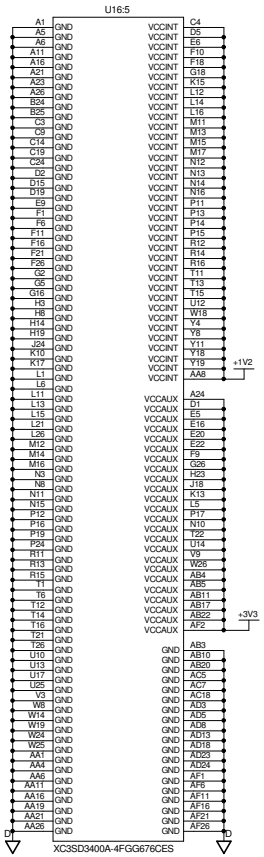

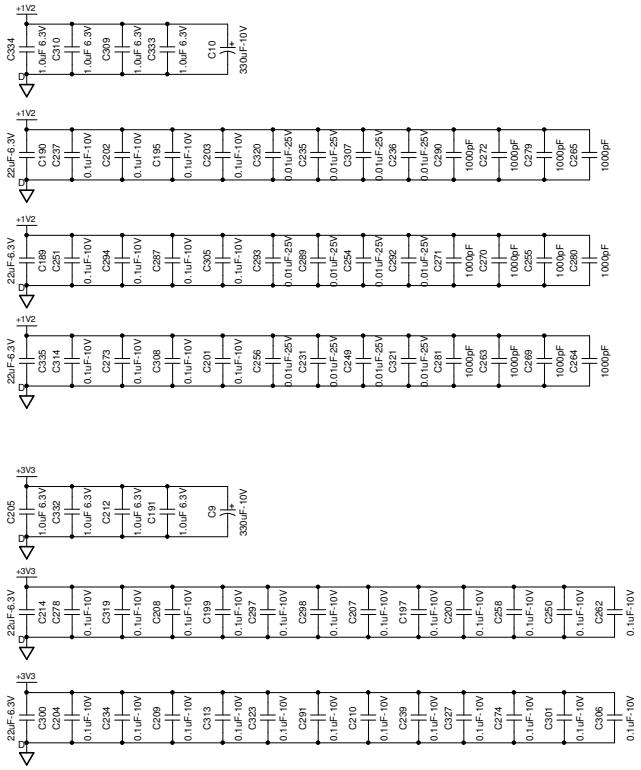

FPGA POWER

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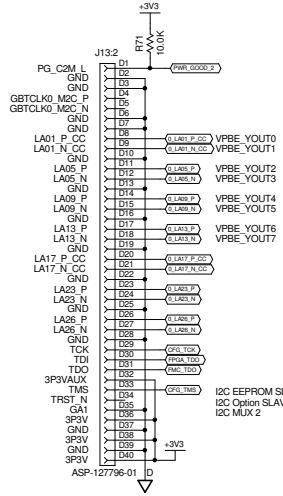
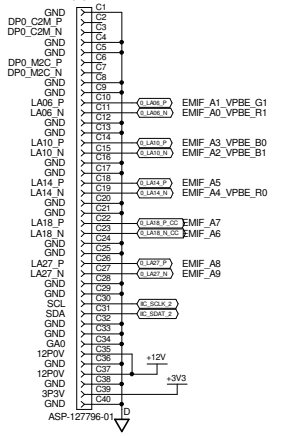
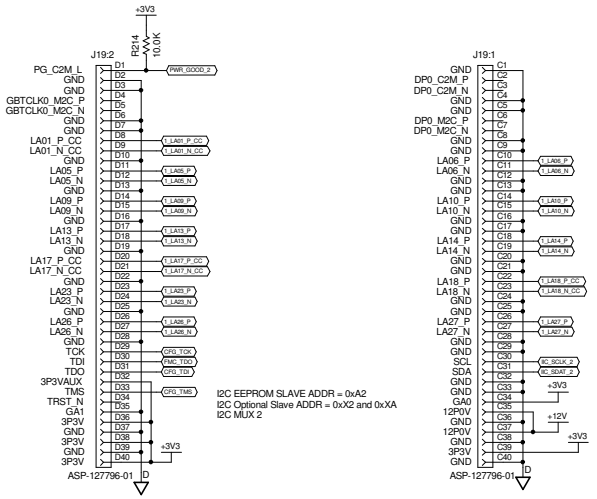




FMC (LPC) INTERFACE #1



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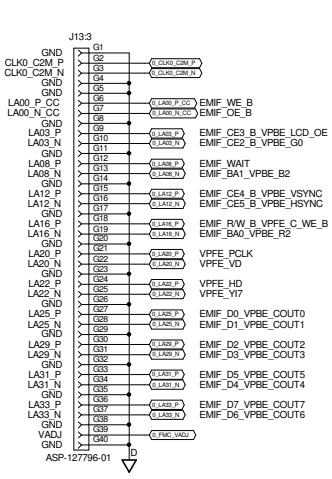
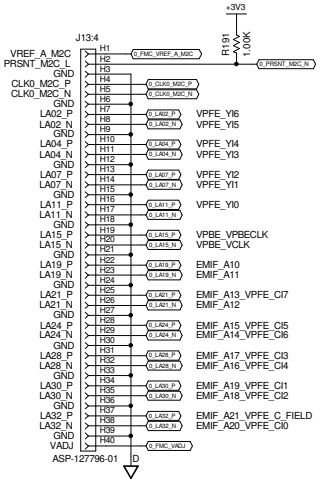
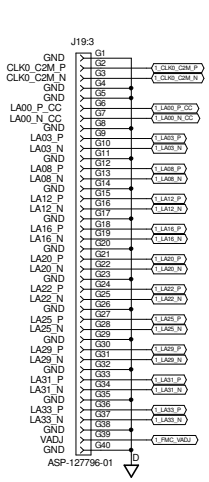
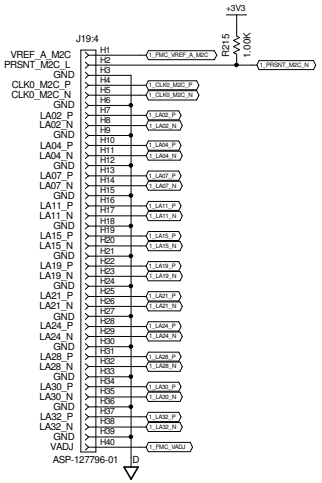
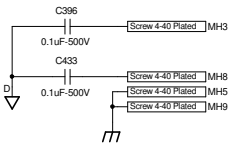
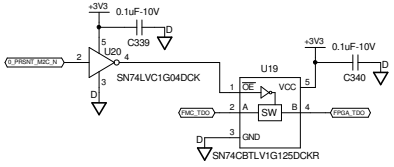


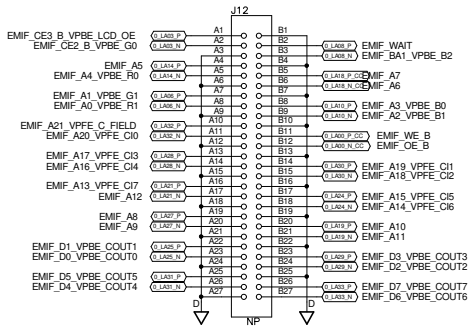




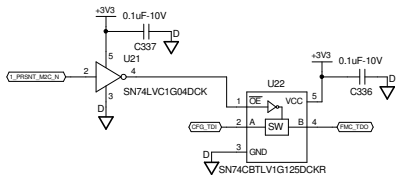


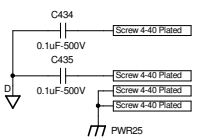






SOFT TOUCH PRO





INTERFACES

LYRTECH SIGNAL PROCESSING

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Drawn by: Roger Gagnon	Approved by: David Bourget	Page: 14 of 14