



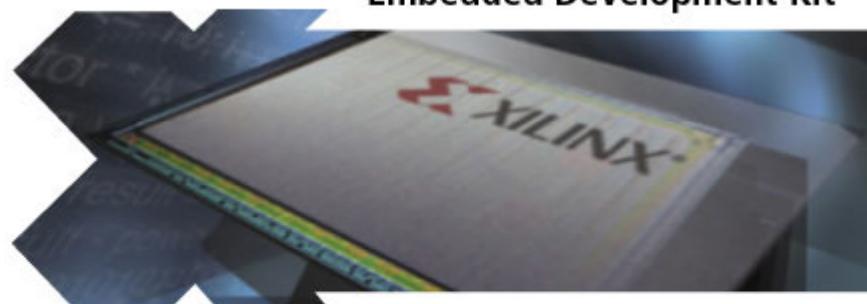
# ML505/506/507

## Standard IP Design

## Adding a USB Controller

June 2008

Embedded Development Kit



**PowerPC**



**Platform Studio™**



**MicroBlaze™**



**XILINX®**

# Overview

- Hardware Setup
- Software Requirements
- Add Standard IP
- Generate a Bitstream
- Transfer the Bitstream onto the FPGA
- Loading a Bootloop into the Block RAM
- Generate and use ACE file



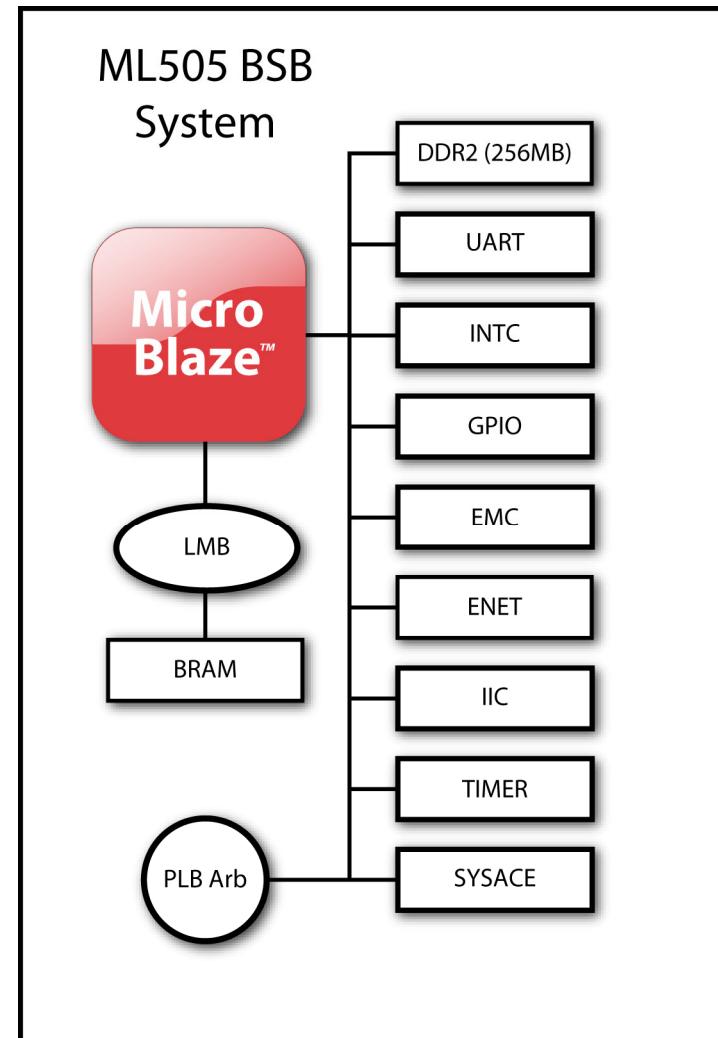
# Overview

- Standard IP Added:
  - External Peripheral Controller – xps\_epc
  - util\_bus\_split
- Standard IP removed:
  - System ACE Controller – xps\_sysace



# ML505 BSB Hardware

- The ML505 MicroBlaze design hardware includes:
  - DDR2 Interface (256 MB)
  - BRAM
  - External Memory Controller (EMC)
    - ZBT SRAM
  - Networking
  - UART
  - Interrupt Controller
  - System ACE CF Interface
  - GPIO (IIC, LEDs and LCD)
  - PLB Arbiter



# Additional Setup Details

- Refer to ml505\_overview\_setup.ppt for details on:
  - Software Requirements
  - ML505 Board Setup
    - Equipment and Cables
    - Software
    - Network
  - Terminal Programs
    - This presentation requires the 9600-8-N-1 Baud terminal setup



# Hardware Setup

- Connect the Xilinx Parallel Cable IV (PC4) to the ML505 board

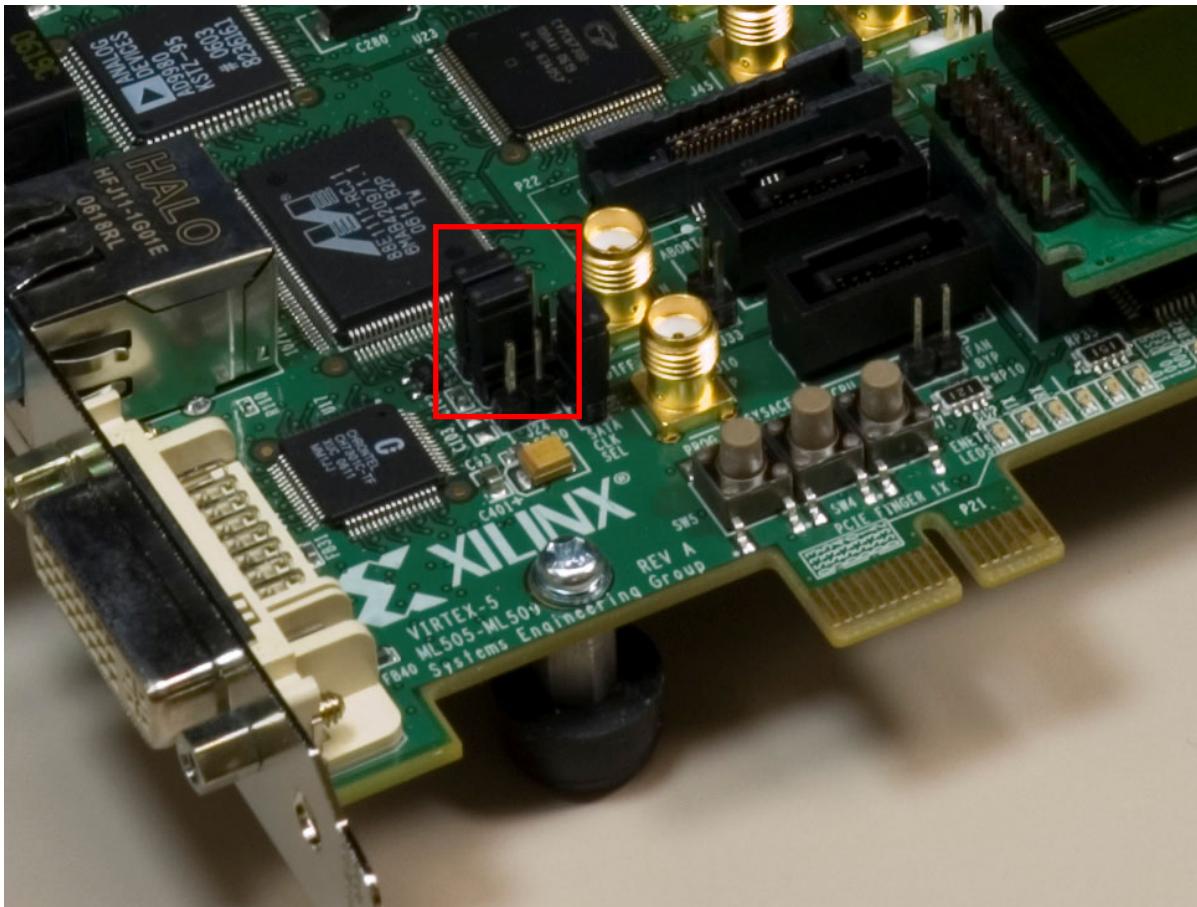


- Connect the RS232 null modem cable to the ML505 board



# Setting Up the Hardware

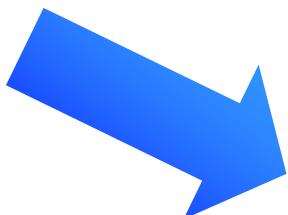
- Set ML505 Jumpers for GMII
  - Set both J22 and J23 to positions 1-2 (as shown)



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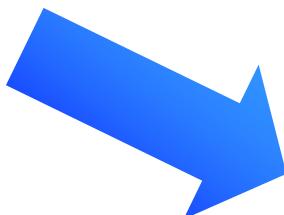
# ISE Software Requirement

- Xilinx ISE 10.1i SP2 software



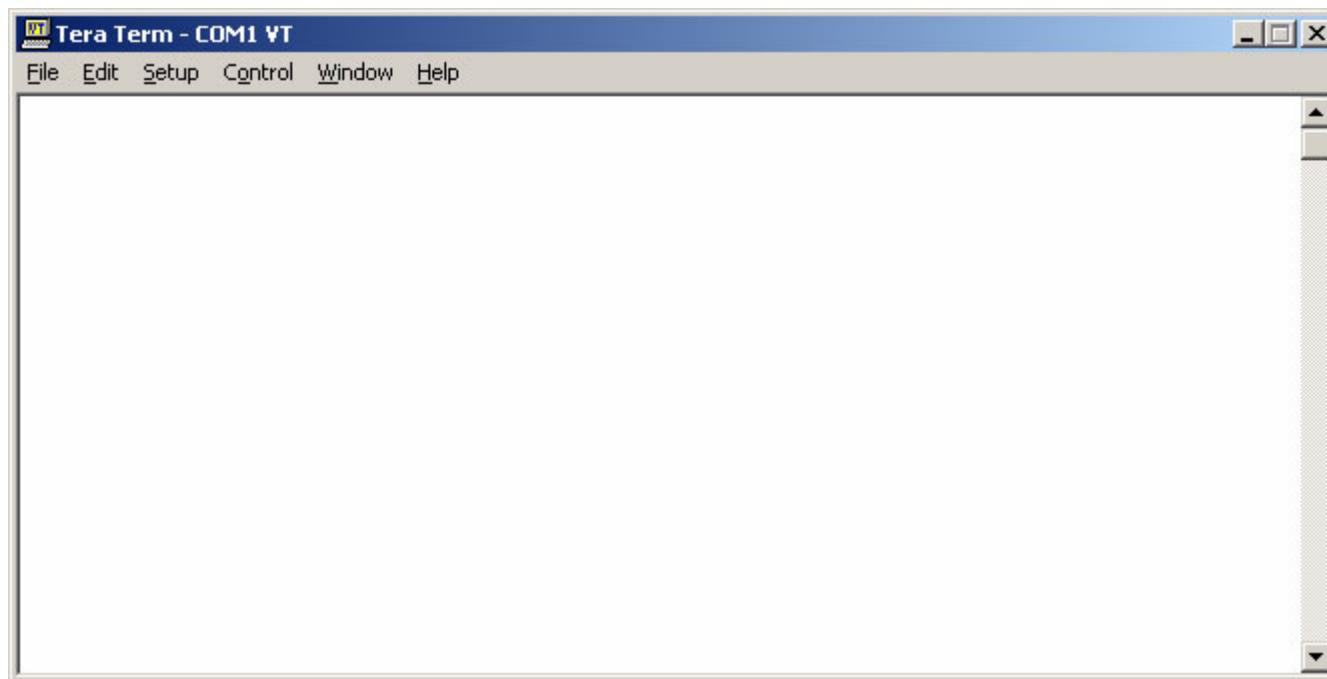
# EDK Software Requirement

- Xilinx EDK 10.1i SP2 software



# Software Setup

- Start the Terminal Program:



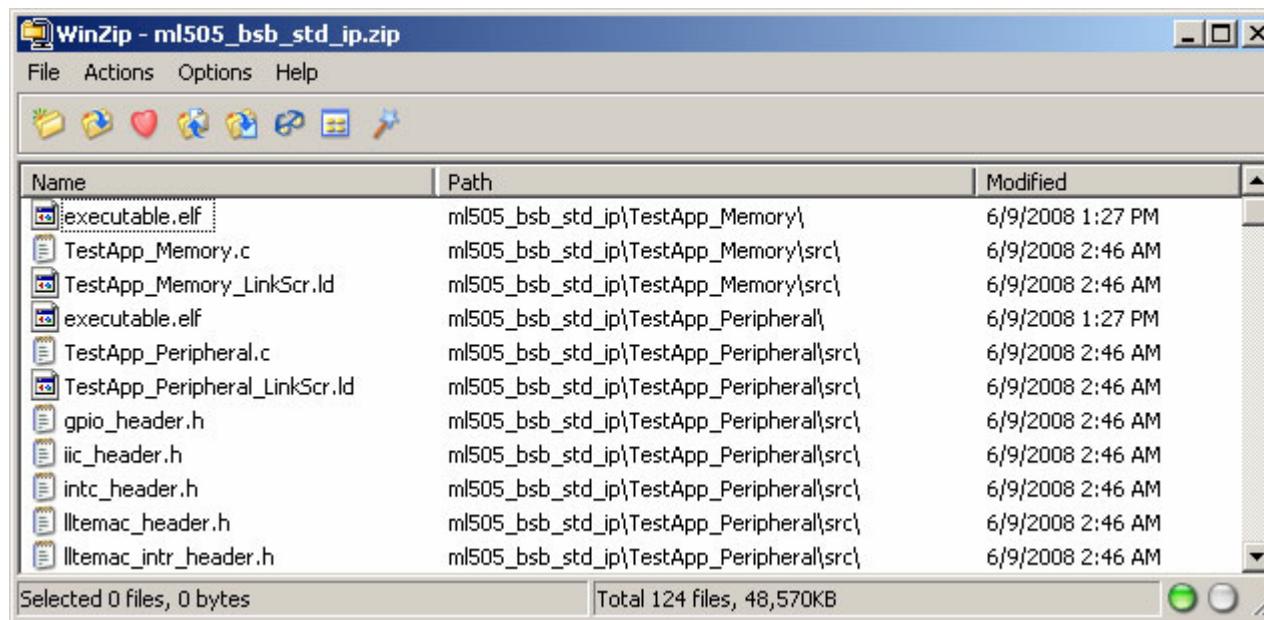
# Using the Pre-Built Design

- Unzip **ml505\_bsb\_std\_ip\_usb.zip** and locate pre-built bitstream and executable software files:
  - ml505\_bsb\_std\_ip\_usb/implementation/download.bit**
  - ml505\_bsb\_std\_ip\_usb/microblaze\_0/code/\*.elf**
- Configure FPGA
  - Launch XPS project, **ml505\_bsb\_system.xmp**
  - From the menu, select **Project → Launch EDK Shell** and type:  
**impact –batch etc/download.cmd**
  - Go to [Slide 52](#), to run the software application
- For a tutorial on how to create the contents of the **ml505\_bsb\_std\_ip\_usb.zip** continue to the next slide



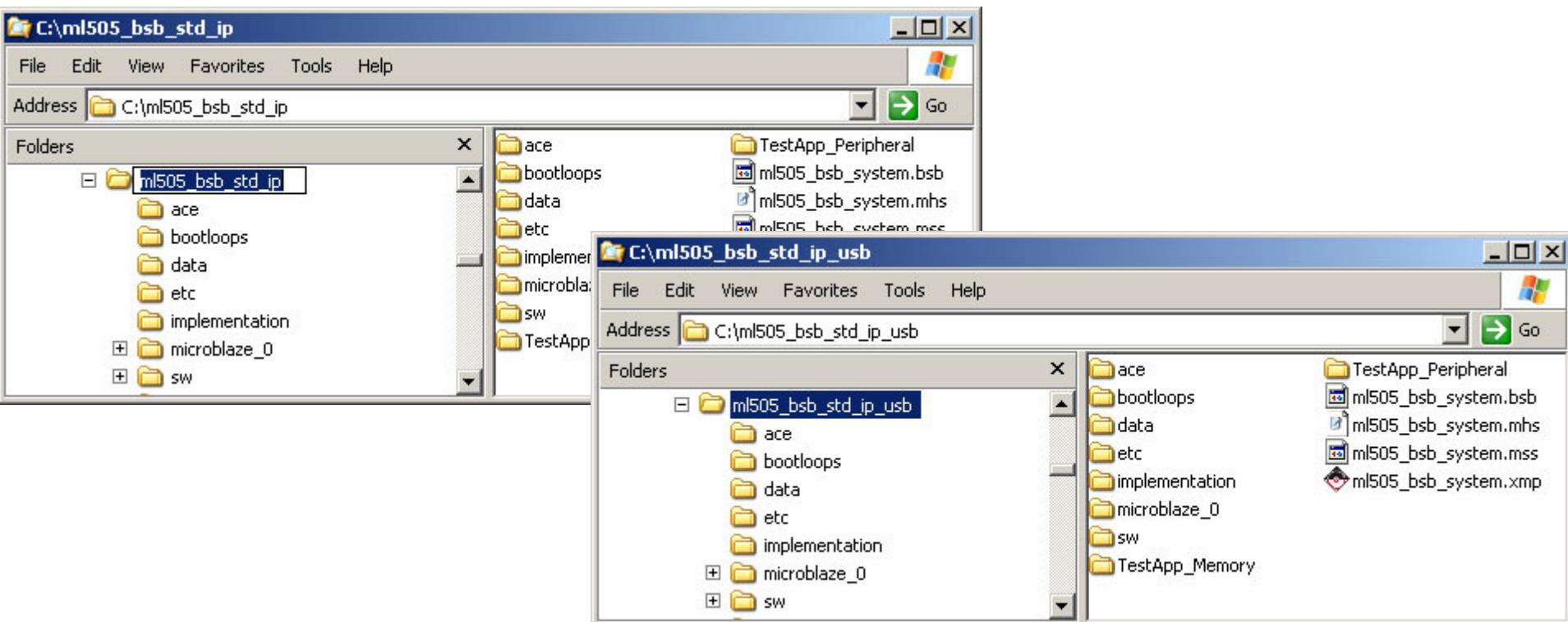
# Extracting the Design

- Unzip the ml505\_bsb\_std\_ip.zip file
  - This creates ISE and EDK project directories



# Extracting the Design

- Rename the project directory to  
**ml505\_bsb\_std\_ip\_usb**

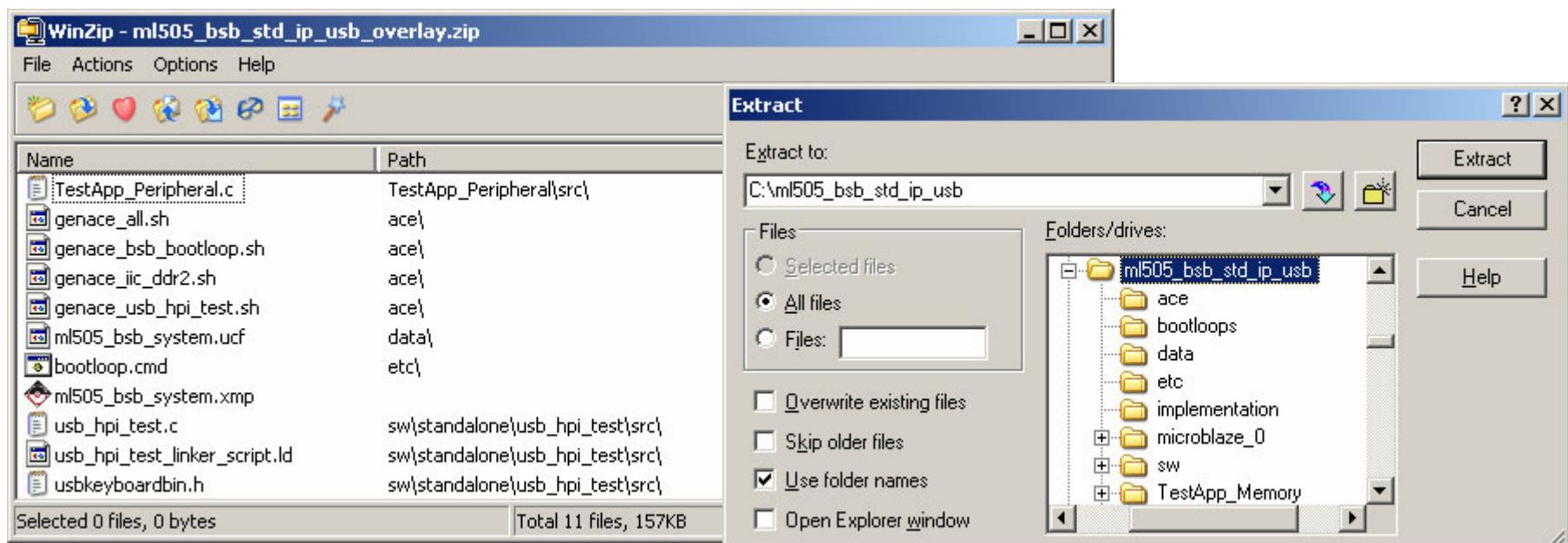


# Design Modifications

- Add overlay files
  - UCF file to match USB Design
  - Software, MSS, and XMP files for USB Design

# Extracting the Design

- Unzip the [ml505\\_bsb\\_std\\_ip\\_usb\\_overlay.zip](#) file
  - Unzip to the ml505\_bsb\_std\_ip\_usb directory
  - UCF file to match USB Design
  - Software, MSS, and XMP files for USB Design

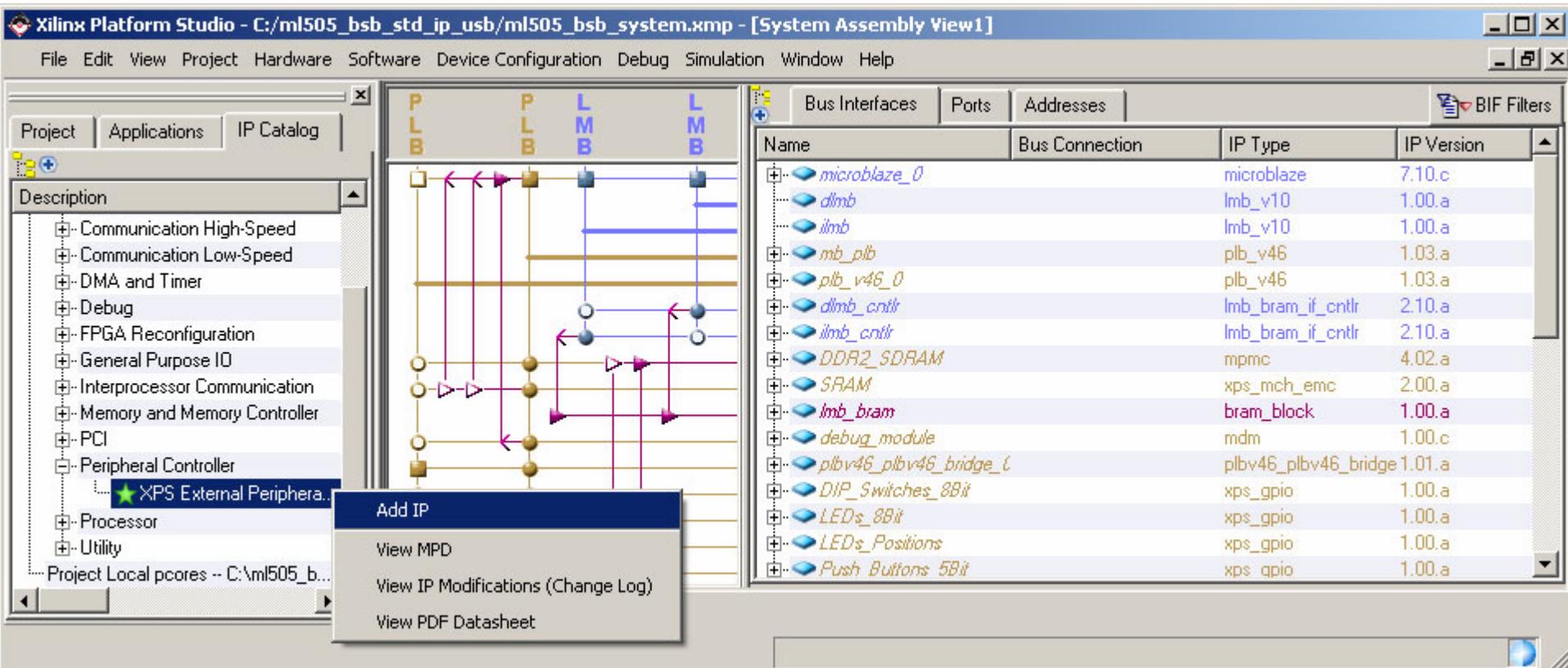


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# Add and Configure IP

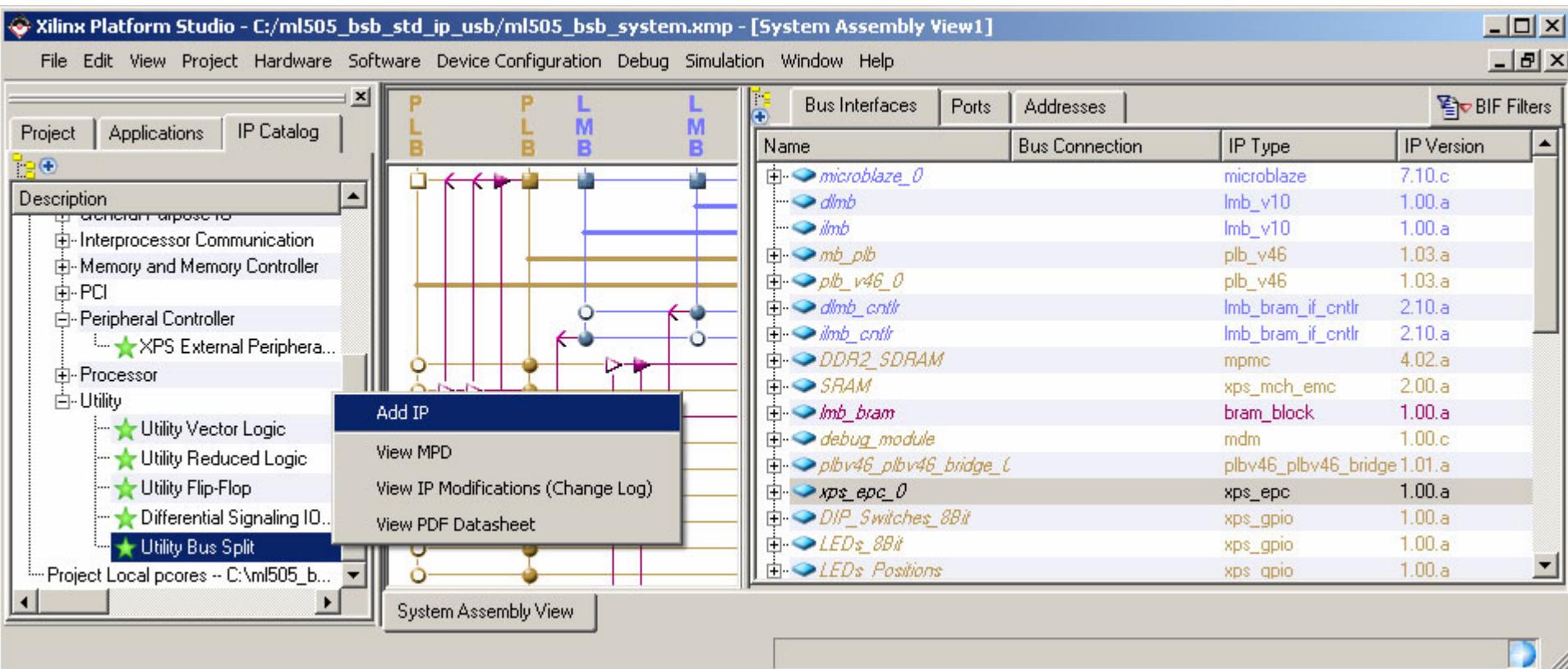
# Add Standard IP

- Launch EDK project <design path>\ml505\_bsb\_system.xmp
- Right-click on the **XPS External Peripheral Controller** and select **Add IP...**



# Add Standard IP

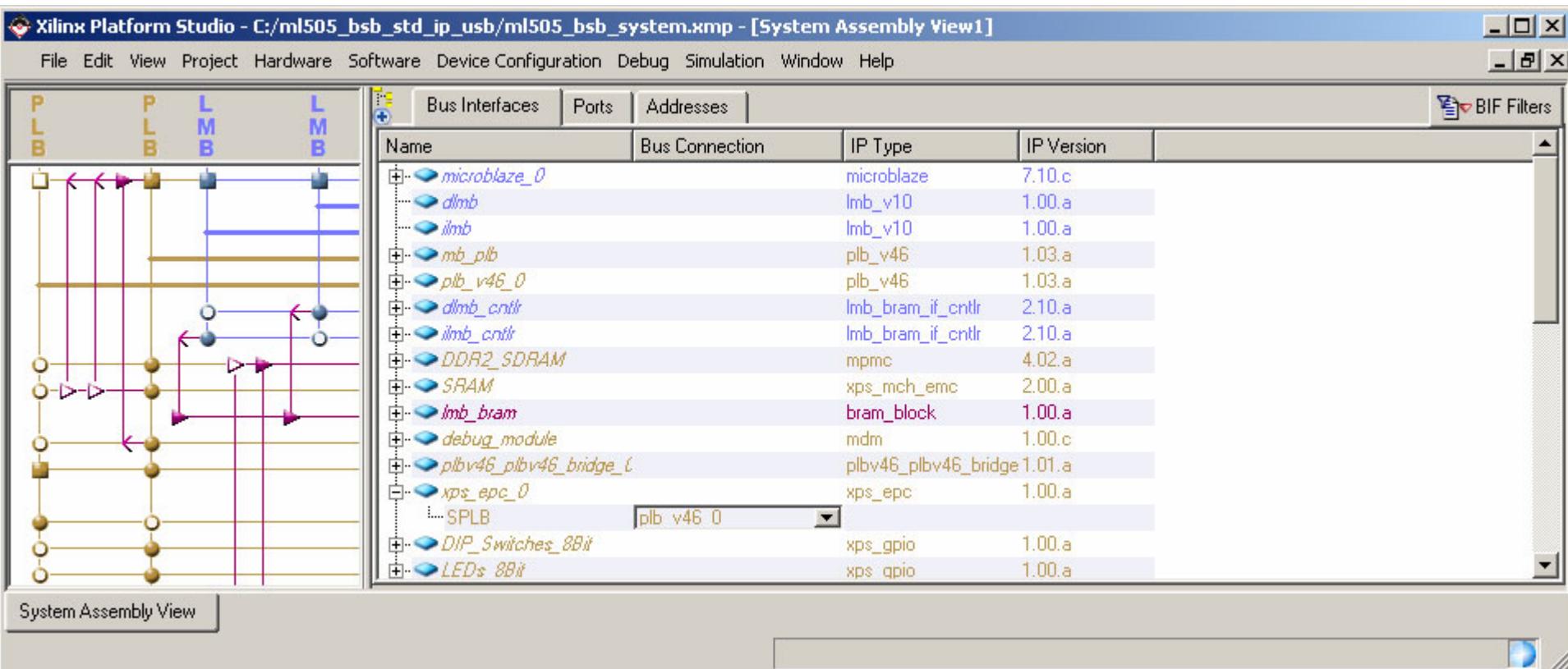
- Right-click on the Utility Bus Split and select Add IP...



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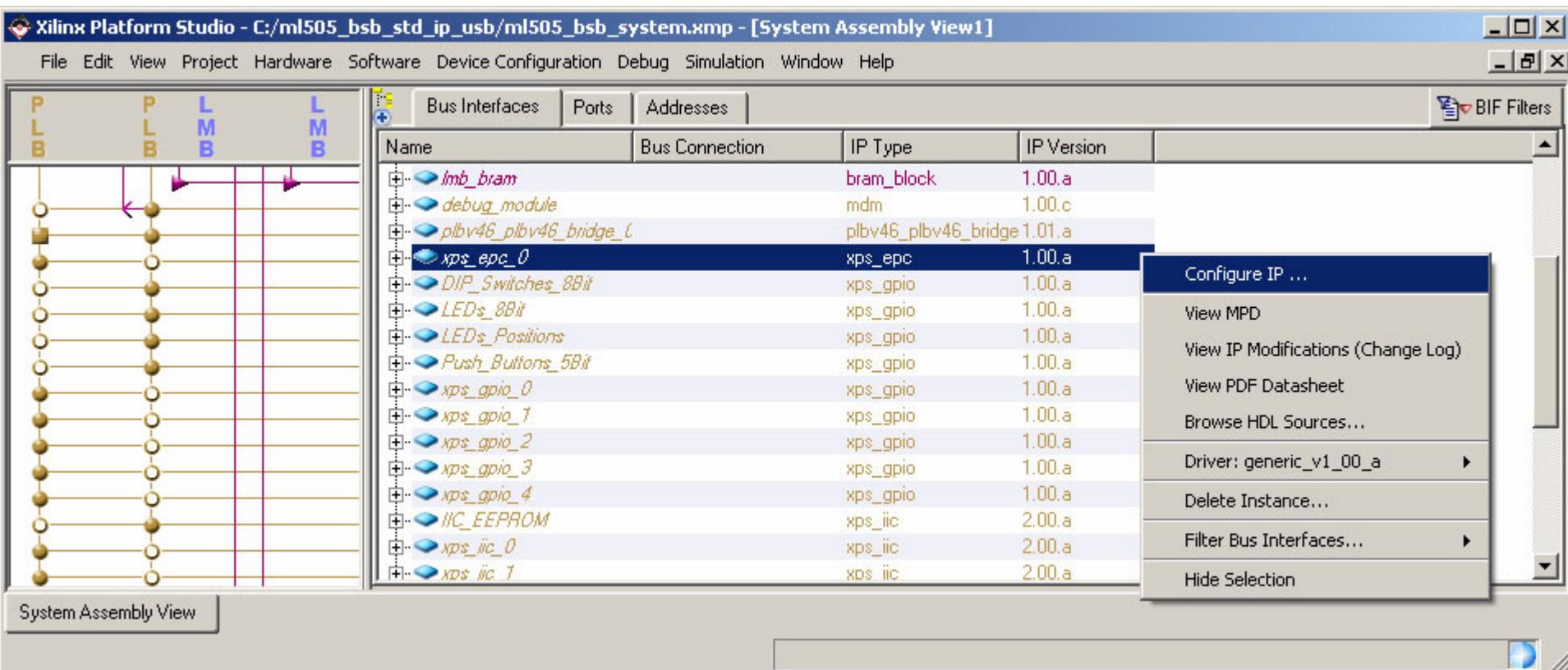
# Connect Buses

- Connect **xps\_epc\_0** to **plb\_v46\_0**



# Add Standard IP

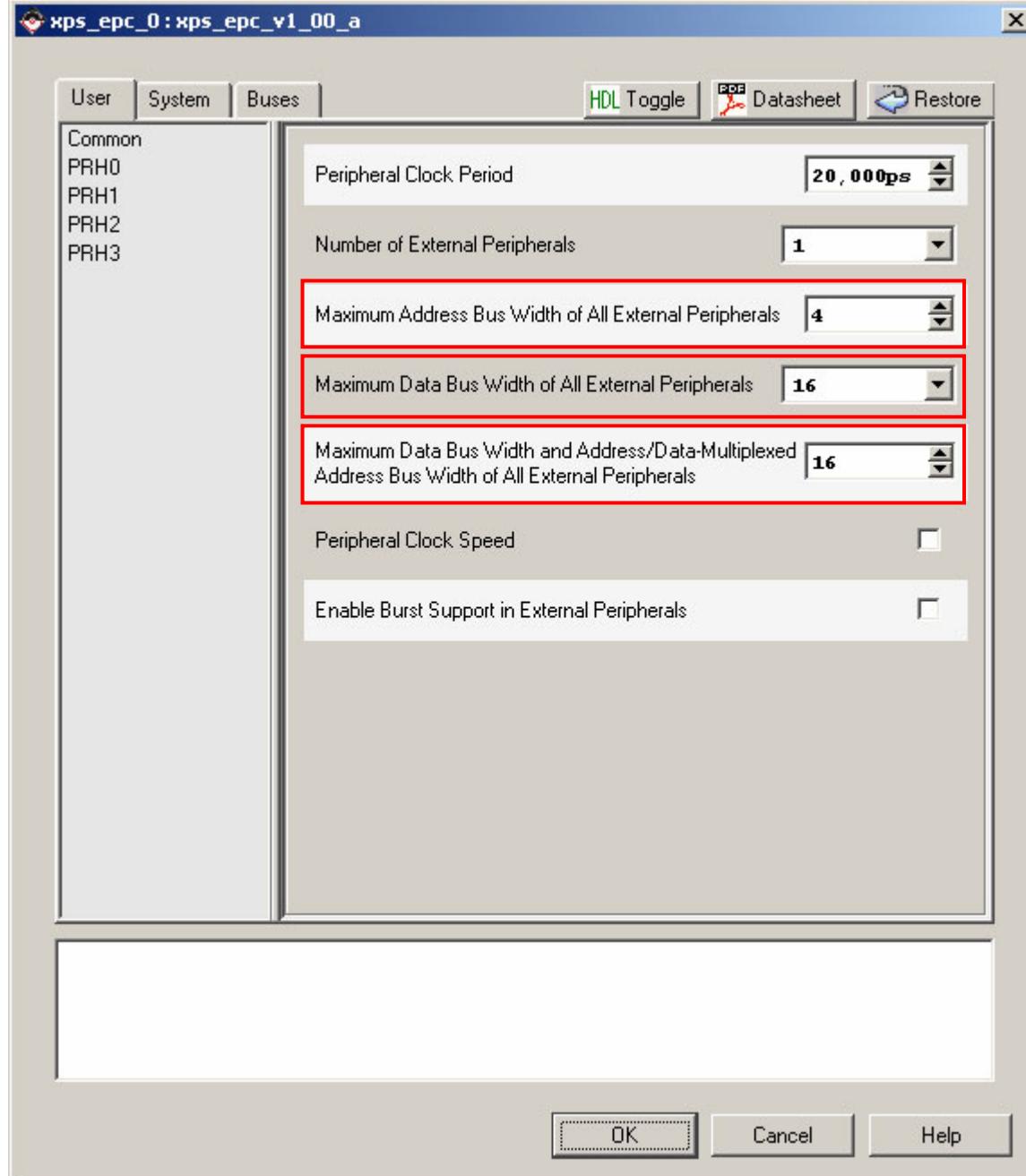
- Right-click on the **xps\_epc\_0** and select **Configure IP...**



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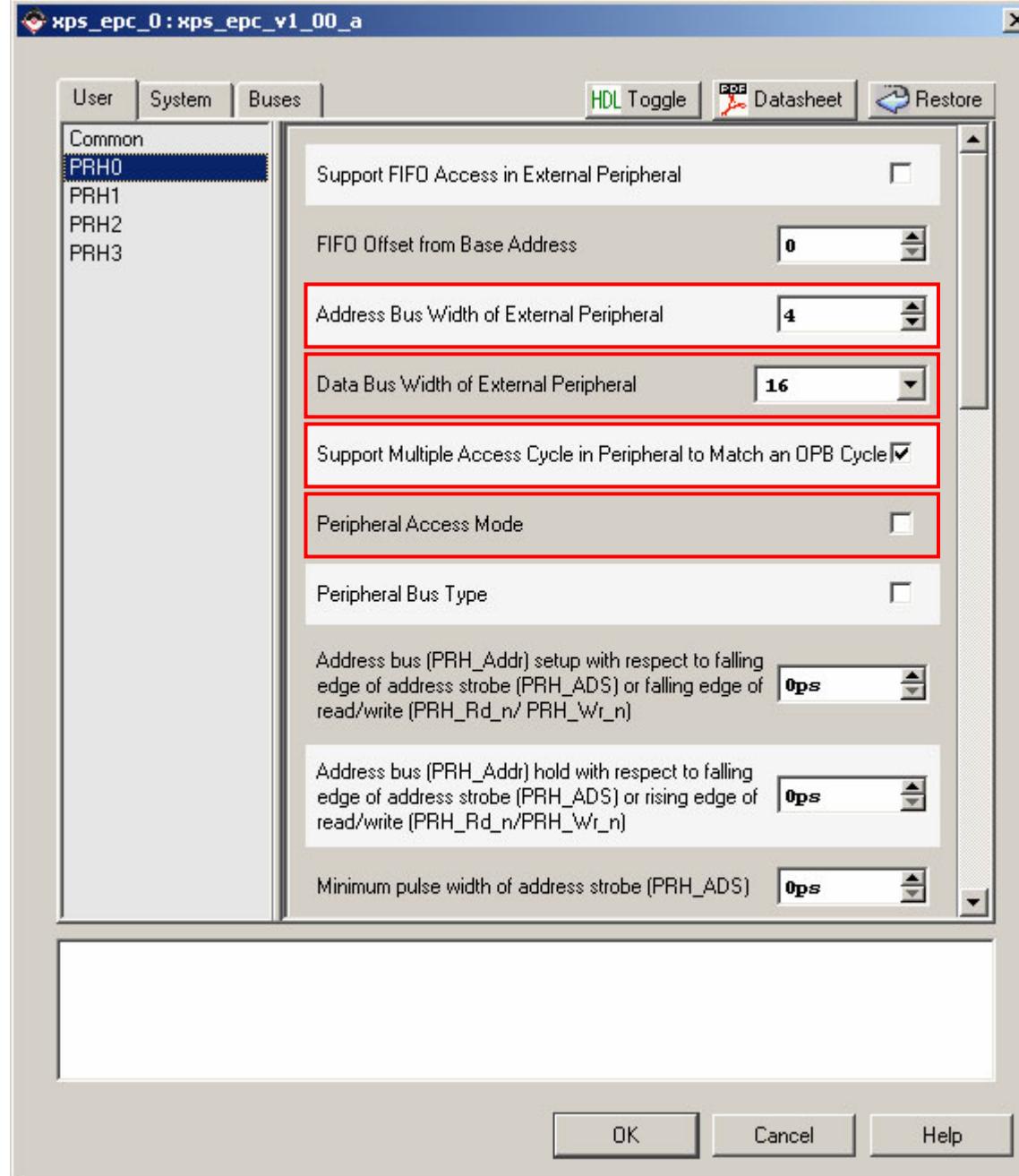
# Configure IP

- Under the Common tab, set the following parameters:
  - Set Max Addr Bus Width to **4**
  - Set Max Data Bus Width to **16**
  - Set Max Multiplexed Addr/Data Bus Width to **16**



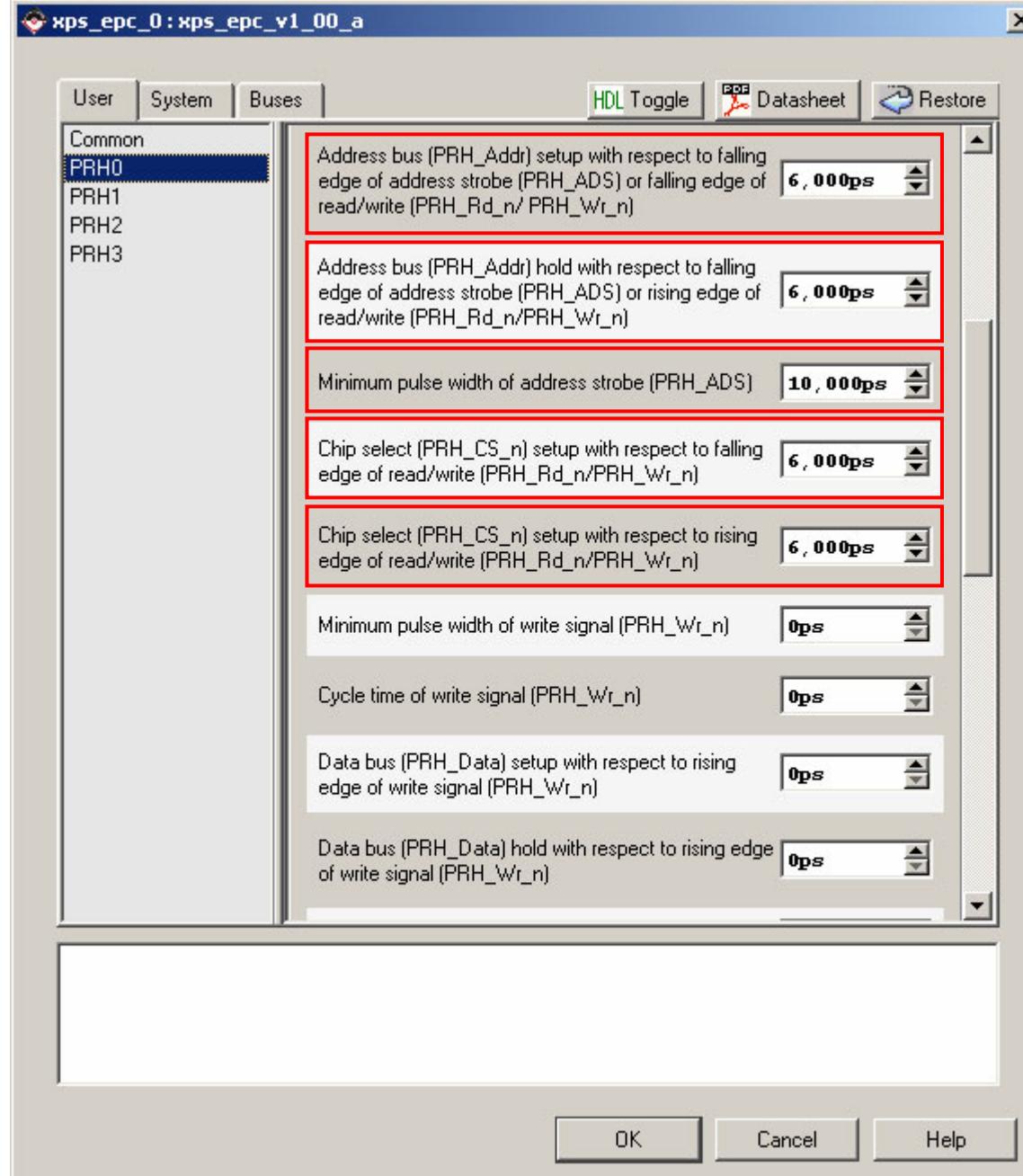
# Configure IP

- Under the PRH0 tab, set the following parameters:
  - Set Addr Bus Width to 4
  - Set Data Bus Width to 16
  - Select the Multiple Access Cycle option
  - De-select the Peripheral Access Mode option



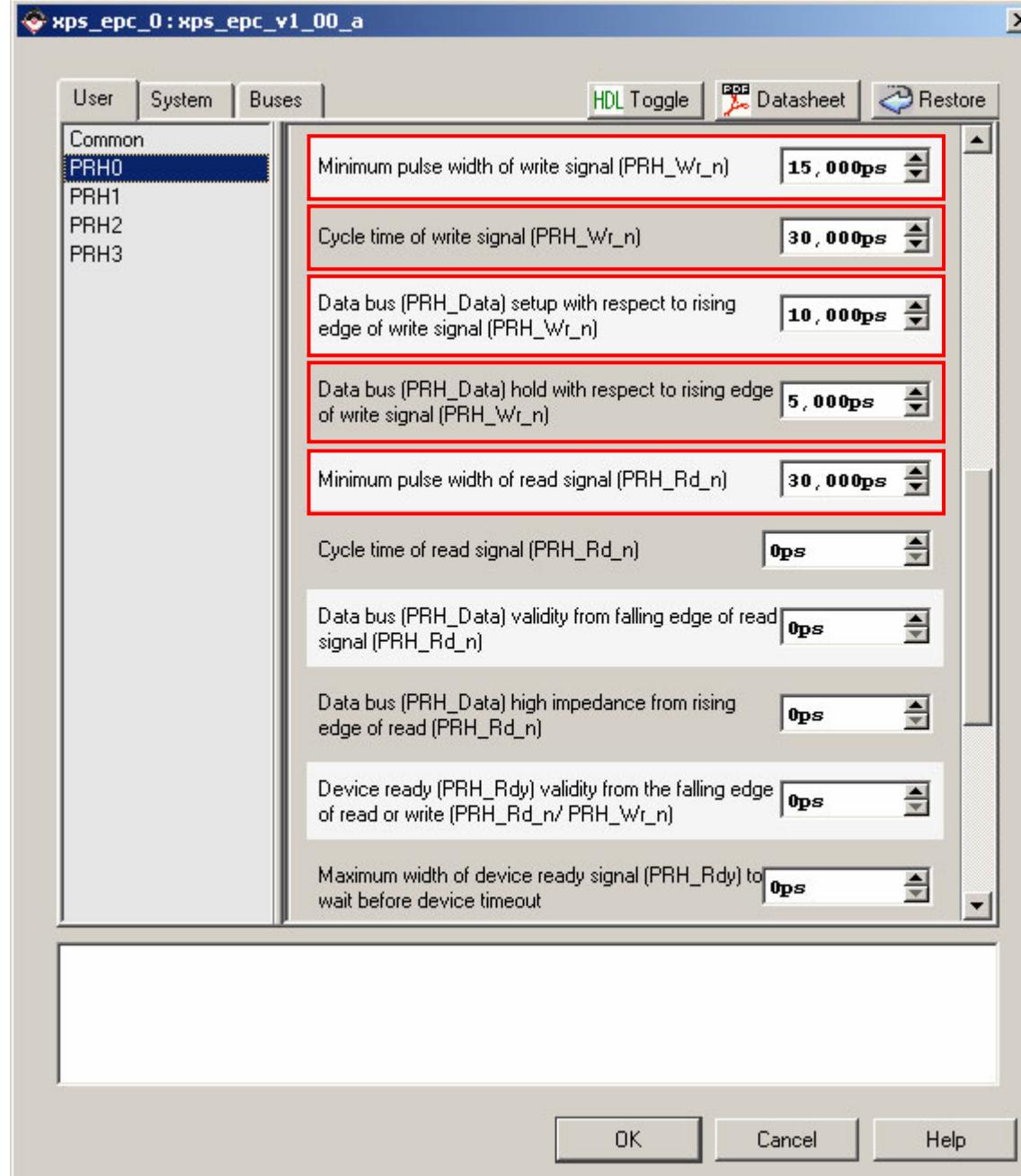
# Configure IP

- Under the PRH0 tab, set the following parameters:
  - Set Addr TSU (Setup) to **6000ps**
  - Set Addr TH (Hold) to **6000ps**
  - Set Min Pulse Width to **10000ps**
  - Set Chip Select TSU to **6000ps**
  - Set Chip Select TH to **6000ps**



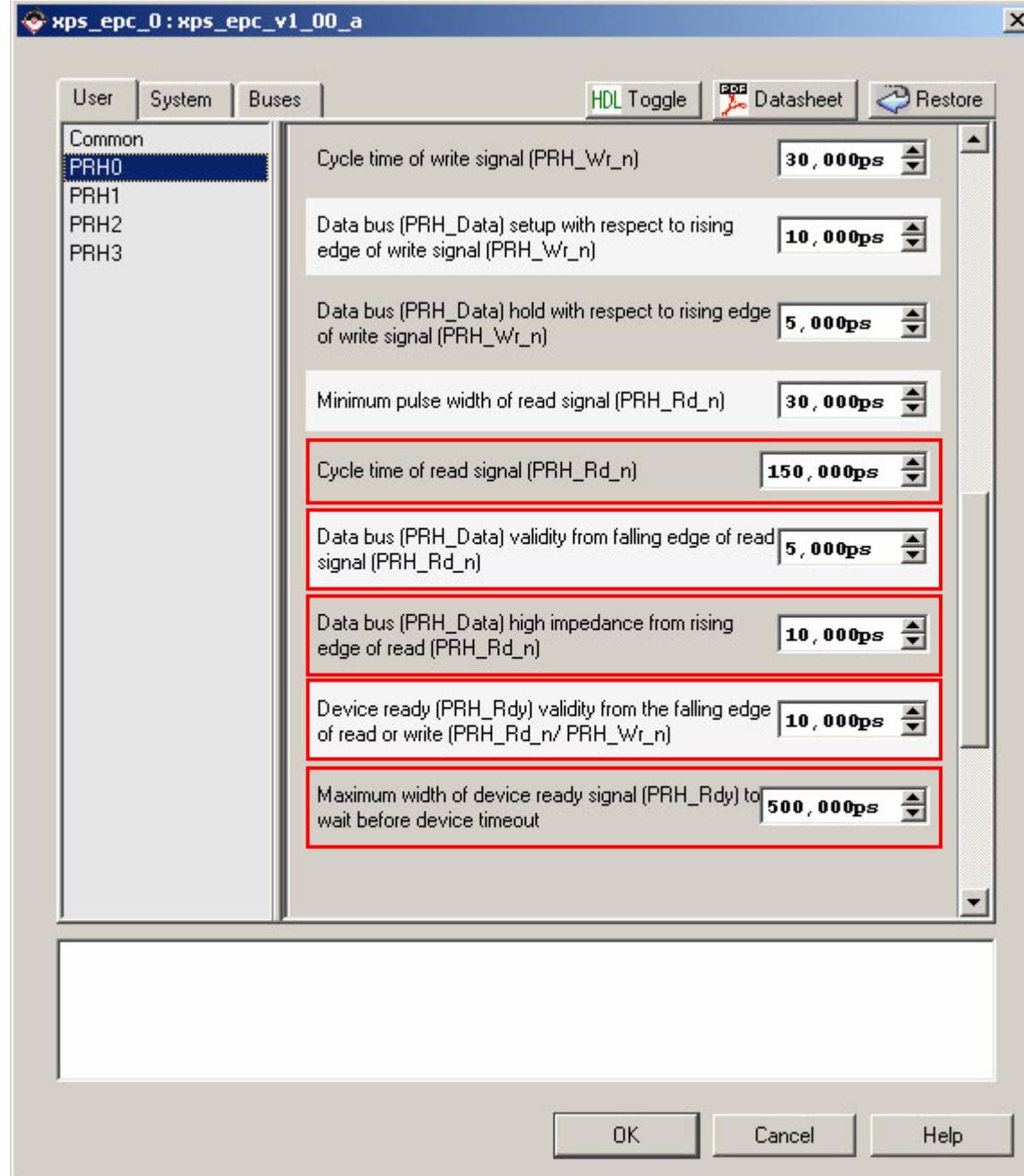
# Configure IP

- Under the PRH0 tab, set the following parameters:
  - Set Write Min Pulse Width to **15000ps**
  - Set Write Cycle Time to **30000ps**
  - Set Data TSU to **10000ps**
  - Set Data TH to **5000ps**
  - Set Read Min Pulse Width to **30000ps**



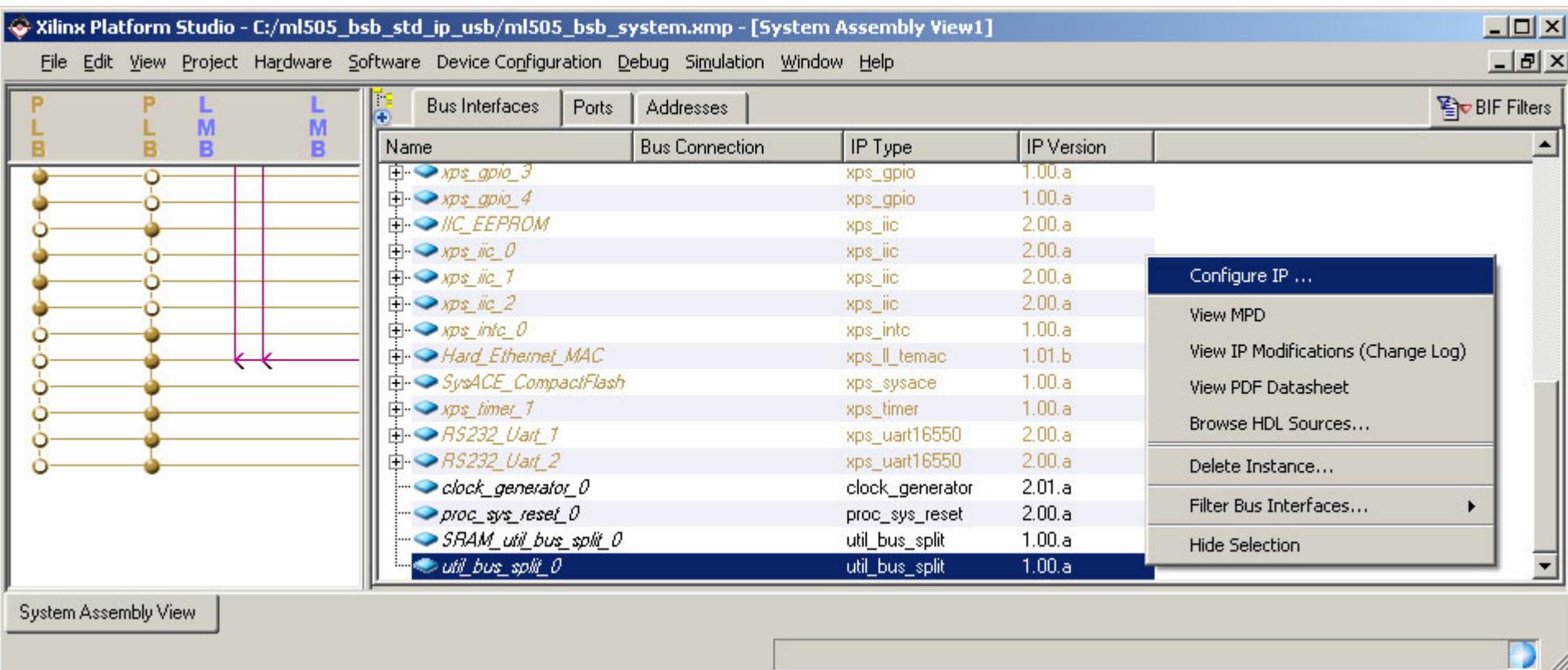
# Configure IP

- Under the PRH0 tab, set the following parameters:
  - Set Read Cycle Time to **15000ps**
  - Set Data Bus Valid to **5000ps**
  - Set Data Bus Hi-Z to **10000ps**
  - Set Device Ready Valid to **10000ps**
  - Set Max Ready Width (Timeout) to **500000ps**



# Add Standard IP

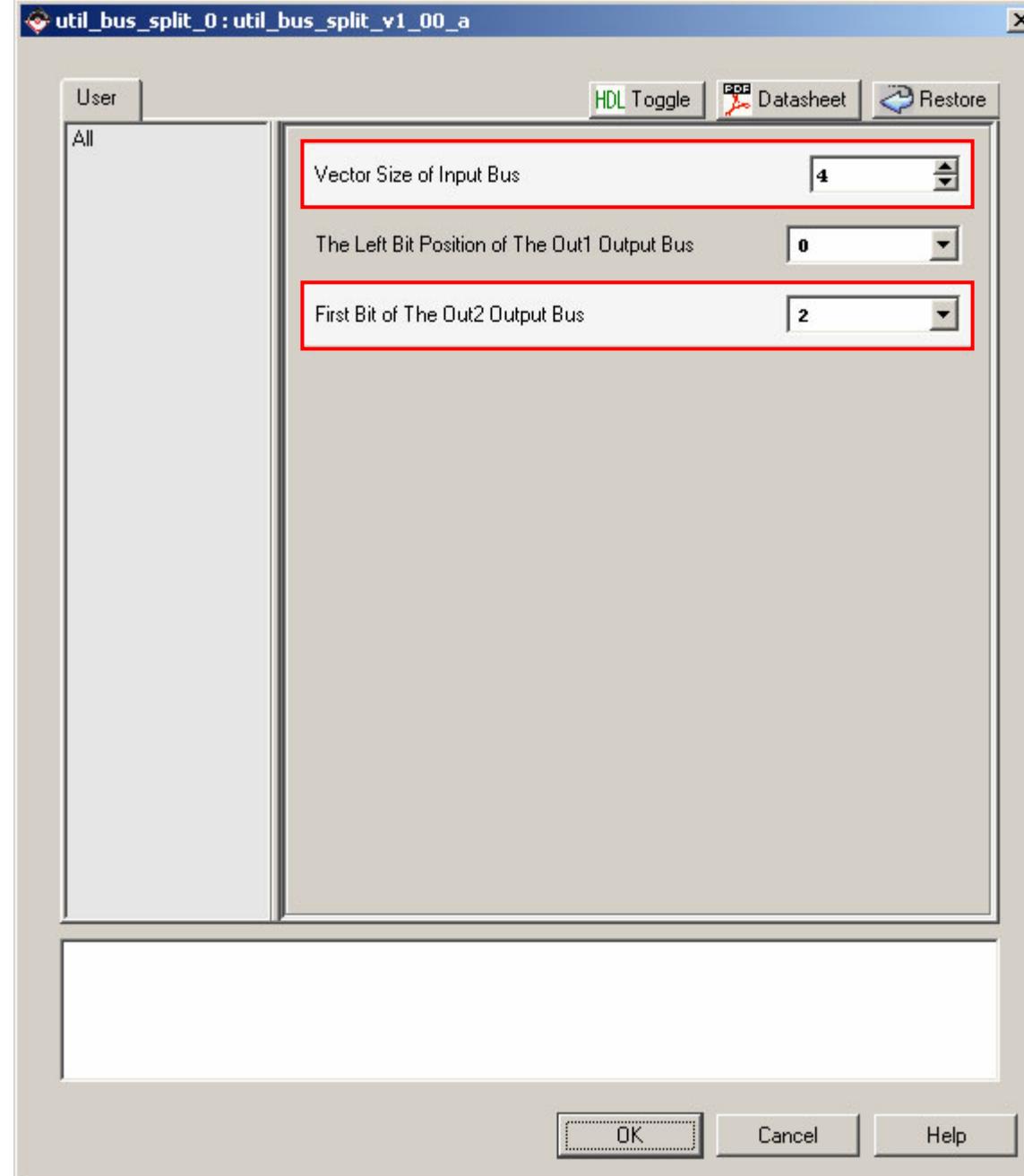
- Right-click on the util\_bus\_split\_0 and select Configure IP...



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# Configure IP

- Under the All tab, set the following parameters:
  - Input Vector Size: **4**
  - First Bit of Out2 Bus: **2**



# Generate Addresses

- Select the Address Tab
- The **xps\_epc\_0** addresses are not yet assigned

Xilinx Platform Studio - C:/ml505\_bsb\_std\_ip\_usb/ml505\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Generate Addresses

Instance	Name	Base Address	High Address	Size	Lock	Bus Interface(s)	Bus Connection
mb_plb	C_BASEADDR			U	<input type="checkbox"/>	Not Applicable	
plb_v46_0	C_BASEADDR			U	<input type="checkbox"/>	Not Applicable	
xps_epc_0	C_PRH0_BASEADDR			U	<input type="checkbox"/>	SPLB	plb_v46_0
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	ilmb
LEDs_8Bit	C_BASEADDR	0x81400000	0x8140ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
LEDs_Positions	C_BASEADDR	0x81420000	0x8142ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
Push-buttons_5Bit	C_BASEADDR	0x81440000	0x8144ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
DIP_Switches_8Bit	C_BASEADDR	0x81460000	0x8146ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_gpio_4	C_BASEADDR	0x81480000	0x8148ffff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
plbv46_plbv46_bridg...	C_RNG0_BASEADDR	0x81480000	0x814fffff	512K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_gpio_3	C_BASEADDR	0x814a0000	0x814affff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
xps_gpio_1	C_BASEADDR	0x814c0000	0x814cffff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
xps_gpio_2	C_BASEADDR	0x814e0000	0x814effff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0

System Assembly View



# Generate Addresses

- Click Generate Addresses and view the new addresses

Xilinx Platform Studio - C:/ml505\_bsb\_std\_ip\_usb/ml505\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses

Instance	Name	Base Address	High Address	Size	Lock	Bus Interface(s)	Bus Connection
mb_plb	C_BASEADDR			U	<input checked="" type="checkbox"/>	Not Applicable	
plb_v46_0	C_BASEADDR			U	<input checked="" type="checkbox"/>	Not Applicable	
xps_epc_0	C_PRHO_BASEADDR	0x80800000	0x8080ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	ilmb
LEDs_8Bit	C_BASEADDR	0x81400000	0x8140ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
LEDs_Positions	C_BASEADDR	0x81420000	0x8142ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
Push-buttons_5Bit	C_BASEADDR	0x81440000	0x8144ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
DIP_Switches_8Bit	C_BASEADDR	0x81460000	0x8146ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_gpio_4	C_BASEADDR	0x81480000	0x8148ffff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
plbv46_plbv46_bridge_0_C_RNG0_BASEADDR	C_RNG0_BASEADDR	0x81480000	0x814fffff	512K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_gpio_3	C_BASEADDR	0x814a0000	0x814affff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
xps_gpio_1	C_BASEADDR	0x814c0000	0x814cffff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
xps_gpio_2	C_BASEADDR	0x814e0000	0x814effff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0

System Assembly View



# Lock Addresses

- Lock the new addresses

Xilinx Platform Studio - C:/ml505\_bsb\_std\_ip\_usb/ml505\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Generate Addresses

Instance	Name	Base Address	High Address	Size	Lock	Bus Interface(s)	Bus Connection
mb_plb	C_BASEADDR			U	<input type="checkbox"/>	Not Applicable	
plb_v46_0	C_BASEADDR			U	<input type="checkbox"/>	Not Applicable	
xps_epc_0	C_PRHO_BASEADDR	0x80800000	0x8080ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	dlmb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000ffff	64K	<input checked="" type="checkbox"/>	SLMB	ilmb
LEDs_8Bit	C_BASEADDR	0x81400000	0x8140ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
LEDs_Positions	C_BASEADDR	0x81420000	0x8142ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
Push-buttons_5Bit	C_BASEADDR	0x81440000	0x8144ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
DIP_Switches_8Bit	C_BASEADDR	0x81460000	0x8146ffff	64K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_gpio_4	C_BASEADDR	0x81480000	0x8148ffff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
plbv46_plbv46_bridge_0_C_RNG0_BASEADDR	C_RNG0_BASEADDR	0x81480000	0x814fffff	512K	<input checked="" type="checkbox"/>	SPLB	mb_plb
xps_gpio_3	C_BASEADDR	0x814a0000	0x814affff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
xps_gpio_1	C_BASEADDR	0x814c0000	0x814cffff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0
xps_gpio_2	C_BASEADDR	0x814e0000	0x814effff	64K	<input checked="" type="checkbox"/>	SPLB	plb_v46_0

System Assembly View



# Connect Ports

- Click on the Ports Tab and expand the **xps\_epc\_0**
- Connect **PRH\_Rdy** and **PRH\_Clk** to **net\_vcc**

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
PRH_Data_T	No Connection	0	[0:(C_PRH_MAX_AD...]			
PRH_Data_O	No Connection	0	[0:(C_PRH_MAX_AD...]			
PRH_Data_I	No Connection	1	[0:(C_PRH_MAX_AD...]			
PRH_Data	No Connection	I0	[0:(C_PRH_MAX_AD...]			
PRH_Rdy	net_vcc	I	[0:(C_NUM_PERIPHE...]			
PRH_Burst	No Connection	0				
PRH_Wr_n	No Connection	0				
PRH_Rd_n	No Connection	0				
PRH_RNW	No Connection	0				
PRH_BE	No Connection	0	[0:(C_PRH_MAX_DW...]			
PRH_ADS	No Connection	0				
PRH_Addr	No Connection	0	[0:(C_PRH_MAX_AWI...]			
PRH_CS_n	No Connection	0	[0:(C_NUM_PERIPHE...]			
PRH_Rst	No Connection	I	RST			
PRH_Clk	net_vcc	I	CLK			

# Connect Ports

- Make these nets external: **PRH\_CS\_n**, **PRH\_Rd\_n**, **PRH\_Wr\_n**, and **PRH\_Data**

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
PRH_Data_T	No Connection	0	[0:(C_PRH_MAX_AD...]			
PRH_Data_0	No Connection	0	[0:(C_PRH_MAX_AD...]			
PRH_Data_I	No Connection	1	[0:(C_PRH_MAX_AD...]			
PRH_Data	xps epc 0 PRH Data	I/O	[0:(C_PRH_MAX_AD...]			
PRH_Rdy	net vcc	1	[0:(C_NUM_PERIPHE...]			
PRH_Burst	No Connection	0				
PRH_Wr_n	xps epc 0 PRH Wr n	0				
PRH_Rd_n	xps epc 0 PRH Rd n	0				
PRH_RNW	No Connection	0				
PRH_BE	No Connection	0	[0:(C_PRH_MAX_DW...]			
PRH_ADS	No Connection	0				
PRH_Addr	No Connection	0	[0:(C_PRH_MAX_AWI...]			
PRH_CS_n	xps epc 0 PRH CS n	0	[0:(C_NUM_PERIPHE...]			
PRH_Rst	No Connection	1		RST		
PRH_Clk	net vcc	1		CLK		



# Connect Ports

- Connect PRH\_Addr to xps\_epc\_0\_PRH\_Addr\_split

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
PRH_Data_T	No Connection	0	[0:(C_PRH_MAX_AD...]			
PRH_Data_O	No Connection	0	[0:(C_PRH_MAX_AD...]			
PRH_Data_I	No Connection	I	[0:(C_PRH_MAX_AD...]			
PRH_Data	xps epc 0 PRH Data	IO	[0:(C_PRH_MAX_AD...]			
PRH_Rdy	net vcc	I	[0:(C_NUM_PERIPHE...]			
PRH_Burst	No Connection	0				
PRH_Wr_n	xps epc 0 PRH Wr n	0				
PRH_Rd_n	xps epc 0 PRH Rd n	0				
PRH_RNW	No Connection	0				
PRH_BE	No Connection	0	[0:(C_PRH_MAX_DW...]			
PRH_ADS	No Connection	0				
PRH_Addr	xps epc 0 PRH Addr split	0	[0:(C_PRH_MAX_AWI...]			
PRH_CS_n	xps epc 0 PRH CS n	0	[0:(C_NUM_PERIPHE...]			
PRH_Rst	No Connection	I		RST		
PRH_Clk	net vcc	I		CLK		

# Connect Ports

- Expand the **util\_bus\_split\_0**
- Connect **Sig** to **xps\_epc\_0\_PRH\_Addr\_split**
- Connect **Out1** to **xps\_epc\_0\_PRH\_Addr**

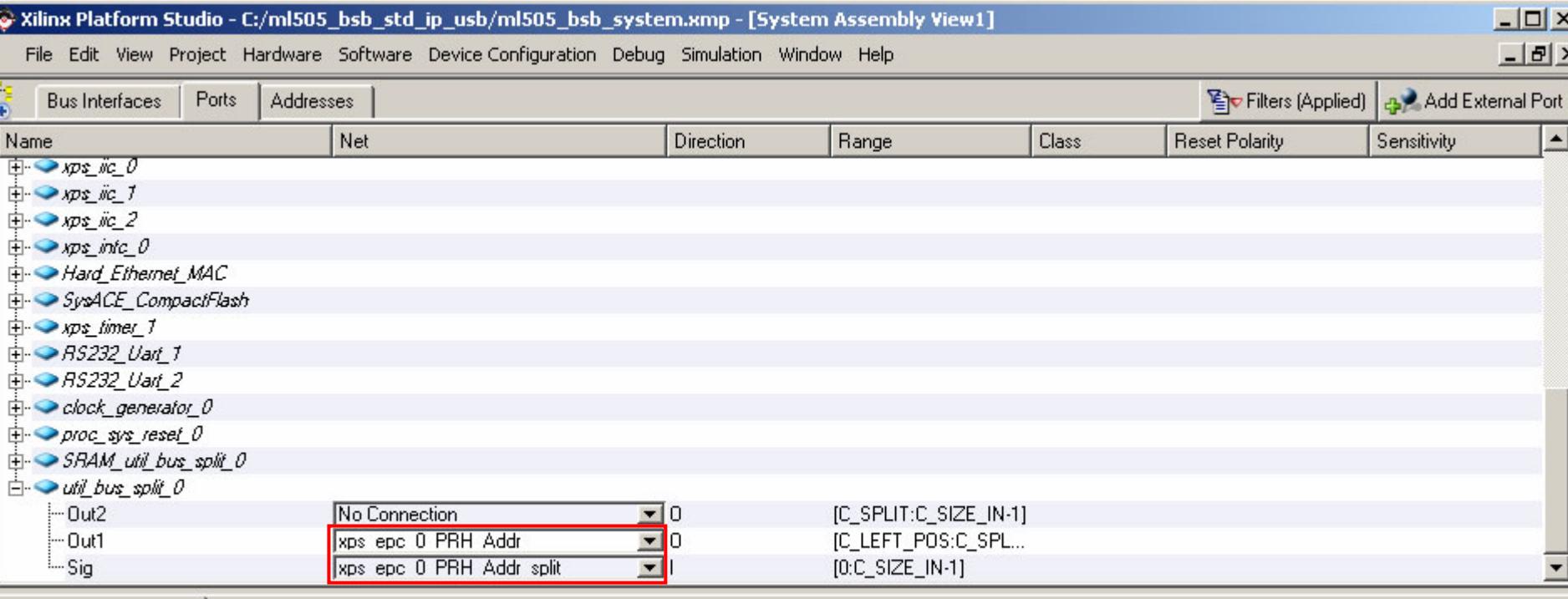
Xilinx Platform Studio - C:/ml505\_bsb\_std\_ip\_usb/ml505\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
+ xps_iic_0						
+ xps_iic_1						
+ xps_iic_2						
+ xps_ifc_0						
+ Hard_Ethernet_MAC						
+ SysACE_CompactFlash						
+ xps_timer_1						
+ RS232_Uart_1						
+ RS232_Uart_2						
+ clock_generator_0						
+ proc_sys_reset_0						
+ SRAM_util_bus_split_0						
- util_bus_split_0						
- Out2	No Connection	0	[C_SPLIT:C_SIZE_IN-1]			
- Out1	xps epc 0 PRH Addr	0	[C_LEFT_POS:C_SPL...			
- Sig	xps epc 0 PRH Addr split	1	[0:C_SIZE_IN-1]			

System Assembly View



# Connect Ports

- Add three external ports
- Connect these ports as shown on the next slide

Xilinx Platform Studio - C:/ml505\_bsb\_std\_ip\_usb/ml505\_bsb\_system.xmp - [System Assembly View1]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Bus Interfaces Ports Addresses Filters (Applied) Add External Port

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
External Ports						
ExternalPort_2	net ExternalPort 2	0				
ExternalPort_1	net ExternalPort 1	0				
ExternalPort_0	net ExternalPort 0	0				
xps_epc_0_PRH_Data	xps epc 0 PRH Data	I/O	[15:0]			
xps_epc_0_PRH_Wr_n_pin	xps epc 0 PRH Wr n	0				
xps_epc_0_PRH_Rd_n_pin	xps epc 0 PRH Rd n	0				
xps_epc_0_PRH_CS_n_pin	xps epc 0 PRH CS n	0	[0:0]			
SRAM_Mem_LBON_pin	SRAM Mem LBON	0				
xps_iic_2_Sda	xps iic 2 Sda	I/O				
xps_iic_2_Scl	xps iic 2 Scl	I/O				
xps_iic_1_Sda	xps iic 1 Sda	I/O				
xps_iic_1_Scl	xps iic 1 Scl	I/O				
xps_iic_0_Sda	xps iic 0 Sda	I/O				
xps_iic_0_Scl	xps iic 0 Scl	I/O				
xps_iic_0_Gpo_pin	xps iic 0 Gpo	0	[31:31]			

System Assembly View



# Connect Ports

- Name: **usb\_hpi\_reset\_n\_pin** Net: **sys\_rst\_s**, Direction Out, Class RST, and Reset Polarity set to “1”
- Name: **usb\_hpi\_int\_pin** Net: **usb\_hpi\_int**, Direction In, Class INTERRUPT, and Sensitivity set to LEVEL\_HIGH
- Name: **xps\_epc\_0\_PRH\_Addr\_pin** Net: **xps\_epc\_0\_PRH\_Addr**, Direction Out, and Range set to [0:1]

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_epc_0_PRH_Addr_pin	xps epc 0 PRH Addr	[0]	[0:1]			
usb_hpi_int_pin	usb hpi int	[I]		INTERRUPT		LEVEL HIGH
usb_hpi_reset_n_pin	sys rst s	[0]		RST	[1]	
xps_epc_0_PRH_Data	xps epc 0 PRH Data	[0]	[0:15]			
xps_epc_0_PRH_Wr_n_pin	xps epc 0 PRH Wr n	[0]				
xps_epc_0_PRH_Rd_n_pin	xps epc 0 PRH Rd n	[0]				
xps_epc_0_PRH_CS_n_pin	xps epc 0 PRH CS n	[0]	[0:0]			
SRAM_Mem_LBON_pin	SRAM Mem LBON	[0]				



# Connect Ports

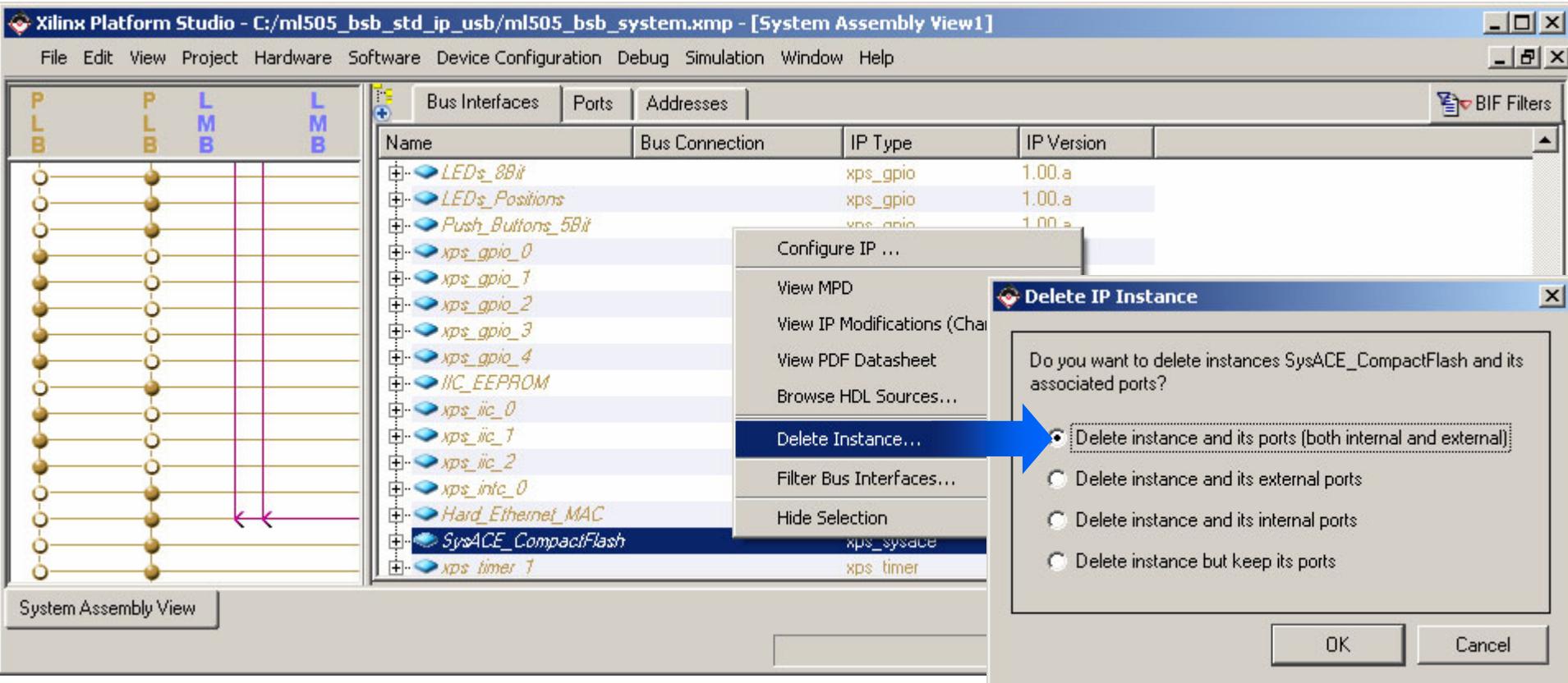
- On external port **xps\_epc\_0\_PRH\_Data\_pin**, change the range from **[0:15]** to **[15:0]**

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
<b>xps_epc_0_PRH_Data</b>	xps epc 0 PRH Data	I/O	<b>[15:0]</b>			
xps_epc_0_PRH_Addr_pin	xps epc 0 PRH Addr	I/O	[0:1]			
usb_hpi_int_pin	usb hpi int	I		INTERRUPT		LEVEL HIGH
usb_hpi_reset_n_pin	sys rst s	O		RST	1	
xps_epc_0_PRH_Wr_n_pin	xps epc 0 PRH Wr n	O				
xps_epc_0_PRH_Rd_n_pin	xps epc 0 PRH Rd n	O				
xps_epc_0_PRH_CS_n_pin	xps epc 0 PRH CS n	O	[0:0]			
SRAM_Mem_LBON_pin	SRAM Mem LBON	O				
xps_iic_2_Sda	xps iic 2 Sda	I/O				
xps_iic_2_Scl	xps iic 2 Scl	I/O				
xps_iic_1_Sda	xps iic 1 Sda	I/O				
xps_iic_1_Scl	xps iic 1 Scl	I/O				
xps_iic_0_Sda	xps iic 0 Sda	I/O				
xps_iic_0_Scl	xps iic 0 Scl	I/O				
xps_iic_0_Gnd_pin	xps iic 0 Gnd	I/O	[31:31]			



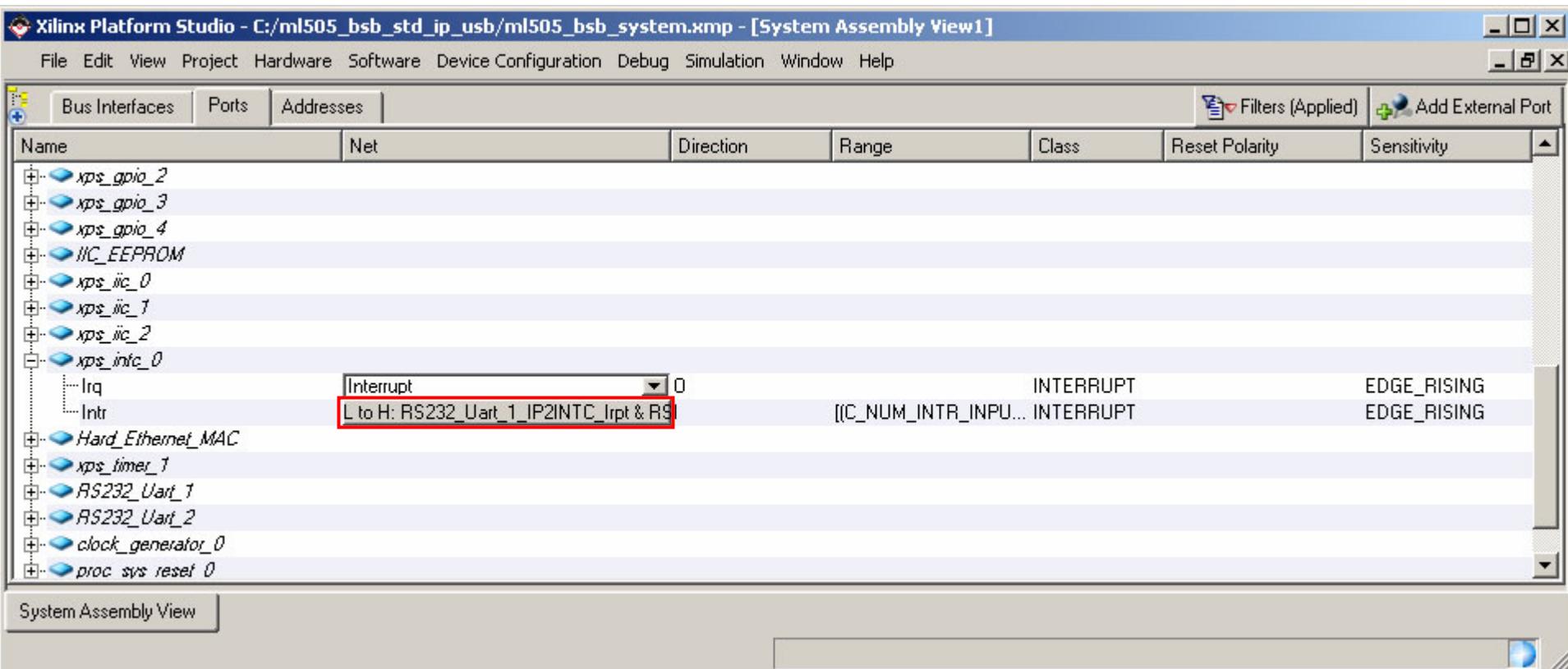
# Delete System ACE

- Delete SysACE\_CompactFlash, and its ports



# Setup Interrupts

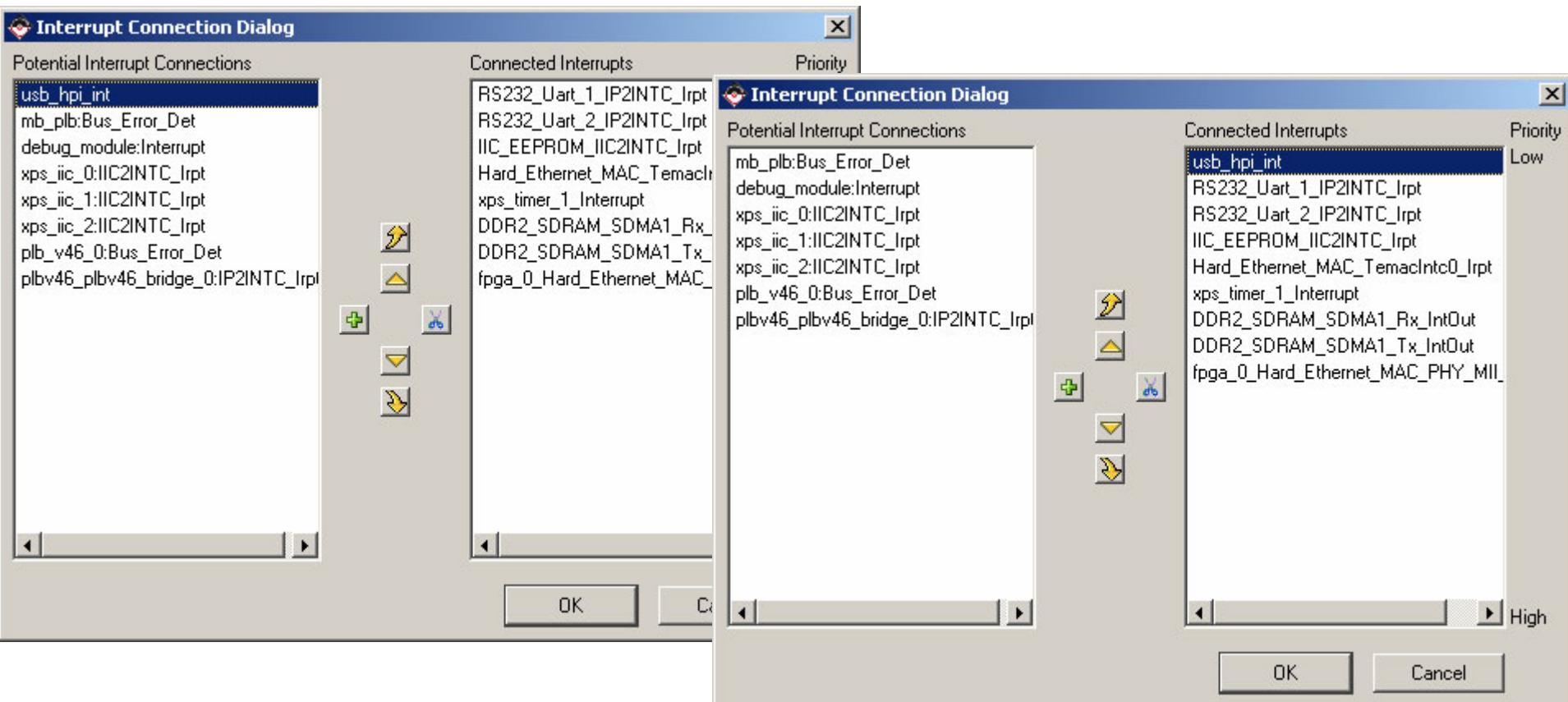
- Expand **xps\_intc\_0** and click on the gray Intr area to open the Interrupts dialog



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# Setup Interrupts

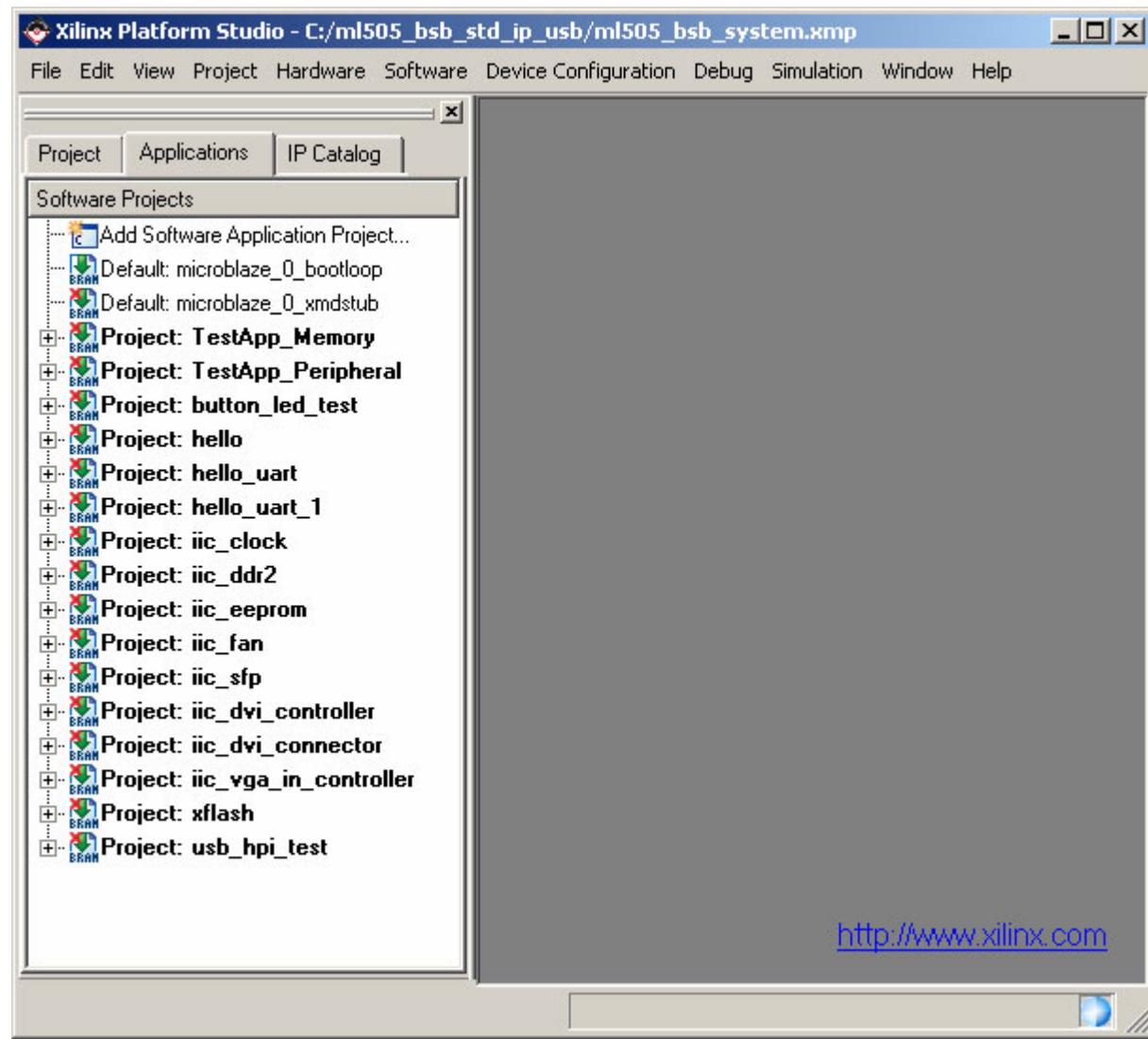
- Add **usb\_hpi\_int** to the Interrupts; move it to the top



# Adding Applications

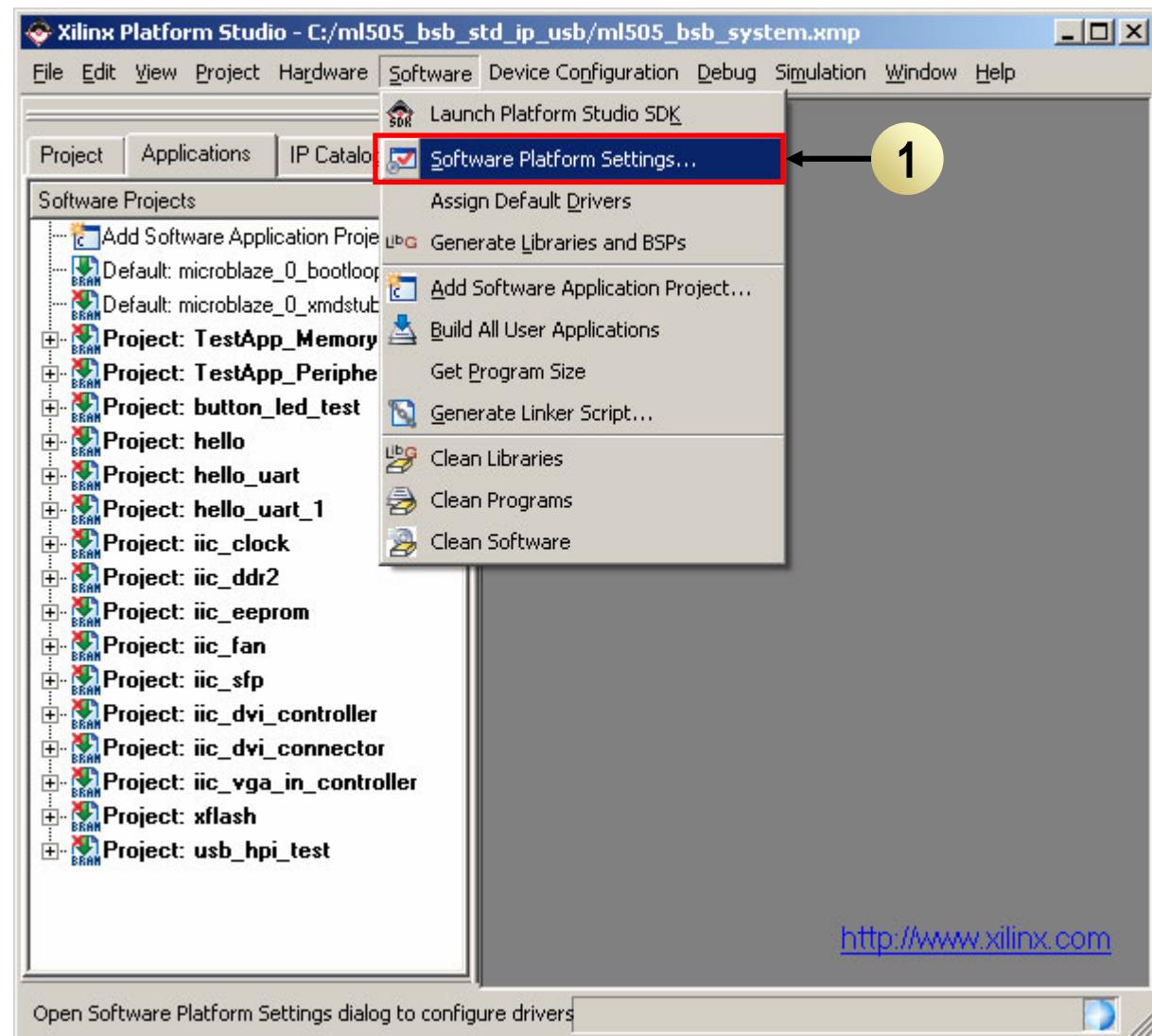
# Adding Applications

- A USB Test Project was added
  - **usb\_hpi\_test**
- The projects using System ACE were removed or modified
  - Modified:  
**TestApp\_Peripheral**
  - Removed:  
**bootload\_lcd**  
**piezo**  
**testfatfs**  
**sysace\_rebooter**



# Software Platform Settings

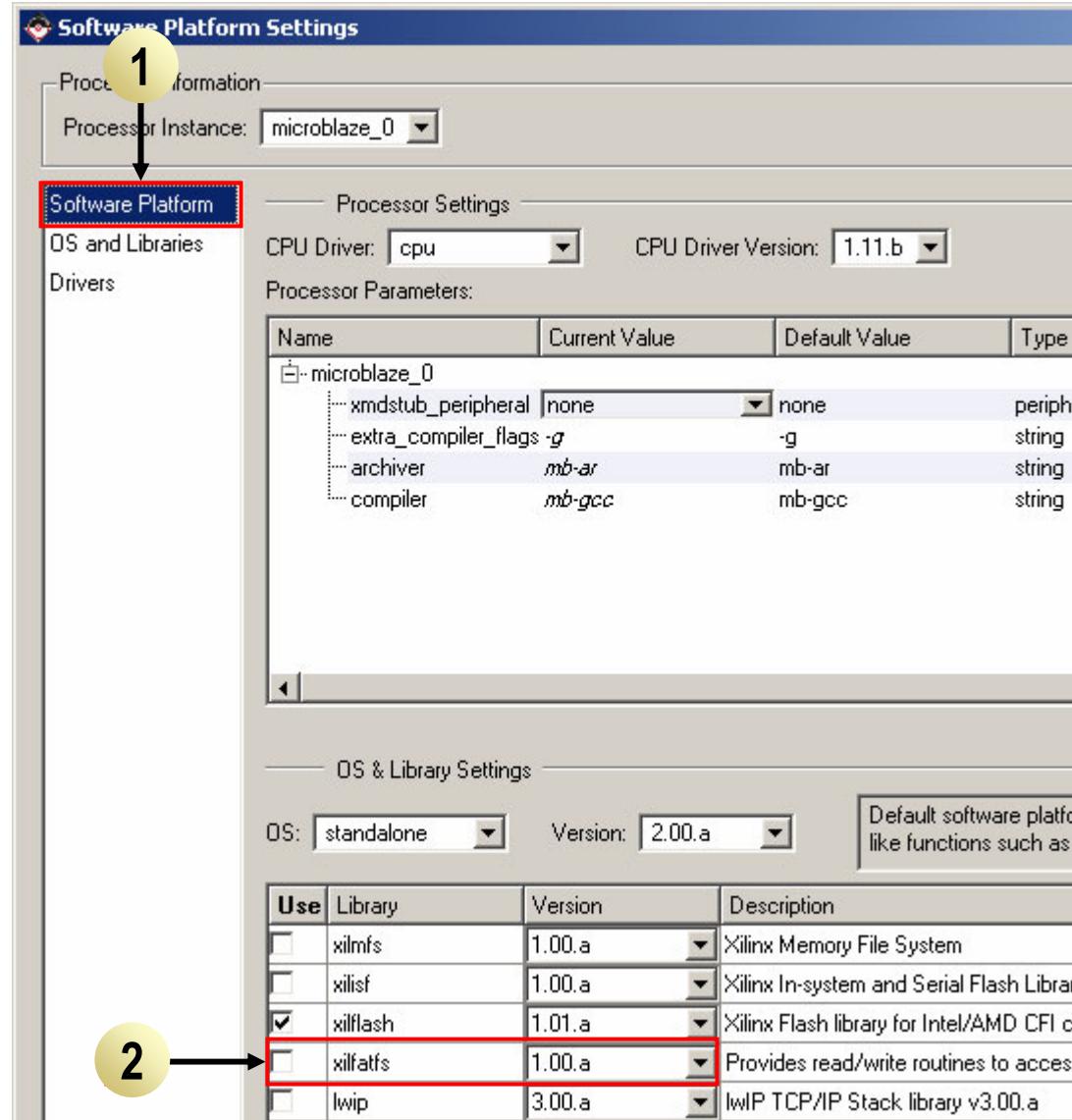
- Select Software → Software Platform Settings... (1)



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# Software Platform Settings

- Under Software Platform (1)
  - De-select **xilfatfs** (2)

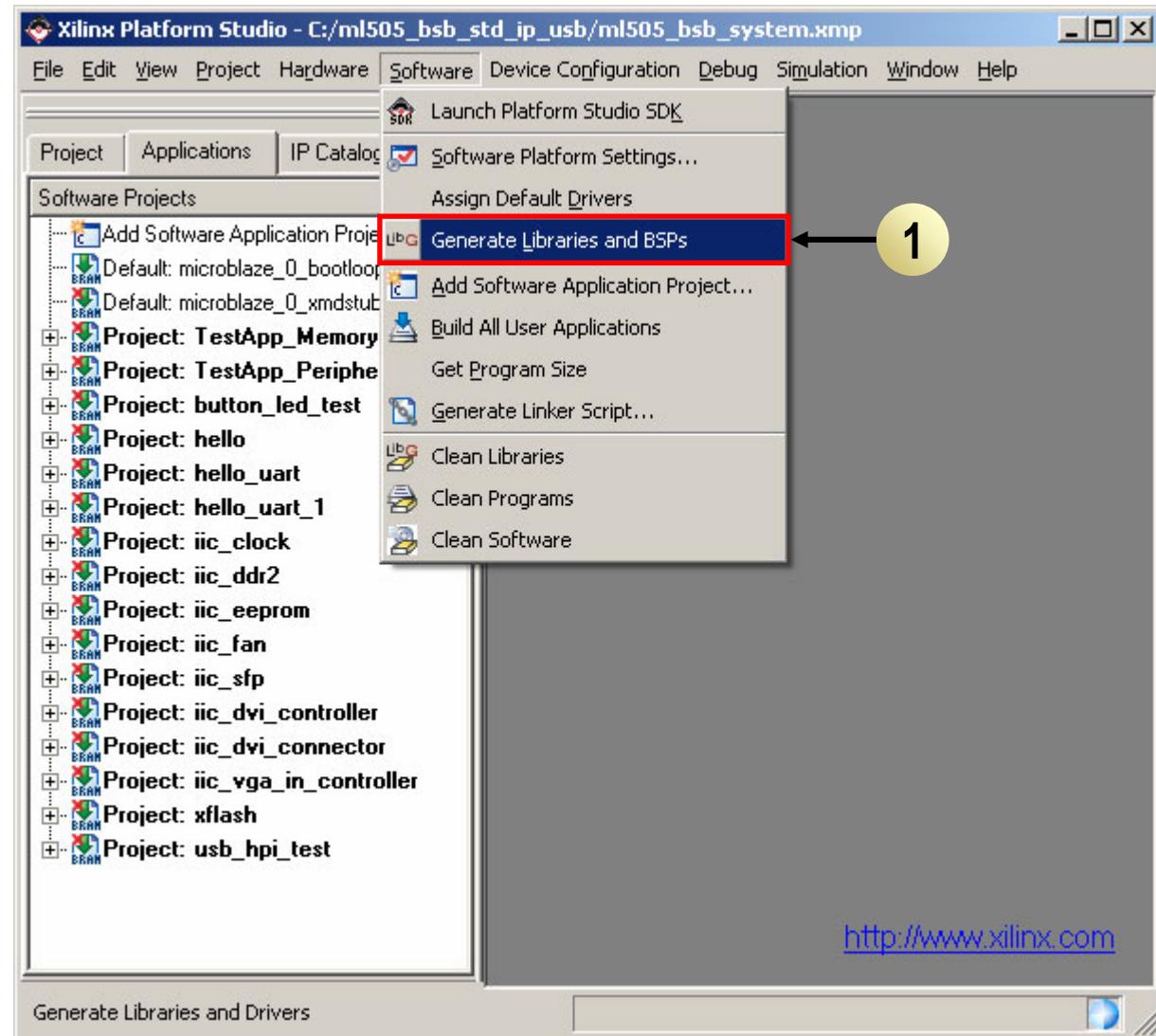


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# Compile Design

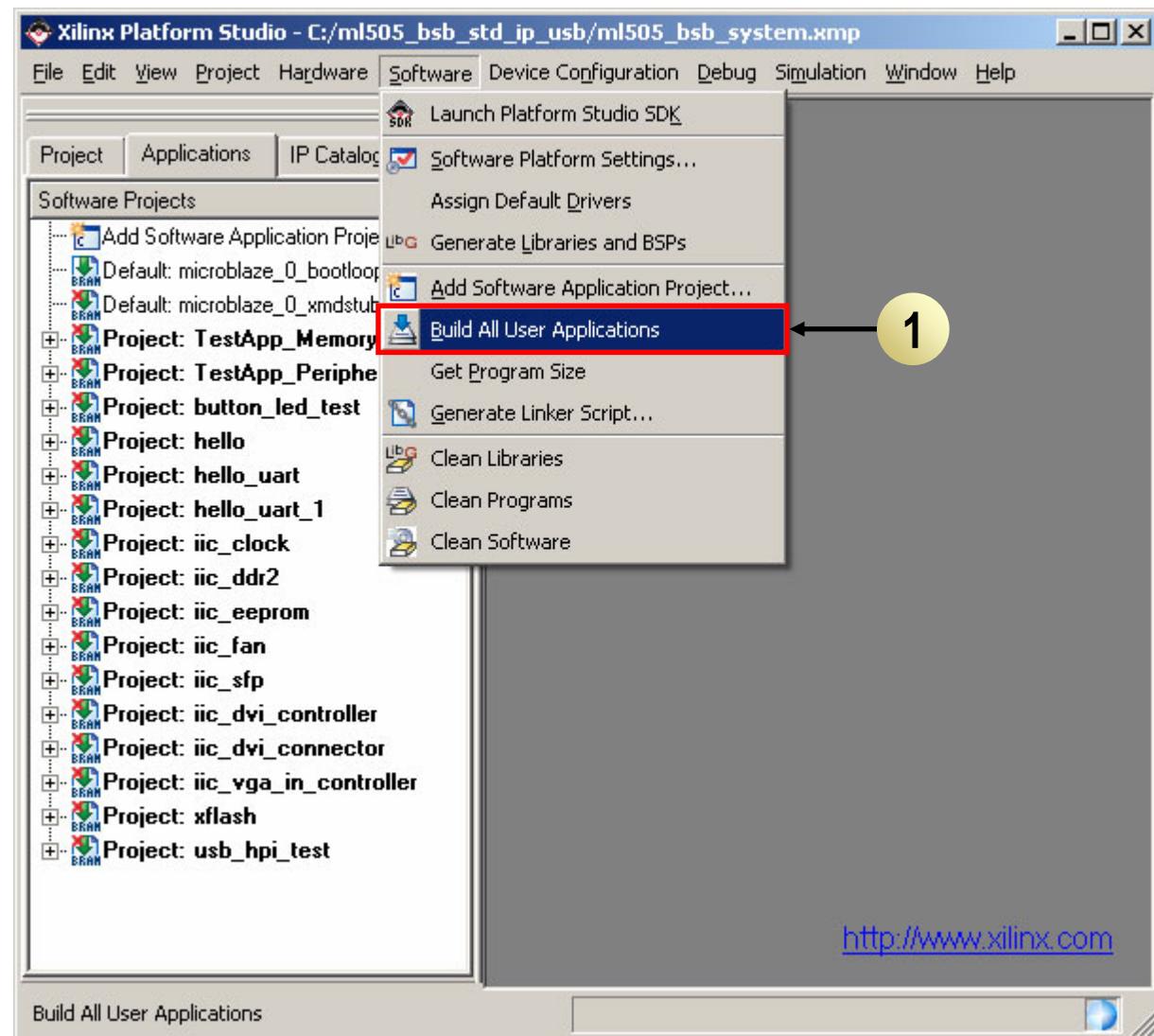
# Generate Bitstream

- Generate the libraries needed to create the bitstream
  - Select **Software** → **Generate Libraries and BSPs (1)**



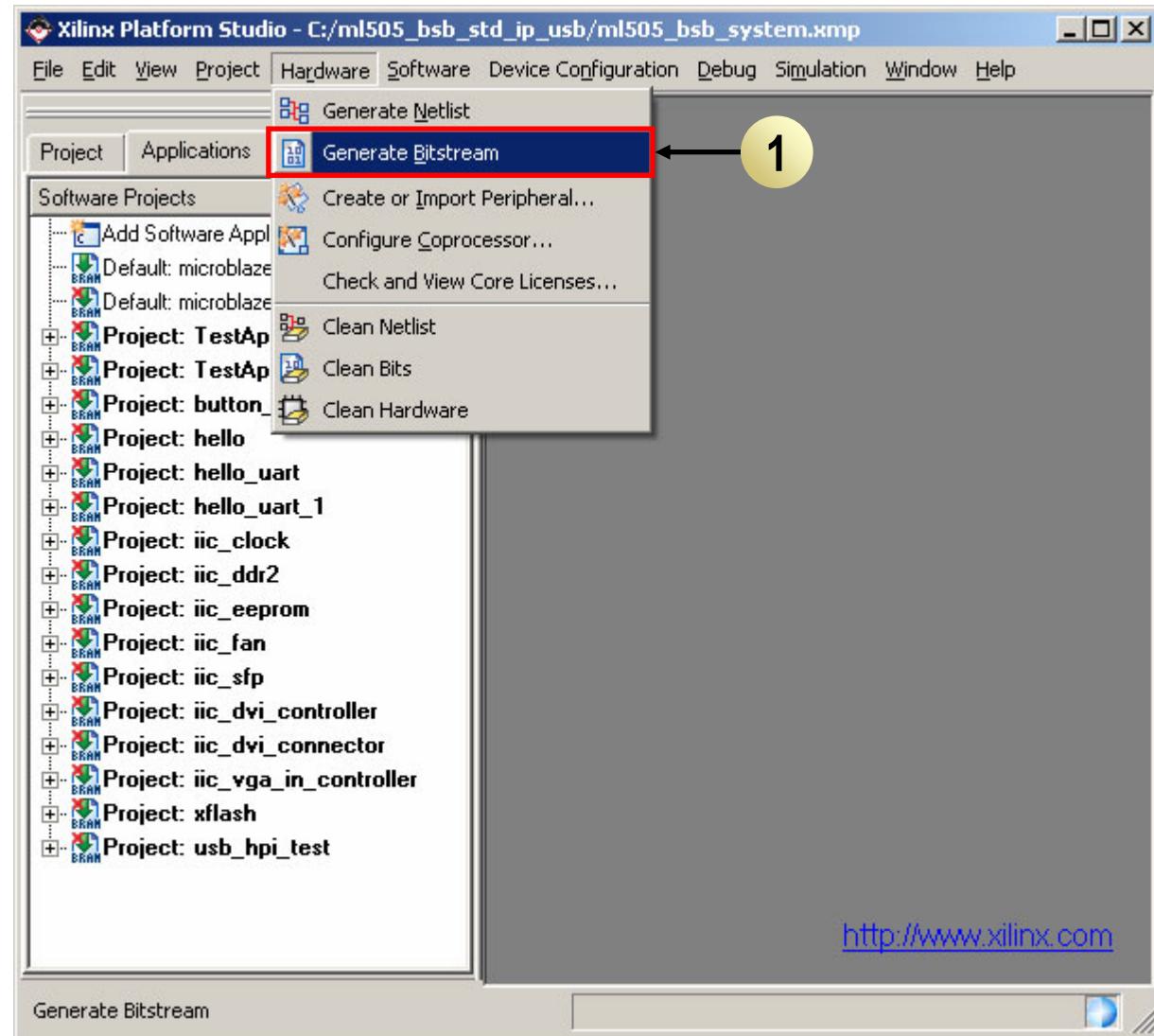
# Generate Bitstream

- Compile the applications and create an executable (executable.elf)
  - Select Software → Build All User Applications (1)



# Generate Bitstream

- Create the hardware design that is located in <project directory>/implementation
  - Select **Hardware** → **Generate Bitstream** (1)  
**(Takes roughly 60 minutes)**



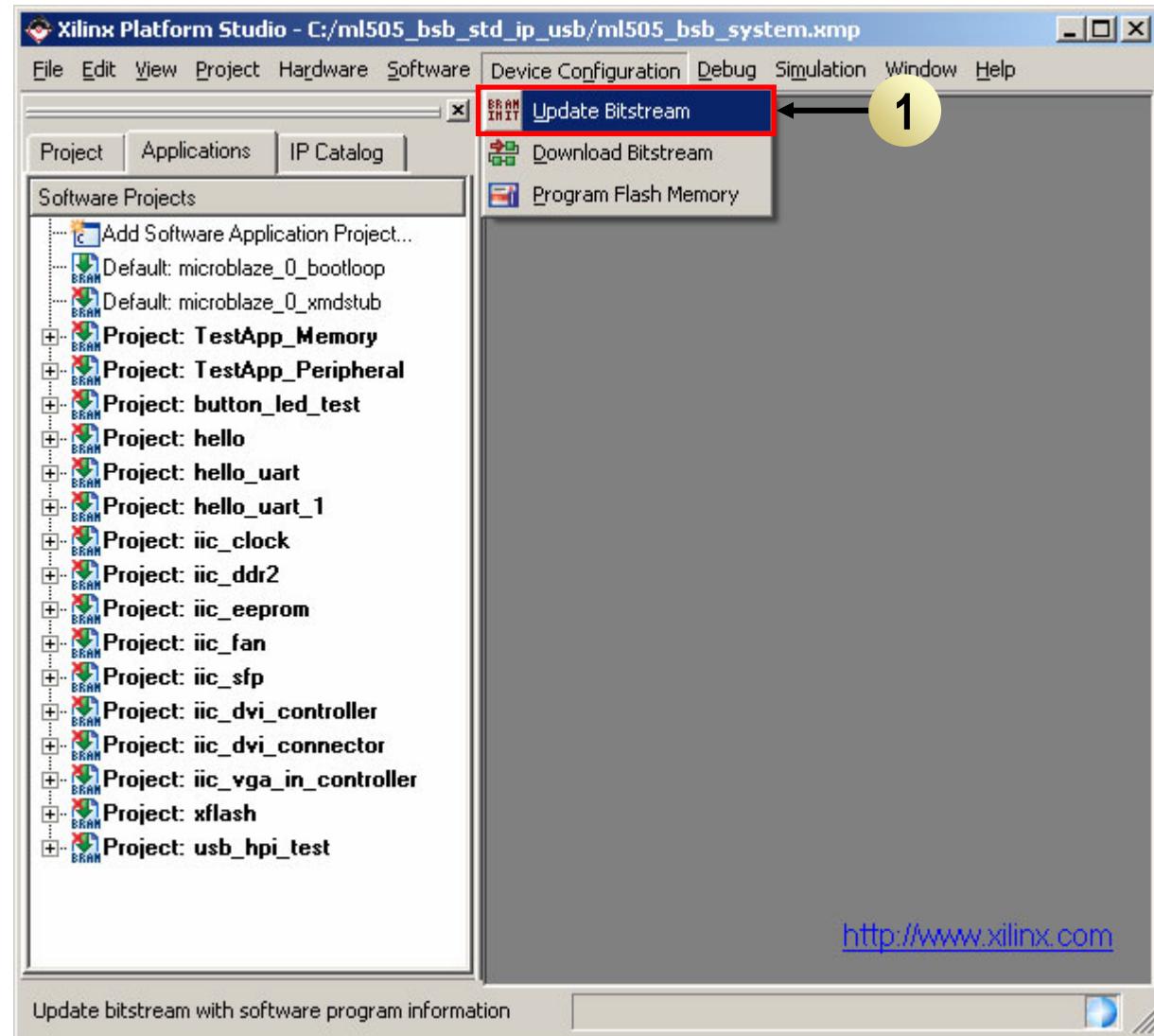
# Loading Bootloop into BRAM

- A concatenated software/hardware file, known as an ACE file, is useful for loading large programs, such as a VxWorks or Linux demo, into the external memory
- A bootloop program must be used to occupy the processor until the software is loaded into memory
- The following pages show how to initialize a bootloop program into block RAM and to test its existence



# Loading Bootloop into BRAM

- Update the bitstream (download.bit) with a bootloop ELF file (microblaze\_0.elf)
  - Select Device Configuration → Update Bitstream (1)

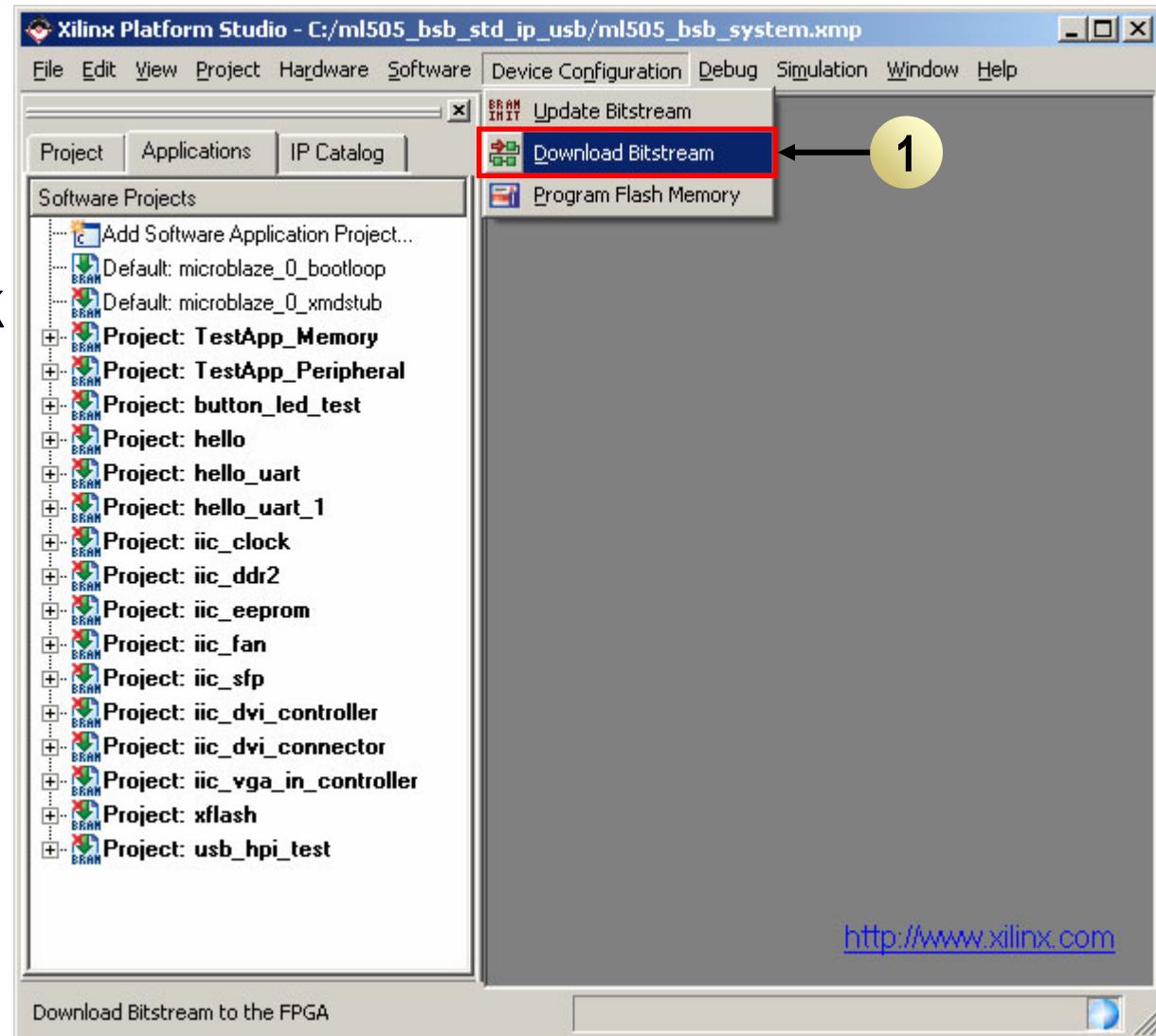


<http://www.xilinx.com>

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# Loading Bootloop into BRAM

- Load the new design onto the FPGA and load the bootloop program into the block RAM
  - Select Device Configuration → Download Bitstream (1)

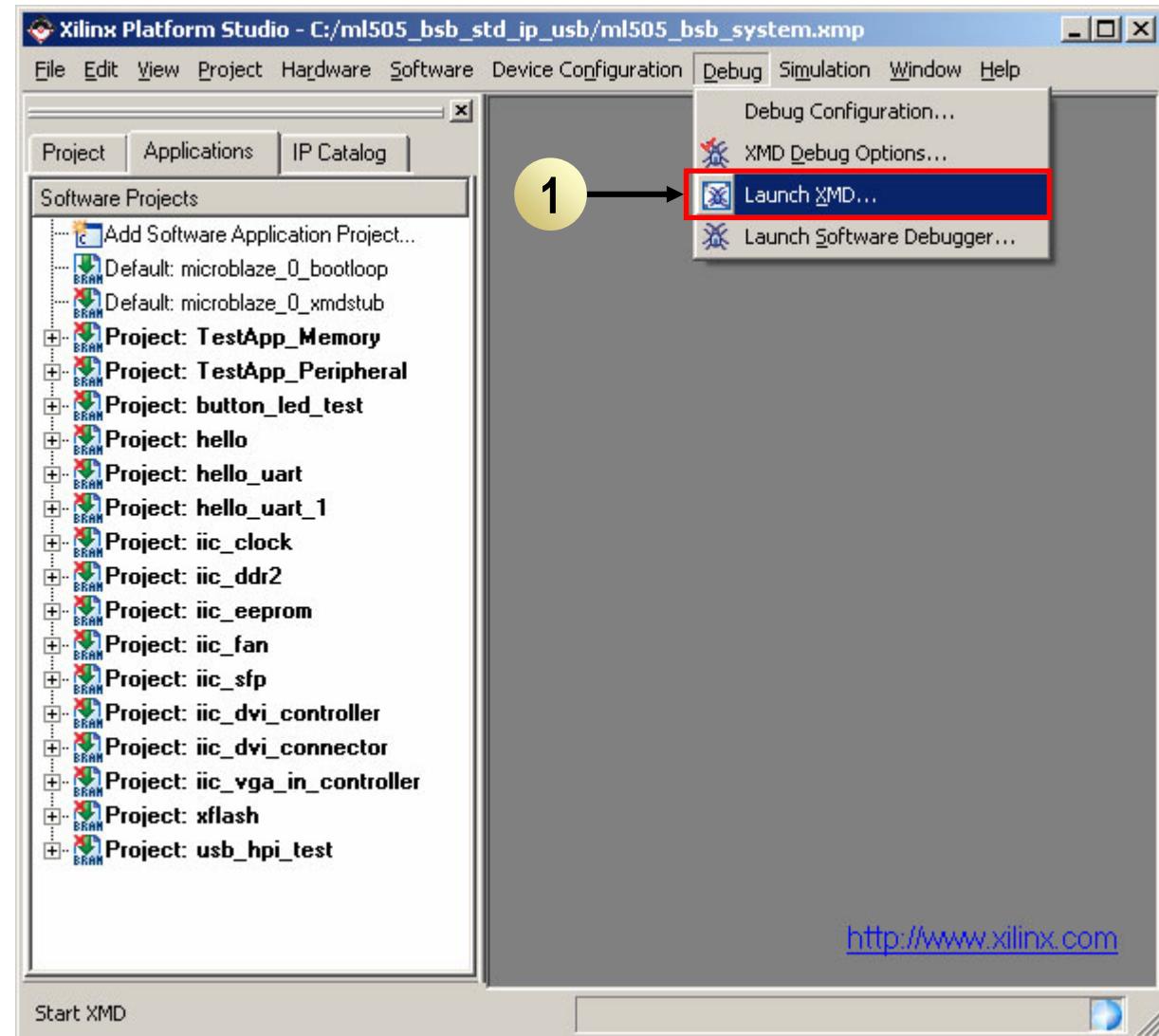


<http://www.xilinx.com>

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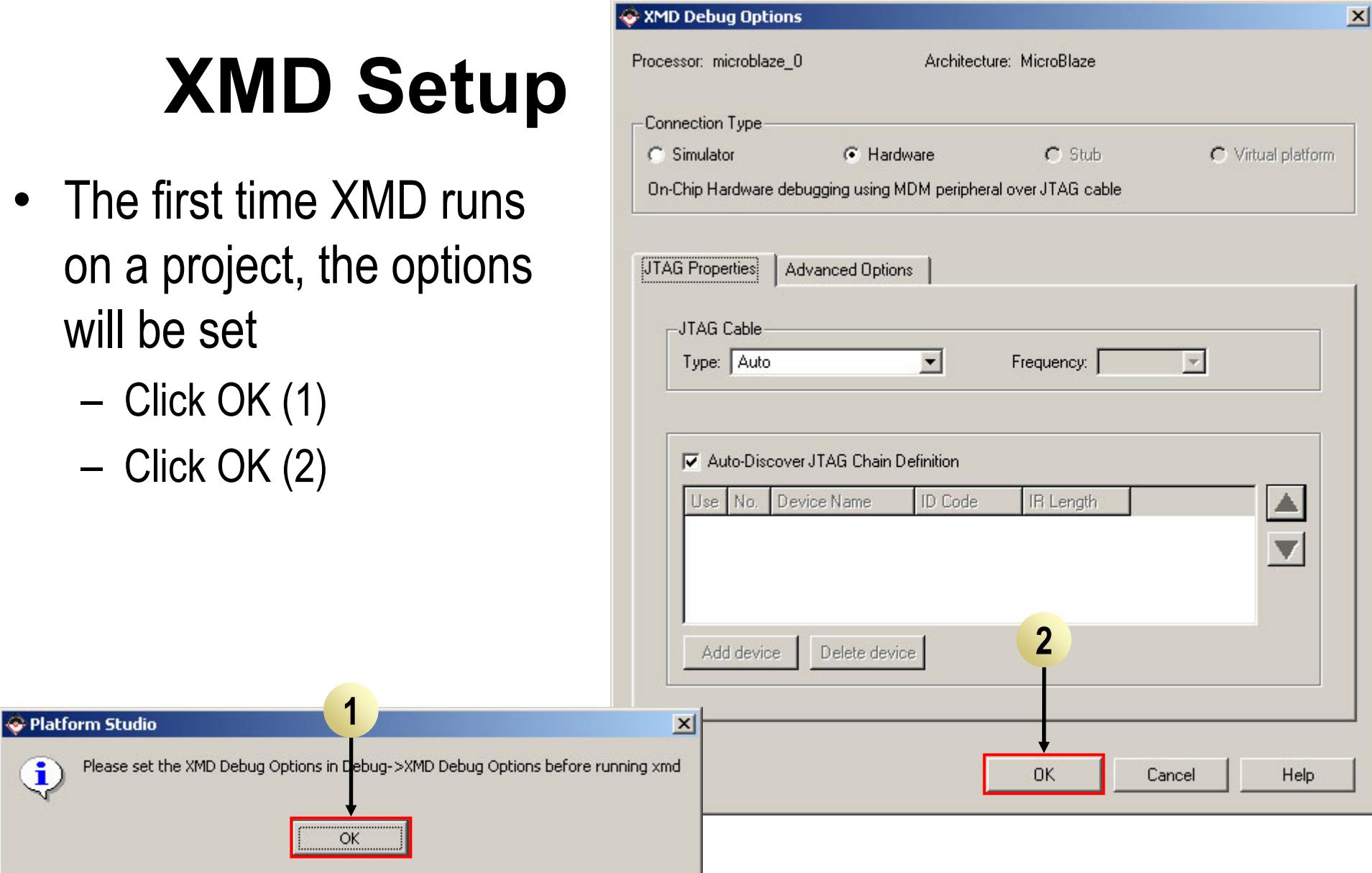
# Loading Bootloop into BRAM

- A memory read can be executed to test if the bootloop was successfully loaded
  - Select Debug → Launch XMD (1)



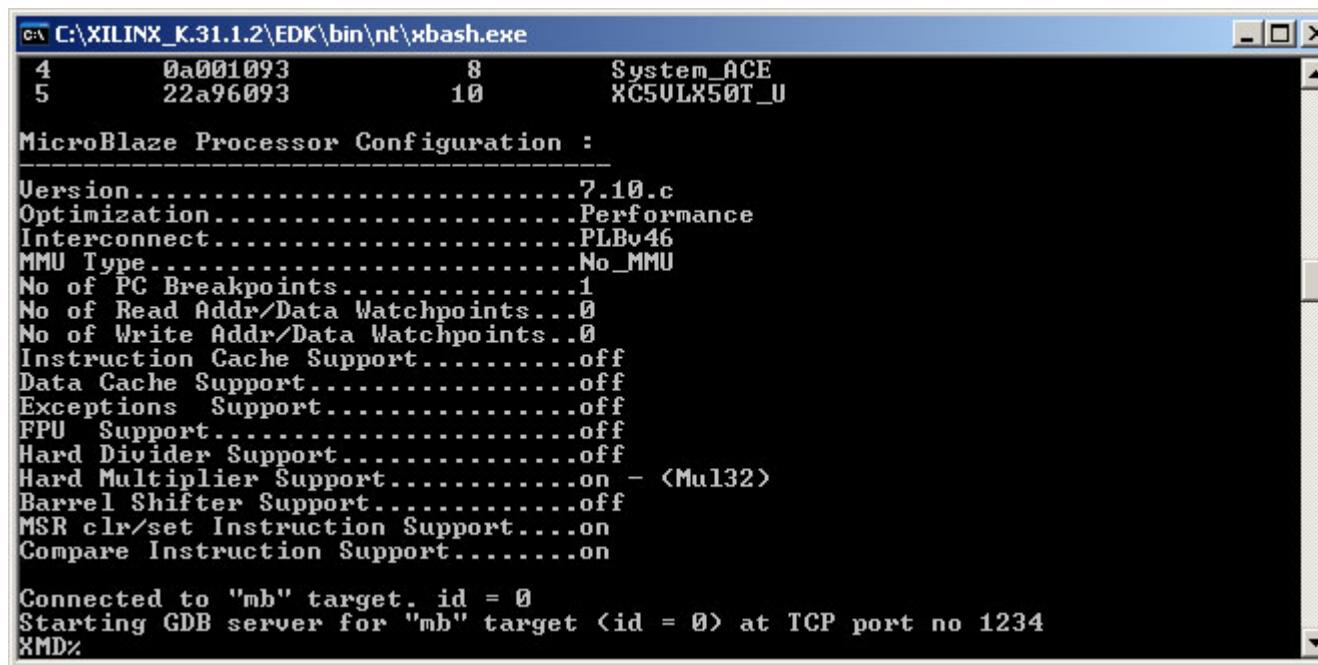
# XMD Setup

- The first time XMD runs on a project, the options will be set
  - Click OK (1)
  - Click OK (2)



# Loading Bootloop into BRAM

- XMD opens and connects to the processor, using the default options



```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
4      0a001093      8      System_ACE
5      22a96093      10     XC5ULX50T_U

MicroBlaze Processor Configuration :
-----
Version..... 7.10.c
Optimization..... Performance
Interconnect..... PLBu46
MMU Type..... No_MMU
No of PC Breakpoints..... 1
No of Read Addr/Data Watchpoints... 0
No of Write Addr/Data Watchpoints... 0
Instruction Cache Support..... off
Data Cache Support..... off
Exceptions Support..... off
FPU Support..... off
Hard Divider Support..... off
Hard Multiplier Support..... on - <Mul32>
Barrel Shifter Support..... off
MSR clr/set Instruction Support.... on
Compare Instruction Support..... on

Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD%
```



# Loading Bootloop into BRAM

- To execute a memory read, type **mrd 0x00000000**
- This will read the memory address at the reset vector; the value should be **0xB8000000** as shown below

```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
MicroBlaze Processor Configuration :
Version..... 7.10.c
Optimization..... Performance
Interconnect..... PLBv46
MMU Type..... No_MMU
No of PC Breakpoints..... 1
No of Read Addr/Data Watchpoints .. 0
No of Write Addr/Data Watchpoints.. 0
Instruction Cache Support..... off
Data Cache Support..... off
Exceptions Support..... off
FPU Support..... off
Hard Divider Support..... off
Hard Multiplier Support..... on - <Mul32>
Barrel Shifter Support..... off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on

Connected to "mb" target. id = 0
Starting GDB server for "mb" target <id = 0> at TCP port no 1234
XMD% mrd 0x00000000
0: B8000000

XMD%
```



# Download ELF File

- Download the usb\_hpi\_test ELF file from XMD  
dow microblaze\_0/code/usb\_hpi\_test.elf (1)  
con (2)

The screenshot shows a terminal window titled 'C:\XILINX\_K.31.1.2\EDK\bin\nt\xbash.exe'. The window contains the following text:

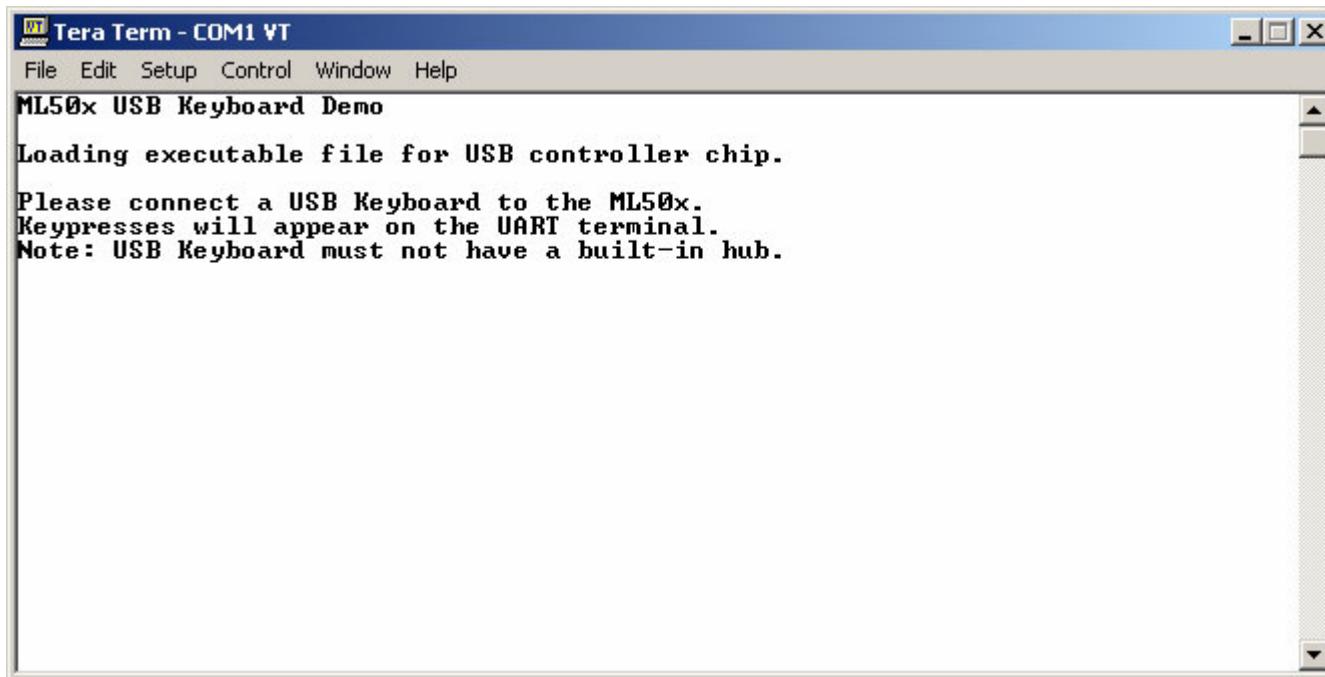
```
XMD% dow microblaze_0/code/usb_hpi_test.elf
System Reset .... DONE
Downloading Program -- microblaze_0/code/usb_hpi_test.elf
section, .vectors.reset: 0x00000000-0x00000007
section, .vectors.sw_exception: 0x00000008-0x0000000f
section, .vectors.interrupt: 0x00000010-0x00000017
section, .vectors.hw_exception: 0x00000020-0x00000027
section, .text: 0x90000000-0x9000138f
section, .init: 0x90001390-0x900013b3
section, .fini: 0x900013b4-0x900013cf
section, .ctors: 0x900013d0-0x900013d7
section, .dtors: 0x900013d8-0x900013df
section, .rodata: 0x900013e0-0x900018b9
section, .data: 0x900018c0-0x90004943
section, .eh_frame: 0x90004944-0x90004947
section, .jcr: 0x90004948-0x9000494b
section, .bss: 0x90004950-0x90004977
section, .heap: 0x90004978-0x90004d77
section, .stack: 0x90004d78-0x90005177
Setting PC with Program Start Address 0x00000000
RUNNING> XMD%
```

Two numbered callouts point to specific lines in the terminal output:

- 1 points to the command 'dow microblaze\_0/code/usb\_hpi\_test.elf'.
- 2 points to the command 'con'.

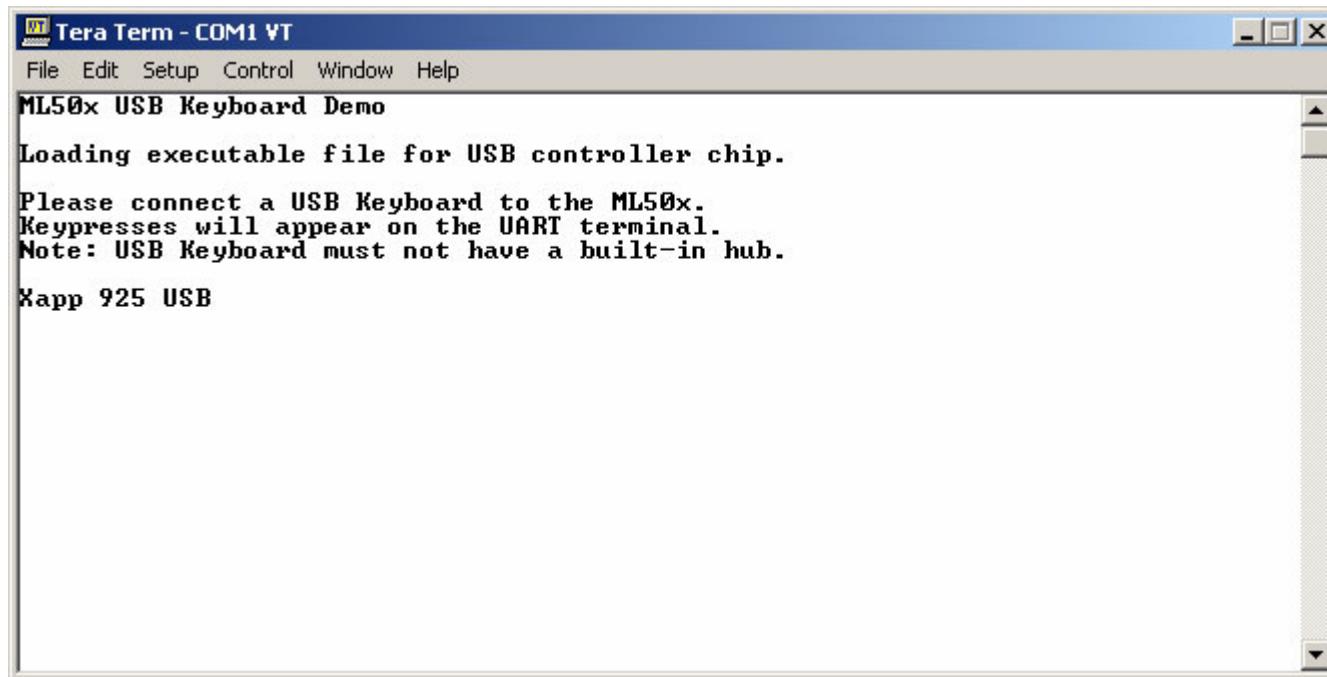
# Run usb\_hpi\_test

- View the output in the terminal program



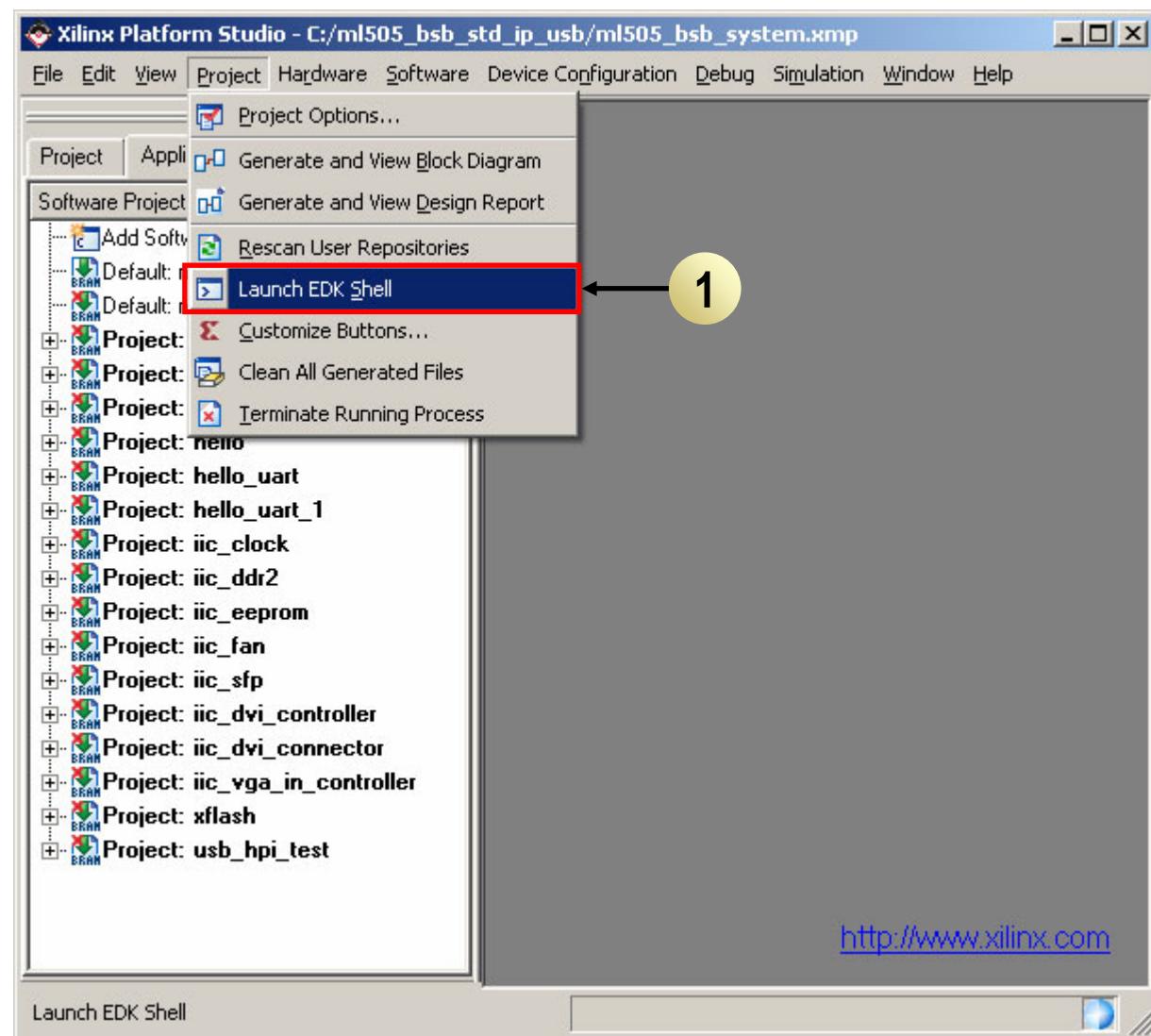
# Run usb\_hpi\_test

- Connect a USB keyboard (disconnect and reconnect if needed)
- Type “Xapp 925 USB”



# Create an ACE File

- Open an EDK shell
  - Select Project → Launch EDK Shell (1)
  - This shell is used for entering and executing the commands to create a concatenated (HW+SW ) ACE file



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# Create an ACE File

- At the bash prompt, type (1):

```
cd ace
```

```
./genace_usb_hpi_test.sh
```



A screenshot of a terminal window titled "bash-2.05\$". The window shows the command line "cd ace" followed by "bash-2.05\$ ./genace\_usb\_hpi\_test.sh". The last command is highlighted with a red rectangular box. A yellow circle containing the number "1" is positioned to the right of the highlighted command, with a thin black arrow pointing from the circle to the command itself.

# Create an ACE File

- This creates a concatenated (HW+SW) ACE file
  - Input: usb\_hpi\_test ELF file, download.bit
- The genace\_usb\_hpi\_test.sh script uses XMD and a genace.tcl script with ML505 appropriate options to generate an ACE file (1)

The screenshot shows a terminal window titled 'C:\XILINX\_K.31.1.2\EDK\bin\nt\xbash.exe'. The window displays the following command-line output:

```
c:\ C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
Device ID Code IR Length Part Name
1 02a96093 10 xc5vlx50t

Copying ../microblaze_0/code/usb_hpi_test.svf File to usb_hpi_test.svf File
#####
Writing Processor JTAG "continue" command to SVF file 'sw_suffix.svf'

JTAG chain configuration
Device ID Code IR Length Part Name
1 02a96093 10 xc5vlx50t

Info:Processor started. Type "stop" to stop processor
RUNNING>
#####
Converting SVF file 'usb_hpi_test.svf' to SystemACE file 'usb_hpi_test.ace'
Executing 'impact -batch svf2ace.scr'

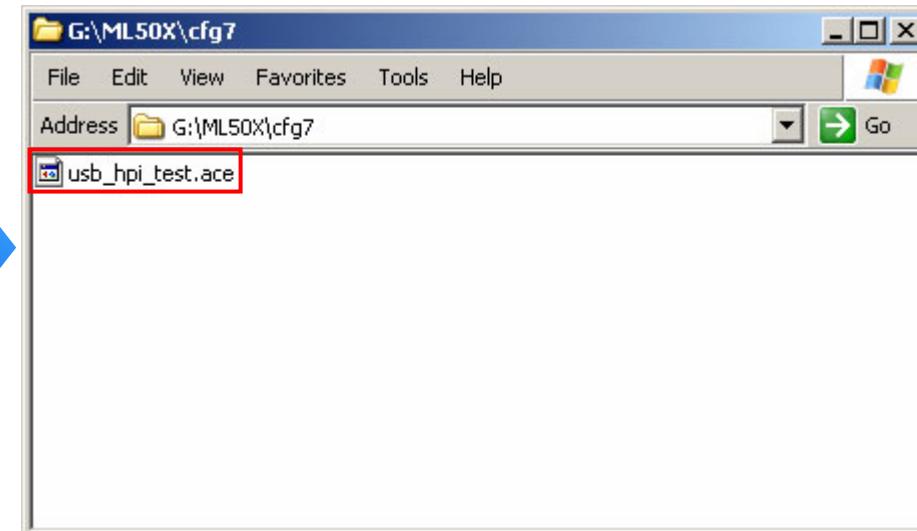
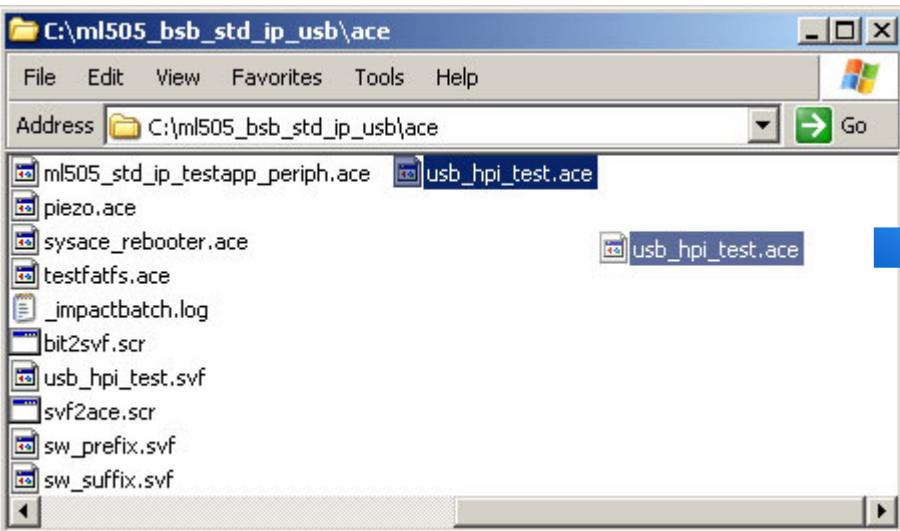
SystemACE file 'usb_hpi_test.ace' created successfully
```

A yellow circle with the number '1' is drawn around the line 'SystemACE file 'usb\_hpi\_test.ace' created successfully'.



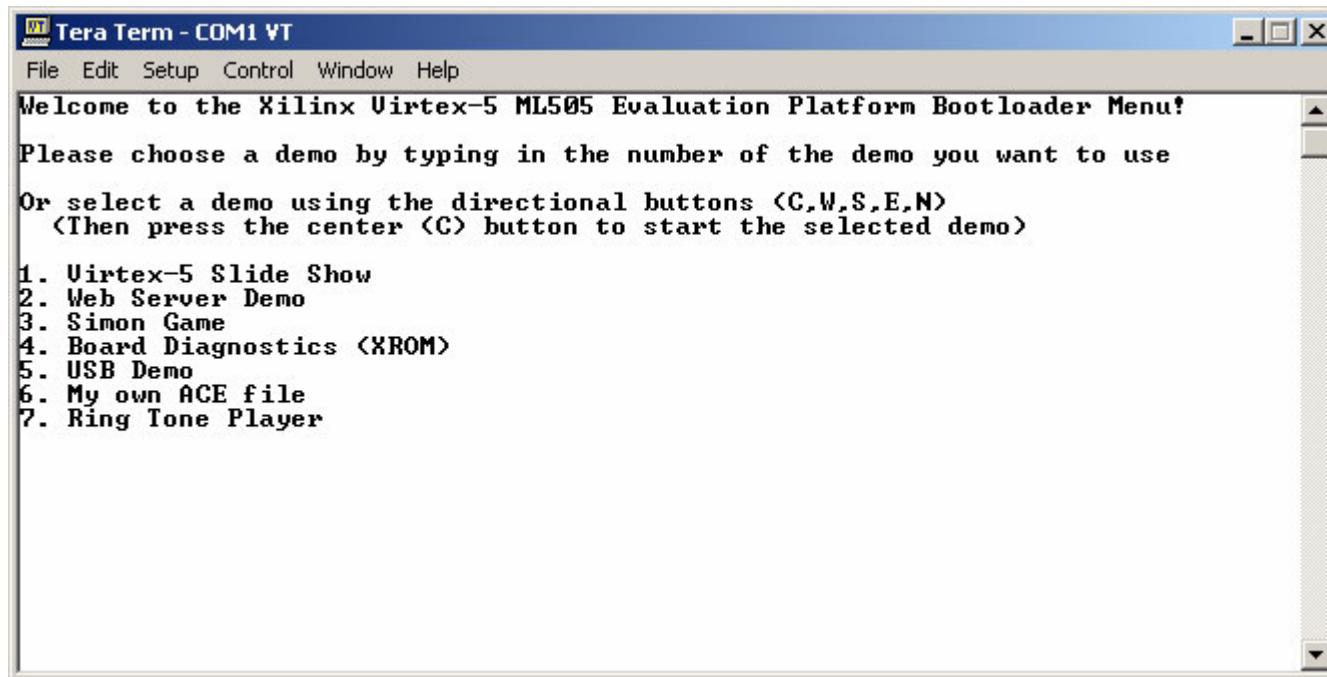
# Run ACE File

- Copy `usb_hpi_test.ace` to the `ML50X\cfg7` directory on your CompactFlash card
  - **Important:** Delete any existing ace files in this `cfg7` directory
  - **Note:** Use a CompactFlash reader to mount the CompactFlash as a disk drive



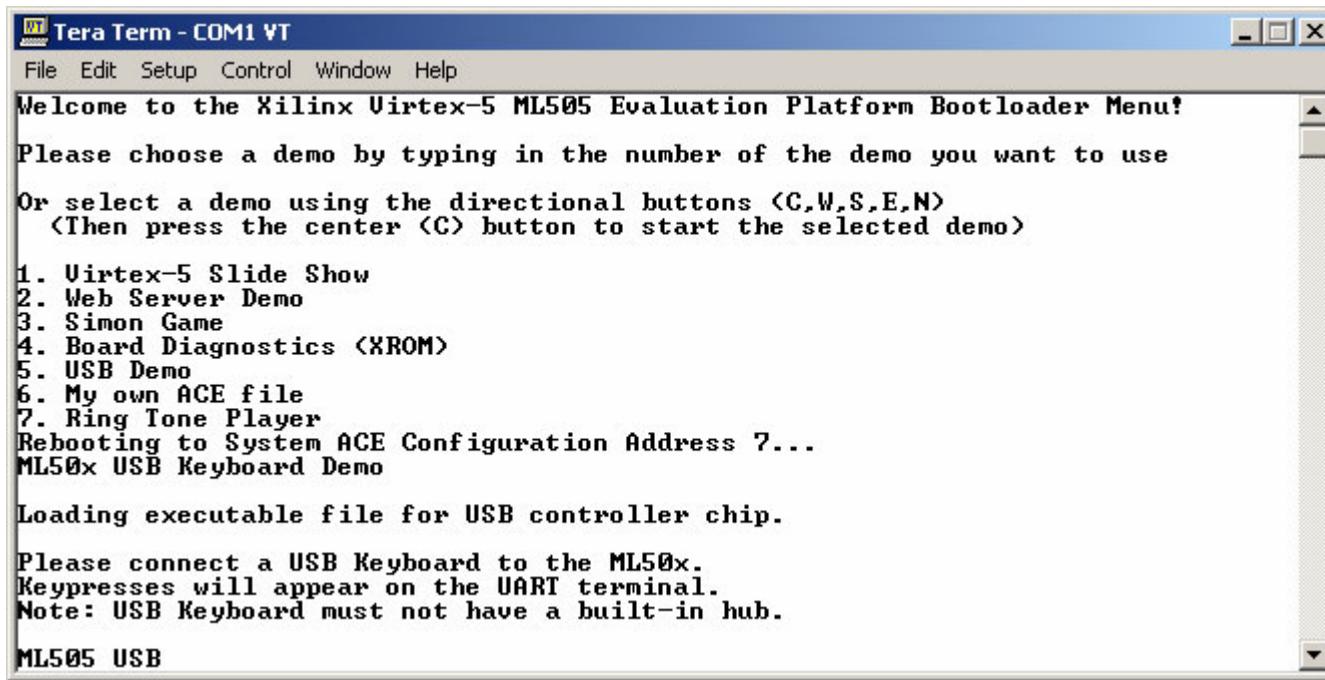
# Run ACE File

- Eject the CompactFlash from your PC and insert it back into the ML505
- Type 7 to run the newly created ACE file



# Using the ACE File

- The usb\_hpi\_test application output after booting ACE file
- Connect a keyboard and type “ML505 USB”



# Documentation

- Virtex-5
  - Silicon Devices  
[http://www.xilinx.com/products/silicon\\_solutions](http://www.xilinx.com/products/silicon_solutions)
  - Virtex-5 Multi-Platform FPGA  
[http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5)
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds100.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf)
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)

# Documentation

- Virtex-5
  - Virtex-5 FPGA User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug190.pdf](http://www.xilinx.com/support/documentation/user_guides/ug190.pdf)
  - Virtex-5 FPGA Configuration User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug191.pdf](http://www.xilinx.com/support/documentation/user_guides/ug191.pdf)
  - Virtex-5 System Monitor User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug192.pdf](http://www.xilinx.com/support/documentation/user_guides/ug192.pdf)
  - Virtex-5 Packaging and Pinout Specification  
[http://www.xilinx.com/support/documentation/user\\_guides/ug195.pdf](http://www.xilinx.com/support/documentation/user_guides/ug195.pdf)

# Documentation

- Virtex-5 RocketIO
  - RocketIO GTP Transceivers  
[http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5/capabilities/RocketIO\\_GTP.htm](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTP.htm)
  - RocketIO GTX Transceivers  
[http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5/capabilities/RocketIO\\_GTX.htm](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTX.htm)
  - RocketIO GTP Transceiver User Guide – UG196  
[http://www.xilinx.com/support/documentation/user\\_guides/ug196.pdf](http://www.xilinx.com/support/documentation/user_guides/ug196.pdf)
  - RocketIO GTX Transceiver User Guide – UG198  
[http://www.xilinx.com/support/documentation/user\\_guides/ug198.pdf](http://www.xilinx.com/support/documentation/user_guides/ug198.pdf)

# Documentation

- Design Resources
  - ISE Development Tools and IP  
<http://www.xilinx.com/ise>
  - Integrated Software Environment (ISE) Foundation Resources  
[http://www.xilinx.com/ise/logic\\_design\\_prod/foundation.htm](http://www.xilinx.com/ise/logic_design_prod/foundation.htm)
  - ISE Manuals  
[http://www.xilinx.com/support/software\\_manuals.htm](http://www.xilinx.com/support/software_manuals.htm)
  - ISE Development System Reference Guide  
<http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf>
  - ISE Development System Libraries Guide  
[http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5\\_hdl/virtex5\\_hdl.pdf](http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf)

# Documentation

- Additional Design Resources
  - Customer Support  
<http://www.xilinx.com/support>
  - Xilinx Design Services:  
<http://www.xilinx.com/xds>
  - Titanium Dedicated Engineering:  
<http://www.xilinx.com/titanium>
  - Education Services:  
<http://www.xilinx.com/education>
  - Xilinx On Board (Board and kit locator):  
<http://www.xilinx.com/xob>

# Documentation

- Platform Studio
  - Embedded Development Kit (EDK) Resources  
<http://www.xilinx.com/edk>
  - Embedded System Tools Reference Manual  
[http://www.xilinx.com/support/documentation/sw\\_manuals/edk10\\_est\\_rm.pdf](http://www.xilinx.com/support/documentation/sw_manuals/edk10_est_rm.pdf)
  - EDK Concepts, Tools, and Techniques  
[http://www.xilinx.com/ise/embedded/edk92i\\_docs/edk\\_ctt.pdf](http://www.xilinx.com/ise/embedded/edk92i_docs/edk_ctt.pdf)

# Documentation

- MicroBlaze
  - MicroBlaze Processor  
<http://www.xilinx.com/microblaze>
  - MicroBlaze Processor Reference Guide – UG081  
[http://www.xilinx.com/support/documentation/sw\\_manuals\(mb\\_ref\\_guide.pdf](http://www.xilinx.com/support/documentation/sw_manuals(mb_ref_guide.pdf)

# Documentation

- PLB v4.6 IP
  - Processor Local Bus (PLB) v4.6 Data Sheet – DS531  
[http://www.xilinx.com/support/documentation/ip\\_documentation/plb\\_v46.pdf](http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf)
  - Multi-Port Memory Controller (MPMC) – DS643  
[http://www.xilinx.com/support/documentation/ip\\_documentation/mpmc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf)
  - XPS Multi-CHannel External Memory Controller (XPS MCH EMC) – DS575  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_mch\\_emc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf)
  - XPS LocalLink TEMAC – DS537  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ll\\_temac.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf)
  - XPS LocalLink FIFO – DS568  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ll\\_fifo.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf)

# Documentation

- PLB v4.6 IP
  - XPS IIC Bus Interface – DS606  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_iic.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf)
  - XPS SYSACE (System ACE) Interface Controller – DS583  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_sysace.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf)
  - XPS Timer/Counter – DS573  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_timer.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf)
  - XPS Interrupt Controller – DS572  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_intc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf)
  - Using and Creating Interrupt-Based Systems Application Note  
[http://www.xilinx.com/support/documentation/application\\_notes/xapp778.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp778.pdf)

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- PLB v4.6 IP
  - XPS General Purpose Input/Output (GPIO) – DS569  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_gpio.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf)
  - XPS External Peripheral Controller (EPC) – DS581  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_epc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_epc.pdf)
  - XPS 16550 UART – DS577  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_uart16550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_uart16550.pdf)
  - PLBV46 to DCR Bridge Data Sheet – DS578  
[http://www.xilinx.com/support/documentation/ip\\_documentation/plbv46\\_dcr\\_bridge.pdf](http://www.xilinx.com/support/documentation/ip_documentation/plbv46_dcr_bridge.pdf)

# Documentation

- IP
  - Local Memory Bus Data Sheet – DS445  
[http://www.xilinx.com/support/documentation/ip\\_documentation/lmb\\_v10.pdf](http://www.xilinx.com/support/documentation/ip_documentation/lmb_v10.pdf)
  - Block RAM Block Data Sheet – DS444  
[http://www.xilinx.com/support/documentation/ip\\_documentation/bram\\_block.pdf](http://www.xilinx.com/support/documentation/ip_documentation/bram_block.pdf)
  - Microprocessor Debug Module Data Sheet – DS641  
[http://www.xilinx.com/support/documentation/ip\\_documentation/mdm.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mdm.pdf)
  - LMB Block RAM Interface Controller Data Sheet – DS452  
[http://www.xilinx.com/support/documentation/ip\\_documentation/lmb\\_bram\\_if\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/lmb_bram_if_cntlr.pdf)
  - Device Control Register Bus (DCR) v2.9 Data Sheet – DS406  
[http://www.xilinx.com/support/documentation/ip\\_documentation/dcr\\_v29.pdf](http://www.xilinx.com/support/documentation/ip_documentation/dcr_v29.pdf)

# Documentation

- IP
  - JTAGPPC Controller Data Sheet – DS298  
[http://www.xilinx.com/support/documentation/ip\\_documentation/jtagppc\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/jtagppc_cntlr.pdf)
  - Processor System Reset Module Data Sheet – DS402  
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