AR# 24935

MIG v2.0 - Spartan-3/-3E/-3A memory implementation guidelines for DDR/DDR2 SDRAM interfaces

Description

The *Xilinx Memory Interface Generator (MIG) 2.0 User Guide* includes Memory Implementation Guidelines in *Section V: Appendices*.

This section outlines general pin assignment guidelines for DDR/DDR2 SDRAM implementation.

However, additional guidelines should be followed when targeting Spartan-3/-3E/-3A/-3A DSP devices.

Solution

Starting with the MIG 2.1 release, this information is available in the MIG User Guide.

Please see the MIG User Guide for further information.

MIG generates a UCF file that follows the guidelines listed below.

Xilinx recommends using the pin-out created by MIG.

Follow the guidelines below if the MIG pin-out is modified.

The IOBs for DQ bits must be placed five tiles above or six tiles below the IOB tile for the associated DQS bit.

This is necessary because the MIG design uses low-skew routing resources to route DQS to the data capture FIFOs corresponding to that DQS.

For Example

If DQS is placed in either W3 or W4 (these two IOBs share a tile) in an XC3S1500-FG676, the following +5 tiles can be used for DQ placement:

- W1/W2
- U7/V7
- Virtex-4/V5
- Virtex-II/V3
- U5/U6

The following -6 tiles can be for DQ placement:

- W5/V6
- W6/W7
- Y1/Y2
- AA1/AA2
- Y4/Y5
- AA3/AA4

WARNING: Unbonded tiles (even though they cannot be used) count toward this +5/-6 guideline.

Consequently, it is possible that a pin-out that meets the above requirements for a specific bus width cannot be supported on a larger device in the same package (even though the package is "pin-out compatible").

MIG can be used to generate a pin-out compatible with multiple devices in the same package.

To verify the pin placement of the DQ and DQS bits, you can check the net skew and delay values in the FPGA Editor and the "Clock Report" section of the design's PAR report (.par file).

See (Xilinx Answer 25245) for steps to verify the DQ and DQS skew and delay values.

- The "rst_dqs_div_in" and "rst_dqs_div_out" IOBs must be placed in the center of the DQ bits.

As an example, if the data bus is 64 bits, "rst_dqs_div_in" and "rst_dqs_div_out" should be placed between DQ[31] and DQ[32].

If this is not followed, the data capture might not be reliable.

This is necessary because the MIG design uses the RST_DQS_DIV feedback loop to generate a Write Enable to all the data capture FIFOs.

See XAPP768c for further information on the Spartan-3 design.

- Spartan-3 architectures only have two FIFOs per CLB.

Because each bit of data requires two FIFOs (one for rising edge data and one for falling edge data), the MIG designs use two columns of CLBs.

One CLB column is dedicated for the odd numbered bits and one is dedicated for the even numbered bits.

Because of Spartan-3 routing restrictions, pad0 (top) must be assigned to the first column CLBs and pad 1 (bottom) assigned to second column of CLBs.

With this routing implementation, the DQ lines from both pads will have the same route delay.

- The CK/CK_N, address, RAS_N, CAS_N, WE_N, CS_N, and ODT must be placed together in banks that are on the same side of the device.

This helps to avoid clock skew on these signals that are registered on the rising edge of CK.

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