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NOTE: PLEASE REVIEW THE ML310 BOM FOR ITEMS DESIGNATED AS "NOSTUFF".

NOSTUFF ITEMS ARE NOT POPULATED ON THE PCB.

THE ML310 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT
NOSTUFF DISCRETES AND COMPONENTS.

XILINX PART NUMBERS

SCHEMATICS	0381171-02
PCB ARTWORK	0531311-02
PCB FABRICATION	1280333-02

 XILINX
 SCH P/N 0381171-02
 ART P/N 0531311-02
 FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFROM

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Date: 6-4-2004_12:54 Ver: x.x

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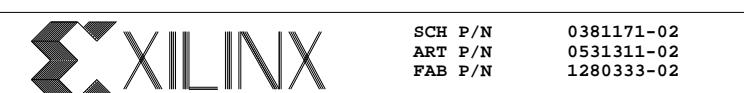
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SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFROM

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Date: 10-6-2003_14:59 Ver: x.x

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SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFROM

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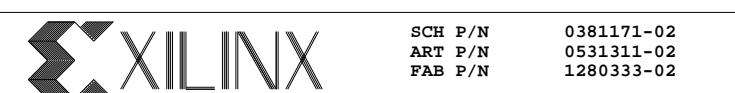
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SCH P/N 0381171-02
ART P/N 0531311-02
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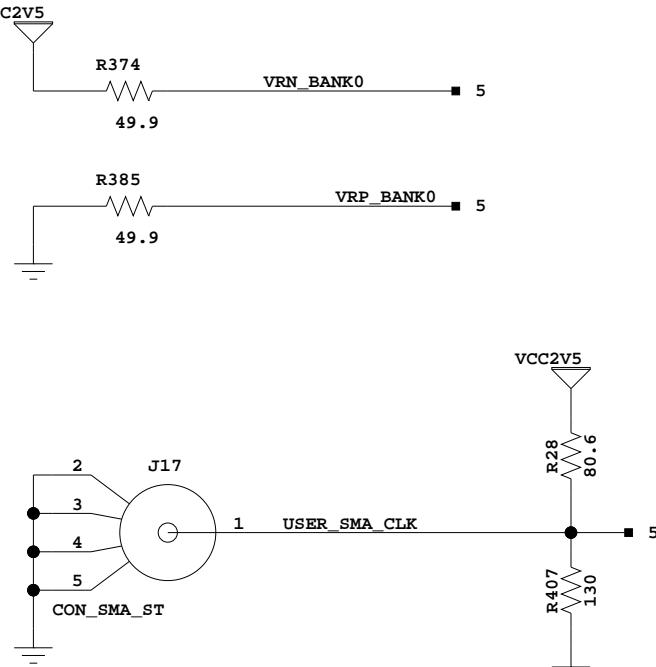
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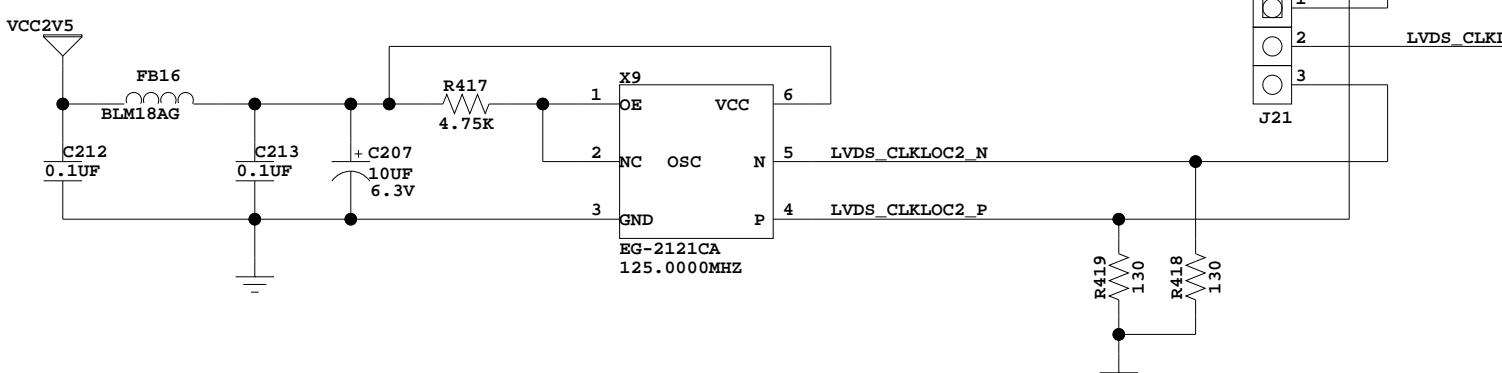
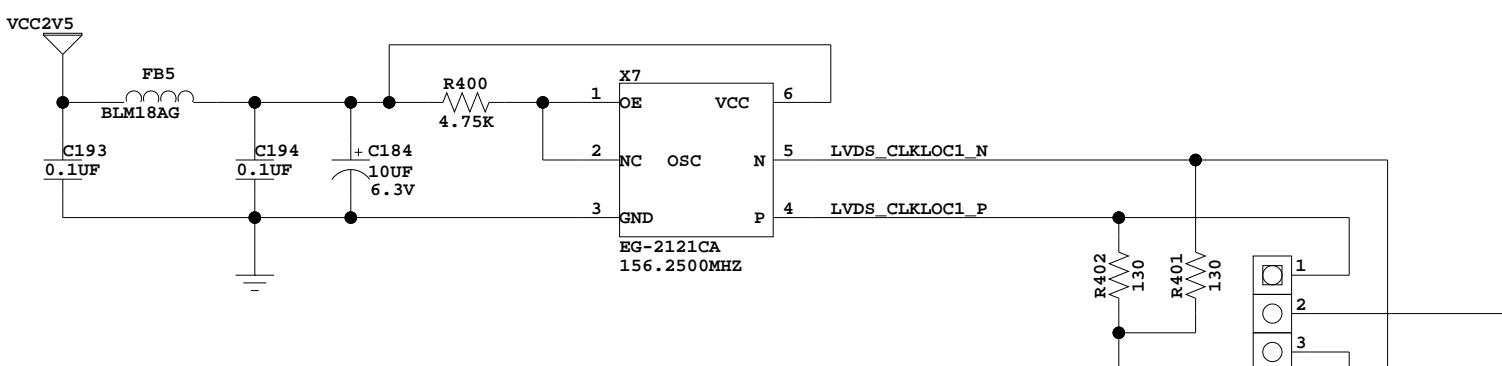
XC2VP20-BANK0

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(DIE DOWN)



NOTE: 130 OHM RESISTORS ON EG-2121 OUTPUTS ARE
INTENDED TO PROVIDE A LOAD FOR THE PECL
DRIVERS AND SHOULD BE PLACED NEAR THE OSC.



5 ■ VRN_BANK0	E24	IO_L01P_0/VRN_0_E24
5 ■ VRP_BANK0	E25	IO_L01N_0/VRP_0_E25
20 ■ SYSACE_MPIRQ	F23	IO_L02P_0_F23
20 ■ SYSACE_MPBRDY	F24	IO_L02N_0_F24
20 ■ SYSACE_MPCE	E22	IO_L03P_0/VREF_0_E22
20 ■ SYSACE_MPDE	E23	IO_L03N_0_E23
20 ■ SYSACE_MPWE	G23	IO_L05_0/No_Pair_G23
20 ■ SYSACE_MPDI5	G22	IO_L06P_0_H22
20 ■ SYSACE_MPDI4	H22	IO_L06N_0_K17
20 ■ SYSACE_MPDI3	F21	IO_L07P_0_F21
20 ■ SYSACE_MPDI2	F22	IO_L07N_0_F22
20 ■ SYSACE_MPDI1	C24	IO_L08P_0_C24
20 ■ SYSACE_MPDI0	D24	IO_L08N_0_D24
20 ■ SYSACE_MPDO9	G21	IO_L09P_0/VREF_0_G21
20 ■ SYSACE_MPDO8	H21	IO_L09N_0_H21
20 ■ SYSACE_MPDO7	D21	IO_L37P_0_D21
20 ■ SYSACE_MPDO6	E21	IO_L37N_0_E21
20 ■ SYSACE_MPDO5	C23	IO_L38P_0_C23
20 ■ SYSACE_MPDO4	D23	IO_L38N_0_D23
20 ■ SYSACE_MPDO3	G20	IO_L39P_0_G20
20 ■ SYSACE_MPDO2	H20	IO_L39N_0_H20
20 ■ SYSACE_MPDO1	D20	IO_L43P_0_D20
20 ■ SYSACE_MPDO0	E20	IO_L43N_0_E20
20 ■ SYSACE_MPAP6	A23	IO_L44P_0_A23
20 ■ SYSACE_MPAP5	B23	IO_L44N_0_B23
20 ■ SYSACE_MPAP4	G19	IO_L45P_0/VREF_0_G19
20 ■ SYSACE_MPAP3	H19	IO_L45N_0_H19
20 ■ SYSACE_MPAP2	E18	IO_L46P_0_E18
20 ■ SYSACE_MPAP1	E19	IO_L46N_0_E19
20 ■ SYSACE_MPAP0	B22	IO_L47P_0_B22
20 ■ SYSACE_CLK_OE	C22	IO_L47N_0_C22
47 ■ FPGA_LCD_DB0	F19	IO_L48P_0_F19
47 ■ FPGA_LCD_DB1	F20	IO_L48N_0_F20
47 ■ FPGA_LCD_DB2	F17	IO_L49P_0_F17
47 ■ FPGA_LCD_DB3	G17	IO_L49N_0_G17
47 ■ FPGA_LCD_DB4	B21	IO_L50_0/No_Pair_B21
47 ■ FPGA_LCD_DB5	A21	IO_L53_0/No_Pair_A21
47 ■ FPGA_LCD_DB6	G18	IO_L54P_0_G18
47 ■ FPGA_LCD_DB7	H18	IO_L54N_0_H18
47 ■ FPGA_LCD_DIR	C20	IO_L56P_0_C20
47 ■ FPGA_LCD_E	C21	IO_L56N_0_C21
46 ■ FPGA_LCD_RW	H17	IO_L57P_0/VREF_0_H17
46 ■ FPGA_LCD_RS	J17	IO_L57N_0_J17
18 ■ PM_IO_78	D17	IO_L67P_0_D17
18 ■ PM_IO_79	E17	IO_L67N_0_E17
18 ■ PM_IO_80	C18	IO_L68P_0_C18
18 ■ PM_IO_81	D18	IO_L68N_0_D18
18 ■ PM_IO_82	H16	IO_L69P_0/VREF_0_H16
18 ■ PM_IO_83	J16	IO_L69N_0_J16
48 ■ FPGA_CPU_RESET_N	NC	IO_L73P_0_D16
48 ■ FPGA_CPU_RESET_N	E16	IO_L73N_0_E16
5,10 ■ LVDS_CLKLOC_P	F16	IO_L75P_0/GCLK4S_F16
5,10 ■ LVDS_CLKLOC_N	G16	IO_L75N_0/GCLK5P_G16
18 ■ PM_CLK_TOP	B16	IO_L74P_0/GCLK6S_B16
5 ■ USER_SMA_CLK	C16	IO_L74N_0/GCLK7P_C16

NOTE: IN ORDER TO FACILITATE TEST POINT INSERTION FOR
BGA PACKAGE DEVICES, THE UNUSED PINS ON THE BGAs
ARE TIED TO AN "UNUSED PIN" NET EVEN THOUGH THEY
APPEAR TO BE NO-CONNECTS IN THE SCHEMATIC. PLEASE
CHECK THE NETLISTS BEFORE MODIFYING ANY NC PINS ON
A BGA PACKAGE TO ENSURE THE LAYOUT AND SCHEMATIC
REMAIN CONSISTENT.



SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFORM

BANK0: SYSACE, LCD, SPI

Date: 6-4-2004_12:58 Ver: X.X

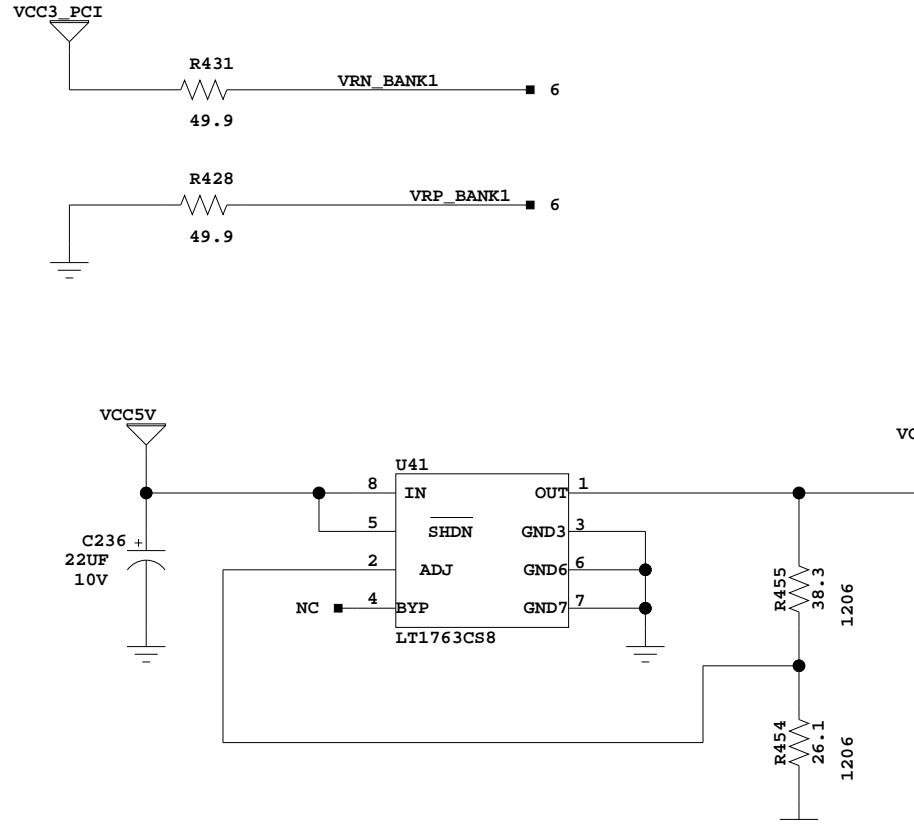
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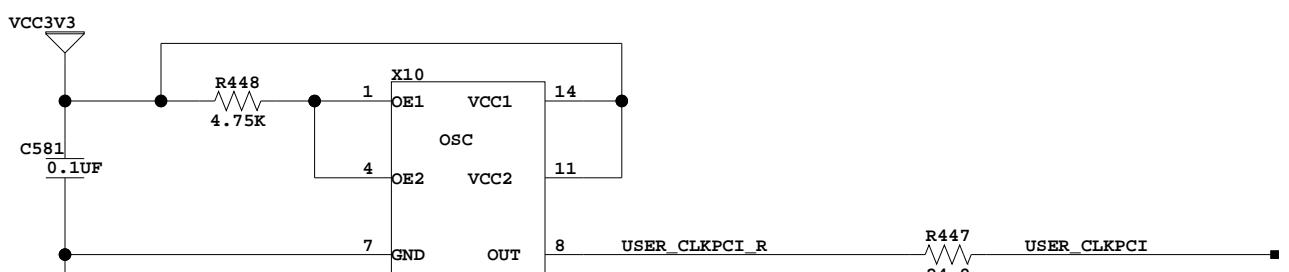
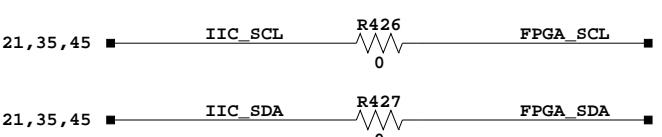
XC2VP20-BANK1

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(DIE DOWN)



NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.

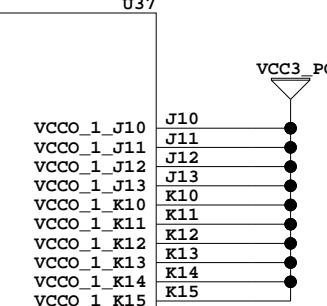


NOTE: X10 IS REPLACED WITH A 100MHZ 3.3V OSCILLATOR

AND IS USED AS THE PRIMARY FPGA REFCLK INPUT ON PRODUCTION BOARDS AS A LOWER COST ALTERNATIVE TO USING A 100MHZ 2.5V OSCILLATOR IN LOCATION X6.

XS10
SOCKETED
14-PIN DIP

6 ■ VRN_BANK1	E6
6 ■ VRP_BANK1	E7
18 ■ PM_IO_3V_0	F7
18 ■ PM_IO_3V_1	F8
18 ■ PM_IO_3V_2	E8
18 ■ PM_IO_3V_3	E9
18 ■ PM_IO_3V_4	NC ■ G8
18 ■ PM_IO_3V_5	H9
18 ■ PM_IO_3V_6	G9
18 ■ PM_IO_3V_7	F9
18 ■ PM_IO_3V_8	F10
18 ■ PM_IO_3V_9	D7
18 ■ PM_IO_3V_10	C7
18 ■ PM_IO_3V_11	H10
18 ■ PM_IO_3V_12	G10
18 ■ PM_IO_3V_13	E10
18 ■ PM_IO_3V_14	D10
18 ■ PM_IO_3V_15	D8
18 ■ PM_IO_3V_16	C8
18 ■ PM_IO_3V_17	H11
18 ■ PM_IO_3V_18	G11
18 ■ PM_IO_3V_19	E11
18 ■ PM_IO_3V_20	D11
18 ■ PM_IO_3V_21	B8
18 ■ PM_IO_3V_22	A8
18 ■ PM_IO_3V_23	H12
18 ■ PM_IO_3V_24	G12
18 ■ PM_IO_3V_25	E12
19 ■ JTAG_SRC_SEL	NC ■ E13
48 ■ UART0_TXD	B9
48 ■ UART0_RTS_N	F11
48 ■ UART0_RXD	F12
48 ■ UART0_CTS_N	G14
48 ■ UART0_RTS_N	F14
48 ■ UART0_CTS_N	B10
46 ■ DBG_LED_0	NC ■ A10
46 ■ DBG_LED_1	H13
46 ■ DBG_LED_2	G13
46 ■ DBG_LED_3	C10
46 ■ DBG_LED_4	C11
46 ■ DBG_LED_5	J14
46 ■ DBG_LED_6	H14
46 ■ DBG_LED_7	E14
46 ■ FPGA_SCL	D13
6 ■ FPGA_SDA	C13
6 ■ IIC_ALERT_N	J15
35,45 ■ IIC_IRQ_N	H15
45 ■ IIC_THERM_N	E15
35,45 ■ IIC_THERM_N	D15
7 ■ PCI_P_CLK5	C15
6 ■ USER_CLKPCI	B15
9,18 ■ LVDS_CLKEXT_P	G15
9,18 ■ LVDS_CLKEXT_N	F15
IO_L74P_1/GCLK0S_C15	
IO_L74N_1/GCLK1P_B15	
IO_L75P_1/GCLK2S_G15	
IO_L75N_1/GCLK3P_F15	



SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFROM

BANK1: PM I/O, UART, DEBUG LED, I2C

Date: 1-5-2004_13:05 Ver: X.X

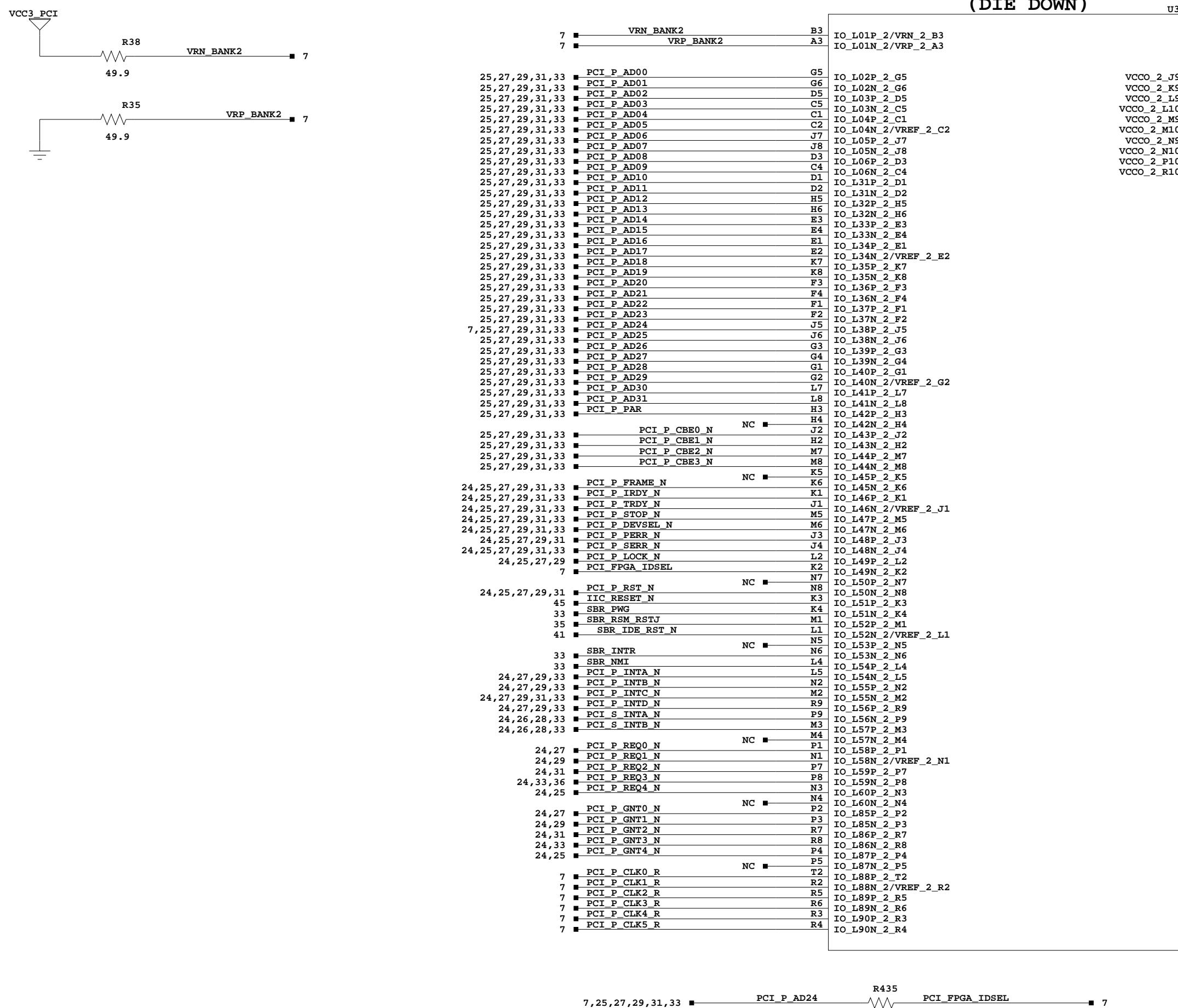
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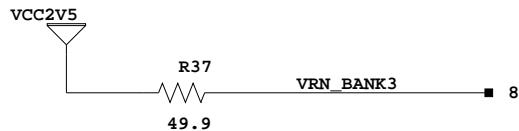
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(DIE DOWN)



	SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
BANK2: PCI BUS, RESET, INTR	
Date:	10-6-2003_14:59
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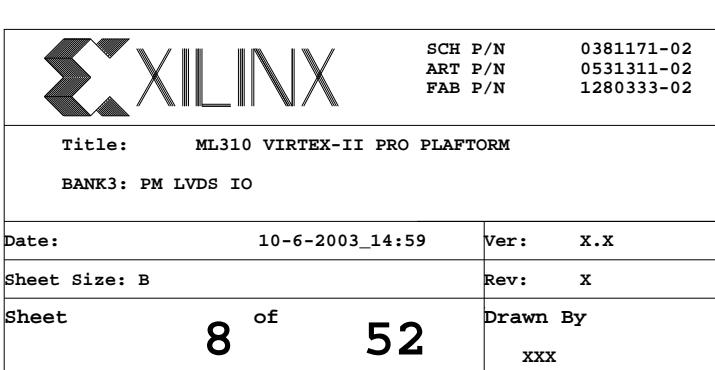
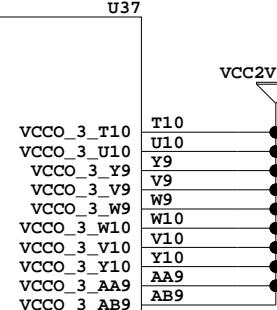


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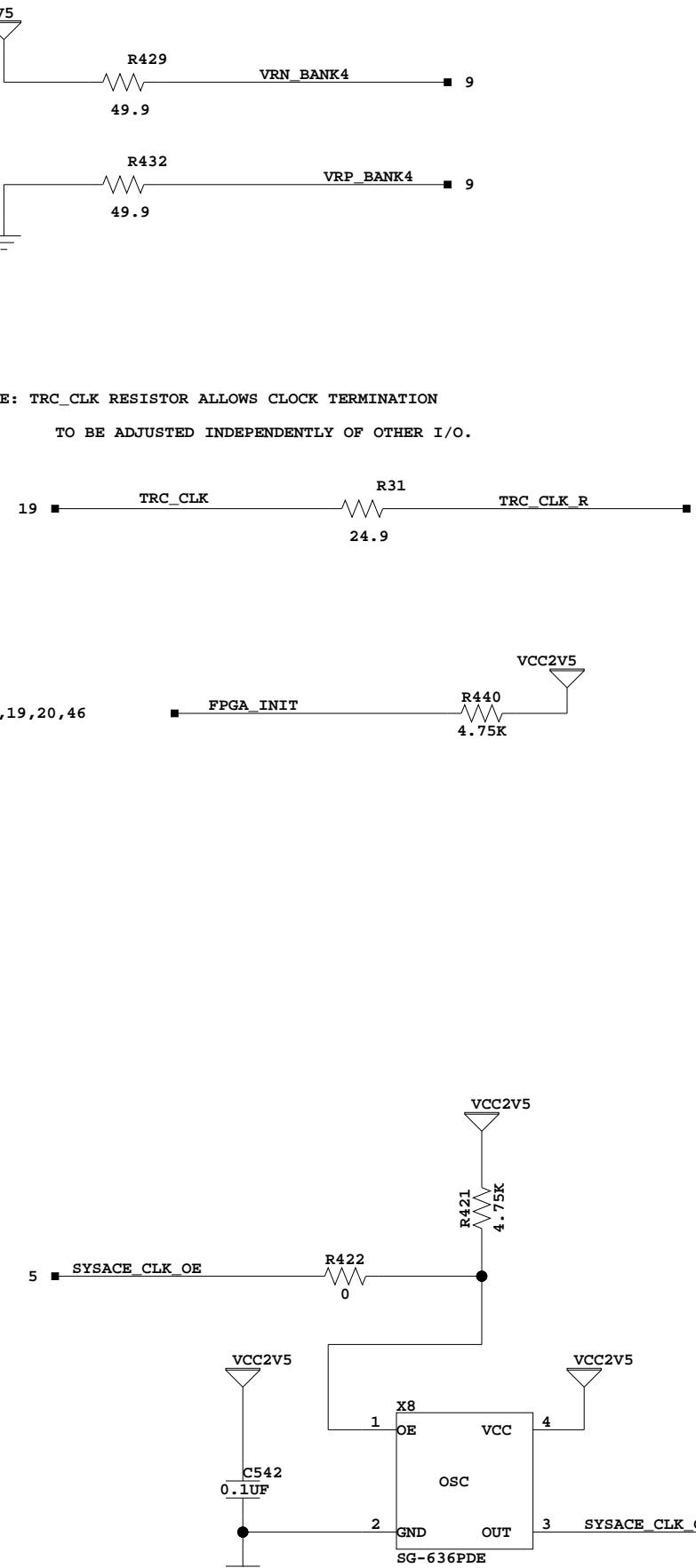
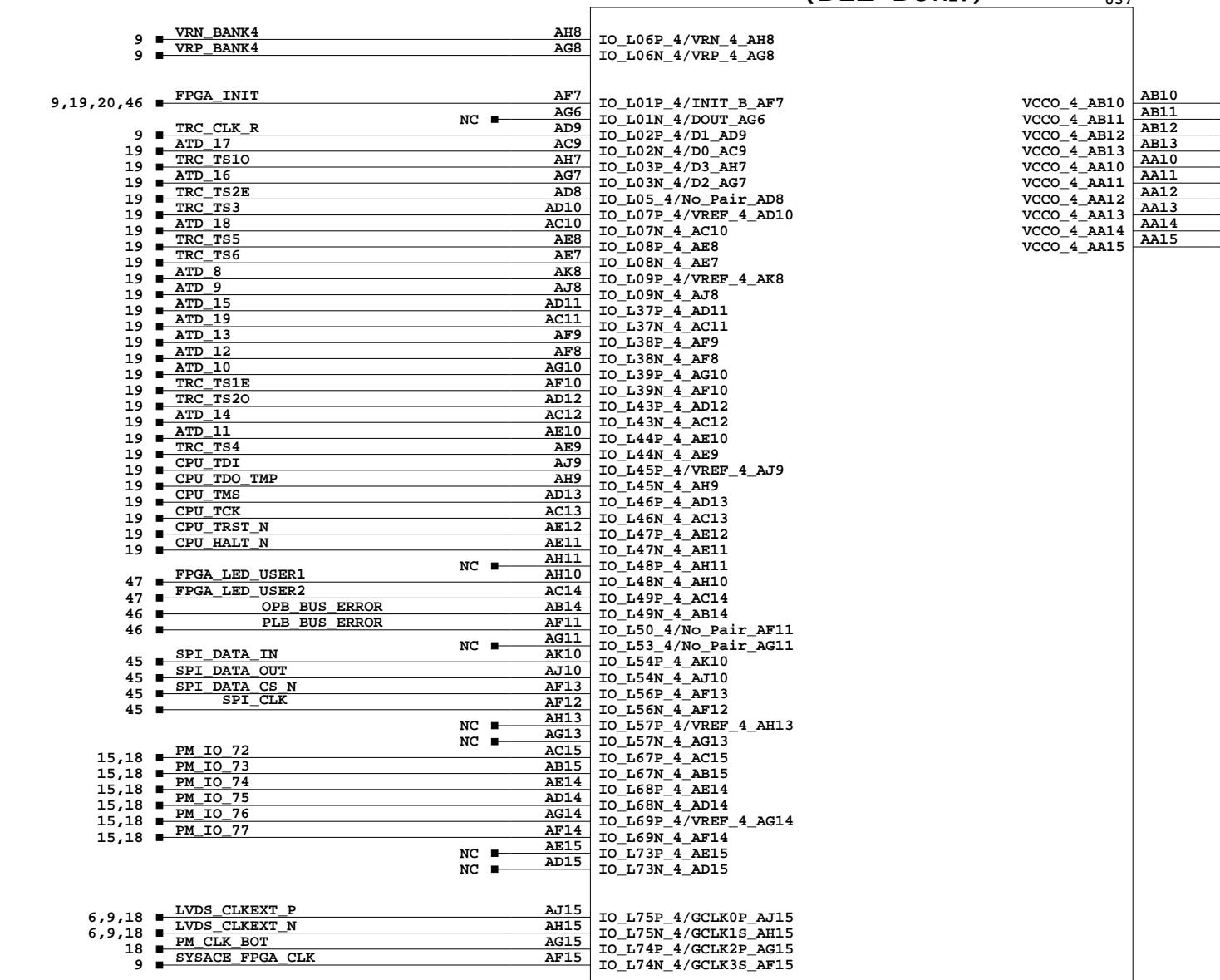
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	VRN_BANK3	AJ3	U37
8	VRN_BANK3	IO_L01P_3/VRN_3_AK3 IO_L01N_3/VRP_3_AJ3	
15,18	PM_IO_0	AH5	
15,18	PM_IO_1	AG5	
15,18	PM_IO_2	AH2	
15,18	PM_IO_3	AH1	IO_L02P_3_AH5 IO_L02N_3_AG5
15,18	PM_IO_4	AH4	IO_L03P_3_AH2 IO_L03N_3/VREF_3_AH1
15,18	PM_IO_5	AG3	IO_L04P_3_AH4 IO_L04N_3_AG3
15,18	PM_IO_6	AD6	IO_L05P_3_AD6 IO_L05N_3_AD5
15,18	PM_IO_7	NC ■ AD5	IO_L06P_3_AG2 IO_L06N_3_AG1
15,18	PM_IO_8	AG1	IO_L131P_3_AF6 IO_L132P_3_AB8
15,18	PM_IO_9	AE5	IO_L131N_3_AE5 IO_L132N_3_AB7
15,18	PM_IO_10	AB8	IO_L133P_3_AE4 IO_L133N_3/VREF_3_AE3
15,18	PM_IO_11	AE4	IO_L134P_3_AF4 IO_L134N_3_AF3
15,18	PM_IO_12	AF4	IO_L135P_3_AC6 IO_L135N_3_AC5
15,18	PM_IO_13	AF3	IO_L136P_3_AF2 IO_L136N_3_AF1
15,18	PM_IO_14	AC6	IO_L137P_3_AD4 IO_L137N_3_AD3
15,18	PM_IO_15	AC5	IO_L138P_3_AA8 IO_L138N_3_AA7
15,18	PM_IO_16	AF1	IO_L139P_3_AE2 IO_L139N_3/VREF_3_AE1
15,18	PM_IO_17	AD4	IO_L140P_3_AB6 IO_L140N_3_AB5
15,18	PM_IO_18	AD3	IO_L141P_3_Y8 IO_L141N_3_Y7
15,18	PM_IO_19	AA8	IO_L142P_3_AD2 IO_L142N_3_AD1
15,18	PM_IO_20	AE1	IO_L143P_3_AC4 IO_L143N_3_AC3
15,18	PM_IO_21	AB6	IO_L144P_3_AA6 IO_L144N_3_AA5
15,18	PM_IO_22	AB5	IO_L145P_3_AC2 IO_L145N_3/VREF_3_AB2
15,18	PM_IO_23	AD1	IO_L146P_3_AB4 IO_L146N_3_AB3
15,18	PM_IO_24	AC4	IO_L147P_3_W8 IO_L147N_3_W7
15,18	PM_IO_25	AC3	IO_L148P_3_AA4 IO_L148N_3_AA3
15,18	PM_IO_26	AA6	IO_L149P_3_Y5 IO_L149N_3_Y4
15,18	PM_IO_27	AA5	IO_L150P_3_W6 IO_L150N_3_W5
15,18	PM_IO_28	AC2	IO_L151P_3_AB1 IO_L151N_3/VREF_3_AA1
15,18	PM_IO_29	AB2	IO_L152P_3_W4 IO_L152N_3_W3
15,18	PM_IO_30	AB4	IO_L153P_3_V8 IO_L153N_3_V7
15,18	PM_IO_31	AB3	IO_L154P_3_AA2 IO_L154N_3_Y2
15,18	PM_IO_32	W8	IO_L155P_3_V6 IO_L155N_3_V5
15,18	PM_IO_33	W5	IO_L156P_3_U8 IO_L156N_3_U7
15,18	PM_IO_34	AA4	IO_L157P_3_Y1 IO_L157N_3/VREF_3_W1
15,18	PM_IO_35	AA3	IO_L158P_3_V4 IO_L158N_3_V3
18	PM_IO_36	Y5	IO_L159P_3_U9 IO_L159N_3_T9
18	PM_IO_37	Y4	IO_L160P_3_W2 IO_L160N_3_V2
18	PM_IO_38	W6	IO_L161P_3_U5 IO_L161N_3_U4
18	PM_IO_39	W5	IO_L162P_3_T8 IO_L162N_3_T7
18	PM_IO_40	AB1	IO_L163P_3_U3 IO_L163N_3_T5
18	PM_IO_41	AA1	IO_L164P_3_U2 IO_L164N_3_V1
18	PM_IO_42	W4	IO_L165P_3_U1
18	PM_IO_43	W3	
18	PM_IO_44	V8	
18	PM_IO_45	V7	
18	PM_IO_46	AA2	
18	PM_IO_47	Y2	
18	PM_IO_48	V6	
18	PM_IO_49	V5	
18	PM_IO_50	U8	
18	PM_IO_51	U7	
18	PM_IO_52	Y1	
18	PM_IO_53	W1	
18	PM_IO_54	V4	
18	PM_IO_55	V3	
18	PM_IO_56	U9	
18	PM_IO_57	T9	
18	PM_IO_58	W2	
18	PM_IO_59	V2	
18	PM_IO_60	U5	
18	PM_IO_61	U4	
18	PM_IO_62	T8	
18	PM_IO_63	T7	
18	PM_IO_64	U3	
18	PM_IO_65	U2	
18	PM_IO_66	T4	
18	PM_IO_67	T3	
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18	PM_IO_71	U1	

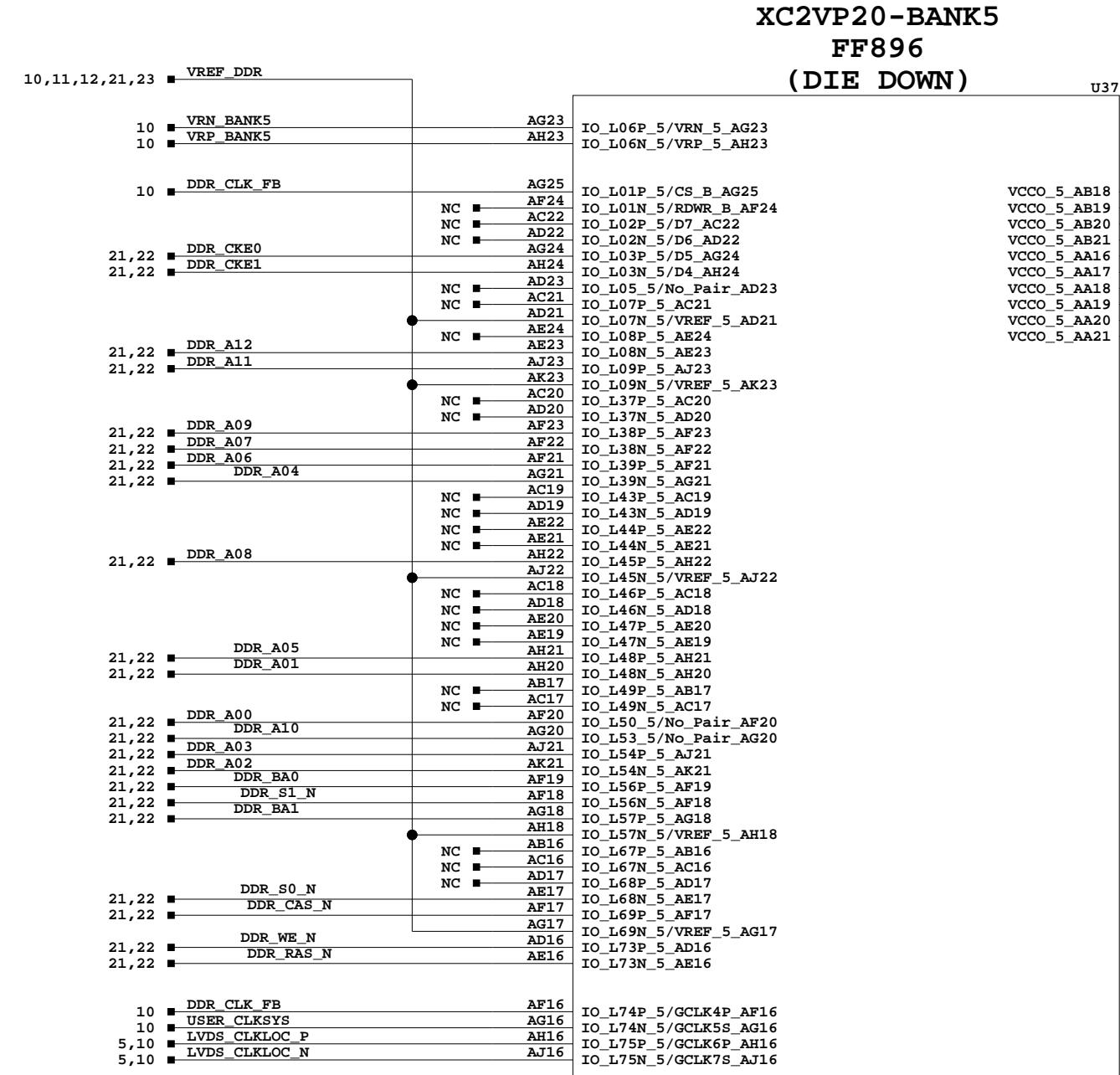
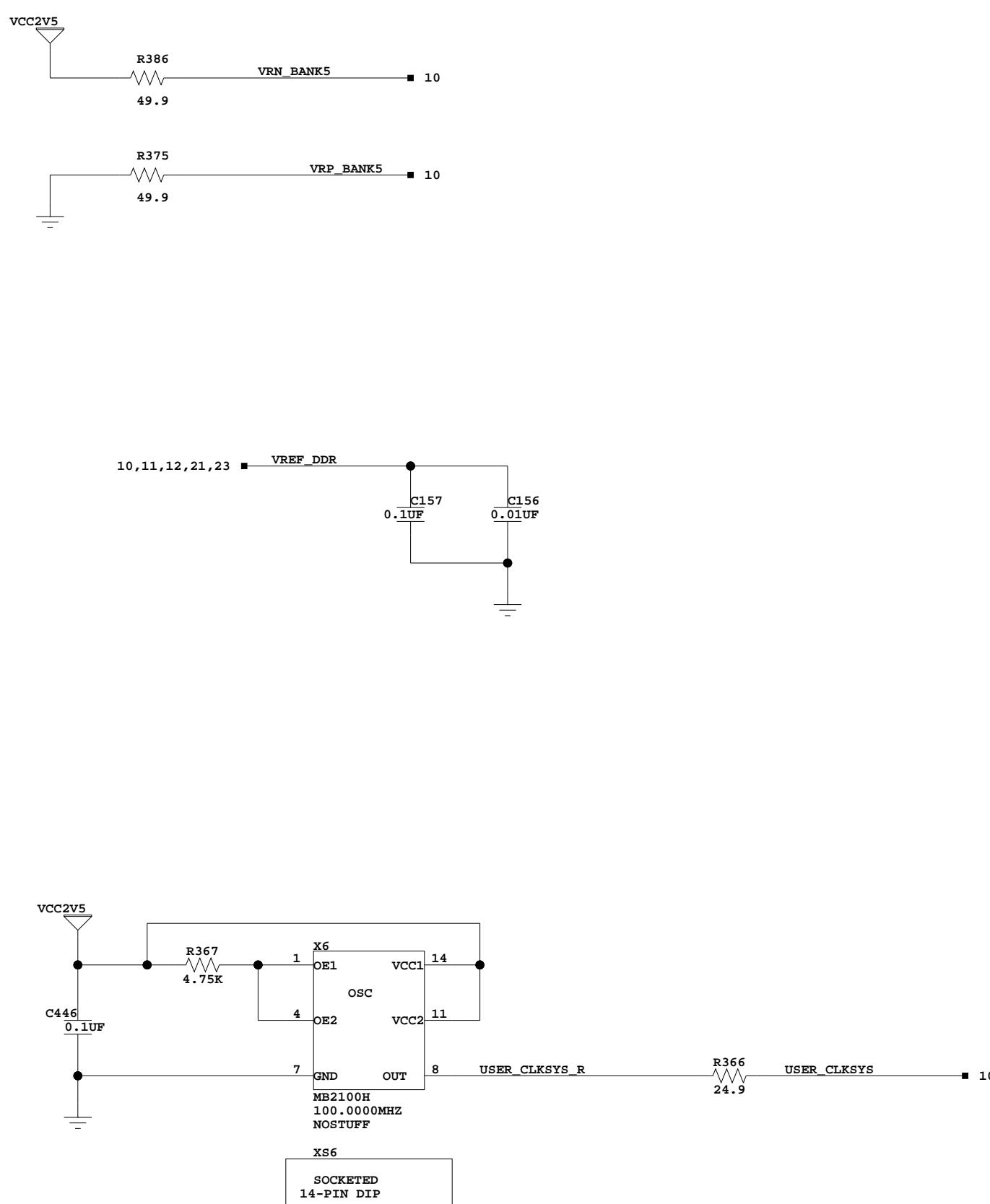


XC2VP20-BANK4
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Date: 1-5-2004_13:05 Ver: x.x
Sheet Size: B Rev: x
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SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02



SCH P/N	0381171-02
ART P/N	0531311-02
FAB P/N	1280333-02

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RANKS: DDB

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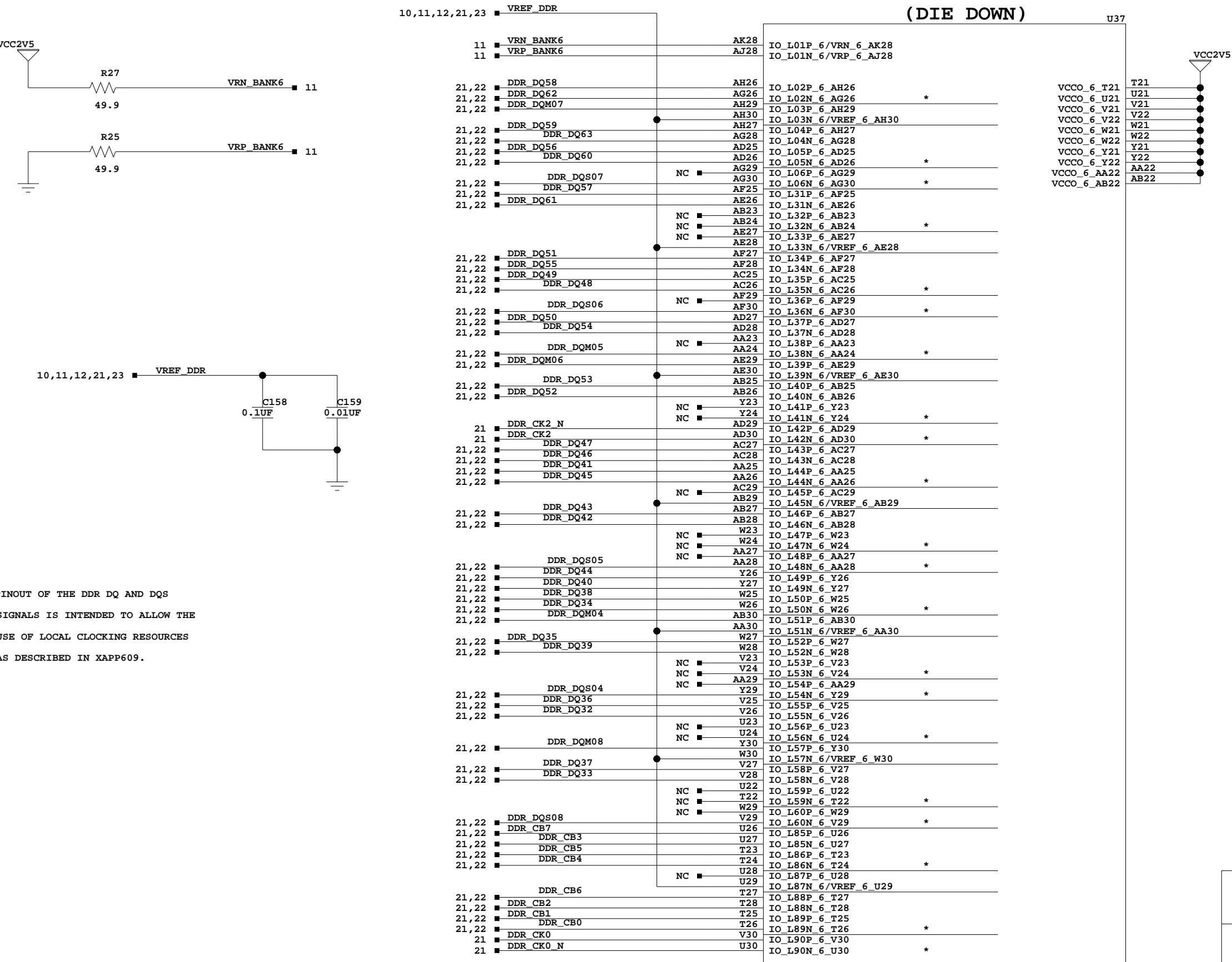
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XC2VP20-BANK6

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(DIE DOWN)



SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFROM

BANK6: DDR

Date: 10-6-2003_14:59 Ver: x.x

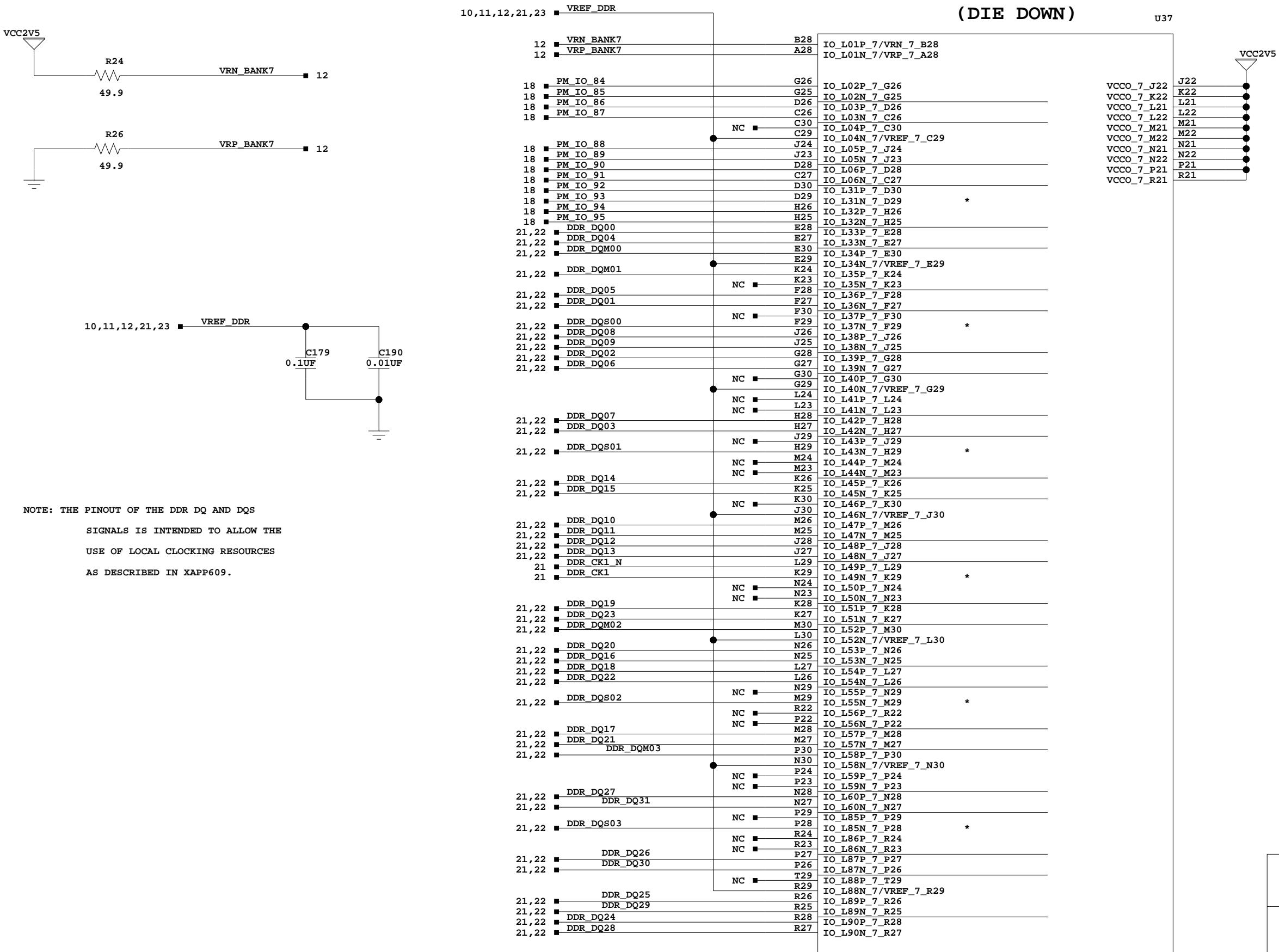
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Sheet 11 of 52 Drawn By xxx

XC2VP20-BANK7

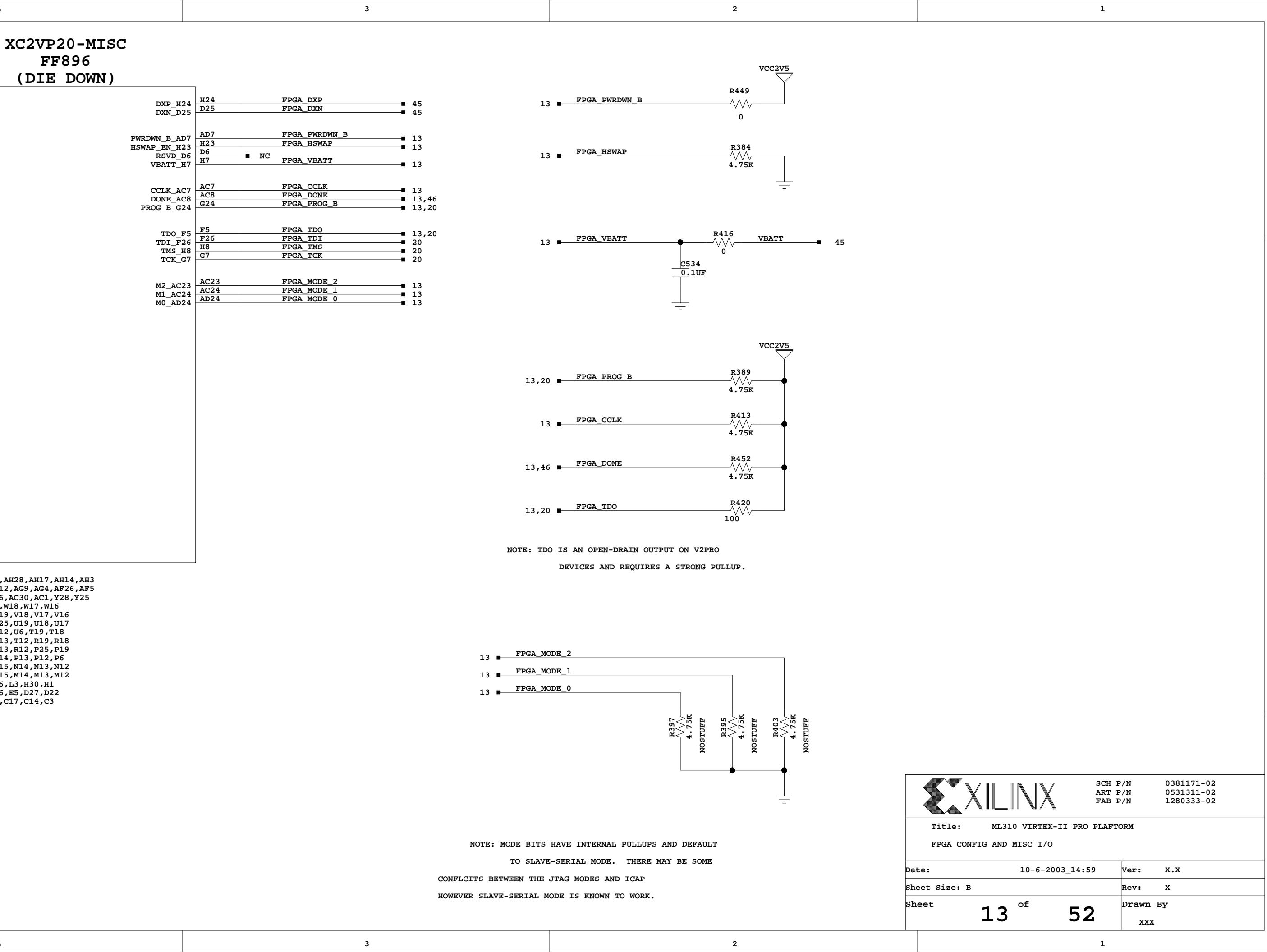
FF896

(DIE DOWN)



NOTE: THE PINOUT OF THE DDR DQ AND DQS SIGNALS IS INTENDED TO ALLOW THE USE OF LOCAL CLOCKING RESOURCES AS DESCRIBED IN XAPP609.

XILINX	SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
BANK7: DDR	
Date: 10-6-2003_14:59	Ver: x.x
Sheet Size: B	Rev: x
Sheet 12 of 52	Drawn By xxx

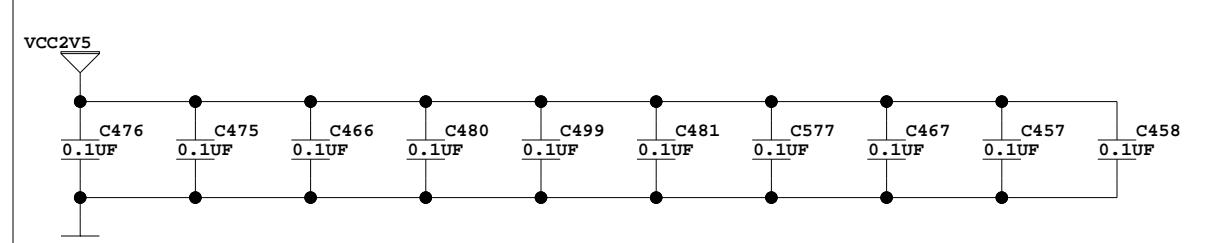


4

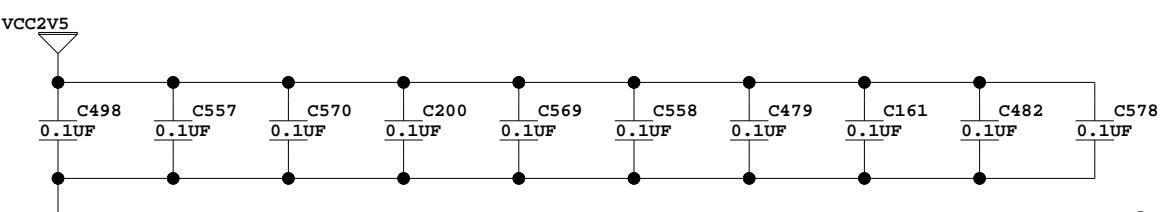
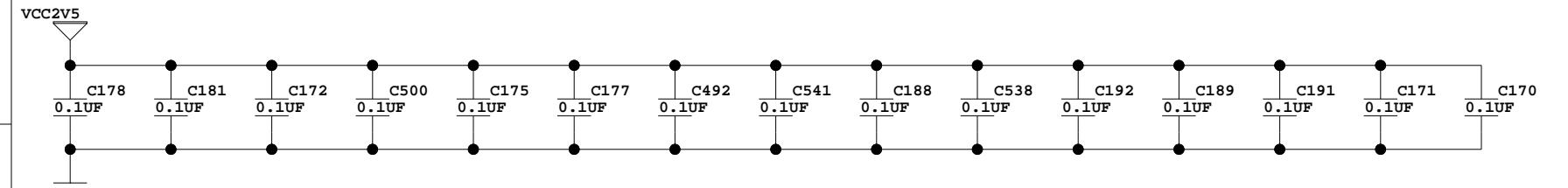
3

2

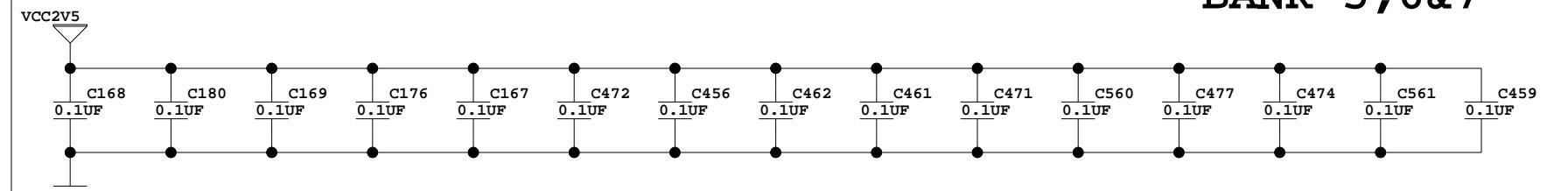
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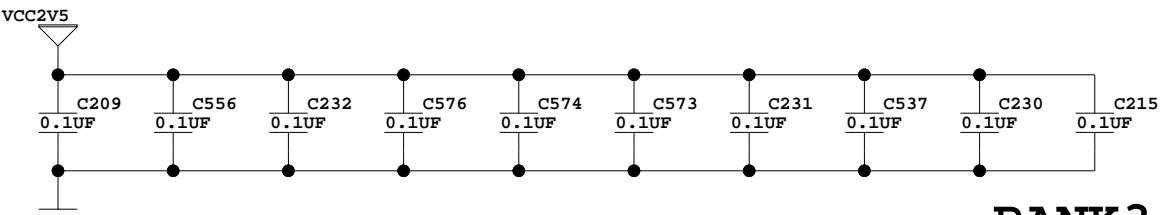
BANK 0



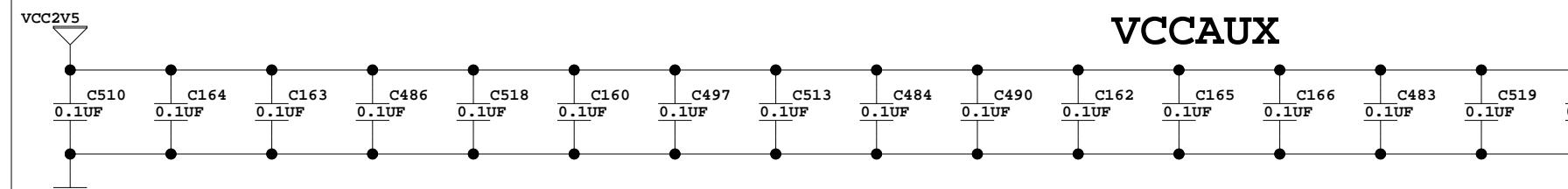
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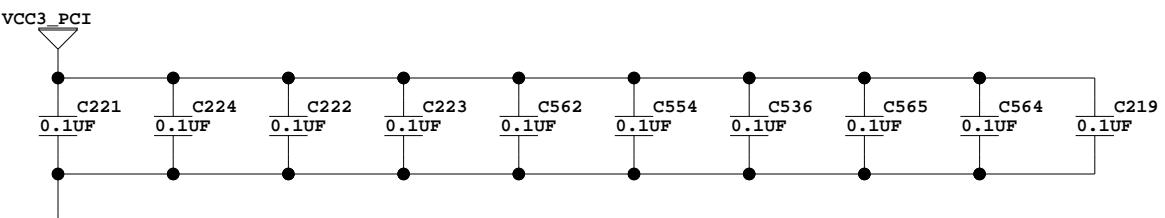
BANK 5, 6 & 7



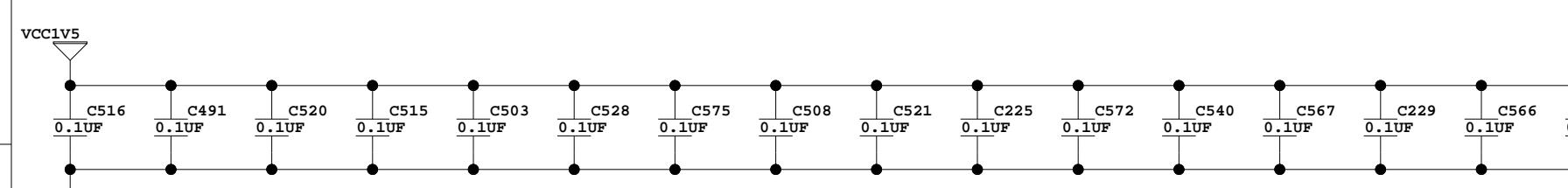
BANK 3



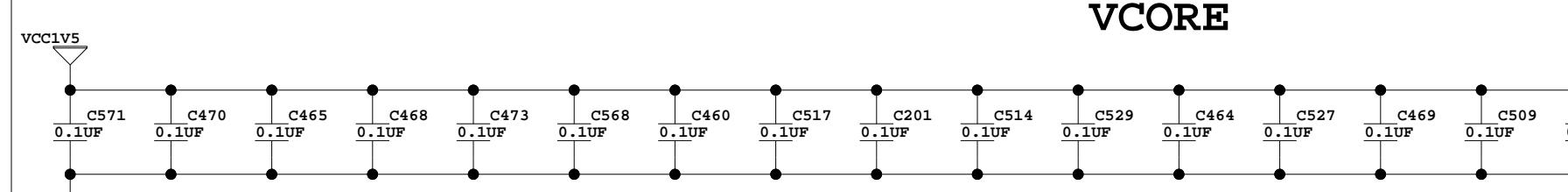
VCCAUX



BANK 1

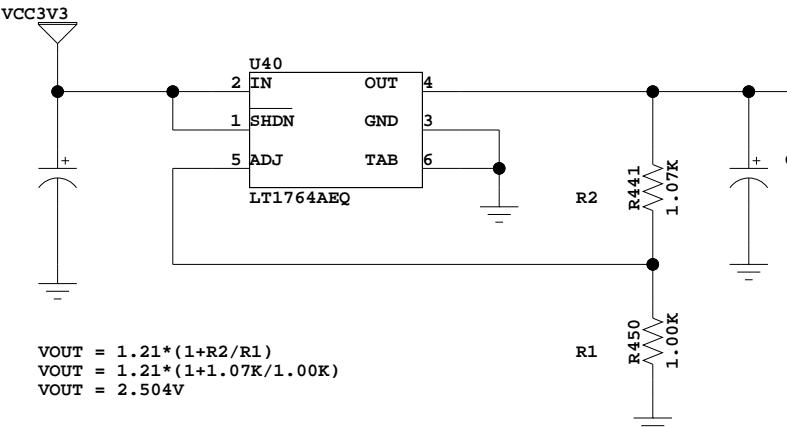


BANK 2

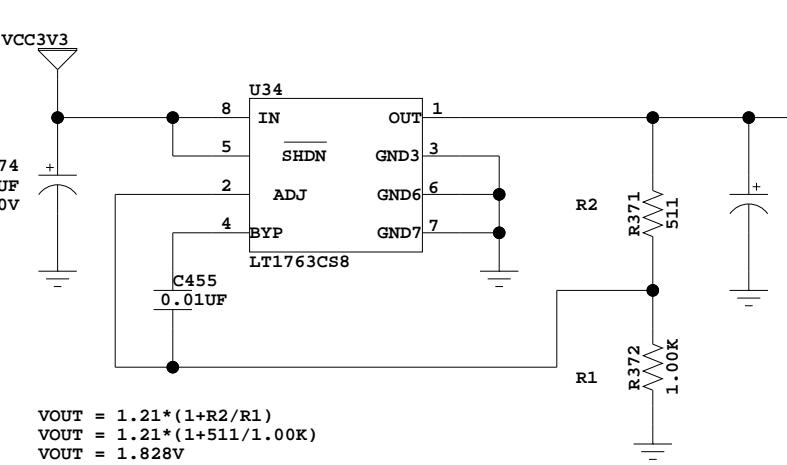
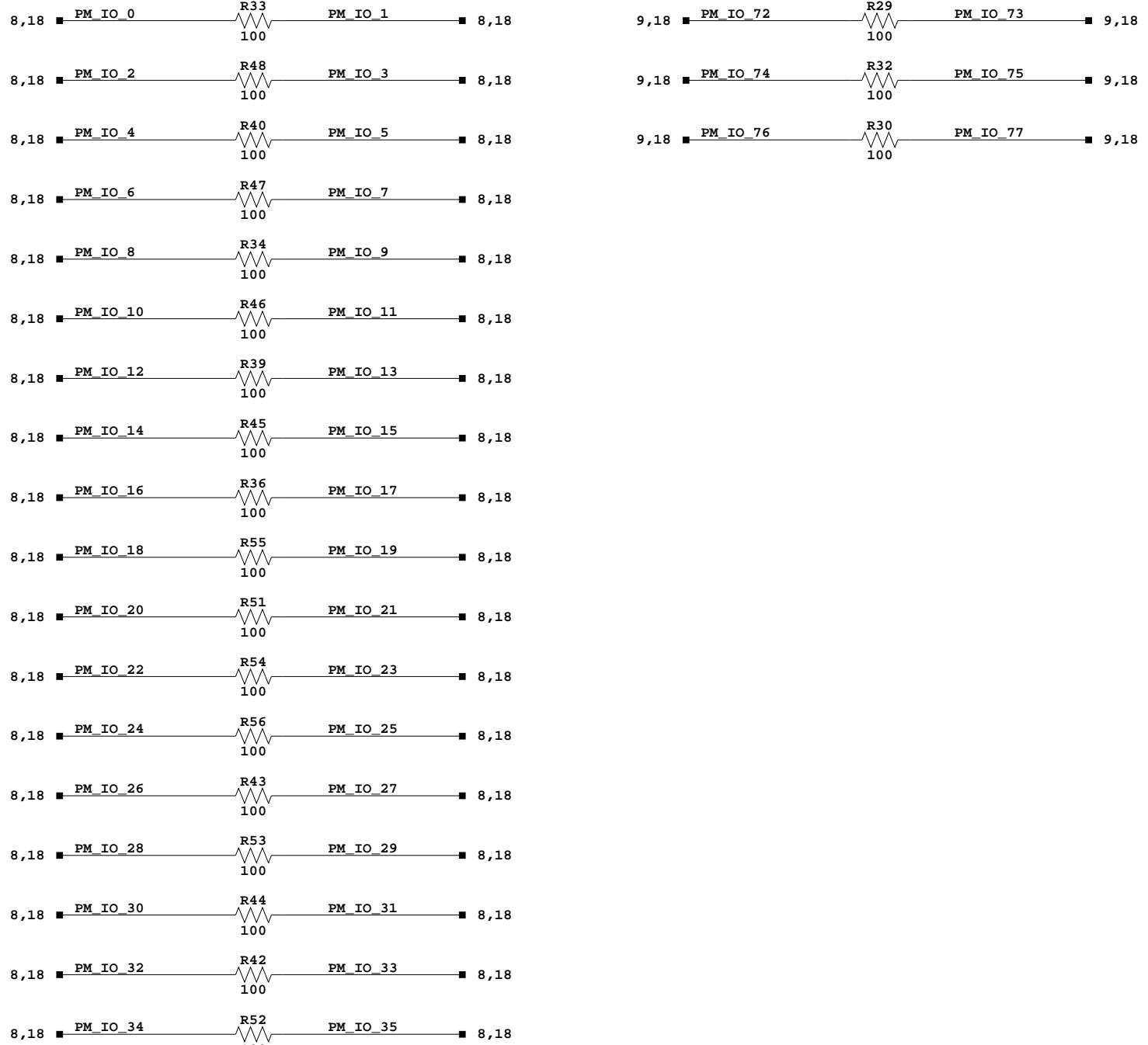


VCORE

	XILINX	SCH P/N ART P/N FAB P/N	0381171-02 0531311-02 1280333-02
Title:	ML310 VIRTEX-II PRO PLATFROM		
FPGA DECOUPLING			
Date:	1-5-2004_13:05	Ver:	x.x
Sheet Size:	B	Rev:	x
Sheet	14 of 52	Drawn By	xxx

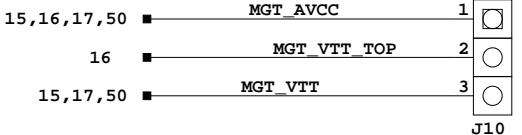
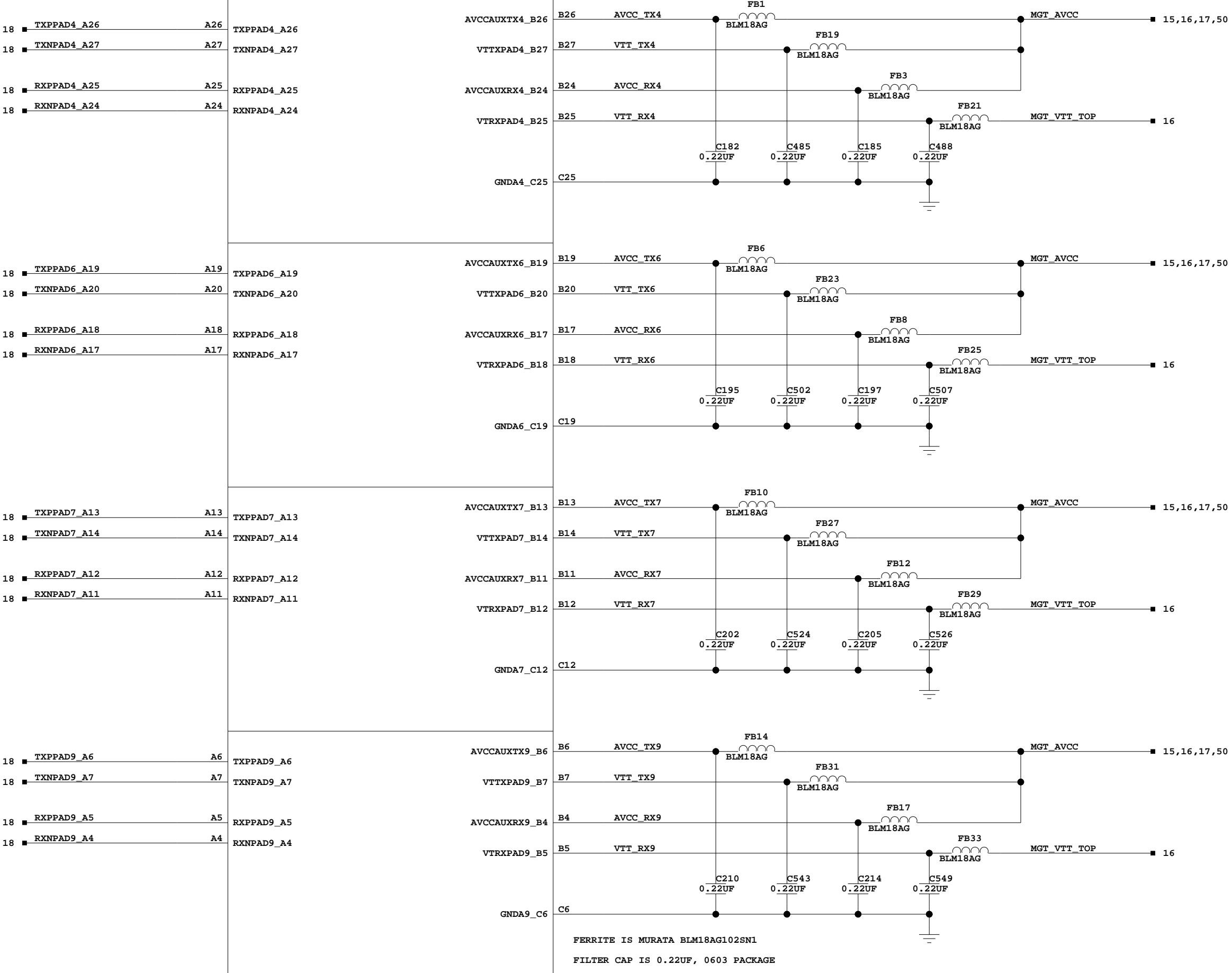


LVDS RECEIVE TERMINATION



		SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM		MGT POWER SUPPLIES,LVDS TERMINATION
Date:	10-6-2003_14:59	Ver: X.X
Sheet Size:	B	Rev: X
Sheet	15 of 52	Drawn By XXX

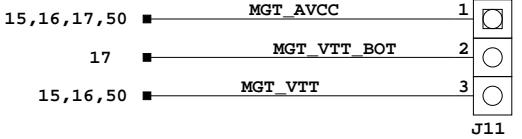
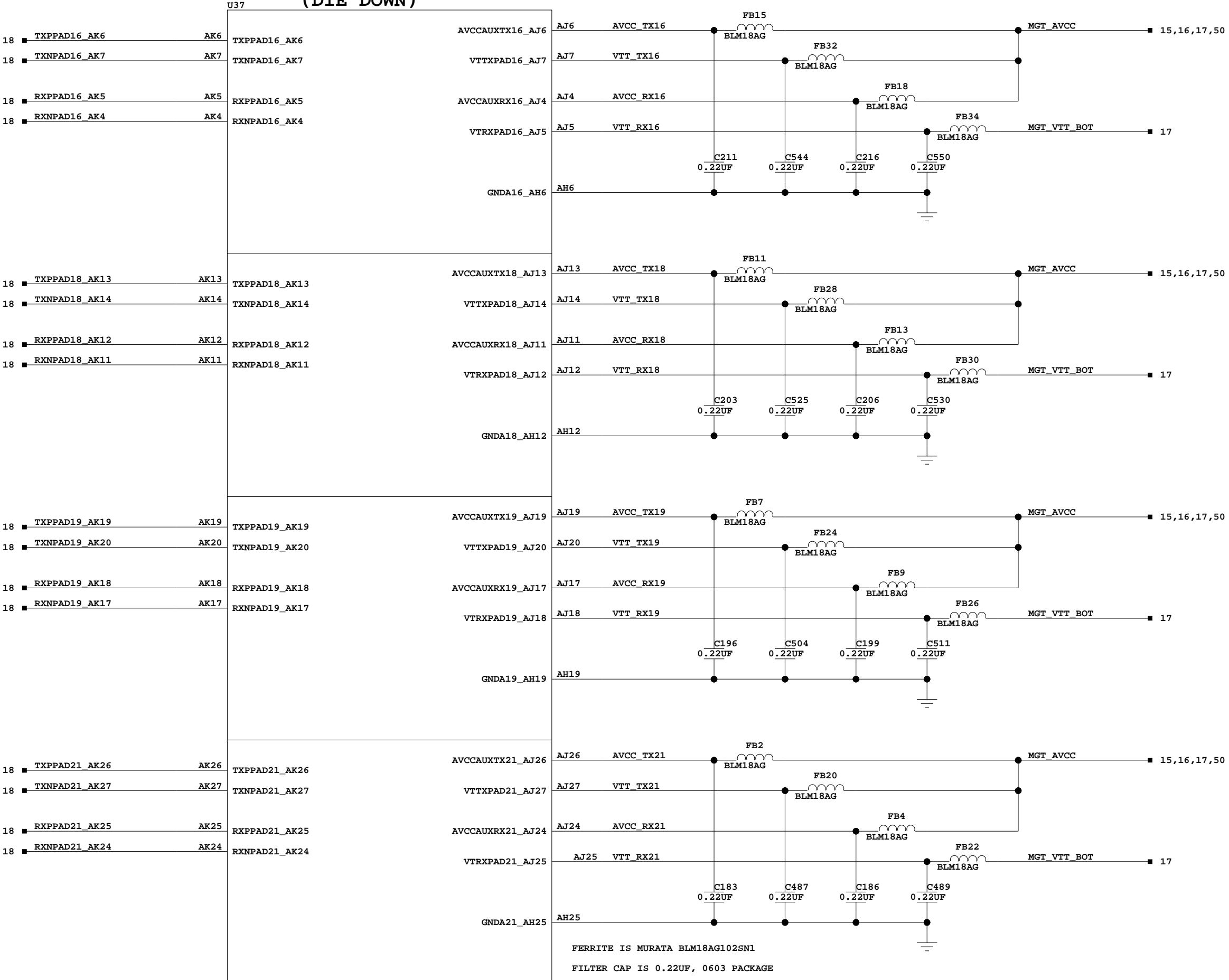
XC2VP20-TOP
FF896
(DIE DOWN)



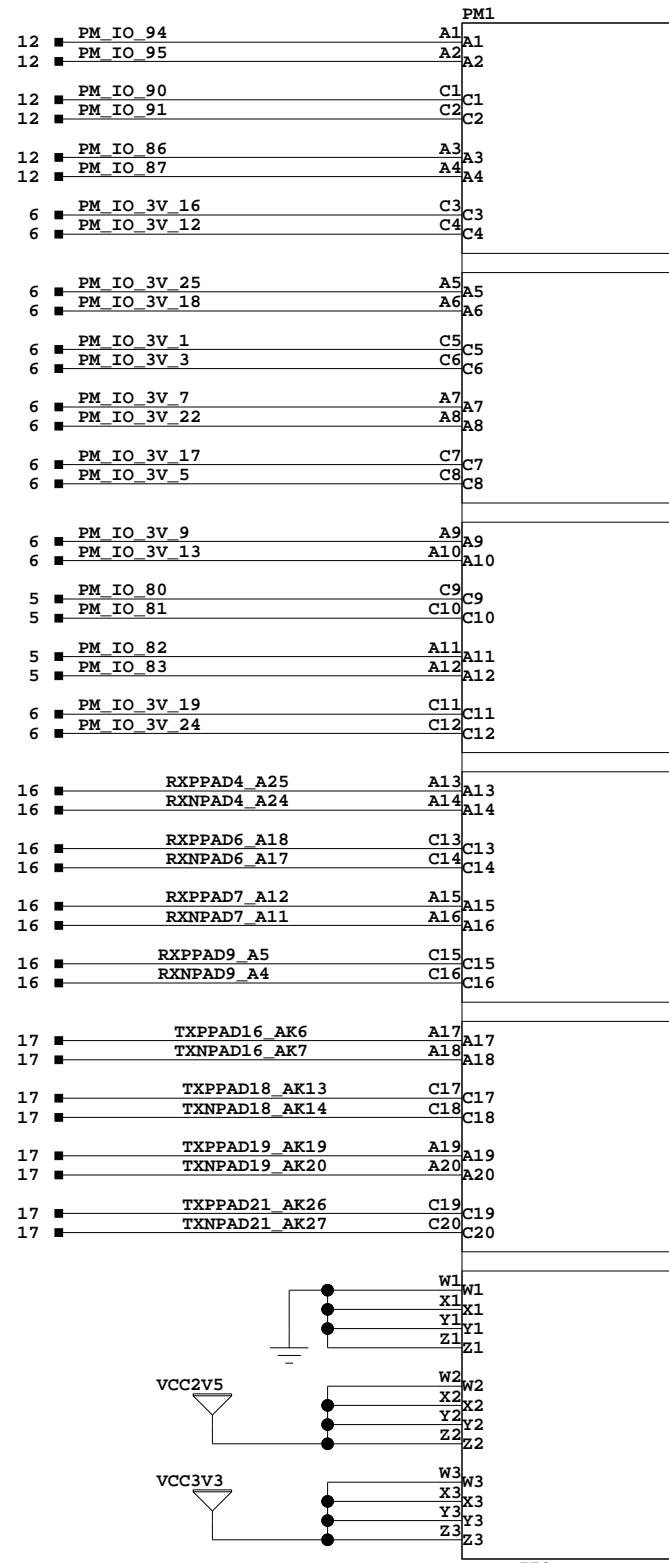
XILINX

SCH P/N	0381171-02
ART P/N	0531311-02
FAB P/N	1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
TOP MGT TRANSCEIVERS	
Date:	6-4-2004_12:59
Sheet Size:	B
Sheet	16 of 52
Drawn By	xxx

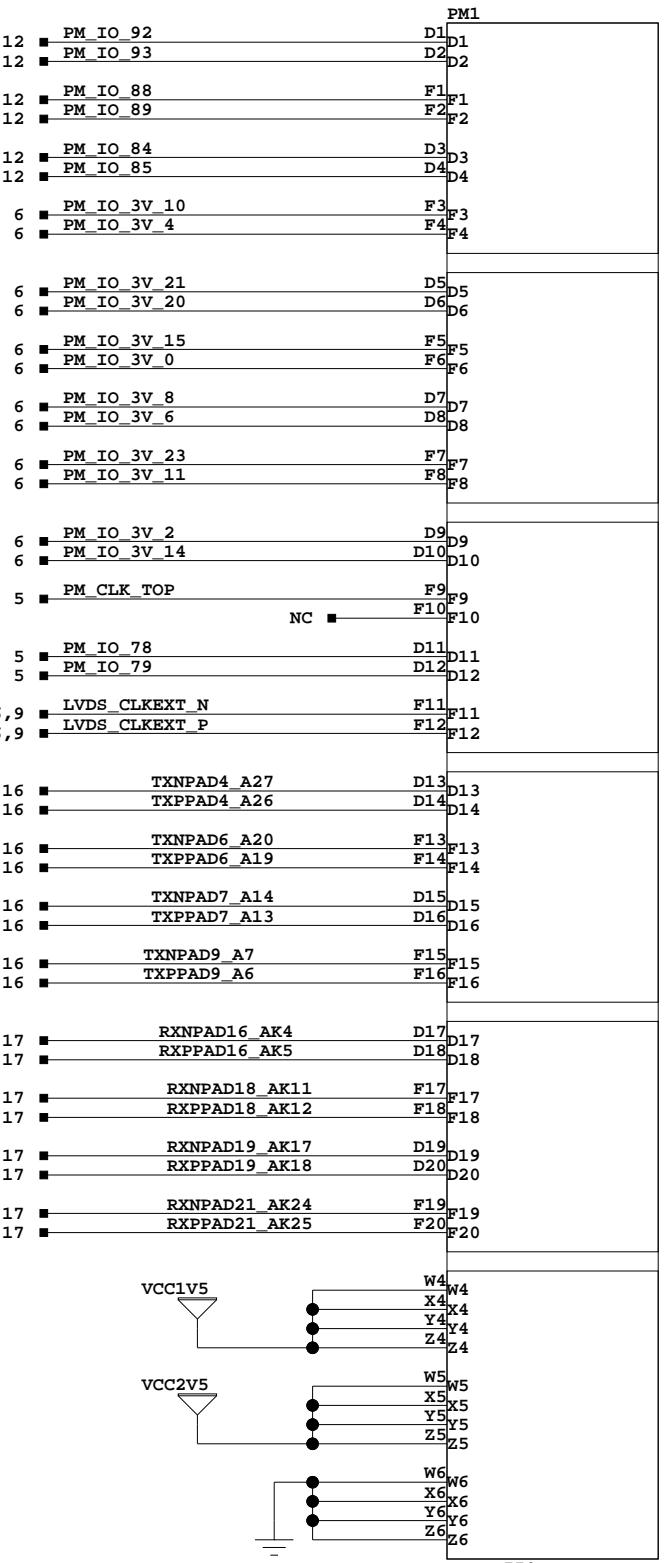
**XC2VP20-BOT
FF896
(DIE DOWN)**



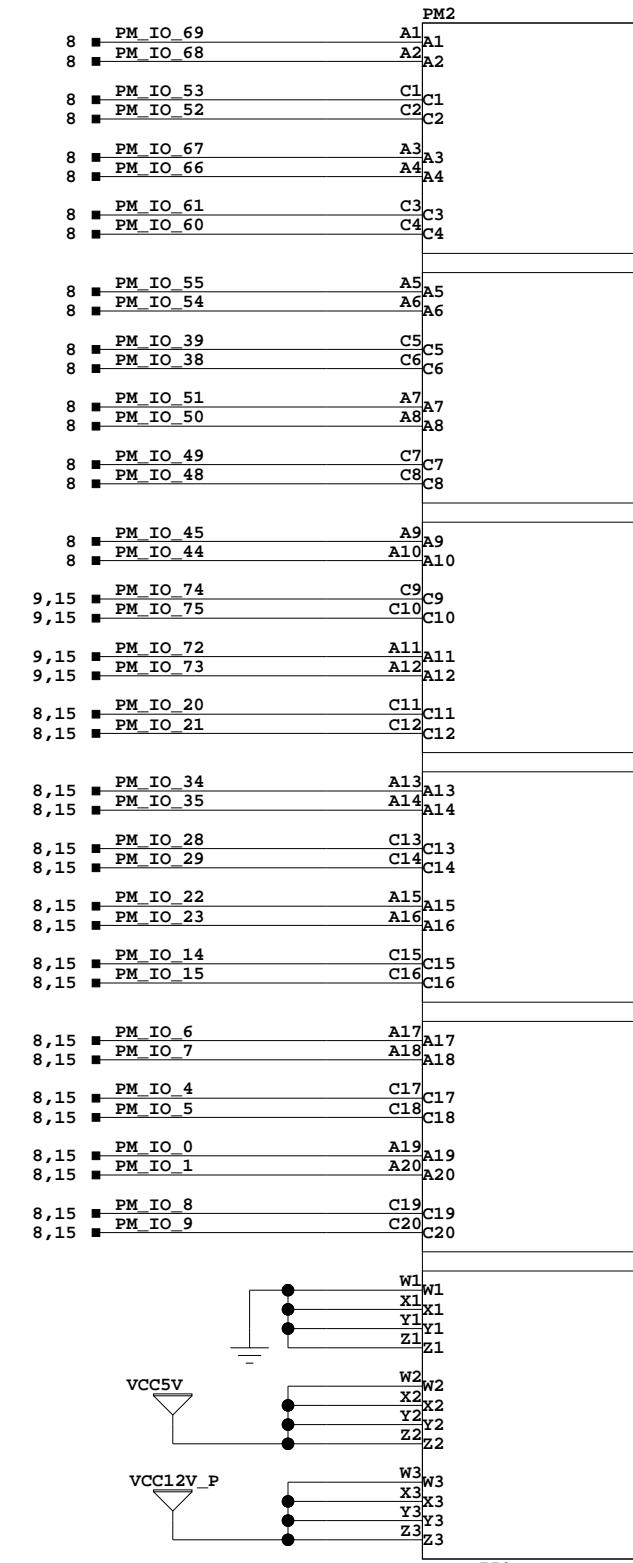
	SCH P/N ART P/N FAB P/N	0381171-02 0531311-02 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM		
BOT MGT TRANSCEIVERS		
Date:	6-4-2004_12:59	Ver: X.X
Sheet Size: B		Rev: X
Sheet 17 of 52		Drawn By xxx



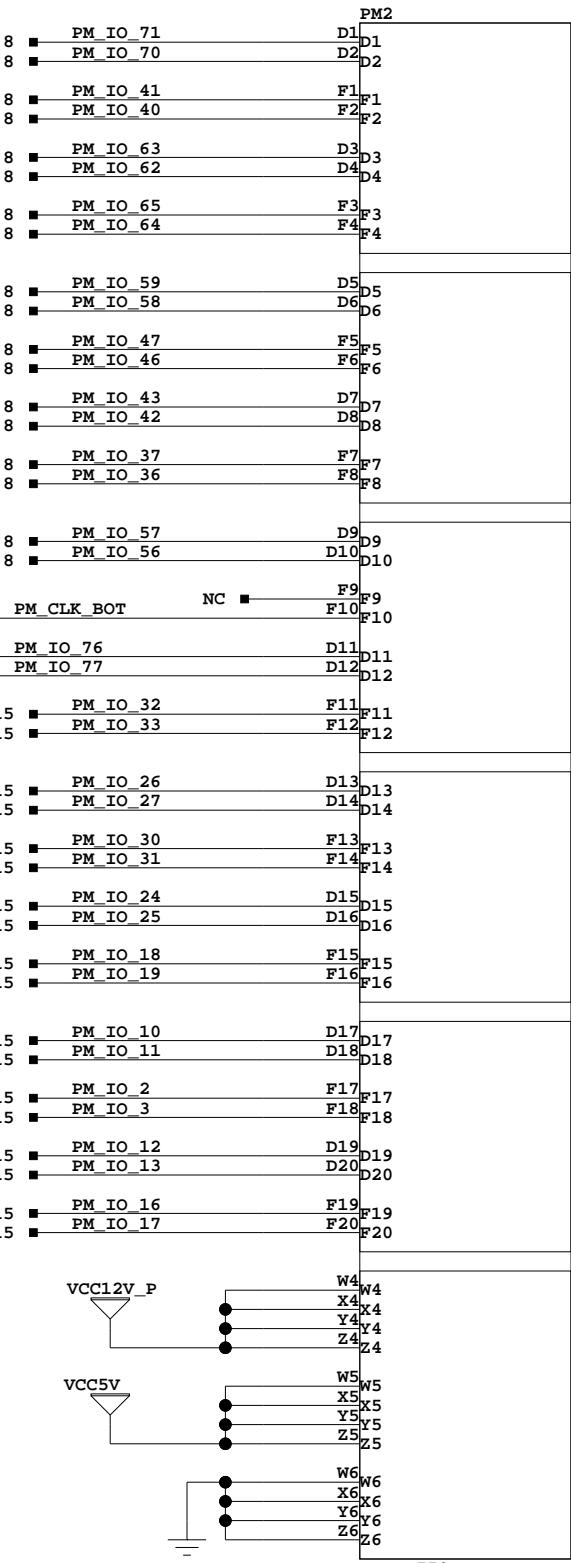
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GND;B11,B12,B13,B14,B15
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GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20



GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20



GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
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SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

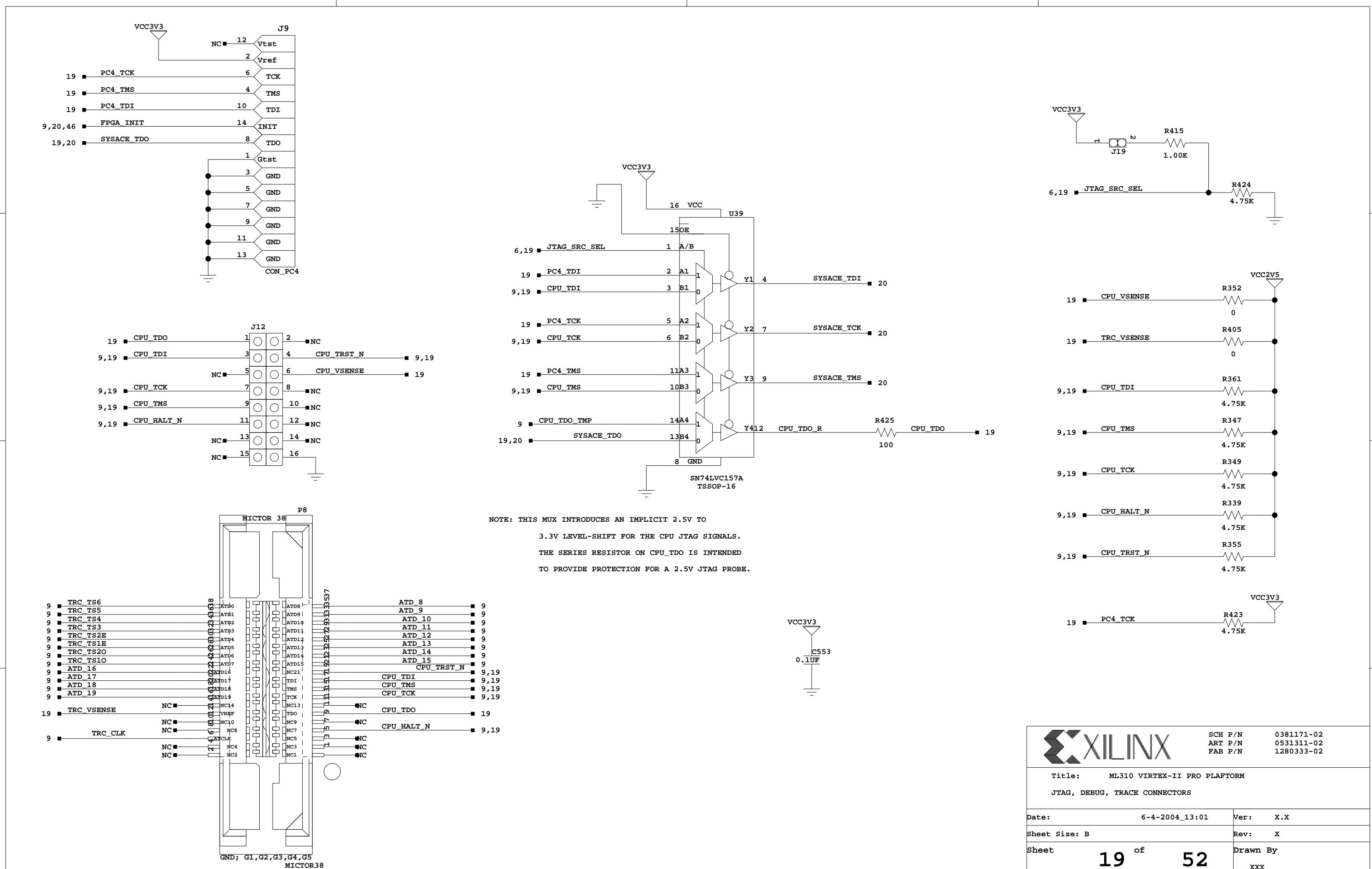
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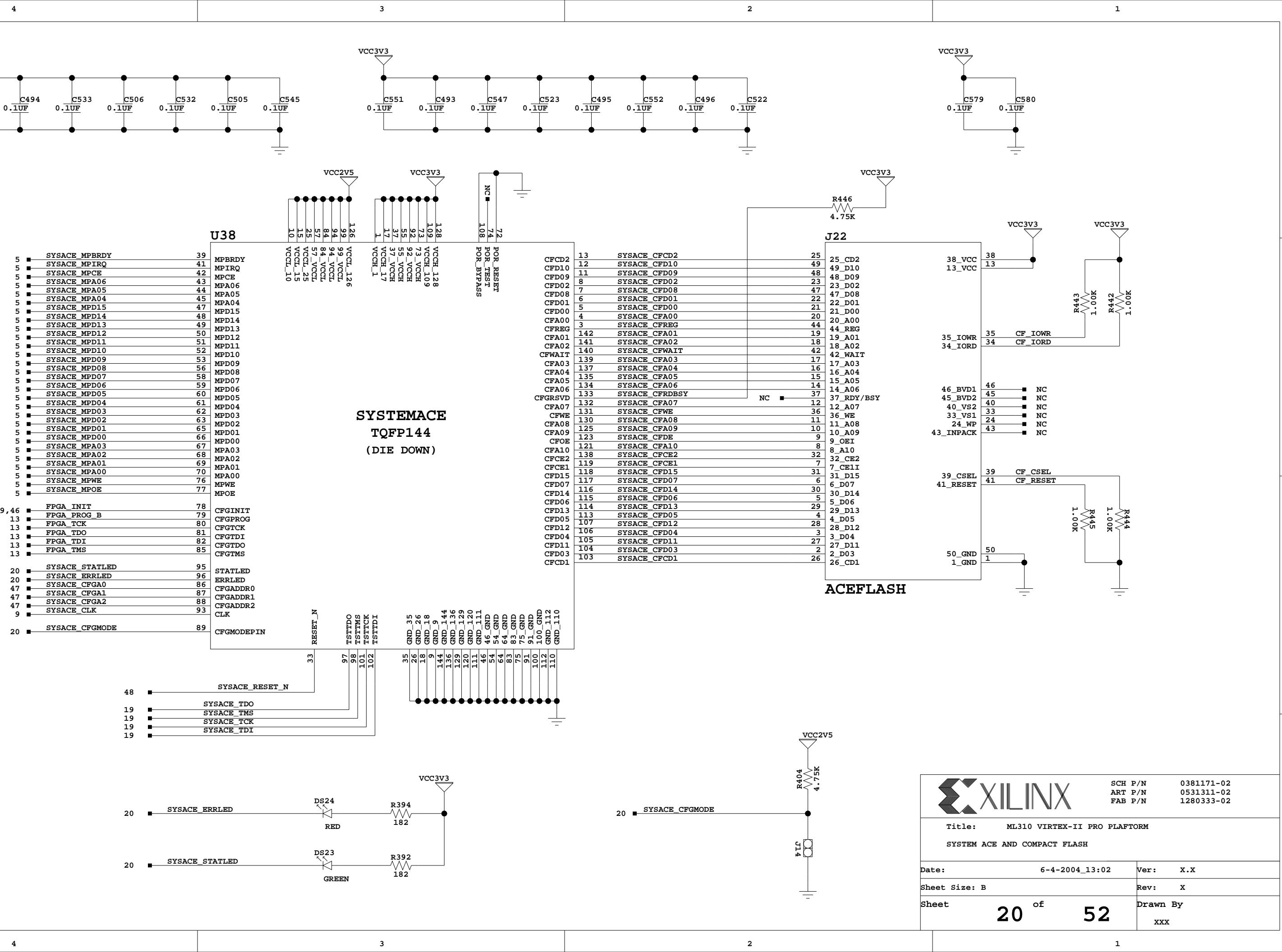
PERSONALITY MODULE CONNECTORS

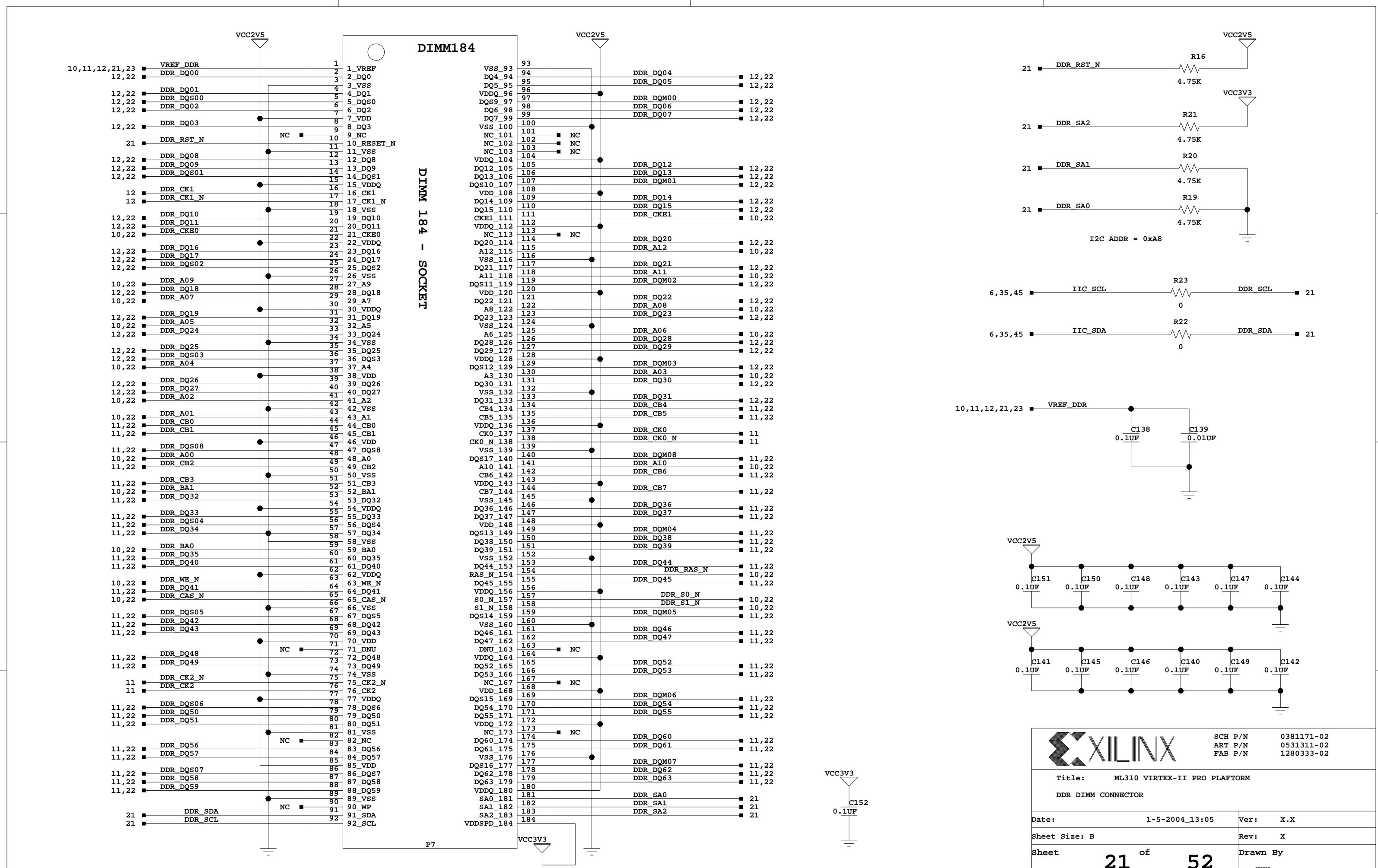
Date: 10-6-2003_14:59 Ver: X.X

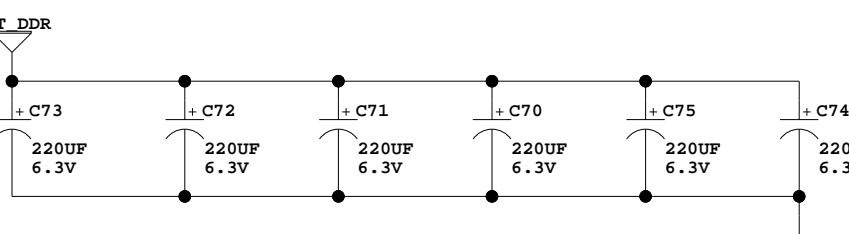
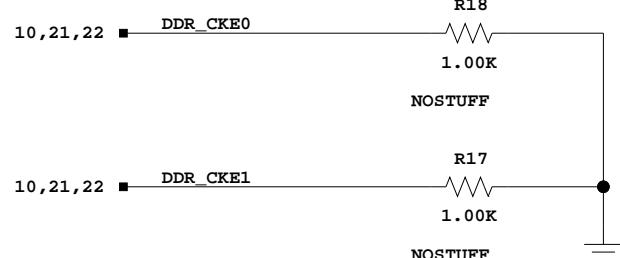
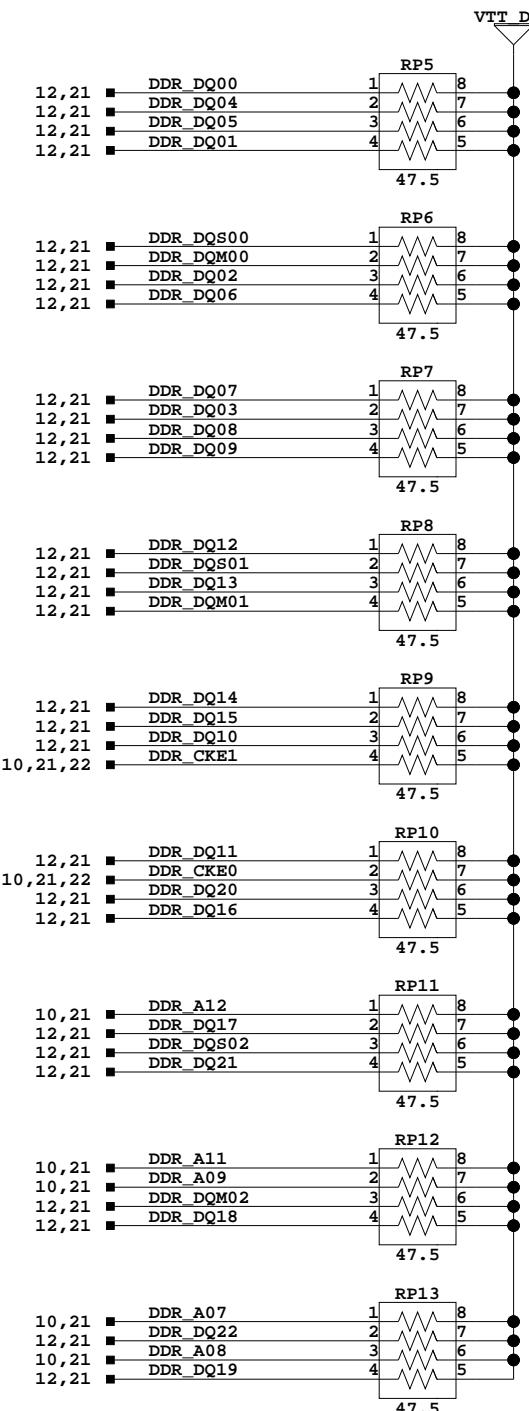
Sheet Size: B Rev: X

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C

C

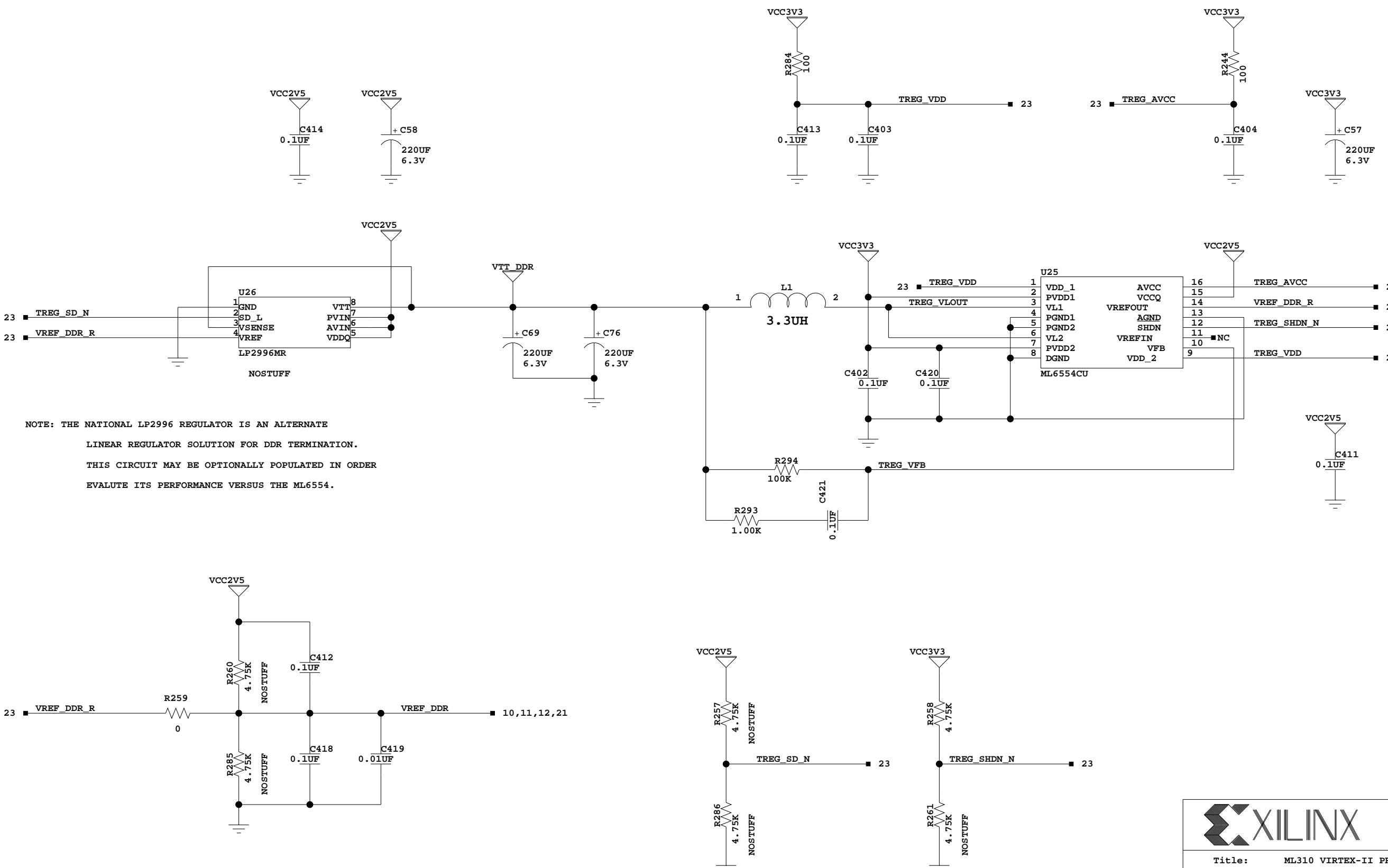
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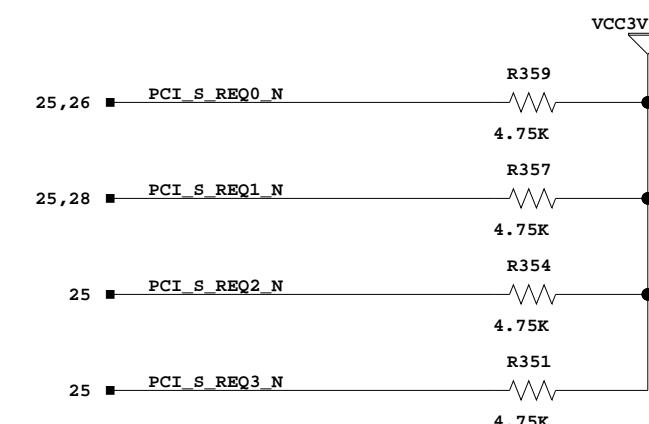
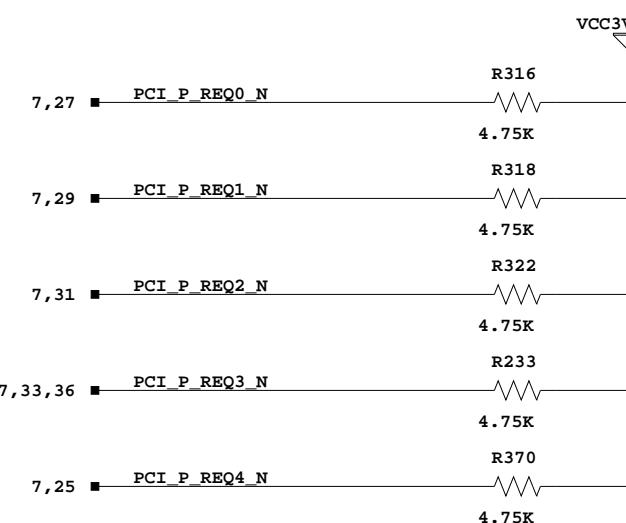
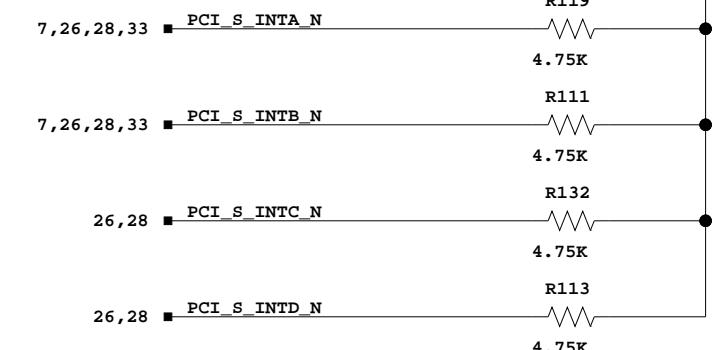
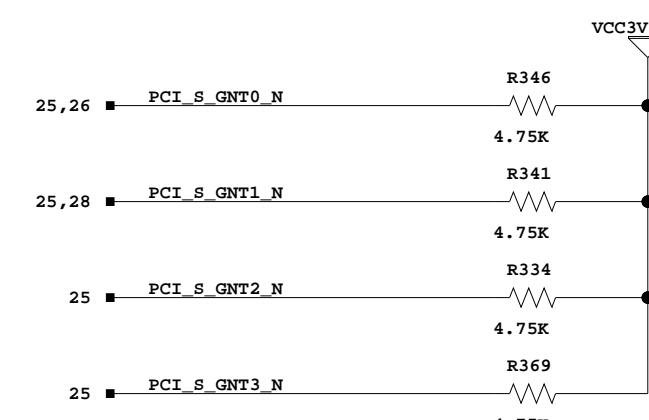
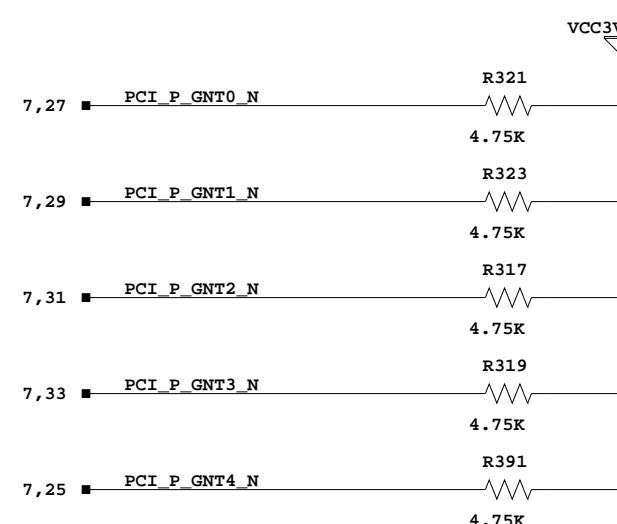
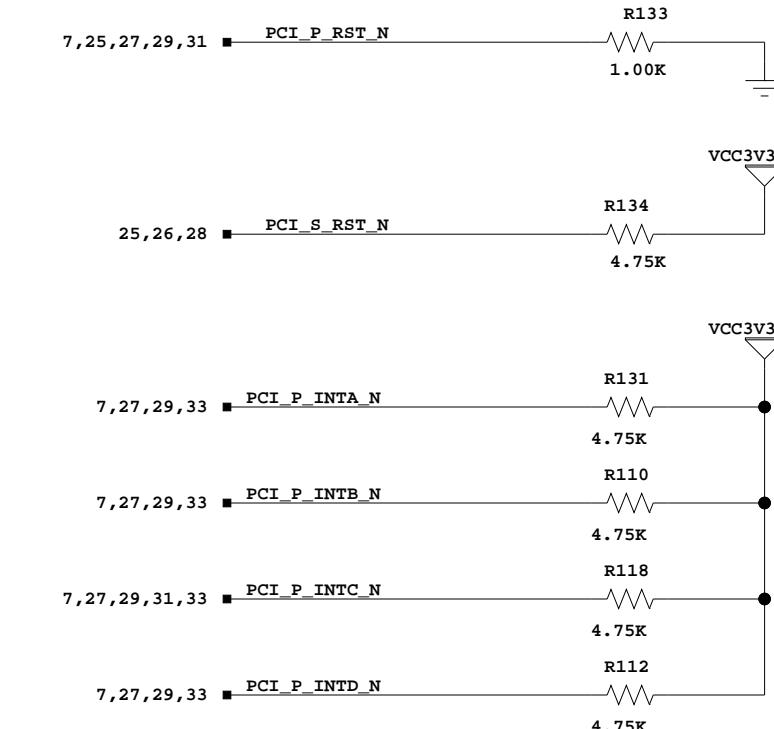
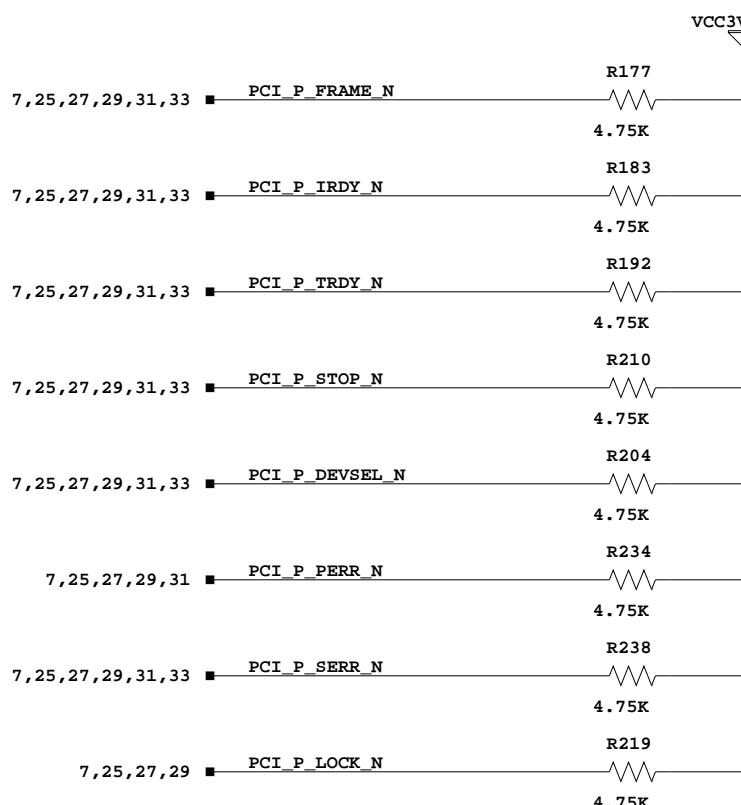
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A

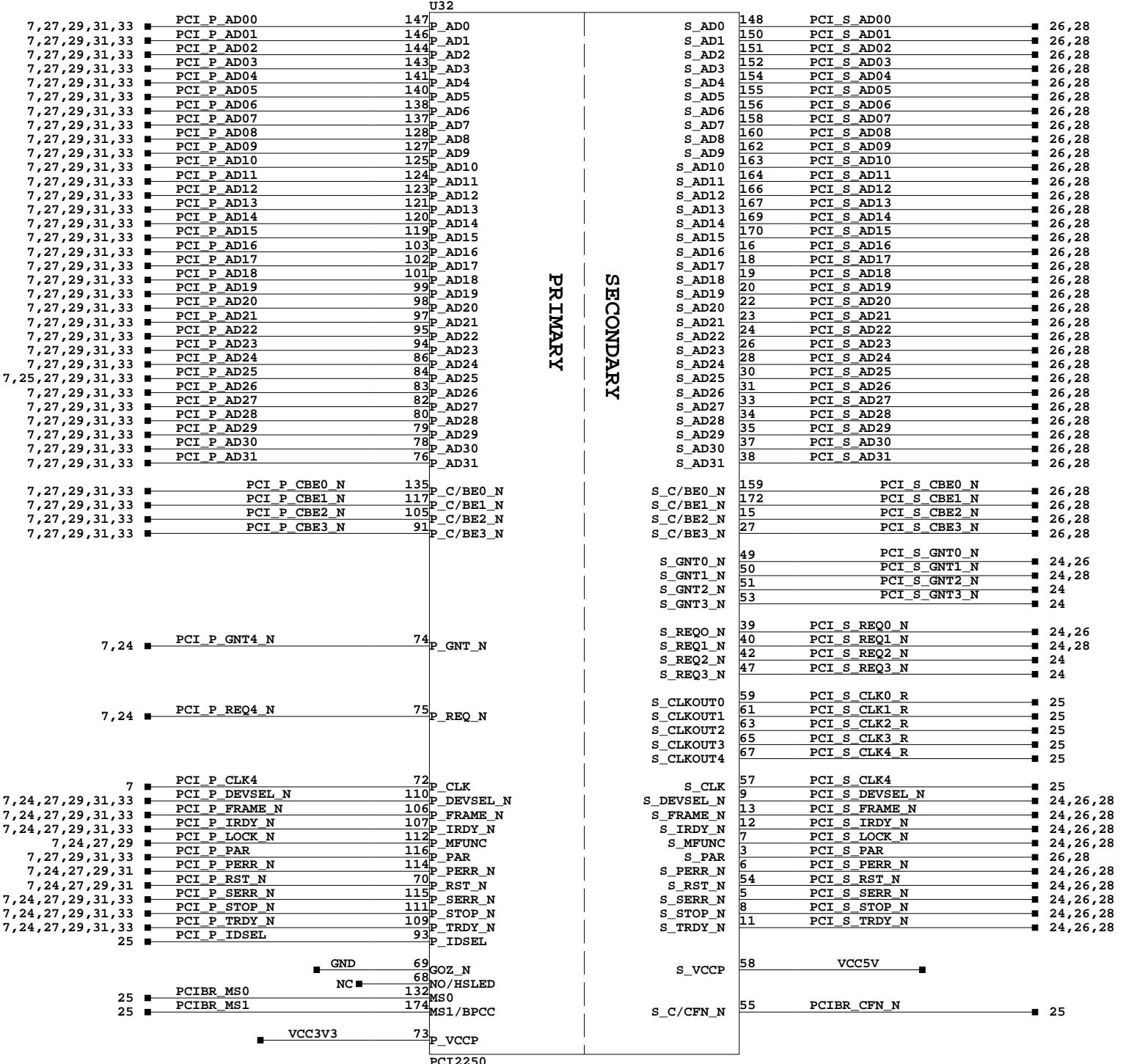
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XILINX	SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
DDR SSTL-2 TERMINATION	
Date: 1-5-2004_13:05	Ver: X.X
Sheet Size: B	Rev: X
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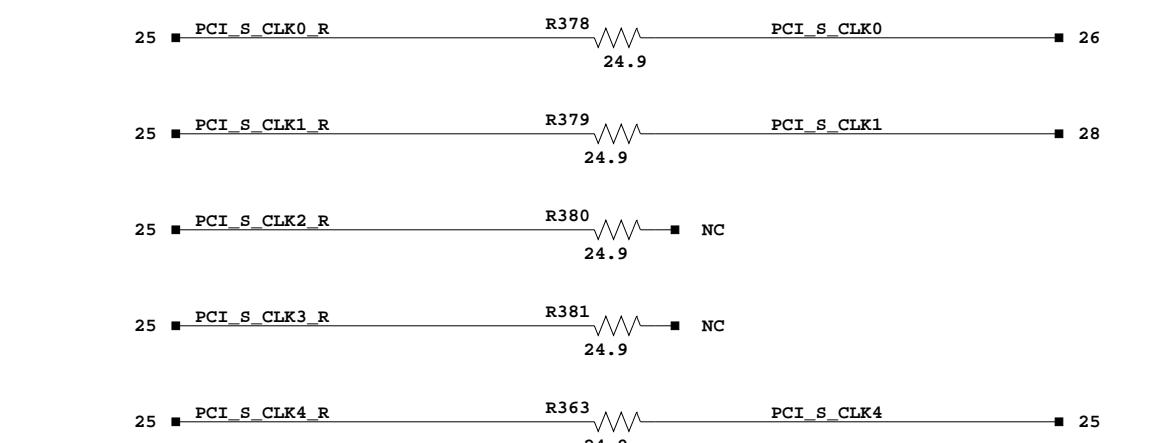
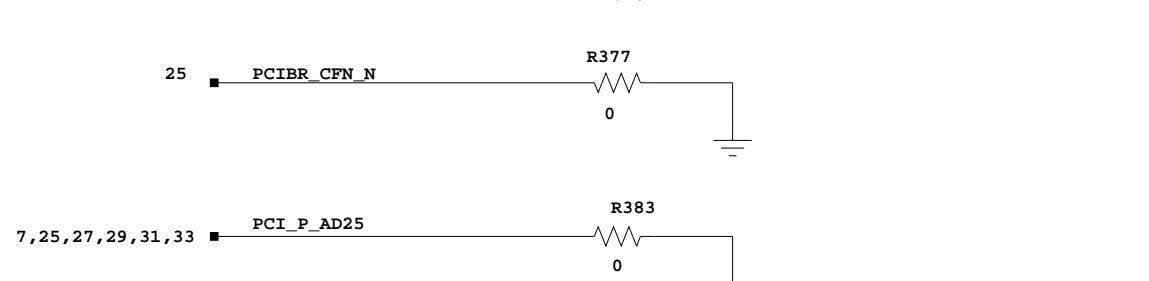
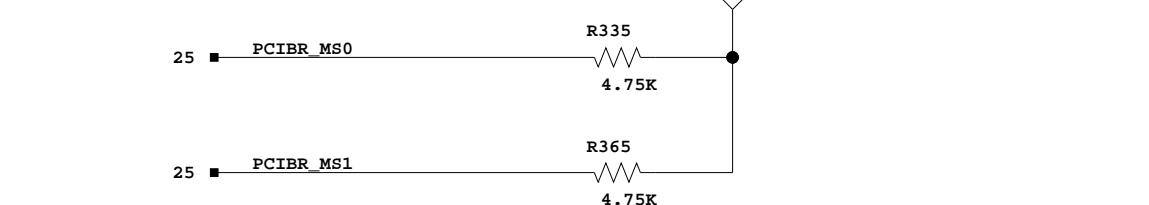
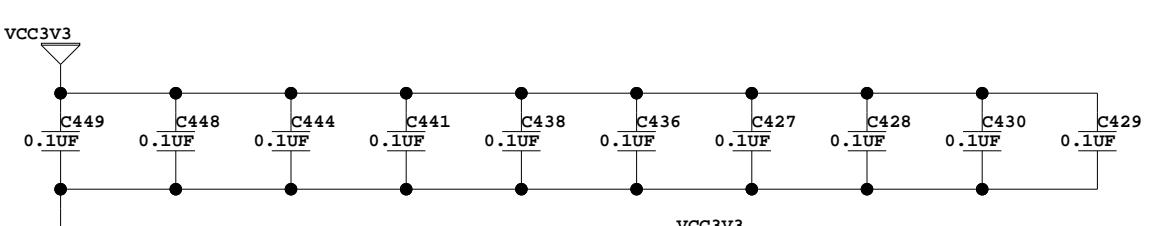
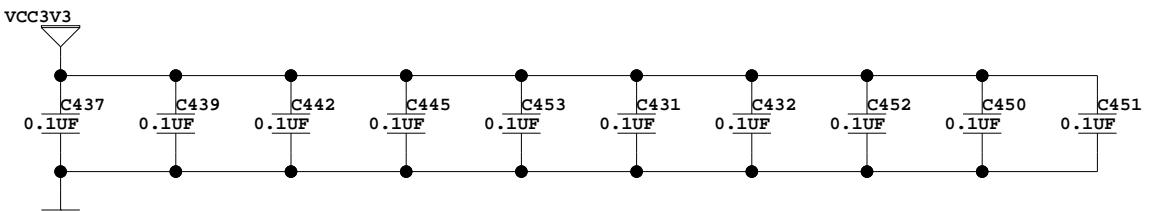


PCI-PCI BRIDGE
PCI2250_PGF

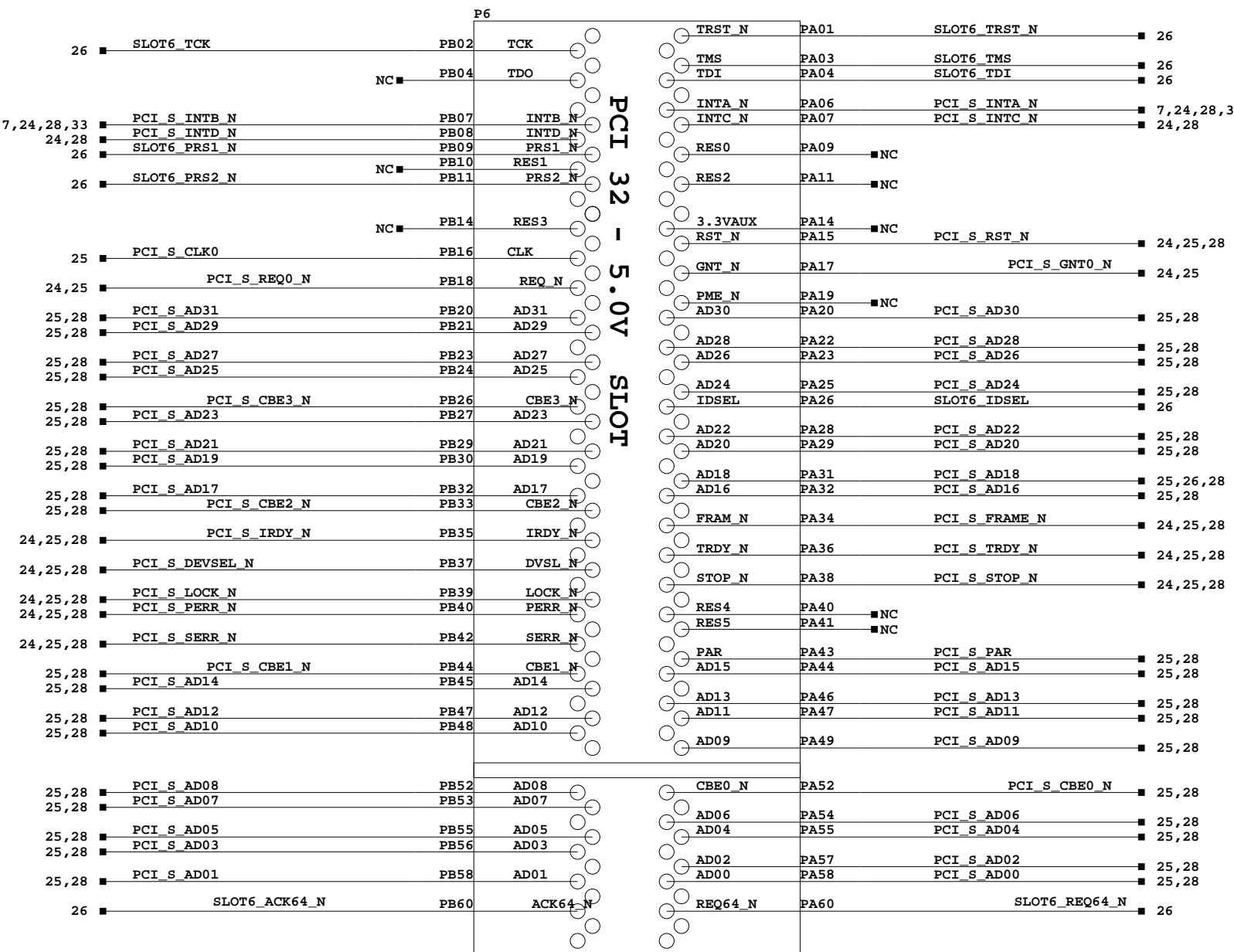


VCC3V3;10,17,25,32,44,52,62,66,81,88,100
VCC3V3;108,118,126,139,145,153,161,168,176

GND;1,14,21,29,36,45,56,60,64,71,77,89
GND;96,104,113,122,130,133,142,149,157,165,171
NC=2,4,41,43,46,48,85,87,90,92,129,131,134,136,173,175



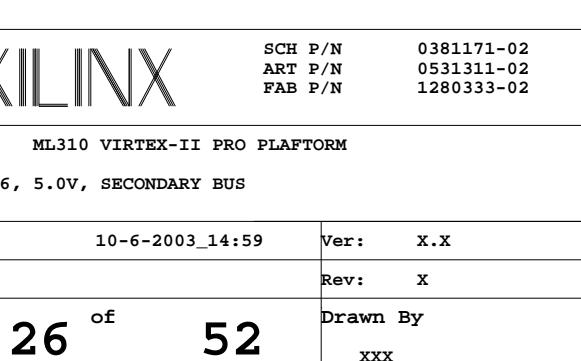
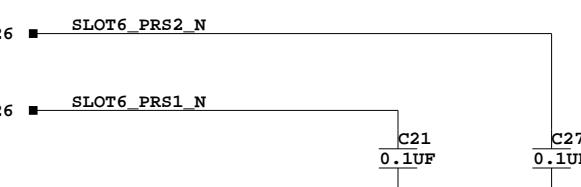
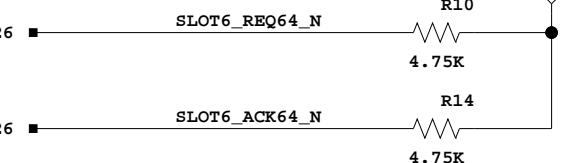
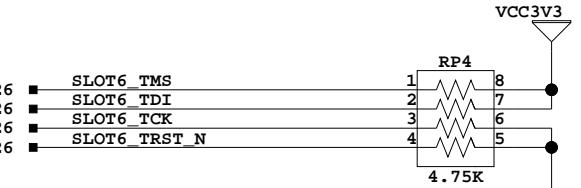
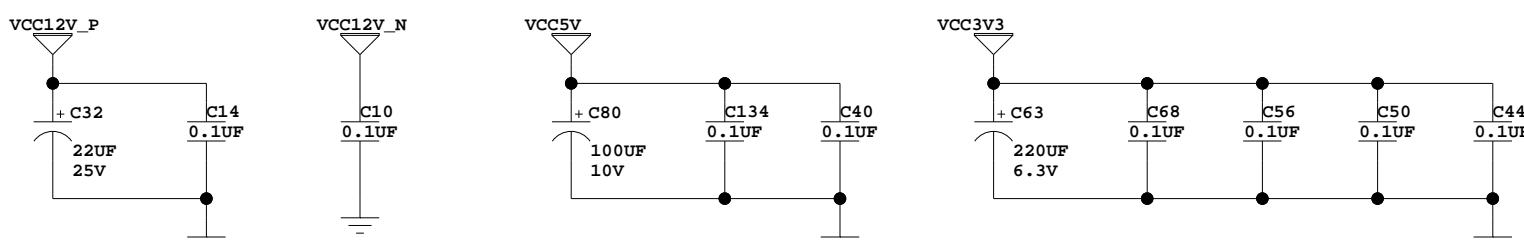
XILINX	SCH P/N 0381171-02
ART P/N 0531311-02	
FAB P/N 1280333-02	
Title: ML310 VIRTEX-II PRO PLATFROM	
PCI-PCI BRIDGE	
Date: 10-6-2003_14:59 Ver: X.X	
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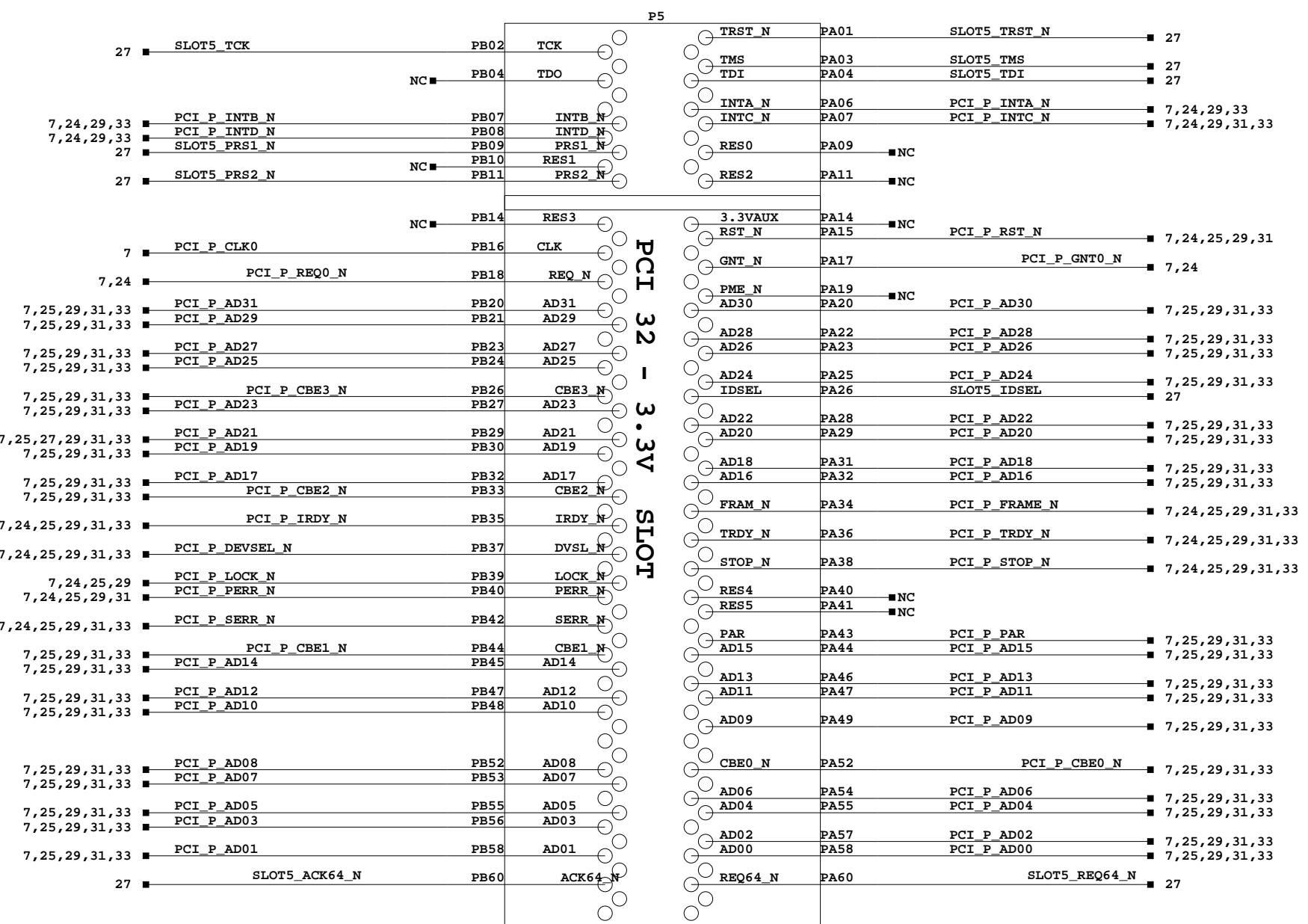


VCC12V_P; PA02
VCC12V_N; PB01
VCC5V; FA05, PB05, PB06, PA08
VCC5V; PA61, PB61, PA62, PB62
VCC3V3; PA21, PB25, PA27, PB31, PA33, PB36
VCC3V3; PA39, PB41, PB43, PA45, PA53, PB54

VCCIO VCC5V; PA10, PA16, PB19, PB59, PA59

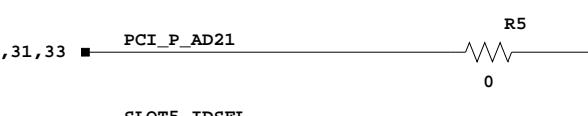
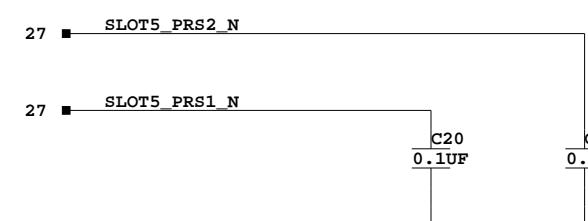
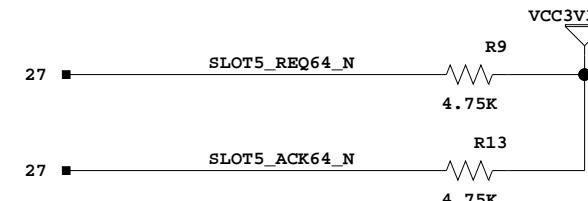
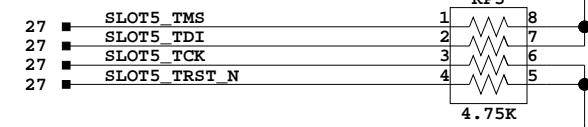
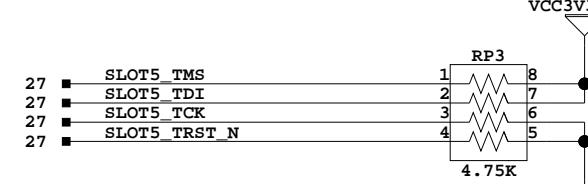
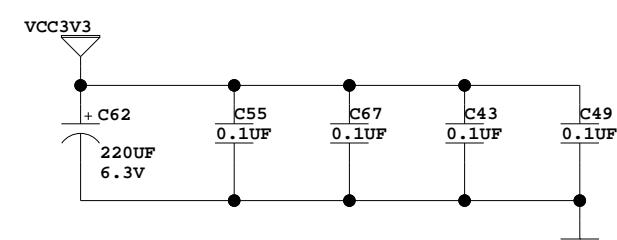
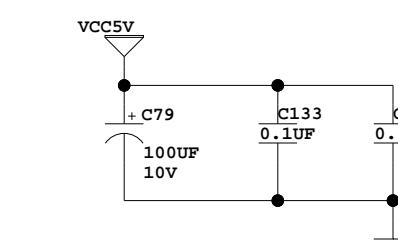
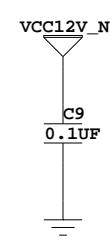
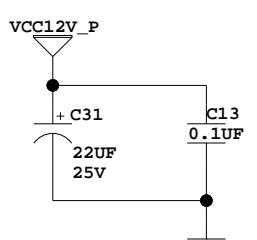
GND; PB03, PB15, PB17, PA18, PB22, PA24
GND; PB28, PA30, PB34, PA35, PA37, PB38
GND; PA42, PB46, PA48, PB49, PA56, PB57
GND; PB12, PA12, PB13, PA13





VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

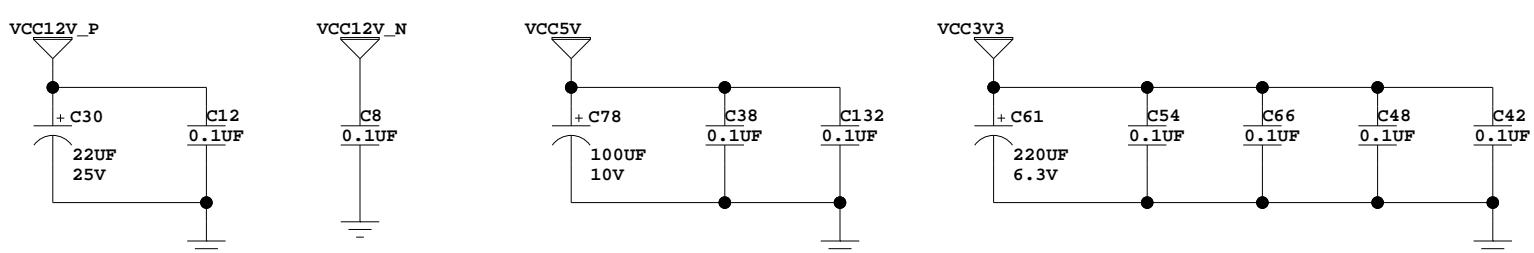
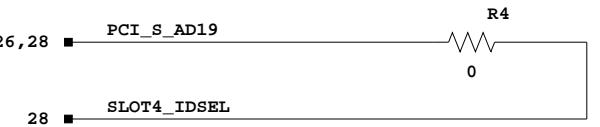
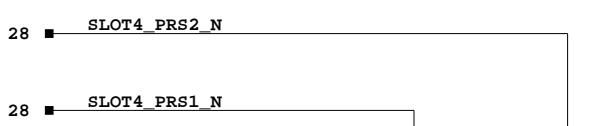
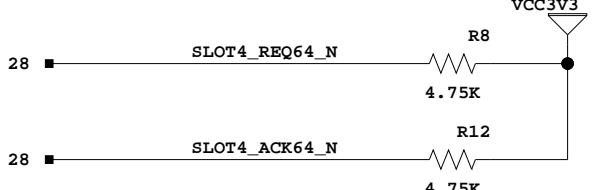
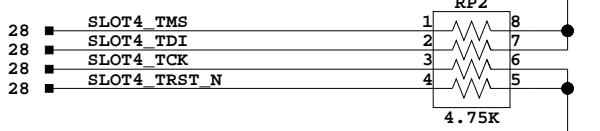
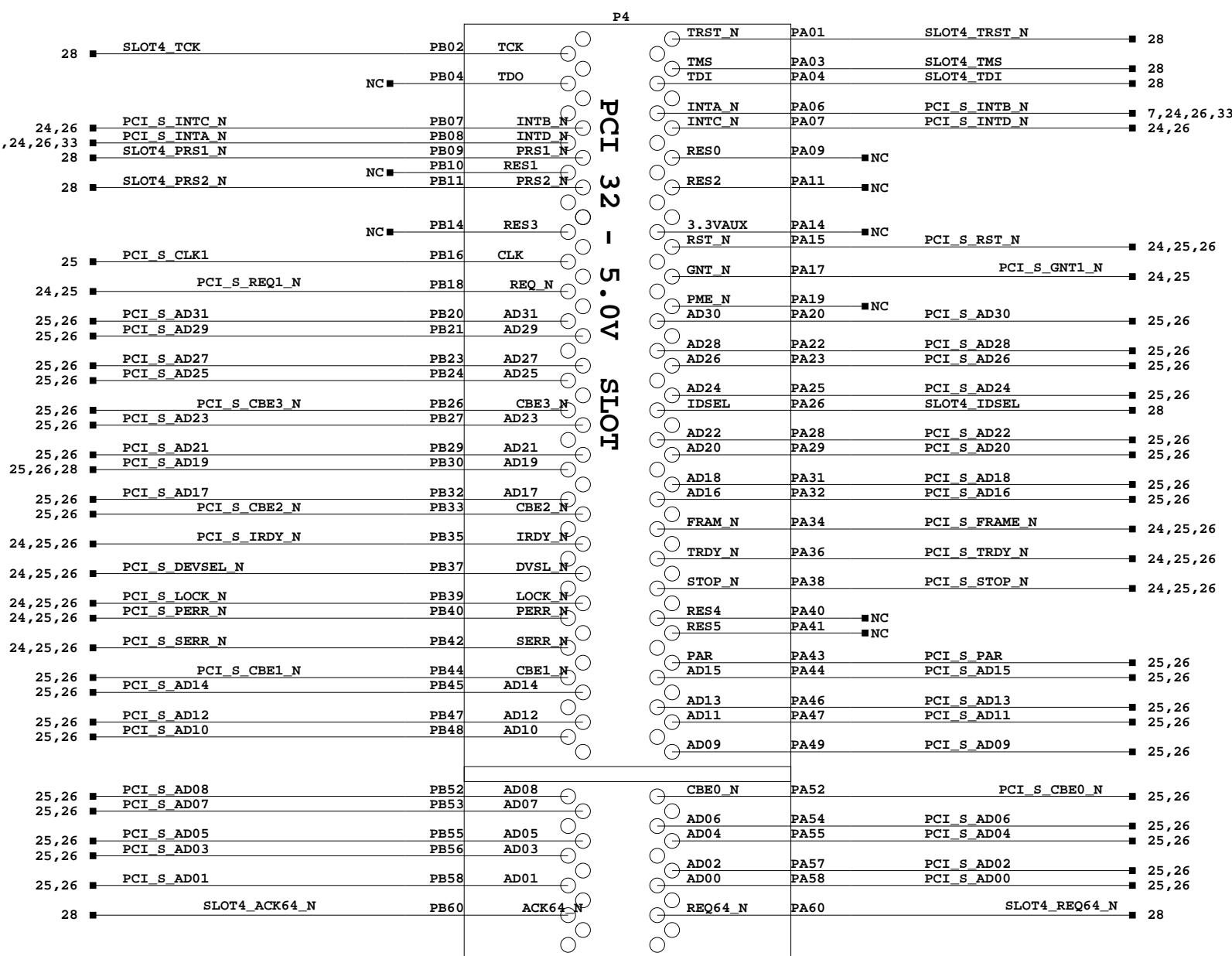
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GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB50,PA50,PB51,PA51



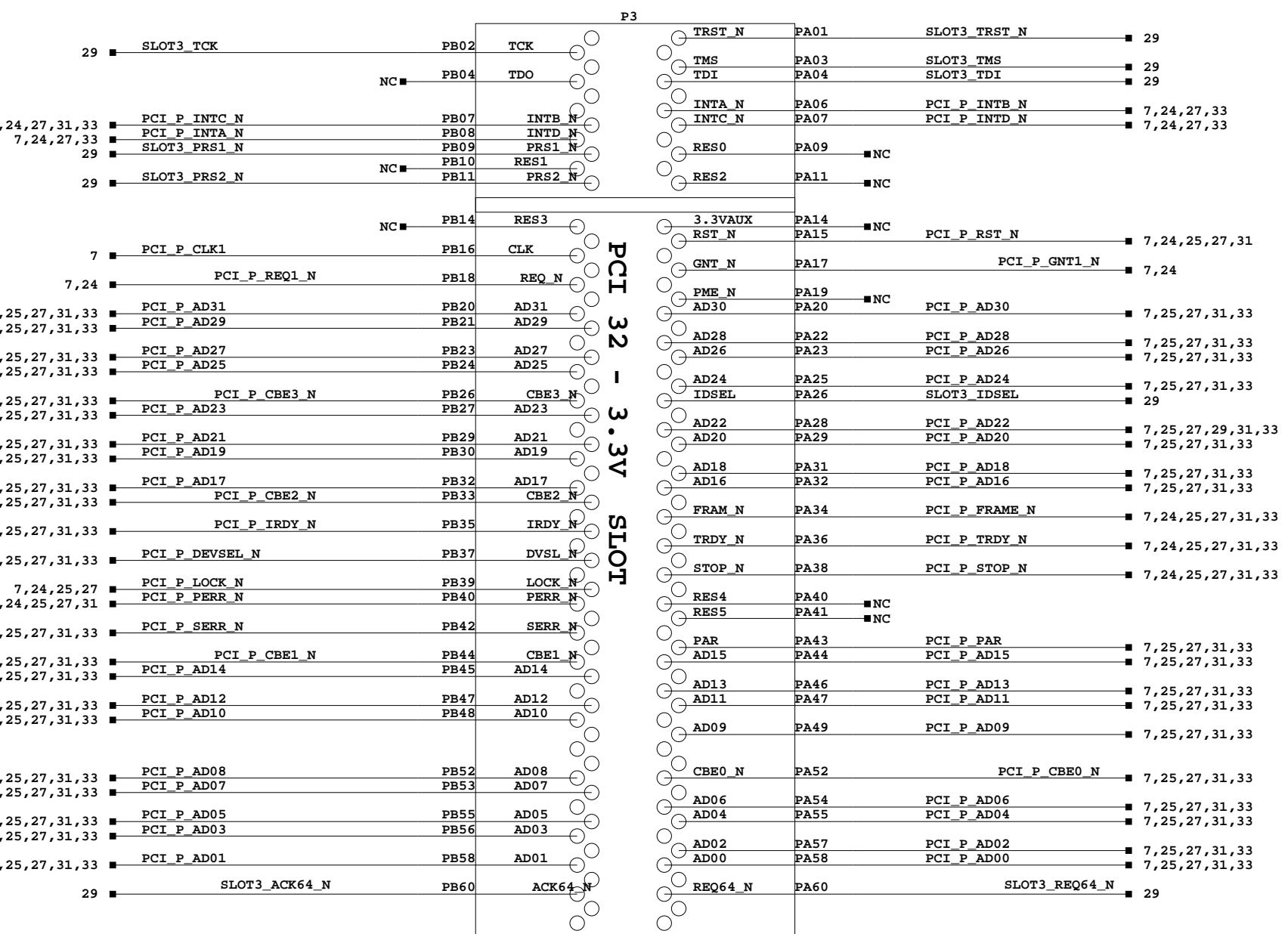
7,25,27,29,31,33 ■ PCI_P_AD21 0 R5

27 ■ SLOT5_IDSEL 0

XILINX	SCH P/N 0381171-02
	ART P/N 0531311-02
	FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
PCI SLOT 5, 3.3V, PRIMARY BUS	
Date: 10-6-2003_14:59	Ver: X.X
Sheet Size: B	Rev: X
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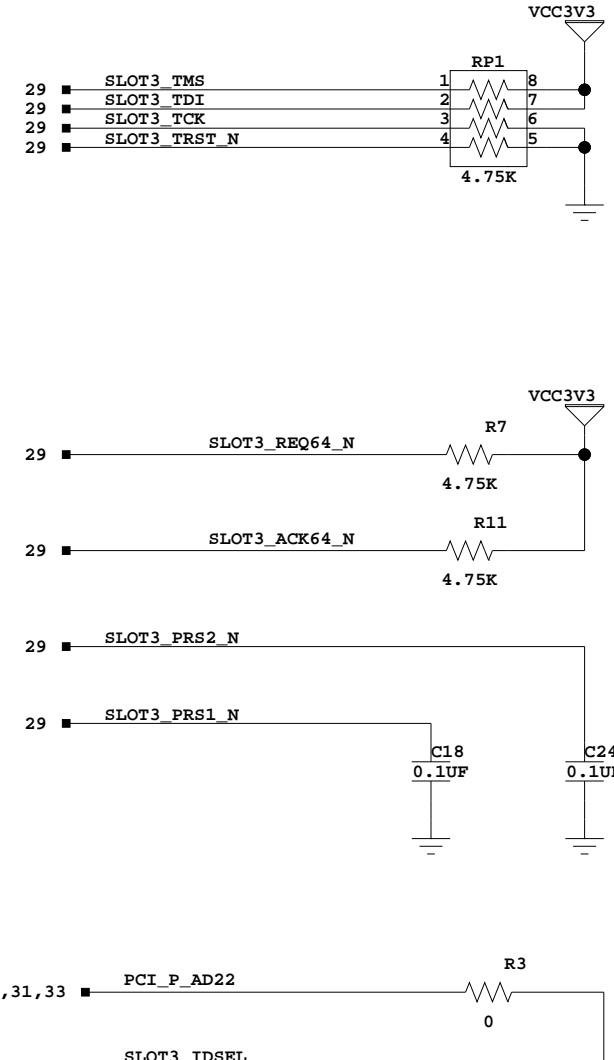
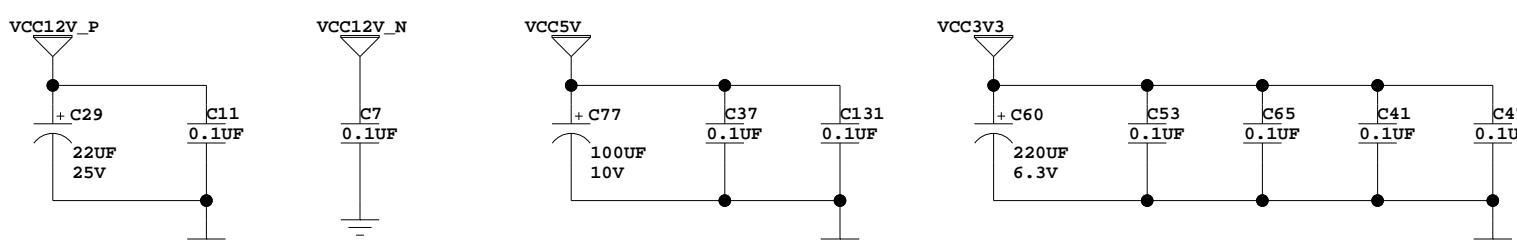
XILINX		SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM PCI SLOT 4, 5.0V, SECONDARY BUS		
Date:	10-6-2003_14:59	Ver: X.X
Sheet Size:	B	Rev: X
Sheet	28 of 52	Drawn By XXX



VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;FA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB50,PA50,PB51,PA51



XILINX		SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM PCI SLOT 3, 3.3V, PRIMARY BUS		
Date:	10-6-2003_14:59	Ver: X.X
Sheet Size:	B	Rev: X
Sheet	29 of 52	Drawn By XXX

D

D

C

C

B

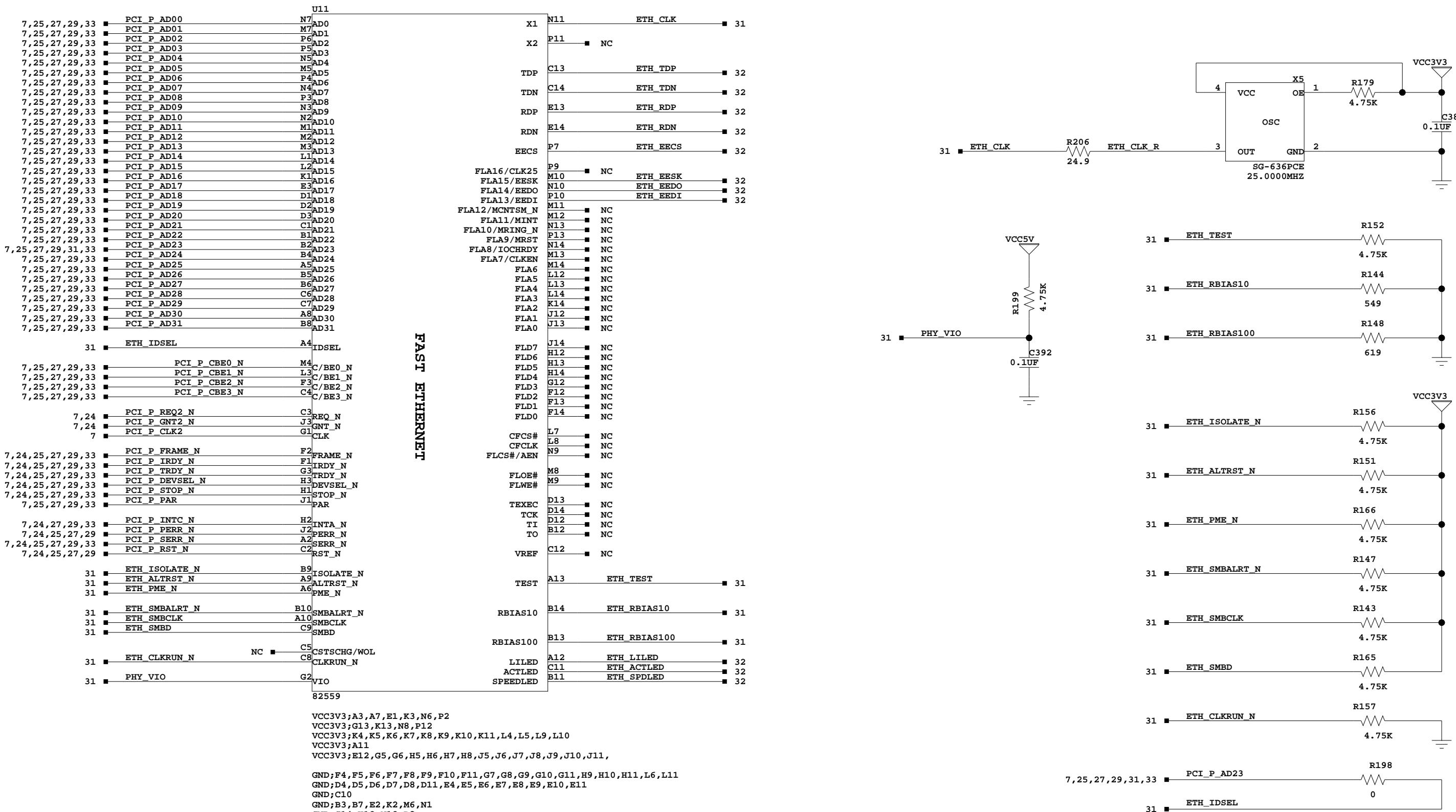
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A

A

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Title: ML310 VIRTEX-II PRO PLATFROM			
<<BLANK>>			
Date:	1-5-2004_13:05	Ver:	X.X
Sheet Size:	B	Rev:	X
Sheet	30	of	52
		Drawn By	xxx



NC=A1,A14,P9,P10,G4,H4,P1,P14



SCH P/N	0381171-02
ART P/N	0531311-02
FAB P/N	1280333-02

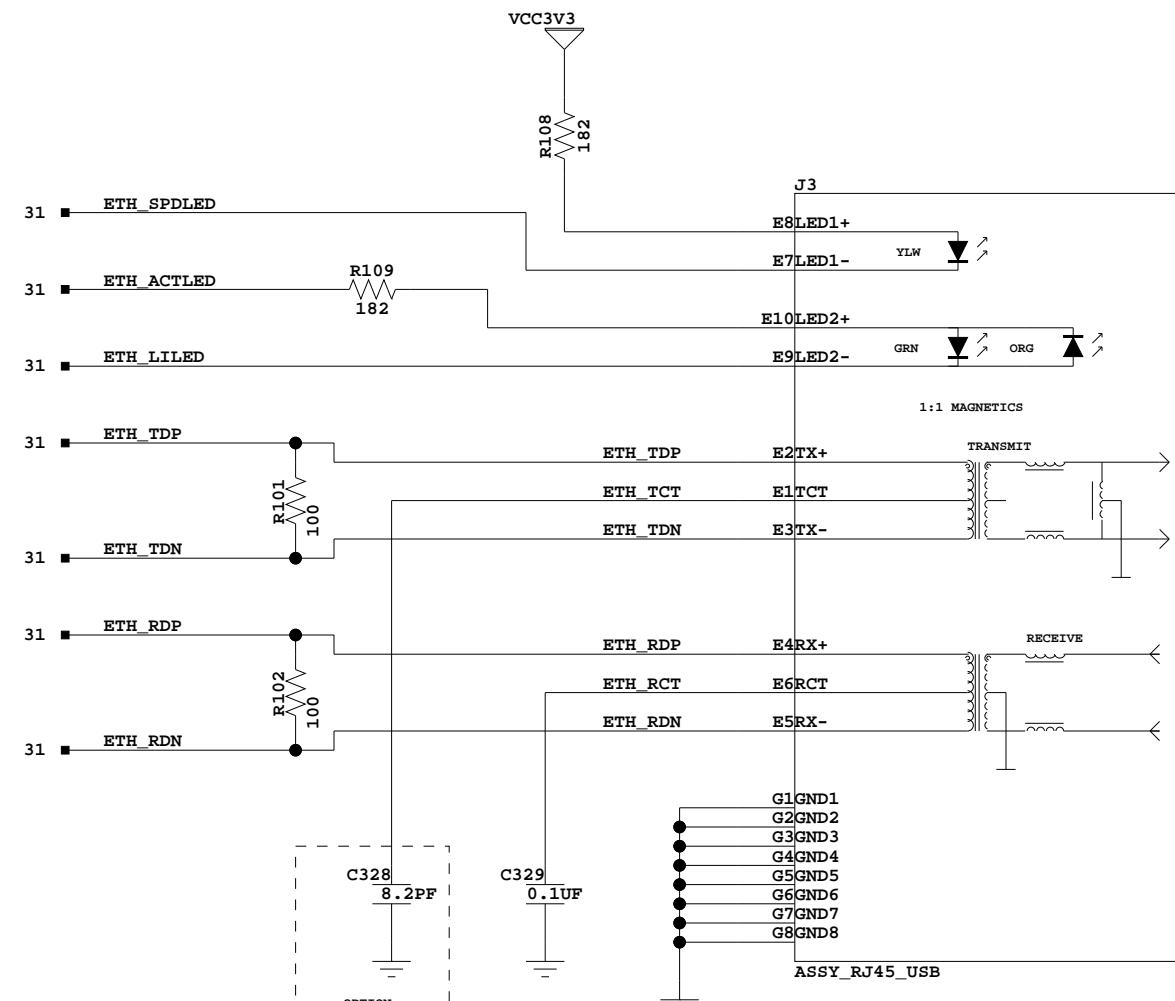
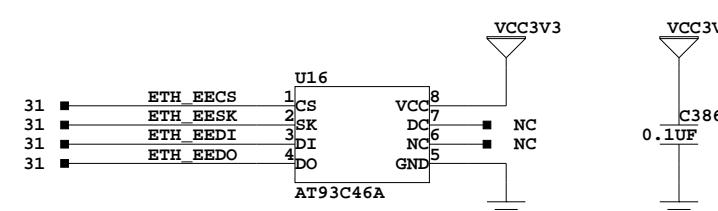
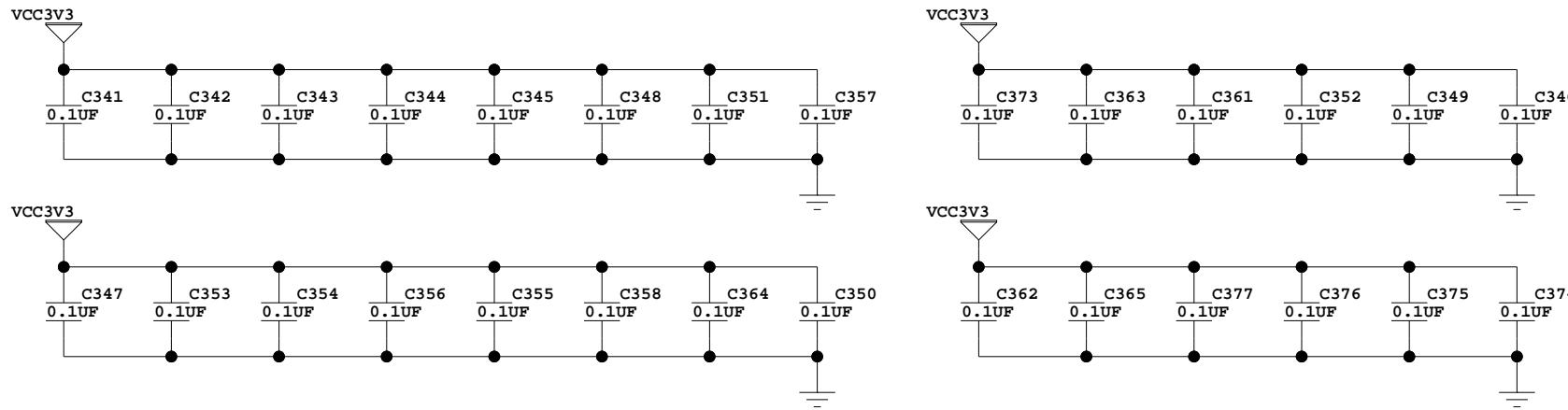
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PCIE ETHERNET MAC/RHY

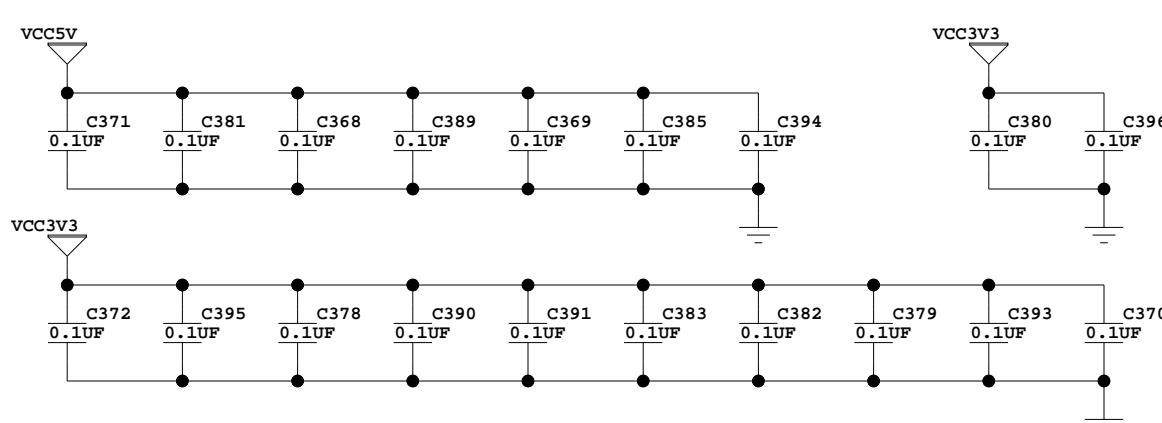
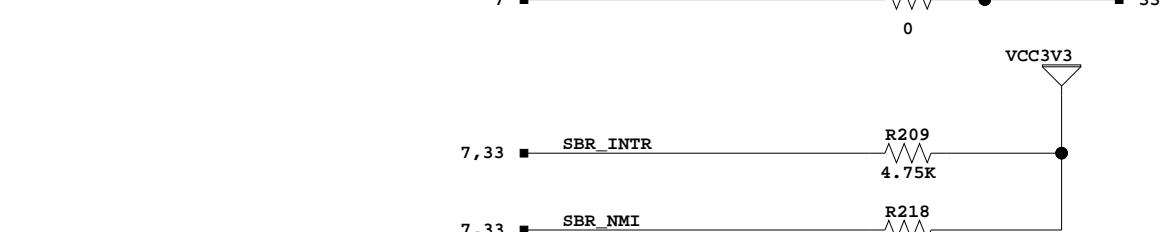
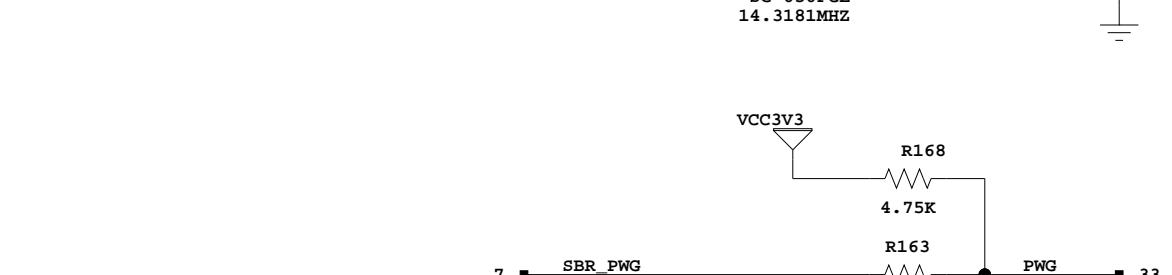
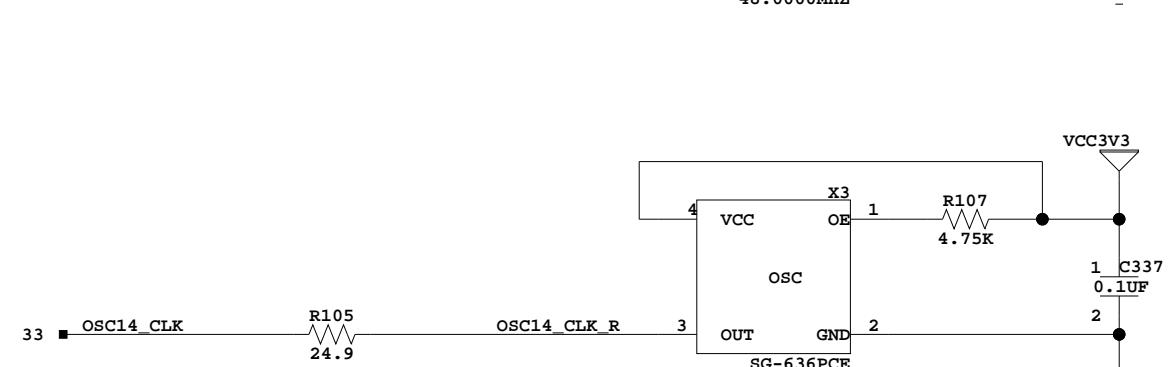
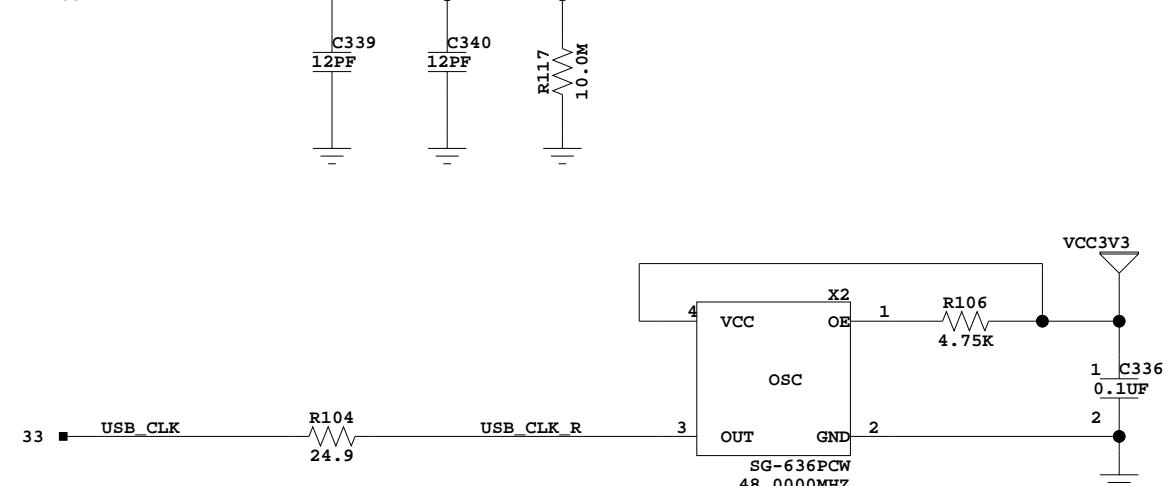
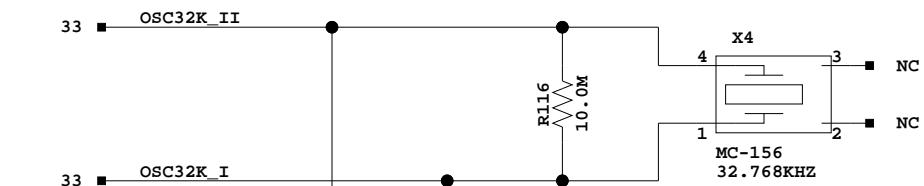
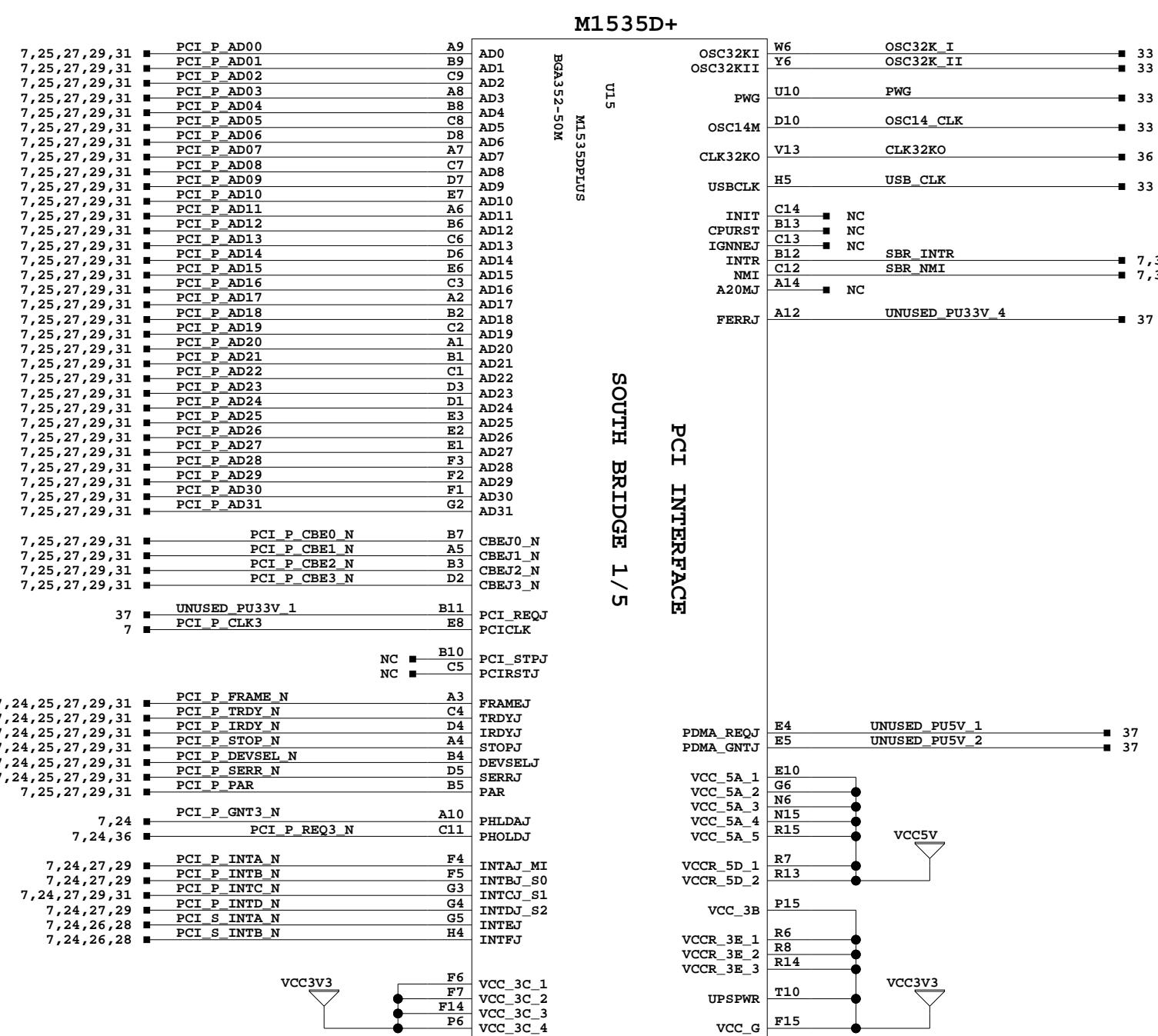
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Drawn By

xxx



	SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
PCI ETHERNET INTERFACE, PROM	
Date:	10-6-2003_14:59
Sheet Size:	B
Sheet	32 of 52 Drawn By xxx



XILINX
SCH P/N 0381171-02
ART P/N 0531311-02
FAB P/N 1280333-02

Title: ML310 VIRTEX-II PRO PLATFROM
PCI SOUTH BRIDGE, PART 1

Date: 10-6-2003_14:59 Ver: X.X
Sheet Size: B Rev: X
Sheet 33 of 52 Drawn By XXX

M1535D+	
STROBJ	PP_STROBE_N_R
AUTOFDJ	PP_AUTOFD_N_R
PDO	PP_DATA0_R
ERRORJ	PP_ERROR_N_R
PDI	PP_INIT_N_R
PRINITJ	PP_DATA2_R
PD2	PP_SLCTIN_N_R
SLCTINJ	PP_DATA3_R
PD3	PP_DATA4_R
PD4	PP_DATA5_R
PD5	PP_DATA6_R
PD6	PP_DATA7_R
PD7	PP_ACK_N_R
PRNACKJ	PP_BUSY_R
BUSY	PP_PEND_R
PE	PP_SELECT_R
SLCT	SIN1
	UART1_RXD
	J5 UART1_TXD
	H1 UART1_RTS_N
	RTS1J 36,39
	J3 UART1_DTR_N
	DTR1J
	J4 UART1_CTS_N
	CTS1J
	H3 UART1_DSR_N
	DSR1J
	G1 UART1_DCD_N
	DCD1J
	J2 UART1_RI_N
	SIN2
	K4 UART2_RXD
	K2 UART2_TXD
	RTS2J 36,39
	K3 UART2_RTS_N
	L2 UART2_DTR_N
	DTR2J
	K1 UART2_CTS_N
	CTS2J
	K5 UART2_DSR_N
	DSR2J
	J1 UART2_DCD_N
	DCD2J
	L1 UART2_RI_N
	R12J
OVCRJ1	T6 USB1_OVCR_N
OVCRJ0	T5 USB0_OVCR_N
USB_FWENJ	V9 USB_POWER_N
GPIO22	U5 GPIO_23
GPIO23	U6 GPIO_22
USBP0+	W8 USB0_DP_R
USBP0-	V8 USB0_DN_R
USBP1+	U9 USB1_DP_R
USBP1-	Y7 USB1_DN_R
USBP2+	W7 GPIO_34
USBP2-	V7 UNUSED_PD_1
USBP3+	U8 GPIO_36
USBP3-	T8 UNUSED_PD_2
IRRXH	L4 UNUSED_PD_3
IRRX	L3 UNUSED_PD_4
IRTX	M1 NC
KBCLK	U11 KBCLK_R
KBDATA	U12 KBDATA_R
	V12 KBINH 34,47
MSCLK	T11 MSCLK_R
MSDATA	T12 MSDATA_R

U15
PARALLEL PORT
SERIAL
PORT1
PORT2
SERIAL
SERIAL
USB PORTS
KEYBOARD
IRDA
MOUSE

BGA352-50M
ML1535DPLUS

SOUTH BRIDGE 2/5

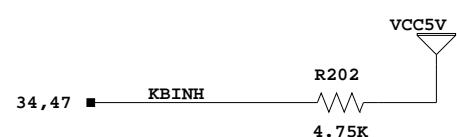
M1535D+

M1535D+	
U15	PIDED0
	PIDED1
	PIDED2
	PIDED3
	PIDED4
	PIDED5
	PIDED6
	PIDED7
	PIDED8
	PIDED9
	PIDED10
	PIDED11
	PIDED12
	PIDED13
	PIDED14
	PIDED15
	PIDEA0
	PIDEA1
	PIDEA2
	SIRQI
	PIDE DRQ
	H18 PIDE DMACK_N_R
	H17 PIDE IORDY_R
	H16 PIDE DIOR_N_R
	G20 PIDE DIOW_N_R
	J17 PIDE CS1_N_R
	J18 PIDE CS3_N_R
	D11 PIDE PDIAG_N_R
	SIDED0
	SIDED1
	SIDED2
	SIDED3
	C15 SIDED4
	A15 SIDED5
	D14 SIDED6
	E13 SIDED7
	D13 SIDED8
	E14 SIDED9
	B15 SIDED10
	D15 SIDED11
	A16 SIDED12
	C16 SIDED13
	E16 SIDED14
	B17 SIDED15
	A19 SIDE A0_R
	C18 SIDE A1_R
	B19 SIDE A2_R
	SIRQII
	SIDERDRQ
	SIDE DAKJ
	SIDERDY
	SIDEIORJ
	D17 SIDE DIOW_N_R
	C19 SIDE CS1_N_R
	A20 SIDE CS3_N_R
	E11 SIDE PDIAG_N_R
	G15
	K16 VCC3V3

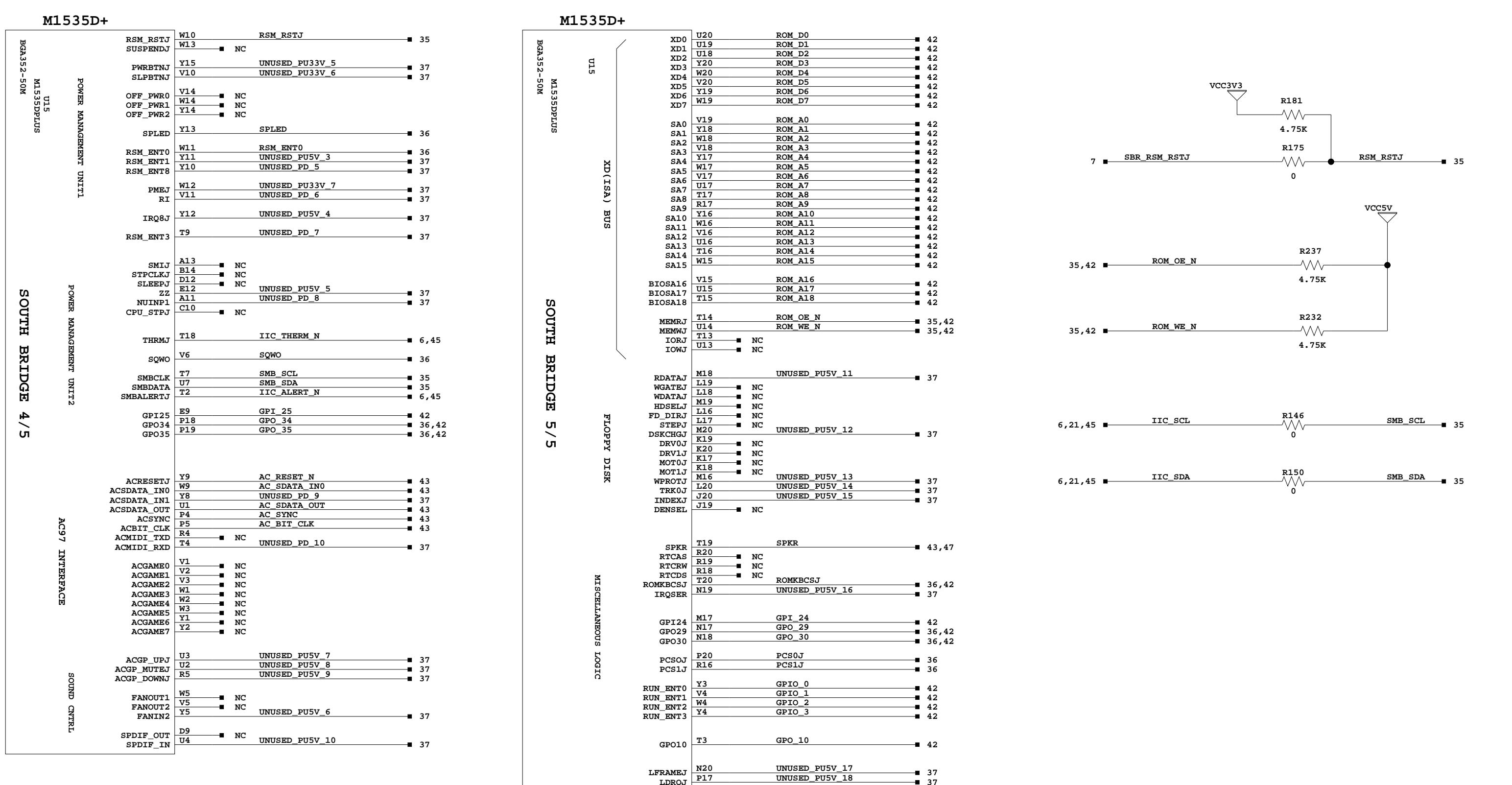
SOUTH BRIDGE 3/5

GROUP F

VCC=3.3V



XILINX	SCH P/N 0381171-02
	ART P/N 0531311-02
	FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
PCI SOUTH BRIDGE, PART 2-3	
Date:	10-6-2003_14:59
Sheet Size:	B
Sheet	34 of 52 Drawn By XXX



CH P/N	0381171-02
RT P/N	0531311-02
AB P/N	1280333-02

title: MI-310 VIRTEX-II PRO BLASTORM

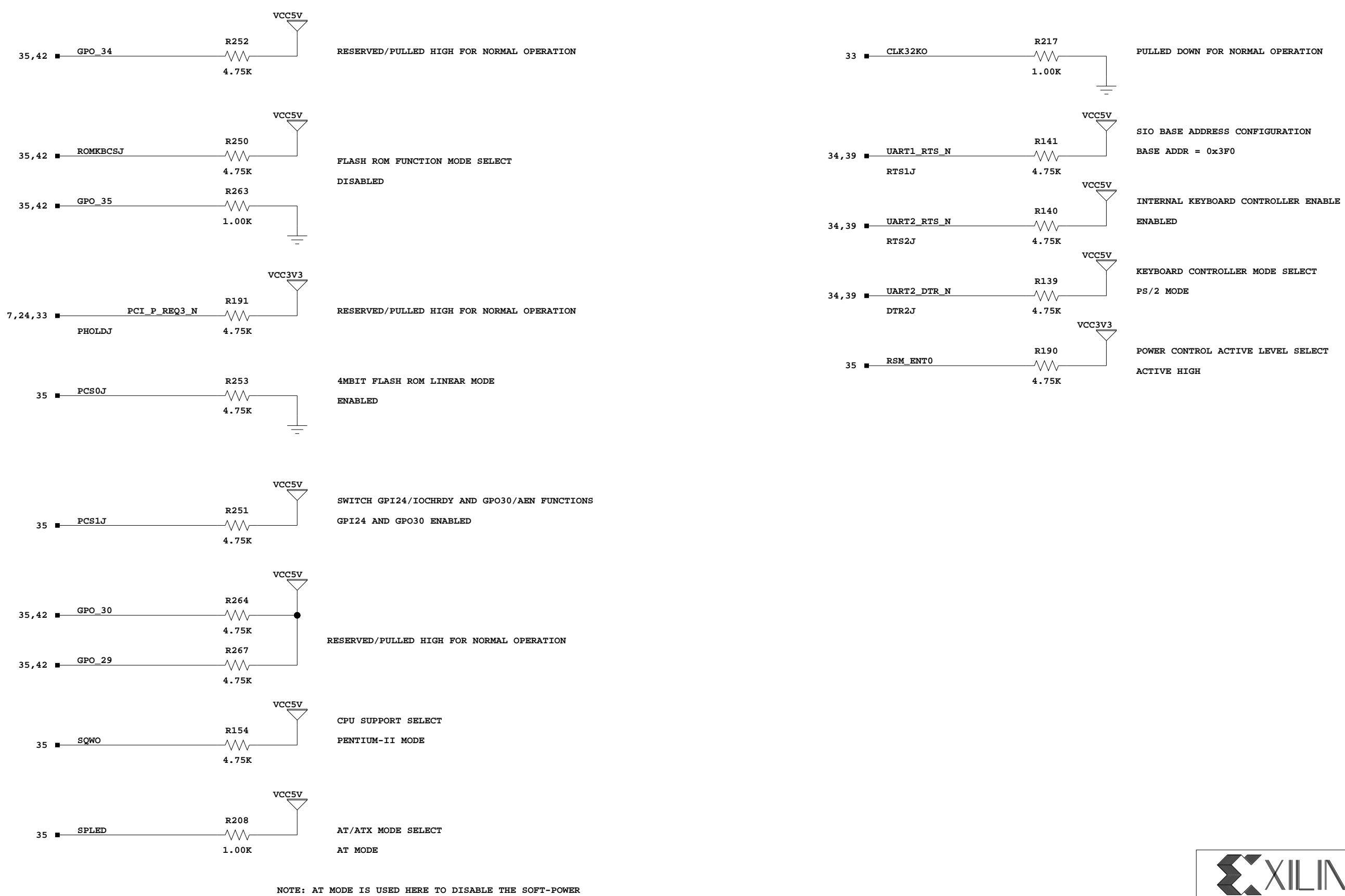
ST. SOUTH BRIDGE - PART 4-5

Page 10 of 10

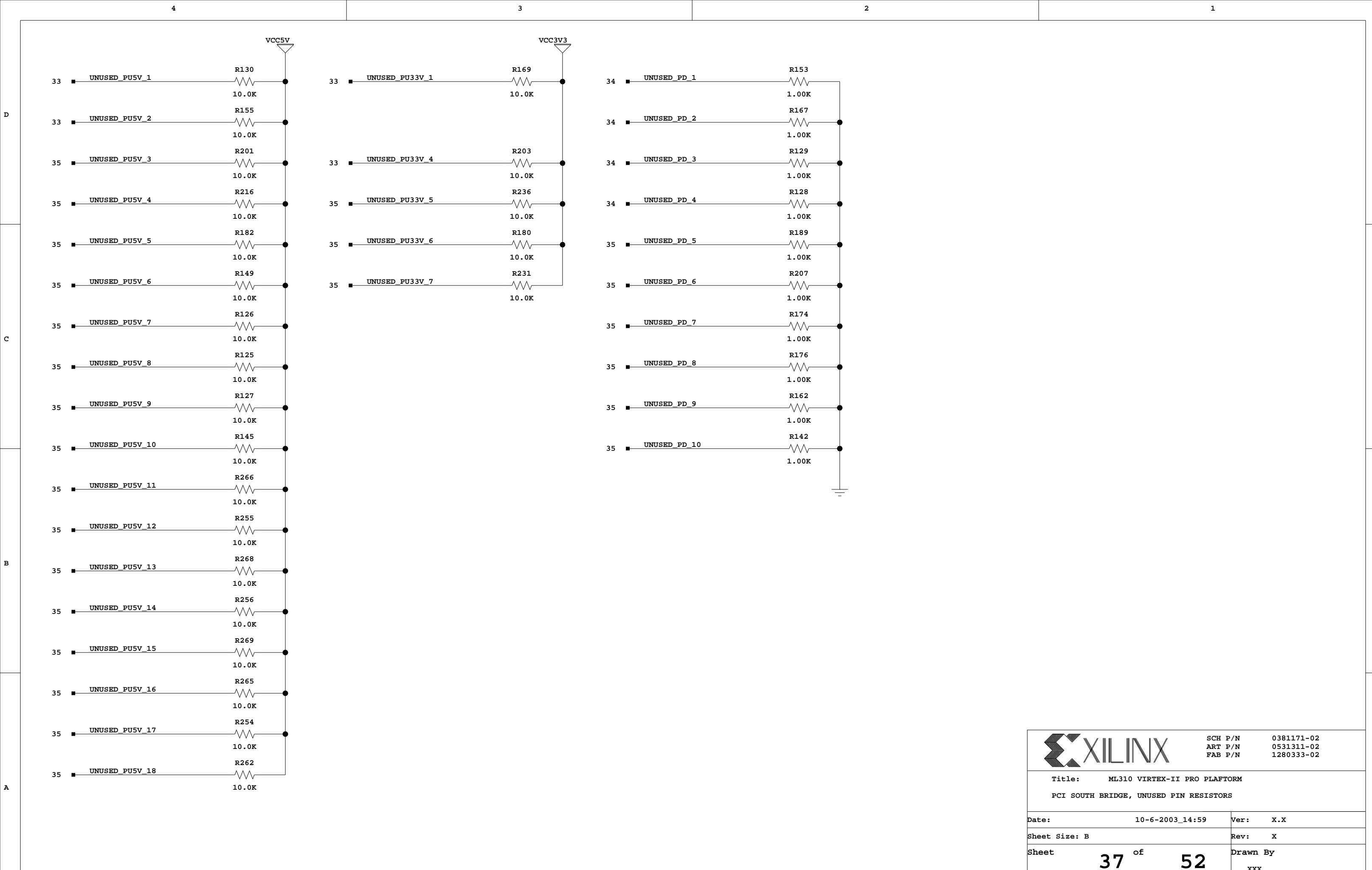
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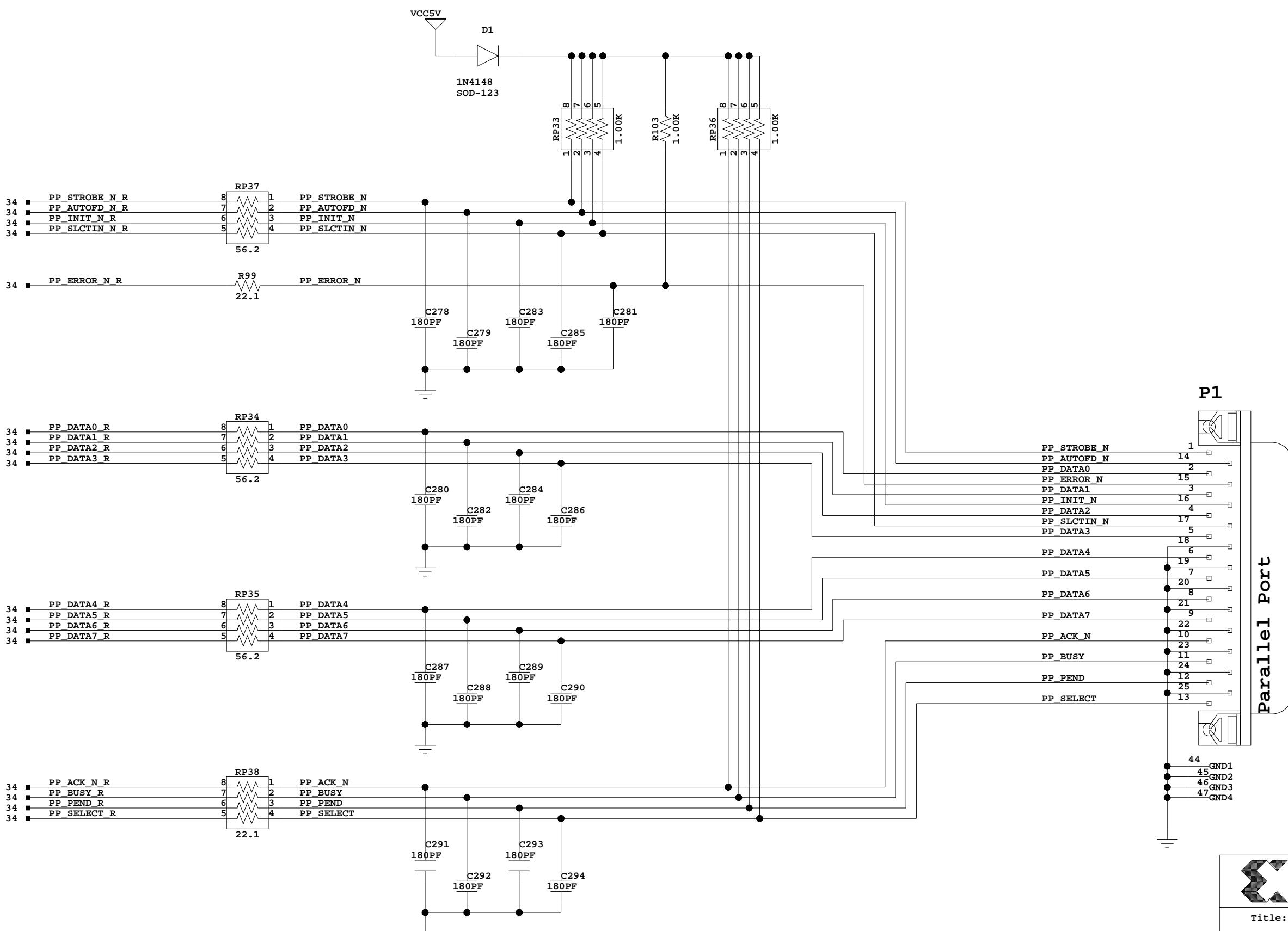
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ART P/N 0531311-02		FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM		
PCI SOUTH BRIDGE, CONFIG RESISTORS		
Date: 10-6-2003_14:59	Ver: X.X	
Sheet Size: B	Rev: X	
Sheet 36 of 52	Drawn By XXX	

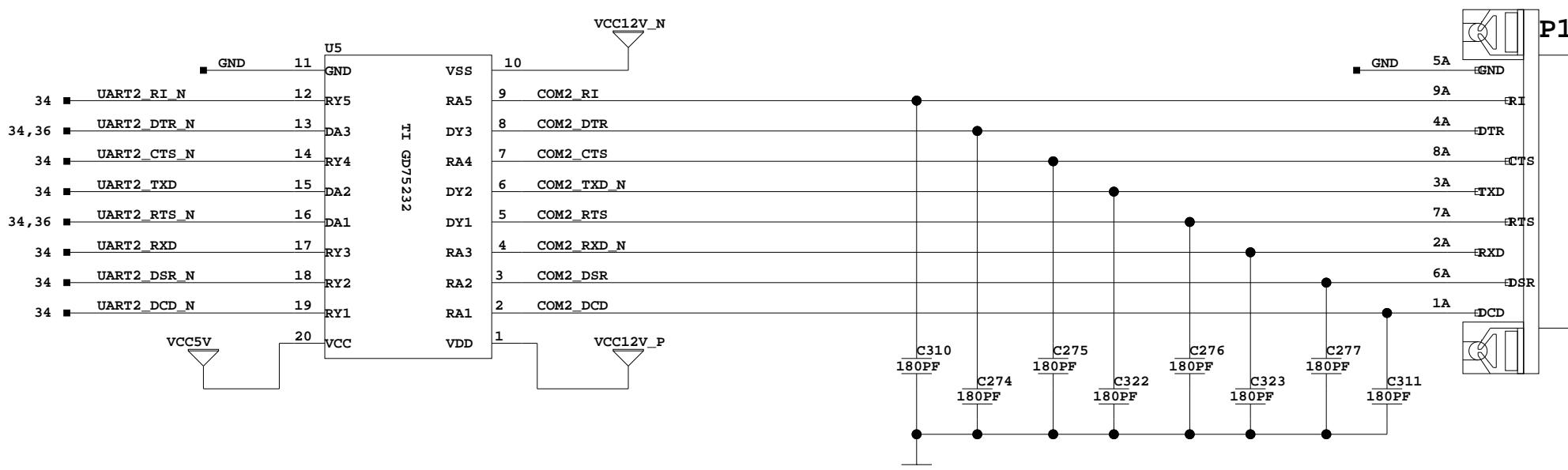
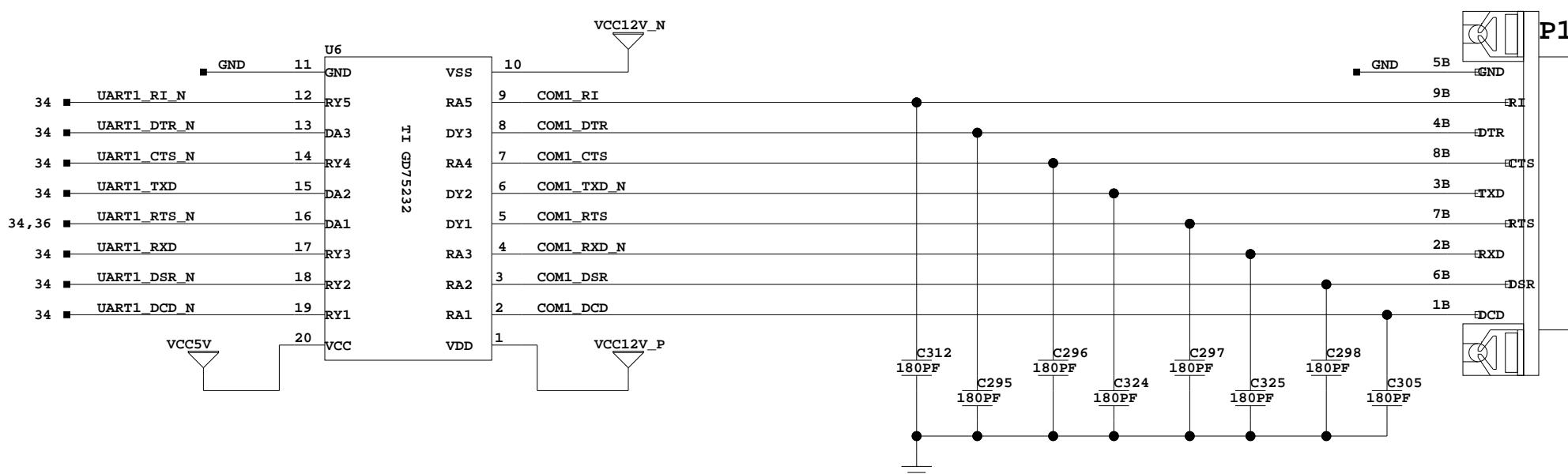


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Title: ML310 VIRTEX-II PRO PLATFROM	
PCI SOUTH BRIDGE, UNUSED PIN RESISTORS	
Date: 10-6-2003_14:59	Ver: X.X
Sheet Size: B	Rev: X
Sheet 37 of 52	Drawn By XXX



XILINX	SCH P/N 0381171-02
	ART P/N 0531311-02
	FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
PARALLEL PORT INTERFACE	
Date: 10-6-2003_14:59	Ver: X.X
Sheet Size: B	Rev: X
Sheet 38 of 52	Drawn By XXX

NOTE: PORT B IS ADJACENT TO THE PS/2 CONNECTOR
WHERE COM1 IS TRADITIONALLY LOCATED. THE
CONNECTOR NAMES ARE MISLEADING.



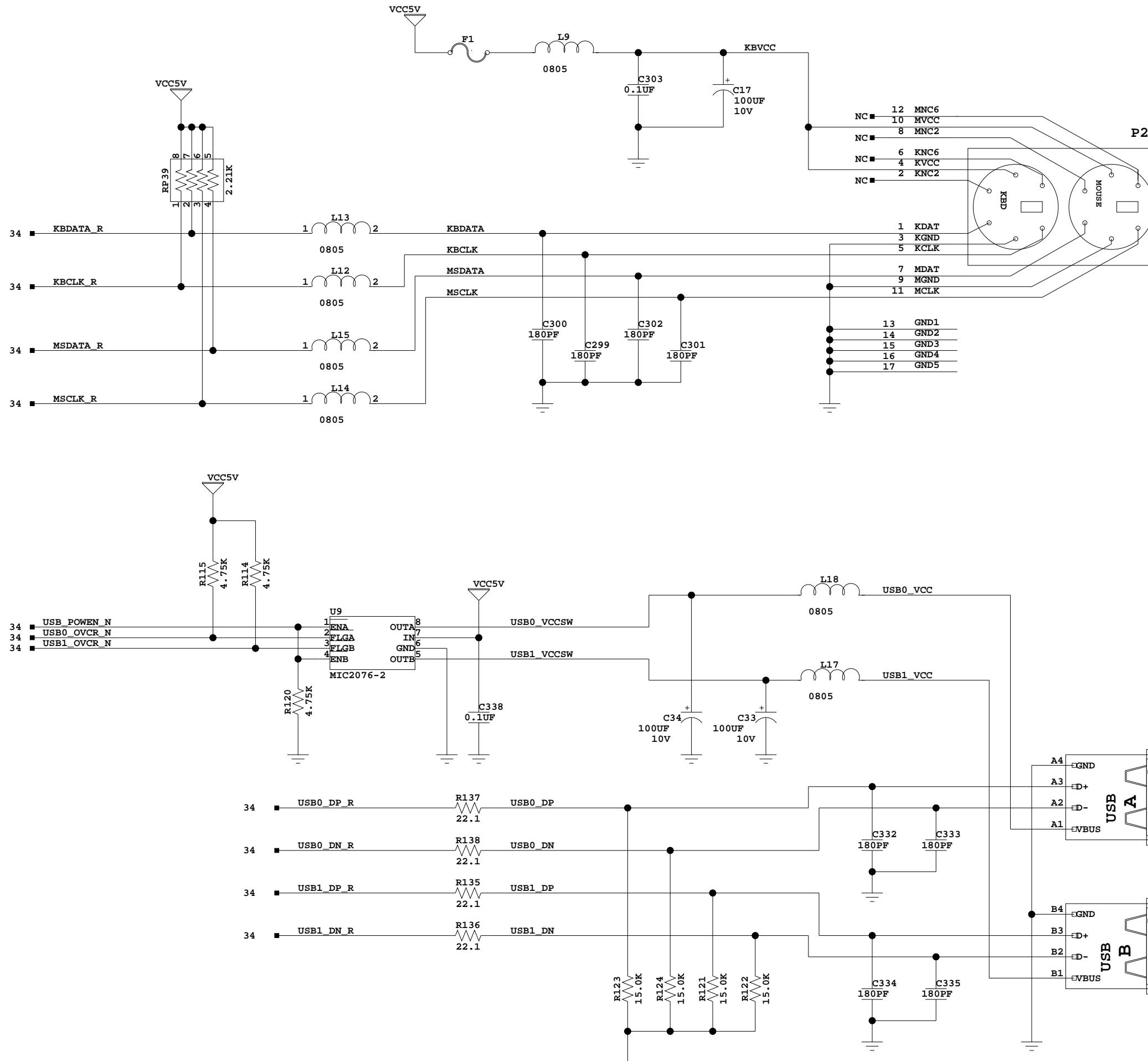
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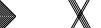
RS232 SERIAL PORT INTERFACE

Date: 1-5-2004_13:05 Ver: X.X

Sheet Size: B Rev: X

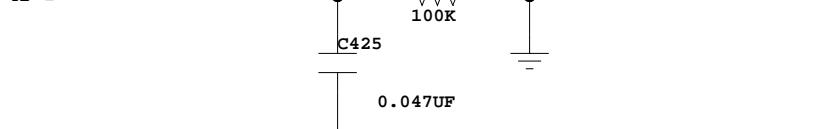
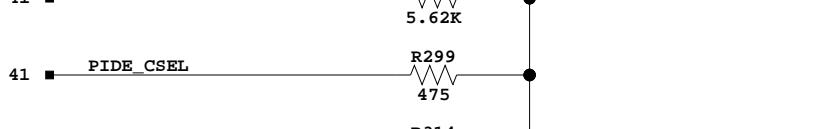
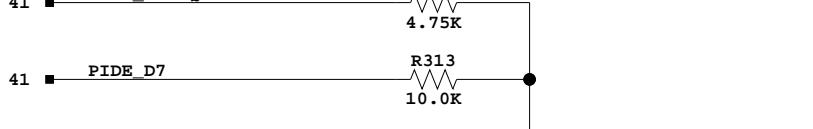
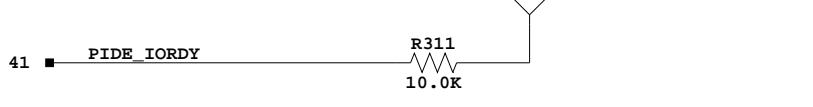
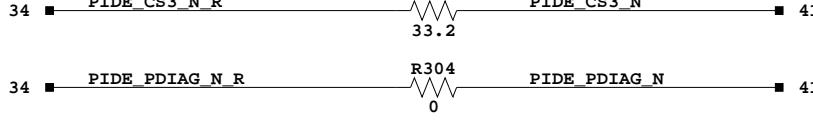
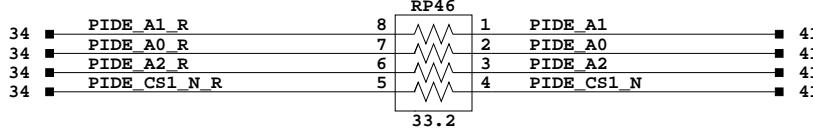
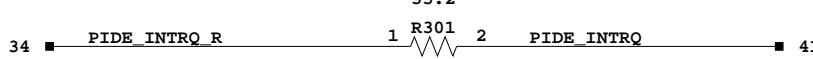
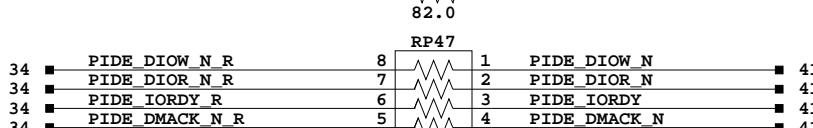
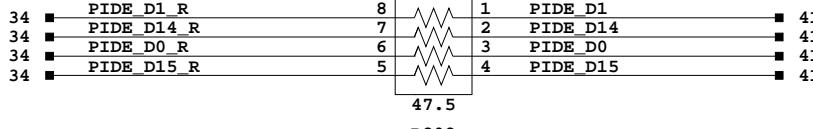
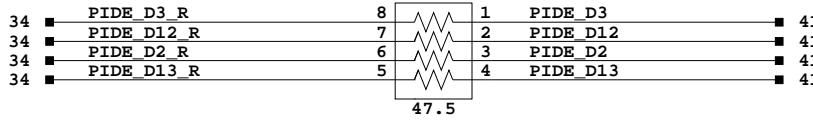
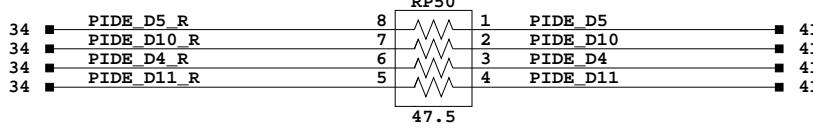
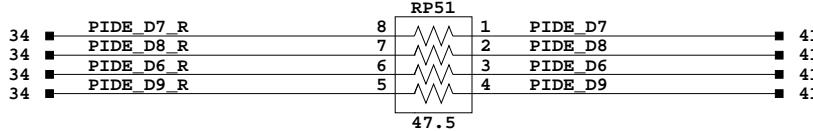
Sheet 39 of 52 Drawn By XXX



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		ART P/N	0531311-02
		FAB P/N	1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM			
KBD/MOUSE AND USB INTERFACES			
Date:	10-6-2003_14:59	Ver:	X.X
Sheet Size: B		Rev:	X
Sheet	of	Drawn By	
40	52	XXX	

Pin 20 must be removed.

Silkscreen:
"IDE PRIMARY"



Mark Pin 1

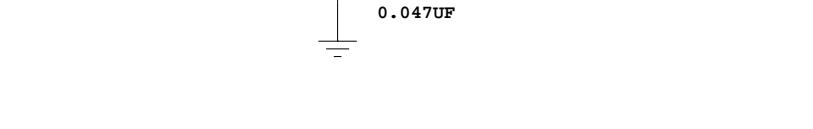
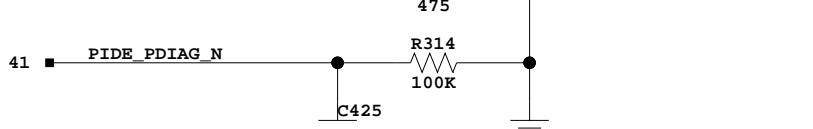
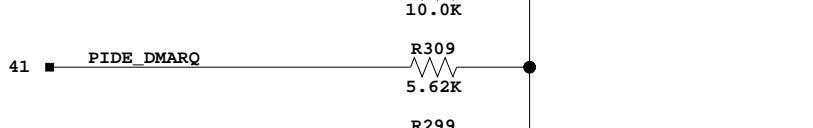
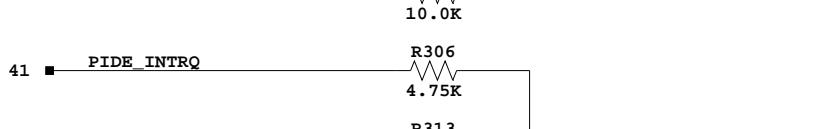
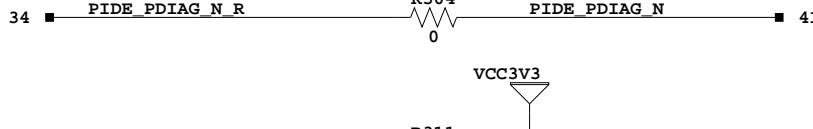
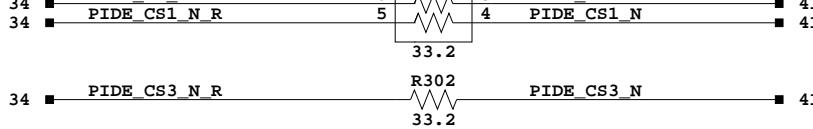
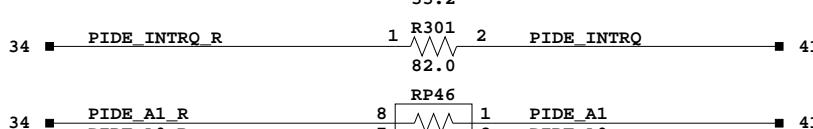
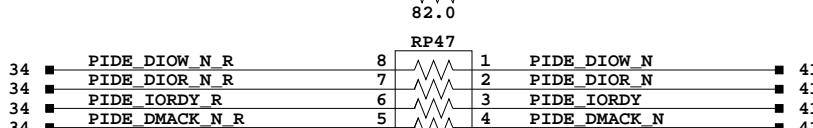
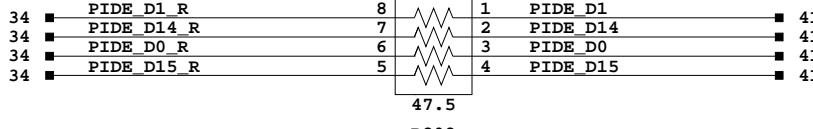
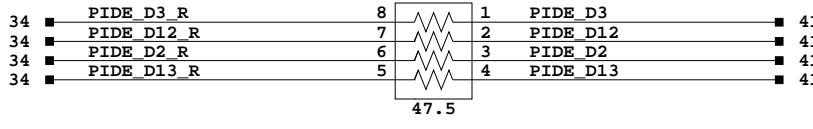
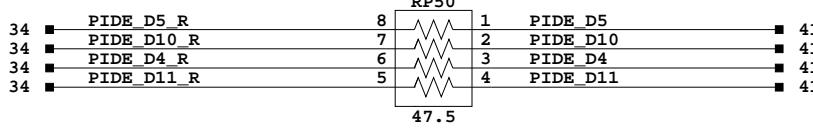
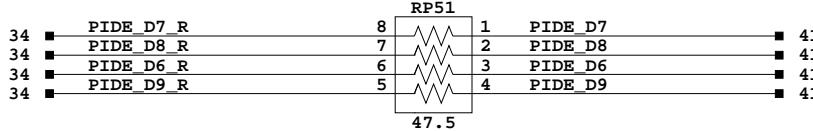
Pin20-Key

J16

IDE PRIMARY CONN

Pin 20 must be removed.

Silkscreen:
"IDE PRIMARY"



Mark Pin 1

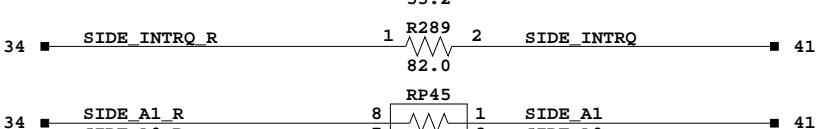
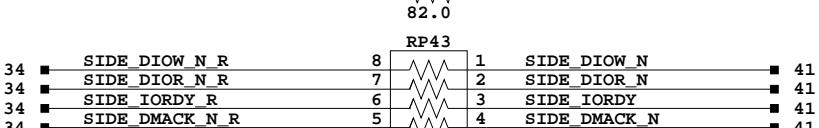
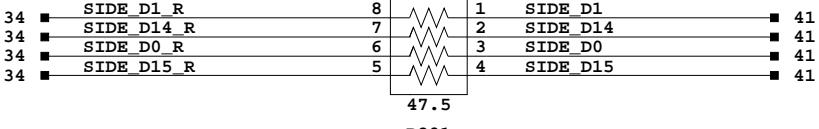
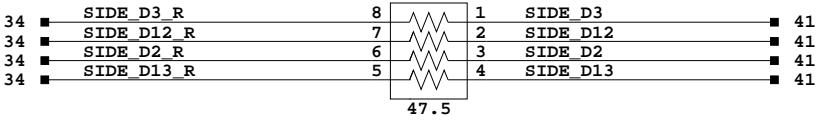
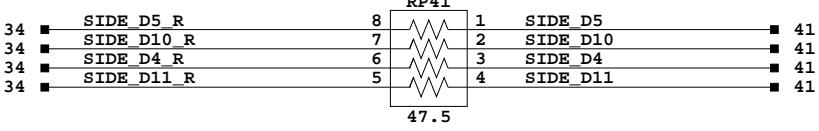
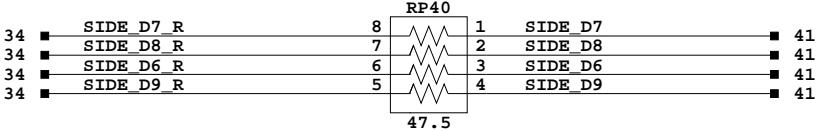
Pin20-Key

J16

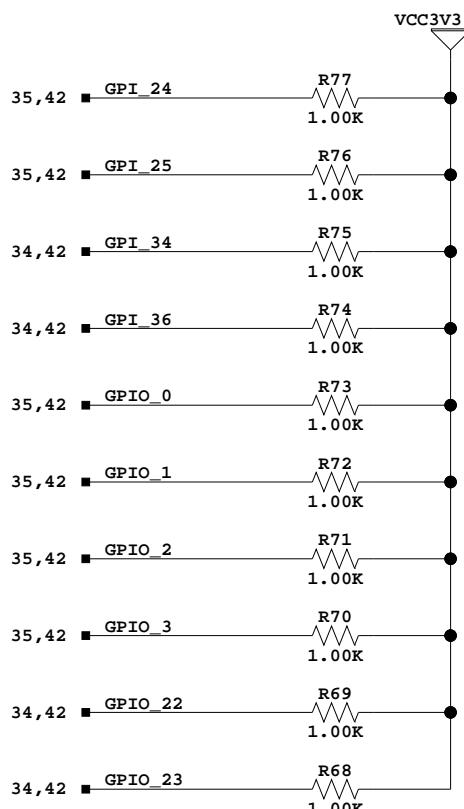
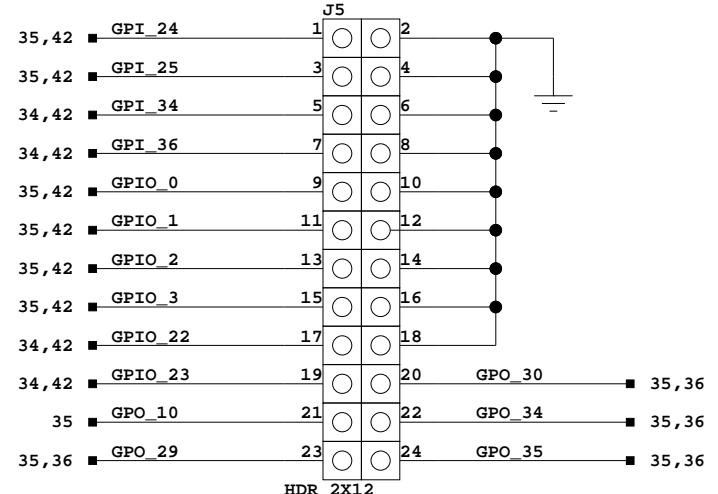
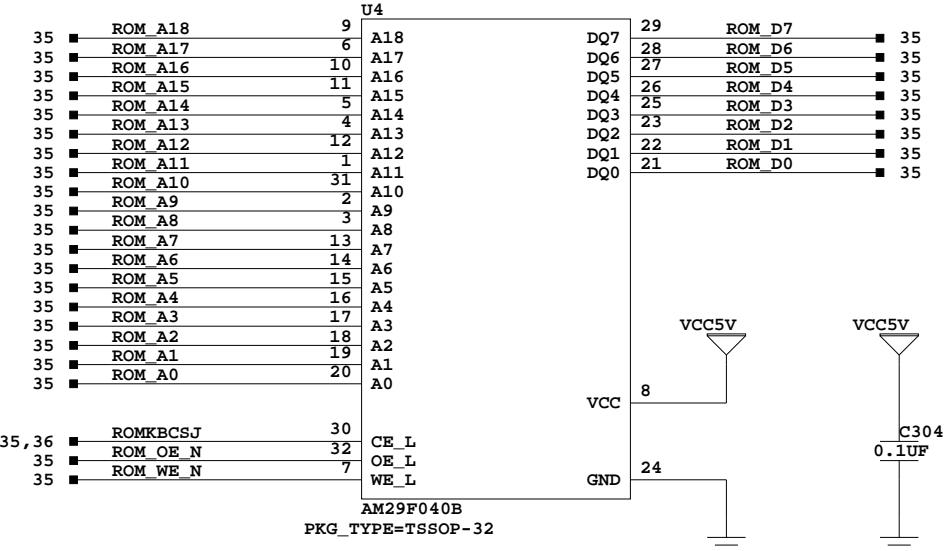
IDE PRIMARY CONN

Pin 20 must be removed.

Silkscreen:
"IDE SECONDARY"



SOUTH BRIDGE GPIO HEADER



SCH P/N	0381171-02
ART P/N	0531311-02
FAB P/N	1280333-02

title: MI-310. WIRETEX II. PRO. BILLETARY

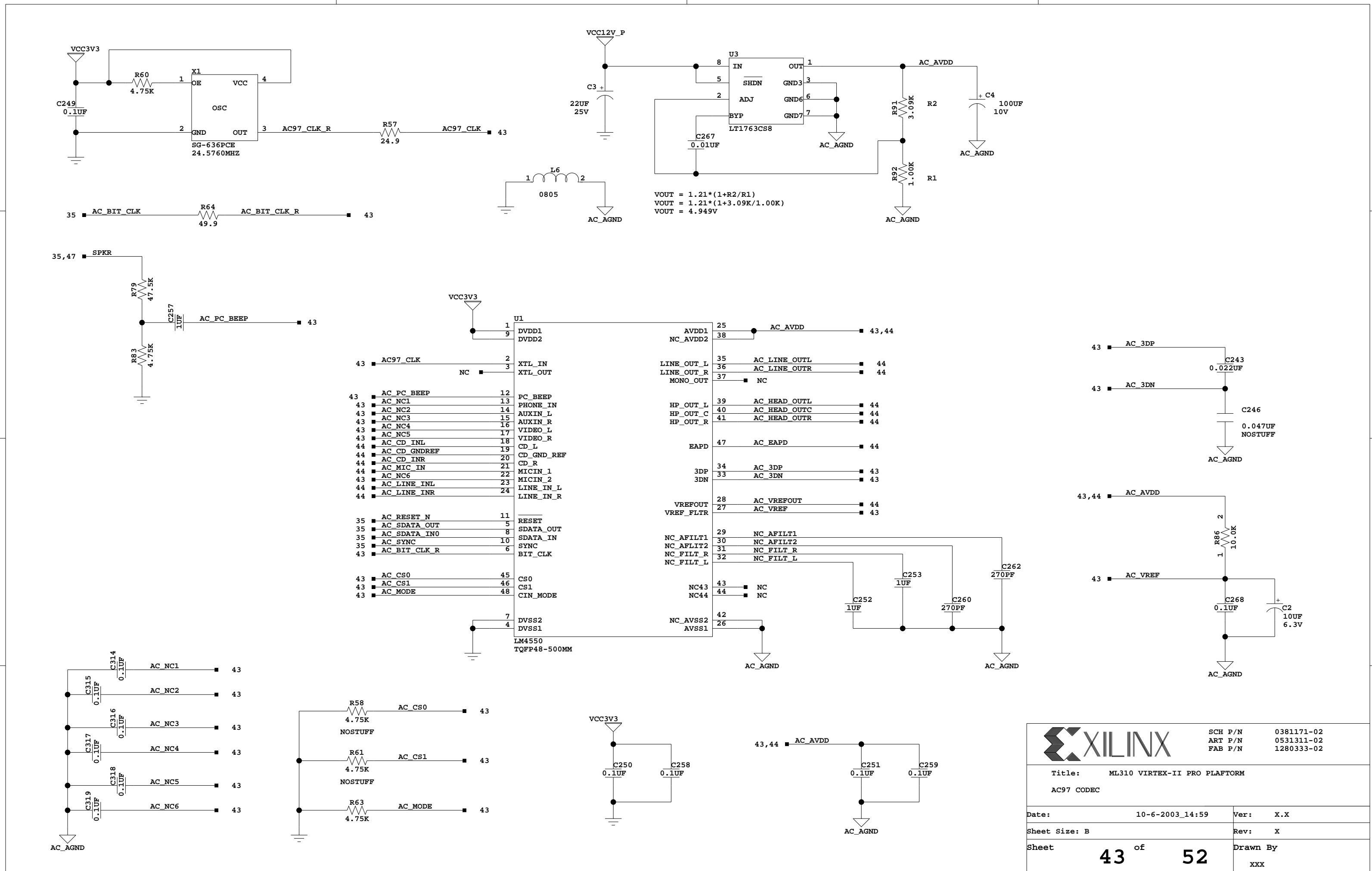
SOUTH BRIDGE ROM AND CBIO

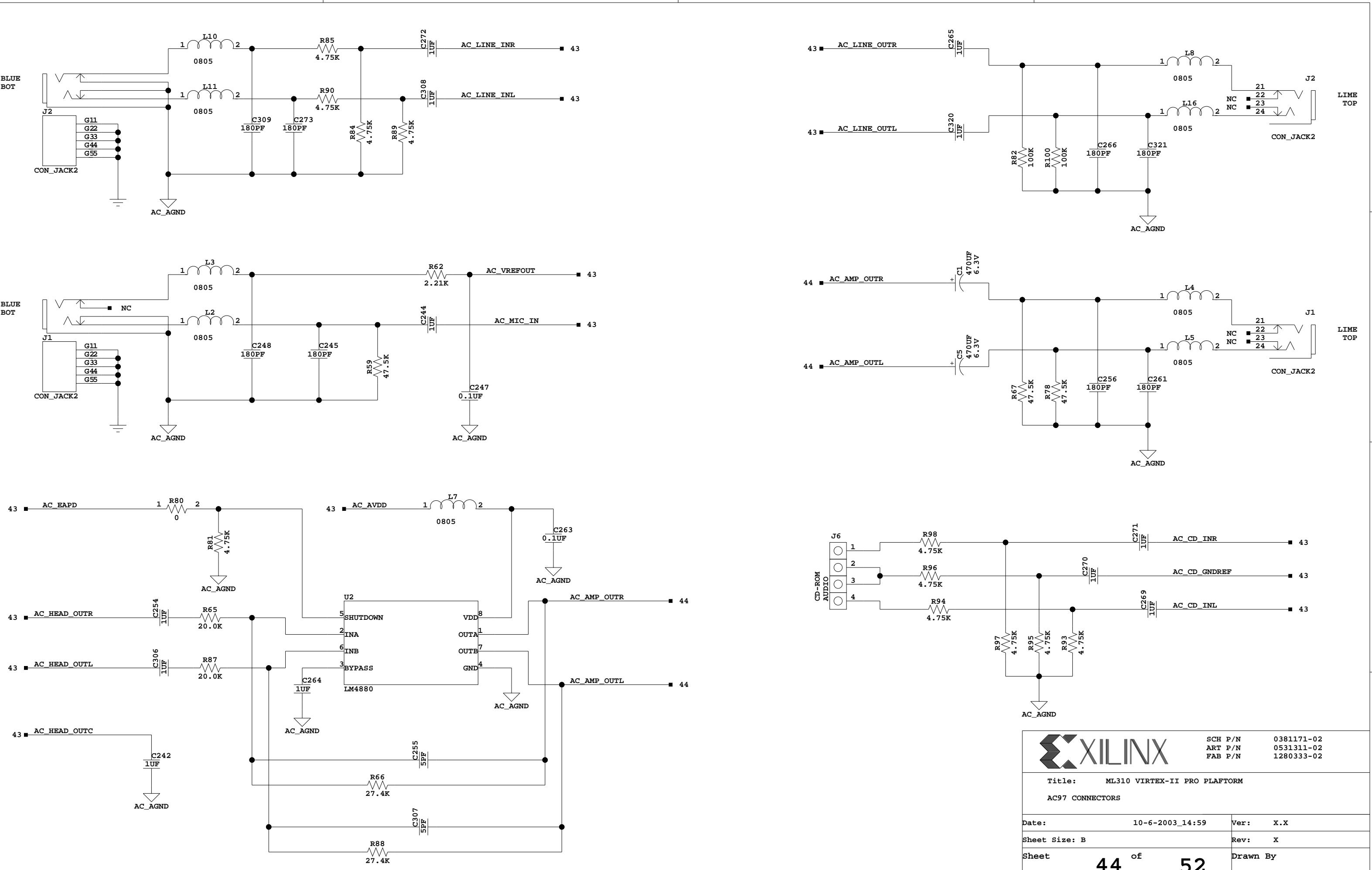
6-16-2004 18:00 Ver: x x

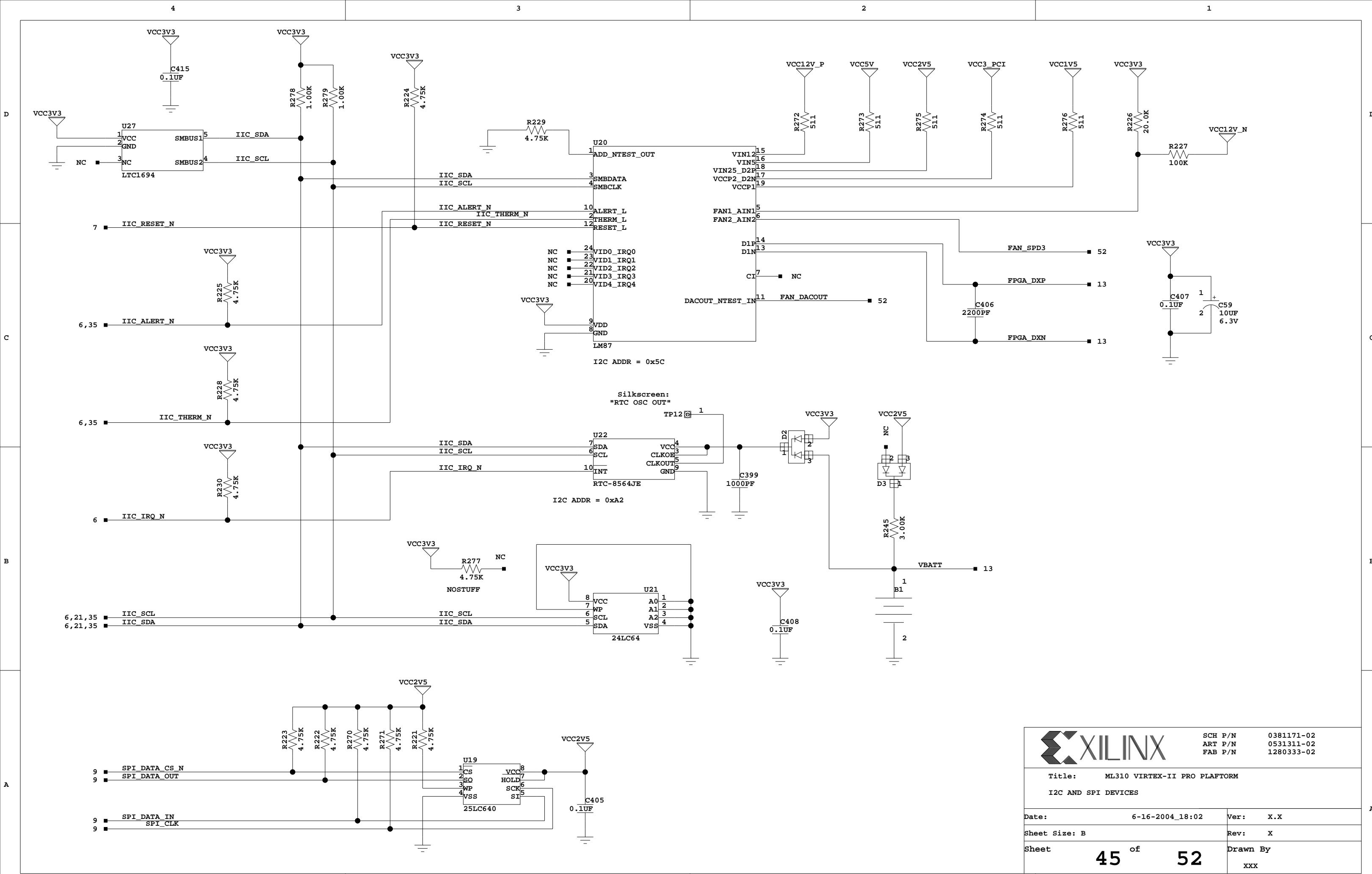
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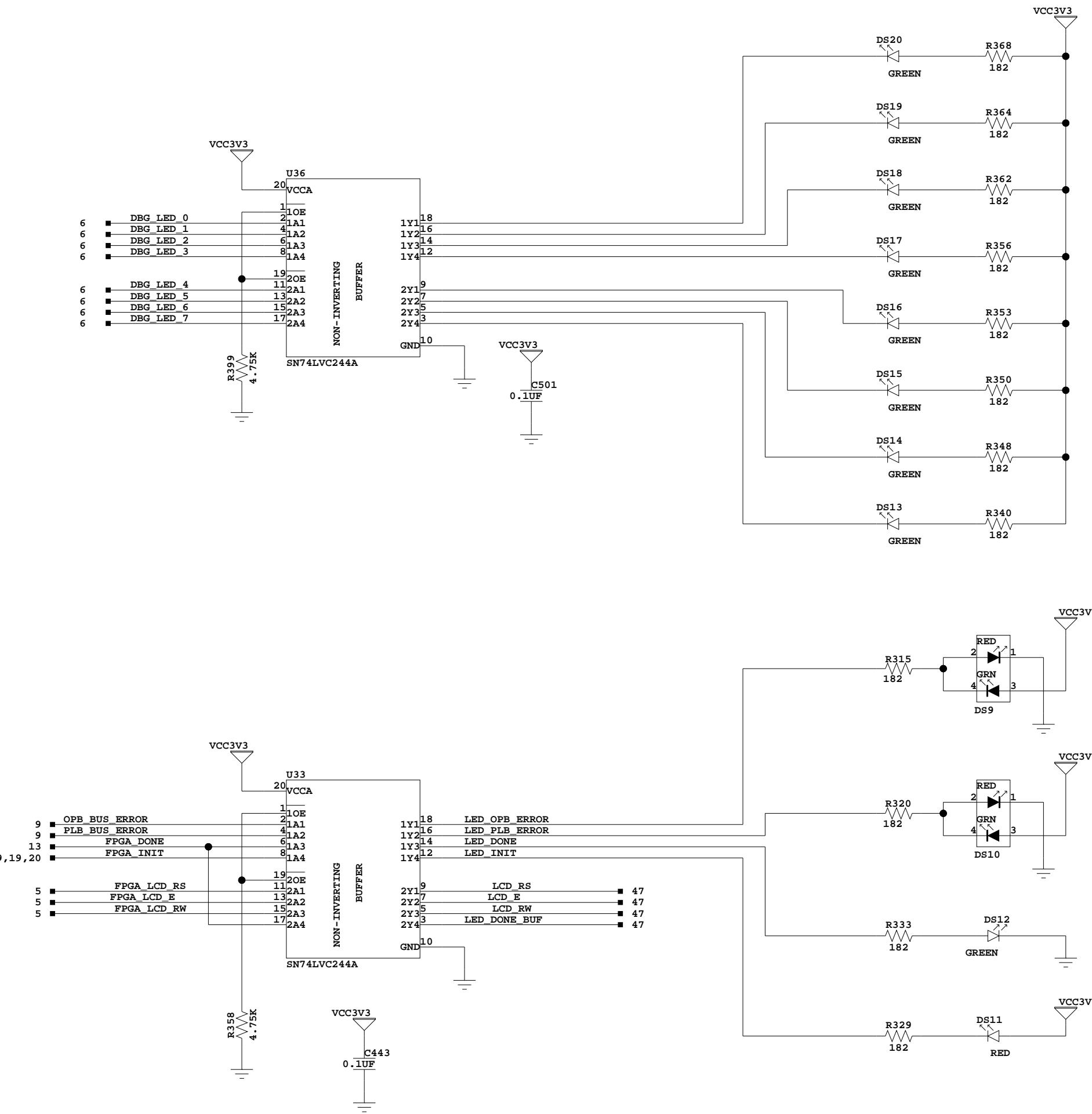
t _____ of _____ - _____ Drawn By _____

42 of 52

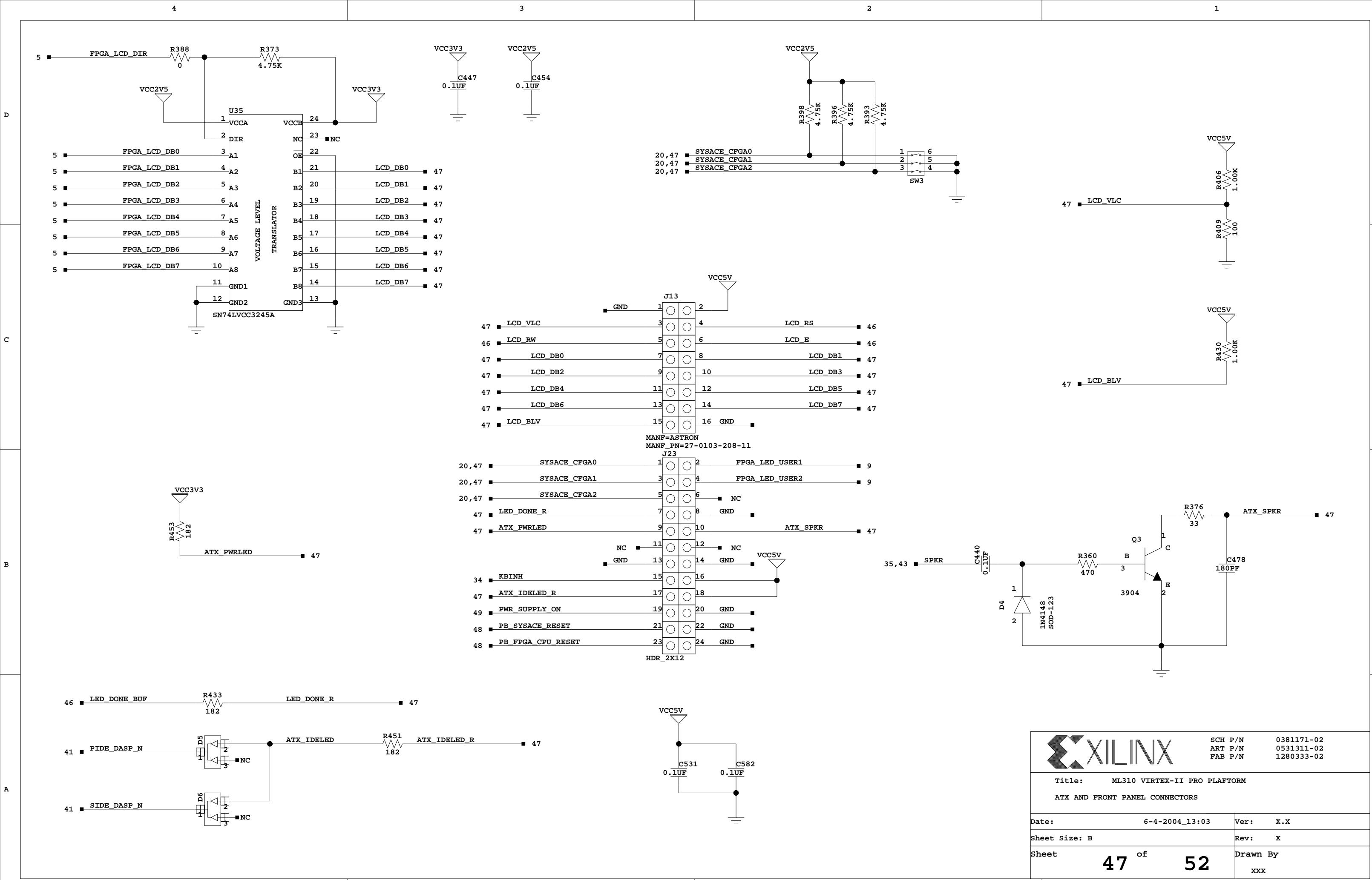






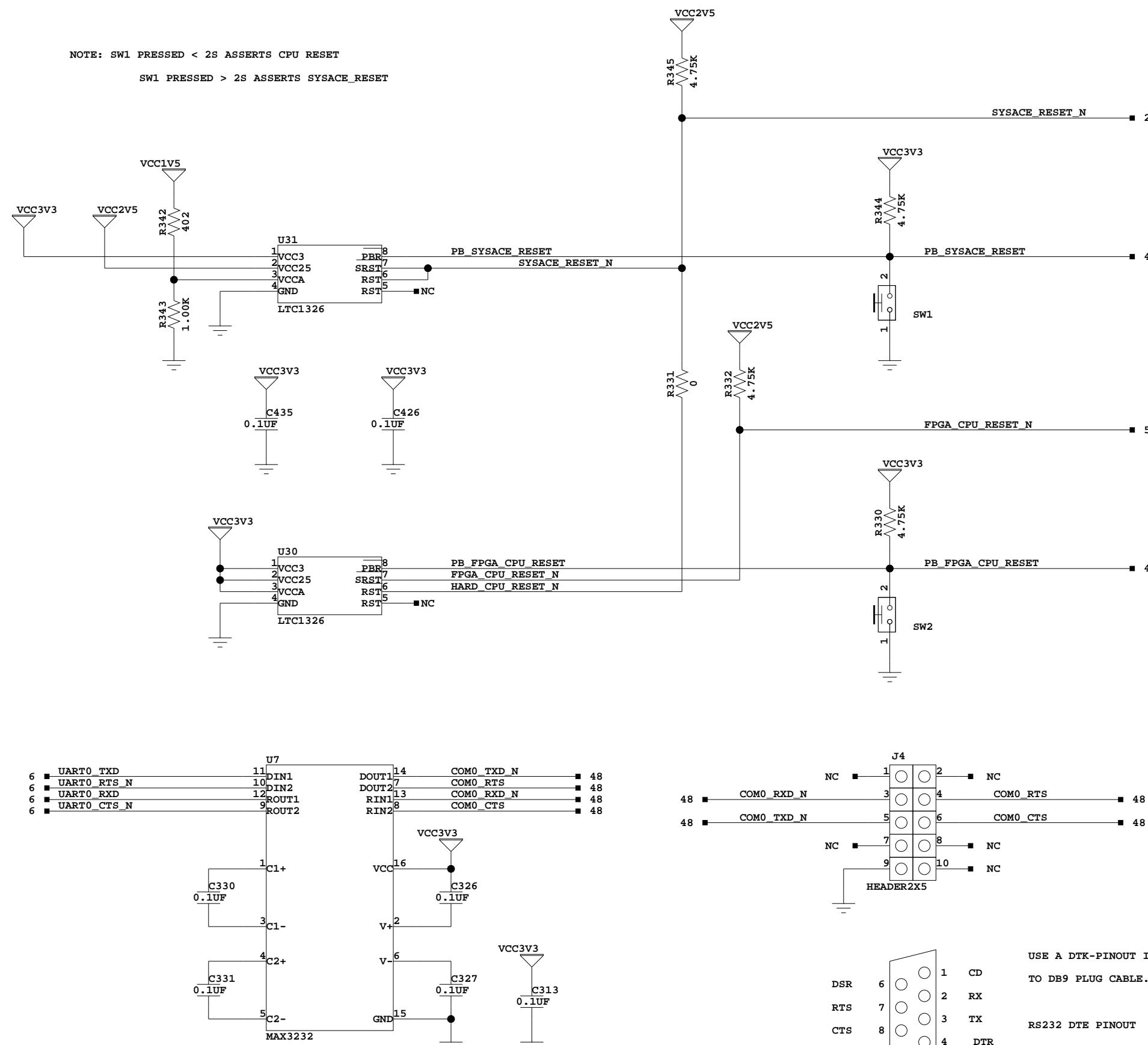


XILINX	SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
DEBUG AND STATUS LEDS	
Date: 10-6-2003_14:59	Ver: X.X
Sheet Size: B	Rev: X
Sheet	Drawn By
46 of 51	xxx

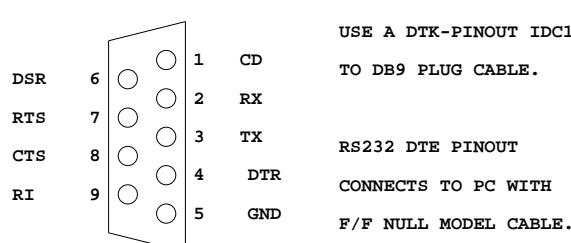


NOTE: SW1 PRESSED < 2S ASSERTS CPU RESET

SW1 PRESSED > 2S ASSERTS SYSACE RESET



LOOKING INTO DB9 BLUG



USE A DTK-PINOUT IDC1

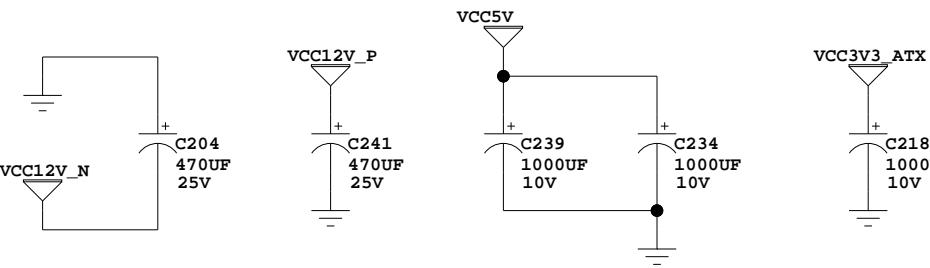
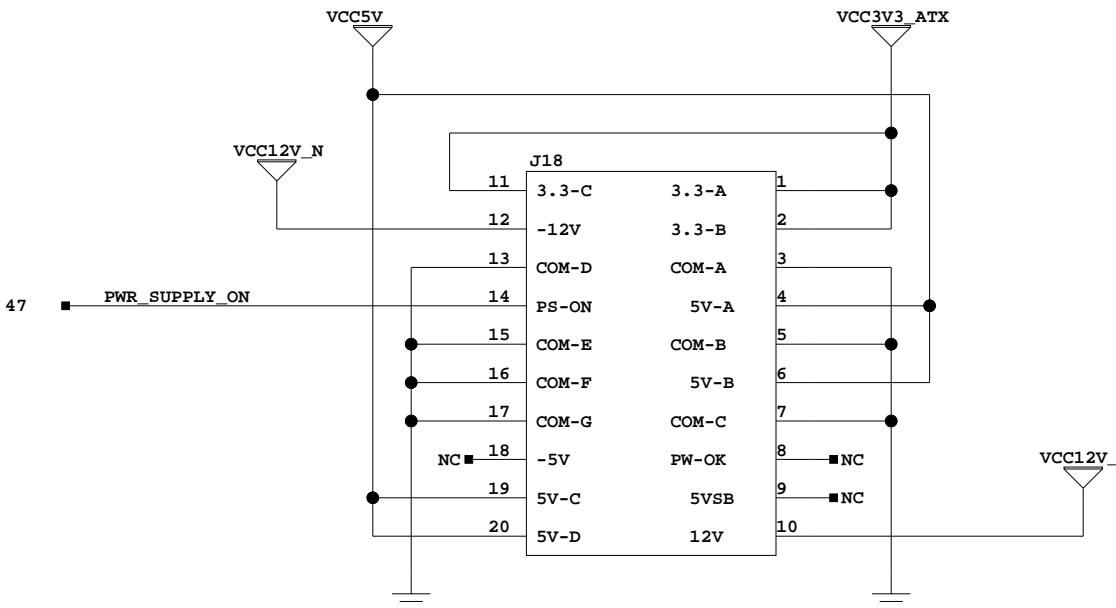
TO DB9 PLUG CABLE

RS232 DTE PINOUT

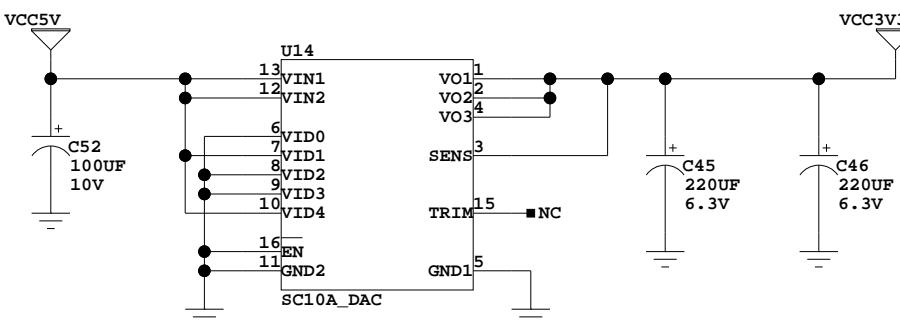
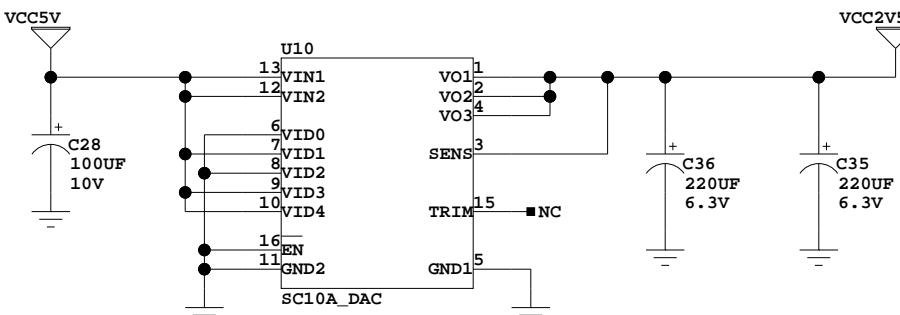
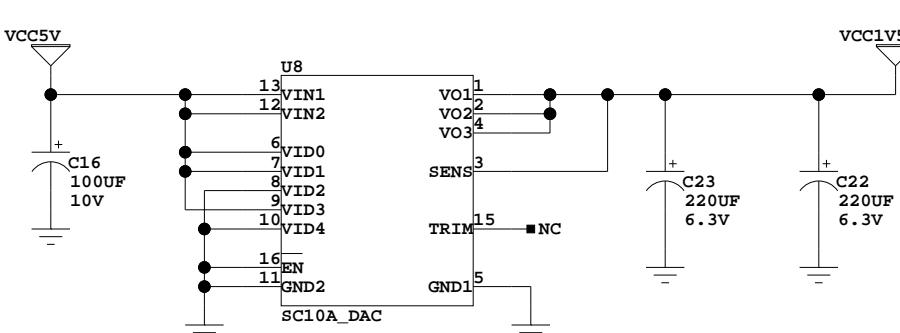
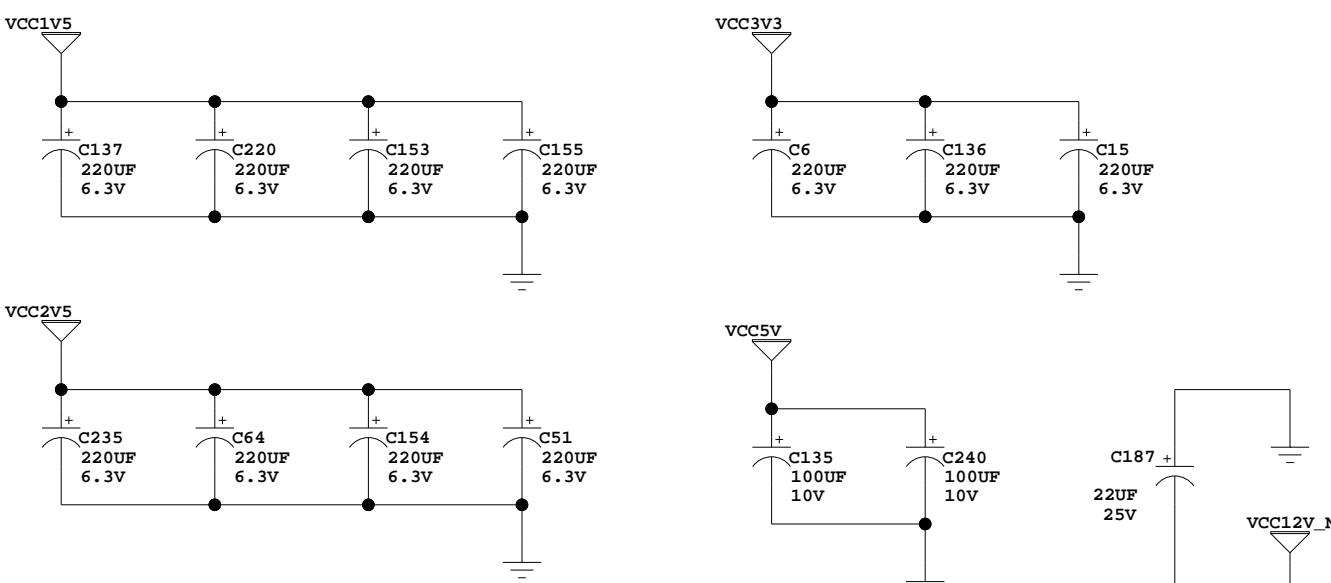
CONNECTS TO PC WITH

E/E NULL MODEL CABLE

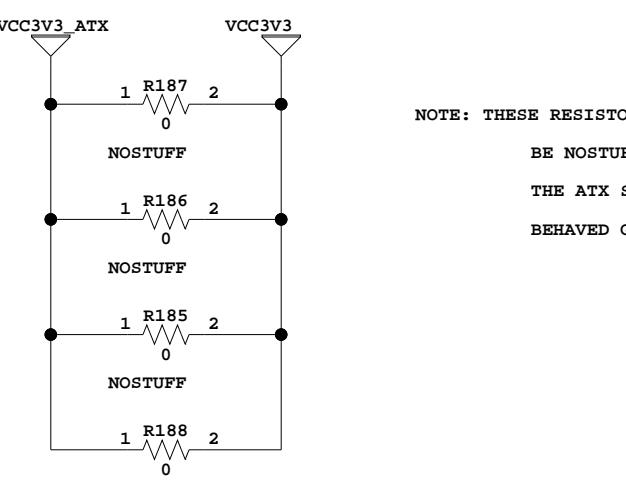
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Title: ML310 VIRTEX-II PRO PLATFROM			
RESET SWITCHES AND FPGA SERIAL PORT			
Date:	6-4-2004_13:04	Ver:	X.X
Sheet Size: B		Rev:	X
Sheet	48 of 52	Drawn By	
		XXX	



ATX Power Connector

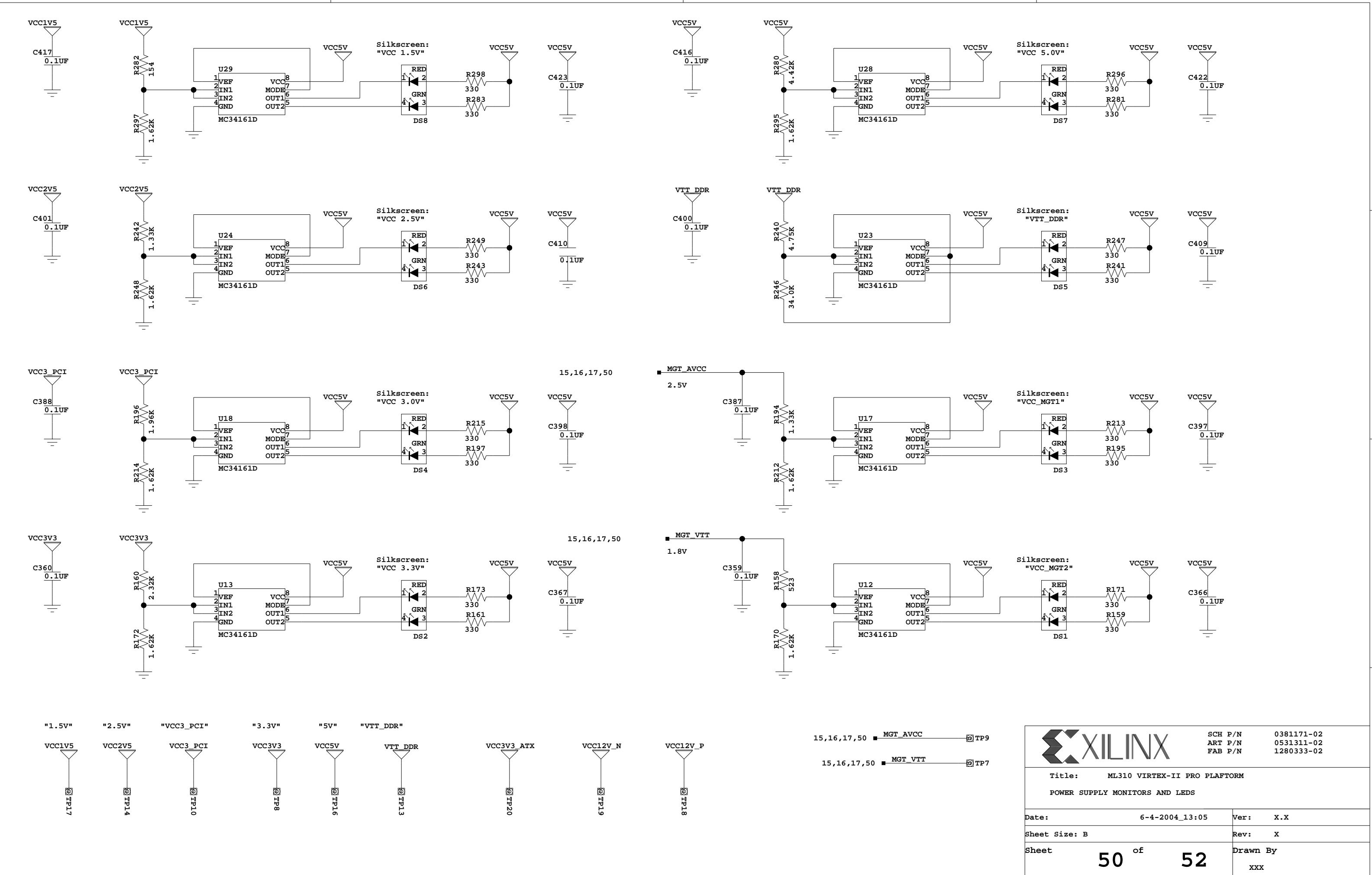


NOTE: TYPICAL ATX POWER SUPPLIES MAY NOT PRODUCE A WELL-REGULATED 3.3V SUPPLY UNLESS THERE IS A MINIMUM LOAD ON THE 5V OUTPUT. THEREFORE 3.3V IS REGULATED SEPARATELY FOR ON-BOARD USE.

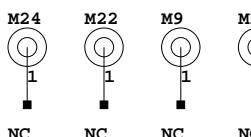
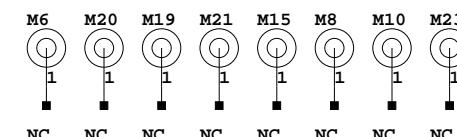
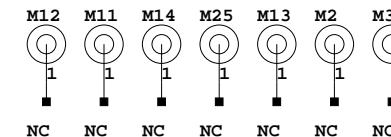
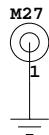
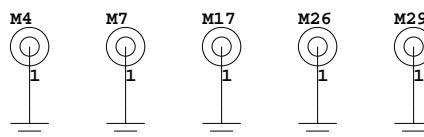
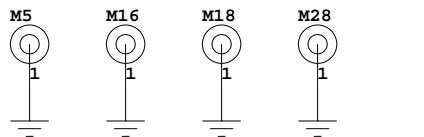


XILINX

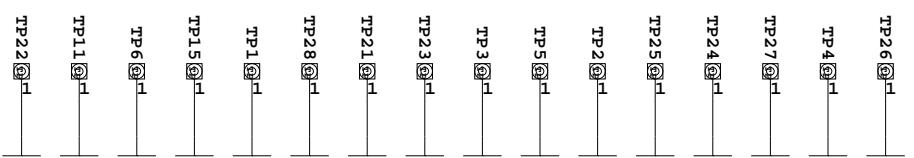
SCH P/N	0381171-02
ART P/N	0531311-02
FAB P/N	1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
ATX CONNECTOR AND DC-DC CONVERTORS	
Date:	10-6-2003_14:59
Sheet Size:	B
Sheet	49 of 52
Drawn By	xxx



Mounting holes for ATX Form Factor

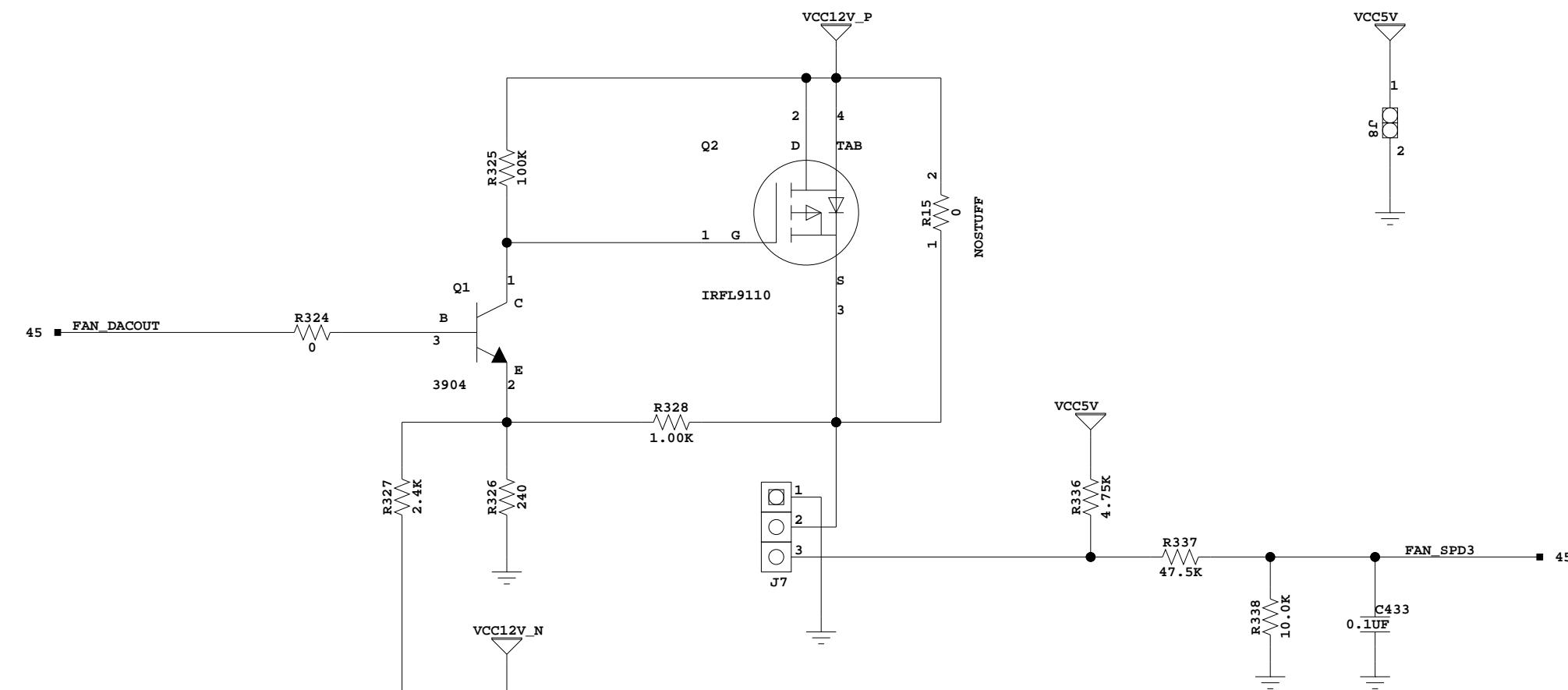


Spread out on the board.



Silkscreen:
"GND"

		SCH P/N 0381171-02
		ART P/N 0531311-02
		FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM		
ATX MOUNTING HOLES AND TEST POINTS		
Date:	1-5-2004_13:05	Ver: x.x
Sheet Size:	B	Rev: X
Sheet	51 of 52	Drawn By xxx



XILINX	SCH P/N 0381171-02 ART P/N 0531311-02 FAB P/N 1280333-02
Title: ML310 VIRTEX-II PRO PLATFROM	
FPGA FAN SWITCH AND TACH	
Date: 6-4-2004_13:06	Ver: X.X
Sheet Size: B	Rev: X
Sheet 52 of 52	Drawn By xxx