Final Project: 2bits Full Adder Layout

第_7_組/學號___41171105H__/姓名__盧昱廷____

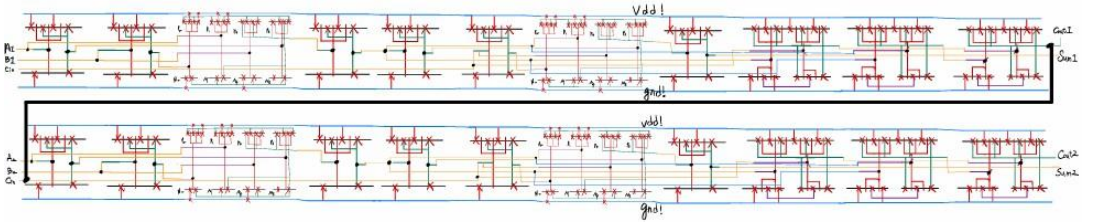
	系級/學號	姓名
組員 1	科技系 115/41171109H	林易辰
	貢獻度:棒狀圖繪製/DRC 除錯 25%	
組員 2	科技系 115/41171105H	盧昱廷
	貢獻度: layout 繪製/ DRC 除錯 25%	
組員 3	機電系 116/41273102H	呂崇聖
	貢獻度: layout 繪製/ DRC 除錯 25%	
組員 4	機電系 116/ 41273158H	吳東翰
	貢獻度: layout 繪製/ DRC 除錯 25%	

例如: 貢獻度:佈局/尺寸/DRC 除錯… (25%)

1. Stick Diagram (15%)

Please draw the stick diagram of 2bit Full adder layout

以下是 stick diagram

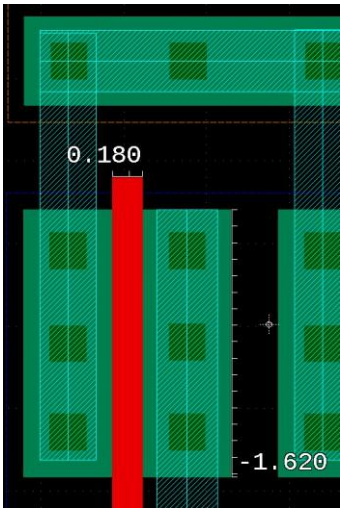


2. PMOS/NMOS Size check (15%)

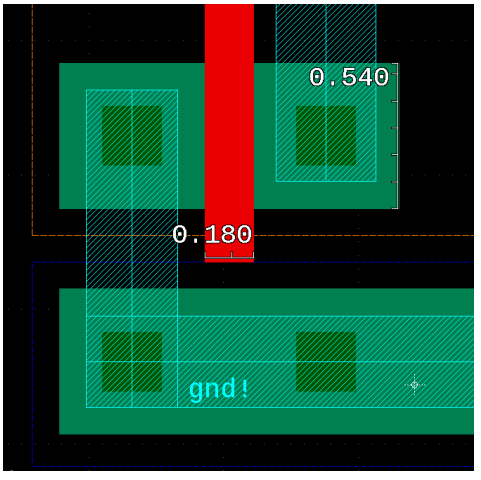
Please measured all PMOS width/length (W/L), all NMOS width/length (W/L)

Inverter: Pmos/ Nmos

Pmos：W=1.620um L=0.18um

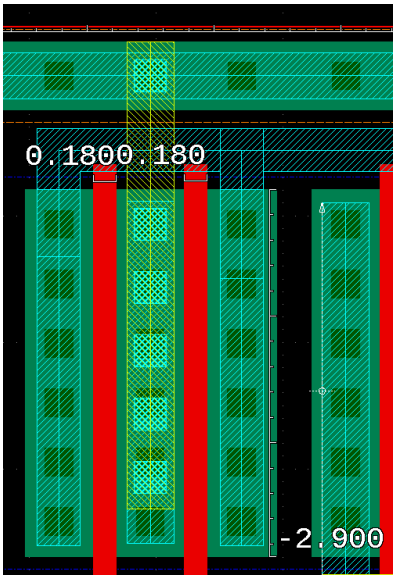


Nmos：W=0.540um,L=0.180um

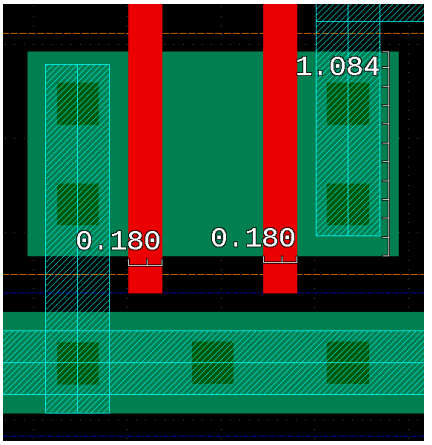


XNOR:pmos/nmos

Pmos：W=2.900um,L=0.18um

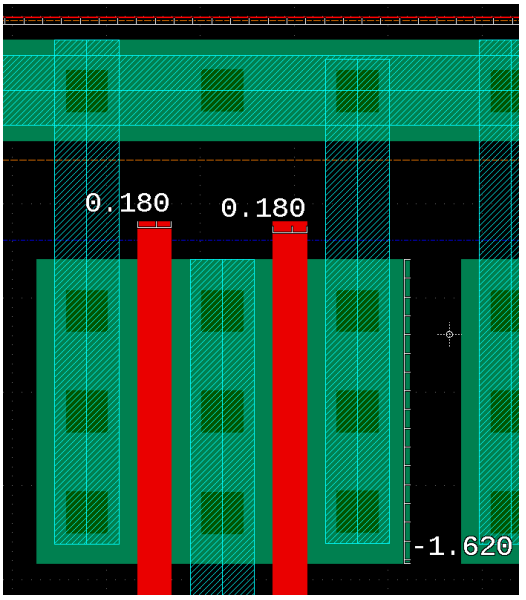


Nmos：W=1.084um,L=0.18um

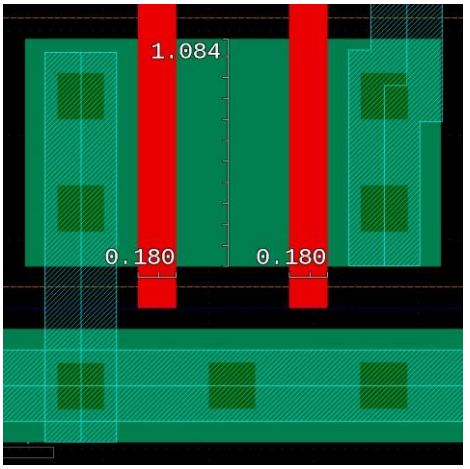


NAND:pmos/nmos

Pmos：W=1.620um,L=0.180um



Nmos：W=1.084um,L=0.18um

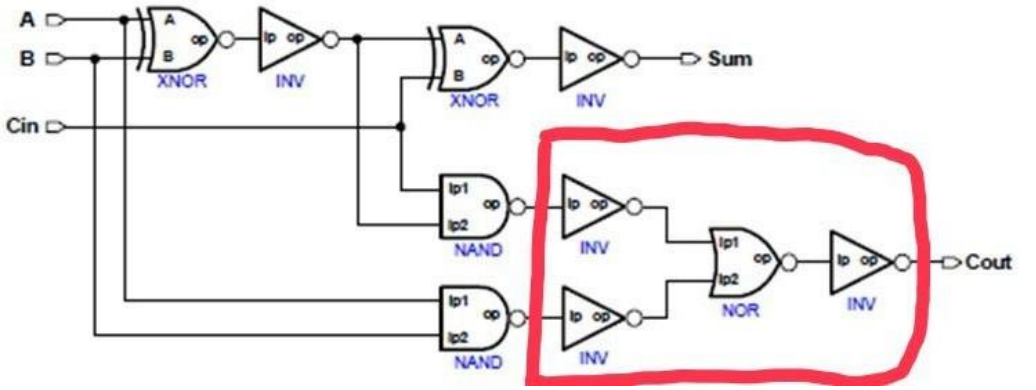


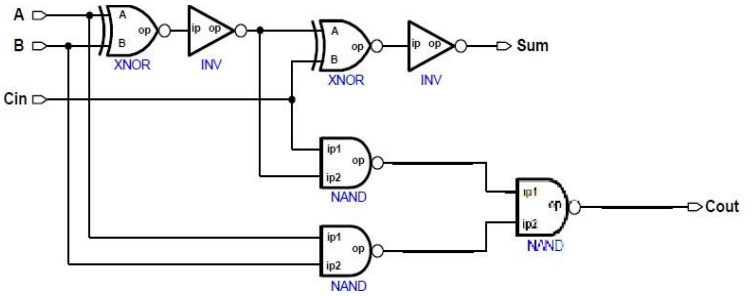
3. Layout versus schematic discussion (20%)

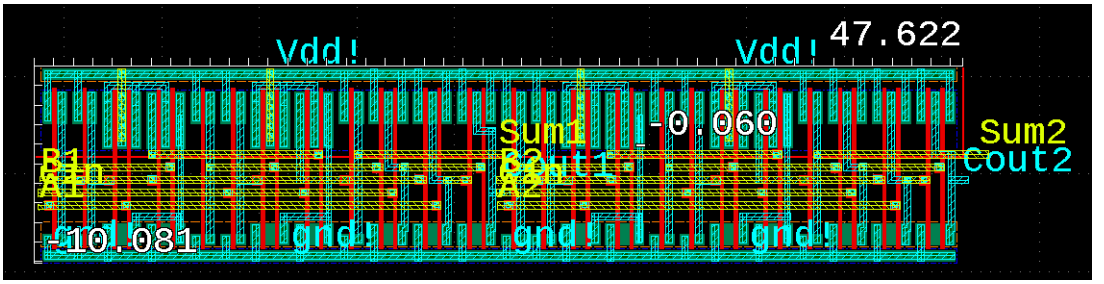
Please explain the relationship between the layout of each part and its logic gate circuits.

將 XNOR without two input INV 的前面先接兩顆 INV，後面接一顆 INV 後，再將其與 Cin 接到下一個 XNOR without two input INV 前面的 INV，，接著接 INV 到 Sum。然後將其與 Cin 接到 NAND，再與 A和 B 做的 NAND 進行一次 NAND 得到 Cout，此為 1 bit 全加器。將以上的複製一份，把第一份的 Cout 接到第二份的 Cin，就完成了 2 bits full adder。

我們將紅色部分改為 NAND。

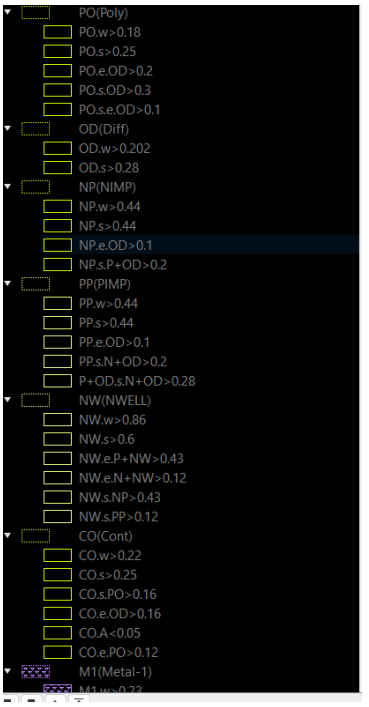


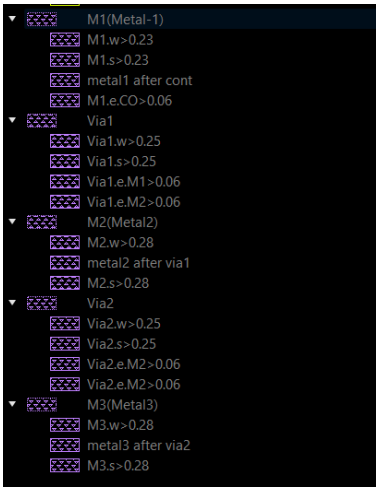

A
B
Cin
XNOR
INV
XNOR
INV
Sum
NAND
NAND
NAND
Cout


Vdd!
Vdd!
47.622
Sum1
-0.060
Sum2
Cout2
-10.081
gnd!
gnd!
gnd!

4. DRC error check (20%)

Please copy the DRC error message or mask windows

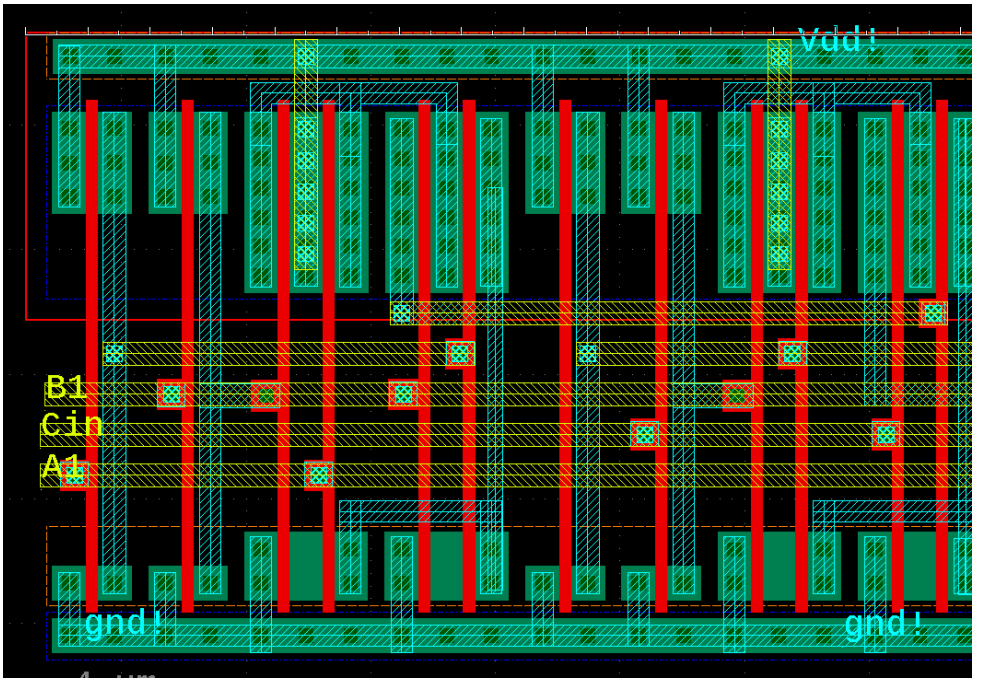


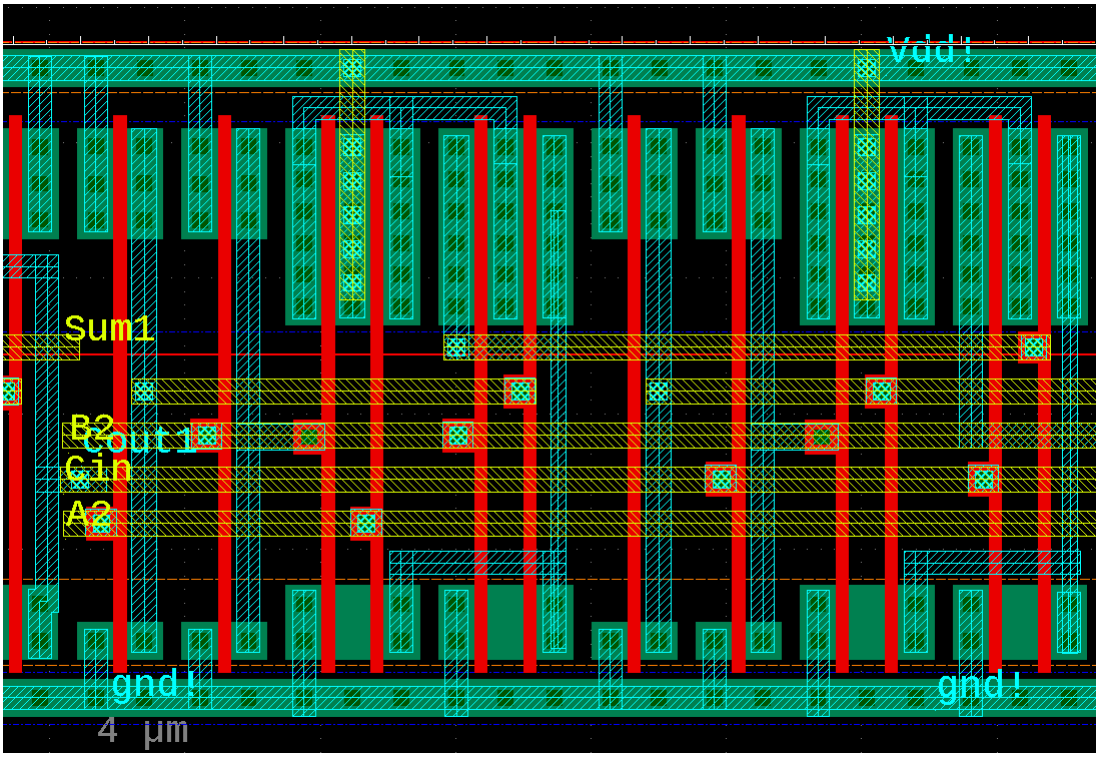


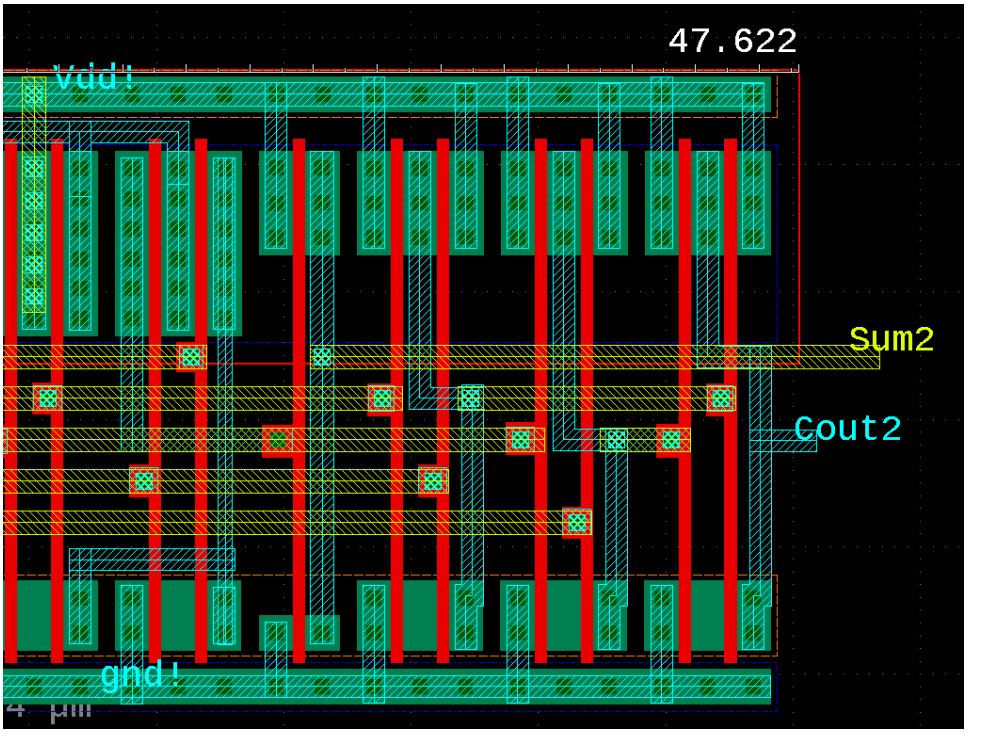
5. Label Text check (15%)

Please show each node of A, B, Cin, Cout, Sum, vdd!, gnd!

名字都已標上




Vdd!
Sum1
B2
Cout1
Cin
A2
gnd!
gnd!
4 µm


47.622
Vdd!
Sum2
Cout2
gnd!
4 µm

6. Layout Size (15%)

Please measure the chip size

Size:47.622µm x 10.081µm = 480.077382 µm²