Output

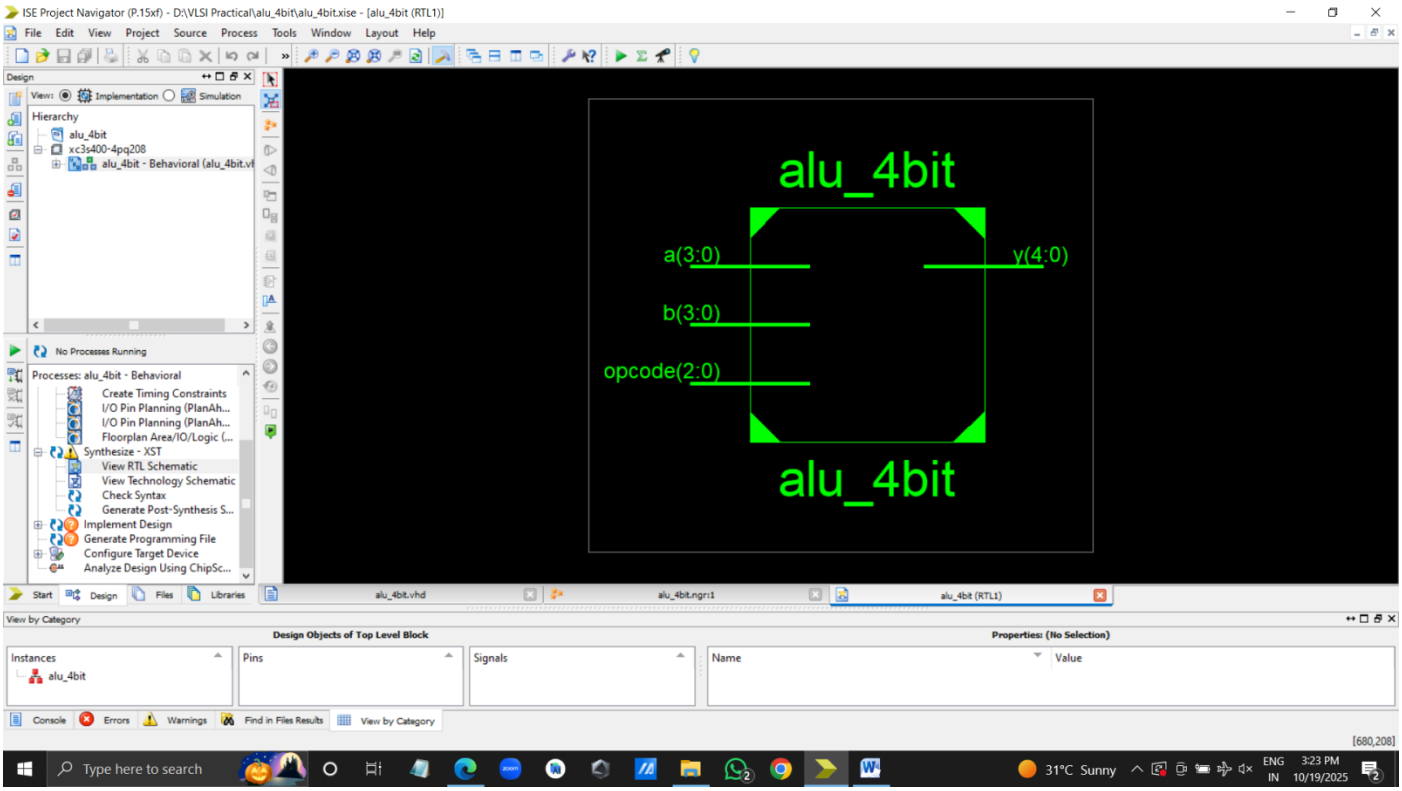
4-bit Arithmetic Logic Unit

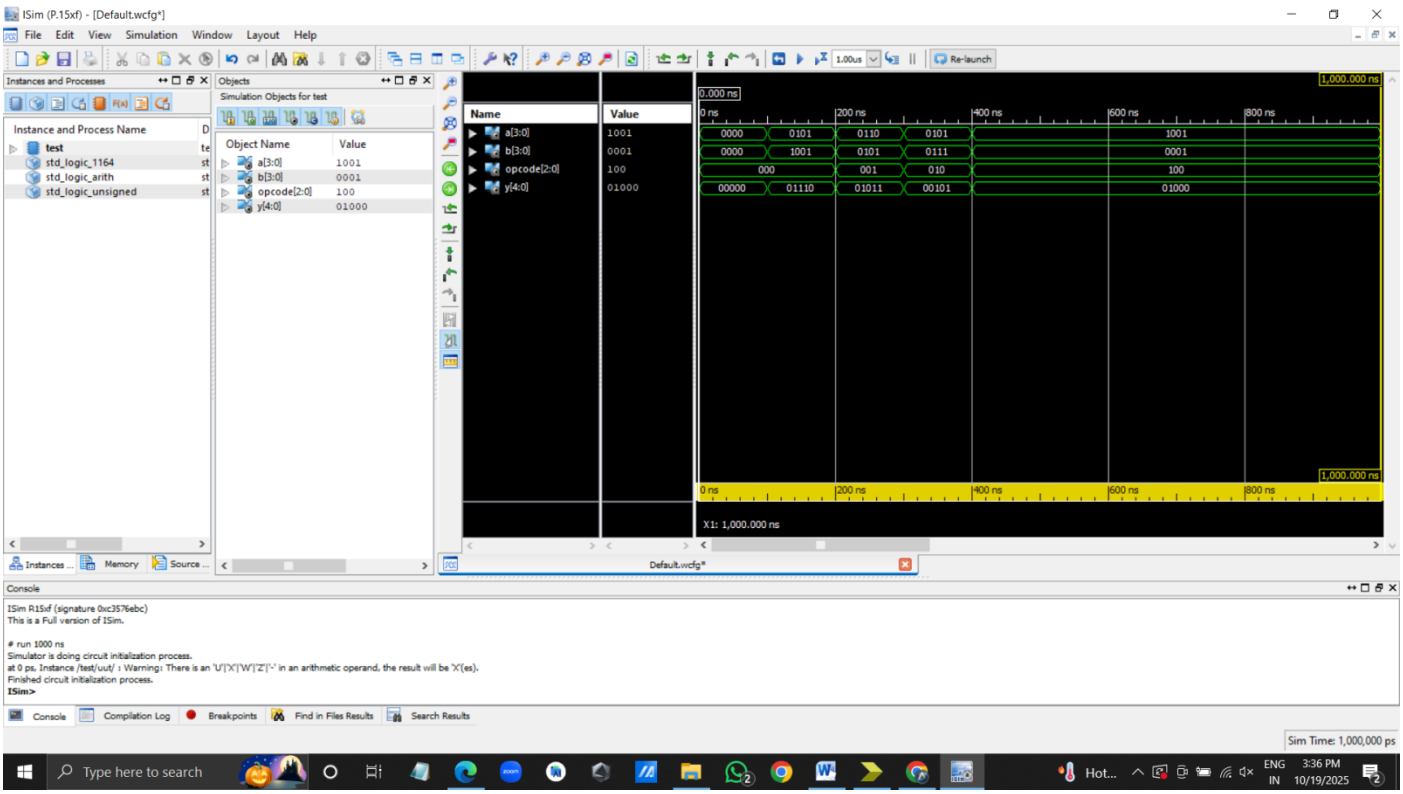
Program for ALU 4-bit :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
Entity alu_4bit is
 Port ( a,b: in STD_LOGIC_VECTOR ( 3 downto 0);
        opcode : in STD_LOGIC_VECTOR ( 2 downto 0);
        Y : out  STD_LOGIC_VECTOR ( 4 downto 0));
End alu_4bit;
architecture Behavioral of alu_4bit is
        SIGNAL as,bs,ys : STD_LOGIC_VECTOR(4 downto 0);
Begin
as<='0'&a;
bs<='0'&b;
process(as,bs,opcode,ys)
begin
        case opcode is
                when  "000"=> ys<=as+bs; y(4)<=ys(4);
                when  "001"=> ys<=as+bs; y(4)<=ys(4);
                when  "010"=> ys<=as and bs;
                when  "011"=> ys<=as nand bs;
                when  "100"=> ys<=as xor bs;
                when  "101"=> ys<=as xnor bs;
                when  "110"=> ys<=as or bs;
                when  others=>ys<= '0' & as (3 downto 0);
        end case;
end process;
y(3 downto 0)<=ys(3 downto 0);
end behavioral;
```

UCF Alu 4 bit :

```
NET "a<0>"  LOC= "p57";
NET "a<1>"  LOC= "p52";
NET "a<2>"  LOC= "p51";
NET "a<3>"  LOC= "p50";
NET "b<0>"  LOC= "p43";
NET "b<1>"  LOC= "p42";
NET "b<2>"  LOC= "p40";
NET "b<3>"  LOC= "p39";
NET "opcode<0>"  LOC= "p36";
NET "opcode<1>"  LOC= "p35";
NET "opcode<2>"  LOC= "p34";
NET "y<0>"  LOC= "p80";
NET "y<1>"  LOC= "p79";
NET "y<2>"  LOC= "p78";
NET "y<3>"  LOC= "p77";
NET "y<4>"  LOC= "p76";
```


ISE Project Navigator (P.15xf) - D:\VLSI Practical\alu_4bit\alu_4bit.xise - [alu_4bit (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
alu_4bit
xc3s400-4pq208
alu_4bit - Behavioral (alu_4bit.vh
No Processes Running
Processes: alu_4bit - Behavioral
Create Timing Constraints
I/O Pin Planning (PlanAh...
I/O Pin Planning (PlanAh...
Floorplan Area/IO/Logic (...
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipSc...
alu_4bit
a(3:0)
b(3:0)
opcode(2:0)
y(4:0)
alu_4bit
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
Type here to search
31°C Sunny
ENG IN
3:23 PM
10/19/2025


ISim (P.15xf) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
test
std_logic_1164
std_logic_arith
std_logic_unsigned
Objects
Simulation Objects for test
Object Name
Value
a[3:0] 1001
b[3:0] 0001
opcode[2:0] 100
y[4:0] 01000
Name
Value
a[3:0]
b[3:0]
opcode[2:0]
y[4:0]
0.000 ns
200 ns
400 ns
600 ns
800 ns
1,000.000 ns
X1: 1,000.000 ns
Default.wcfg*
Console
ISim R15xf (signature 0xc3576ebc)
This is a Full version of ISim.
run 1000 ns
Simulator is doing circuit initialization process.
at 0 ps, Instance /test/uut/ : Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
Type here to search
ENG IN
3:36 PM
10/19/2025