Output

LCD Controller

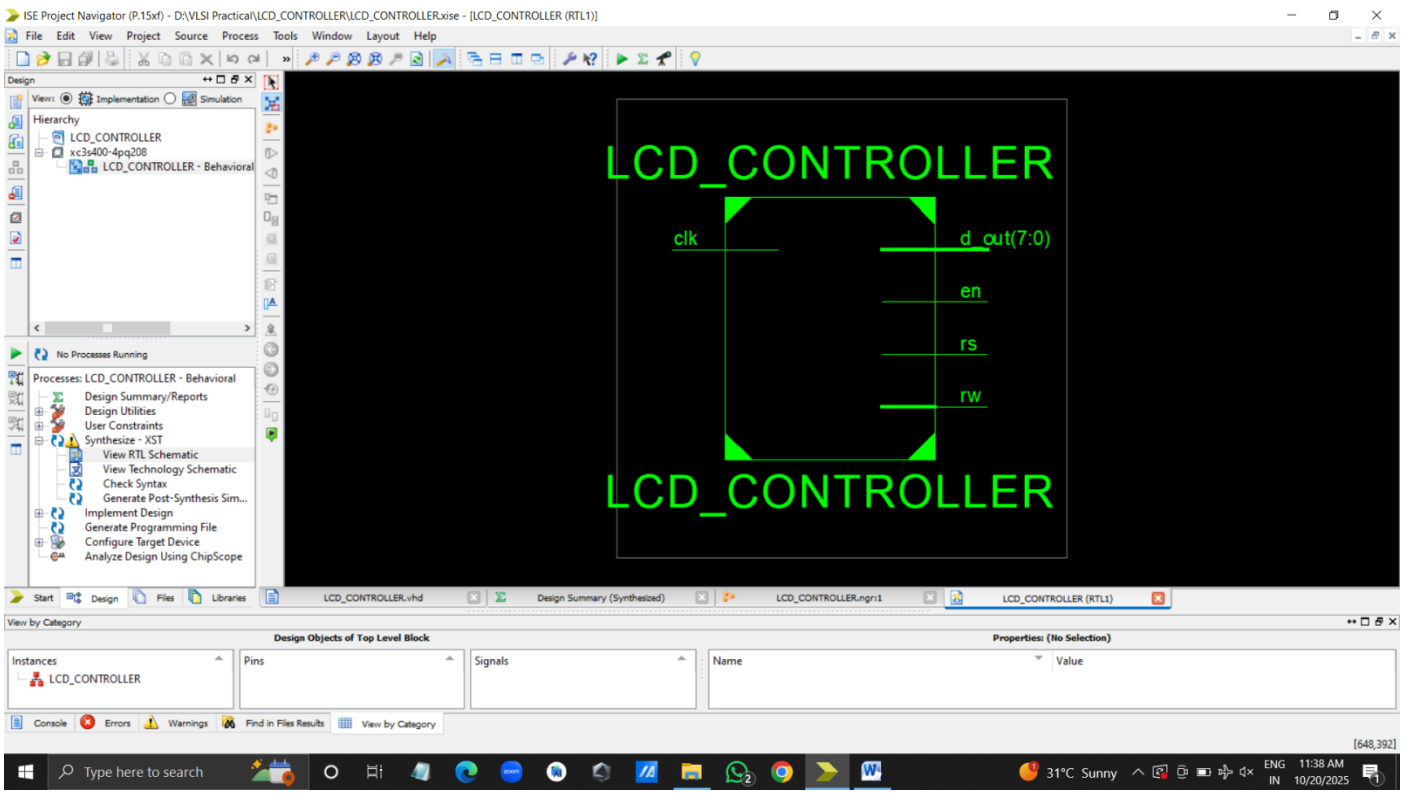
Program for LCD CONTROLLER :

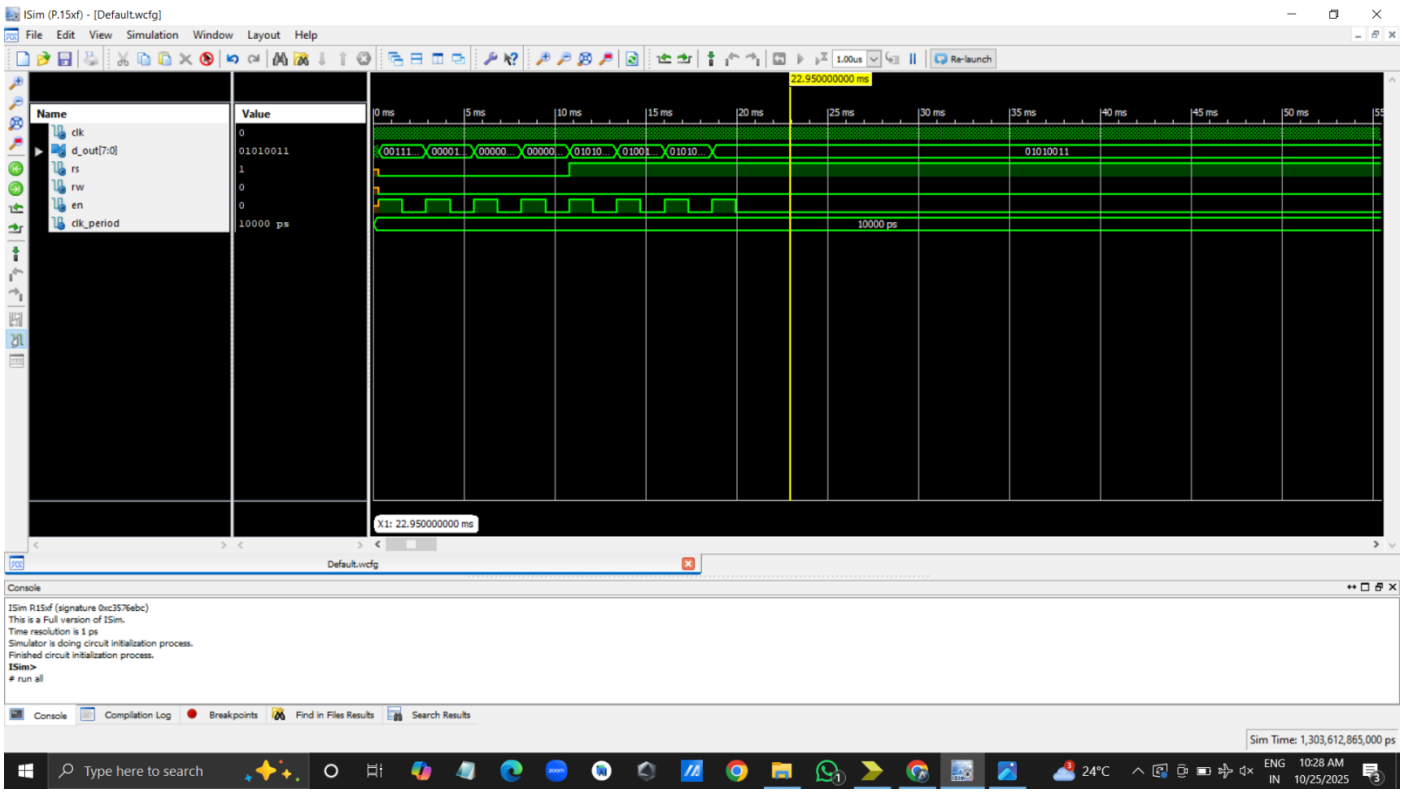
```
entity LCD_CONTROLLER is
        port(clk:in std_logic;
        d_out:out std_logic_vector(7 downto 0);
        rs,rw,en:out std_logic);
end LCD_CONTROLLER;
architecture Behavioral of LCD_CONTROLLER is
        type state is (s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11,s12,s13,s14,s15);
        signal pr_state, ns_state:state;
        signal clk_lcd: std_logic_vector(15 downto 0):=(others=>'0');
begin
        process(clk)
        begin
                if rising_edge(clk) then
                        clk_lcd<=clk_lcd+1;
                end if;
        end process;

        process(clk_lcd(15), pr_state, ns_state) then
        begin
                if rising_edge(clk_lcd(15)) then
                        pr_state<=ns_state;
                end if;
        end process;
        process(clk_lcd(15), pr_state, ns_state)
        begin
                if rising_edge(clk_lcd(15)) then
                        case pr_state is
                                when s0=> d_out<=x"38"; rs<='0';rw<='0';en<='1';ns_state<=s1;
                                when s1=> d_out<=x"38"; rs<='0';rw<='0';en<='0';ns_state<=s2;
                                when s2=> d_out<=x"0C"; rs<='0';rw<='0';en<='1';ns_state<=s3;
                                when s3=> d_out<=x" 0C"; rs<='0';rw<='0';en<='0';ns_state<=s4;
```

```
                    when s4=> d_out<=x"06"; rs<='0';rw<='0';en<='1';ns_state<=s5;
                    when s5=> d_out<=x"06"; rs<='0';rw<='0';en<='0';ns_state<=s6;
                    when s6=> d_out<=x"01"; rs<='0';rw<='0';en<='1';ns_state<=s7;
                    when s7=> d_out<=x"01"; rs<='0';rw<='0';en<='0';ns_state<=s8;
                    when s8=> d_out<=x"53"; rs<='1';rw<='0';en<='1';ns_state<=s9;
                    when s9=> d_out<=x"53"; rs<='1';rw<='0';en<='0';ns_state<=s10;
                    when s10=> d_out<=x"49"; rs<='1';rw<='0';en<='1';ns_state<=s11;
                    when s11=> d_out<=x"49"; rs<='1';rw<='0';en<='0';ns_state<=s12;
                    when s12=> d_out<=x"54"; rs<='1';rw<='0';en<='1';ns_state<=s13;
                    when s13=> d_out<=x"54"; rs<='1';rw<='0';en<='0';ns_state<=s14;
                    when s14=> d_out<=x"53"; rs<='1';rw<='0';en<='1';ns_state<=s15;
                    when s15=> d_out<=x"53"; rs<='1';rw<='0';en<='0';ns_state<=s15;
                end case;
            end if;
        end process;
end behavioral;
```

UCF For LCD Controller :

```
NET "clk" LOC="p181";
NET "d_out<0>"  LOC= "p167";
NET "d_out<1>"  LOC= "p166";
NET "d_out<2>"  LOC= "p165";
NET "d_out<3>"  LOC= "p162";
NET "d_out<4>"  LOC= "p161";
NET "d_out<5>"  LOC= "p156";
NET "d_out<6>"  LOC= "p155";
NET "d_out<7>"  LOC= "p154";
NET "en"  LOC="p168";
NET "rs"  LOC="p171";
NET "rw" LOC="p169";
```


ISE Project Navigator (P.15xf) - D:\VLSI Practical\LCD_CONTROLLER\LCD_CONTROLLER.xise - [LCD_CONTROLLER (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
LCD_CONTROLLER
xc3s400-4pq208
LCD_CONTROLLER - Behavioral
No Processes Running
Processes: LCD_CONTROLLER - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Sim...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
LCD_CONTROLLER
clk
d_out(7:0)
en
rs
rw
LCD_CONTROLLER
Design Objects of Top Level Block
Properties: (No Selection)
Instances
LCD_CONTROLLER
Pins
Signals
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
Type here to search
31°C Sunny
ENG IN
11:38 AM
10/20/2025


ISim (P.15xf) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
clk
d_out[7:0]
rs
rw
en
clk_period
0
01010011
1
0
0
10000 ps
22.950000000 ms
0 ms
5 ms
10 ms
15 ms
20 ms
25 ms
30 ms
35 ms
40 ms
45 ms
50 ms
00111...
00001...
00000...
00000...
01010...
01001...
01010...
01010011
10000 ps
X1: 22.950000000 ms
Default.wcfg
Console
ISim R.15xf (signature 0xc3576ebc)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
run all
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,303,612,865,000 ps
Type here to search
24°C
ENG IN
10:28 AM
10/25/2025