Boolean Algebra

Contents

Simplifying

De Morgan's Laws

$\wedge$ is the `AND` operator and $\vee$ is the `OR` operator.

Remember

$$\neg(A \vee B) \equiv \neg A \wedge \neg B$$
$$\neg(A \wedge B) \equiv \neg A \vee \neg B$$

$$X \wedge 0 = 0 \qquad X \wedge 1 = X$$
$$X \wedge X = X \qquad X \wedge \neg X = 0$$
$$X \vee 0 = X \qquad X \vee 1 = 1$$
$$X \vee X = X \qquad X \vee \neg X = 1$$
$$\neg\neg X = X$$

$\vee$ and $\wedge$ are commutative and associative with themselves.

$\wedge$ is distributive over $\vee$, so $X \wedge (Y \vee Z) = (X \wedge Y) \vee (X \wedge Z)$

Absorption

The absorption rules state that if you have different operators inside and outside of the bracket and the variable outside the bracket also appears inside the bracket, then the whole thing is the variable on the outside of the bracket.

Remember

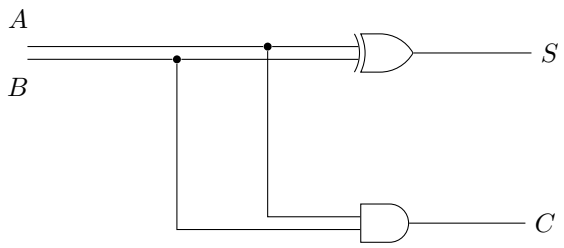
$$X \vee (X \wedge Y) = X$$
$$X \wedge (X \vee Y) = X$$

Karnaugh maps

IT WRAPS!

Flip flops

A half adder is $S = A \veebar B$, $C = A \wedge B$.



D-type

A rising edge D-type flip flop has two inputs: a clock signal and an input called D. It has two outputs: Q and $\neg Q$. When the clock pulse rises, Q is set to the value of D.

D-type flip flops are good for registers, static RAM, and CPU-internal cache. SRAM is faster and more expensive than regular dynamic RAM which must be periodically refreshed. SRAM is used for cache memory; DRAM is used for main memory.

SR-NOR-latch

NOR gates connected together with S and R inputs representing set and reset. The outputs are the opposite of each other. If both inputs are on, then both outputs are off (this is an undefined state). When one input is pulsed, its corresponding output (on the opposite side of this diagram) will remain on until the other input is pulsed, when the outputs will switch.