Ve370 Introduction to Computer Organization

Fall 2019

Instructor: Gang Zheng, Ph.D.
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Office Hours: W 4:00pm – 6:00pm / Th 10:00am – 12:00pm, or by appointment
Time: M 2:00 – 3:40pm (even weeks), T/Th 2:00 – 3:40pm
Classroom: D509 (M), D112 (Tu), C113 (Th)
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Course Description:
This course is designed to cover basic concepts of computer organization and hardware; instructions executed by a processor and how to use these instructions in simple assembly-language programs; stored-program concept; datapath and control for multiple implementations of a processor; performance evaluation, pipelining, caches, virtual memory, input/output, parallelism.

Credits: 4

Prerequisites*:* Ve270 and Ve280

Course Objectives (what will be taught):

1) To teach students how computers execute machine-level instructions.
2) To teach students how to write assembly language programs and translate them to machine level instructions.
3) To teach students how to design the datapath and control unit for pipelined and non-pipelined processors.
4) To teach students about data and control hazards.
5) To teach students the principles of caches and memory.
6) To teach students how processors, memory, and I/O are combined into a computer.

Course Outcomes (what students are expected to achieve):

1) Given a simple programming task and an instruction-set architecture, write an assembly language program that implements the task, translate the assembly-language program into machine-level instructions, and trace the execution of the program.
2) Model the computer hardware including datapath and control logic for a given instruction-set architecture, both for a single-cycle and pipelined processor, by using schematic capturing tools or hardware description languages (HDLs).
3) Be able to identify and resolve potential data, control, and structural hazards
4) Understand the memory hierarchy including cache, main memory, hard disk, and how data is stored in that hierarchical structure, and be able to recognize memory hits and misses

5) Understand the memory mapped I/O concept and how I/O devices interface the CPU
6) Be able to use library and internet resources for literature research to learn the current issues, technologies, and future development trends in computing

Textbook:

David Patterson and John Hennessy, *Computer Organization and Design - Hardware/Software Interface*, 4th edition, Morgan Kaufmann, 2008, ISBN 978-0-12-374493-7

Course Policies:

- **Honor Code:** All students in the class are bound by the Honor Code of the Joint Institute (see the related sections in JI *Student Handbook* for details). You may not seek to gain an unfair advantage over your fellow students; you may not consult, look at, or possess the unpublished work of another without their permission; and you must appropriately acknowledge your use of another's work.
- Attendance: Attendance will be randomly taken. 5% will be deducted from the final grade for each absence starting from the 4th one.
- Participation: Active participation in course meetings is expected for all students. With each submitted assignment, students should be prepared to explain their solutions to the class.
- Submission: Project reports are due on the specified date. The instructor reserves the right to waive the penalty for emergencies (e.g. hospitalization) or arrangement made with the instructor 24 hours prior to the due date.
- Individual Assignments: Project 1 and 4 and homework for literature search are individual assignments. Students are encouraged to discuss course topics and help each other understand the project/homework requirements better. However, all submissions must represent your own work. Duplicated submission is absolutely not allowed and will trigger an honor code violation investigation.
- Group Assignments: Project 2 and 3 are team efforts. The work submitted must reflect the work of the team. The grade for a group assignment will be shared among the entire team equally, unless specified differently.

Course Outline: (*Tentative and subject to adjustment.*)

Week	Date	Topics	Reading
1	9/10	Course Introduction, introduction to computer	1, Lecture Notes
	9/12	MIPS assembly, operations and operands	2.1-2.3, 2.6, 2.7
2	9/16	MIPS assembly, operations and operands	
	9/17	Function calls (Project 1)	2.8, 2.12-2.14, B.1-B.4
	9/19	Assembly programming	Handouts
3	9/24	Function calls (continue)	
	9/26	Instruction coding	2.5, 2.9, 2.10, B.10
4	9/30	Instruction coding (Project 1 due)	
	10/1	**National Holiday, no class**	
	10/3	**National Holiday, no class**	
5	10/8	Single cycle processor (Project2)	4.1-4.4
	10/10	Pipelined processor	4.5, 4.6

6	10/14	Data hazards	4.7
	10/15	Data hazards	
	10/17	Data hazards	
7	10/22	*Discussion / Lab*	
	10/24	**Midterm Exam**	
8	10/28	Control hazards	4.8
	10/29	Control hazards	
	10/31	Exceptions	4.9
9	11/5	*Discussion / Lab*	4.9
	11/7	Cache memory (Project 2 due)	5.1-5.3, 5.7
10	11/11	Cache memory (Project 3)	
	11/12	Cache memory	
	11/14	Lecture on literature search (Project 4)	handouts
11	11/19	Virtual memory, literature review	5.4-5.6, 5.10, 5.12
	11/21	Virtual memory (Project 3 due)	
12	11/25	Virtual memory,	
	11/26	I/Os and interfaces	6.1-6.6
	11/28	*Discussion*	
13	12/3	*Parallelism, multiprocessors*	7.1-7.4, 7.11, 9.1
	12/5	Review (Project 4 due)	
14	TBD	**Final Exam**	

Course Assessment Methods:

Homework:

Homework problems are designed for students to revisit and practice the important concepts in computer organization and design. Homework assignments are also assigned for students to gain confidence in solving engineering problems in this class. Tentatively, nine homework sets will be assigned. **Homework assignments will NOT be graded.** But homework problems may be discussed at the discussion sessions and solutions will be provided.

Homework for literature search:

The ability to search and find literatures relevant to a specific topic is important for conducting research, resolving real-life engineering problems, and continuing one's intellectual growth in the life time. The homework for literature search is designed for the students to get familiarized with the resources available in a college library physically and online virtually, and to learn tools that may facilitate the searching process.

Examination:

The examinations shall measure the ability to carry out analysis, design, and verification processes of digital circuits and systems. There will be two paper-based examinations. The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.

Project:

The projects are designed for students to practice the important concepts discussed in the lectures on a system level and to have a better understanding of the concepts and techniques with hands-on experience. The design projects utilize contemporary software tools in aid of design. Documented design outcomes and/or demonstration of the projects will be required.

Grading Policy:

Homework for literature search*	2%
Midterm Exam	30%
Final Exam	30%
Project 1*	5%
Project 2**	25%
Project 3**	5%
Project 4*	3%
Homework	*0%*
Total	**100%**

*Individual assignments
**Group assignments

Note: final letter grades may be curved.