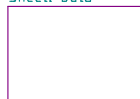


Sheet: Memory



File: Memory.sch

Sheet: Data



File: Data.sch

Sheet: Address Registers



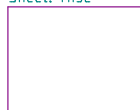
File: AddrRegs.sch

Sheet: Control



File: Control.sch

Sheet: Misc



File: Misc.sch

This is the FISC2 TTL CPU. Each one of the fivesheets on the left holds the main five sections of the design.

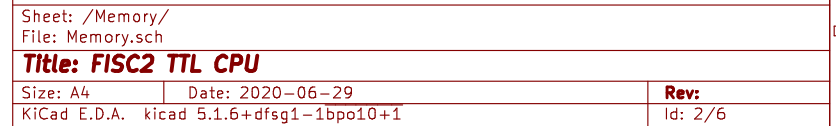
Sheet: /
File: FISC2.sch

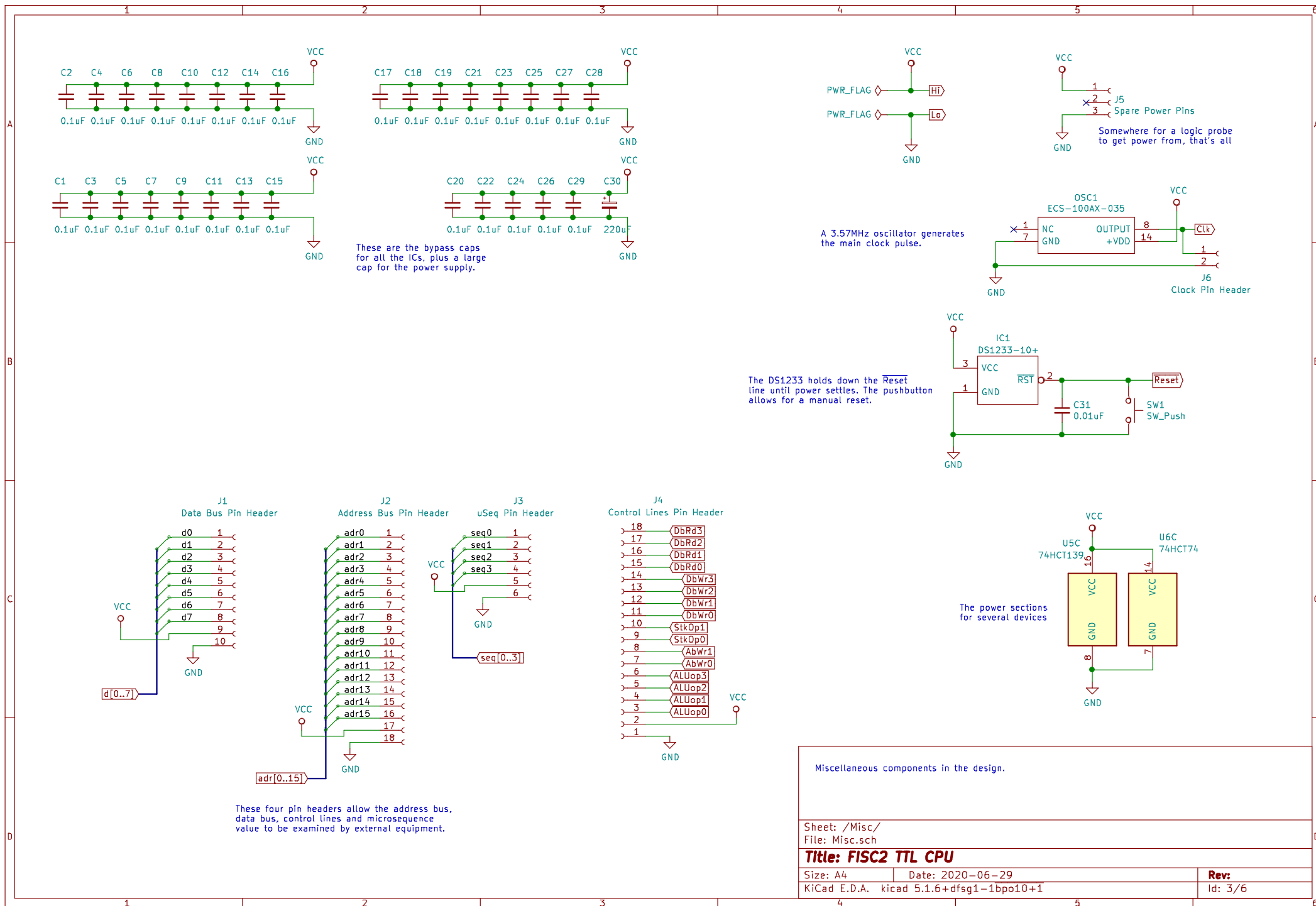
Title: FISC2 TTL CPU

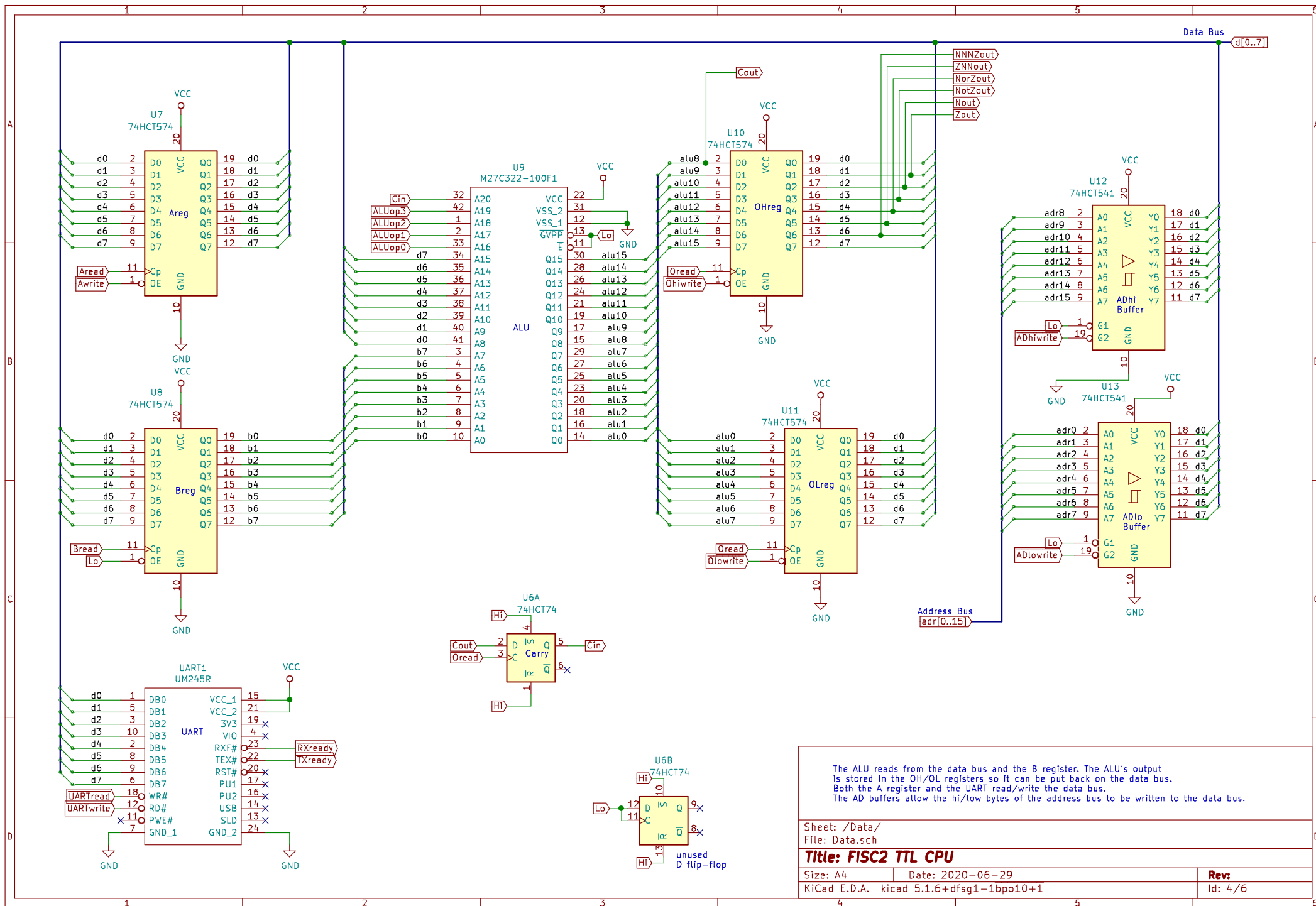
Size: A4 Date: 2020-06-29

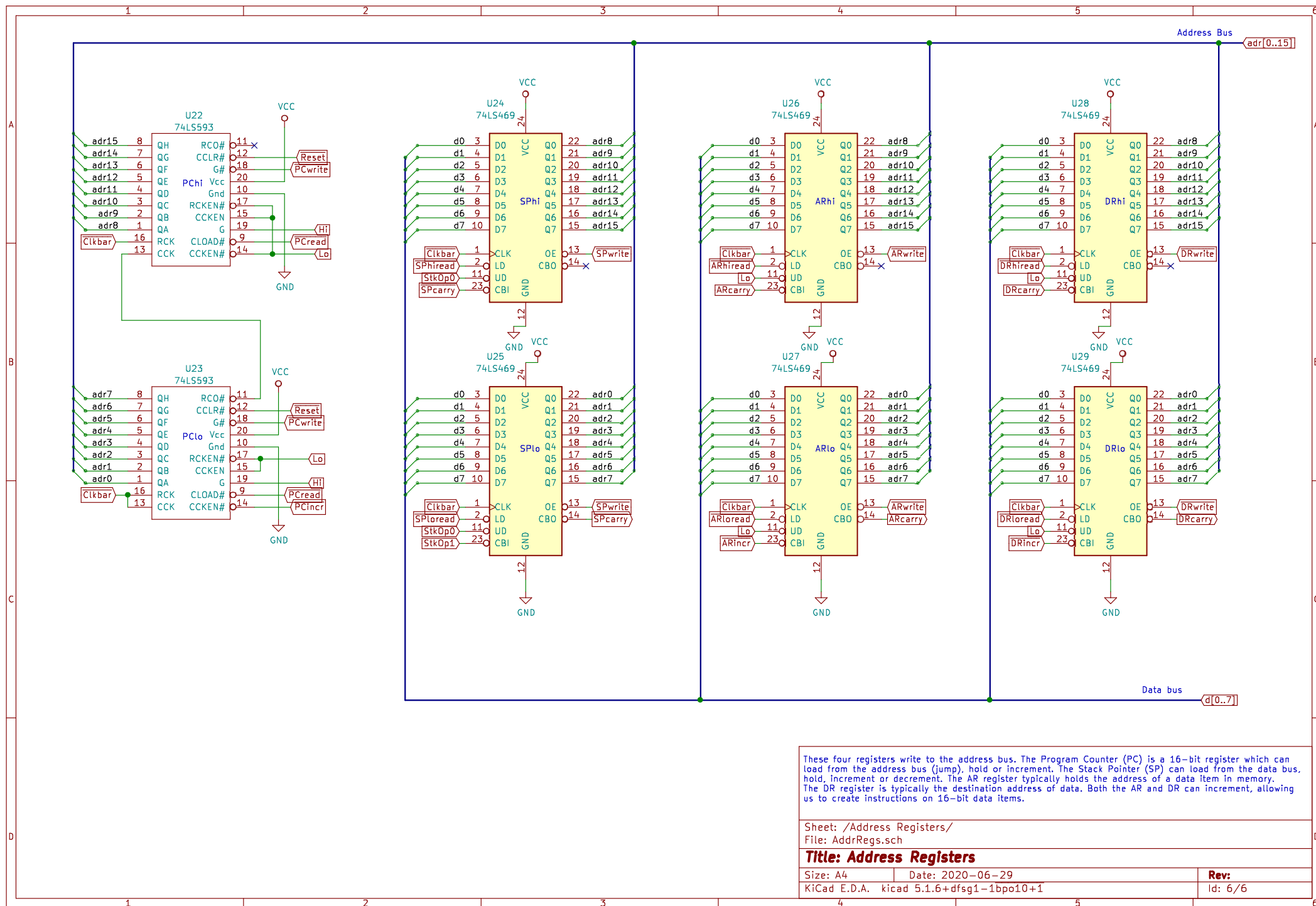
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Rev:
Id: 1/6









These four registers write to the address bus. The Program Counter (PC) is a 16-bit register which can load from the address bus (jump), hold or increment. The Stack Pointer (SP) can load from the data bus, hold, increment or decrement. The AR register typically holds the address of a data item in memory. The DR register is typically the destination address of data. Both the AR and DR can increment, allowing us to create instructions on 16-bit data items.

Sheet: /Address Registers/
File: AddrRegs.sch

Title: Address Registers

Size: A4 Date: 2020-06-29

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Rev:

Id: 6/6