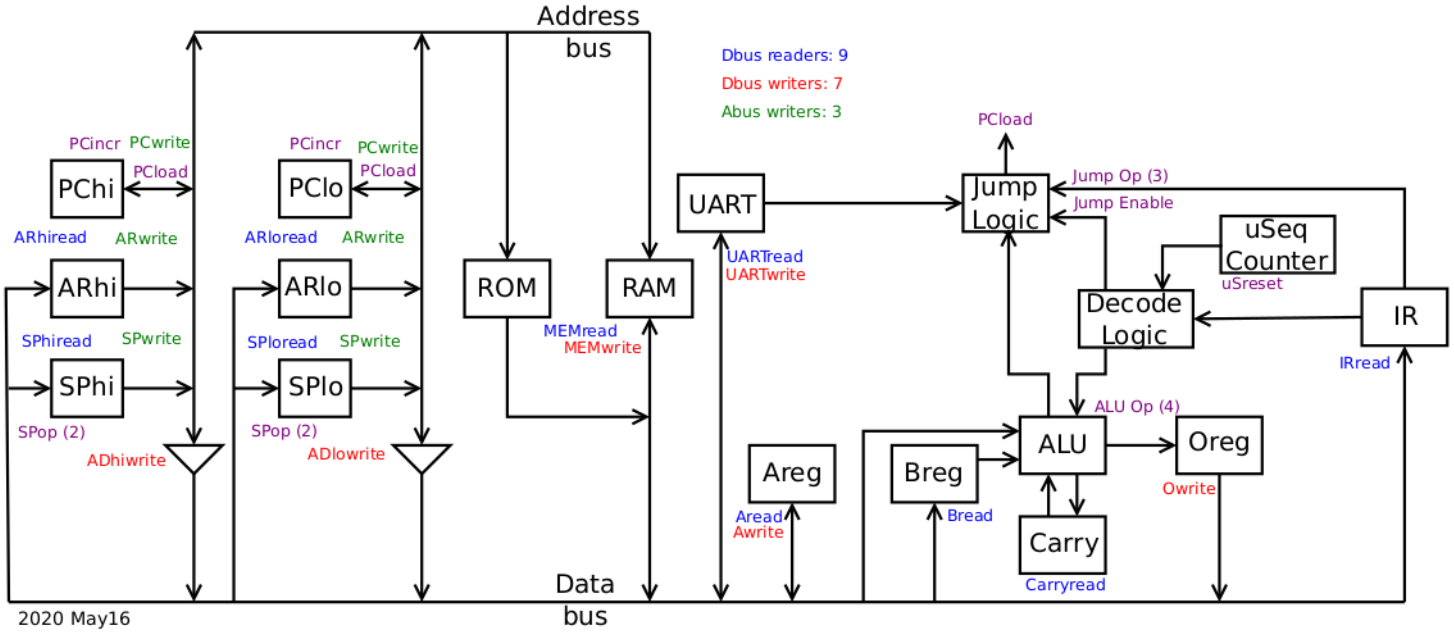


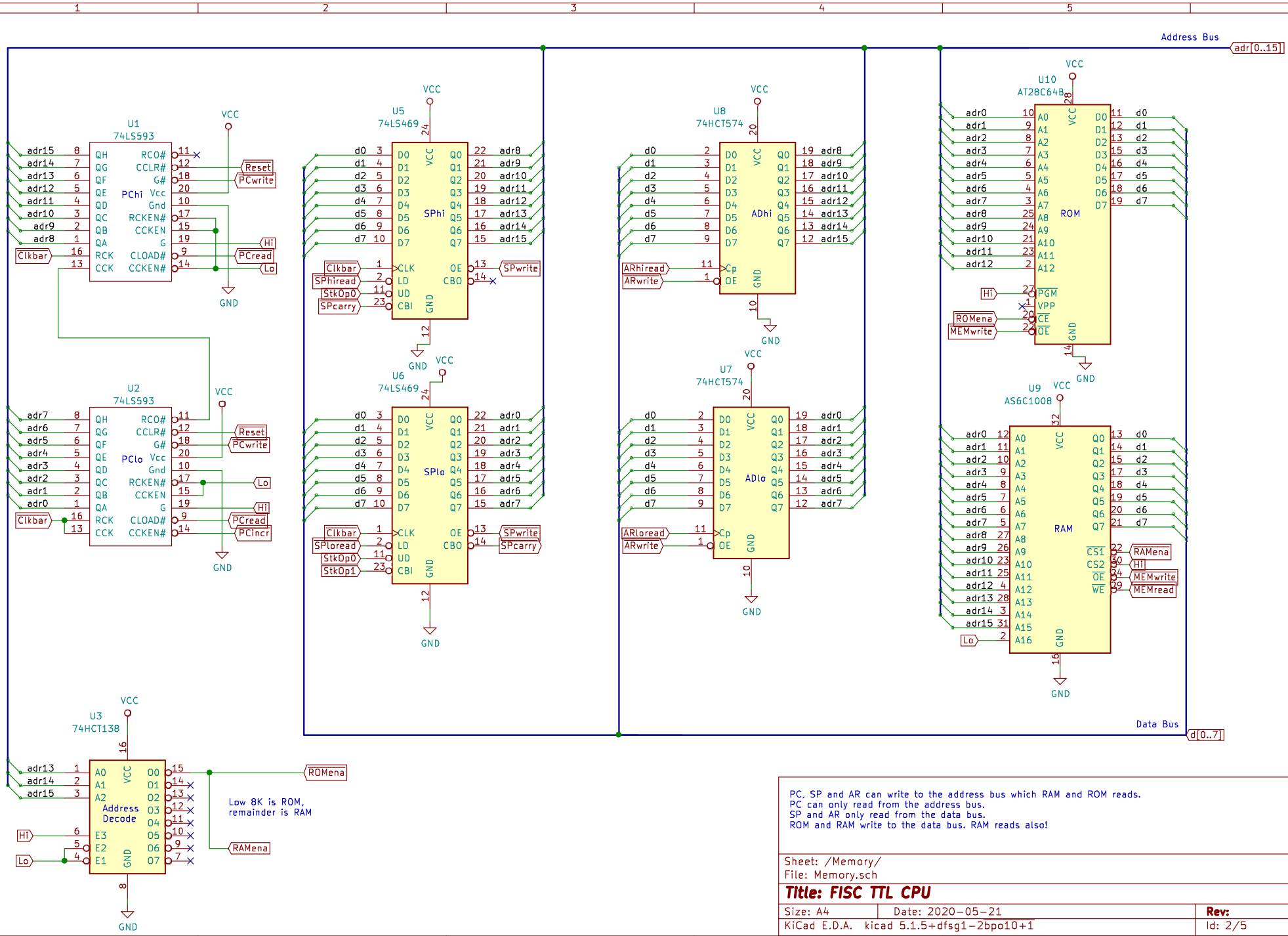
Sheet: Memory
File: Memory.sch

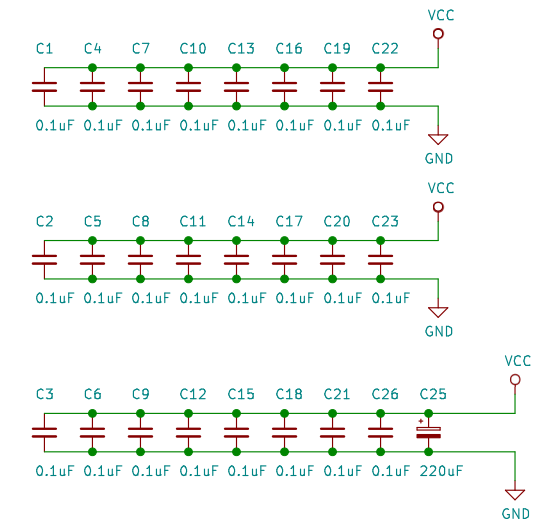
Sheet: Data
File: Data.sch

Sheet: Misc
File: Misc.sch

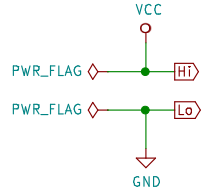
Sheet: Control
File: Control.sch

This is the FISC TTL CPU. Each one of the four sheets on the left holds the main four sections of the design.

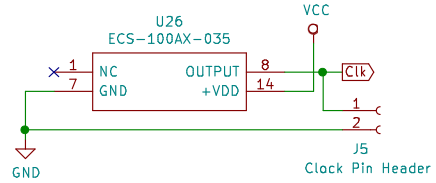

Address Bus
adr[0..15]
Data Bus
d[0..7]
U1
74LS593
U2
74LS593
U3
74HCT138
Address Decode
U5
74LS469
SPhi
U6
74LS469
SPlo
U8
74HCT574
ADhi
U7
74HCT574
ADlo
U10
AT28C64B
ROM
U9
AS6C1008
RAM
VCC
GND
Reset
PCwrite
PCread
PCincr
Hi
Lo
Clkbar
SPhiread
SPloread
SPwrite
SPcarry
ARhiread
ARloread
ARwrite
StkOp0
StkOp1
ROMena
RAMena
MEMwrite
MEMread
Low 8K is ROM,
remainder is RAM
PC, SP and AR can write to the address bus which RAM and ROM reads.
PC can only read from the address bus.
SP and AR only read from the data bus.
ROM and RAM write to the data bus. RAM reads also!
Sheet: /Memory/
File: Memory.sch
Title: FISC TTL CPU
Size: A4
Date: 2020-05-21
Rev:
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 2/5

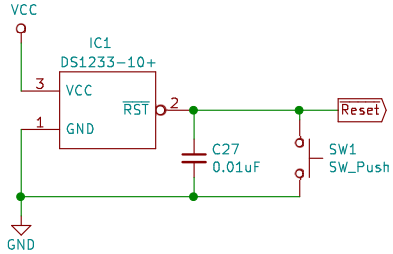


These are the bypass caps for all the ICs, plus a large cap for the power supply.

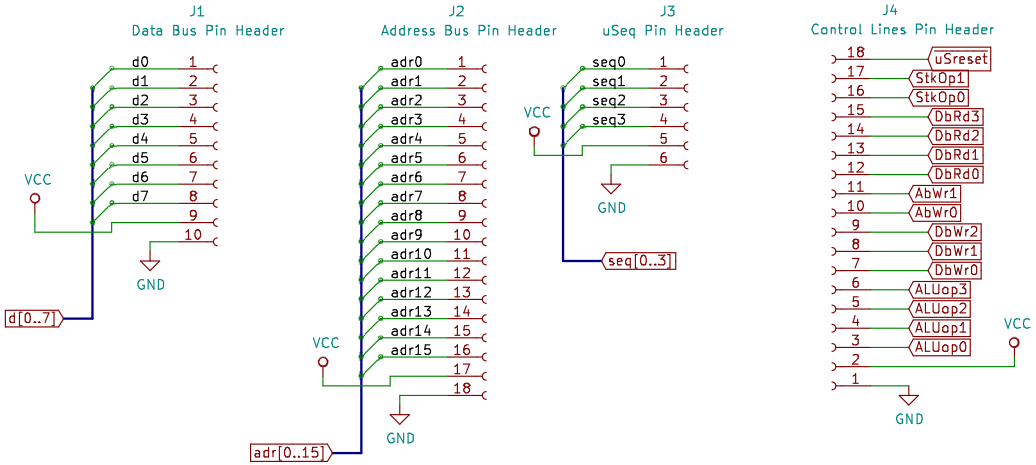


A 3.57MHz oscillator generates the main clock pulse.

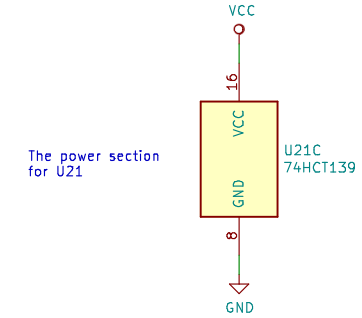




The DS1233 holds down the Reset line until power settles. The pushbutton allows for a manual reset.



These three pin headers allow the address bus, data bus and microsequence value to be examined by external equipment.



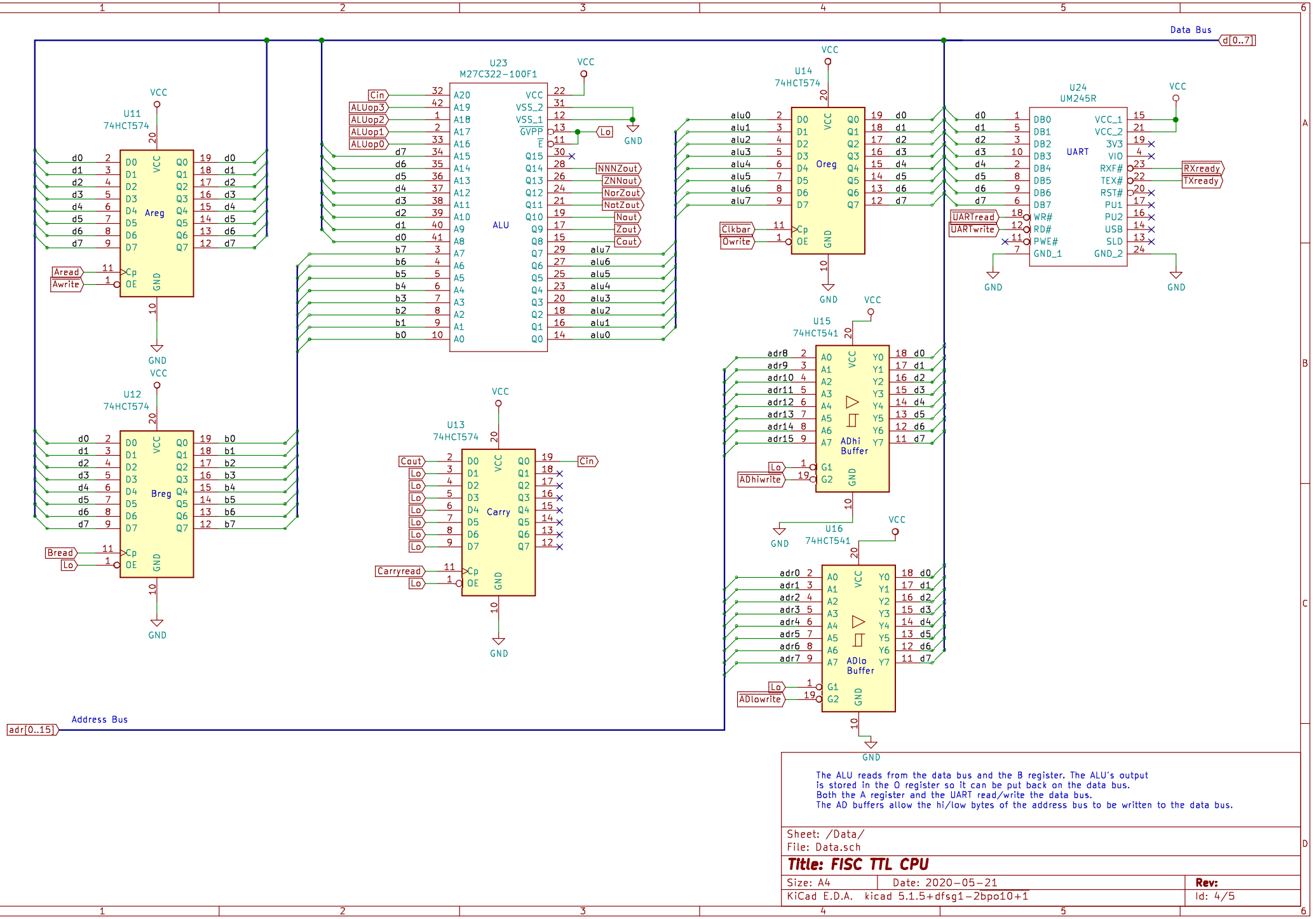
The power section for U21

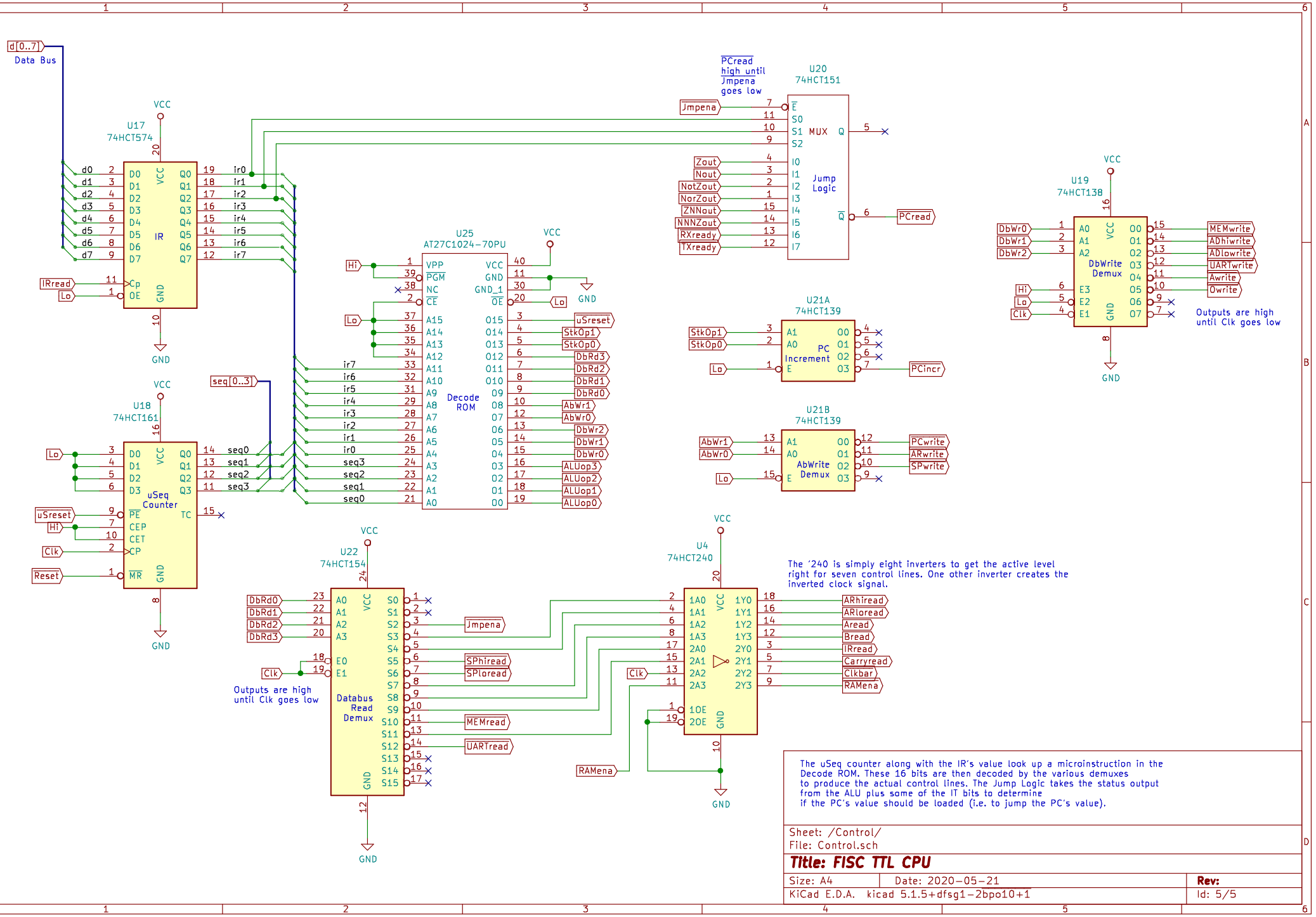
Miscellaneous components in the design.

Sheet: /Misc/
File: Misc.sch

Title: FISC TTL CPU

Size: A4	Date: 2020-05-21	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 3/5


Data Bus
d[0..7]
Address Bus
adr[0..15]
U11
74HCT574
Areg
U12
74HCT574
Breg
U13
74HCT574
Carry
U23
M27C322-100F1
ALU
U14
74HCT574
Oreg
U15
74HCT541
ADhi Buffer
U16
74HCT541
ADlo Buffer
U24
UM245R
UART
VCC
GND
Aread
Awrite
Bread
Carryread
Clkbar
Owrite
ADhiwrite
ADlowrite
UARTread
UARTwrite
RXready
TXready
Cin
Cout
Zout
Nout
NNNZout
ZNNout
NorZout
NotZout
ALUop0
ALUop1
ALUop2
ALUop3
The ALU reads from the data bus and the B register. The ALU's output
is stored in the O register so it can be put back on the data bus.
Both the A register and the UART read/write the data bus.
The AD buffers allow the hi/low bytes of the address bus to be written to the data bus.
Sheet: /Data/
File: Data.sch
Title: FISC TTL CPU
Size: A4
Date: 2020-05-21
Rev:
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 4/5


d[0..7]
Data Bus
U17
74HCT574
IR
IRread
U18
74HCT161
uSeq
Counter
uSreset
Reset
U25
AT27C1024-70PU
Decode
ROM
seq[0..3]
U20
74HCT151
PCread
high until
Jmpena
goes low
Jump
Logic
U21A
74HCT139
PC
Increment
PCincr
U21B
AbWrite
Demux
PCwrite
ARwrite
SPwrite
U19
74HCT138
DbWrite
Demux
MEMwrite
ADhiwrite
ADlowrite
UARTwrite
Awrite
Owrite
Outputs are high
until Clk goes low
U22
74HCT154
Databus
Read
Demux
Outputs are high
until Clk goes low
U4
74HCT240
The '240 is simply eight inverters to get the active level
right for seven control lines. One other inverter creates the
inverted clock signal.
The uSeq counter along with the IR's value look up a microinstruction in the
Decode ROM. These 16 bits are then decoded by the various demuxes
to produce the actual control lines. The Jump Logic takes the status output
from the ALU plus some of the IT bits to determine
if the PC's value should be loaded (i.e. to jump the PC's value).
Sheet: /Control/
File: Control.sch
Title: FISC TTL CPU
Size: A4
Date: 2020-05-21
Rev:
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 5/5