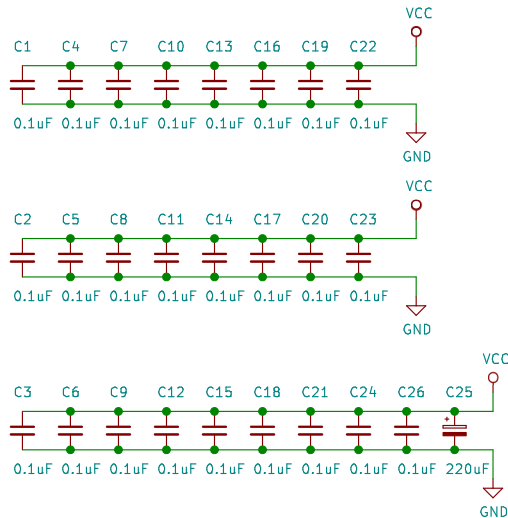
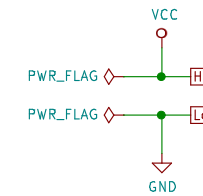


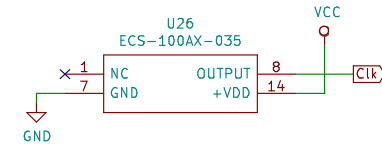
PC, SP and AR can write to the address bus which RAM and ROM reads.
 PC can only read from the address bus.
 SP and AR only read from the data bus.
 ROM and RAM write to the data bus. RAM reads also!



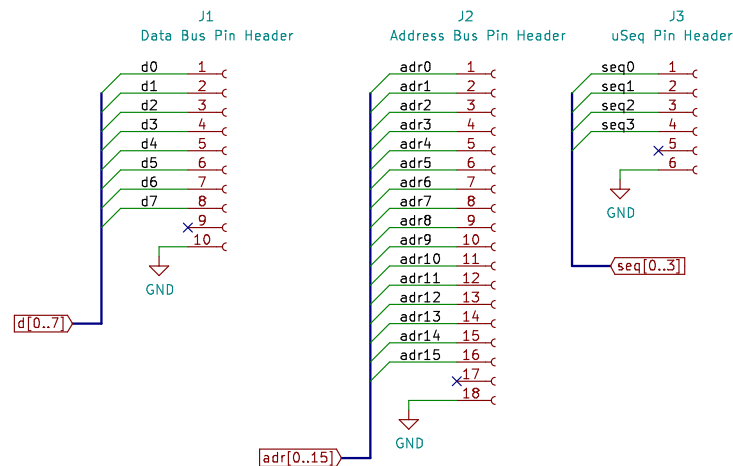
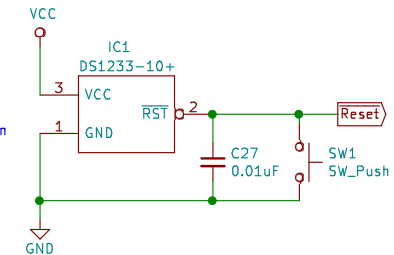
These are the bypass caps for all the ICs, plus a large cap for the power supply.



A 3.57MHz oscillator generates the main clock pulse.

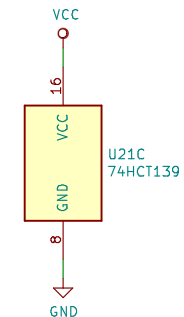


The DS1233 holds down the Reset line until power settles. The pushbutton allows for a manual reset.



These three pin headers allow the address bus, data bus and microsequence value to be examined by external equipment.

The power section for U21



Miscellaneous components in the design.

Sheet: /Misc/
File: Misc.sch

Title:

Size: A4

Date:

KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1

Rev:

Id: 3/5

