Interconnection Network

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//Module for machine a
module amodule(input binput,output reg boutput);
        //Whenever b sends an input, the output boutput is generated which is later printed in the testbench along with the timestamp
        always@(binput) begin
                boutput=binput;
        end
endmodule
//Module for machine b
module bmodule(input ainput,output reg aoutput);
        //Whenever a sends an input, the output aoutput is generated which is later printed in the testbench along with the timestamp
        always@(ainput) begin
                aoutput=ainput;
        end
endmodule
```

Machine A sends message to machine B and vice versa, periodically. Each of the machine prints the received message with the time stamp

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`timescale 1ns/100ps
module testbench;
        // inputs
        reg ainput;
        reg binput;
        //outputs
        wire aoutput;
        wire boutput;

        integer i;
        // amodule is the machine a, where binput is the input given by b and boutput is the corresponding output generated
        amodule inst1 (binput,boutput);
        // bmodule is the machine b, where ainput is the input given by a and aoutput is the corresponding output generated
        bmodule inst2 (ainput,aoutput);

        initial begin
                $dumpfile("network.vcd");
                $dumpvars(0, testbench);
                ainput=1'b1;
                binput=1'b0;
                for(i=1;i<=5;i=i+1) begin
                        // ainput is varied with time
                        #10 ainput=~ainput;
                        // displaying the output
                                #0 $display("Time=%3d Ainput=%d Aoutput=%d",$time,ainput,aoutput);
                        // binput is varied with time
                        #20 binput=~binput;
                        // displaying the output
                                #0 $display("Time=%3d Binput=%d Boutput=%d",$time,binput,boutput);

                end
        end
endmodule
```

Loading file '/home/dibyadarshan/Desktop/Logisim and verilog/Assignment1COA/Q6/6a/t_network.v'...   Verilog ▼ Tab Width: 8 ▼   Ln 1, Col 1   ▾   INS

The time is printed using $time function