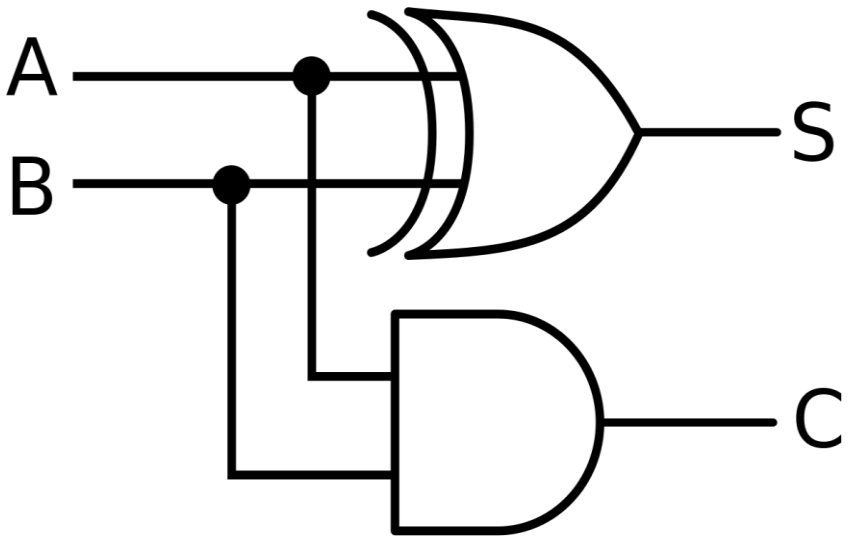
Half Adder

Adds two 1 bit quantities to give corresponding sum and carry outputs

Truth table:

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Block Diagram:



Verilog code:

```
module halfAdder (output reg sum, output reg carry, input op1, input op2);

    // thread for half adder operations
    always @ (op1 or op2) begin

        // sum bit of two operands
        sum = op1 ^ op2;
        // carry bit of two operands
        carry = op1 & op2;

    end

endmodule
```

Explanation:

Using data flow modelling the above block diagram is coded in the module.