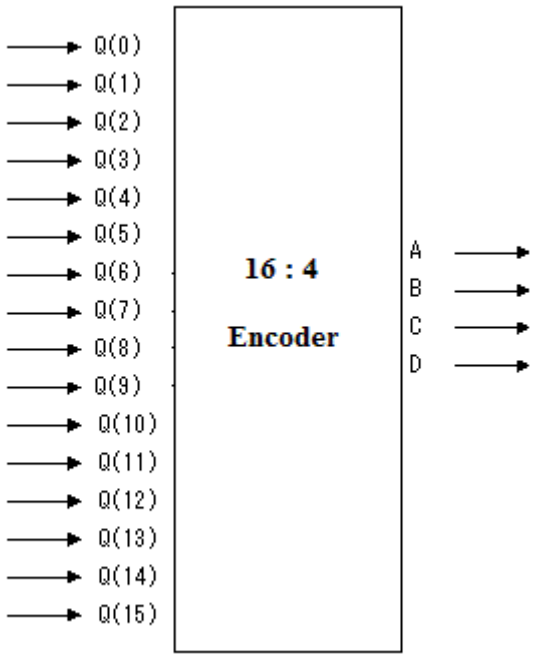
Encoder

15 bit input indicating decimal value is encoded to give corresponding 4 bit binary value

Truth table:

OUTPUTS				INPUTS															
A	B	C	D	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{10}	X_{11}	X_{12}	X_{13}	X_{14}	X_{15}
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Block Diagram:



Verilog code:

```
module encoder (output reg [0:3] out, input [0:15] in);

    // thread to decode input
    always @ (in) begin
        // check which input and give corresponding output
        case (in)
            16'b0000000000000001 : out = 4'b0000;
            16'b0000000000000010 : out = 4'b0001;
            16'b0000000000000100 : out = 4'b0010;
            16'b0000000000001000 : out = 4'b0011;
            16'b0000000000010000 : out = 4'b0100;
            16'b0000000000100000 : out = 4'b0101;
            16'b0000000001000000 : out = 4'b0110;
            16'b0000000010000000 : out = 4'b0111;
            16'b0000000100000000 : out = 4'b1000;
            16'b0000001000000000 : out = 4'b1001;
            16'b0000010000000000 : out = 4'b1010;
            16'b0000100000000000 : out = 4'b1011;
            16'b0001000000000000 : out = 4'b1100;
            16'b0010000000000000 : out = 4'b1101;
            16'b0100000000000000 : out = 4'b1110;
            16'b1000000000000000 : out = 4'b1111;
            default: out = 4'bxxxx;
        endcase

    end


endmodule
```

Explanation:

Using behavioral modelling the behaviour of the circuit is coded using switch cases for the in variable giving corresponding out variable values.