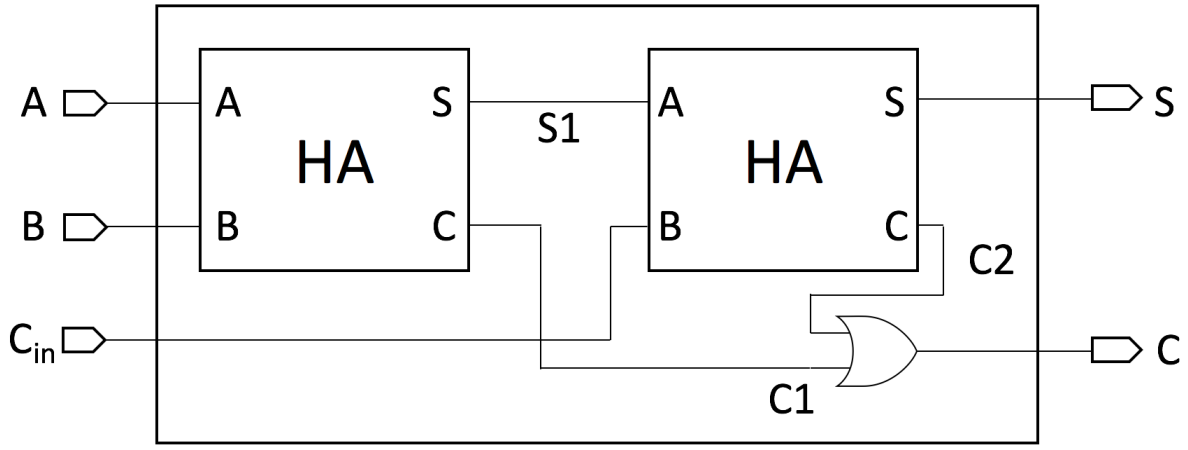
Full Adder

Adds three 1 bit quantities to give corresponding sum and carry outputs

Truth table:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Block Diagram:



Verilog code:

```
module fullAdder (output sum, output carry, input op1, input op2,input op3);

    wire isum,i1carry,i2carry;
    // thread for full adder operations
    //'i' stands for intermediate

        // using half adder the first time
        halfAdder inst1 (isum,i1carry,op1,op2);
        // calculating the sum
        halfAdder inst2 (sum,i2carry,isum,op3);
        // calculating the carry
        assign carry = i1carry|i2carry;


endmodule
```

Explanation:

Using data flow modelling the above block diagram is coded in the full adder module using two half adder modules.