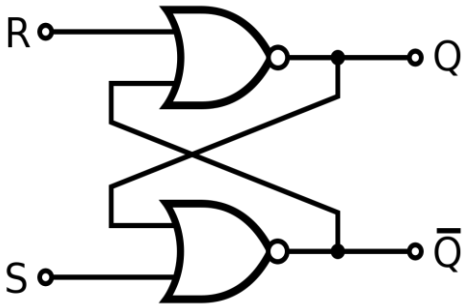
1 bit Memory Element

Uses D flip flop to store 1 bit data in memory.

Construction:

RS Latch:

1. Block Diagram:

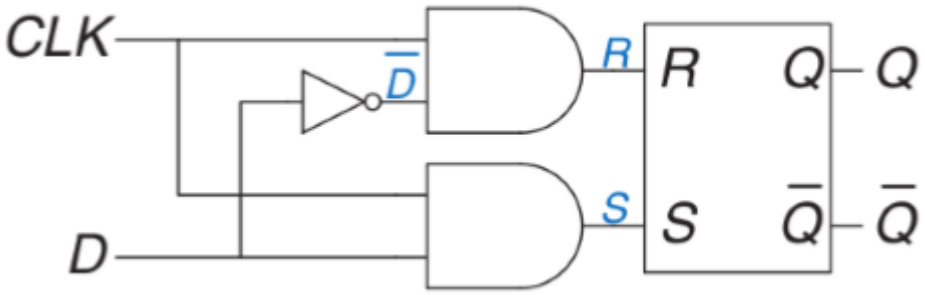


2. Verilog Code:

```
module RSl (output reg q, output reg qn, input r, input s);

    // rs latch modeling
    always @(q, qn, r, s) begin
        q <= ~ (qn | r);
        qn <= ~ (q | s);

    end

endmodule
```

D Latch using RS Latch:

1. Block Diagram:

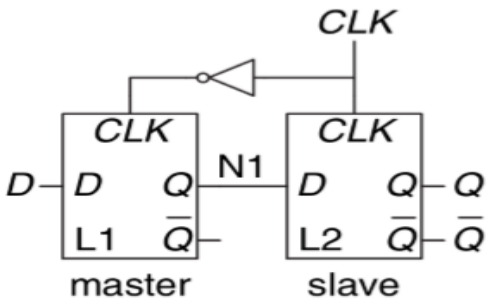


2. Verilog Code:

```
module Dl (output q, output qn, input d, input clk);

    reg r, s;

    // using rs latch module
    RSl RSlinstDl (q, qn, r, s);

    // d latch modelling
    always @ (r, s, d, clk) begin
        r <= (~ d) & clk;
        s <= d & clk;
    end


endmodule
```

D flip-flop using master slave D Latch:

1. Block Diagram:



2. Verilog Code:

```
module Dff (output q, output  qn, input d, input clk, input res);

    reg nclk;
    wire qi, qni;

    // active low reset signal
    wire new_d;
    assign new_d = d & res;

    // D latch 1
    Dl inst1 (qi, qni, new_d, nclk);
    // D latch 2
    Dl inst2 (q, qn, qi, clk);

    // complement of clock
    always @ (clk) begin
        nclk <= ~clk;
    end

endmodule
```

Explanation:

Using the above block diagrams each module is coded and used as blocks in other modules.

It helps to store 1 bit data in memory along with a active low reset signal. The master slave configuration allows the sequential circuit to be positive edge triggered.