



1. Description

1.1. Project

Project Name	STM32F746G_DISCO
Board Name	custom
Generated with:	STM32CubeMX 6.1.0
Date	11/30/2020

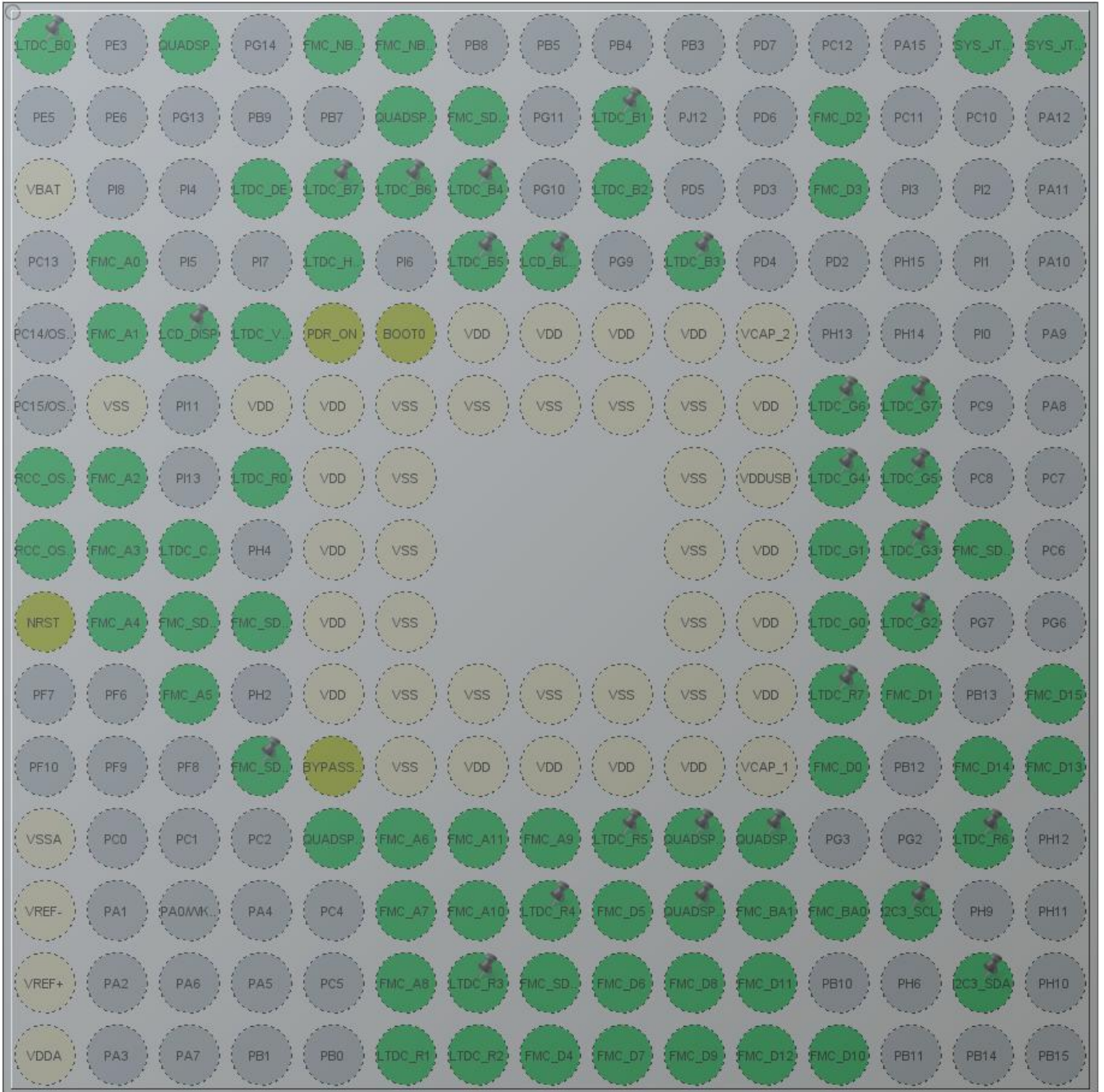
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration



TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4	I/O	LTDC_B0	
A3	PE2	I/O	QUADSPI_BK1_IO2	
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B6	PB6	I/O	QUADSPI_BK1_NCS	
B7	PG15	I/O	FMC_SDNCAS	
B9	PJ13	I/O	LTDC_B1	
B12	PD0	I/O	FMC_D2	
C1	VBAT	Power		
C4	PK7	I/O	LTDC_DE	
C5	PK6	I/O	LTDC_B7	
C6	PK5	I/O	LTDC_B6	
C7	PG12	I/O	LTDC_B4	
C9	PJ14	I/O	LTDC_B2	
C12	PD1	I/O	FMC_D3	
D2	PF0	I/O	FMC_A0	
D5	PI10	I/O	LTDC_HSYNC	
D7	PK4	I/O	LTDC_B5	
D8	PK3 *	I/O	GPIO_Output	LCD_BL_CTRL
D10	PJ15	I/O	LTDC_B3	
E2	PF1	I/O	FMC_A1	
E3	PI12 *	I/O	GPIO_Output	LCD_DISP
E4	PI9	I/O	LTDC_VSYNC	
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		

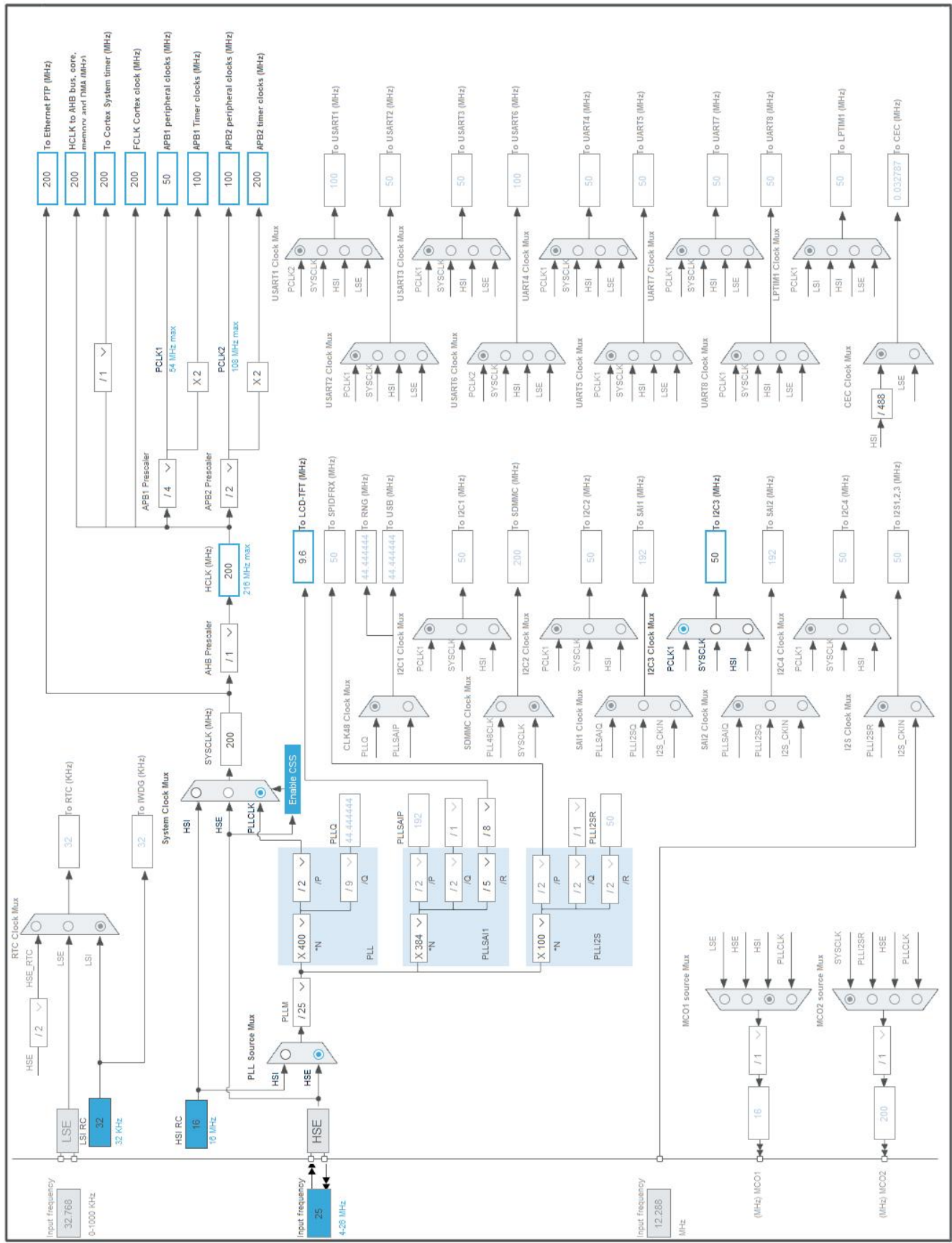
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	PK1	I/O	LTDC_G6	
F13	PK2	I/O	LTDC_G7	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G4	PI15	I/O	LTDC_R0	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	PJ11	I/O	LTDC_G4	
G13	PK0	I/O	LTDC_G5	
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	
H3	PI14	I/O	LTDC_CLK	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power		
H12	PJ8	I/O	LTDC_G1	
H13	PJ10	I/O	LTDC_G3	
H14	PG8	I/O	FMC_SDCLK	
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	
J3	PH5	I/O	FMC_SDNWE	
J4	PH3	I/O	FMC_SDNE0	
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	PJ7	I/O	LTDC_G0	
J13	PJ9	I/O	LTDC_G2	
K3	PF5	I/O	FMC_A5	
K5	VDD	Power		
K6	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	PJ6	I/O	LTDC_R7	
K13	PD15	I/O	FMC_D1	
K15	PD10	I/O	FMC_D15	
L4	PC3	I/O	FMC_SDCKE0	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M5	PB2	I/O	QUADSPI_CLK	
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	
M9	PJ4	I/O	LTDC_R5	
M10	PD12	I/O	QUADSPI_BK1_IO1	
M11	PD13	I/O	QUADSPI_BK1_IO3	
M14	PJ5	I/O	LTDC_R6	
N1	VREF-	Power		
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N8	PJ3	I/O	LTDC_R4	
N9	PE8	I/O	FMC_D5	
N10	PD11	I/O	QUADSPI_BK1_IO0	
N11	PG5	I/O	FMC_BA1	
N12	PG4	I/O	FMC_BA0	
N13	PH7	I/O	I2C3_SCL	
P1	VREF+	Power		
P6	PF14	I/O	FMC_A8	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P7	PJ2	I/O	LTDC_R3	
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
P14	PH8	I/O	I2C3_SDA	
R1	VDDA	Power		
R6	PJ0	I/O	LTDC_R1	
R7	PJ1	I/O	LTDC_R2	
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32F746G_DISCO
Project Folder	C:\TouchGFXProjects\Lab_HW3
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0xA00
Minimum Stack Size	0xA00

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_CRC_Init	CRC
4	MX_DMA2D_Init	DMA2D
5	MX_FMC_Init	FMC
6	MX_I2C3_Init	I2C3
7	MX_LTDC_Init	LTDC
8	MX_QUADSPI_Init	QUADSPI

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746NGHx
Datasheet	DS10916_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

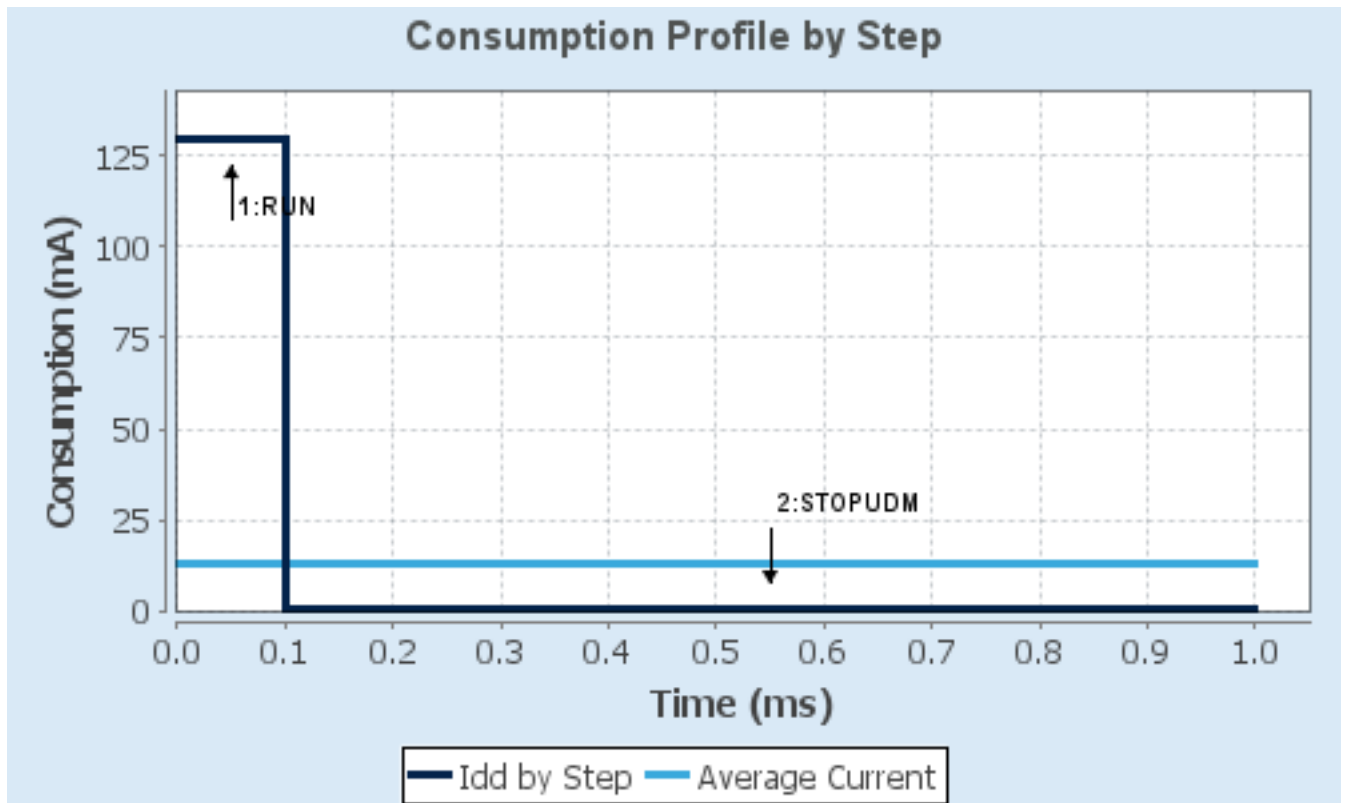
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 μ A
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	92.56	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCELERATOR	Enabled *
Instruction Prefetch	Enabled *
CPU ICache	Enabled *
CPU DCache	Enabled *

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers *
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Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Enabled *
MPU Region Base Address	0x90000000 *
MPU Region Size	256MB *
MPU SubRegion Disable	0x0 *
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS PERMITTED *
MPU Instruction Access	ENABLE
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Enabled *
MPU Region Base Address	0x90000000 *
MPU Region Size	16MB *
MPU SubRegion Disable	0x0 *
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS PERMITTED *
MPU Instruction Access	ENABLE
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	ENABLE *
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

7.2. CRC

mode: Activated

7.2.1. Parameter Settings:

Basic Parameters:

Default Polynomial State Enable

Default Init Value State Enable

Advanced Parameters:

Input Data Inversion Mode None

Output Data Inversion Mode Disable

Input Data Format Bytes

7.3. DMA2D

mode: Activated

7.3.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0
DMA2D Bytes Swap	Bytes in regular order in output FIFO
DMA2D Line Offset Mode	Line offsets expressed in pixels

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

7.4. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

7.4.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	3 memory clock cycles *
Write protection	Disabled
SDRAM common clock	2 HCLK clock cycles *
SDRAM common burst read	Enabled *
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	2 *
Exit self-refresh delay	7 *
Self-refresh time	4 *
SDRAM common row cycle delay	7 *
Write recovery time	3 *
SDRAM common row precharge delay	2 *
Row to column delay	2 *

7.5. I2C3

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00C0EAF *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. LTDC

Display Type: RGB888 (24 bits)

7.6.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	41 *
Horizontal Back Porch	13 *
Active Width	480 *
Horizontal Front Porch	32 *

HSync Width	40
Accumulated Horizontal Back Porch Width	53
Accumulated Active Width	533
Total Width	565

Synchronization for Height:

Vertical Synchronization Height	10 *
Vertical Back Porch	2
Active Height	272 *
Vertical Front Porch	2
VSynC Height	9
Accumulated Vertical Back Porch Height	11
Accumulated Active Height	283
Total Height	285

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.6.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers	1 layer *
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Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	480 *
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	272 *

Pixel Parameters:

Layer 0 - Pixel Format	RGB565 *
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Blending:

Layer 0 - Alpha constant for blending	
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	255 *
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Frame Buffer:	
Layer 0 - Color Frame Buffer Start Address	0xC0000000 *
Layer 0 - Color Frame Buffer Line Length (Image Width)	480 *
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	272 *

7.7. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.7.1. Parameter Settings:

General Parameters:

Clock Prescaler	1 *
Fifo Threshold	4 *
Sample Shifting	Sample Shifting Half Cycle *
Flash Size	24 *
Chip Select High Time	6 Cycles *
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.9. SYS

Debug: Serial Wire

Timebase Source: TIM6

7.10. FREERTOS

Interface: CMSIS_V1

7.10.1. Config parameters:

API:

FreeRTOS API	CMSIS v1
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Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled *
USE_COUNTING_SEMAPHORES	Enabled *
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Enabled *
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

RECORD_STACK_HIGH_ADDRESS Disabled

Memory management settings:

Memory Allocation **Dynamic ***
TOTAL_HEAP_SIZE **65536 ***
Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK **Enabled ***
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Disabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled
MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t
USE_POSIX_ERRNO Disabled

7.10.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled
uxTaskPriorityGet Enabled
vTaskDelete Enabled
vTaskCleanUpResources Disabled
vTaskSuspend Enabled
vTaskDelayUntil Disabled
vTaskDelay Enabled
xTaskGetSchedulerState Enabled
xTaskResumeFromISR Enabled
xQueueGetMutexHolder Disabled

xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.10.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled
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Project settings (see parameter description first):

Use FW pack heap file	Enabled
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* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PH8	I2C3_SDA	Alternate Function Open Drain	Pull-up	Very High *	
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ11	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ9	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ3	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ2	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB6	QUADSPI_BK1_ NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PD12	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD13	QUADSPI_BK1_I O3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD11	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
RCC	PH0/OSC_I N	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
GPIO	PK3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL_CTRL
	PI12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DISP

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
LTDC global interrupt	true	5	0
DMA2D global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FMC global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
LTDC global error interrupt	unused		
QUADSPI global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
LTDC global interrupt	false	true	true
DMA2D global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00166116.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00124865.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00145382.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164549.pdf
Application note	http://www.st.com/resource/en/application_note/DM00173083.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210367.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note http://www.st.com/resource/en/application_note/DM00340311.pdf
Application note http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note http://www.st.com/resource/en/application_note/DM00600614.pdf